DIGITAL EXPANSION SYSTEM FOR ASTRAC I

by

Harry R. Eckes

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SIGNED: Harry R Ecker

APPROVAL BY THESIS DIRECTOR

This thesis has been approved on the date shown below:

G. A. Korn
G. A. Korn
Professor of Electrical Engineering

4/29/63
Date

ABSTRACT

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This report presents the design and application of a digital expansion system for the Arizona Statistical Repetitive Analog Computer (ASTRAC I).

The system is composed of two modules which are made up of three operational amplifiers, two bistable multivibrators, two Schmitt triggers, two inverting/differentiating amplifiers, and a number of plug-in electronic switches and diodes for assembling digital gate circuits.

The digital-expansion modules give ASTRAC I additional decision-making capacity and aid in the study of optimal-system design, sampled-data systems, correlation-function estimation, and nonlinear system simulation, to name only a few applications.

Optimization-type solution of a boundary value problem, simulation of a point mass striking a reflecting frictionless surface, and estimation of correlation functions are presented as examples of applications for the digital system.

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CHAPTER I

INTRODUCTION

Modern electronic analog computation has evolved the high-speed repetitive analog computer with associated equipment which permits studies in many diversified fields. The Arizona Statistical Repetitive Analog Computer (ASTRAC I) combines modern high speed analog computation with digital logic and control. This report describes the development and application of a digital expansion system which extends the capabilities of ASTRAC I.

1.1 ASTRAC I¹

The Arizona Statistical Repetitive Analog computer (ASTRAC I) (Fig. 1.1) combines a new memory-equipped repetitive analog computer with digital logic and control. The resulting synthesis of high-speed analog computation with digital automatic programming is of particular interest in connection with Monte-Carlo-type studies of random processes^{2,3}, which serve to illustrate ASTRAC system operation in Figure 1.2.

Referring to Fig. 1.2, an analog-computer simulated control system, communications system queuing problem, etc. is supplied random inputs, initial conditions, or parameters from noise generators with Gaussian or random-impulse output. Reset pulses from a simple digital control unit cause repetitive simulation⁴ of the process under study between 10 and 100 times per second. Accurate sample-hold (analog memory) units read selected process variables at push-button preset times t_1, t_2

Fig. 1.1 Arizona Statistical Repetitive Analog Computer (ASTRAC I)
Analog/Hybrid Computer Laboratory, University of Arizona, Tucson,
Arizona.

Fig. 1.2 ASTRAC I Operation for Random-Process Studies. This figure based on reference 1.

after the start of each repetitive computer run. A hybrid analog/digital statistics computer accepts these samples to compute statistical averages over 100 to 10,000 computer runs, as determined by a preset run counter in the control unit. In this manner one can estimate ensemble averages such as mean-square delay error, correlation functions, and probabilities for very complicated nonstationary as well as stationary random processes.

Each of the six analog modules in ASTRAC I comprises two summers, two electronically controlled integrator memory amplifiers, and one analog comparator.

In addition to these amplifier modules ASTRAC I comprises an Amplitude-distribution Analyzer⁵, Statistics (averaging) computer⁶, Sample-hold Module⁷, Random-noise Generator⁸, Pseudo-random-noise Generator⁹, Multipliers, Function Generators, a digital expansion system, and a digital control unit¹⁰. There is also various recording and read out equipment.

1.2 DIGITAL EXPANSION SYSTEM

An electronic analog computer equipped with accurate memory circuits, decision-making comparators, and analog switches can tackle a whole new field of combined analog/digital computing techniques, including automatic program changes, iterative sub-routines, multiplexing of difference-differential equation setups for partial differential equations, simulation of sampled-data or digital systems, and automatic parameter optimization^{11,12,13}. ASTRAC I combines these features with provisions for digital as well as analog control of integrators, memory units, and analog switches by means of a simple all-digital control

unit and a digital expansion system (Fig. 1.3).

The block diagram representation (Fig. 1.4) illustrates how the digital expansion system ties in with ASTRAC I.

The digital expansion system uses bistable computer elements, patched diode gates and switches, and analog operational amplifiers to obtain the functions indicated. The analog and digital components communicate by means of comparators and analog switches, which are the basic analog-to-digital and digital-to-analog converters.

Uses of the individual components in the digital expansion system are:

Flip-Flops

Set electronic switches.

Act as counters to mark alternating time intervals.

Digital storage.

Schmitt triggers

Set electronic switches.

Inverter amplifiers

Complement logic.

Inexpensive analog inverter.

Differentiating amplifiers

Produce pulses from a square wave.

Analog operational amplifiers

Summers.

Integrators.

Generation of nonlinear functions.

Fig. 1.3 One of the Digital Expansion Modules for (ASTRAC I).

Fig. 1.4 Block-Diagram Representation Illustrating how the Digital Expansion System Ties in with ASTRAC I.

Patched diode gates and switches

Mode switching of operational amplifiers.

AND and OR logic.

CHAPTER II

DIGITAL EXPANSION SYSTEM DESCRIPTION

In the previous chapter we have become acquainted with the ASTRAC I and how the digital expansion system ties into the overall computer network. The digital expansion system (Fig. 1.3) consists of individual modules, each comprised of digital and analog components combined in a general purpose patchbay.

2.1 DIGITAL COMPONENTS

The digital portion of each module is made up of two bistable multivibrators or flip-flops (F.F.), two Schmitt triggers (S.T.) and two inverting/differentiating amplifiers. Figure 2.1 shows the symbols and logic function of each component.

Each flip-flop has SET and RESET inputs which allow asymmetrical operation and, when shorted together, permit symmetrical operation. Manual SET and RESET is also provided. The two outputs are high voltage complementary signals which permit the component to be used as an electronic switch driver. A neon bulb indicates the output state.

The input of the Schmitt trigger is designed so that the device switches at zero input voltage. Electronic switches must also be controlled by the Schmitt trigger, so that high-voltage complementing (push-pull) outputs are provided. No indication of the Schmitt trigger output state is provided, since one of the two outputs always follows the polarity of the input signal.

Inexpensive inverting/differentiating amplifiers, whose primary

Fig. 2.1 Symbols and logic for the digital components of the digital expansion system.

Fig. 2.2 Analog symbols for the digital expansion system.

purpose is digital inversion and pulse differentiation, may be used as an analog inverter in computer setups where accuracy is of secondary importance.

2.2 ANALOG ELEMENTS

The analog elements (Fig. 2.2) of each module consist of three operational amplifiers and a number of patched diodes and electronic switches.

University of Arizona Model III operational amplifiers¹⁴ are used. ASTRAC modules mount the amplifiers directly behind the patchbay to minimize wiring capacitance, so that high-speed analog computation is possible.

The electronic switches are six-diode bridge switches housed in brass cans designed to plug into the Schmitt trigger or flip-flop outputs controlling them. Two or more switches can be controlled by the same Schmitt trigger or flip-flop, since the design of the units permits them to be stacked.

2.3 PATCHBAY

The general-purpose design of the patchbay lends itself well to nonlinear-system simulation. Nylon banana jacks are the primary receptacles, for network elements mounted on General Radio type plugs, while Switchcraft Tini-jax interconnect with ASTRAC I shielded patch cords.

Below the symbols of each Schmitt trigger and flip-flop is a four-pin receptacle which accepts the electronic switch plug-in cans. The digital elements just above each receptacle automatically become the controlling logic for any switch in place.

Each flip-flop has screw-driver adjustments for output-level trimming, a mechanical SET/RESET switch, and a neon light indicating the output state. Output-level trimming is provided for each Schmitt trigger, and a toggle switch makes it possible to reverse the logic to the electronic switch receptacle manually. These controls and indicators are located within each element symbol.

Lights directly above the operational amplifier symbols indicate an overload condition of the respective amplifier.

CHAPTER III

EXAMPLES OF APPLICATIONS

The digital expansion modules aid ASTRAC I in parameter-effect analysis¹⁵, studies of optimal systems, correlation-function estimation⁶, simulation of nonlinear dynamical system, and many other computer applications.

Three interesting examples, viz., simulation of limit stops, optimization-type iterative solution of a boundary value problem, and estimation of correlation functions will be discussed here.

3.1 LIMIT STOPS¹⁶

Analog-computer simulation of hard impact elastic and semi-elastic stops should be approached with caution because serious scaling problems may be caused by the possibly very large impact forces. An electronic differential analyzer equipped with digital expansion modules can eliminate this scaling problem by employing digitally-switched storage integrators to simulate limit-stop action.

Figure 3.1a shows the linear motion of a point mass free to move under the action of external forces (gravity) for $y > 0$; there is a limit stop at $y = 0$. The computer setup shown in Fig. 3.1b is a simplified high-speed electronic implementation of an older relay circuit described in Ref. 16 (p 5-48). Instead of directly simulating the possibly very large impact forces reversing the velocity at impact, the iterative differential analyzer samples a fraction of the velocity at impact and introduces this as the initial velocity in the reverse

(a)

(b)

Fig. 3.1 Simulation of a point mass striking a reflecting frictionless surface.

direction after impact. The ratio of the velocity before and after impact is the coefficient of restitution, $\underline{a}$.

The operation of this simulation (Fig. 3.1b) depends on the special switched circuits illustrated in Fig. 3.2 to 3.5. In the circuit of Fig. 3.2, switch 2, controlled by signal w , functions as the COMPUTE-RESET control. When in COMPUTE, the circuit may either integrate x_1 or track (invert) x_2 . Switch 1 functions as the INTEGRATE-TRACK control. The circuits of Fig. 3.3 and 3.4 are similar, except that the circuit of Fig. 3.3 has no COMPUTE-RESET control, and the circuit of Fig. 3.4 has no INTEGRATE-TRACK control. The circuit of Fig. 3.5 acts as a SPDT switch.

Before the mass is released the circuit is in RESET. In RESET the output of integrator 3 ($y_0 > 0$) causes u to put integrator 1 in INTEGRATE and integrator 2 in TRACK. Integrator 1 integrates $-g$ (acceleration due to gravity). Integrator 2 then tracks $-\dot{a}y_1$, which is inverted and fed to integrator 3. Integrator 3 produces $(a+1)y = z$. When z passes through zero ($y=0$) the analog comparator and Schmitt trigger 1 change state switching integrator 2 to INTEGRATE and integrator 1 to TRACK. As a result, integrator 2 now integrates $-g$ to produce $\dot{y}_2 = \dot{y}$, while integrator 1 tracks $-\dot{a}y_2$, so that integrator 3 produces $-(1+a)y$. Since integrator 2 was tracking $-\dot{a}y_1 = \dot{a}y$ before impact, $\dot{y}_2$ starts with the correct reversed velocity after impact. At the start, the output from potentiometer 3 is y , while after the first impact it is $-y$, and the sign alternates each time $y=0$. The combination of amplifier 5 and electronic switch 6 compensates for this change in sign to produce the correct output.

The coefficient of restitution $\underline{a}$ is set by potentiometers 1 and 2.

Fig. 3.2 Integrator 1 for the Setup of Fig. 3.1. Electronic Switch 2 is a starting control as well as an initial velocity switch.

Fig. 3.3 Integrator 2 for the Setup of Fig. 3.1.

Fig. 3.4 Integrator 3 for the Setup of Fig. 3.1.

Fig. 3.5 Electronic Switch for the Setup of Fig. 3.1.

Fig. 3.6 Analog Comparator and Switch Driver for the Setup of Fig. 3.1.

Fig. 3.7 Waveforms of a point mass striking a reflecting frictionless surface for a coefficient of restitution of 0.8.

Fig. 3.8 Auto-Parameter Optimization for Boundary Value Problem.

Waveforms shown in Fig. 3.7 are copies of a Sanborn recording taken for a coefficient of restitution $a = 0.8$.

3.2 OPTIMIZATION-TYPE SOLUTION OF A BOUNDARY VALUE PROBLEM

A technique for optimizing a system or plant that has received attention in the past few years is parameter perturbation^{15,17}.

Figure 3.8 shows the block diagram of the computer setup for an optimization-type solution of a second-order boundary value problem. A simple differential equation, $\ddot{y} + y = 0$, was implemented on ASTRAC I with a repetition rate of 100 cycles per second. Figure 3.9 shows the controlling logic for the setup. The simulation of Fig. 3.8 adjusts the initial velocity (α) to the proper value to make the solution at time t_1 equal to the desired solution y_L .

A small perturbation signal $\Delta\alpha$, alternating in polarity every computer run, is added to the initial velocity of the system. An error $\pm\delta y$ is then introduced into the solution of each computer run yielding $y(t) \pm \delta y$. The negative of the desired solution y_L at time t_1 , is added to $y(t) \pm \delta y$, and the absolute value of the error $|e| = |y(t) \pm \delta y - y_L|$ formed. Sample-hold 1 produces $|y(t_1) \pm \delta y - y_L|$ and sample-holds 2 and 3, operating on alternating t_1 pulses, give $|y(t_1) + \delta y - y_L|$ and $|y(t_1) - \delta y - y_L|$, respectively. The difference of these signals, formed by inverters 4 and 5, is the product of the change in $|e|$ and the sign of $\Delta\alpha$ ($\Delta e \text{sgn} \Delta\alpha$).¹⁸ Integrator 6 produces a voltage which causes $y(t_1)$ to approach the desired value y_L at time t_1 .

For large errors the bridge limiter allows a large perturbation to enter the system. As the error decreases the bridge limiter control voltages decrease causing less perturbation to enter the system.

(a)

(b)

Fig. 3.9 Control logic of Auto-Parameter Optimization for Boundary Value Problem. (a) Logic block diagram. (b) Timing diagram.

Fig. 3.10 Waveforms of the Auto-Parameter Optimizer.

Figure 3.10 shows waveforms of interest for the block diagram in Figure 3.8. The problem was scaled down to a repetition rate of 10 cps, so that Sanborn recordings could be made. The system is initially at rest, except for .2 volt perturbation. As y_L is switched to twenty volts, an error voltage develops, the bridge limiter allows an increase in the perturbation, and convergence takes place with a small amount of overshoot.

The setup can, in principle, be adapted to multiple-parameter optimization. The circuit would be switched from one parameter to another as required by a suitable multiple-parameter optimization routine.

3.3 ESTIMATION OF CORRELATION FUNCTIONS

ASTRAC I is especially adaptable to studies of random processes, Fig. 1.2. The Statistics Computer⁶ (sample-averaging unit) is a simple analog-to-digital converter/adder which reads samples $^k x(t_1)$ or $^k y(t_1)$ of computer solutions $x(t)$ and $y(t)$ at digitally preset times t_1 and t_2 once per computer run and adds these functions to form sample averages

$$\frac{1}{N} \sum_{k=1}^N {}^k x(t_1) \quad , \quad \frac{1}{N} \sum_{k=1}^N |{}^k x(t_1)| \quad , \quad \text{or} \quad \frac{1}{100N} \sum_{k=1}^N {}^k x^2(t_1)$$

which are read out directly on digital counters.

The correlation function

$$R_{xy}(\tau) = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} x(t) y(t + \tau) dt$$

is approximated by the sample average¹⁹

$$\frac{1}{N} \sum_{k=1}^N {}^k x(t_1) {}^k y(t_1 + \tau)$$

where $^k x(t)$ refers to the value of $x(t)$ at the time t during the k^{th} computer run. To avoid the use of a multiplier, we use the squaring capability of the Statistics Computer in elementary quarter square

multiplication defined by

$$\frac{1}{4} [(x+y)^2 - (x-y)^2] = xy$$

We need not form both squares simultaneously; we sample and square

$$x(t_1) + y(t_2) \quad \text{and} \quad x(t_1) - y(t_2) \quad t_2 - t_1 = \tau$$

during alternate computer runs, to obtain

$$\frac{50}{n} \sum_{k=1}^{n/2} \left\{ \frac{[{}^k x(t_1) + {}^k y(t_2)]^2 - [{}^{k+1} x(t_1) - {}^{k+1} y(t_2)]^2}{100} \right\} \approx R_{xy}(\tau).$$

The scale factors shown are introduced in the above equation since two computer runs form a single term of the sum, and the sample-averaging unit divides the square by 100.

Refer to Fig. 3.11⁶, with the electronic switch ON the circuit of amplifiers 3 and 4 forms a summing network producing $-[x(t_1) + y(t)]$. When the electronic switch is OFF, a subtractor circuit is formed; the output of amplifier 3 is $-[x(t_1) - y(t)]$. On the k^{th} computer run the flip-flop turns the electronic switch ON and puts the Statistics Computer in the forward count mode. At time t_2 of this computer run the output of sample hold 2 holds ${}^k x(t_1) + {}^k y(t_2)$. A count proportional to the square of this voltage is stored in the Statistics Computer.

On the succeeding computer run $(k+1^{\text{st}})$ the flip-flop turns the electronic switch OFF and reverses the count direction of the Statistics Computer. At time t_2 of this computer run $(k+1^{\text{st}})$ sample hold 2 holds ${}^{k+1} x(t_1) - {}^{k+1} y(t_2)$. A count proportional to the square of this voltage is subtracted from the previous count.

Autocorrelation of random Gaussian noise, and of random-phase sine wave was performed using the above scheme. Forty thousand samples were taken at each value of τ .

The Gaussian noise was the result of filtering a random telegraph wave generated by a radioactive source⁸. The filter time constant was 1m sec. Data obtained gave a curve within ten percent of the theoretical curve, errors being due largely to calibration of the diode squaring circuit of the Statistics Computer. The estimation of the autocorrelation of the sine wave was within two percent of the theoretical curve.

The noise and sine wave were then mixed and the autocorrelation of the resulting signal estimated. The result was again within ten percent of the theoretical curve.

Estimation of the crosscorrelation of the above signal and a pulse train whose repetition rate was equal to the sine wave frequency gave the expected curve.

Fig. 3.11 Computer Setup for Estimation of Correlation Function.

APPENDIX

ELECTRONIC SYSTEM DESIGN

Cost, available power supplies, and the requirement that the digital expansion system be compatible with ASTRAC I required vacuum tube circuit design.

A.1 FLIP-FLOP

The design of the flip-flop includes provisions for symmetrical as well as asymmetrical triggering, visual indications of present state, and a manual SET/RESET switch.

The flip-flop is required to operate with a number of different circuits ranging from fast pulse circuits to slow analog comparators. Amplifiers are used at the inputs of the flip-flop to obtain fast high voltage signal for proper transition of the binary.

The need for switching high-voltage analog signals requires the flip-flop to have push-pull ± 100 volt low-impedance output waveforms. Cathode-follower stages with provisions for level trimming are used.

A conventional design was used for the binary²⁰. An external bias source allows a greater transition in the waveform.

Figure A.1 shows the circuit diagram of the flip-flop. The input waveforms are differentiated and amplified by the pentode amplifiers. The amplifiers are biased well below cutoff, so that only positive-going input pulses are amplified, and some degree of discrimination against noise is obtained. The amplifier outputs are

Fig. A.1 Bistable Multivibrator.

fast high-voltage negative pulses.

These pulses are a-c coupled through steering diodes to the grids of the binary, so that the output of only one amplifier is felt by the binary at the same time.

The plates of the binary swing between saturation voltage and approximately cutoff voltage. Voltage-divider networks consist of three neon bulbs, a variable resistor, and the cathode follower grid leak resistor cause a shift in the d-c levels of the binary outputs with very little loss in voltage swing. The cathode followers isolate the outputs of binary from any external load and develop the desired low-impedance output. The output levels are trimmed by variable resistors in the divider networks.

The output waveforms have a 10-90 percent rise time of 2.5μ sec, while the fall time is 2μ sec. Each output level may be adjusted through approximately 20 volts.

Binary action is obtained by shorting the inputs and applying a pulse train or square wave, while SET/RESET operation is obtained by separately triggering the two inputs. A three position Switchcraft "Lev-R-Switch" is used for manual SET/RESET.

A.2 SCHMITT TRIGGER

A conventional design was used for the Schmitt trigger²¹. It was desired that the switching level of the Schmitt trigger be at zero volts. This requires both positive and negative voltage supplies. To stabilize the switching level, a regulator tube is used to decrease the positive voltage supply.

One of the functions of the Schmitt trigger is to drive electronic switches which control signals as large as the computer reference voltage (100V). This requires the Schmitt trigger to have complementary high-voltage output signals. Triode amplifiers are used to obtain the necessary amplification for the output signal.

Figure A.2 shows a diagram of the Schmitt trigger. The switching level is controlled by the $100k\Omega$ variable resistor in the feedback loop of the device while the $5k\Omega$ variable resistor in the cathode of the input stage effects the hysteresis. The speed-up capacitors in the circuits also have an effect on the switching points.

The voltage of the second stage varies between cutoff and approximately 50 volts. The level of this voltage is shifted and amplified by the next triode stage. The complement is obtained by an additional amplifier. These two voltages are then applied to cathode followers which produce the desired output voltage and impedance levels. Adjustment of the output level is accomplished by the $50k\Omega$ variable resistors at the followers inputs.

Complementary output square pulses slightly greater than ± 100 volts are obtained when an input signal swings about zero volts. The 10 to 90 percent rise and fall time is 2μ sec. When properly adjusted, the hysteresis is less than one volt at 10kc.

A.3 INVERTING/DIFFERENTIATING AMPLIFIER

To allow the amplifier to be used in any desired computer setup requiring digital inversion, a high-gain device with negative feedback was chosen. This design gives good frequency-response characteristics

and very low output impedance.

The pentode amplifier and cathode follower form an amplifier that has zero output voltage for zero input voltage, (Fig. A.3). The gain is approximately 300. With the feedback and input resistors in place, a unity-gain inverter is formed. The screen-bypass capacitor shown increases the bandwidth, as does the capacitor across the neon bulbs.

A 60 volt square wave with 0.1μ sec rise and fall times was used as an input test signal. The 10 to 90 percent rise time of the amplifier is 0.9μ sec, while the fall time is 0.7μ sec with no overshoot. Applying the test signal to the capacitor input produces pulses with a 25μ sec decay time constant.

A.3 DIODE-BRIDGE SWITCH

A six-diode bridge was chosen as the electronic switch to be used in conjunction with the digital modules. This switch has the advantage of faster turn-off time than a four-diode bridge²². The circuit diagram of the bridge is shown in Fig. A.4. Operation of the switch is covered in the literature.

The electronic switch is the basic digital-analog link in the digital expansion system. Analog-program switching is the primary job of the switch. Circuit configurations using the switch are shown in Fig. A.5.

Switching spikes are the main objection to the use of electronic switches, for such spikes are difficult to eliminate and contribute to error. If matched diodes and perfectly symmetrical driver pulses are used, the spikes will be trivial in most computer setups.

Fig. A.3 Inverting/Differentiating Amplifier.

Fig. A.5 Applications of the Analog Switch.

Driving-pulse level trimming is provided in the digital expansion system. This is adequate, since the spikes observed at the outputs of the circuits of Fig. A.5 contribute little error when computer repetition rates 100 or lower are used (Figs. A.6 to A.9).

Offset voltages caused by the switch are minimized through proper adjustment of the supply voltages for the switches.

(a)

(b)

Fig. A.6 Switching spikes at the output of the circuit in Fig. A.5(a) for zero input voltage. Horz. scale: $2\mu\text{sec}/\text{cm}$, Vert. scale: $2\text{V}/\text{cm}$. (a) Output as the switch is turned on. (b) Output as the switch is turned off.

(a)

(b)

Fig. A.7 Switching spikes at the output of the circuit in Fig. A.5(b) for zero input voltage. Horz. scale: $2\mu\text{sec}/\text{cm}$, Vert. scale: $0.2\text{V}/\text{cm}$. (a) Output as the switch is turned off. (b) Output as the switch is turned on.

(a)

(b)

Fig. A.8 Switching spikes at the output of the circuit in Fig. A.5(c) for zero input voltage. Horz. scale: $0.5\mu\text{sec}/\text{cm}$, Vert. scale: $.05\text{V}/\text{cm}$. (a) Output as the switch is turned on. (b) Output as the switch is turned off.

(a)

(b)

Fig. A.9 Switching spikes at the output of the circuit in Fig. A.5(d) for zero input voltage. Horz. scale: $0.5\mu\text{sec}/\text{cm}$, Vert. scale: $.05\text{V}/\text{cm}$. (a) Output as the switch is turned on. (b) Output as the switch is turned off.

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