A NEW HIGH PERFORMANCE COMPUTER D-C AMPLIFIER

by

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TABLE OF CONTENTS

	Page
LIST OF ILLUSTRATIONS	v
LIST OF TABLES	vi
ABSTRACT	vii
INTRODUCTION	1
Specifications	1
Present State-of-the-Art	2
OVERALL DESIGN	7
AN IMPROVED LOW-IMPEDANCE OUTPUT STAGE	10
THE INTERMEDIATE-FREQUENCY AMPLIFIER AND EQUALIZATION	13
THE LOW-DRIFT, HOT-SUBSTRATE STAGE	16
ADJUSTMENT PROCEDURE AND TEST RESULTS	18
APPENDIX: TEST CIRCUITS	20
LIST OF REFERENCES	23

LIST OF ILLUSTRATIONS

Figure	Page
1. Block diagram and frequency response of the new d-c amplifier	8
2. Circuit diagram of the computer d-c amplifier	11
3. Unity gain inverter equivalent circuit at low and intermediate frequencies	15
4. Measured open-loop frequency response	19
5. Square wave response	19
A.1. Test circuit for voltage offset and noise . .	20
A.2. Test circuit for bias-current offset	20
A.3. Test circuit for square-wave response, capacitive load, and settling time	21
A.4. Test circuit for error at 10 KHz	22
A.5. Test circuit for open-loop gain	22

LIST OF TABLES

Table	Page
1. Performance of the New d-c Amplifier	viii
2. Comparison of Several d-c Amplifiers	3
3. Output Stage--With and Without Negative Feedback	12

ABSTRACT

A new computer d-c amplifier designed for very fast as well as for real time analog/hybrid computation combines large bandwidth (30 MHz gain-bandwidth product) and high mid-band gain (68 db at 10 KHz) with full ± 10 -V, 30 mA output to 5.0 MHz, and low open-loop output impedance (50 ohms at 10 KHz). High d-c gain (120 db) and exceptionally low drift (50 pA/deg C, 2.5 μ V/deg C) is obtained with the aid of an inexpensive hot-substrate integrated-circuit pre-amplifier rather than with conventional chopper stabilization. A three-channel feedforward design employs an overcurrent-protected 30 mA class AB wideband output stage in the high-frequency channel, a feedback-equalized integrated-circuit operational amplifier as the intermediate-frequency channel, and the hot-substrate integrated differential amplifier stage as the low-frequency channel. Overcurrent protection makes the new amplifier short-circuit proof.

Table 1 shows the performance of the new d-c amplifier.

Table 1. Performance of the New d-c Amplifier

Typical Performance at 25°C		Unit
Open-Loop Gain	120	db
Unity Gain Bandwidth	30	MHz
Rated Output		
Voltage	± 10	V
Current	± 30	mA
Max Freq for Rated Output	5.0	MHz
Input Offset		
Voltage	Adj to Zero	mV
Bias Current	Adj to Zero	nA
Input Offset Drift		
Voltage	± 2.5	$\mu\text{V}/^\circ\text{C}$
Bias Current	± 50	$\text{pA}/^\circ\text{C}$
Input Noise	15	μVrms
Open-Loop Output Impedance		
at 100 Hz	100	Ω
at 10 KHz	50	Ω
Unity-Gain Inverter		
Freq. Response ± 3 db	10	MHz
Error at 10 KHz	0.1	%
Capacitive Load	0.001	μF
Quiescent Current	20	mA

INTRODUCTION

The performance requirements of a new generation of analog/hybrid computers leads naturally to the design of improved computer d-c amplifiers, which are equally useful in many control and instrumentation applications.

Specifications

The University of Arizona's new LOCUST computer will be capable of ultra-fast iterative operation with up to 2000 differential-equation solutions per second. Computer accuracy at such high computing speeds requires large intermediate-frequency gain: thus, dynamic errors within 0.1 per cent at the typical computing frequency of 10 KHz requires that the amplifiers used for integration and phase inversion have a gain of at least 66 db at that frequency [1]. Such high closed-loop gain at 5 to 10 KHz combined with stable operation and good transient response necessitates gain-bandwidth products of at least 20 MHz. In addition, the analog/hybrid computer must also be capable of real-time or "slow" simulation, possibly requiring open-loop integration for as long as several minutes. The integrator output-error equation [2]

$$\text{d-c}_{\text{error}} = \frac{t}{RC} (e + Ri)$$

where RC is the integrator time constant, and e and i are the offset voltage and current referred to the amplifier input point, imposes a requirement of $i \leq 0.25$ nA and $e \leq 50$ μ V to produce drift error less than 1.0 mV/sec over the expected laboratory temperature range of $25 \text{ deg C} \pm 10 \text{ deg C}$. D-c accuracy within 0.01 per cent requires a minimum d-c gain of 111 db using all inputs for a total summer gain of 3^4 . Similarly high d-c gain is desirable for accurate low-frequency integration [1].

Present State-of-the-Art

Table 2 shows measured amplifier performance actually obtained, together with a comparison of similar performance data for currently available commercial d-c amplifiers and for the d-c amplifiers presently used in the University of Arizona's ASTRAC II hybrid computer.

Fast operational amplifiers combined with low drift and full ± 10 -V, 30 mA output to 1.0 MHz generally require the use of a feedforward connection [1] to a wide-band class AB output stage. Although several transistor solid-state operational amplifiers meeting these requirements have been available for several years, there have been some recent additions to the wide-band class of d-c amplifiers. Use of differential FET input stages has reduced input bias current by typically two orders of magnitude, with voltage

Table 2. Comparison of Several d-c Amplifiers

Typical Performance at 25°C					
Amplifier type	New d-c Amplifier	ASTRAC II	Analog Devices Model 210	Burr-Brown Model 3010	Unit
	Hot-substrate differential input stage	Bipolar transistor chopper stabilized	FET chopper stabilized	MOSFET chopper stabilized	
Open-Loop Gain	120	150	160	160	db
Unity Gain Bandwidth	30	20	20	15	MHz
Rated Output Voltage	± 10	± 10	± 10	± 10	V
Current	± 30	± 30	± 20	± 20	mA
Max Freq for Rated Output	5.0	1.0	0.5(min)	1.2	MHz
Input Offset Drift Voltage	± 2.5	± 10	$\pm 0.5(\text{max})$	± 0.2	$\mu\text{V}/^\circ\text{C}$
Bias Current	± 50	± 100	$\pm 1(\text{max})$	± 0.5	$\text{pA}/^\circ\text{C}$
Input Noise	15	20	10	6	μVrms

Table 2.--Continued

Input Impedance	24	50	500	500	Kohm
Quiescent Current	+25 -20	<u>+25</u>	+40 -10	<u>+5</u>	mA mA

drift about the same as that obtained with a conventional bipolar transistor differential input stage.

For applications requiring ultra-low current offset and drift as well as low voltage offset and drift, chopper-stabilization has been added to fast amplifiers. The MOSFET chopper with negligible current offset and zero voltage offset excels the performance of a bipolar transistor chopper and approaches the performance of mechanical choppers. It should be noted, in this connection, that operational amplifiers with carefully matched and compensated FET or bipolar transistor differential-input stages actually have lower drift than chopper-stabilized amplifiers using a transistor chopper.

Integrated-circuit operational amplifiers are finding increased application in circuit and system design. Advantages of the monolithic operational amplifiers are small size, good voltage drift and differential bias-current drift due to excellent transistor matching and thermal coupling on the chip, and low cost. Disadvantages of presently available integrated-circuit operational amplifiers for use in a high-quality hybrid/analog computer are: relatively large input bias-current requirements (hundreds of nanoamperes), limited gain-bandwidth product (1.0 MHz typical for a compensated unity-gain inverter), inadequate output current (2 to 10 mA), and a restricted full-power output (+10-V, 2 to 10 mA to 10 KHz). Lack of

high-beta high-frequency PNP transistors, the limitations placed upon resistance values and tolerances, plus the oversight of feedforward techniques are among the reasons integrated-circuit operational amplifiers have not yet approached the sophistication obtainable with discrete-component operational amplifiers. Many integrated-circuit-operational amplifier manufacturers have not included input-overvoltage or output-overcurrent protection. One exception is the Westinghouse Type WM174Q, which is short-circuit proof to ground. The scheme used in the WM174Q is used for overcurrent protection in the amplifier described here.

OVERALL DESIGN

The block diagram of Fig. 1a illustrates the basic amplifier design, which employs a three-channel feedforward circuit. Starting from the amplifier input (summing junction), the three channels are: the high-frequency channel to the wideband class AB output stage, the intermediate-frequency channel to the Motorola MC1433G integrated-circuit operational amplifier, and the low-frequency channel to the Fairchild μ A726C hot-substrate preamplifier. Figure 1b illustrates the frequency response of each channel and their combination.

The limitations on bandwidth and output current of the integrated-circuit amplifier are eliminated by cascading the integrated-circuit amplifier with the high-current output stage and by feeding the high frequencies directly from the summing junction to the output stage.

The original design called for a chopper-stabilized preamplifier in the low-frequency channel to reduce input voltage and bias-current offsets and drift to within acceptable limits. Since the advent of the new integrated-circuit hot-substrate differential amplifier, it was decided that a chopper channel would not be necessary.

The entire amplifier is intended for easy assembly on a printed-circuit board with a minimum of adjustments;

Fig. 1. Block diagram and frequency response of the new d-c amplifier. (a) Block diagram showing signal flow through the three channels. (b) Open-loop Bode plot of the three channels and their combination. Dotted lines show the roll-off of a more conventional 6 db/octave feedforward amplifier. Note that the "zero" needed at 40 KHz lowers the gain at 10 KHz. An improvement in the open-loop gain of only 6 db at 10 KHz will decrease the dynamic error of a phase inverter operating at 10 KHz, by a factor of two.

(A)

Fig. 1. Block diagram and frequency response of the new d-c amplifier.

this is a necessary requirement for the University of Arizona's Hybrid/Analog Computer Laboratory, which utilizes student technicians for the assembly and testing of the completed amplifiers. This, in fact, was the main reason for employing an integrated circuit in the intermediate-frequency channel.

AN IMPROVED LOW-IMPEDANCE OUTPUT STAGE

Figure 2a shows the circuit diagram of the output stage. The output stage consists of a pair of emitter followers (Q7 and Q8), which provide low output impedance as well as wide bandwidth and high output current. Diodes D4 and D5 provide bias and V_{BE} temperature tracking for the emitter followers.

Diodes D6 and D7 and resistors R39 and R40 form the overcurrent-protection circuit. When the output current is sufficient to produce a 0.6 V drop across resistor R39 or R40, diode D6 or D7 begins conducting, thereby "robbing" the bases of transistors Q7 and Q8, respectively, of any more available current.

A novel feature is the provision of transistor Q3, which combines with Q6 into a feedback-pair. This circuit provides a high-gain input for the output of the intermediate-frequency channel. Degenerative voltage feedback increases the input impedance, lowers the output impedance (which decreases the d-c amplifier's open-loop output impedance, a desirable feature), and supplies the necessary level shift for the output of the intermediate-frequency amplifier. The stage gain of the feedback pair is approximately $1 + R37/R34 [3]$. Capacitors C16 and C17 shape the frequency response of the output stage.

Fig. 2. Circuit diagram of the computer d-c amplifier. (a) The wideband class AB output stage has low open-loop output impedance, full ± 10 -V, 30 mA output to 5.0 MHz, and provides two convenient input points for the summation of the signals from the high-frequency channel and the intermediate-frequency amplifier. (b) The intermediate-frequency integrated-circuit amplifier accurately controls the gain and frequency response of the intermediate-frequency signals by feedback through the three-terminal equalizer network. (c) The hot-substrate differential preamplifier provides low-offset/low-drift amplification of low frequencies down to d-c.

Fig. 2. Circuit diagram of the computer d-c amplifier.

The high-frequency channel input to the fast output stage is through emitter follower Q4, which prevents blocking with step inputs [1]. The gain of transistor Q5 is determined by the ratio of the collector impedance and the emitter resistor, R32.

Table 3 demonstrates how the degenerative voltage feedback of the feedback pair lowers the open-loop output impedance and consequentially determines the gain of the high-frequency and intermediate-frequency channels.

Table 3. Output Stage--With and Without Negative Feedback

	R37= ∞	R37=330 Kohm	Unit
Open-Loop Output Impedance (100 Hz)	330	100	ohm
Gain of the Feedback Pair	46	36	db
Gain of the High-Freq Channel	45	36	db

THE INTERMEDIATE-FREQUENCY AMPLIFIER AND EQUALIZATION

Figure 2b shows the circuit diagram of the intermediate-frequency channel. As required by the specifications discussed earlier, the error at 10 KHz must be within 0.1 per cent, requiring a gain of at least 66 db. An amplifier having a gain-bandwidth product of 20 MHz and a 6 db/octave roll-off, will meet this requirement of 66 db at 10 KHz. Note, however, that a feedforward amplifier must have a "zero" at the intersection of the low-frequency channel and the high-frequency channel to insure good transient response [4]; this necessarily lowers the gain at 10 KHz, as demonstrated in Fig. 1b. Figure 1b also shows the roll-off achieved with a feedback-equalized integrated-circuit operational amplifier (Motorola Type MC1433G), to obtain increased gain at 10 KHz. The transfer function of the intermediate-frequency operational amplifier is given by minus the ratio of its feedback and input short-circuit transfer impedances, i.e., [1]

$$\frac{E_o(s)}{E_i(s)} = \frac{-K}{R17} \left[\frac{1+sT_2}{(1+sT_1)(1+sT_3)} \right]$$

where

$$\left| \frac{E_o}{E_i} \right| = 1000$$

$$R21 = R22 = \frac{KT_2}{T_1 + T_3}$$

$$R_{23} = \frac{KT_2}{(T_1+T_3)(T_1+T_3-2T_2)}$$

$$C_{14} = \frac{T_1(T_1+T_3)}{KT_2} \quad C_{15} = \frac{T_3(T_1+T_3)}{KT_2}$$

Since resistor R17 effectively returns the summing junction of the overall amplifier to ground, this resistance must be large enough to maintain a sufficiently large feedback ratio when the entire amplifier serves as an inverter or summer. Referring to Fig. 3, the unity gain inverter feedback ratio at low and intermediate frequencies is given by [1]

$$\beta = \left(1 + \frac{R_f}{R_i} + \frac{R_f}{R_{in}}\right)^{-1}$$

where $R_f = R_i$ are the external feedback and summing resistors and $R_{in} \approx R_{17}$ is the amplifier input impedance. With an input impedance of 24 Kohm, $\beta = 0.415$, as compared to $\beta = 0.5$ for a high input impedance amplifier. The error equation, $\epsilon = 1/A\beta$ [1] for the overall amplifier shows that the required gain at 10 KHz for 0.1 per cent error for this amplifier is only 1.5 db greater than the required gain (66 db) would be for $R_{17} = \infty$.

Fig. 3. Unity gain inverter equivalent circuit at low and intermediate frequencies.

THE LOW-DRIFT, HOT-SUBSTRATE STAGE

Figure 2c shows the low-frequency channel input stage, a Fairchild μA726C temperature-controlled differential pair. This device, constructed on a single silicon chip, contains a well-matched transistor pair Q1a , Q1b and an active temperature-regulating circuit. A temperature-compensated constant-current source (Q2) supplies the emitter currents for the differential pair.

Several design constraints must be observed.

1. The common-mode voltage of the MC1433G is limited to 8 V.
2. The collector load impedances of Q1a and Q1b must be small to limit voltage drift (referred to the overall amplifier input) caused by the differential bias-current drift of the MC1433G .
3. The collector-to-base voltage of Q1a and Q1b must be large enough to ensure proper operation.

These constraints are satisfied with the connection of a voltage-dropping resistor divider, R13 and R14 , to the collector resistors R8 and R9 of Q1 .

The μA726C hot-substrate differential stage is specified to have a voltage drift of $2.0 \mu\text{V/deg C}$ maximum and a differential bias-current drift of 10 to 30 pA/deg C , typical. In actual fact, the measured bias-current drift,

as opposed to differential bias-current drift, was also found to be exceptionally low (50 pA/deg C, typical). Resistor R2 determines the temperature of the heated substrate. As the temperature of the substrate increases, the substrate heater current increases; I_{co} leakage, and current gain of the differential pair increase, so that bias-current temperature drift decreases, and amplifier noise increases. These effects, plus the ambient temperature range, should be taken into account.

Since the d-c amplifier is to be used in a laboratory environment, R2 was chosen to be 121 Kohms, which produces a chip temperature of 80 deg C [5]. The heater current at this chip temperature is 4.5 mA at 25 deg C ambient temperature.

Connection from the two collectors of the differential input stage to the differential input of the intermediate-frequency amplifier preserves true differential action for lowest possible drift. The temperature-compensated constant-current generator, Q2, sets the current in each collector of Q1 at 30 μ A. Capacitors C8 and C11 roll off the low-frequency channel, which has a gain of 20 db, as shown in Fig. 1b. Input bias-current and voltage offset can be nulled out with potentiometers R6 and R12, respectively, although few adjustments are required in practice. Diodes D1 and D2 protect the input stage from the student computer programmer.

ADJUSTMENT PROCEDURE AND TEST RESULTS

Adjusting the input bias-current and voltage offset to zero are the only adjustment procedures required. (See the Appendix for all test circuits described in this section.) A Bode plot of the actual frequency response is given in Fig. 4. Figure 5 shows the amplifier square-wave response with and without a 0.001 μF load. The combined slew and settling time to 0.1 per cent of a 10-V square-wave is within 10 μsec . Measurement of the unity-gain inverter error at 10 KHz shows that the combined dynamic and phase shift error is within 0.1 per cent. Noise from d-c to 10 KHz is 15 μVrms . Open-loop gain is 120 db, and voltage and bias-current drift are $\pm 2.5 \mu\text{V/deg C}$ and $\pm 50 \text{ pA/deg C}$ over a 0 deg C to 40 deg C range.

Fig. 4. Measured open-loop frequency response. (Compare with the Bode plot of Fig. 1b.)

Fig. 5. Square-wave response. (a) Without capacitive load. (b) With $0.001 \mu\text{F}$ load. Oscilloscope settings are 2.0 V/cm and $1.0 \mu\text{s/cm}$. Design for good transient response is often a bit more difficult with feed-forward amplifiers, but careful equalization has produced the desired result of fast step response with small overshoot.

APPENDIX

TEST CIRCUITS

$$V_{\text{offset}} = \frac{E_o (V_{dc})}{1000}$$

$$\text{Noise} = \frac{E_o (V_{rms})}{1000}$$

Fig. A.1. Test circuit for voltage offset and noise.

$$I_{\text{offset}} = \frac{E_o}{10^7}$$

Fig. A.2. Test circuit for bias-current offset.

Settling-time measurement deviation (* and ** are matched resistor pairs).

$$\frac{E_i(t) - E_{\epsilon}(t)}{10K} + \frac{E_o(t) - E_{\epsilon}(t)}{10K} = 0$$

$$E_{\epsilon}(t) = \frac{E_o(t) + E_i(t)}{2}$$

For t sufficiently large $E_o = -E_i$

Let " t " be the time when $E_o(t) + E_i(t)$ is within 0.1% of E_i .

E_{ϵ} is measured at E' to avoid "loading" the summing junction.

Fig. A.3. Test circuit for square-wave response, capacitive load, and settling time.

Fig. A.4. Test circuit for error at 10 KHz.

Fig. A.5. Test circuit for open-loop gain. This test circuit requires shielding from 60 Hz sources and careful voltage offset balancing.

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