A NEW DIGITAL ATTENUATOR SYSTEM
FOR HYBRID COMPUTERS

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ABSTRACT

Digital Attenuators are simple multiplying digital-to-analog converters used to replace coefficient-setting potentiometers in the modern analog/hybrid computers. This report describes a new digital attenuator system employing low phase-shift miniature metal-film ladder networks switched by latching reed relays which give the system a non-destructive coefficient memory even when the computer is switched off. New digital control logic employs serial data transmission, which not only permits one to set all 200 attenuators of a typical hybrid computer installation within 20 milliseconds, but also requires only one address line per 14-bit attenuator. For maximum contact life relay contacts are switched only when no current is flowing. The digital computer static-check routine can readily check individual relays to simplify maintenance.

Particular emphasis in this report is on a digital-attenuator system designed for a very fast repetitive computer, but the same design approach is readily applied to "slow" analog computers, and appears to be even more advantageous there.

INTRODUCTION

In most electronic analog computers multiplication of voltages by constant coefficients has been implemented with potentiometers. In small computer systems, the potentiometers are set by hand. In larger systems employing 100 or more potentiometers, servo-setting systems have been introduced. Aside from being subject to mechanical wear and misadjustment, a servo potentiometer-setting system requires a considerable time for positioning the potentiometers. Potentiometers must be addressed and set one at a time. Usually, the desired coefficients are stored on punched paper tape, and the tape is read slowly until all potentiometers have been set. A typical setup time for 100 potentiometers might be 12 minutes.¹

The digital attenuator represents an attempt to decrease the time required for setting coefficients, thereby greatly reducing the setup time associated with an analog computer. A typical digital attenuator system consists of a digital computer or tape-reading system for storing coefficient settings, an address network for addressing individual attenuators, a manual switching system for setting coefficients manually, a buffer register, and many (100 to 500) digital attenuator networks (Figure 1).

Figure 1. A Digital Attenuator System

Each digital attenuator is, essentially, a multiplying digital-to-analog converter, which can be set to any desired coefficient. After the coefficient has been set, the analog input voltage is applied as the reference voltage on the digital-to-analog converter, which scales it down by the desired ratio (Figure 2).

There are several obvious advantages to a digital attenuator system. Perhaps the most significant is that the system has no mechanical parts, with the possible exception of relays, to slow down the setting of coefficients. Coefficients are set by using digital switches controlled by a digital computer, instead of being set by a slow electromechanical servo system. A second advantage is that digital-attenuator setting intrinsically accounts for the effect of the load on the attenuator, while setting of a potentiometer requires feedback of the output voltage with the load connected. Hence, the digital attenuators can be set even before the computer patch panels have been put in place.

Several versions of the digital attenuator are already on the market, but like anything new, they still suffer from various handicaps. Some digital attenuator systems require a separate amplifier for each attenuator. This is quite costly, as often in computer problems an amplifier or integrator may have as inputs the outputs of several digital attenuators. All present systems share the

Figure 2. A Typical Digital Attenuator

necessity to address all of the bits (usually 14) of each digital attenuator register in parallel. This results in complex and expensive address logic requiring multiple connections to every attenuator.

Another possible handicap, when relay switching is employed, is the large amount of current required by the 1400 relays in 100 digital attenuators. This current may easily exceed one or two amperes, and thus generate a substantial amount of heat. Electronic switching is much faster, but the non-zero resistance of the switch presents difficulties, especially in fast low-impedance analog computers. One commercially available system employs electronic (FET) switches rather than relays. To reduce the error caused by the non-zero switch resistance, this system employs error feedback to adjust the least significant bits of the digital-to-analog converter network.

Not all of the available digital attenuator systems are handicapped by all of these problems; but each of them has at least one of these problems, and generally more than one. The new digital attenuator system described here attempts to overcome these handicaps while still keeping the cost of the digital attenuator down to a figure which will make it practical and profitable to use.

TABLE OF SPECIFICATIONS

Specifications are given not only for the digital attenuator designed in this paper, built for a very fast repetitive computer, but also for a typical digital attenuator that might be built for a "slow" analog computer.

	Fast Computer	Slow Computer
Number of Bits	14	16
Static Accuracy	.02% of half scale	.02% of half scale
Resolution	.01%	.01%
Gain Range	0.0002-3.2767	0.0001-13.1071
Feedback Resistance	10K	1M
Ladder Resistance	2.0514K	50K
Maximum Load on Input	13.3ma	4ma
Setting time per 200 attenuators	20 msec	20 msec

DESIGN OF A DIGITAL ATTENUATOR SYSTEM

To develop a digital attenuator which overcomes all of the disadvantages mentioned is no simple task, for many of the requirements are conflicting. To clarify the objectives, the following list of proposed requirements has been compiled. The order in which the requirements are listed does not necessarily indicate their respective importance.

1. Individual digital attenuators should not require separate amplifiers. In other words, each attenuator must be a free element capable of being patched into any of the computer amplifiers or integrators.
2. Switching of digital attenuators must be so fast that the setting of 100 coefficients will not present a significant delay. As a design objective, a total setting time of 0.5 seconds was chosen as the maximum acceptable.
3. Serial transmission of data is preferred to parallel transmission. Parallel entry requires one address gate-tree for each bit of each digital attenuator (100 attenuators x 14 bits = 1400 lines); serial entry requires only a single address gate-tree for each digital attenuator. Note that

serial addressing will conflict with requirement number 2.

4. The load on the amplifier driving an attenuator network must not exceed that of a comparable coefficient-setting potentiometer.
5. The digital attenuator should have a range of coefficient settings from 0.0001 to at least 3.2767.
6. A digital attenuator must not reduce the feedback ratio, β ,³ of the succeeding amplifier more than a coefficient-setting potentiometer.
7. The attenuator network should not require any adjustments.

Having accepted the requirements that the digital attenuator be patchable and capable of accepting data serially, the design procedure can be separated into four areas:

1. The Attenuator Network
2. The Switches
3. The Memory and Addressing Network
4. The Control Logic

These four areas will be discussed in detail.

The Attenuator Network

The function of the attenuator network is to convert an input voltage to a summing-junction current which is scaled by the proper coefficient (Figure 3). The design of an attenuator network offers many possibilities, but perhaps the first question to be considered is the choice between binary weighting and binary-coded-decimal weighting. Binary weighting was selected for reasons to be considered later; consequently, only binary networks will be discussed.

Figure 4 illustrates some binary-weighted attenuator designs;² many other combinations are possible. Figure 4a shows a simple binary-weighted summing network employing SPDT (form C) relays to prevent capacitive feedthrough. Since the required $2^{14}:1$ resistance ratio is not practical, the low-current branches may be implemented with T-network transfer impedances³ (Figure 4b). This network also permits use of the somewhat less expensive SPST (form A or B) relays. Both Figures 4a and b employ summing-junction patching, which should work well for "slow" analog computers, but may not be practical for very fast repetitive computers.

The circuit of Figure 4c permits patching to either gain-of-1 or gain-of-10 amplifier inputs if the latter are loaded as shown. The simple ladder network of Figure 5 can be similarly patched and permits especially simple

Figure 3. A Typical Attenuator Network

Figure 4. Binary-Weighted Summing Networks

Figure 5. Binary-Weighted-Ladder Summing Networks

construction, since an entire set of similar metal-film resistors can be deposited on a ceramic substrate in a single operation.

To eliminate the necessity of patching into two different amplifier inputs, the configuration in Figure 5a can be rearranged as in Figure 5b, and the digital computer can be employed not only to set the coefficient but also to set the gain. This network still provides isolation from the summing junction, and the patching is always made to a gain-of-10 input.

The choice of resistance values in Figures 4 and 5 must satisfy the following requirements:

1. The load on the driving amplifier must not be greater than that of a comparable coefficient-setting potentiometer.
2. The summing-junction-to-ground impedance must not be so low that it excessively reduces the operational amplifier's feedback ratio and hence its bandwidth.
3. The impedances associated with the attenuator must not be so high that distributed capacitances unduly attenuate high frequencies; the phase shift of the digital attenuator should be less than that of a coefficient potentiometer.

The capacitances associated with high impedances (above 30K ohms) tend to lower the frequency response of very fast repetitive computers. For this reason, the feedback resistor for the design computer was selected as 10K ohms, and also an upper limit of 30K ohms was placed on attenuator resistors.

To best demonstrate the tradeoffs that must be considered when designing the attenuator network, the equivalent circuit of a binary-weighted digital attenuator, with only its most significant bit energized, should be studied. When only the most significant bit is energized and the input is one volt, then the output voltage represents one-half the maximum coefficient setting for the particular ladder network. The maximum coefficient associated with a binary-weighted ladder will always be a power of two. For an attenuator to handle a coefficient setting of 10, it must be capable of going to the next higher power of two. If 0.0001 is the minimum coefficient, the attenuator must be able to go to 13.1071 to be capable of handling a coefficient setting of 10.

With a given feedback resistor, $R_F = 10K$, and a given input, $E_{in} = 1$ volt, the transfer equation of the amplifier in Figure 6 can be solved for the input and ladder resistances, R_1 and R , thus establishing a relationship between them and the output. Using this equation, specifically

$$E_o = - \frac{R_F}{2(R+R_I)} E_{in}$$

Figure 6. Binary-Weighted Digital Attenuator

$$R + R_1 = - \frac{R_F}{2} \frac{E_{in}}{E_{out}} = - \frac{5K}{E_{out}}$$

it is possible to associate specific maximum coefficient settings with the resistor values. For example, if a maximum coefficient setting of 10 were mandatory, 13.1071 must be the design value of the largest coefficient, making the output with only the most significant bit energized -6.5535 volts. This would require that $R + R_1 = 762.9$ ohms.

To modify this design for a "slow" analog computer one would apply the following considerations.

1. If summing-junction patching is permitted, the input resistor, R_1 , could be reduced to zero. This allows all of the resistance to be in the attenuator network, thereby reducing the load on the driving amplifier.
2. "Slow" computer design permits the feedback resistor to be as high as 100K. This, in turn, permits the ladder resistances to be much higher thus greatly reducing the load on the driving amplifier, and making higher coefficient settings possible.

Unfortunately, for a very fast computer a feedback resistor of at most 10K is mandatory, and summing-junction

patching is prohibited; therefore, to achieve a coefficient-setting of 10 we must require that $R + R_1 = 762.9$ ohms. The maximum load on an amplifier driving a 2K ohm potentiometer set at 1.000 and connected to a 1K ohm input resistor is 670 ohms. The minimum input impedance of a ladder network is approximately $R/2$.⁴ To maintain the potentiometer loading conditions, the ladder resistance R must then be at least 1340 ohms. This conflict must be resolved.

To study the effect of the total resistance R_T (where $R_T = R + R_1$) on the maximum coefficient setting, a table of Maximum Coefficient vs Resistance was compiled:

Entry	Maximum Coefficient	$R_T = R + R_1$	Resolution
1	16.383	610.3	.1%
2	13.1072	762.9	.01%
3	8.191	1220	.1%
4	6.5536	1525.7	.01%
5	4.095	2440	.1%
6	3.2767	3051.4	.01%
7	2.047	4882	.1%
8	1.6383	6103	.01%

Since R_1 , the input resistor, must be at least 1K (a gain-of-10 input), if R is to be at least 1.5K, the best configuration is the sixth entry, with a maximum coefficient setting of 3.2767. This enables R_1 to be 1K and R to be 2.0514K.

After considering all of the compromises, it was decided to design a digital attenuator containing 14 bits with a maximum coefficient of 3.2767 with .02% resolution. One can accomplish this by using a 15 bit binary counting scheme and ignoring the least significant bit. A ladder network with $R = 2051.4$ ohms and an input-output accuracy of $.01\% \pm 5$ ppm/ $^{\circ}\text{C}$ was selected as the attenuator network.

A significant monetary savings can be realized by taking advantage of the fact that the accuracy of the least significant bit resistors of the ladder has very little effect on the transfer function. Thus a 14 bit ladder network can be constructed from two 7 bit ladder networks, one of the desired accuracy and one of a lower accuracy. This approach can be extended such that several ladders of varying accuracies are used. A computer program was written to perform an error analysis of a general ladder network, thus providing a tool for analyzing ladder network combinations.

When a coefficient greater than 3.2767 is required, a free amplifier must ordinarily be committed. It is possible, however, to parallel two attenuators, which adds their separate coefficient settings.

To improve network compromises, some digital attenuator systems associate an amplifier with each attenuator.⁵ If the additional cost of such an amplifier is accepted, it would seem desirable to switch the feedback

network rather than the input network, so that the amplifier offset and noise are not amplified along with the signal (Figure 7).

The Switches

Ladder networks (Figures 5a and b) require SPDT switches, which are somewhat more expensive than SPST switches. These switches may be realized either by electronic switching or relays.

FET electronic switches are very fast and are probably sufficiently accurate for slow analog computers, but the low impedances associated with a fast repetitive computer make the switch impedance significant. This non-negligible forward resistance may necessitate periodic adjustment of the resistors in the most significant bits of the ladder network. An alternative, as noted earlier, is to use error feedback to compensate for adjustments that may have been necessitated by the switch impedances (Figure 8).

Reed relays have very low ON impedance and are generally less expensive than high quality electronic switches, but they are much slower. One relay settling time is from 3 to 5 milliseconds, while an electronic switch can be operated at speeds in the microsecond region. Also, relays are mechanical devices, but since they can be operated "dry" (with the contacts not carrying

Figure 7. Simple Version of a Summing Amplifier
with Switched Gain

Figure 8. Simplified Block Diagram of a Digital Attenuator Employing Error Feedback

current), their expected lifetime is quite acceptable (about 100,000,000 operations).⁶

Relays do offer an additional advantage; they are available in a form that employs magnetic latching, thereby making the relay not only a switch but a memory device as well. Magnetic latching relays permit the relay-coil power to be turned off unless the analog computer is in the POT SET mode. This eliminates considerable power consumption, with the attendant heat dissipation, at only slight additional cost. The freedom to ground the relay-coil lines in the COMPUTE mode should also reduce digital noise in hybrid computers.

It should be stressed that, while the 3 to 5 millisecond settling time for a typical reed relay, plus the address and transfer from memory time, is still not prohibitive, parallel addressing of 14 reed relays each in 100 different attenuators would be very cumbersome.

Memory and Addressing System

Since a digital attenuator must retain the desired coefficient after setting, it must have memory. This can be achieved several ways. One alternative, as mentioned earlier, is the use of magnetic latching relays and a single relay driver for all relays. While this technique is undoubtedly the least expensive, it is relatively slow,

probably requiring 7 seconds or so to set 100 attenuators. What is worse this technique requires separate addressing of each relay of each attenuator.

No doubt the fastest technique would be to use flip-flops for memory and electronic switches for analog switching. This would permit 100 attenuators to be set in a few milliseconds at most, but we would be forced to contend with the finite ON impedance of the electronic switches.

A compromise between the two aforementioned techniques eliminates many of their disadvantages. It is the use of a flip-flop as the memory element together with a reed relay as the switch (Figure 9). This technique enables the digital control system to set each flip-flop in about 10 microseconds and then continue on to the next attenuator, without having to wait for each relay to settle. Using this technique, all attenuators can be set in little more time than is required to set a single relay. This system is, in fact, so fast that it becomes possible to combine the relay-driving flip-flops for each attenuator into a shift register with serial input. This greatly simplifies the digital attenuator's addressing scheme, requiring only one line per attenuator instead of 14 to 16, thus greatly reducing the cost (Figure 10).

At a shift rate of 100KC and a relay settling time of 5 milliseconds, 100 attenuators can be set in only 20

Figure 9. Selected Attenuator Scheme

(a) Parallel Addressing--14 lines and 14 gates to every attenuator

(b) Serial Addressing--only one gate and one line to each attenuator

Figure 10. A Comparison of Serial and Parallel Addressing

milliseconds--while the computer operator is moving his hand from the POT SET switch to the COMPUTE switch.

A further refinement of the above technique once again uses magnetic latching relays, so that in the COMPUTE mode the power to the flip-flops driving the relays can be disconnected. This also permits the memory to be retained even if the computer power is cut off; and, as mentioned earlier, this helps to reduce both digital noise and excess heat.

The Control Logic

Each digital attenuator must be capable of being set by both the digital computer and the manual coefficient-setting network on the computer control panel. Manual setting favors BCD weighting of the digital attenuator network, while most digital computers favor binary weighting. Since the use of BCD weighting requires three additional bits per attenuator and thus three more relays per attenuator, binary weighting is much less expensive for any large number of attenuators. Therefore, binary weighting was chosen.

The selection of a binary weighting scheme necessitates the use of a binary buffer register. When the digital computer is in use, stored addresses and coefficient settings are transferred in parallel to the buffer register from the computer input/output bus. The addressing tree

opens the logic to the correct attenuator, and then the coefficient setting is shifted serially into that attenuator.

When the manual coefficient-setting network is in use, the decimal coefficient, set on BCD switches, must first be converted to binary before it can be transferred into the buffer register. To facilitate this conversion the manual BCD switches are used to preset a BCD counter. This counter then counts the correct preset number of clock pulses, at a 100KC clock rate, into the same binary counter/shift buffer register that accepts parallel entry from the digital computer input/output bus (Figure 11). After the preset BCD counter counts to zero the contents of the buffer register is shifted, as before, into the attenuator, which is now addressed by the manual address selector on the control console.

Several switches must be made available to the operator besides the normal POT SET mode control switch. One switch must provide a selection of either the MANUAL or the AUOTMATIC attenuator setting modes. If AUTOMATIC is selected, then the operator must push a pushbutton switch to initiate the computer program. After all the attenuators have been set, the ATTENUATOR SETTING indicator light goes out. If MANUAL is selected the operator must set the correct address and desired coefficient on the BCD switches

Figure 11. Control Schematic

and then push the pushbutton switch which initiates the manual setting routine.

The counter/shift buffer register is used for both AUTOMATIC and MANUAL coefficient setting, but functions differently in each mode. In the AUTOMATIC mode, the register accepts parallel information from the digital computer output bus and then shifts the information serially to the correct attenuator. In the MANUAL mode, the register accepts and counts clock pulses until the preset BCD counter reaches zero; then the register contents shift serially into the addressed attenuator. To implement these changes, a set of logic gates controls each individual flip-flop in the buffer register. These gates are controlled by the TRANSFER ENABLE, SHIFT ENABLE, and COUNT ENABLE signals shown in the simplified diagram of Figure 12.

The control signals for both the MANUAL and AUTOMATIC modes are compared in Figure 13. Note that in either mode the last pulse resets all of the flip-flops in the control logic, and in the AUTOMATIC mode it also sends a signal back to the computer to show that the coefficient has been set. Appendix A contains a schematic diagram of a typical digital attenuator card.

Figure 12. Simplified Timing Logic

(a) Timing for manual mode

(b) Timing for automatic mode

Figure 13. Timing Diagrams

Checking Attenuator Settings

One matter still to be considered is that of checking attenuator settings. Sufficient checking of digital-computer-set coefficients is readily incorporated into the normal digital-computer-controlled static-check routine.⁷ This routine is fairly slow, but it need only be run as part of normal static-check procedure. The digital computer can be programmed to provide a printout of both the desired value of each program variable and the recorded value, and can detect any discrepancy. When a discrepancy does occur a simple digital computer sub-routine can be used to test the attenuators involved to determine which particular relay has failed.

Each attenuator network is equipped with relays which connect 10 volts to the input and a linkage D/A converter and/or the computer digital voltmeter to the output whenever the computer is in the MANUAL POT SET mode. The BCD switches for the address establish these connections, which are interrupted as soon as the coefficient set pushbutton is energized, and reconnect only after the attenuator has been set. In the MANUAL POT SET mode, each attenuator setting is read on the digital voltmeter as soon as the attenuator is addressed. The mode-control logic timing is shown in simplified form in Figure 13.

Construction

This digital attenuator system has been built, as described, at the University of Arizona's Analog/Hybrid Computing Laboratory. The prototype digital attenuator card was custom made, while the control logic was implemented with Computer Controls Corporation general purpose S-Pac logic elements.

A photograph of the attenuator card (Figure 14) shows to what extent the physical size of the card depends on the reed relays. Magnetic latching relays are now available in TO-5 cans. An attenuator card implemented using these relays and integrated flip-flops would be so small that it could be plugged directly into the rear of a standard analog-computer patchbay, thus doing away with all analog signal wiring that is necessary between potentiometers and the patchbay.

Figure 14. Photograph of Attenuator Card

TESTING AND RESULTS

Tests were conducted to determine the setting speed, static accuracy, and frequency response of the typical attenuator-amplifier combination shown in Appendix

A. The results were as follows:

Setting time, extrapolated to 200 attenuators	20 msec
Static Accuracy	0.02%
Phase-Shift Error at	
100 cps	--
1K cps	0.2%
10K cps	0.5%
20K cps	1%

Comparison with phase-shift measurements for gain-of-1 and gain-of-10 amplifiers indicate that the phase-shift error is primarily due to the amplifier in a fast low-impedance computer; however, in a "slow" analog computer the stray capacitances associated with the higher impedances will tend to cause more phase-shift error than the amplifier.

In the low-impedance computer, the phase-shift errors of the attenuator-amplifier combination was found to be almost exactly the same as that of the corresponding potentiometer-amplifier combination.

APPENDIX A

SCHEMATIC OF ATTENUATOR CARD

R = 2.0514K   C = 100pf
R1 = 1.5K   D--1N4009
R2 = 22K   Q--2N3638

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