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PUNCH-THROUGH SPACE-CHARGE LIMITED LOADS

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PUNCH-THROUGH SPACE-CHARGE LIMITED LOADS

by

Ali Abdalkareem Musallam

A Dissertation Submitted to the Faculty of the DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

In Partial Fulfillment of the Requirement For the Degree of DOCTOR OF PHILOSOPHY

WITH A MAJOR IN ELECTRICAL ENGINEERING

In the Graduate College

THE UNIVERSITY OF ARIZONA

1987
As members of the Final Examination Committee, we certify that we have read the dissertation prepared by Ali Abdulkareem Musallam entitled Punch-Through Space-Charge Limited Loads and recommend that it be accepted as fulfilling the dissertation requirement for the Degree of Doctor of Philosophy.

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Final approval and acceptance of this dissertation is contingent upon the candidate's submission of the final copy of the dissertation to the Graduate College.

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ABSTRACT

There are several important semiconductor devices in which the transport of carriers is controlled by punch-through space-charge effects. Examples include the Bipolar Mode Static Induction Transistor (BSIT), ultrasmall Punch-through MOSFETs, and BARITT diodes for microwave applications. The development of punch-through space-charge type of devices is a technology motivated by the demanding high density among the IC chips.

This dissertation discusses a device which operates in a punch-through condition with space-charge control of currents. It is a two terminal device, which could be fabricated with no deviation from today's technology. The device structure is simple, with two n⁺ or p⁺ regions formed in p⁻ or n⁻ substrate, respectively. Punch-through space-charge limited structures both n⁺p⁻n⁺ and p⁺n⁻p⁺, were simulated using a general one-dimensional semiconductor device performance simulation program GESIM1 for dynamic and static analysis. The results of simulation show that the potential barrier height decreases with increasing applied potential and with a reduction of the spacing L between the n⁺ diffusion in an n⁺p⁻n⁺ structure. The resistance increases as the spacing L is increased.
A two-dimensional analytical model of carrier transport in the device was developed. This model accounts for surface effects as well as the space-charge limited flow. Also, a one-dimensional model that includes mobile carriers effects on the device operation. Structures of various configurations were fabricated and tested. Electrical evaluations of these structures provided large value resistors in a remarkably small area compared to traditional integrated resistors. The resistance was observed to increase with the spacing $L$ and with the resistivity of the starting substrate. These punch-through space-charge limited loads should have applications as an alternative approach for integrated resistors in high-speed VLSI applications. They can provide very small area, large value resistors based on the space-charge limiting action of the device. The range of resistance value is large, and small dimensions lead to small capacitance and fast switching times.
CHAPTER 1

INTRODUCTION

The desire to increase the density of semiconductor devices per Integrated Circuit (IC) chip has advanced its complexity from small-scale integration (SSI) to medium-scale integration (MSI), then to large-scale integration (LSI), and then to very-large-scale integration (VLSI). The topography of very large scale integrated (VLSI) circuits is characterized by narrow lines with fine pitch, near-vertical steps, thin gate dielectrics, and shallow junctions. The advancement of IC complexity and packing density is summarized in Fig. 1.1. Curve (a) shows the exponential growth of the number of components per IC chip, while curve (b) shows the exponential decrease of the minimum device dimensions.

The main advantage of such a decrease in device dimensions is that the intrinsic switching time in MOSFETs, for example, decreases linearly (The intrinsic delay is given approximately by the channel length divided by the carrier velocity). However, shrinking device dimensions laterally as well as vertically causes some semiconductor devices to attain an undesired punch-through condition where
Fig. 1.1 Curve (a): Exponential Growth of the Number of Components per IC Chip. (After Moore.)

Curve (b): Exponential Decrease of the Minimum Device Dimensions.
the transport of carriers is controlled by punch-through space-charge effects.

Recent research shows that punch-through space charge devices can be used as loads. Due to device geometry scaling, low current levels are required; therefore, large valued resistors are essential. Diffused or implanted IC resistors consume large areas of the IC chip, which limits the packing density. Therefore, it is desirable to replace such resistors. Two terminal punch-through devices can be used as non-linear loads which offer large resistance values in a reasonably small area. For illustration, a numerical example is given below.

A comparison of a 120.0 kΩ punch-through device, also called a punch-through space-charge limited load (PTSCLL), with a 120.0 kΩ Dogbone diffused resistor using 1 μm geometries gives the results shown in Fig. 1.2. Assuming that, 80.0 Ω/square, (Emitter) Phosphorous doped region defines the PTSCLL and 1.5 kΩ/square, (Base) Boron doped region defines the dogbone resistor, the PTSCLL is orders of magnitude smaller than the dogbone resistor. Besides the reduced area, the PTSCLL also has less sidewall capacitance.
Fig. 1.2 Comparison of Diffused Integrated Resistor with Space-Charge Limited-Load (SCLL) Using 1 µm Geometries.
1.1 Punch-through Phenomena and Devices

A brief review of the impact of punch through on devices is presented in this section. If the spacing between the drain and source regions of a MOSFET is sufficiently small and the resistivity of the substrate on which the device is fabricated is sufficiently high, the depletion region can affect operation. This region is associated with the reverse-biased drain-substrate junction and can spread with increasing drain voltage. It will eventually touch the depletion region associated with the source-substrate junction. This condition is commonly referred to as "punch-through", and is illustrated in the cross-sectional view of a silicon n-channel MOSFET shown in Fig. 1.3(a). This is an undesirable result usually avoided.

Furthermore, this condition will occur even when the MOSFET is in inversion, where the gate bias voltage is higher than the threshold voltage \( V_T \) (formation of a surface electron inversion layer). Directly below the inversion layer, the depletion region can extend from drain to source. In such a situation, the applied gate voltage will be able to modulate the space-charge limited current from drain to source and the observed drain-to-source current will consist of two components: the usual drift current flowing through the inversion layer and the (injected) space-charge limited
Fig. 1.3 Cross-Sectional Representation of an n-Channel MOSFET
current flowing through the depletion region (i.e. through the bulk of the p-substrate in the case of an n-channel).

Moreover, if the gate bias is much smaller than the threshold voltage $V_T$ (transistor is off), accumulation of carriers at the surface near the source junction occurs and punch-through will take place for large drain bias. In this situation only one component of drain current will be observed; the space-charge current flowing through the bulk. This state is illustrated in the cross-sectional view of a silicon n-channel MOSFET shown in Fig. 1.3(b), and again is undesirable but may be present.

In addition when the base width of a bipolar junction transistor (BJT) is reduced to submicron dimensions, and the base conductivity is decreased in order to increase the transistor gain, it becomes increasingly likely that the collector-base space-charge region may reach through to the emitter-base space-charge region completely depleting the base region, again an undesirable punch-through condition.

In some semiconductor devices punch-through conditions are very desirable. Example include the BARITT (Barrier injection Transit Time) diode constructed of a semiconductor material sandwiched between two metal contacts, the DOVETT (Double Velocity Transit Time) diode which has an n+-p-n-n+ configuration, and another rather interesting semiconductor device, the Static Induction
Transistor (SIT) which is very similar to the Junction-Field-Effect Transistor (JFET) with a shorter channel length. It exhibits a non-saturating (triode-like) I-V characteristic. Table 1-1 illustrates schematically the cross-section and I-V characteristics of some semiconductor devices where punch-through space-charge-limited flow provides the main control of carrier transport.

1.2 Historical Background

The theory for Punch-Through Space-Charge Limited (PTSCL) current was given by [Mott and Gurney, 1940] where they developed the Square-Law nature of space-charge-limited current in a gap type semiconductor structure. Because of this square-law nature, one would expect a transition from the saturating pentode-like characteristics of conventional MOS transistors to triode-like characteristics dominated by the SCL current as the channel length becomes smaller. This transition has been theoretically predicted by [Geurst, 1966], and [Rittner and Neumark, 1966 and 1967] and has been observed in thin-film silicon-on-sapphire MOS structures by [Zuleeg, 1966] and [Hagon, 1966].

The SCL mechanism was reported as a controlling mechanism (i.e., control of the potential barrier height in order to modulate the injection of carriers toward the adjacent junction) in Shockley's Analog Transistor [1952]
Table 1.1 Schematic and I-V Characteristics of Some Examples of Semiconductor Punch-Through Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>Structure</th>
<th>I-V Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>BJT</td>
<td><img src="image" alt="BJT Schematic" /></td>
<td>$I_c$</td>
</tr>
<tr>
<td>BARITT Diode</td>
<td><img src="image" alt="BARITT Diode Schematic" /></td>
<td>$I_B = \text{constant}$</td>
</tr>
<tr>
<td>SIT</td>
<td><img src="image" alt="SIT Schematic" /></td>
<td>$I_D$</td>
</tr>
<tr>
<td>DOVETT</td>
<td><img src="image" alt="DOVETT Schematic" /></td>
<td>$I$</td>
</tr>
</tbody>
</table>
and Teszner's short channel FET [1964], Richman's MOS Transistor [1969] where he also reported that the space-charge-limited current becomes appreciable only when the transit time of the injected carriers $t$ is shorter than their relaxation time within the gap region $\tau$. That is,

$$t = L/v_n = L^2/\mu_n V_D$$

(1.1)

where $v_n$ is the velocity of the injected electrons and is a function of distance, and $\mu_n$ is their mobility within the gap region. The SCL mechanism was also reported as a controlling mechanism in Nishizawa's SIT Transistor [1975] and Ohmi's punch-through Transistor [1980]. A lateral version of the punch-through Transistor was also published by [Wilamowski and Jaeger, 1982]. The space-charge-limited current flow has been observed to acquire a nonlinear characteristics with the operating applied bias voltage [Mott and Gurney, 1940]. Also in 1951, Watanabe and Nishizawa published the results of analyses of the 2-, 3/2, and 1-power space-charge conduction law in the injection-type diode [Watanabe, et al., 1951], while [Shockley, et al., 1953] and [Dacey, 1953] reported individually the 2-power and 3/2-power law.

Another type of punch-through mechanism has been observed by [Ratnam and Bhattacharyya, 1982] as a result of their studies of the dc characteristics of an ion-implanted Buried Channel MOSFET (BCMOSFET). They have reported that
for a suitable bias at the gate, hole accumulation takes
place at the Si-SiO₂ interface for a p-channel BCMOSFET and
an "accumulation-punchthrough" mode of operation is
possible. This condition can be useful in designing
paristatic CCD's where the charge transfer is in the twin

The Junction Gate Static Induction Transistor (JSIT)
[Nishizawa, et al.,1975], [Nishizawa,1977], [Nishizawa and
Yamamoto,1978], and [Mochida, et al.,1978] can be easily
designed for normally off device called a bipolar mode SIT
(BSIT) with a saturating I-V characteristic [Nishizawa, et
al.,1982]. In this case it is required that the gate to gate
spacing and the impurity concentration must be designed to
realize the complete pinch-off of the channel due to the
gate to channel built-in voltage. Moreover, the ratio of
the channel length to the gate to gate spacing is required
to be larger than 0.7 in order to establish a potential
barrier in the channel even when a certain drain voltage is
applied. This ratio must be increased to increase this
blocking drain voltage [Ohmi,1980], [Nishizawa, et
al.,1980]. Sensitivity of performance of the BSIT to
process variations has been discussed in [Stork and
Plummer,1981]. Speed performance of the BSIT is published in
[Nishizawa, et al.,1979] where it is called Schottkey SITL.
A detailed theory of SCL for various devices is given in
[Kim and Yans,1970], [Mattson and Wilamowski,1983].
1.3 Scope of the Work

Designers of semiconductor devices usually regard punch-through as an undesirable effect which is to be avoided by all available means. However, when carefully controlled, the punch-through current in a short channel MOSFET for example, may be used to advantage. An approach to FET design based on controlled punch-through current offers a possible alternative to scaling methods [Dennard, et al., 1974], [Brews, et al., 1980], [Fichtner, et al., 1983] commonly used for down-sizing MOSFETs to submicron dimensions. These scaling techniques involve scaling down the vertical dimensions (e.g., gate insulator thickness, junction depth, etc.) to avoid short-channel effects caused by horizontal dimensions scaling.

The use of ion-implantation in the fabrication of small geometry semiconductor devices has been confirmed [Dennard, et al., 1974] to offer a significant improvement in their design in addition to the controllability and preciseness of such processing technique. Furthermore, enhancement of the operating range of submicron punch-through MOSFETs has been demonstrated by [Grossman, Hwang and Fang, 1984]. This was achieved by introducing a significant and controllable barrier-limited component of current through the placement of a heavily doped layer underneath the conducting channel as illustrated in Fig. 1.4.
Fig. 1.4 Short-Channel MOSFET with a Deep p⁺ Implant.
Another type of semiconductor device mentioned in the previous sections, the Static Induction Transistor (SIT), Fig. 1.5, was invented by Nishizawa in 1951. The SIT operates under punch-through conditions and accordingly, exhibits triode-like characteristics. The mechanism of operation of the SIT is the control of the potential barrier height in order to modulate the injection of carriers toward the drain electrode. The SIT provides the maximum operating limits of both the high speed field effect transistor (FET) and the high speed Bipolar Transistor (BPT).

The SIT has been characterized by high input impedance, low output resistance, high transconductance, and negative temperature characteristics [Plotka and Wilamowski, 1981]. Fabrication of SIT's has been realized in the form of high frequency and high-power transistors [Nishizawa and Yamamoto, 1978]: 40 W at 200 MHz and 10 W at 10 GHz. SIT's are widely used in microwave applications but seldom in integrated circuit construction [Nishizawa and Wilamowski, 1977].

The conventional SIT structure illustrated in Fig. 1.5 can be designed to give a saturating I-V characteristics by choosing proper channel dimension and impurity concentration in the channel such that there exists a potential barrier between the source and the drain without an applied bias voltage. This device is called the Bipolar Mode Static Induction Transistor (BSIT). The BSIT has been
Fig. 1.5 Cross-Section of Static Induction Transistor, n-Channel/p-Channel.
proved experimentally to be characterized by: low drain voltage for the onset of current saturation, i.e., low impedance [Nishizawa, et al., 1978], high current gain, high current density, and high transconductance irrespective to relatively low impurity concentration in the channel, and the operational principle of BSIT is described in [Nishizawa, et al., 1980]. The BSIT has been applied to SIT logic (SITL) having I²L (SITI²L) [Nishizawa and Wilamowski, 1977] and ISL circuit configuration (SITSL) [Nishizawa, et al., 1979], which have been demonstrated experimentally to exhibit excellent power-delay characteristics.

Modeling of such devices to upgrade the understanding of their physical behavior is tempting. However, one-dimensional analytical modeling is not justifiable due to the many directional effects that arises from scaling-down geometries and technological aspects involved in the fabrications of these devices. Therefore, the need of two- or three-dimensional modeling techniques is of concern. But, two- or three-dimensional analytical techniques may not be feasible and one usually drifts into the use of numerical computations as has been the case in analyzing the conduction mechanism underlying the triode like characteristics of a very-short channel MOSFET using a two-dimensional computer program in order to solve Poisson's equation and the current-continuity equation taking also the
effect of carrier velocity saturation into account [Dang and Konaka, 1980].

When analysing the nature of the conduction mechanisms in semiconductor devices, two fundamental governing equations, Poisson's equation and the current-continuity equation are solved. Because of the complex nature of these two fundamental equations, and the complexity of device physics, exact solutions are seldom feasible. However, numerical computer computations can be used as a tool for solving such complex equations with, of course, some certain degree of approximations.

Analytical solutions of these aforementioned equations demand certain approximations concerning device behavior in order to simplify the mathematics and hence provide analytical models for potential, electric field, etc.

One common approximation in semiconductor device theory is called the depletion approximation.

Features of the depletion approximations can be characterized as follow:
1) assume complete ionization in the depletion region.
2) neglect the injected mobile carriers.
3) well defined boundaries of the space-charge depletion region, i.e., idealization of the charge distribution at the metalurgical junction.
These assumptions are usually used with Poisson's equation in order to develop explanations of device performance.

Because of these assumptions, depletion approximations are not qualified for use when analyzing devices operating in a punch-through condition, because the mobile carrier density injected into the drift region (punch through channel) may be comparable or greater than the ionized impurity density in the drift region, therefore it cannot be neglected. Moreover, the carrier mobility is a function of the field. Hence, it is required to have a knowledge of the exact form and value of the carrier mobility and impurity doping profile.

Summarizing, semiconductor devices are being designed smaller and smaller to cope with the needs for higher speed and higher density in very-large-scale integrated circuits (VLSI's). Beside important technological problems many physical problems inherent in very-short channel devices such as their operating mechanism and hot electron effects limit device understanding and design. The operating parameters such as the electric fields and potentials are multidimensional. Calculations of such parameters using one-dimensional analysis and the depletion approximations gives very poor modeling. An alternative to such calculations usually involves computer numerical
simulation [Wilamowski, Mattson and Staszak, 1984], [Sze, 1981].

Therefore it is the purpose of this work to describe new methods for analyzing and modeling punch-through semiconductor devices to overcome the weakness of depletion approximations. This work provides an exact analytical one-dimensional solution of Poisson's equation without simplifying assumptions as well as a quasi-two-dimensional analytical solution of Poisson equation including short-channel effects and surface charges effect. These topics are presented in Chapter 2.

In addition a new application of a diode which operates in a punch-through condition with space-charge control of currents is presented. The structure is simple, with two N+ or P+ regions formed in P- or N-substrate, respectively. These punch-through diodes should have applications as a replacement for integrated resistors in high-speed VLSI applications. They can provide very small area, large value resistors based on the space-charge limiting action of the device. Thus, they could be called punch-through space-charge limited-loads (PTSCLL). The range of the resistance values is large in a very small area compared to integrated resistors. Small dimensions lead to small capacitances and fast switching times. This device was simulated using a general one-dimensional semiconductor device simulation program GESIM1 for dynamic and static
performance. Structures with various configurations were fabricated and tested. Results of the computer simulations, the experiments and the theoretical aspects of the device are all presented in Chapter 3. Finally, in Chapter 4 the results are summarized and the practicality of using the PTSCLL for VLSI applications is discussed. Thus, this dissertation makes two contributions to the theoretical understanding of space charge limited current flow in semiconductor devices as well as providing detailed theoretical and experimental information about a new silicon two terminal device which will be useful as a load in VLSI circuits. The device called a Punch-through Space Charge Limited Load (PTSCLL) can provide large value resistors in small volumes. They can be fabricated during standard bipolar or MOS silicon processing steps. They also emit light at high current density levels which may be useful in certain applications.
Continued evolution towards VLSI circuits demands device structures which offer high performance, but at the same time electrical characteristics in such devices must be reasonably tolerant of process perturbations. Good performance in terms of large transconductance, fast switching speed, and small physical area are clearly desirable. Such characteristics, however, should not be sought at the expense of reproducibility and sensitivity of device parameters to process variations.

The fabrication of small-geometry devices requires the use of micrometer and submicrometer technology (fine-line technology). This fine-line technology involves various processes such as x-ray lithography, multi-level resist, reactive ion etching, etc., which can create damage at the interface. Accordingly the effective inversion layer mobility changes and the need for device parameter modeling can be seen. Also, as the lateral device dimensions are reduced, the carrier-transport mechanisms in the device changes and the charge-neutrality is perturbed. For instance, if the doping concentration in the silicon substrate is not sufficiently high, punch-through can occur.
in the channel of MOS devices for a small applied bias voltage. Consequently, the current transport mechanism become space-charge limited. Furthermore, as lateral dimensions become comparable to the vertical dimensions, problems become two dimensional. There are a number of two-dimensional numerical computer programs available which determine the device parameters reasonably accurately. However, such analyses are not adequate for the application to statistical modeling in process diagnosis due to the requirement of a significant computation time. Also, a numerical analysis does not allow one to see the physical mechanism involved. Therefore, two-dimensional analytical models of device performance as a function of the fabrication parameters and operating conditions are desired. This chapter will address the effects of device structural parameters, process parameters and operating conditions on the transport mechanisms of carriers involved in Bipolar and MOSFET devices. Also, one-and-two-dimensional analytical models for such devices will be presented.

2.1 Occurrence of Punch-through

When discussing the effects of parameters (structural, process and bias) on devices performances, it is helpful to divide them into two broad categories: MOSFET devices and Bipolar devices.
2.1.1 MOSFET Devices

Since the maximum frequency of operation of an insulated-gate field-effect transistor is directly proportional to the ratio of its transconductance to the active channel capacitance from gate to channel neglecting parasitic capacitances, it follows that the maximum frequency at which the device will operate may be increased by decreasing the channel length. This will both increase its transconductance and decrease the active channel capacitance. However, a punch-through condition can occur for small drain to source bias voltage when extremely small channel lengths are used. Furthermore, carrier velocity saturation effects will be observed in devices with very small channel lengths because of the high electric field strength that will result between source and drain under typical operating conditions.

To show the magnitude of a parameter's impact on device behavior, two separate cases will be examined:

a) channel length \( L \) and channel doping \( N \)

b) channel length and insulator thickness \( h \)

Of course, bias conditions are important in either case.

a) Effects of \( L \) and \( N_{BC} \)

It has been demonstrated experimentally that MOSFETs having a short-channel length and a high-resistivity substrate (low concentration) exhibit a non-saturation \( I-V \)
characteristic [Richman, 1969], where the current transport mechanism has been explained by space-charge-limited current. The drain voltage required to achieve punch-through for a MOSFET is related to the channel length $L$ and the impurity concentration of the substrate $N_{BC}$. A one-dimensional approximation predicts that

$$V_{pt} = \left(qN_{BC}L^2/2\varepsilon_S\right) - V_{bi} \quad (2.1)$$

where $V_{bi}$ is the drain-substrate built-in voltage, $\varepsilon_S$ is the dielectric constant of the substrate, and $q$ is the unit charge.

Figure 2.1 (a) and (b) show the I-V characteristics observed by Richman in MOS Transistors [1969]. As can be seen, there is a transition from pentode-like characteristics (Fig. 2.1a) of conventional MOSFETs to triode-like characteristics (Fig. 2.1b). This characteristic is dominated by the space-charge-limited current as the channel length is made smaller. On the other hand, the substrate concentration is seen from Eq. (2.1) to increase the drain punch-through voltage. If made very high, breakdown of drain-substrate junction would occur before reach-through of drain's depletion region to the corresponding source depletion region.
Fig. 2.1 Electrical Characteristics of a p-Channel MOSFET Structure Fabricated on a 40,000 Ω-cm n-Type Silicon Substrate. W = 50 mils, Tox = 2000A of SiO₂. [After Richman, 1969]
b) Effects of L and Insulator Thickness h

Authors [Geurst, 1966] [Newmark and Rittner, 1966 and 1967] have shown theoretically that the ratio of the thickness of the gate insulator to the spacing between the drain and source electrodes, \((h/L)\), plays a very important role in determining the output conductance of the device. This ratio will also determine the extent to which the space-charge-limited current will dominate the current-voltage characteristics. Neumark and Rittner extended the basic theory of Geurst. They showed that as the ratio \(L/h\) decreases, the transition from the saturating pentode-like characteristics of conventional MOSFETs to triode-like characteristics dominated by punch-through will be observed at lower values of drain voltage. In addition the output transconductance will increase. Their theoretical results are shown in Fig. 2.2. A plot of drain current vs. drain voltage with \(\beta\) being a parameter is shown. \(\beta\) is proportional to the ratio \(L/h\) \((\beta = \pi L/h)\).

Experimental verification of these predictions can also be seen in Fig. 2.3. This shows the current-voltage characteristics associated with two p-channel MOSFETs. They have been simultaneously fabricated on a single n-type substrate with virtually the same values of channel length and channel width, but with different thickness of gate insulator. Note that the device fabricated with a relatively thin gate insulator exhibits saturating pentode-like
Fig. 2.2 I-V Characteristics of Single Gate Devices. 
(L = 10 μm, εr = 11, μ = 300 
300 cm²/v-sec) 

[After Neumark and Rittner, 1967]
Fig. 2.3 Current-Voltage Characteristics Associated with a p-Channel MOSFET Fabricated on a 7.5 Ω-cm n-Type Silicon Substrate. $L = 0.25$ mil.

[After Richman, 1969]

(a) $T_{ox} = 600$A of Silicon Dioxide Covered by 400A of Silicon Nitride.

(b) $T_{ox} = 15000$A of Silicon Dioxide Covered by 400A of Silicon Nitride.
characteristics, while the device fabricated with the much thicker gate insulator exhibits triode-like characteristics over the same range of drain current and drain voltage. Thus as $h$ is increased, $\beta$ decreases and the device characteristics revert to the space charge limited mode of operation.

2.1.2 Bipolar Devices

Conventional bipolar transistors continue to play an important role in modern high speed circuits because of their high transconductance. Overall performance improvements in speed and packing density have been achieved in recent years through improved fabrication technologies. Such improvements have included decreased parasitic capacitances, smaller series resistances, and smaller device area. These have been achieved through oxide isolation, composite masking, polysilicon contacts and interconnects, as well as other techniques. Intrinsic device speed has been improved through decreased basewidth. Continued reduction of bipolar junction transistor (BJT) basewidths ultimately results in punch-through from the collector-base junction to the emitter-base junction. Moreover, the base doping level is ideally very low in order to maximize the emitter injection efficiency $\gamma$. Therefore, the avalanche breakdown voltage of the collector-base junction is high.
However, collector-emitter punch-through can take place before the collector-base junction can avalanche.

The base region of diffused transistors is relatively heavily doped. The punch-through voltage is usually high. Therefore, the voltage limitation of diffused transistors is usually due to the avalanche breakdown of the collector-base junction and not to a collector-emitter punch-through condition.

2.2 Punch-through Space-charge

2.2.1 Mechanisms and Principles

A) In MOSFET Devices

Punch-through occurs when the drain depletion layer spreads out towards the source with increasing drain voltage, resulting in a field distribution along the drain edge and the source region which permits a finite injection of source majority carriers into the bulk depletion region where they are minority carriers. Conduction between source and drain then exists as a space-charge-limited current flow and tends to follow a square-low relationship at high current levels. This mechanism is characterized by a transition from a pentode-like to a triode-like I-V characteristic.

The effect of punch-through on the output characteristics of a 4.5 μm, p-channel device is shown in
Fig. 2.4. This figure illustrates the square law nature of the space-charge-limited punch-through current and the effect of gate bias on it. A practical definition for the punch-through voltage $V_{pt}$ must be based on the drain voltage at which a certain punch-through current flows. $V_{pt}$ is dependent on the current level chosen and on the gate bias as can be seen from Fig. 2.4. Further, practical measurement of an exact value of $V_{pt}$ for gate voltages above the threshold voltage is impossible due to the gate induced channel current which accompanies the punch-through current. Punch-through in an MOS transistor is a complex mechanism, influenced by the physical parameters of the device. Therefore, characterizing such a complex mechanism by defining a punch-through voltage $V_{pt}$ is not useful.

B) In Bipolar Devices

Punch-through occurs as increasing collector-base voltage causes the expanding collector-base junction space-charge region to meet the emitter-base junction space-charge region. This can happen if the BJT has a base region that is sufficiently thin and lightly doped. Punch-through is accompanied by a sharp rise in collector-emitter current caused by the high field across the thin base. It places an upper limit on the permissible $V_{CE}$. A schematic explanation is offered in Fig. 2.5. The dashed line in Fig. 2.5(b) shows the equilibrium potential profile for the $P^+N^+\text{BJT}$ of
Fig. 2.4 Effect of Punch-Through on the Output Characteristics of an Experimental p-Channel MOST. Reduction of Gate Voltage Well Below Threshold Does Not Eliminate Punch-Through Current for Large Drain Bias $V_{DS} (>20V)$. $L = 4.5 \, \mu m$, $N_{BC} = 5.4 \times 10^{14} \, \text{cm}^{-3}$, $T_{ox} = 0.14 \, \mu m$. 

Experimental Results (p-Channel)
Fig. 2.5 Punch-Through. (a) Physical Representation of a Thin-Base BJT. (b) Equilibrium (Dashed line) and Collector-Reverse-Biased (Solid line) Potential Profiles Showing Lowered Barrier at the Emitter Junction in the Latter Case. (c) Output Characteristics Observed in a BJT when Punch-Through Occurs.
the alloyed-junction type represented in Fig. 2.5(a). Potential barriers on either side of the base region tend to keep holes within the emitter and collector regions under these conditions. But with a reverse bias on the collector junction, its growing space-charge region interacts with the potential barrier in the base, reducing its height. Consequently, holes from the emitter pour over the barrier and are swept to the collector by the high field across the collector-junction space-charge region, with the current-voltage behavior shown in Fig. 2.5(c) as a result.

The availability of holes in the emitter region as a function of energy, for contributing to the punch-through current is described by

\[ i.e. \quad 1 - P(E) = \exp\left[-(E_F - E)/kT\right] \] (2.2)

where \( E_F \) is the Fermi energy and \( E \) is the hole energy. Because of Boltzmann factor in Eq. (2.2), hole availability increases exponentially.

2.2.2 Space-Charge Limited Flow

A) MOSFET Devices

To study the nature of the drain-to-source conduction mechanism for drain voltage beyond punch-through, it is worthwhile to neglect the effect of the insulated gate electrode by treating the simplified one-dimensional gap-type
semiconductor structure in Fig. 2.6. The structure consists of two parallel n+ regions of area A diffused into opposite sides of a high-resistivity p-type (∏) silicon substrate. The regions are separated by a distance, L. It will be assumed that the spacing L is sufficiently small, and the resistivity of the p-type region is sufficiently high, so that punch-through exists with the applied drain voltage $V_D$ equal to zero. The energy-band diagram for the structure is shown in Fig. 2.7.

Under punch-through conditions, the depletion region will extend throughout the p-type gap from $y=0$ to $y=L$. The depletion region charge will consist almost entirely of ionized acceptors and the free carrier concentration will be extremely small. Consequently, very little current would be expected to flow from "drain" to "source" with the application of small positive voltage $V_D$. However, electrons can be injected from the highly doped source region into the depletion drift region by Schottky emission. If L is sufficiently small, they can reach the drain electrode where they will be collected. Also, for extremely small values of L, it is possible for electrons to tunnel through the potential barrier. In either case, the electrons that are injected into the depletion region will create a negative space charge cloud in the gap from $y=0$ to $y=L$. The concentration of electrons will be largest near the injecting electrode at $y=0$ and decrease as y increases
Fig. 2.6 Simplified n⁺pn⁺ Gap Type Semiconductor Structure with Applied Voltage $+V_D$. 
Fig. 2.7 Energy Band Diagram Associated with Space-Charge-Limited Injection of Electrons across a Gap-Type Semiconductor Structure. (a) Zero Bias Condition. (b) Electron Injection with Applied Voltage.
across the drift region. The presence of the large concentration of negative charge in the space-charge region near \( y=0 \) will tend to limit the amount of additional electron injection from the source. Therefore, the total observed current across the gap region will be "space-charge-limited". The total drain to source space-charge-limited current can be assumed to be a drift current and is given by

\[
I_{SC\text{l}} = - n q v_n A \tag{2.3}
\]

where \( v_n \) is the velocity of the injected electrons in the \( y \) direction, \( n \) is injected electron concentration, \( q \) is the electron charge and \( A \) is the cross-sectional area. The electron concentration per unit volume, \( n \), and \( v_n \) will be functions of \( y \). Under steady-state conditions, the current density in the \( y \) direction must be constant from \( y=0 \) to \( y=L \), and this will require that the product of the electron concentration times the electron velocity be constant within this region. Since \( n \) is largest at \( y=0 \), the electron velocity there will be much less than that at \( y=L \) where \( n \) will be comparatively small. The electron velocity in the drift region, as a function of \( y \), will be related to the electric field in the \( y \)-direction.

\[
v_n(y) = - v_n E_y(y) \quad v_n < v_{sat} \tag{2.4}
\]
where $\mu_n$ is the mobility of the injected electrons in the gap region.

The electric field is related to the electron concentration through Poisson's equation. Assume the density of the ionized impurities in the drift region is small compared to the injected mobile electron carrier density in the same region.

Thus, Poisson's equation can be written as

$$ \frac{dE_y}{dy} = - \left( -\frac{qn}{\varepsilon_s} \right) $$  \hspace{1cm} (2.5)

or

$$ q n = \varepsilon_s \frac{dE_y}{dy} $$  \hspace{1cm} (2.6)

Substituting (2.6) into (2.3) yields

$$ I_{SCL} = -\varepsilon_S \varepsilon_n A \frac{dE_y}{dy} = \varepsilon_S \mu_n A E_y \frac{dE_y}{dy} $$  \hspace{1cm} (2.7)

Eq. (2.7) can be integrated and solved for the electric field. The result is

$$ E_y = - \left[ \frac{2(y I_{SCL} + C)}{\varepsilon_S \mu_n A} \right]^{\frac{1}{2}} $$  \hspace{1cm} (2.8)

where $C$ is constant of integration. The electric field is directed in the negative $y$-direction. It is maximum at $y=L$ and minimum at $y=0$. 
Since the magnitude of the electric field intensity is smallest at \( y=0 \) because of the large electron concentration there, we can assume the condition

\[ E_y(y=0) \approx 0 \quad (2.9) \]

substituting condition (2.9) into (2.8) yields, \( c=0 \) and Eq. (2.8) becomes

\[ E_y \approx - \left[ 2 \frac{y \ ISCL}{\varepsilon_s \ \nu_n \ A} \right]^{1/2} \quad (2.10) \]

the drain voltage can now be obtained by integrating \( E_y \) from \( y=0 \) to \( y=L \). Thus

\[ V_D \approx - \int E_y \ dy = L^{3/2} \left( 8 ISCL / 9 \varepsilon_s \nu_n A \right)^{1/2} \quad (2.11) \]

Equation (2.11) can be rearranged and solved for the space-charge-limited current resulting from the injection of electrons from the source. Hence

\[ ISCL = \frac{9 \varepsilon_s \ \nu_n \ A \ V_D^2}{8 \ L^3} \quad (2.12) \]

Similarly, for a gap-type semiconductor structure with p+ drain and source regions, the space-charge-limited current resulting from injection of holes from the source
region into the drift n-type region with negative applied drain voltage is given approximately by

\[
I_{SCL} = \frac{9 \varepsilon_s \mu_p A V_D^2}{8 L^3}
\]  

(2.13)

where \( \mu_p \) is the mobility of the injected holes in the gap region.

Now, it may be worthwhile to give a brief discussion of the effect of device parameters and operating conditions on the space-charge-limited current

1) Effect of \( L \) and \( N_{BC} \) on \( I_{SCL} \)

As can be seen from Eq. (2.12) or (2.13), the space-charge-limited current is a very strong function of the spacing between source and drain \( L \) (i.e., \( I_{SCL} = f(L^{-3}) \). A small change in \( L \) causes a very rapid change on \( I_{SCL} \). When \( L \) gets very large; the space-charge-limited current will vanish, and we are left with only drift current for punch-through MOSFET in the on-state. This basically is the transition from triode-like characteristics of the MOSFET to a pentode-like characteristics. The background substrate concentration controls the value of the source-drain punch-through voltage. This breakdown is either punch-through or avalanche breakdown depending on \( L \) and \( N_{BC} \). With punch-through space-charge-limited current will exist. It was
assumed that the injected carrier density was larger than the background thermally generated carriers. This simplifies Poisson's equation for calculating the drain voltage and hence the space-charge-limited current. If the two carrier densities are comparable the assumption does not hold and we should include both densities in Poisson's equation.

2) Effect of Gate Bias on $I_{SCL}$

In a MOSFET operating in punch-through the application of the gate voltage will affect the flow of current from drain to source. An inversion layer will be formed for gate voltages above the threshold voltage. Below this inversion layer, the punch-through generated depletion region will extend from drain to source. Therefore, two components of drain-to-source current will be observed, one component is the usual drift current flowing through the inversion layer, and the other component is due to the injected space-charge-limited current flowing through the depletion region.

Increasingly negative gate voltage for n-channel MOSFETs will reduce the drift component by depleting the surface inversion layer. For gate voltages which are lower than the threshold voltage of the device, the inversion layer will be depleted completely and only space-charge-limited current will flow from drain to source. As the applied gate voltage is even made more negative, it will
tend to retard the flow of injected electrons from source and the total observed space-charge current will decrease. For large negative gate bias, all surface space-charge-limited current will be eliminated by the effect of the high gate field. However, for lightly doped substrate, the depth of the drain depletion region will be quite large, and substantial amount of the space-charge-limited current will flow from drain to source by way of a path through the bulk of the substrate.

Thus, the application of large negative gate voltage in an n-channel MOSFET operating in punch-through will have a tendency to terminate the drift current flowing through the inversion layer by means of completely depleting the layer. Also, the gate voltage will diminish the space-charge-limited current by retarding the flow of the injected electrons from the source at the silicon surface. There will still be space-charge-limited current flowing through the bulk of the substrate due to punch-through. This current is far enough removed from the silicon surface to remain virtually unaffected by the gate field.

3) Effect of Substrate Bias on $I_{SCL}$

The application of a negative substrate-to-source potential can retard the punch-through related space-charge-limited current flowing through the bulk path and enable complete cut-off of this component of drain to source
conduction. The effect of a reverse (negative) substrate bias upon the drift component of the drain-to-source current is very small. Thus, under punch-through conditions, a reverse-biased substrate will act as a grid, retarding the flow of carriers injected from the source and thereby establishing cut-off of punch-through current components over a wide range of applied drain voltages.

B) In Bipolar Devices

Consider the p⁺n⁺p⁺ BJT of the alloyed-junction type represented in Fig. 2.8(a). We shall regard the p layers as being very heavily doped and the junctions between the n and p layers as being step discontinuities as shown in Fig. 2.8(b). Also, shown in Fig. 2.8(c), the equilibrium electrostatic potential profile for the structure with $V_{CE}=0$ (dashed curve) and $V_{CE}<0$.

It will be assumed that the base width $W_B$ is sufficiently small, and the resistivity of the n-type base region is sufficiently high so that punch-through (complete depletion of the base width) exists with the applied collector bias $V_{CE}$ equal to zero. Under punch-through conditions, the depletion region will extend throughout the base from $x=0$ to $x=W_B$. The charge in the depleted base will consist almost entirely of ionized donors, and the free carrier concentration will be extremely small. A negative collector voltage $V_{CE}$ will reverse bias the collector-base
Fig. 2.8 (a) Physical Representation of a Thin-Base BJT. (b) Excess Acceptor Concentration vs. Distance in the Thin-Base BJT. (c) Equilibrium (Dashed Line) and Collector-Reverse Biased (Solid Line) Potential Profiles Showing a Lowered Barrier at the Emitter Junction.
junction, while the emitter-base junction will be forward biased. The potential profile under bias conditions is shown in Fig. 2.8(c) (solid line). The potential barrier in the base tends to keep holes within the emitter region. An increase in $V_{CE}$ will reduce the base potential barrier height. Consequently, holes at the emitter side will pour over the barrier and be swept to the collector.

This conduction mechanism is controlled by the availability of holes. They can be associated with either thermionic injection, diffusion, or both. For further explanation see [Sze, 1981]. As $V_{CE}$ is increased in a negative direction the potential hump shown in Fig. 2.8(c) will decrease, and ultimately may vanish attaining a "flat band" condition. This corresponds to very large flow of holes through the depleted base region. The fast moving holes will create a large positive space-charge region in the depleted base. The presence of this space-charge cloud in the depletion region tends to limit the amount of additional hole injection from the emitter; therefore, the total observed current will become space-charge-limited due to moving mobile carriers, holes.

This physical situation can be analyzed in an approximate fashion by treating it as a capacitor problem. The incremental double layer involved consists of the emitter region as the negative plate and the moving positive charge in the base as the positive plate. Assuming that
the holes, \((P - P_0)\), are uniformly distributed through the base region, is a crude approximation but useful. But with this assumption we may apply the capacitor law to obtain:

\[
C = \frac{Q}{V_{CE}} = \frac{Aq(P - P_0)WB}{V_{CE}} \approx \frac{AqPWB}{V_{CE}}
\]

For a parallel-plate capacitor, the capacitance per unit area is given by

\[
\frac{C}{A} = \frac{\varepsilon_s}{WB} = \frac{qPWB}{V_{CE}}
\]

solve Eq. (2.15) for the injected carrier concentration. Hence

\[
p = \frac{\varepsilon_s V_{CE}}{qWB^2}
\]

The current is constant throughout the device and is given by

\[
I = qA\mu_p pE
\]

where \(A\) is the cross-sectional area, \(q\) is the unit charge, \(\mu_p\) is the injected hole mobility in the base, and \(E\) is the electric field, and is given as an approximation by

\[
E = \frac{V_{CE}}{WB}
\]
Substituting Equations (2.16) and (2.18) into (2.17) leads to the hole controlled space-charge-limited current. The square-law nature of this type of current is obtained. Thus

\[ I = A \mu_p \varepsilon_s V_{CE}^2 / W_B^3 \]  

(2.19)

2.3 Analytical Solutions of Poisson's Equation

The differential equations relating electrostatic potential, electric field, charge density, and carrier densities are nonlinear. Thus the analytical problem posed by the PN junction is difficult, even if we take the equilibrium condition of the simplest possible kind of junction. One method for overcoming this problem relies on the use of numerical analysis in order to accurately predict the electrical characteristics of semiconductor devices. Unfortunately, these equations usually require time-consuming numerical calculations with a computer.

An alternative method is to apply an initial simplifying assumption called the depletion approximation, which often makes an analytical treatment possible. The depletion approximation involves departures from an exact solution. Therefore, it is the purpose of this section to point out the shortcomings of the depletion approximation method when applied to small geometry semiconductor devices. Also presented is an exact one-dimensional solution of
Poisson's equation for vertical small geometry devices. Finally, a quasi-two-dimensional analytical solution of Poisson's equation for devices with scaled-down lateral dimensions such as short channel MOSFETs is presented.

2.3.1 Weakness of the Depletion Approximation

To visualize the charges "uncovered" near a PN junction, one can sketch them in heuristic fashion as shown in Fig. 2.9(a). Focusing now on the space charge \( \rho \), having the dimensions \( \text{c/cm}^3 \), we see that the resulting profile is shown in Fig. 2.9(b). The first assumption involved is the idealization of this charge-density profile with the result shown in Fig. 2.9(c). The second assumption is that the space-charge region has a negligible population of mobile carriers. The third assumption is complete ionization of the dopant concentration in the space charge region. These assumptions lead to the depletion approximation.

Consider the left-hand side of Fig. 2.9(c). Shown is an abrupt, well-defined boundary located at \(-X_0/2\) separating the left-hand neutral region from the region of donor-ion space charge. Since the actual boundary between the neutral region and the region of donor-ion charge is diffused, it seems harsh to idealize it into the form of a sharp boundary. Taken a step further logically, this approximation seems to require an infinite diffusion current
Fig. 2.9 Applying the Depletion Approximation to a Symmetric Junction. (a) Carrier Profiles with Heuristic Representation of Ionic Charges "Uncovered" by Depleted Carrier Populations. (b) Charge-Density Profile Consistent with (a). (c) Idealized "Depletion Approximation" Charge-Density Profile Corresponding to Actual Profile in (b).
of electrons from the left-side neutral region to the donor-ion space charge region at the boundary because of the large gradient in concentration according to Fick's first law. It states that the flux of a diffusing species is proportional to the negative of the concentration gradient:

\[ f = - D_p \frac{\partial p}{\partial x} \]  

(2.20)

The minus sign enters because a concentration increasing to the left leads to diffusion to the right. \( D_p \) is the diffusivity, diffusion constant, or diffusion coefficient, for holes and has the dimensions cm\(^2\)/sec.

By multiplying the particle flux by the charge on each particle, we obtain the current density

\[ J_p = - q D_p \frac{\partial p}{\partial x} \]  

(2.21)

and for electrons

\[ J_n = q D_n \frac{\partial n}{\partial x} \]  

(2.22)

Because the charge in this case is \(-q\) on each particle, the current density of electrons arising from diffusion is positive.

The right-hand side of Eq. (2.21) and Eq. (2.22), express the change of concentration with respect to space,
the x-component. The abrupt change of concentration for almost zero change in space leads to an infinite diffusion current density. Thus, the first assumption leads to infinite diffusion currents, but it can be used by recognizing that it is an assumption.

The depletion approximation does not accurately predict many of the effects seen in small geometry semiconductor devices. It does set many semiconductor problems aside in order to address a related, but mathematically, simpler problem. This is often done in addressing problems.

The problem of analyzing a linearly graded junction is more complicated than that posed by the step junction. When the depletion approximation is applied to this case, we effectively substitute an electrostatic problem for the portion of the actual problem residing near the junction. But for the region lying outside of this zone, we assume pure neutrality. For a better picture of the errors and problems inherent in this matter see the illustration shown in Fig. 2.10.

In conclusion, it may be worth pointing out some constraints under which the depletion approximations is not advisable to be used:

1) Small Geometry: when lateral device dimensions become comparable to the vertical dimensions, the problem becomes two or maybe three-dimensional.
Fig. 2.10 Equilibrium Profiles for a Linearly Graded Junction. (a) Depletion - Approximation and Actual (Dashed line) Charge-Density Profiles. (b) Approximate and Actual Electric-Field Consistent with (a). Potential Profiles Consistent with (a) and (b). The Approximate Profile (Solid line) is based on an Assumption of Neutrality Outside the Region of Thickness $x_0$, and on the Depletion Approximation within the Region. (d) Equilibrium Band Diagram for this Linearly Graded Junction.
The space charge region becomes comparable to the device dimensions.

2) Physical Mechanism: devices that operate under punch-through conditions, mobile carriers have to be included in the analysis of such devices.

3) High Level Injections: when carrier transport is by means of high level injection, nonuniform distribution of carriers occur such as in some special cases of BJT.

4) Nonuniformity of Dopants: junctions always have nonuniform distributions of dopants so mobility is no longer a constant, but varies slightly with position.

5) Hot-Electron: hot-electron conduction in some type of devices such as hot-electron transistors, sometime referred to as Tunnel Transistors, constructed of metal-insulator-metal-insulator-metal (MIMIM) can not be explained by the depletion approximation.

Nonetheless, the use of the depletion approximation in solving the continuity equation (Poisson's Equation) for
device characteristics still provides useful insight, in
spite of its shortcomings.

2.3.2 One-Dimensional Solution Including
Mobile Carriers Effects

In punched-through gap type of devices such as short
channel MOSFETs and BARITT diode, when the current is
sufficiently high such that the injected carrier density is
comparable to the background ionized-impurity density of the
depleted channel (GAP), the mobile carriers injected into
this region will influence the field distribution. The
depletion approximation is not suitable for solving
Poisson's equation as discussed in the last section.
Hence, the mobile carriers have to be included when
characterizing the depleted channel region. Consequently,
Poisson's equation can be written as:

\[ \frac{dE}{dx} = \frac{\rho}{\varepsilon_S} + \frac{J}{\varepsilon_S} v(E) \] (2.23)

where \( \rho \) is charge-density of the ionized impurities in the
gap region, \( v(E) \) is velocity of mobile-carriers and is a
function of the electric field in the gap region, and \( J \) is
the injected current density (function of applied voltage).
The first term in the right side of Eq. (2.23) accounts for
the background ionized-impurities in the gap region and
equal to \( qN_B/\varepsilon_S \), (assuming complete ionization), while the
second term on the right accounts for the injected mobile-
carriers assuming constant current flow through the drift region, i.e.

\[ J = q \, v(E) \, C_m \]  \hspace{1cm} (2.24)

where \( C_m \) is the concentration per unit volume of the injected mobile-carriers holes or electrons depending on the type of current carriers. Note that in order to have a constant current flow through the gap, the product \( v(E)C_m \) in Eq. (2.24) must be constant. However, \( C_m \) is a function of \( x \) and will be large near \( x = 0 \); the current carrier velocity there will be much less than near \( x = L \), where \( C_m \) will be comparatively small.

The mobile-carrier's velocity is related to the electric field through the relation

\[ v(E) = \mu E \]  \hspace{1cm} (2.25)

where \( \mu \) is the carrier's mobility and is a field-dependent also. An equation reported by Trofimenkoff [42] of the form

\[ \mu = \frac{\mu_0}{1 + E/E_s} \]  \hspace{1cm} (2.26)

where \( \mu_0 \) is the low field mobility, and \( E_s \) is the critical field given by the ratio of the scattering-limited
velocity to the low-field mobility. Equation (2.26) gives a good approximation to experimental measurements of the mobility as a function of the field. Substituting Eq. (2.26) into Eq. (2.25) and using the relation \( \mu_o = V_s/E_s \), we obtain an expression for the \( v - E \) relation (for silicon)

\[
v(E) = \frac{V_s}{1 + (E_s/E)}
\]

Substituting Eq. (2.27) into Eq. (2.23) and rearranging to have the form

\[
\frac{dE}{dx} = \frac{\rho}{\varepsilon_s} + \frac{J}{\varepsilon_s V_s} + \frac{JE_s}{\varepsilon_s V_s E}
\]

multiplying both sides of Eq. (2.28) by \( E \)

\[
\frac{dE}{dx} E = \frac{\rho E}{\varepsilon_s} + \frac{JE}{\varepsilon_s V_s} + \frac{JE_s}{\varepsilon_s V_s}
\]

factoring out \( JE_s/\varepsilon_s V_s \) from the right hand side of Eq. (2.29) and simplifying it to the form

\[
\frac{dE}{dx} E = \alpha (1 + \beta E)
\]

where
\[ \alpha = \frac{J}{\varepsilon S} \frac{E_S}{\varepsilon S} \]  
(2.31)

and

\[ \beta = \left( \rho V_S + J \right) / J E_S \]  
(2.32)

Introducing a variable \( s \) in Eq. (2.30) defined by

\[ s = \int \frac{dx}{E} \quad ; \quad ds = \frac{dx}{E} \]  
(2.33)

by substituting the second definition of Eq. (2.33) into Eq. (2.30), get

\[ ds = \frac{dE}{\alpha \left( 1 + \beta E \right)} \]  
(2.34)

Eq. (2.34) can now be integrated to find an analytical solution for the electric field as a function of the variable \( s \)

\[ E = \frac{1}{\beta} \left[ \exp \left( k_1 + \alpha \beta s \right) - 1 \right] \]  
(2.35)

where \( k_1 \) is a constant of integration and can be obtained from boundary conditions for the electric field.

Potential distribution can also be obtained from Poisson's equation as follows:
\[- \frac{d \phi}{dx} = E \]  
\hspace{1cm} (2.36)

or

\[- \frac{d \phi}{dx} E = E^2 \]  
\hspace{1cm} (2.37)

using the relation between \( s \) and \( x \) in Eq. (2.37) leads to

\[- \frac{d \phi}{ds} = E^2 \]  
\hspace{1cm} (2.38)

Equation (2.38) can now be integrated to obtain an analytical expression for the potential distribution as a function of the introduced variable \( s \).

\[- \phi \equiv V = \frac{1}{\beta^2} \left[ \frac{1}{2\alpha\beta} \exp(2k_1 + 2\alpha\beta s) \right. \]  
\[\left. - \frac{2}{\alpha\beta} \exp(k_1 + \alpha\beta s) + s \right] + k_2 \]  
\hspace{1cm} (2.39)

where \( k_2 \) is constant of integration and can be obtained from boundary conditions for the potential. The total thickness \( X(s) \) of the gap drift layer can be obtained by integrating Eq. (2.33), and adding a third constant to account for the difference between \( x \) and \( s \).
\[ \int dx = \int E \, ds \]
\[ = \frac{1}{\beta} \int [\exp(k_1 + \alpha \beta \, s) - 1] \, ds \quad (2.40) \]

Therefore
\[ X(s) = \frac{1}{\beta} \left[ \frac{1}{\alpha \beta} \exp(k_1 + \alpha \beta \, s) - s \right] + k_3 \quad (2.41) \]

\( k_3 \) is constant of integration and can be determined as follows:
At a certain position in the gap region from \( x=0 \) to \( x=L \), the variables \( s \) and \( x \) ultimately will be equal. Hence, we can pin \( s \) and \( x \) at the position zero of the gap, i.e.
\[ s \equiv x \equiv 0 \quad (2.42) \]

Substituting the condition in Eq. (2.42) into Eq. (2.41) and solving for \( k_3 \)
\[ k_3 = -\frac{1}{\alpha \beta^2} \frac{e^{k_1}}{e^{k_1}} \quad (2.43) \]

Substitute (2.43) back into eq. (2.41)
\[ X(s) = \frac{1}{\beta} \left[ \frac{1}{\alpha \beta} e^{k_1} [\exp(\alpha \beta \, s) - 1] - s \right] \quad (2.44) \]
The constants $k_1$ and $k_2$ can now be obtained with the aid of the boundary conditions at $x=0$ and $x=L$ corresponding to the potential distribution in Eq. (2.39). Having found $k_1$ and $k_2$, for a given total width of the drift region $L$ and a given ionized doping density $N_A$, we can use Eqs. (2.39) and (2.44) to obtain the I-V relation. The electric field also can be observed in Eq. (2.35).

To illustrate the above approach, we will arbitrarily choose boundary conditions for the potential in Eq. (2.39) and solve for $k_1$ and $k_2$. From the potential distribution illustrated in the schematic diagram shown in Fig. 2.11, the boundary conditions are

\[
\begin{align*}
-\phi(x) & = a_1 \\
& \bigg|_{x=0} \bigg|_{s=0} \\
-\phi(x) & = a_2 \\
& \bigg|_{x=L} \bigg|_{s=s_L}
\end{align*}
\]

Substituting Eq. (2.45) into Eq. (2.39), we have

\[
a_1 = \frac{1}{\beta^2} \left[ \frac{1}{2\alpha\beta} e^{2k_1} - \frac{2}{\alpha\beta} e^{k_1} \right] + k_2 \quad (2.46)
\]

\[
a_2 = \frac{1}{\beta^2} \left[ \frac{1}{2\alpha\beta} \exp(2k_1 + \alpha\beta s_L) \right]
\]

\[
- \frac{2}{\alpha\beta} \exp(k_1 + \alpha\beta s_L) + s_L \right] + k_2 \quad (2.47)
\]
Fig. 2.11 Typical Potential Distribution of a Gap Type Device (e.g., Bulk Barrier Diode).
Eliminating $k_2$ from Eq. (2.46) and substituting the result into Eq. (2.47) leads to an equation in terms of the constant $k_1$ and the boundary condition values. Hence,

$$a_2 - a_1 = \frac{1}{\beta^2} \left( \frac{1}{2 \alpha \beta} e^{2k_1} \left[ \exp(2 \alpha \beta s_L) - 1 \right] \right)$$

$$- \frac{2}{\alpha \beta} e^{k_1} \left[ \exp(\alpha \beta s_L) - 1 \right] + s_L$$  \hspace{1cm} (2.48)

We also have from Eq. (2.44) and the second boundary condition in Eq. (2.45) the following result

$$L(s) = \frac{1}{\beta} \left( \frac{1}{\alpha \beta} e^{k_1} \left[ \exp(\alpha \beta s_L) - 1 \right] - s_L \right)$$  \hspace{1cm} (2.49)

By rearranging Eq. (2.49) to obtain a solution for $k_1$ as a function of $s_L$. Therefore

$$e^{k_1} = \frac{\alpha \beta^2 L - \alpha \beta s_L}{\exp(\alpha \beta s_L) - 1}$$  \hspace{1cm} (2.50)

Equation (2.50) can be plotted for $e^{k_1}$ vs. $s_L$ with the current density as a parameter via $\alpha$ and $\beta$ as illustrated in Fig. 2.12. Furthermore, from this generated plot, we pick an arbitrary value for $e^{k_1}$ and find the
Fig. 2.12 Illustration Plot of Eq. (2.50) for $e^{K_1}$ as a Function of $S_L$ with the Current Density $J$ as a Parameter.
corresponding values of $s_L$ and $J$ as illustrated by the dashed lines in Fig. 2.12. These obtained values of $k_1$, $s_L$ and $J$ can be substituted into Eq. (2.48) which will lead to the difference in potential at the boundaries. However, from the schematic shown in Fig. 2.11, note that the difference $(a_2 - a_1)$ usually corresponds to the total applied voltage across the device if the structure is symmetric where the built-in potential across each junction is of the same magnitude. To have a symmetry in the built-in potential drop across each junction, they must have the same doping concentration and cross-sectional area. Accordingly, Eq. (2.48) leads to a relation between the applied voltage and the observed current flowing through the device.

2.3.3 Quasi Two-dimensional Solution

A fundamental electrical limitation in VLSI will be the spacing of the surface diffusions that form p-n junctions (source and drain of an MOS, for example). Reverse bias on one diffused junction creates a field pattern that can lower the potential barrier separating it from an adjacent diffused junction. When this barrier lowering is large enough, the adjacent diffusion behaves as a source, resulting in a new current path. If the lateral spacings, however, are scaled-down into a dimension comparable to the corresponding vertical ones, the
electrical field pattern will consist of two components, a lateral component in addition to a transverse component. The latter can be created by the oxide charge and surface states at the silicon-silicon dioxide interface. These originate from some processing actions and are associated with excess mobile ionic charges adhered on the silicon surface, as well as fixed and trap charges in the oxide film. Substrate bias, and gate electrode bias will also affect transverse fields for the case of MOS structures. Shown in Fig. 2.13(a) is an illustration of the two dimensional electric field distribution which creates a complex potential distribution in a short n-type channel MOS cross-section structure. Figure 2.13(b) shows the distributions in an n+pn+ bulk barrier device with a thin p-region. The two components of fields illustrated in Fig. 2.13 are a representation for the multi-dimensional electric field. It consists of longitudinal vector $E_L$ and transverse component $E_t$.

Obviously, a one-dimensional Poisson equation solution is not valid for analytical modeling of such structures. Inclusion of a second dimension is required in order to account for the multi-directional electric field. The electric field is approximated for simplicity in a two dimensional manner as shown in Fig. 2.13.

The two-dimensional (2-D) Poisson's equation in region A (Fig. 2.13) is
Fig. 2.13a Illustration of the Electric Field and the Potential Distributions in a Short Channel MOS. \( E_L \) is the Longitudinal or Lateral Field, \( E_T \) is the Transverse Field.

Fig. 2.13b Illustration of Electric Field and Potential Distributions in an \( n^+p^+n^+ \) Diode Fabricated Using Planar Technology with Small Spacing \( L \). Note that the Direction of \( E_T \) is Dependent on the Type of Charges at the Interface.
\[
\frac{dE_t}{dx} + \frac{dE_t}{dy} = \frac{q N_A}{\varepsilon_s} \quad (2.51)
\]

where \( n \) and \( p \ll N_A \)

A key approximation used to solve this equation analytically was first given by [Elmansy and Boothroyd, 1977]. The approximation has been improved and used extensively by [KO, 1982], [HSU, et al., 1983] and [Hu, et al., 1985] to study the effects of high electric fields near the drain in MOSFETs. These authors have shown that the electric fields and potentials calculated using this approximation are in close agreement with those obtained by 2-D numerical simulation.

Now, to solve Eq. (2.51) we can apply the same approximation. We can make the potential \( \phi(x,y) \) a function of \( y \) only as follows:

Let the surface potential be \( \phi(y) \)

\[
E_{x(x=0)} \approx -\frac{\phi(y) - V'_G}{X_{ox}} \left( \frac{\varepsilon_{ox}}{\varepsilon_s} \right) \quad (2.52)
\]

and

\[
V'_G \equiv V_G + V_{FB} \quad (2.53)
\]

where \( V_G \) is the applied gate bias for the case of Fig. 2.13(a), and \( V_{FB} \) is flat-band voltage due to non-ideality.
factors (charges) mentioned earlier. In 1985 Jain and Balk used this approximation to solve Poisson's equation (2.51) for the case when space charge layers due to source and drain meet and the whole region under the gate is depleted.

Equation (2.51) can be written in terms of $E_x$ and $E_y$ instead of $E_t$ and $E_l$ respectively.

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} = \frac{q}{\varepsilon_s} N_A$$ \hspace{1cm} (2.54)

Numerical simulations using MINIMOS shows that the lowest barrier path is at a distance $x = x_j$ from the surface where $x_j$ is the depth of the source-substrate/drain-substrate junctions. Along this path the vertical electric field $E_x$ drops to zero. Hence

$$\frac{dE_x}{dx} \approx \frac{\phi(y) - V_G}{x_{ox} W_o} \left( \frac{\varepsilon_{ox}}{\varepsilon_s} \right)$$ \hspace{1cm} (2.55)

where $W_o$ is the depth of the $n^+$ region. Substituting Eq. (2.55) into Eq. (2.54), we get

$$\frac{dE_y}{dy} = -\frac{\phi(y) - V_G'}{x_{ox} W_o} \left( \frac{\varepsilon_{ox}}{\varepsilon_s} \right) + \frac{q}{\varepsilon_s} N_A$$ \hspace{1cm} (2.56)
with: \( \varepsilon_{ox} \) - oxide dielectric constant, \( \varepsilon_s \) - silicon dielectric constant, and \( X_{OX} \) - oxide thickness under the gate electrode.

Rewriting Eq.(2.56) in terms of the potential \( \phi(y) \) instead of the electric field \( E_y \)

\[
\frac{d^2 \phi}{dy^2} + \frac{\varepsilon_s (V_G' - \phi(y))}{X_{OX} W_o} = -\frac{q N_A}{\varepsilon_s} \tag{2.57}
\]

Define

\[
y_o^2 = X_{OX} W_o \frac{\varepsilon_s}{\varepsilon_{ox}} \tag{2.58}
\]

\[
\phi_o = V_G' + X_{OX} W_o \frac{q N_A}{\varepsilon_{ox}} \tag{2.59}
\]

Using the definitions (2.58) and (2.59) in Eq.(2.57), we get the final Poisson's equation

\[
\frac{d^2 \phi}{dy^2} - \frac{\phi}{y_o^2} = -\frac{\phi_o}{y_o^2} \tag{2.60}
\]

The solution for the potential \( \phi(y) \) in Eq.(2.60) is of the form

\[
\phi(y) = \phi_o - \frac{1}{2} y_o k_1 \exp(-y/y_o) + k_2 \exp(y/y_o) \tag{2.61}
\]

where \( k_1 \) and \( k_2 \) are constants of integration and can be obtained from boundary conditions for the potential \( \phi(y) \).

For illustration, we can follow the same procedure as in Section 2.3.2 and Fig. 2.11. We define the boundary conditions as follow

\[ @ y = 0 ; \phi (y) = a_1 \]  
\[ @ y = L ; \phi (y) = a_2 \]

Substituting the conditions in Eqs. (2.62) and (2.63) into the solution in Eq. (2.61), we get the following two equations

\[ a_1 = \phi_0 - \frac{1}{2} Y_0 k_1 + k_2 \]  
\[ a_2 = \phi_0 - \frac{1}{2} Y_0 k_1 \exp(-L/Y_0) k_2 \exp(L/Y_0) \]

Solving Eqs. (2.64) and (2.65) for \( k_1 \) and \( k_2 \) in terms of the boundary conditions \( a_1 \) and \( a_2 \) leads to the following results

\[ k_1 = \frac{a_2 - \phi_0}{Y_0 \sinh(L/Y_0)} - \frac{(a_1 - \phi_0) \exp(L/Y_0)}{Y_0 \sinh(L/Y_0)} \]
Replacing \( k_1 \) and \( k_2 \) in Eq. (2.61) by their solutions from Eqs. (2.66) and (2.67) and simplifying the results, we get a final solution for the potential distribution in the \( n^+p_n^+ \) structure shown in Fig. 2.11. Thus

\[
(y)-\phi_0 = \frac{(a_2-\phi_0) \sinh(y/\gamma_0) + (a_1-\phi_0) \sinh[(L-y)/\gamma_0]}{\sinh(L/\gamma_0)}
\]

(2.68)

The potential \( \phi(y) \) in Eq. (2.68) includes the following

1- surface effects.

2- small geometries effect.

The current flowing through the structure can be obtained from the following relation

\[
I = I_0 \exp[q\phi(y)/kT]
\]

(2.69)

Note that \( a_1 \) and \( a_2 \) in Eq. (2.68) are the boundary conditions and are functions of the applied voltage. Therefore, the current in Eq. (2.69) is seen to have an exponential dependance on the applied voltage.
CHAPTER 3

PUNCH-THROUGH SPACE-CHARGE LIMITED LOAD (SCLL)

The performance of bipolar and MOS silicon devices is approaching limits imposed by device physics and dimensions. The physics imposed limits often relate to carrier diffusion phenomena limited transit times. The dimension imposed limits usually relate to storage and depletion capacitances. Shrinking the device size and lowering the power of a single stage leads to lower currents requiring large value resistors. At the same time, the values of the sheet resistance and unit capacitance remain unchanged. This has caused device researchers to investigate resistor like devices based on different operating or processing principles. One result is to use polysilicon resistors. However, doped polysilicon layers frequently require additional processing effort. It is also relatively difficult to control the resistance of such layers because the resistance depends not only on the impurity concentration, but also on the grain size of the polycrystalline silicon.

This chapter will discuss a device which operates in a punch-through condition with space-charge control of currents. This device can be considered as an alternative
to integrated resistors, and active loads. The punch-through condition in bipolar devices was identified some time ago as an undesirable condition to be avoided by all means. It caused loss of control and gain in standard bipolar devices. Also, in the case of MOS devices, punch-through is considered as an undesirable effect.

In order to avoid punch-through in small devices, a much higher impurity concentration than usual is required. This problem is especially important for micrometer and submicrometer geometries. Increasing impurity concentrations causes large parasitic capacitances and, therefore, lower device speed.

However, a properly designed and fabricated two terminal device operating in a punch-through mode can provide stable high values of resistance in small areas on a chip [Wilamowski, et al., 1986]. Large voltage drop at low current density is possible when space-charge neutrality is not satisfied and current flow is controlled by the space charge of the moving carriers. The resistance can be linear over a broad range of operating conditions, although it is a nonlinear device. It also offers fast switching speeds due to reduced area and low impurity concentration.

A description of the device operating mechanisms and principles are offered in Section 3.1. Analytical device modeling including temperature and mobile carrier effects are presented in Section 3.2. Computer simulations using a
general one-dimensional device performance simulation program (GESIM1) giving steady-state and transient analysis are in Section 3.3. Device design and electrical evaluations are covered in section 3.4. Finally, a comparison of theoretical and experimental results and a comparison of punch-through space-charge limited load with standard IC resistors are presented in Sections 3.5 and 3.6 respectively.

3.1 Operating Principles

Figure 3.1(a) and (b) show the cross sectional structures of n+p-n+ and p+n-p+ punch-through space-charge limited-loads. With an increase in the applied voltage, the thickness of the depletion layer associated with the drain-substrate junction increases. When the depletion layer reaches the adjacent source-substrate junction, punch-through occurs. Carriers are injected from the source region into the depletion region, and current starts to flow. The applied voltage when the depletion layers just touch is designated the punch-through voltage $V_{Pt}$. Punch-through voltage $V_{Pt}$ can be controlled by geometry and substrate resistivity. Analytical expression for $V_{Pt}$ will be given in the next section.

Consider the n+p-n+ structure in Fig. 3.1(a). In this case the current flow is due to electrons which are
Fig. 3.1 Punch-Through Space-Charge-Limited-Load (PTSCLL) Structures.
injected from the n+ forward biased junction into the p-substrate and collected by the reverse biased drain junction. The current continues to increase with the applied voltage until a flat-band condition is reached. At this voltage the level of electron injected carriers from the injecting electrode into the depleted substrate region is large. This increase in the injected electrons in the depletion region creates a space-charge cloud, negative for n-channel devices. This negative cloud retards the injection of electrons and therefore, the current flow is also limited. Thus, the current observed to flow through the structure in this region of operation is space-charge-limited. Finally, breakdown of the reverse biased junction is reached. This is usually an avalanche breakdown and the current is very large and independent of the applied voltage.

This description of device operation applies for p+n-p+ devices with the major difference being that holes are the mobile carriers.

3.2 Analytical Device Modeling

In this section, analytical modeling of the carrier transport mechanisms involved in the operation of the n+p-n+ PTSCLL (similar results apply to the p+n-p+ structure) will be offered. The approach is to first use the simple one-
dimensional depletion approximation to predict the I-V relation. Then the effect of mobile carriers on the I-V characteristics is added. Finally, a quasi-two-dimensional model for the device is developed to account for inherent effects associated with the device technology. Based on these, models of the temperature effect on the device behavior will be obtained analytically. The analytical results will be evaluated experimentally in latter part of this chapter.

3.2.1 I-V Characteristics

Figure 3.2 shows the idealized one-dimensional n+p-n+ Punch-Through Space-Charge Limited-Load (PTSCLL) structure. Also shown are the charge, electric field and potential distributions before punch-through conditions based on the depletion approximation. The n+p- junctions will be modeled as one-sided abrupt junction, thereby neglecting the depletion regions associated with the n+ materials since they are heavily doped. For applied positive voltage less than punch-through, the resulting current is very small. It is limited by the reverse-biased drain junction. The current density is given approximately by the thermal generation current density associated with the depleted regions of widths $W_1$ and $W_2$.

$$J \approx \left( \frac{q n_i}{\tau_p} \right) (W_1 + W_2)$$  \hspace{1cm} (3.1)
Fig. 3.2  (a) $n^+p^+n^+$ Structure.  (b) Charge Distribution.  
(c) Electric Field.  (d) Potential Distribution 
Based on the Depletion Approximation.
where $\tau_p$ is the effective lifetime and $n_i$ is the intrinsic carrier density. $W_1$ and $W_2$ are the depletion region widths as illustrated in Fig. 3.2. $W_1$ and $W_2$ are obtained from the single pn junction analysis to have the form

$$W_1 = [\frac{2\varepsilon_s}{qN_A}(V_{bi} - V_1)]^u$$  \hspace{1cm} (3.2)$$

and

$$W_2 = [\frac{2\varepsilon_s}{qN_A}(V_{bi} + V_2)]^u$$  \hspace{1cm} (3.3)$$

where $N_A$ is the impurity density of the p- layer, $V_1$ and $V_2$ are defined in Fig. 3.2 and $V_{bi}$ is the built-in voltage at each junction assuming symmetrical structure. As the applied voltage increases, the depletion width $W_2$ increases and $W_1$ decreases, but ultimately they touch completely depleting the p- region. The punch-through voltage can be obtained from the following conditions,

$$V_1 + V_2 = V = V_{pt}$$  \hspace{1cm} (3.4)$$

at

$$W_1 + W_2 = L$$  \hspace{1cm} (3.5)$$

From Eqs. (3.2), (3.3), (3.4) and (3.5), the depletion approximation predicts the punch-through voltage to be

$$V_{pt} = \frac{qN_A}{2\varepsilon_s}L^2 - L\left[\frac{2qN_A}{\varepsilon_s} V_{bi}\right]^u$$  \hspace{1cm} (3.6)$$

At punch-through the electric field and potential distribution are as illustrated in Fig. 3.3. Note that the
Fig. 3.3 (a) Structure at Punch-Through Based on the Depletion Approximation; (b) Electric Field Distribution at Punch-Through Applied Voltage; (c) Electrostatic Potential Distribution Right at Punch-Through.
electric field increases linearly with distance across the p-drift region.

The depletion approximation for applied voltages less than the punch through voltage predicts a current density slowly increasing due to thermally generated carriers in an increasing volume associated with an increasing $W_2$. It predicts a rapidly increasing $W_2$ with no change in $W_1$ ($\cdot V_1 = 0$) until all of the ionized acceptor impurities are uncovered at punch through. The voltage $V_{pt}$ is predicted by Eq. (3.6).

Since all of the ionized impurities provide the space charge needed to realize the punch through voltage, any increase in applied voltage must be offset by some other mechanism. This mechanism is the reduction of the barrier potential, $(V_{bi} - V_1)$ because of an increasing $V_1$. An increase in applied potential above $V_{pt}$ reduces the potential barrier. This causes an exponential increase in current as developed below. After punch-through, Poisson equation is

$$\frac{d^2(-\phi)}{dx^2} = \frac{dE}{dx} = \frac{qN_A}{\varepsilon_S}, \text{ for } 0 < x < L \quad (3.7)$$

Integrating Eq. (3.7) twice we get the following expressions for the electric field and the potential

$$E(x) = \left(\frac{qN_A}{\varepsilon_S}\right)x + k_1 \quad (3.8)$$
and

\[ \phi(x) = -(qN_A/2\varepsilon_s)x^2 - k_1 x + k_2 \]  \hspace{1cm} (3.9)

where \( K_1 \) and \( K_2 \) are constants of integration and can be determined from the boundary conditions. From Fig. 3.3(c), the boundary conditions are

@ \( x = 0 \) \hspace{1cm} \( \phi = V_{bi} - V_1 \)  \hspace{1cm} (3.10)

@ \( x = L \) \hspace{1cm} \( \phi = V_{bi} + V_2 \)

Substituting the conditions from Eq. (3.10) into Eq. (3.9), give analytical expressions for the electric field and the potential distribution for \( V_{Pt} V V_{FB} \) as

\[ E(x) = (qN_A/\varepsilon_s)x + \frac{|V_{FB}|-V}{L} \]  \hspace{1cm} (3.11)

\[ \phi(x) = -(qN_A/2\varepsilon_s)x^2 + \frac{|V_{FB}|-V}{L} x + (V_{bi} - V_1) \]  \hspace{1cm} (3.12)

where \( V_{FB} \) is the flat-band voltage given by

\[ |V_{FB}| = (q N_A / 2\varepsilon_s) L^2 \]  \hspace{1cm} (3.13)

The flat-band condition is defined as the applied voltage at which the potential barrier at junction 1 vanishes as illustrated in Fig. 3.4. The position at which the potential barrier is maximum \( X_0 \), decreases as \( V \) increases. It can be calculated from Eq. (3.11) by setting the field to zero.
Fig. 3.4 Potential Distribution at Various Operating Conditions Based on the Depletion Approximation. Note that: Barrier Height is Equal to $V_{bi} - V_L$. 
In the region \( V_{pt} < V < |V_{FB}| \) of the device operation, electrons flow over the barrier from the heavily doped cathode/source electrode into the p\(^-\) drift region by thermionic emission and/or by diffusion. They have to overcome a potential barrier in the p\(^-\) region before reaching the reverse-biased n\(^+\) collecting electrode. The barrier height decreases as the applied voltage progresses further and ultimately will disappear as shown in Fig. 3.4. The height of this barrier can be calculated from Eqs. (3.12) and (3.14), that is

\[
x_0 = \frac{\varepsilon_s}{qN_A} ; \quad V_{pt} \leq V \leq |V_{FB}|
\]

For voltages larger than \( V_{pt} \), and lower than \( V_{FB} \), the current is due to the thermionic emission process and/or diffusion process and increases rapidly as the height of the barrier decreases. It is given by the well known exponential expression

\[
J = J_0 \exp\left[-\frac{q(V_{bi} - V_1)}{kT}\right]
= J_0 \exp\left[-\frac{q(|V_{FB}| - V)^2}{4kT |V_{FB}|}\right]
\]

where the pre-exponential factor \( J_0 \) depends on the carrier's injection whether thermionic emission or diffusion. However, if the injection is due to thermionic-emission, then, \( J_0 \) has the form
where $A^*$ is the Richardson's constant and $T$ is the absolute temperature. Further, for voltages exceeding the flat-band voltage, the potential is as seen in the top curve of Fig. 3.4 where disappearance of the potential barrier is realized, and therefore a substantial increase in the electron injection (high injection condition) into the depleted p-type region. Accumulation of electrons in this region where they create an internal negative space-charge which affects the potential distribution. This will control the current flow as the voltage is increased by limiting further injection of electrons. This is the well known space-charge limited current flow phenomena [Mott and Gurney, 1940]. The current exhibits a $V^2$-dependence for high electric fields beyond the saturation of velocity. Therefore

$$\frac{3}{8} = \frac{9}{4} \frac{\mu_n \varepsilon_s}{L^2}$$

for small field, where $\mu_n$ is the mobility of electrons in the p-region. For this region the dynamic resistance, $R$, is given by:

$$R = \frac{dV}{dI} = \frac{4}{9} \frac{L^3}{\mu_n \varepsilon_s \frac{A}{V}} = \frac{V}{2I}$$

where $A$ is the area. The carrier transit time $\tau$ is given by
\[ \tau = R \cdot C = \frac{4}{9} \frac{L^2}{\mu_n V} \quad (3.20) \]

However, under conditions of high electric field, the carrier velocity is the saturation velocity \( V_s \) [Wilamowski, et al., 1986] and the relationships become quite simple as shown below:

\[ J = 2 V_S \varepsilon_S \frac{V}{L^2} \quad (3.21) \]

\[ R = \frac{1}{2 \frac{V_S}{\varepsilon_S} \frac{L^2}{A}} \quad (3.22) \]

and

\[ \tau = \frac{L}{2 V_S} \quad (3.23) \]

Using the high electric field approximation which is reasonable for small dimensions, the relationship between \( I \) and \( V \) can be calculated as a function of doping and spacing for a 20 square micron area (the \( n^+ \) region cross-sectional area). The results are shown in Fig. 3.5(a) and Fig. 3.5(b). Note that some small voltage is required to reach the punch-through condition. Exceeding that voltage, the device appears to be pure resistance. Equation (3.22) shows that \( R \) is a function of geometry only for this theoretical model and therefore, independently controllable.
Fig. 3.5 Calculated I-V Characteristics of PTSCL Loads for Various Spacing Between Cathode and Anode (a) and for Various Substrate Doping (b).
However, this model is one-dimensional and many approximations are involved. Furthermore, the structure shown in Fig. 3.1 is two-dimensional and the need for a two-dimensional analytical model can be seen. However, solution of the two-dimensional continuity equation analytically may not be dealt with successfully. An alternative approach is to use of numerical computation. This is a time consuming process and involves the loss of physical insight of how the device operates. Nevertheless, using certain approximations the two-dimensional continuity equation can be solved as was described in Chapter 2, Section 3. This leads to an analytical model for the structure shown in Fig. 3.1. The two-dimensional continuity equation was introduced in Eq. 2.51. Applying the approximations described in Chapter 2 leads to the following one-dimensional equation,

\[
\frac{d^2\phi}{dy^2} - \frac{\phi}{y^2_o} = - \frac{\phi_0}{y^2_o}
\]  

(2.60)

where

\[ Y_o^2 = W_o \times_{ox} \varepsilon_s / \varepsilon_{ox} \]

and

\[ \phi_0 = V_G' + W_o \times_{ox} q N_A / \varepsilon_{ox} \]

A solution of this equation for the potential \( \phi(y) \) is of the form
\[ \phi(y) = \phi_o - \frac{1}{2} y_0 k_1 \exp(-y/y_o) + k_2 \exp(y/y_o) \quad (3.24) \]

where \( k_1 \) and \( k_2 \) can be obtained from the boundary conditions shown in Fig. 3.6 and are given by

@ \( y = 0 \):
\[ \phi(y) = V_{bi} - V_1 = V_s \approx V_{bi} \quad (3.25) \]

@ \( y = L \):
\[ \phi(y) = V_{bi} + V_2 = V_2 \quad (3.26) \]

Substituting the boundary conditions from Eqs. (3.25) and (3.26) into the equation for the potential described by Eq. (3.24) leads to the following expression

\[ \phi(y) - \phi_o = \frac{1}{\sinh(L/y_o)} \left[(V_d - \phi_o) \sinh(y/y_o) \right. \\
\left. + (V_{bi} - \phi_o) \sinh \frac{L-y}{y_o} \right] \quad (3.27) \]

To find the position of the potential maximum, we impose the condition

\[ \left. \frac{d\phi(y)}{dy} \right|_{y=y_b} = 0 \quad (3.28) \]

where \( y_b \) is the position along the channel of the maximum potential. \( \phi(y_b) \) is the barrier height in the path of the current flow. Invoking the condition in Eq. (3.28) into Eq. (3.27), solving for \( y_b \) we get the following
Fig. 3.6 Potential Distribution across the SCLL Structure Shown in Fig. 3.1. $V_1$ is the Voltage Drop across the Forward-Biased Junction, while $V_2$ is the Voltage Drop across the Reverse-Biased Junction.
Now the potential barrier in the path of the injected carriers can be obtained from Eqs. (3.27) and (3.29) where \( Y_b \) has to be substituted for \( y \). Thus

\[
\phi(Y_b) - \phi(BL) = \phi_0 + \frac{1}{\sinh(L/Y_0)} \left[ (V_d - \phi_0) \sinh(Y_b/Y_0) \right. \\
\left. + (V_{bi} - \phi_0) \frac{L - Y_b}{Y_0} \right] 
\]

(3.31)

The current flow is exponentially proportional to the potential barrier lowering. In other words, the current is proportional to the exponential of negative of actual barrier height in the channel. Therefore

\[
I = I_0 \exp[ \frac{q \phi_{BL}}{kT} ] 
\]

(3.32a)

or

\[
I = A \exp[ - \frac{q(V_{bi} - \phi_{BL})}{kT} ] 
\]

(3.32b)

where \( \phi_{BL} \) is the potential barrier lowering and is a strong function of the applied voltage, \( V_{bi} \) is Schottky barrier or the built-in potential at the metalurgical junction, \( I_0 \) and
are dependent on the controlling mechanisms of carriers injection either by thermionic emission or by diffusion and can be determined experimentally.

The expressions obtained in Eqs. 3.32 are only applicable for $V_{pt} < V < V_{FB}$. The drastic increase of the mobile (injected) carriers has to be included in the solution of the continuity equation for $V > V_{FB}$. However, for this region of operation, above the flat-band voltage, the expression obtained in Eq. (3.18) is valid for the low electric field case and the expression in Eq. (3.21) for the case of a saturating velocity (high field) of carriers. The experimental I-V characteristics will be shown at the end of this chapter.

3.2.2 Temperature Effect

As was observed earlier, the I-V characteristics of the space-charge limited-load has been characterized in two different main regions of operation, that is, between punch-through and flat-band conditions, $V_{pt} < V < V_{FB}$ and above the flat-band, $V > V_{FB}$. The former region was characterized by carrier flow over a potential barrier. The carriers were due to either thermionic emission or diffusion for $V_{pt} < V < V_{FB}$. For $V > V_{FB}$ the current was described as space charge-limited flow. The two different regions of operation necessitate two separate models to predict the temperature effects on the I-V characteristics.
a) For the region \( V_{pt} < V_d < V_{PB} \):

From the expression given in Eq. (3.32a) we see that the current is an explicit function of temperature as can be seen in the exponential factor, \( I_0 \) is an implicit function of temperature. Furthermore, the potential barrier lowering is an implicit function of temperature. Nevertheless, the total current was observed experimentally to exhibit a positive temperature coefficient. The current increases with temperature. This is due to the fact that the potential barrier lowering increases with temperature (the potential barrier height decreases with temperature) and that \( I_0 \) is a very strong function of temperature as will be illustrated.

To obtain the temperature coefficient for the current in this region of operation we can rewrite Eq. (3.32a) as follows:

\[
I = I_0(T) \exp\left[ \frac{q \phi_{BL}}{kT} (1 + \alpha T) \right]
\]

Differentiate Eq. (3.33) with respect to temperature. Note that \( \phi_{BL} \) is only a function of the applied voltage. Then

\[
\frac{dI}{dT} = \frac{dI_0(T)}{dT} \exp\left[ \frac{q \phi_{BL}}{kT} \right] \exp\left[ \frac{q \phi_{BL}}{kT} \right] \frac{\alpha \phi_{BL}}{kT}
\]

\[
+ I_0(T) \left( \exp\left[ \frac{q \phi_{BL}}{kT} \right] \exp\left[ \frac{q \phi_{BL}}{kT} \right] \frac{1}{kT} \right)
\]

\[
+ I_0(T) \left( \frac{\alpha \phi_{BL}}{k} \right) \frac{d\alpha}{dT} \exp\left[ \frac{q \phi_{BL}}{kT} \right] \exp\left[ \frac{q \phi_{BL}}{kT} \right] \frac{q \phi_{BL}}{kT}
\]

Note (3.34)
Equation (3.34) can be simplified by factoring out $I$ in the right hand side. Thus

$$\frac{dI}{dT} = I \left[ \frac{1}{I_0} \frac{dI_0}{dT} - \frac{q \phi_{BL_0}}{kT^2} + \left( \frac{q \phi_{BL_0}}{k} \right) \frac{d\alpha}{dT} \right]$$

or

$$\frac{1}{I} \frac{dI}{dT} = \frac{1}{I_0} \frac{dI_0}{dT} - \frac{q \phi_{BL_0}}{kT^2} + \left( \frac{q \phi_{BL_0}}{k} \right) \frac{d\alpha}{dT} \quad (3.35)$$

However, is not a strong function of temperature and accordingly we can neglect the third term in the right of Eq. 3.35. Moreover, to find an expression for $I_0$ we will consider the two controlling mechanisms mentioned earlier. Thus, if the carrier transport is controlled by thermionic emission, then, $I_0$ is of the form

$$I_0 = A^* T^2 A \exp(-\frac{qV_{bi}}{kT}) \quad (3.36)$$

where $A^*$ is Richardson constant, and $A$ is the effective cross-sectional area. Therefore, the total current expression is given by

$$I = A^* T^2 A \exp(-\frac{qV_{bi}}{kT}) \exp[q \phi_{BL_0} (1 + \alpha T)/kT]$$

$$= A^* T^2 A \exp[-q(V_{bi} - \phi_{BL_0})/kT] \exp(q \frac{\phi_{BL_0}}{k}) \quad (3.37)$$
Substituting Eq. (3.36) into Eq. (3.35), we get the following result

\[
\frac{1}{I} \frac{dI}{dT} = \frac{2}{T} + \frac{qV_{bi}}{kT^2} - \frac{q\phi_{BL0}}{kT^2} = \frac{2}{T} + \frac{q}{kT^2} \left( V_{bi} - \phi_{BL0} \right)
\]

Eq. (3.38) can be obtained experimentally by plotting \( \ln(I/A_1) \) vs. \( q/kT \) for a fixed applied voltage. The slope of the curve is the difference \( V_{bi} - \phi_{BL0} \) as shown in Fig. 3.7, where 12 volts was applied to the device. \( A_1 \) is defined by the following expression

\[
A_1 = A^* T^2 \exp\left( \frac{q\alpha\phi_{BL0}}{k} \right)
\]

The slope of the curve of Fig. 3.7 is equal to 0.002889V. Substituting this value into Eq. (3.38), we have the final expression of the current temperature coefficient. Thus

\[
\frac{1}{I} \frac{dI}{dT} = \frac{2}{T} + \frac{334.96 \ O K}{T^2}
\]

If the carrier transport is controlled by diffusion, then \( I_0 \) takes the form of the saturation current in a p-n junction and is
Fig. 3.7 Plot of the Normalized Current vs. 1/T.
where \( n_i \) is the intrinsic concentration and a very strong function of temperature, \( \mu_n \) is the mobility of electrons, \( N_A \) is the impurity concentration in the channel, and, \( W_n \) is the junction depth of the injecting \( n^+ \) electrode. Substituting Eq. (3.41) into Eq. (3.35) gives

\[
\frac{1}{I} \frac{dI}{dT} = \frac{1}{T} + \frac{2}{n_i} \frac{dn_i}{dT} - \frac{q\phi_{BLO}}{kT^2}
\]  
(3.42)

However, \( n_i \) is given by

\[
n_i = C T^{3/2} \exp\left(-\frac{E_g}{2kT}\right)
\]  
(3.43)

where \( C \) is the proportionality constant and depends on the mass of the carriers. Substituting Eq. (3.43) into Eq. (3.42) leads to

\[
\frac{1}{I} \frac{dI}{dT} = \frac{4}{T} + \frac{2E_g}{kT^2} - \frac{2}{kT} \frac{dE_g}{dT} - \frac{q\phi_{BLO}}{kT^2}
\]  
(3.44)

Although the band gap \( E_g \) is a function of temperature, the third term in the right of Eq. (3.44) can be neglected compared to the other terms for small variation of temperature. \( \phi_{BLO} \) can be obtained from the slope of the curve in Fig. 3.7. \( V_{bi} \) is approximately 0.7V. Therefore,
the current temperature coefficient for the case of diffusion is approximately given by

\[
\frac{1}{I} \frac{dI}{dT} \approx \frac{4}{T} + \frac{17726.26 \deg}{T^2}
\]  

(3.45)

Therefore, for \( V_{pt} < V < V_{FB} \) either Eq. (3.40) or Eq. (3.45) can be used to model the temperature effect on the I-V characteristics of the SCELL. The former is to be used if the source of carriers is due to thermionic emission and the latter if diffusion phenomena is dominant.

(b) For the region \( V_d > V_{FB} \):

For this region of operation, the expression given in Eq. (3.18) can be used for modeling the temperature effects.

\[
I = 9A \mu_n \epsilon_s V^2 /8L^3
\]  

(3.46)

In this region of operation, the only parameter that changes with temperature is the mobility. Electrons in the drift region can be considered as the majority carriers justified by the high injection condition. Thus

\[
\frac{dI}{dT} = \frac{I}{\mu_n} \frac{d\mu_n}{dT}
\]

or
The mobility $\mu_{in}$ is described by Conwell and Weisskopf, [1950].

$$\mu_{in} = \frac{64\sqrt{\pi} \varepsilon^2 (2kT)^{3/2}}{N_A q^3 m^{1/2}} \left[ \ln \left[ 1 + \left( \frac{12 \pi \varepsilon e kT}{q^2 N_A^{1/3}} \right)^2 \right] \right]^{-1}$$  \hspace{1cm} (3.48)

where $N_A$ is the ionized impurity density. The mobility is expected to increase with temperature. Substituting Eq. (3.48) into Eq. (3.47), gives

$$\frac{1}{I} \frac{dI}{dT} = \frac{1}{\mu_{in}} \frac{d\mu_{in}}{dT} = \frac{8.85582 \times 10^8 T}{2T} \frac{1}{[N_A^{2/3} + 4.42791 \times 10^8 T^2] \ln [1 + 4.42791 \times 10^8 T^2]} \frac{1}{N_A^{3/2}}$$ \hspace{1cm} (3.49)

Figure 3.8 shows a plot of Eqs. (3.40) and (3.49) as a function of the inverse of temperature. This shows theoretically that operating the device in the space charge limited flow region $V > V_{FB}$, provides a lower temperature coefficient when compared with voltages such that $V_{PT} < V < V_{FB}$.

Figure 3.9 shows the experimental I-V characteristics with the temperature as a parameter. The current is seen to increase with temperature, because of the increase in barrier height lowering and in the pre-exponential factor.
\[ \text{Eq. (3.40)} \text{ for } V_{pt} < V_d < V_{FB} \]

\[ \text{Eq. (3.49)} \text{ for } N_a = 3 \times 10^{14} \text{cm}^{-3}, \]

\[ V_d > V_{FB} \]

Fig. 3.8 Temperature Coefficient for the Current vs. $1/T$ for the Regions Between Punch-Through and Flat-Band (Top Curve) and above Flat-Band (Bottom Curve).
Fig. 3.9 Experimental I-V Characteristics for Three Different Temperatures.
3.2.3 Analytical I-V Characteristic Including Mobile Carrier Effect

The analytical solution of the 1-D Poisson's equation including mobile carriers was derived in Chapter 2, Section 2.3.2. The parameters $a_1$ and $a_2$ can be obtained from Fig. 3.6

\[
a_1 = V_{bi} - V_1 \\
a_2 = V_{bi} + V_2
\]

Note that the difference $a_2 - a_1$, is the total applied voltage $V$. Therefore, from Eq. (2.48)

\[
v = \frac{1}{\beta^2} \left[ \frac{1}{2\alpha\beta} e^{2k_1[\exp(2\alpha\beta S_L) - 1]} - \frac{2}{\alpha\beta} e^{k_1 [\exp(\alpha\beta S_L) - 1] + S_L} \right] \tag{3.50}
\]

\[
\alpha \equiv \frac{J_E S}{\varepsilon_S V_S} \tag{3.51}
\]

\[
\beta \equiv \frac{(qN_A V_S + J) / J_E S} \tag{3.52}
\]

\[
e^{k_1} = \frac{\alpha \beta^2 L - \alpha \beta S_L}{\exp(\alpha \beta S_L) - 1} \tag{3.53}
\]

where Eqs. (3.50) through (3.53) are also derived in Chapter 2. From Eq. (3.53), we can generate a plot of $e^{k_1}$ vs. $S_L$ with current density $J$ as a parameter via $\alpha$ and $\beta$. Fig. 3.10 shows such a plot with current density ranges from 40 amp/cm$^2$ (top curve) to 200 amp/cm$^2$ (bottom curve). The parameters have values chosen as follows: $L = 6 \ \mu$m, $N_A = \ldots$
Fig. 3.10 Plot of $e^k_1$ vs. $S_L$ from Eq. (3.53) with the Current Density as a Parameter.
2 \times 10^{14} \text{ cm}^{-3}, \ E_s = 3 \times 10^4 \ \text{v/cm} \text{ and } V_s = 1 \times 10^7 \ \text{cm/sec}. \ The \ horizontal \ dashed \ line \ in \ Fig. \ 3.10, \ provides \ the \ values \ of \ \sigma_L \ for \ different \ current \ densities \ for \ a \ constant \ value, \ \varepsilon k_1 = 6. \ The \ resulting \ data \ is \ listed \ in \ Table \ 3.1. \ Using \ the \ data \ from \ Table \ 3.1, \ and \ Eq. \ (3.50) \ the \ values \ of \ applied \ voltage \ corresponding \ to \ the \ chosen \ values \ of \ the \ SCELL \ current \ density \ can \ be \ calculated. \ The \ results \ are \ listed \ in \ Table \ 3.2. \ A \ plot \ of \ the \ theoretically \ predicted \ current \ density \ J \ vs. \ the \ applied \ voltage \ is \ shown \ in \ Fig. \ 3.11 \ for \ two \ cases. \ Figure \ 3.11(a) \ shows \ the \ theoretical \ J-V \ characteristic \ including \ mobile \ carrier \ effects \ as \ developed \ from \ Table \ 3.2. \ Figure \ 3.11(b) \ shows \ the \ theoretical \ J-V \ characteristic \ obtained \ from \ Eqs. \ (3.16) \ and \ (3.18) \ based \ on \ the \ 1-D \ depletion \ approximation.

The \ curve \ shown \ in \ Fig. \ 3.11(a) \ is \ an \ exact \ one-dimensional \ theoretical \ solution \ including \ mobile \ carrier \ concentrations. \ At \ low \ voltages, \ the \ solution \ in \ Eq. \ (3.50) \ includes \ the \ effect \ of \ the \ ionized \ impurities \ as \ well \ as \ the \ mobile \ carriers. \ The \ magnitude \ of \ the \ mobile \ carriers \ is \ small \ in \ this \ region \ of \ operation. \ Figure \ 3.11(b) \ shows \ the \ theoretical \ V \ vs. \ J \ plot \ when \ the \ mobile \ carriers \ are \ neglected. \ At \ high \ voltages, \ the \ magnitude \ of \ the \ mobile \ carriers \ becomes \ very \ large \ compared \ to \ the \ ionized \ impurities \ so \ this \ plot \ will \ not \ be \ a \ good \ approximation \ to \ reality. \ However, \ Fig. \ 3.11(a) \ takes \ both \ ionized \ impurities \ and \ mobile \ carriers \ into \ account \ and \ therefore
Table 3.1 Data from figure 3.10 for $e^{k_1}=6$.

<table>
<thead>
<tr>
<th>$J$ (amp/cm²)</th>
<th>$s_L$ (cm²/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>$18.92 \times 10^{-9}$</td>
</tr>
<tr>
<td>60</td>
<td>$14.25 \times 10^{-9}$</td>
</tr>
<tr>
<td>80</td>
<td>$11.65 \times 10^{-9}$</td>
</tr>
<tr>
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<td>$9.90 \times 10^{-9}$</td>
</tr>
<tr>
<td>120</td>
<td>$8.80 \times 10^{-9}$</td>
</tr>
<tr>
<td>140</td>
<td>$8.00 \times 10^{-9}$</td>
</tr>
<tr>
<td>160</td>
<td>$7.30 \times 10^{-9}$</td>
</tr>
<tr>
<td>180</td>
<td>$6.84 \times 10^{-9}$</td>
</tr>
<tr>
<td>200</td>
<td>$6.43 \times 10^{-9}$</td>
</tr>
</tbody>
</table>

Parameters:

- $L = 6$ micrometer
- $N_A = 2 \times 10^{14}$ cm⁻³
- $E_S = 3 \times 10^4$ V/cm
- $V_S = 1 \times 10^7$ cm/sec
Table 3.2 I-V numerical data from Eq. (3.50) and (3.53) for $e^{k_1} = 6$.

<table>
<thead>
<tr>
<th>$J$ (amp/cm²)</th>
<th>$s_L$ cm²/V</th>
<th>$V$ (volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.001</td>
<td>336.62x10⁻⁹</td>
<td>5.55</td>
</tr>
<tr>
<td>0.100</td>
<td>187.57x10⁻⁹</td>
<td>5.55416</td>
</tr>
<tr>
<td>1.000</td>
<td>113.35x10⁻⁹</td>
<td>5.60582</td>
</tr>
<tr>
<td>5.000</td>
<td>64.046x10⁻⁹</td>
<td>6.17245</td>
</tr>
<tr>
<td>10.00</td>
<td>45.500x10⁻⁹</td>
<td>7.20928</td>
</tr>
<tr>
<td>20.00</td>
<td>30.190x10⁻⁹</td>
<td>8.85861</td>
</tr>
<tr>
<td>40.00</td>
<td>18.920x10⁻⁹</td>
<td>12.32862</td>
</tr>
<tr>
<td>60.00</td>
<td>14.250x10⁻⁹</td>
<td>15.59500</td>
</tr>
<tr>
<td>80.00</td>
<td>11.650x10⁻⁹</td>
<td>18.5500</td>
</tr>
<tr>
<td>100.0</td>
<td>9.9000x10⁻⁹</td>
<td>20.95166</td>
</tr>
<tr>
<td>120.0</td>
<td>8.8000x10⁻⁹</td>
<td>23.56413</td>
</tr>
<tr>
<td>140.0</td>
<td>8.0000x10⁻⁹</td>
<td>26.03788</td>
</tr>
<tr>
<td>160.0</td>
<td>7.3000x10⁻⁹</td>
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</tr>
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<td>180.0</td>
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</tr>
<tr>
<td>200.0</td>
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<td>300.0</td>
<td>5.140x10⁻⁹</td>
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</tr>
<tr>
<td>400.0</td>
<td>4.4750x10⁻⁹</td>
<td>45.82010</td>
</tr>
</tbody>
</table>

Parameters:

$E_S = 3 \times 10^4$ V/cm
$L = 6$ micrometer
$N_A = 2 \times 10^{14}$ cm⁻³
$V_S = 1 \times 10^7$ cm/sec
Fig. 3.11 Theoretical J-V Characteristics of SCLL Based on Two 1-D Models, a) Including Mobile Carrier Effects, and b) the Depletion Approximation.
(b) Equations (3.16) and (3.18)

Fig. 3.11 (Continued)
should be a better predictor of measured I-V characteristics.

The curves for low values of applied voltage have the same shape. The agreement is attributed to the fact that the contribution of mobile carriers is negligible at low applied voltages. Conversely the contribution of the ionized impurities is negligible at high applied voltages. There is a disagreement around the knee of the curves where the flat-band condition occurs. Around the flat-band condition, the two impurity densities are comparable; therefore, neither one can be neglected. Figure 3.11(a) takes this into account while the knee of the curve in Fig. 3.11(b) is the boundary between the two transport mechanisms described earlier.

The discrepancy in the values of the current density for the two cases is caused by two parameters, \( K_1 \) for the mobile carrier case and the pre-exponential multiplier in Eq. (3.16). The former can be obtained experimentally, the latter depends on the carrier transport mechanisms.

3.3 Computer Device Simulation

Punch-through and space-charge phenomena are complicated in nature and, in order to fully investigate and understand their behavior, a computer simulation is necessary. Most of the existing computer simulation
programs use various combinations of simplified approaches in order to simplify algorithms. Frequently, assumptions are: space charge neutrality, Boltzman statistic, neglecting recombination, or dominance of one type of carriers. However, for small geometry, high speed devices for VLSI applications, such assumptions are not valid and a more general approach is needed. A general one-dimensional semiconductor device performance simulation program (GESIM1) was published [Wilamowski, et al.,1984]. This program allows the user to simulate the static and dynamic performance of a device. The GESIM1 simulation includes all parasitic effects and provides information about the detailed transient behavior of such devices. The input data required consists of the impurity concentration distribution and the applied terminal voltages. The steady-state solution is found first, and then transient analysis is performed for any given voltage excitation. It is also possible to incorporate the GESIM1 simulation into a circuit and solve for operating conditions. In this case transient terminal voltages and currents are predicted from the simulation.

3.3.1 GESIM1: Principles

Basic Equations

Five basic differential equations, which are solved in one-dimension in this program are given below
Transport equations:

\[
J_p = -qD_p \text{grad } p - q \mu_p \text{grad } \phi \tag{3.54a}
\]

\[
J_n = qD_n \text{grad } n - q \mu_n \text{grad } \phi \tag{3.54b}
\]

where \(J_p\) and \(J_n\) are the hole and electron current density, respectively, \(D_p\) and \(D_n\) hole and electron diffusion constant, \(p\) and \(n\) the density of holes and electrons, \(\mu_p\) and \(\mu_n\) hole and electron mobility and \(\phi\) the potential.

Continuity equations:

\[
\frac{\partial p}{\partial t} = - \frac{1}{q} \text{div } J_p + G_p - U_p \tag{3.55a}
\]

\[
\frac{\partial n}{\partial t} = - \frac{1}{q} \text{div } J_n + G_n - U_n \tag{3.55b}
\]

where \(G_p\) and \(G_n\) are the hole and electron generation rate, and \(U_p\) and \(U_n\) are the recombination rates respectively.

\[
U_p = U_n = \frac{pn - n_i^2}{\tau_p(n + n_i) + \tau_n(p + n_i)} \tag{3.56a}
\]

\[
G_p = G_n = 0 \tag{3.56b}
\]

where \(\tau_p\) and \(\tau_n\) are hole and electron minority-carrier lifetimes, respectively.

Poisson's equation:

\[
\text{div grad } \phi = - \frac{q}{\varepsilon_s} (N_d - N_a + p - n) \tag{3.57}
\]
Mobilities are electrical field dependent and are expressed as

\[
\mu_p = \mu_{p_0} \frac{1}{1 + \left| \frac{E}{2V_s} \left( \mu_{p_0} + \mu_{n_0} \right) \right|}
\]

\[
\mu = \mu \frac{1}{1 + \left| \frac{E}{2V_s} \left( \mu_{p_0} + \mu_{n_0} \right) \right|}
\]

where \( \mu_{p_0} \) and \( \mu_{n_0} \) are the hole and electron low-field mobilities, respectively, and \( V_s \) is the saturated velocity, while the diffusion constants are electrical field independent:

\[
D_p = \frac{kT}{q} \mu_{p_0}
\]

\[
D_n = \frac{kT}{q} \mu_{n_0}
\]

Instead of the standard finite difference simulation method, a different approach was used. The device was divided into large regions with a relatively small number of mesh points. Linearization between points was performed and analytical solutions were calculated. An explicit iterative procedure was used.
3.3.2 Results: Steady-state and Transient Analysis

Punch-through space-charge limited loads were simulated using the GESIM1 program. The one-dimensional simulations gave the results discussed below.

Figure 3.12 shows the J-V characteristics of a n^+p^-n^+ punch-through, space-charge limited load (PTSCLL): the spacing between the n^+ regions L = 3 μm and the background substrate concentration of the p-region as a parameter varying from $10^{13} - 2 \times 10^{14}$ cm$^{-3}$. As can be seen, the punch-through voltage increases with the increase of the p-region's concentration as was predicted from the definition of the punch-through voltage in Eq. (3.6). Moreover, the incremental resistance is not a strong function of the substrate concentration. This is evident from Fig. 3.12.

Figure 3.13 shows the J-V characteristics from the steady-state simulation of the n^+p^-n^+ PTSCLL with the spacing L varying from 1 μm to 6 μm and $N_{BC} = 5 \times 10^{13}$ cm$^{-3}$. The resistance is seen to increase as the spacing increases which was predicted theoretically and given in Eq. (3.19).

In case of integrated circuits not the value of the incremental resistance ($dV/dI$) is of importance. Therefore, a comparison of results from Equations (3.19), (3.22) and numerical simulation for the incremental resistance as a function of spacing are shown in Fig. 3.14 for a current density of 100 amp/cm$^2$ and $N_{BC} = 5 \times 10^{13}$ cm$^{-3}$. It shows that the numerical simulation curve is intermediate between the
Fig. 3.12 J-V Characteristics of Punch-Through Space-Charge Limited Loads
Fig. 3.13 Steady-State Analysis of Punch-Through Structure; J-V Characteristics.
Fig. 3.14 Punch-Through Structure; Incremental Resistance vs. Spacing Between Anode and Cathode.
two cases caused by assuming that the velocity of injected electrons is $\mu_n E$ or $V_{Sat}$. Figures 3.15 through 3.18 show the calculated static variations of potential, electric field, space-charge and minority carrier concentration (electrons) for the n$^+p^-n^+$ PTSCELL as a function of distance along the channel for different voltages or spacings using GESIM1.

Figures 3.15 (a) and (b) show plots of the potential versus distance for an n$^+p^-n^+$ PTSCELL with $N_{BC} = 5 \times 10^{13} \text{cm}^{-3}$ for various voltages and $L = 3 \text{micrometer (a)}$ and for various values of $L$ and $V = 1 \text{volt (b)}$. The metallurgical cathode or source junction is at $x = 2 \text{micrometer}$. These simulation shows that the potential in Fig. 3.15(a) drops due to the space charge close to the cathode/source junction and then it rises to the applied value at the anode junction at $x = 5 \mu m$. The magnitude of the potential barrier height shown in Fig. 3.15(b) is seen to decrease from $-0.17 \text{v}$ at $L = 6 \mu m$ to zero at $L = 1 \mu m$ due to source electrons and small dimensions. Obviously the space charge due to injected electrons has a considerable effect on the device performance.

Figures 3.16 (a) and (b) show the electric field distributions for the conditions mentioned with respect to Fig. 3.15 (a) and (b) respectively. Note that the space charge close to the cathode gives rise to a retarding force acting on the electrons. This has to be overcome by the
(a) Potential Distribution; V is a Parameter.

Fig. 3.15 Steady-State Analysis of PTSCLL; Potential Distribution.
(b) Potential Distribution; L is a Parameter.

Fig. 3.15 (Continued)
Electric field, V/cm (x10^4)

Spacing L = 3 \mu m

n^+ p^- n^+ structure
N_{BC} = 5 \times 10^{13} \text{ cm}^{-3}

(a) Electric Field; L = \mu m, V is a Parameter.

Fig. 3.16 Steady-State Analysis of PTSCLL; Electric Field Distribution.
(b) Electric Field; $V = 1$ Volt, $L$ is a Parameter.

Fig. 3.16 (Continued)
The 1-D simulation predicts performance that will be very different from a resistor.

Figures 3.17 (a) and (b) show space charge concentrations as a function of distance for the same parameter variables as in the preceding figures. Note the dipole like distributions close to each metallurgical junction and the negative charge in the channel region caused by the electrons flowing to the anode.

Figures 3.18 (a) and (b) show the electron concentration in the p- region as a function of distance for the conditions previously identified. It is interesting to note that the electrons concentration is predicted to be larger than the acceptor impurity concentration.

Summarizing, the simulation shows that a space-charge generated potential barrier exists very close to the cathode/source region. On the left side of the potential barrier the electric field is positive, thereby retarding electrons. On the other side of the barrier electrons are swept to the anode/drain. In the lightly doped p-region the electron concentration is much larger than the intrinsic concentration and the donor impurity concentration, even for the 7 \( \mu \)m structure. Thus, there are more electrons in the p- region than is the case for the usual p-n junction. That can also explain the existence of current flow even before "punch-thorugh" occurs, \( V < V_{pt} \).
(a) Space-Charge; $L = 3 \mu m$, $V$ is a Parameter.

Fig. 3.17 Steady-State Analysis of PTSCLL; Space-Charge Concentration vs. Distance.
(b) Space-Charge; $V = 1$ Volt, $L$ is a Parameter.

Fig. 3.17 (Continued)
Fig. 3.18 Steady-State Analysis of PTSCLL; Minority Carrier Distribution.

(a) Minority Carrier Distribution; \( L = 3 \ \mu \text{m} \), \( V \) is a Parameter.
(b) Minority Carrier Distribution; $V = 1\text{ Volt}$, $L$ is a Parameter.

Fig. 3.18 (Continued)
Transient analysis 1-D simulations of punch-through space charge limited loads was also performed. Results of simulating a 6 μm p+n-p+ PTSCLL are shown in Figures 3.19 and 3.20. Figure 3.19 gives the carrier distribution versus distance during switching from 2 to 10 volts as a function of time in 30 psec increments. Figure 3.20 presents the charge distribution for the same operating conditions. As can be seen, the time predicted for the device to reach steady state is comparable with the dielectric relaxation time, and is of the order of picoseconds. Therefore, this device can be considered to be very fast. Also it should be pointed out that during the operation both the cathode/source and anode/drain are surrounded by thick depletion layers; therefore, the parasitic capacitance to the substrate is very low.

3.4 Design and Fabrication of PTSCLL

3.4.1 Design

Punch-through space-charge limited loads of various configurations were designed. The main parameters of concern for the design consideration are the spacing between cathode/source and anode/drain L, the background substrate concentration N_{BC}, the junction depth and the geometry of cathode/source and anode/drain. Cathode/source and anode/drain doping concentrations are of less importance. Their doping concentration if large has little effect on the
Fig. 3.19 Transient Analysis of Punch-Through Structure; Minority Carriers Distribution
Fig. 3.20 Transient Analysis of Punch-Through Structure; Space-Charge Analysis.
performance of the device. It is desirable that the device be symmetric so the I-V characteristic is symmetrical.

It is recommended that the PTSCLL be operated deep in the space-charge limited flow region where the applied bias is larger than the flat-band voltage. The advantages are a low temperature coefficient and an incremental resistance that is directly controlled by the total applied voltage as can be seen from Eq. (3.19). In this operating mode the injected mobile carrier density from the injecting electrode (cathode/source) into the channel (substrate) is much larger than the ionized impurity density. Therefore, the substrate concentration of ionized impurities can be neglected. Consequently, the effect of substrate concentration on the resistance is essentially eliminated. The mobility of the injected mobile carriers is dependent on the substrate concentration; however, it is constant over a wide range of moderate concentrations. Therefore, the mobility is assumed to be a function of temperature only.

Returning to Eq. (3.19), the resistance is proportional to $L^3$ and inversely proportional to the cross-sectional area as well as the applied voltage. For a desired value of $R$, $L$ can be calculated as a function of the area and the applied voltage as follows:

$$L = (9 \frac{\mu_n \epsilon_s A VR}{4})^{1/3}$$  (3.60)
The cross-section area is defined mainly by the geometry or width of the cathode/source and anode/drain junctions. It is recommended that this be made small so that larger incremental resistances and smaller capacitances are obtained resulting in faster switching speeds and small surface area devices. It is desirable to operate the PTSCLL in the space charge limited flow region. This will result in fast large values resistors in small surface areas. The applied voltage can also be small. To attain this mode, the minimum value of \( V \) should be larger than the flat-band voltage.

The flat-band voltage defined in Eq. (3.13) depends on the background concentration as well as the spacing \( L \) squared. To sustain the space-charge limited flow condition and obtain large value resistors, the background concentration should be minimized. Then the flat-band voltage is reduced. Note that a desire to reduce device dimensions and operating voltages will enhance PTSCLL operating performance. Thus the device is compatible with IC development.

The junction depths of cathode/source-substrate and anode/drain-substrate are preferred to be shallow. Then the lateral dimensions (channel length and width) are much larger than the vertical ones (junction depth and oxide thickness). The short channel effects are reduced and the
two-dimensional effects from the interface charges are reduced as well.

Capacitance Calculations

Figure 3.21 shows a cross-sectional view of the PTSCLL. Also illustrated in the figure are the parasitic depletion region capacitances \( C_{cs} \), \( C_{os} \), and \( C_{as} \) between the cathode/source and substrate, the oxide and substrate, and the anode/drain and substrate regions, respectively.

If a positive voltage is applied to the anode/source terminal, the cathode/source-substrate junction is forward biased with a voltage drop \( V_F \). The anode/drain-substrate junction is reversed biased with a voltage drop \( V_R \). The depletion regions associated with each junction are respectively

\[
W_1 = \left[ \frac{2\varepsilon_S (V_{bi} - V_F)}{q N_A} \right]^{1/2} \quad (3.61)
\]

and

\[
W_2 = \left[ \frac{2\varepsilon_S (V_{bi} + V_R)}{q N_A} \right]^{1/2} \quad (3.62)
\]

These depletion widths \( W_1 \) and \( W_2 \) were obtained under the assumption that the channel is not completely depleted and the cathode/source and anode/drain are heavily doped. Then the depletion region extends into the p-type substrate only since \( N_D >> N_A \).
Fig. 3.21 Cross-Sectional View of PTSCLL
Including the Capacitances
(Parasitic)
Since there is a voltage-dependent charge $Q$ associated with the depletion region, the small-signal capacitance is

$$C = \frac{dQ}{dV} = \frac{dQ}{dW} \frac{dW}{dV}$$  \hspace{1cm} (3.63)

The charge is

$$dQ = A q N_A dW$$  \hspace{1cm} (3.64)

From Equations (3.61) through (3.64), the capacitances $C_{cs}$ and $C_{as}$ can be determined.

$$C_{cs} = \frac{dQ_1}{dV_F} = \frac{dQ_1}{dW_1} \frac{dW_1}{dV_F} = \frac{C_{cso}}{(1 - \frac{V_F}{V_{bi}})^{1/2}}$$  \hspace{1cm} (3.65)

and

$$C_{as} = \frac{C_{aso}}{(1 + \frac{V_R}{V_{bi}})^{1/2}}$$  \hspace{1cm} (3.66)

where $C_{cso}$ and $C_{aso}$ are the values of $C_{cs}$ and $C_{as}$ for $V_F$ and $V_R$ equal to zero, respectively.

The capacitance associated with the depletion region under the oxide $C_{os}$ is a function of the properties of the
field oxide grown at the surface and does not depend on the applied voltage bias. Therefore, $C_{OS}$ is a constant with respect to device biasing.

The depletion region is associated with the properties of the SiO$_2$ dependent charge, $Q_3$, defined by

$$Q_3 = A q N_A W_3$$  \hspace{1cm} (3.67)

where $W_3$ is the depletion width caused by the potential due to the oxide and interface charges. This is illustrated in Fig. 3.21. A corresponding potential is given by

$$\phi_0 = \frac{q N_A W_3^2}{2 \varepsilon_s}$$  \hspace{1cm} (3.68)

Equation (3.68) can now be solved for the depletion width $W_3$.

$$W_3 = \left[ \frac{2 \varepsilon_s \phi_0}{q N_A} \right]^{1/2}$$  \hspace{1cm} (3.69)

The capacitance $C_{OS}$ per unit area can now be obtained from Eqs. (3.67) and (3.69)

$$C_{OS} = \frac{Q_3 W_3}{W_3} = \left[ \frac{2 \varepsilon_s q N_A}{\phi_0} \right]^{1/2}$$  \hspace{1cm} (3.70)
3.4.2 Fabrication

Punch-through space-charge limited loads of various configurations were fabricated and tested. Two designs of the structures are shown in Figures 3.22 and 3.23. Devices were fabricated with various spacing between the cathode/source and anode/drain: 2, 3, 4, 5, 6, 8, and 10 μm.

The devices were fabricated in p-type silicon substrates as well as n-type. The orientation of the substrates were <111> with a wide range of resistivities. The field oxide was thermally grown at 1100 degrees Celsius in wet atmosphere. Pre-implant oxidation was performed at 1100 degrees Celsius in a dry atmosphere followed by the implantation for cathode/source and anode/drain. The implant energy was 80 Kev and implant dose of 5×10^{15} atoms/cm² were used. Annealing was performed at 900 degrees Celsius in a nitrogen environment for 30 minutes followed by drive-in at 1100 degrees Celsius in a nitrogen ambient for 20 minutes. Evaporated aluminum was deposited for contacts and connections.

3.4.3 Experimental Evaluation

After the field oxidation step, the oxide thickness was 5000 Angstrom measured using a color chart. The pre-implant oxide thickness was maintained around 700-800 Angstrom such that the gaussian profile of the implanted junction was sustained. Using the groove and stain
Fig. 3.22  PTSCLL Structure; Preliminary Design.
Fig. 3.23 PTSCLL Structure; Revised Design.
techniques for measuring the cathode/source and anode/drain junction depths resulted in a value of 0.5 \( \mu \text{m} \). The sheet resistance was 5 \( \Omega/\text{square} \) measured using the four point probe method. Finally, the evaporated aluminum thickness was 3000 Angstrom measured using the Tencore Alpha Step profile measurement.

Electrical measurements of the I-V characteristics of the preliminary design in Fig. 3.22 shows a nonsymmetrical characteristic. Therefore this design was replaced with the revised design shown in Fig. 3.23. This structure exhibited a symmetrical I-V characteristic. The I-V characteristics of the latter design for the n+p-n+ structure with background concentration of \( 8 \times 10^{12}/\text{cm}^{-3} \) and spacing of 4 (upper curve), 6, 8 and 10 \( \mu \text{m} \) (lowest curve) is shown in Fig. 3.24. The horizontal scale is 5\( \text{v/div} \) and vertical scale is 0.1\( \text{ma/div} \). The incremental resistance for the 10 \( \mu \text{m} \) device is 125k\( \Omega \) over a range of 20 volts. Table 3.3 shows a summary of the experimental results for both designs shown in Figures 3.22 and 3.23 for an n\textsuperscript{+}p-n\textsuperscript{+} structure.

3.5 Comparison of Theoretical and Experimental Results

Two analytical models were developed (Section 3.2) describing the I-V relationship of the punch-through space-charge-limited loads. The first is a quasi-two-dimensional
Fig. 3.24  I-V Characteristics of the Structure from Fig. 3.23
4 μm Spacing Upper Curve and 10 μm Spacing in
Lowest Curve. $N_{BC} = 8 \times 10^{12}/\text{cm}^3$
Table 3.3 Summary of Experimental Results;
Values of Incremental Resistance (Ω)

<table>
<thead>
<tr>
<th>Background Concentration (cm⁻³)</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>8</th>
<th>10</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 x 10¹³</td>
<td></td>
<td></td>
<td>8.8K</td>
<td>14.0K</td>
<td>23.3K</td>
<td></td>
<td></td>
<td>Fig. 3.22</td>
</tr>
<tr>
<td>1 x 10¹³</td>
<td>8.0K</td>
<td>9.0K</td>
<td>14.0K</td>
<td>18.0K</td>
<td></td>
<td></td>
<td></td>
<td>Fig. 3.22</td>
</tr>
<tr>
<td>8 x 10¹²</td>
<td></td>
<td></td>
<td>67.6K</td>
<td></td>
<td>73.5K</td>
<td>96.0K</td>
<td>156.0K</td>
<td>Fig. 3.23</td>
</tr>
</tbody>
</table>
model (Section 3.2.1). In this model the effect of the interface charges existing in the silicon dioxide and at the silicon/SiO$_2$ surface are included. These charges give rise to a potential drop at the silicon-silicon dioxide interface. This potential leads to a depletion of carriers from the surface and vertical electric field component. This effect is included by solving the two dimensional Poisson's equation for the potential distribution and, therefore, the I-V relationship. This model has been described earlier in Chapter 2.

The second analytical model is a one-dimensional model that includes the effect of mobile carriers on the I-V characteristics. This model was obtained by solving the one-dimensional Poisson's equation including a term to account for the mobile carriers injected into the channel. This model has been described in Chapter 2.

Comparison of the experimental I-V characteristics with the theoretical models will be offered in the following manner: first with the two-dimensional analytical model, then, with the one-dimensional model. Finally, a comparison of the experimentally observed temperature effects on the I-V characteristics will be presented.

Figures 3.25 (a), (b), (c), and (d) show a comparison of the experimental I-V characteristics with the two-dimensional analytical model results for four different spacing: 4, 6, 8 and 10 µm, two different background
Fig. 3.25 Comparison of the Experimental I-V Characteristics with the Theoretical Two-Dimensional Analytical Model.

(a) \( N_A = 5 \times 10^{13} \text{cm}^{-3}, \ L = 4, 8 \ \mu\text{m} \)

\[ N_A = 5 \times 10^{13} \text{cm}^{-3} \]

--- Theoretical

xxxx Experimental

---

\( L = 4 \ \mu\text{m} \)

\( L = 8 \ \mu\text{m} \)
$N_A = 5 \times 10^{13} \text{ cm}^{-3}$

- Theoretical
- Experimental

**Fig. 3.25 (Continued)**

$(b) N_A = 5 \times 10^{13} \text{ cm}^{-3}, L = 6, 10 \text{ } \mu\text{m}$
$N_A = 3 \times 10^{14} \text{cm}^{-3}$

---

Theoretical

xxxx Experimental

---

Fig. 3.25 (Continued)

(c) $N_A = 3 \times 10^{14} \text{cm}^{-3}$, $L = 4, 8 \text{ } \mu\text{m}$
N_A = 3 \times 10^{14} \text{cm}^{-3}

--- Theoretical

xxxx Experimental

L = 6 \mu m

L = 10 \mu m

(d) N_A = 3 \times 10^{14} \text{cm}^{-3}, L = 6, 10 \mu m

Fig. 3.25 (Continued)
concentrations: $5 \times 10^{13}$ and $3 \times 10^{14}$ cm$^{-3}$, with the surface potential of 0.5 volt. The value of $y_0$ increases as the spacing increases as predicted and expected. The experimental and theoretical results match very well except at very low applied voltages and at very high voltages. The former discrepancy is due to the fact that the analytical model does not apply for voltage biases below the punch-through voltage where the surface potential is dominant. The latter discrepancy is due to the fact that the mobile carriers become significant for voltages around and above the flat-band voltage. This quasi 2-D analytical model does not take mobile carriers into account. In the high applied voltage region, $V > V_{FB}$ the theoretically obtained current is larger than the experimental current. The experimental current is limited by the mobile carriers space-charge cloud in the channel therefore retarding further injection of such carriers. Consequently, the current is less than the value that the analytical model predicts.

Figure 3.26 shows a comparison between the experimental I-V characteristics with the one-dimensional model predictions taking the effect of mobile carriers into account. The mismatch of the two curves is in the low voltage region. This discrepancy is due to two effects. The first is that the analytical model does not hold for voltages below the punch-through voltage where the current
Fig. 3.26  Comparison of Experimental I-V Characteristics with the One-Dimensional Analytical Model that Takes the Effect of Mobile Carriers into Account.
is considered to be thermal generation current. The second effect is due to the fact that the observed experimental current is composed of two components: current flowing in the substrate bulk controlled by the applied bias and another component close to the surface caused by the induced surface potential. The mobile carriers analytical model does not account for the second component of current. Therefore, the magnitude of the theoretically obtained current is less than the experimentally observed current. As the applied bias is increased, the bulk or substrate current component becomes more dominant until we reach a point where the surface induced current becomes negligible. The good agreement at high voltages can be seen.

Figure 3.27 shows a comparison of the experimental I-V characteristics of the PTSCLL with the theoretical results obtained from the two-dimensional model for four different values of temperature; that is, 300, 330, 360 and 375 °K. The spacing between cathode and anode is 6 μm and the background concentration is 3 \times 10^{14} \text{ cm}^{-3}.

As can be seen from the figure, a good agreement is established in the intermediate applied bias voltage region where only the substrate ionized impurities are significant. In this region of operation the mobile carriers are negligible. However, at the high applied bias, the mobile carrier density increases and becomes important. Accordingly, for large V the experimental current is space-
xxx Theoretical

- Experimental

\[ N_A = 3 \times 10^{14} \text{cm}^{-3} \]
\[ \phi_0 = 0.5 \text{ V} \]
\[ y_0 = 0.8 \mu \text{m} \]
\[ L = 6 \mu \text{m} \]

Fig. 3.27 Comparison of the I-V Characteristics of the PTSCLL with the Two-Dimensional Analytical Model with the Temperature as a Parameter.
charge limited, and therefore shows a disagreement with the 2-D model.

The current is seen to increase as the temperature increases leading to a positive temperature coefficient. The incremental resistance is a decreasing function of temperature and exhibits a negative temperature coefficient.

3.6 Comparison of Punch-through Space-charge Limited Load with Available Standard IC Loads

Standard integrated circuit resistors are generally fabricated using one of the diffused layers formed during the fabrication process, or in some cases a combination of two diffused layers. The layers available in bipolar technologies for use as resistors include the base diffusion, emitter diffusion, epitaxial layer, the active-base region layer of a transistor, and the epitaxial layer pinched between the base diffusion and the p-type substrate. In the case of MOS technologies, the layers available to the designer include diffused polysilicon and p or n-well. The choice of layer generally depends on the type of technology as well as on the value, tolerance, and temperature coefficient of the resistor required.

The type of standard IC resistors that can be created from the above process technologies can be characterized based on the maximum value that can be
attained in a reasonable surface area, speed, complexity of the process, etc.

1. Diffused Resistors:

Diffused resistors in bipolar technology are formed from the p-type base or the n-type emitter diffusion. The diffused layer used to form the source and drain is used in the case of MOS processes. Diffused resistors in general are simple to design and easy to fabricate. They sustain linear I-V characteristics and are process compatible with bipolar and MOS techniques. However, they require large areas in order to achieve large resistance values. This results in a large sidewall capacitance.

2. Base Pinch Resistors:

This type of resistor is formed from the layer of the active bipolar base region. This layer is "pinched" between the emitter and the collector regions, giving rise to the term pinch resistor. The resulting sheet resistance is large, so that it allows the fabrication of large values of resistance. However, the sheet resistance undergoes the same process-related variations as does the $Q_B$ of the transistor, which is approximately $\pm 50$ percent. Also, the resulting resistance displays a relatively large variation with temperature because of the relatively light doping in the base. Another significant drawback is the limitation
to low operating voltage (~6V) because of the breakdown voltage of the emitter-base junction.

3. Epitaxial and Epitaxial Pinch Resistors:

Epitaxial resistors are formed using the epitaxial layer in the case of bipolar technology. The epitaxial pinch resistor is created between the base of the bipolar transistor and the substrate.

Large values of resistance can be realized in a small area using these structures. Again, because of the light doping in the resistor body, these resistors display a rather large temperature coefficient. Furthermore, the epitaxial layer is not required in most of the process technologies.

4. Polysilicon Resistors:

Usually one layer of polysilicon is required in silicon-gate MOS technologies to form the gates of the transistors. This layer is often used to form this type of resistor. Otherwise, an extra processing step is required.

Large values of resistance can be realized in a relatively small area. However, the polysilicon process is complicated. It is not easy to control the dopant in polysilicon. Moreover, the resistance value not only depends on the impurity concentration, but also on the grain size of the polycrystalline silicon. The resistor exhibits
a parasitic capacitance as in the case of diffused resistors.

5. Well Resistors:

In MOS technologies the well region can be used as the body of a resistor. It is a relatively lightly doped region, therefore, it provides a large sheet resistance. It is much like the epitaxial resistor. However, it displays large tolerance, high voltage coefficient and very high temperature coefficient.

6. MOS Devices as Resistors:

The MOS transistor biased in the triode region is used in many circuits to perform the function of a resistor. The effective sheet resistance is a function of the applied gate bias and can be much higher than polysilicon or diffused resistors. Therefore, large values of resistance can be implemented in a small area. However, the high degree of nonlinearity of the resulting resistor element as well as the extra gate electrode properties makes it undesirable.

7. PTSCLL as Resistors:

Punch-through space-charge limited load can be used to perform the function of a resistor. The effective sheet resistance is a function of the applied anode/drain bias. It is effectively much higher than the sheet resistance of
any of the above listed resistors, allowing large values of resistance to be implemented in a very small area. Since the area consumed is very small, the parasitic capacitance is very small and very fast switching speeds are achieved.

The process of the PTSCLL is simple and does not require any extra steps in most IC processes. It is compatible with both bipolar and MOS technologies. Furthermore, the bias signals applied to the PTSCLL can be very large because of the large breakdown voltage of the contact substrate junctions and the very high power capabilities of the device.

Since the sheet resistance is a function of the applied bias, the incremental resistance is also a function of the applied voltage. Therefore, PTSCLLs might be used as a variable resistor controlled by the voltage applied between the source-drain terminals. Moreover, the resistance is a very strong function of the spacing between cathode and anode; it increases rapidly as L increases because of the third power dependence on L. A relatively low temperature coefficient especially if it is operated in the space-charge limited flow mode is also realized. The principle drawback of this form of resistor is the non-linearity of the I-V characteristics. Nevertheless, it sustains a linear portion over a wide range of operating voltages. Low substrate concentrations are required to achieve large values of resistors unless very small
geometries are used such as a micron or submicron dimensions.
CHAPTER 4

SUMMARY AND CONCLUSIONS

Knowledge of device kinetics, structure, electrical behavior, and other physical properties is vital for understanding and tailoring the load properties to the need of the design and the fabrication process. Only the demonstration of working devices can provide the ultimate test of integrated circuit performance. Electrical modeling can provide faster, but nonetheless accurate, information about the device properties if the models are good. Otherwise devices must be evaluated using alternative methods. The models can be related to geometry and processing, the spacing between cathode and anode and the background substrate concentration for example. Electrical evaluations of the I-V characteristics of the PTSCLL can provide information about the model and the effect of the substrate concentration on the resistance; and geometry.

This chapter summarizes the results of the measurements to evaluate the performance of the devices that has been fabricated in the Microelectronics Laboratory of the University of Arizona. Conclusion based on this work as well as suggestions for further investigations are also given in this chapter.

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4.1 Summary of Experimental Results

The goal of this work was to investigate and characterize the Punch-Through Space-Charge Limited Loads for use as replacements for large value integrated circuit resistors in silicon VLSI circuits specifically and ICs in general. Therefore, it is essential to investigate the effect of geometry and processing on the performance of the device.

(a) Effect of Geometry on the I-V Characteristics:

Figures 4.1 through 4.3 show the experimental I-V characteristics of the PTSCLL for three substrate concentrations: 5x10^13, 2x10^14 and 3x10^14 cm^-3 respectively. In each case the spacing is varied from L = 4 micrometer to L = 10 micrometer in increments of 2 micrometer. The slope of the I-V curve (slope is the reciprocal of the incremental resistance) decreases as the spacing increases. For example R is seen to increase from 70 kohms at L =4 micrometer to 78 kohms at L = 6 micrometer with the substrate concentration kept at a constant level of 2x10^14 cm^-3 as shown in Fig. 4.2.

The I-V characteristic is quite linear at moderate doping levels (in the 10^14 cm^-3 range) over a wide range of applied bias. It is seen to exhibit exponential type for low bias voltages at low doping levels (in the 10^13 cm^-3
Fig. 4.1 Experimental I-V Characteristics of the PTSCLL with Substrate Concentration of $5 \times 10^{13} \text{ cm}^{-3}$ and $L$ is a Parameter.
Fig. 4.2 Experimental I-V Characteristics of the PTSCLL with $N_{BC} = 2 \times 10^{14} \text{cm}^{-3}$ and $L$ is a Parameter.
Fig. 4.3 Experimental I-V Characteristics of the PTSCELL with $N_{BC} = 3 \times 10^{14} \text{cm}^{-3}$ and $L$ is a Parameter.
range) while linear for high applied voltage. This effect can be attributed to the transport mechanisms of carriers where thermionic emission or diffusion is the dominant effect on the carrier's motion for bias levels between punch-through and flat-band. At higher (moderate) doping levels, it is seen that a different mechanisms are inherent in the transport such as interface charges where it is significant at low biases and moderate doping concentrations.

(b) Effect of Substrate Concentration from I-V Measurement:

The substrate concentration has an effect on the transport of carriers and, therefore, the shape of the I-V curve. The resistance as a function of concentration can be described.

Fig. 4.4 shows the experimental I-V characteristic of the PTSCLL. Three curves are shown for substrate concentrations of $5 \times 10^{13}$, $2 \times 10^{14}$ and $3 \times 10^{14}$ cm$^{-3}$ while $L$ is kept constant at 4 micrometer. Figures 4.5 through 4.7 show the I-V characteristics of the PTSCLL with the same specifications given in Fig. 4.4 except that the spacing between cathode and anode has been changed to $L = 6$ micrometer in Fig. 4.5, $L = 8$ micrometer in Fig. 4.6 and $L = 8$ micrometer in Fig. 4.7.
Fig. 4.4 Experimental I-V Characteristics of the PTSCLL with $L = 4$ micrometers and $N_{BC}$ is a Parameter.
Fig. 4.5 Experimental I-V Characteristics of the PTSCLL with \( L = 6 \) micrometers and \( N_{BC} \) is a Parameter.
Fig. 4.6 Experimental I-V Characteristics of the PTSCLL with $L = 8$ micrometers and $N_{BC}$ is a Parameter.
Fig. 4.7 Experimental I-V Characteristics of the PTSCLL with $L = 10$ micrometers and $N_A$ is a Parameter.
The slope of the I-V curve decreases drastically as the substrate concentration increases from $5 \times 10^{13}$ cm$^{-3}$ to a value of $2 \times 10^{14}$ cm$^{-3}$. The resistance changes from a value of 21 kohms at $N_A = 5 \times 10^{13}$ cm$^{-3}$ to a value of 76 kohms at $N_A = 2 \times 10^{14}$ cm$^{-3}$ with $L$ being constant at 8 micrometer. The drastic increase in the resistance or the decrease in the current is due to the fact that the potential barrier lowering is inversely proportional to the substrate concentration as well as the large contribution of this concentration to the flat-band voltage. The current is found to depend on the flat-band voltage as follow:

$$I = I_0 \exp\left[-(V_{FB}-V)^2/(4V_{FB}V_T)\right]$$

where $V$ is the applied voltage, and $V_T$ is the thermal voltage. Finally, as the substrate concentration increases, the punch-through voltage increases resulting in the low currents observed.

(c) Effect of Bias Voltage on the Incremental Resistance:

It was shown in Chapter 3 that the incremental resistance is inversely proportional to the applied voltage. This is observed experimentally and is illustrated in Fig.4.8. A plot of the experimentally obtained incremental resistance vs. the applied voltage bias with $L = 4$ micrometer and $N_A = 5 \times 10^{13}$ cm$^{-3}$ is depicted. The resistance is seen to decrease as the applied voltage increases, and it
Fig. 4.8 Experimentally Obtained Resistance vs. the Applied Voltage Bias with $L = 4$ micrometer and $N_A = 5 \times 10^{13} \text{cm}^{-3}$. 

$N_A = 5 \times 10^{13} \text{cm}^{-3}$

$L = 4 \ \mu\text{m}$
seems to level-off at high voltages. In the high voltage regime, the electric field is very large and velocity saturation occurs. In this regime the relation between the observed current and the applied voltage becomes linear and the incremental resistance is independent of the applied bias as predicted by the one-dimensional model in Chapters 2 & 3.

4.2 Conclusions and Suggestions for Further Investigations

Based on the given results, it can be concluded that Punch-Through Space-Charge Limited Loads (PTSCLL) appear to be useful as substitutes for current commercially available diffused or polysilicon resistors used in Integrated Circuits. In particular for VLSI circuits the reduced PTSCLL geometries provide a substantially larger resistance values when compared with integrated circuit resistors. This can provide improved circuit performance. Large values of resistance in relatively small area satisfies the need to realize large packing densities on a chip. A comparison between the PTSCLL and a dogbone shape diffused resistor using 1 micrometer geometry was undertaken. Each had a resistance value of 120 kilohms. The PTSCLL showed an improvement compared with the diffused resistor with a factor of 13 reduction in the area consumed.
Three analytical models were presented in this study to describe the I-V characteristics and the behavior in the PTSCLL. The first was a one-dimensional solution of Poisson's equation. This model consists of two parts corresponding to two regions of operation of the PTSCLL. The first part is for small voltages, the region below the flat-band voltage condition. This part of the model was derived using the depletion approximation and is valid for applied voltages below the flat-band voltage. The current was shown analytically to depend exponentially on the square of the potential barrier height. The current increases as the barrier height is decreased by the applied voltage. The second part of this model is valid for voltages well above the flat-band voltage. The mobile carriers are the dominant factor and space-charge-limited flow is the main principle of carrier transport.

For this model the current was found to depend on the square of the voltage for the low field case. The current is a linear function of voltage for the high field regime when the velocity of carriers reaches the saturation limit. The failure of this model in the region around the flat-band condition is attributed to the fact that the mobile carrier density is comparable to the ionized impurity density and both densities must be included in the solution. Nonetheless, this model offers a fairly good description of the device behavior and is a very simple model.
The second model results from a one-dimensional solution of Poisson's equation as well. But it accounts for the ionized impurities as well as for the mobile carriers over the whole region of bias operation. Therefore, it is a more exact solution and offers a good description of the I-V characteristics of the PTSCLL. Furthermore, this model is applicable to other semiconductor devices such as MOS and bipolar transistors. There is good agreement of this model with the measured I-V characteristics for intermediate and high voltage regimes. At very low voltages there is a discrepancy between the theory and experiment due to an effect which is accounted for by the third model.

The third and last model is a quasi two-dimensional model. This model is especially useful to predict the I-V characteristic of PTSCLLs at low applied voltages. It includes the surface effects caused by oxide and interface charges. They create a channel between the cathode/source and anode/drain allowing a flow of current even at voltages well below the punch-through voltage. A two-dimensional Poisson's equation was solved taking all charges into account. The equation was transformed into a one-dimensional equation. It was solved to give a general quasi-two-dimensional expression for the potential distribution and the I-V relationship. This model is valid only for biases below the flat-band voltage where the mobile carriers are not significant. It is followed by a second expression to
account for the region above flat-band condition. This model gave a relatively good agreement with the observed experimental results. It offers a good description of the potential distribution and barrier height behavior in the channel region. The current was found to depend exponentially on the barrier height lowering such that any small change in the barrier height causes a drastic change in the current.

It can be concluded that the resistance increases as the substrate concentration increases for the region of operation below flat-band conditions. The reason behind this effect is that the current is delayed to flow as the applied voltage progresses further, and thereby, a larger voltage is required for sufficient current to flow. On the other hand, for regions of bias above flat-band condition, the current and, thereby, the resistance, become relatively independent of the substrate doping and the current carriers are ultimately the mobile carriers. The flow of current is space-charge limited.

The resistance was found to increase as the cathode-anode spacing increases. The resistance was obtained to have a linear dependence on \( L \) for bias regions below flat-band conditions while it was obtained to have \( L^3 \) dependence for bias regions above flat-band conditions.

Furthermore, the resistance was also obtained to have an inverse dependence on the bias voltage for the
punch-through space-charge limited flow region (i.e., region of bias above flat-band voltage) and low field case. However, for high field case the velocity of carriers reaches its saturation limit, and the resistance is independent of bias conditions.

To achieve very large resistance values three approaches can be pursued:

1) Starting with a moderate doping concentration (10^{14} range), and moderate spacing (between 5 and 10 micrometer), then, operate the device in the region below the flat-band voltage.

2) Starting with a moderate concentration as in Step 1 but with smaller spacing, then operate the device in the regime above the flat-band voltage.

3) Starting with a low doping concentration (10^{13} range), and a spacing between 5 and 10 micrometers, then bias the device such that punch-through space-charge regime of operation is attained.

Upon completion of this dissertation, three main suggestions for future improvements come to mind. First, isolate the device from other adjacent devices. This can be done using some type of isolation technique such as a local
oxidation processes or a guard ring type of isolation. If the device is to be used with CMOS technology where wells are required, prevention of latch-up must be considered.

The second recommendation is to start with a low doping concentration and design for small spacing thereby sustaining the punch-through space-charge region of operation. This approach will provide improved speed and packing density.

Third, it is recommended that the field oxide be replaced with a better quality oxide such as a gate oxidation created with an HCL flow along with oxygen. The \(<100>\) crystal orientation for the starting substrate is preferred. These steps will reduce the surface charges thereby reducing the two-dimensional effect giving rise to an improved resistance.
APPENDIX A

Device Simulation Program (GESIM1)

PT.FOR

PROGRAM PT
INCLUDE 'COM.FOR'
COMMON/QWE,' SR
OPEN (UNIT=3, FILE='TEM.DAT', STATUS='OLD')
OPEN (UNIT=5, FILE='IN.DAT', STATUS='OLD')
OPEN (UNIT=6, FILE='OUT.DAT', STATUS='NEW')
OPEN (UNIT=8, FILE='ONN.DAT', RECL=256, STATUS='NEW')
OPEN (UNIT=9, FILE='0FP.DAT', RECL=256, STATUS='NEW')
OPEN (UNIT=11, FILE='EEE.DAT', RECL=256, STATUS='NEW')
OPEN (UNIT=12, FILE='PRP.DAT', RECL=256, STATUS='NEW')
OPEN (UNIT=13, FILE='PRN.DAT', RECL=256, STATUS='NEW')
OPEN (UNIT=14, FILE='PRR.DAT', RECL=256, STATUS='NEW')
OPEN (UNIT=16, FILE='QQQ.DAT', RECL=256, STATUS='NEW')
CALL READWE
CALL DRUKWE
IF (KEY(.EQ. 9) .NE. 9) GO TO 739
EEO = EEO*12.6/11.8
VSAT = 3.0E7
QW = QEL/EEO
QLX = QEL * DX
CF = 0.5 * (UN+UP) / VSAT
QNI = 1.0E7
QNI2 = QNI*QNI
739 CONTINUE
C
SR = 1.0E6
C
DO 306 L = 1,II
C  QQQ(L) = -1.0E9
C306 CONTINUE
IF (QNN(L) .LE. 0) QNN(L) = 1.0
IF (QPP(L) .LE. 0) QPP(L) = 1.0
VFN(L) = -VT* LOG(QNN(L)/QNI) + VVV(L)
VFP(L) = VT* LOG(QPP(L)/QNI) + VVV(L)
EFN(L) = (LOG10(QNN(L)) - 14.0)
EFF(L) = (LOG10(QPP(L)) - 14.0)
DO 112 I = 1,II
QZZ(I) = QPP(I) - QNN(I) + QQQ(I)
112 CONTINUE
C
ITERATION WITH VOLTAGE
DO 200 VE = VV(1), VV(2), VV(3)
C DO 200 JI = 1, 4
C DO 206 L = 1, II
C CONTINUE
LI = 1
CZAS = 0
C
ITERATION WITH TIME
DO 100 J = 1, JJ1
ITE = J
CALL POICON
CZAS = CZAS + T
C IF (ITE .EQ. 1) GO TO 115
IF (ITE .GE. JJ1) GO TO 115
IF (LI .NE. JT1) GO TO 120
LI = LI - JT1
115 CONTINUE
IF (KEY(10) .NE. 10) GO TO 135
WRITE(8,15) (QNN(I), I = 1,II)
WRITE(9,15) (QPP(I), I = 1,II)
WRITE(11,15) (EEE(I), I = 1,II)
WRITE(12,15) (VVV(I), I = 1,II)
WRITE(13,15) (PREO(I), I = 1,II)
WRITE(14,15) (PRH0(I), I = 1,II)
WRITE(15,15) (PRR(I), I = 1,II)
WRITE(16,15) ((QQQ(I)+QPP(I)-QNN(I)), I = 1,II)
135 CONTINUE
IF (KEY(7) .EQ. 7) CALL RYS(1)
IF (KEY(7) .EQ. 5) CALL DRUK
IF (KEY(7) .EQ. 8) CALL RYS(1)
IF (KEY(7) .EQ. 8) CALL DRUK
120 LI = LI +1
100 CONTINUE
200 CONTINUE
REWIND 3
WRITE(3,*) (QNN(K), K=1,II)
WRITE(3,*) (QPP(K), K=1,II)
STOP
12 FORMAT('',9E14.7)
15 FORMAT('',8(2X,E14.7))
END
C
******************************************************************************
********
C END OF MAIN PROGRAM

C

C
SUBROUTINE POICON
INCLUDE 'COM.FOR'
REAL*8 AP1, AP2, AN1, AN2, E1
REAL*8 EP, EM, PP, PM
REAL*8 IQ, SE

POISSON EQUATION

TQX = T/QLX
TEO = T/EEO
CC = 0.0
SE = ES
SV = VS
ESS = ES

DO 100 I = 1, II-1
ZQ = + QW * (QQI(I) - QNN(I) + QPP(I))
C
IQ = + QW * QZ2(I)
SE = SE + IQ * DX
SV = SV - SE * DX
EEE(I) = SE
CC = CC + DX

100 CONTINUE

DV = VE - SV
DE = - DV/CC
SV = VS
V**V(I) = VS

DO 200 I = 1, II-1
SE = EEE(I) + DE
SV = SV - SE * DX
V**V(I+1) = SV
EEE(I) = SE

200 CONTINUE

TRANSPORT EQUATIONS

SLS = 0
AP1 = QPP(I)
AN1 = QNN(I)

DO 110 I = 1, II-1
C2 = (I-1)/II + 0.0
C1 = 1- C2
AN2 = QNN(I+1)
AP2 = QPP(I+1)
E1 = EEE(I)
CD1 = (1 + ABS(CF* E1)) *2
VTI = CD1 * VT
UUN1 = UN/CD1
UUP1 = UP/CD1

DOUBLED CD & VT, HALF OF UU

G1 = - VTI/DX
Z1 = E1/G1
QUN = QEL*UUN1
QUP = QEL*UUP1
\[
\begin{align*}
\text{EF} &= \text{AN2} + \text{AN1} \\
\text{EM} &= \text{AN2} - \text{AN1} \\
\text{PP} &= \text{AP2} + \text{AP1} \\
\text{PM} &= \text{AP2} - \text{AP1} \\
\text{DNE1} &= \text{DNE} \\
\text{DPE1} &= \text{DPE} \\
\text{IF} (\text{ABS}(\text{Z1}) \cdot \text{LT.} \ 0.01) \text{ GO TO 150} \\
&A = \text{EXP}(\text{Z1}) \\
&B = 1/A \\
&C = A - B \\
\text{D} &= A + B \\
\text{G2} &= \text{D} / C \\
\text{C} &= \text{G2} \cdot \text{E1} \\
\text{C} &= 0.5 \cdot \text{SINH}(\text{Z1}) \\
\text{B} &= \text{G2} - 4 \cdot \text{Z1} / (\text{C} \cdot \text{C}) \\
\text{C} &= \text{1/TANH}(\text{Z1}) - \text{Z1} / (\text{SINH}(\text{Z1}) \cdot \text{SINH}(\text{Z1})) \\
\text{DNE} &= \text{QUN} \cdot (\text{EP} - \text{EM} \cdot \text{B}) \\
\text{DPE} &= \text{QUP} \cdot (\text{FP} + \text{PM} \cdot \text{B}) \\
&\text{GO TO 151} \\
\text{150} \text{ CONTINUE} \\
&\text{DNE} = \text{QUN} \cdot \text{EP} \\
&\text{DPE} = \text{QUP} \cdot \text{PP} \\
\text{151} \text{ CONTINUE} \\
&\text{PRN1} = \text{PRN2} \\
&\text{PRP1} = \text{PRP2} \\
&\text{IF} ((\text{KEY}(2) \cdot \text{EQ.} \ 4) \cdot \text{AND.} (\text{ITE} \cdot \text{EQ.} \ 1)) \text{ PRN1} = \text{BETA} \\
&\text{PRN2} = \text{QUN} \cdot (\text{E1} \cdot \text{EP} - \text{G1} \cdot \text{EM}) \\
&\text{PRP2} = \text{QUP} \cdot (\text{E1} \cdot \text{FP} + \text{G1} \cdot \text{PM}) \\
\text{C} &= \text{DJN2} = \text{QUN} \cdot (\text{E1} + \text{G1}) \\
&\text{DJP2} = \text{QUP} \cdot (\text{E1} - \text{G1}) \\
&\text{A12} = \text{TEO} \cdot (\text{C2} \cdot \text{DNE} + \text{C1} \cdot \text{DNE1}) \\
&\text{A21} = \text{TEO} \cdot (\text{C2} \cdot \text{DPE} + \text{C1} \cdot \text{DPE1}) \\
&\text{A11} = - \text{A12} - \text{TOX} \cdot (\text{DJN1} - \text{DJN2}) \\
&\text{A22} = - \text{A21} - \text{TOX} \cdot (\text{DJP2} - \text{DJP1}) \\
&\text{A11} = \text{BETA} \cdot \text{A11} \\
&\text{A12} = \text{BETA} \cdot \text{A12} \\
&\text{C} &= \text{A21} = \text{BETA} \cdot \text{A21} \\
&\text{A22} = \text{BETA} \cdot \text{A22} \\
&\text{DJN1} = \text{QUN} \cdot (\text{E1} - \text{G1}) \\
&\text{DJP1} = \text{QUP} \cdot (\text{E1} + \text{G1}) \\
&\text{IF} (\text{I} \cdot \text{EQ.} \ 1) \text{ GO TO 32} \\
&\text{AM} = \text{TP} \cdot (\text{AN1} + \text{QNI}) + \text{TN} \cdot (\text{AP1} + \text{QNI}) \\
&\text{REC} = (\text{AN1} \cdot \text{AP1} - \text{QNI} \cdot \text{QNI2}) / \text{AM} \\
&\text{PREK} = \text{QLX} \cdot \text{REC}
\end{align*}
\]
DJN = PRN2 - PRN1 - PREK
DJP = PRP2 - PRP1 + PREK
DNT = DJN*TQX
DPT = - DJP*TQX
DELTA = 1 -A11-A22 +A11*A22 -A12*A21
F11 = (1-A22)/DELTA
F12 = A12/DELTA
F21 = A21/DELTA
F22 = (1-A11)/DELTA
DELN = ALFA*(DNT*F11 + DPT*F12)
DELP = ALFA*(DNT*F21 + DPT*F22)

IF((ITE .LT. J1-2) .OR. (KEY(10) .NE. -10)) GO TO 987
WRITE(6,18) DNE,DNE1,DPE,DPE1,C1,C2,TE0,DNT,DPT
WRITE(6,18) A11,A12,A21,A22,F11,F12,F21,F22

987 CONTINUE
C
QZZ(I) = QZZ(I) + DELP - DELN
QON(I) = DELN

DOF(I) = DELP
IF(ITE .EQ. I) GO TO 33
QNN(I) = AN1 + DELN
QPP(I) = AP1 + DELP

33 CONTINUE
SLS = SLS + ABS(DJN) + ABS(DJP)

32 CONTINUE
AP1 = AP2
AN1 = AN2
IF(QNN(I) .LE.0) QNN(I) = 1.0
IF(QPP(I) .LE.0) QPP(I) = 1.0
IF(L1.NE.JT1) GO TO 110
QZZ(I) = QZZ(I) + DELP - DELN
PRR(I) = PREK
PRH0(I) = PRP1
PRE0(I) = PRN1

C
VFN(I) = -VT* LOG(QNN(I)/QNI) + VV(I)
VPP(I) = VT* LOG(QPP(I)/QNI) + VV(I)
VFN(I) = DNE
VPP(I) = DPE
EFN(I) = (LOG10(QNN(I)) - 14.0)
EFF(I) = (LOG10(QPP(I)) - 14.0)

110 CONTINUE
QPP(I) = ABS(2*QPP(2) - QPP(3))
QPP(II) = ABS(2*QPP(II-1) - QPP(II-2))
QNN(I) = ABS(2*QNN(2) - QNN(3))
QNN(II) = ABS(2*QNN(II-1) - QNN(II-2))

C
WRITE(6,18) SLS
WRITE(*,18) SLS
RETURN
18 FORMAT(''!,9E13.5)
17 FORMAT(''A,5E20.9)
19 FORMAT(''A,9E13.5)
10 FORMAT('' !)
END
APPENDIX B

Fabrication of Punch-through Space-charge Limited Loads

B.1 Mask Set Used for Fabrication
Level 1: Diffusion Opposite to N_{BC}; Lightly Doped
Level 2: Diffusion Same as $N_{BC}$; Moderately Doped
Level 3: Diffusion Opposite to $N_{BC}$: Heavily Doped
Level 4: Contact
Level 5: Metallization
B.2 Outline of Process Flow

1. Initial Clean
2. Initial Oxidation
3. Mask 3 Photolithography
4. Implant (opposite to $N_{BC}$)
   a) strips and clean
   b) pre-implant oxidation
      A. Phosphorus (p-type substrate)
      B. Boron (n-type substrate)
5. Post Implant Treatment
   a) Annealing
   b) Drive-in
6. Reoxidation
7. Mask 4 Photolithography
8. Metalization
9. Mask 5 Photolithography
10. Testing
Notes

1. All flowmeters settings on Brooks Instruments R-2-15-AAA, stainless steel float, unless indicated otherwise.

2. All D.I. water rinse same as 1.b) below

1. Initial Clean

Starting material: silicon wafers, 2" or quarters of 3", orientation [111], n- or p-type as required.

   a) Aceton           Ultrasonic   10min
   b) DI Water Rinse   5min         RT
   c) H₂SO₄ : H₂O₂     (3 : 1)      10min 900C
   d) Rinse
   e) H₂O : HF        (10 : 1)      20sec RT
   f) Rinse
   g) HNO₃            (conc)       10min 900C
   h) Rinse
   i) H₂O : HF        (10 : 1)      10sec RT
   j) Rinse
   k) Spin dry

2. Initial Oxidation

Field Oxidation Furnace, 11000C

   a) Dry O₂ : O₂byp= 60  10min
   b) Steam O₂ : O₂byp=60  O₂bub=40  90min
c) Dry O₂ : O₂byp=60 10min

d) Remove wafers, let cool 5min

e) Measure t_ox with color chart

3. Mask 3 Photolithography

Mask 3, KTI 820 positive resist or equivalent

a) Prebake 30min at 1350°C to eliminate any moisture

b) Spin on
   -HMDS : Xylene 50:50 4500 rpm 20sec
   -Photoresist 4500 rpm 20sec

c) Prebake, 90°C, 30min

d) Expose, GCA Direct Wafer Steper, Model 4800

e) Postbake, 1350°C 30min

f) Develop

   H₂O : 809 positive resist developer 42sec RT

g) Rinse

h) Inspect under Microscope

i) Postbake, 1350°C 30min

j) Etch in appropriate bath

   Here: Etch in Buffered HF (BHF) (10 : 1)

   Record etching time

k) Rinse

l) Spin dry

4. Implant (opposite to NBC)
Note: This process is listed for both n- and p-type substrates. This implant should be opposite to the background concentration.

a) Strips and Clean

\[
\begin{align*}
H_2SO_4 : H_2O_2 & \quad (10 : 1) & 100^\circ C & 10\text{min} \\
\text{DI Rinse} \\
H_2SO_4 : H_2O_2 & \quad (3 : 1) & 90^\circ C & 6\text{min} \\
\text{Rinse} \\
H_2O : HF & \quad (20 : 1) & \text{RT} & 10\text{sec} \\
\text{Rinse} \\
HNO_3 & \quad (\text{conc}) & 90^\circ C & 6\text{min} \\
\text{Rinse} \\
H_2O : HF & \quad (20 : 1) & \text{RT} & 10\text{sec} \\
\text{Rinse} \\
\text{Spin dry}
\end{align*}
\]

b) Pre-implant Oxidation

Field Oxidation Furnace, 1100^\circ C

1) Dry \text{O}_2 : \text{O}_2\text{byp}=60 \quad 6\text{min}

2) Remove wafers, let cool 5min

3) Measure \text{t}_{\text{ox}} with color chart, if possible.

c) Phosphorus Implant or Boron Implant

Extrion Ion Implanter

Energy : 80 Kev

Dose : $5 \times 10^{15}$ atoms/cm$^2$
Note: Include a monitor wafer for junction depth and sheet resistance measurements.

5. Post Implant Treatment
Note: wafers are cleaned after the implantation is performed.

A. Annealing

Field Oxidation Furnace, 900°C

Dry N₂ : N₂=60  

B. Drive-In

Field oxidation Furnace, 1100°C

1) Dry N₂ : N₂=60  
2) Remove wafers, let cool 5min
3) Remove oxide from the monitor wafer
4) Measure sheet resistance
5) Measure junction depth

6. Reoxidation

Field Oxidation Furnace at 950°C

a) Steam O₂ : O₂byp=60  
   O₂bub=40  
   25min

b) Remove wafers, let cool 5min

c) Measure t₀ₓ with color chart

7. Mask 4 Photolithography

Mask 4, KTI 747 or equivalent negative resist

a) If wafers were exposed to moisture, prebake 30 min at 1350°C
b) Spin on -HMDS : Xylene 50 :50 4000rpm 20sec
         -Photoresist 4000rpm 20sec
c) Prebake, 850C 30min
d) Expose
e) Develop -Projection Developer bath #1 15sec
         -Projection Developer spray 10sec
         -Projection Developer bath #2 15sec
         -Projection Developer spray 10sec
         -N-butyl acetate spray 20sec
         -blow dry
f) Inspect under Microscope
g) Postbake, 1350C 30min
h) Etch in appropriate bath
   Here : Etch in Buffered HF (BHF) (10 : 1)
   Record etching time
i) Rinse
j) Spin dry

8. Metalization
   a) Strip and Clean
      see procedure in step 4a)
   b) Deposit metal
      Al e-beam evaporation 5000 Angstrom

9. Metal Photolithography
   a) Mask 5, KTI 747 or equivalent
      see procedure in step 7.)
   b) Aluminum etch
c) Photoresist strip

Microstrip 712D or equivalent

Note: Important for wafers, boat and thermometer to be free from any moisture.

10. Testing
LIST OF REFERENCES


