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Analytical modeling of single-event burnout of power transistors

Johnson, Gregory Howard, Ph.D.

The University of Arizona, 1992

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ANALYTICAL MODELING OF SINGLE-EVENT BURNOUT OF POWER TRANSISTORS

by

Gregory Howard Johnson

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As members of the Final Examination Committee, we certify that we have read the dissertation prepared by Gregory Howard Johnson entitled Analytical Modeling of Single-Event Burnout of Power Transistors and recommend that it be accepted as fulfilling the dissertation requirement for the Degree of Doctor of Philosophy.

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DEDICATION

This work is dedicated to all of my dear family and friends who have given me the special support and encouragement necessary for such an achievement. This is especially so for Emily, who had to put up with me the most during my graduate studies.
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When electronic components are to be used in systems destined for operation in the extraterrestrial environment, one must be concerned about the effects of the naturally occurring radiation in outer space. For example, power metal-oxide-semiconductor-field-effect transistors (MOSFETs) and power bipolar junction transistors (BJTs) are susceptible to a phenomenon called single-event burnout (SEB) which may result from bombardment by heavy ions originating from the nuclear reactions within the sun and other stars. SEB is a catastrophic failure mechanism initiated by the passage of a heavy ion through sensitive regions of the power MOSFET or power BJT.

The main thrust of this dissertation is an analytical model describing the device-related aspects of the SEB mechanism. Physical device parameters such as doping concentrations, dimensions of various regions, and operating bias are related to SEB by the model. It is shown that the model predicts a decrease in the SEB susceptibility with a decrease in the internal base resistance (in the power BJT or parasitic BJT in the power MOSFET structure), a decrease in the operating bias, or an increase in the ambient device temperature. These findings are then qualitatively verified with experimental data.
CHAPTER 1

INTRODUCTION

Ever since electronic systems have been designed to operate in space, system designers have been required to take into account the effects of many types of radiation on electronic devices, circuits, and the entire electronic system. One such effect, single-event burnout (SEB), is a sudden catastrophic failure mechanism triggered by a single heavy ion that can occur when power metal-oxide semiconductor field-effect transistors (MOSFETs) and power bipolar junction transistors (BJTs) are operated in the space radiation environment. This dissertation addresses SEB from the point of view of a semiconductor device engineer. An analytical model will be presented that relates the physical parameters and operating conditions of the power transistor to its sensitivity to SEB in a heavy ion environment. The model is not intended to pin-point the exact energy required for burnout but, rather, is intended to identify the relevant device parameters that play a significant role in the SEB mechanism. Once the important device parameters are found, the model is used to show how these parameters can be varied in order to achieve a power transistor design that is more resistant to the SEB phenomenon.

This chapter illustrates how the phenomenon of SEB of power transistors fits into the realm of engineering and science by reviewing: the physical structure and typical applications of the power transistor; the space radiation environment; the heavy ion environment in particular; and a brief discussion of the SEB phenomenon. Subsequent chapters discuss: modeling various aspects of the SEB mechanism; using the model to calculate SEB thresholds; SEB experiments conducted to explain the trends predicted by the analytical model; and methods for designing power MOSFETs and power BJTs which are resistant to SEB in the space radiation environment.
1.1 Power Device Structure and Applications

1.1.1 Power Device Applications

The power MOSFET and power BJT are important devices in designing and building many electronic systems [1]. A primary use of the power transistor is in regulated switching applications. Power supplies and variable speed motor controllers (which are significant components in computer systems, spacecraft systems, etc...) are examples of regulated switching applications.

A simple example of a regulated power supply is shown in Figure 1.1, the well-known buck converter [2]. The power transistor switches at a given frequency, $f_s$, with a duty cycle, $D$. The output voltage, $V$, is given by:

$$V = D V_g.$$  

(1.1)

The output voltage, $V$, is then regulated through the duty cycle, $D$. The control circuitry required for this regulation has been omitted from Figure 1.1. The peak transistor current and

![Figure 1.1: Buck Converter – an example of switching power supply.](image-url)
voltage are given by:

\[ I_{DSMAX} \equiv \frac{V}{R} + \frac{(V_g - V) D}{2 L f_s}, \]

(1.2)

\[ V_{DSMAX} \equiv V_g. \]

(1.3)

A power transistor used in such an application must be able to withstand these maximum values of current and voltage. Power MOSFETs capable of blocking up to about 1000 volts and drawing up to about 100 amperes are available. Similarly, power BJTs capable of blocking up to about 1500 volts and drawing up to about 1000 amperes are available. The graph shown in Figure 1.2 illustrates the range of operation for competing technologies of MOSFETs, BJTs and semiconductor-controlled rectifiers (SCRs) [1].

![Graph showing On-state current and off-state voltage levels for power MOSFETs, BJTs, and SCRs.]

Figure 1.2: On-state current and off-state voltage levels for power MOSFETs, BJTs, and SCRs.
Unless it is necessary to utilize the high voltage and current levels attainable with the power BJT, the power MOSFET is the preferred device in most switching applications. From the point of view of a circuit designer, the gate-drive circuit design of a MOSFET switch is much simpler than either the base-drive circuit design of a BJT switch or the firing scheme of an SCR-based switch. The high input impedance of a MOSFET greatly simplifies the gate-drive circuitry. This is attributed to the negligible current drawn through the gate during the ON state. The only appreciable current is that necessary to charge and discharge the gate capacitance. The BJT, on the other hand, draws large amounts of base current in the ON state, which complicates the base-drive circuitry.

From a switching speed point of view, the power MOSFET is also superior to the BJT and the SCR. Since the MOSFET is a unipolar device, only one carrier type, there are no switching delays associated with recombination of minority carriers when turning off the device. The switching speeds of power MOSFETs are typically orders of magnitude higher than their counterparts [1]. This is especially important for high switching speed applications when switching losses dominate the overall power losses. It should be noted that higher switching frequencies generally reduce overall component size and weight in most switching regulator applications. Size and weight considerations are especially important for spacecraft.

The power MOSFET is not always superior to the power BJT. When high switching speed is not a concern, the power BJT may be the power transistor of choice. The on-state resistance of the power BJT is much lower than that of the power MOSFET at high voltage ratings. This point will be made more clear shortly, but essentially it is because in order for power transistors to block large voltages, rather thick epitaxial regions are required. A thicker slab of material generally equates to a larger resistance. The power BJT has a lower on-state resistance because of carrier modulation from the injected minority carriers, while the power
MOSFET has currents due to majority carriers only, $R_{DS(on)}$. Therefore, for high-voltage, low switching frequency applications the power BJT is the power transistor of choice, since the lower associated on-state resistance will result in lower overall power losses.

The state-of-the-art power MOSFET structure manufactured today is the double-diffused metal oxide semiconductor (DMOS) device. The structure and operation of the DMOS power transistor will be discussed in the next section. Following this discussion, the structure and operation of the power BJT will be given.

1.1.2 Power DMOS Structure and Operation

The cross-section of one cell in an n-channel DMOS power transistor is shown in Figure 1.3. This device is named for the manner in which it is processed. Both the source and the body are diffused using the gate as a mask edge. The channel length is then determined by the difference in diffusion rates of the dopants, rather than by photolithography limitations.

![Figure 1.3: Cross-section of power DMOS transistor structure.](image)
Relatively short channel lengths, on the order of 1μm, can be obtained in this fashion. At first glance, this device appears much different than a traditional lateral MOSFET. A typical lateral MOSFET cross section is shown in Figure 1.4 for comparison.

One apparent difference between the two devices is that the contact to the drain is made on the bottom surface of the DMOS device, rather than on the top surface as in the lateral MOSFET. A rather thick epitaxial drain region is required to drop the large drain to source voltages that the power transistor must block while operating in the OFF state. When contact is made to the drain through the bottom surface metallization and the n+ substrate, the electric field lines can extend through the entire thickness of the epitaxial layer to drop the applied voltage [3].

The bottom contact explains how the DMOS device can withstand high voltages, but what about the high currents? A power transistor must be able to draw large amounts of current while in the ON state. This is achieved by connecting thousands of the DMOS cells in parallel. A popular scheme is to pack the cells in a hexagonal pattern similar to a honeycomb, as shown in Figure 1.5. Note that the gate, metal, and oxide regions have been omitted from Figure 1.5. This parallel combination effectively creates a very wide channel
Figure 1.5: Three dimensional view of power DMOS structure using hexagonal cells and hexagonal cell packing. The gate, oxide, and drain and source metallizations have been omitted from this figure. The channel regions are inverted when the gate is ON, allowing carriers to move from the n+ sources to the n-drain region, while retaining the same channel length of the individual cell, enabling large current flow with the same applied gate to source voltage.

The positive temperature coefficient for the gate to source voltage of the MOSFET enables a stable parallel connection of the individual cells in the DMOS structure. Negative feedback prevents current hogging in the DMOS structure resulting in an approximately equal current distribution among the cells.

The DMOS device operates just as a lateral MOSFET does, except that the currents flow in different paths. Figure 1.6 will be used to illustrate the path that electrons flow in the DMOS device. Since this is an enhancement mode n-channel MOSFET, a positive voltage greater than or equal to the threshold voltage applied to the gate will invert the channel region
Figure 1.6: Flow of electrons in the power DMOS transistor.

Figure 1.7: Parasitic BJT present in the power DMOS transistor structure.
below the gate. This highly conductive path enables electrons to flow from the source through the channel and into the drain, thus turning the MOSFET on. All the cells in the device turn on simultaneously, and currents will flow as shown in Figure 1.6.

All real devices are not without their parasitic elements, and the DMOS structure is certainly no exception. Inherent to the DMOS structure is a parasitic npn bipolar transistor as shown in Figure 1.7. The source, body, and drain regions of the MOSFET comprise the emitter, base, and collector regions of the parasitic BJT. In normal operation of the power MOSFET, this parasitic BJT is always turned off. This is by virtue of the common source-body metallization which shorts out the base-emitter junction of the parasitic BJT. It will later be shown that this parasitic BJT plays a key role in the SEB mechanism.

1.1.2 Power BJT Structure and Operation

Similar to the power MOSFET, a power BJT must be capable of blocking a large voltage when it is turned off and conducting a large current when it is turned ON. The high voltage and high current capabilities of the power BJT result from the device structure shown in Figure 1.8. Note that the vertical structure of the power BJT is almost identical to the vertical structure of the parasitic BJT in the power DMOS transistor. As a brief aside, this is no coincidence. The power DMOS device evolved from the power BJT. The desirable features of the MOSFET gate were essentially ‘added’ to the power BJT structure.

The power BJT is similar in appearance to an integrated BJT with the exception that the collector is contacted on the back surface of the chip. This backside contact allows the designer to use a thick epitaxial layer. The thickness and doping density of this epitaxial layer dictate the voltage that the BJT can block when it is turned off. A thicker and more lightly doped epitaxial layer yields a higher blocking voltage than a thinner or more heavily doped
layer [4]. Note that this applies to the power DMOS device also.

For a BJT, a large emitter area is necessary in order to achieve high conduction currents for a given current density [5]. In a power BJT, the large emitter area is obtained by using several emitter stripes. This segmentation of the emitter reduces current crowding effects that reduce the collector current for a given base-emitter bias [6]. Although the device shown in Figure 1.8 has two emitter stripes, an actual device may have many more. In the power BJT, each emitter stripe is contacted by one common emitter metallization, and the base region is contacted between each emitter stripe by one common base metallization. For clarity, the base and emitter contact metallizations have not been shown in Figure 1.8.
1.2 Operation in the Space Radiation Environment

It is well known that the natural space environment is very different from the terrestrial environment. The major differences concerning the normal operation of electronics in space are the temperature extremes and the naturally occurring radiation. The ambient temperature of the electronics can be controlled with sophisticated heating and cooling units. The radiation must be compensated for by designing the devices and circuits to be resistant to radiation, or radiation hardened (rad hard).

The radiation present in space creates a very hostile environment for semiconductor devices like the power MOSFET and power BJT. Radiation effects can be grouped into four categories: total-ionizing-dose effects, ionizing-dose-rate effects, neutron or displacement damage, and single-event phenomena [7]. Total-dose effects and single-event phenomena occur in a natural space-radiation environment, while dose-rate effects and neutron damage do not [8].

Radiation damage from total-dose or dose-rate effects can result in significant buildup of positive trapped charge and buildup of interface states in any oxide regions (e.g., gate oxides, field oxides, etc...). This charge and interface state buildup can change key electrical properties of an MOS device, such as threshold voltage shifts [9], mobility degradation [10], and loss of current drive [11]. Positive trapped charge within oxides along the periphery of a power MOSFET can lead to breakdown voltage degradation [12, 13]. Charge and interface state buildup can also change properties of a modern BJT such as gain degradation due to an increase in base current [14]. Device performance degradation can be correlated to the total radiation dose, and/or it can be correlated to the rate of the radiation dose.

Radiation damage from neutron exposure can result in crystal dislocations which will alter charge transport properties of the device by introducing energy states within the
forbidden band gap. Typically the resistivity will increase and the minority carrier lifetime will decrease in a radiated area [15]. This can affect bulk regions and the gain of BJTs.

Radiation damage from single-event phenomena, bombardment by single protons or heavy ions, can result in single and multiple bit errors in memory elements and various logic circuitry [16]. In the case of power MOSFETs and power BJTs, single-event phenomena can result in an abrupt and catastrophic thermal destruction of the device. The latter phenomenon, known as single-event burnout, was first reported by Waskiewicz [17]. Following single-event burnout, the power transistor typically develops a short circuit between the power terminals (drain-source or collector-emitter). This, of course, renders the device useless for switching or amplification applications.

The consequences of any of the above forms of radiation damage are very undesirable, since they may render a prime component of a satellite useless. Thus, research in process variations, circuit layouts, and device geometries is under way to produce radiation hardened, or rad-hard, electronics (i.e., electronic equipment less prone to or immune to radiation damage).

1.3 Heavy Ion Environment

Heavy ions (sometimes called cosmic rays) are ubiquitous in the natural space radiation environment [16]. If electronic systems are to be operated in such an environment, it is desirable to know the basic effects that heavy ions have on electronics and the relative abundance of these heavy ions in space. In this section, the fundamental effect from heavy ions and their relative abundance in the space radiation environment is presented.

When an energetic heavy ion passes through an electronic component, it loses energy along its track. One may naively think that energy is primarily lost through collisions with
the target material. Since the heavy ion is positively charged (the outer shell of electrons is stripped off), most of the energy loss is due to electron-hole pair creation. As the heavy ion passes through, a plasma of electron-hole pairs is created (or deposited) along its track length. More details about this column of charge will be presented in a later chapter.

The amount of charge deposited is determined by a quantity called the stopping power of the heavy ion. The stopping power for a given particle is a function of the atomic number, mass, and the entrant energy. Stopping power has units of [energy/distance]. Sometimes the energy deposition is expressed with units of [(energy/distance)/(mass/volume)], where the mass density given refers to the target material. When the energy deposition is given in this manner, it is called the linear energy transfer (LET). Typical units for the above two quantities are [MeV/µm] for the stopping power and [MeV cm²/mg] for the LET. Figure 1.9 shows the approximate dependence of stopping power on energy for the range of ion masses found in the space environment. The lightest ion is of course hydrogen, and the heaviest one shown is iron. It will later be shown that ions heavier than iron are very unlikely

![Figure 1.9: Linear Energy Transfer versus nucleon energy for hydrogen, helium, oxygen, and iron.](image-url)
to be encountered in space. Notice that for a given energy, the stopping power is higher for the more massive ion. Also note that the stopping power varies over four orders of magnitude for the energies and ion species shown.

The information shown in Figures 1.10 [20] and 1.11 [19] gives the relative abundance of elements in the galactic cosmic-ray spectrum. Figure 1.10 shows relative abundance in terms of energy per nucleon, and Figure 1.11 shows relative abundance in terms of atomic number. The actual values of particle fluxes constantly change with time. These figures only give a rough idea of the relative abundance of heavy ions, since the relative abundance changes dynamically. Solar flares are mostly responsible for the changing particle fluxes [21].

Sometimes the environmental data are presented in another way. Figure 1.12 shows the

![Figure 1.10: Particle abundance versus nucleon energy.](image-url)
Figure 1.11: Relative intensity versus atomic number.

total integral flux of particles versus LET encountered in three geosynchronous orbital environments [22]. The y-axis represents the number of particles present per day with LET values above the corresponding x-axis value. Typically, the environments shown are those that are exceeded 0.03%, 10%, and 100% of the time in space. Recall that the environment dynamically changes. The curve labelled 10% is also referred to as the "Adam’s 90% worse-case environment", because this environment is worse than that encountered 90% of the time.

These environment curves are frequently used to predict SEB rates of various components or circuits while operating in the space environment. The SEB hardness of the
power transistor can be characterized by two parameters which may be found experimentally. The first is the critical LET, which is the minimum LET of an incident ion required to initiate SEB. The second is the SEB cross-section, which is a measure of the sensitive surface area of the device that is susceptible to SEB. The determination of these parameters will be discussed in the next chapter. These two parameters can be used together with Figure 1.12 to estimate a SEB rate. For example, using the Adam's 90% worst-case environment, a device will encounter approximately 0.1 particles per cm² - day with an LET of 30 MeV cm²/mg or greater (Note the horizontal axis of Figure 1.12 has units of MeV cm²/g). If the critical LET of the device was 30 MeV cm²/mg, that means that one could expect to see 1 particle striking a 1 cm² region of the device capable of initiating burnout in 10 days. Now if the SEB cross-section, or sensitive area, of the device was 0.1 cm², then one would expect to see 0.01
particles per day that strike a sensitive region and have an LET sufficient to initiate burnout. This translates to one burnout in about 100 days. This particular device would certainly not be suitable to operate in a space application, which may require years of reliable operation.

1.4 Prior Work

In a work of this nature it is very important to establish the originality of the work and the contribution of the author. The contributions of the author have evolved from the work given in reference [23]. At that time, the model was in more of a conceptual stage, and very few computations could be made (none on realistic device structures). The author began to contribute at the time of reference [24]. At this stage, the algorithm for computing the avalanche generated hole current was in development.

For the work in this dissertation, the author developed, implemented, and automated the majority of the numerical techniques used in obtaining solutions in the model. This enabled the author to use the model on realistic device structures, and ultimately to determine the sensitive device regions in the SEB mechanism. The author applied the model to the power bipolar junction transistor device structure, which helped significantly to verify some of the key device parameters responsible for SEB. A detailed model for the role of high-level effects in the SEB process was developed. This model has important consequences for predicting SEB occurrence. The author implemented temperature dependence of the SEB mechanism in the model. Finally, the author has obtained and analyzed experimental data, and used these data to support the predictions made by the analytical model. Throughout the text, a point will be made as to which portions are contributions made by the author and were developed previously.
1.5 Summary

In this introductory chapter, an attempt has been made to show the relevance of the single-event burnout phenomenon. Applications for a switch that can withstand large voltages when turned off and conduct large currents when turned on were presented to show the utility of power transistors in electronic circuitry. The important trade-offs between using the power MOSFET or the power BJT were discussed to point out their differences and similarities. The physical structures and operation of the power MOSFET and power BJT were presented to help set the stage for the analytical model to follow. The hostile space radiation environment where power transistors are frequently required to operate was briefly discussed. Finally, the heavy ion environment, which is one particular form of radiation encountered in space, was described to illustrate how environmental information can be used to predict single-event burnout rates.

In Chapter 2, the SEB mechanism is described and the analytical model is developed. In Chapter 3, the portion of the analytical model that calculates the effects of avalanche generated currents internal to the power transistor is given. In Chapter 4, the analytical model is assembled and sample SEB threshold calculations are performed. In Chapter 5, techniques and results from some SEB experiments performed for comparison to the model are presented. Comparison of the experimental data to the analytical model is presented in Chapter 6. Finally, a summary, conclusions, and areas for future investigation are presented in Chapter 7.
CHAPTER 2

SINGLE-EVENT BURNOUT MECHANISM

2.1 Brief Overview of Burnout Mechanism

Single-event burnout has been attributed to the parasitic BJT of the DMOS structure [23] and the vertical BJT in the power BJT structure [25]. In this discussion of the SEB mechanism, attention will be focussed on the power MOSFET. Since the vertical structure of the power BJT is nearly identical to the vertical structure of the power MOSFET, the same basic SEB mechanism is present.

If the parasitic BJT is turned ON when the MOSFET is turned OFF, second breakdown of the BJT, and hence thermal melt-down, may occur. Second breakdown occurs when thermal runaway sets in due to the simultaneous high current and high voltage present in the parasitic BJT [26]. The mechanism leading to SEB will now be briefly discussed. Figure 2.1 shows the DMOS structure with a heavy ion passing through the parasitic BJT. As the heavy ion traverses the device, electron-hole pairs are generated along its track length creating an ionized plasma filament. This plasma filament supports a short-lived current source in which holes flow up towards ground via the lateral base region, and electrons flow down towards the collector. The short-lived current source initially drives the parasitic BJT locally turning on one cell of the DMOS structure [27].

Depending on how "hard" the BJT is initially turned ON, the currents within the device will either regeneratively increase until burnout occurs, or the currents will die out leaving the device unharmed. A feedback mechanism inherent to the vertical structure of the parasitic BJT will determine whether the currents will increase or decrease. The feedback mechanism consists of four basic components. These components in terms of the parasitic BJT are: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-
Figure 2.1: Power DMOS cross-section with heavy ion strike illustrating the electron-hole pair generation along the ion track length.

generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from this lateral base current. The details of each part in the SEB mechanism will be discussed in the sections to follow.

2.2 Turning on the Parasitic Bipolar Junction Transistor

The parasitic BJT is turned on by a localized current source generated by the passage of the heavy ion. It is hypothesized that the parasitic BJT is turned on as shown in Figures 2.2 and 2.3. Figure 2.2 shows the heavy ion track along a vertical cross section and from the surface of a DMOS cell. Due to the applied bias, holes will flow up towards ground and electrons will flow down towards the drain. The holes flowing towards ground must pass
Figure 2.2: (a) Vertical cross-section of DMOS cell illustrating heavy ion strike and the direction of flow of electrons and holes. Note the flow of holes through the lateral base region on the way to ground in the parasitic BJT. (b) View of ion strike from the surface showing the direction of hole current flow under the n* source region.

Through the base region of the parasitic BJT (for ions that strike outside of the body contact region of the DMOS cell). This hole current through the base region forward biases the base-emitter junction and locally turns-on the parasitic BJT. Figure 2.3 illustrates the turn-on of the parasitic BJT from a top view of the DMOS cell. Figure 2.3a shows the parasitic BJT turned-on locally in the vicinity of the ion strike. As time progresses, more of the cell will turn-on. The cell turn-on can be understood in the following manner. The majority of the hole current flows in the direction shown in Figure 2.2b. This means the voltage drop normal
Figure 2.3: Illustration of the currents spreading within one cell of the DMOS structure as time progresses. The shaded regions indicate regions of the parasitic BJT that are turned on, and the arrows illustrate the hole current flowing beneath the n+ source (emitter) region. Part (a) indicates the region of the parasitic BJT activated shortly after the parasitic BJT turns on, and time progresses in parts (b-d) with (d) occurring if and when the entire cell turns on.

to the direction of current shown in Figure 2.2b will be very small in locations near those turned ON in the parasitic BJT. Thus, regions near those already turned ON will turn ON, quickly developing an equipotential line around the cell perimeter. This is shown in parts (b-d) of Figure 2.3. The final state of the parasitic BJT turn ON is shown in Figure 2.3d, where the entire cell is ON. In the discussions to follow, the state shown in Figure 2.3d will be assumed.
This is certainly a time dependent process. In this model, however, the time dependence of the turn-on of the parasitic BJT will not be considered. A detailed study of the turn-on of the parasitic BJT certainly warrants investigation. Some ideas about future work in this area will be discussed in Chapter 7. For the discussions of this dissertation, it will be assumed that any heavy ion capable of generating enough current to trigger the regenerative feedback mechanism will be capable of turning on the parasitic BJT. This assumption is valid if the heavy-ion-generated current filament exists long enough to turn the transistor on. Once the parasitic BJT is turned on, the current filament is of no further concern in the SEB mechanism. If the current filament were extinguished at or before the turn-on time of the parasitic BJT, the dynamic aspects of this part of the mechanism would be quite important. However, this work focuses on the details of the bipolar-transistor physics. A simple estimate of the lifetime of the current filament will be discussed shortly. A more detailed examination of the time constants could be performed using a device simulator like PISCES or PADRE. This is an important topic in itself and merits additional work. This work develops simple analytic models of the SEB mechanism that can be implemented with modest computer power.

Attention will now be directed towards simple estimates of the lifetime of the current filament. One can view the lifetime of the current filament in two ways. First, the radial diffusion of the filament can be viewed as the limiting factor. Here, the motion of holes towards ground and electrons towards the positive supply will continue until the filament diffuses radially, and the concentration of carriers within the filament is less than the background concentration of the collector region. This analysis is performed in Appendix A. It turns out that assuming only radial diffusion of the carriers, the filament will exist for about 20 ns.

The radial diffusion of carriers within the current filament was discussed in [23]. For this dissertation, this discussion was extended as follows. If one makes simple estimates on
the axial motion of carriers, the lifetime of the filament is not so large. In these estimates, a transit time approximation will be used. Using this approach, the filament will exist at least long enough for holes at the epi-substrate interface to reach the ground contact. A conservative estimate of the minimum distance travelled by the holes is the sum of the thickness of the epitaxial region and the length of the source region (see Figure 2.2a, which illustrates such a path). The fastest that such a hole can travel is the saturation velocity for holes in silicon, $v_{sat}$, which is approximately $6 \times 10^6$ cm/sec [28]. This leads to an equation for the minimum lifetime of the filament given by the transit time approach, $\tau_{fil(lo)}$:

$$\tau_{fil(lo)} = \frac{w + l_s}{v_{sat}}$$

(2.6)

where $l_s$ is the length of the source region. Using $w = 22 \mu m$ and $l_s = 10 \mu m$ (as in the previous example) results in a $\tau_{fil(lo)} = 533$ ps. Note that the breakdown voltage plays a role in the filament lifetime because of the dependence on the epitaxial layer thickness, $w$ (Recall in Chapter 1, that as the breakdown voltage is increased, the epitaxial layer thickness does too).

One can obtain an upper bound estimate for the transit time, $\tau_{fil(\text{hi})}$, by assuming that the high carrier density of the current filament causes the electric field to collapse across the region of transit. The electric field will collapse locally in the region of the current filament. The effect may be approximated by allowing the drain-source voltage to drop evenly across the DMOS structure. Now the voltage is dropped across both the heavily doped substrate layer and the high density current filament. Four-inch wafers typically have a substrate thickness, $w_{sub}$, of 20 mils or 508 $\mu$m. This thickness can then be used to approximate the electric field throughout that region by dividing the drain-source voltage by the sum of $w_{sub}$ and $w$. For the case of the 300 V breakdown structure biased at 290 V this amounts to $(290 \text{ V}) / (508 \mu m + 22 \mu m)$ or 5500 V/cm. The hole velocity corresponding to this level of
electric field is about a third of the saturating velocity or $2 \times 10^6$ cm/sec. This effectively triples the estimate for $\tau_{fil(lo)}$ given by equation 2.6 to get $\tau_{fil(hi)} = 1600$ ps. The interval of values for $\tau_{fil(lo)}$ and $\tau_{fil(hi)}$ for breakdown voltages ranging from 100 V to 500 V are shown in Figure 3.4. For each calculation, the bias level was equal to 96% of the breakdown voltage. It should be noted that the actual time the filament exists is determined by a complex combination of radial and axial transport, plus recombination of the carriers. From this point forward, it will be assumed that any current filament with sufficient strength (to be later defined) will exist long enough to turn on the parasitic BJT. In the sections to follow, the heart of the model of the SEB mechanism will be presented. This discussion will begin with the next section which covers the feedback mechanism.

![Figure 2.4: Relationship of bounded estimates of the current filament lifetime, $\tau_{fil(lo)}$ and $\tau_{fil(hi)}$ to the breakdown voltage of DMOS device.](image-url)
2.3 Feedback Mechanism Inherent to Device Structure

Depending on how hard the parasitic BJT is initially turned on, currents within the device will either: (1) regeneratively increase until the simultaneous high current and high voltage in the device trigger second breakdown and consequently thermal melt-down; or (2) the currents will die out to zero leaving the device unharmed. A feedback mechanism inherent to the device structure dictates whether the currents will regeneratively increase or decrease.

The feedback mechanism relates: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from this lateral base current [24]. The equations governing the feedback mechanism will now be discussed.

The coordinate system for this discussion is shown in Figure 2.5. The origin in $y$ is

![Figure 2.5: Coordinate system used in describing the feedback mechanism inherent to the vertical structure of the parasitic BJT.](image)
defined at the point of the ion strike, which is assumed to be at the drain edge of the MOSFET channel. The regions labelled E, B, and C are the emitter, base, and collector of the parasitic BJT. The length of the source region in the y direction is defined as $y_s$, and the p body – p$^+$ plug interface is defined as $y_p$. The extent of the p$^+$ plug under the n$^+$ source region, $y_e$, is defined as the difference between $y_s$ and $y_p$. In the previous work [23,24], the base region was not divided into two regions of different conductivity. For this dissertation, the feedback model was extended to include both the p$^+$ plug and p body in the base region of the parasitic BJT. It will be shown in Chapter 4 that the extent of the p$^+$ plug is one of the most significant factors affecting the burnout threshold.

The use of a rectangular coordinate system for this calculation simplifies the development of an analytical model and can be justified qualitatively. A rectangular coordinate system neglects the spreading resistance and the cylindrical nature of the current filament. The model is concerned with the turn-on of one cell of the parasitic BJT beyond the critical static condition for the regenerative mechanism to take place resulting in burnout. The rectangular coordinate system describes the system reasonably well along one ‘slice’ of the parasitic BJT ($c_{fg}$, Figure 2.2a). The 2-D nature of the base resistance is not accounted for, but the overall dependence of the critical condition on device parameter variation will be the same. Absolute changes in the critical condition will be different than those predicted by the use of cylindrical coordinates, but relative changes and the order of magnitude of the changes will be the same. As far as the shape of the cell perimeter is concerned (3-D nature of problem), much of the cell perimeter in the DMOS structure is a straight edge. This statement only breaks down near the corners of the hexagons ($c_{fg}$, Figures 2.2 or 2.3). Furthermore, it will be shown shortly that the parasitic BJT is turned-on in regions near the cell edge. Since very little of the device action is taking place far into the interior of the cell, and most of the perimeter of the cell is a straight edge, the rectangular coordinates will suffice.
Now, assuming a potential, $V_{BE}(y)$, exists that is large enough to locally turn on the parasitic BJT, the electron current density injected by the emitter, $j_{EC}(y)$, can be expressed to first order by [5]:

$$j_{EC}(y) = \frac{q D_n n_i^2}{N_{AB} w_B} \exp \left[ \frac{V_{BE}(y)}{kT/q} \right].$$  \hspace{1cm} (2.1)

Note that this current density is not shown in Figure 2.5 to avoid confusion. Also note that the uniformly doped narrow base assumption has been used again.

Since the base-collector junction has a large reverse bias applied across it, the electric field will be large throughout much of the collector region. Therefore, for each electron injected across the base into the collector, there will be avalanche-generated holes returning to the base region. The avalanche-generated hole current density, $j_{HC}(y)$, is given by [24]:

$$j_{HC}(y) = M q v_{sat} \left\{ \frac{D_n n_i^2}{q v_{sat} N_{AB} w_B} \exp \left[ \frac{V_{BE}(y)}{kT/q} \right] \right\}. \hspace{1cm} (2.2)$$

The multiplication factor, $M$, in equation (2.2) is defined as the ratio of the hole density to the electron density at the base side of the base-collector space charge region. $M$ is a function of the electric field, ionization rate, and the injected electron density, and is obtained numerically [24]. The multiplication factor, $M$, will be discussed in the next chapter. The term within the curly brackets in equation (2.2) is the electron density at the base edge of the base-collector space charge region, including the Kirk effect [29]. The Kirk effect assumes that the carriers are traveling at saturation velocity when they enter the base-collector space charge region. Thus, electron density at the base edge of the depletion region (term within curly brackets of equation (2.2)) is simply equation (2.1) divided by $q v_{sat}$. 
Due to the forward bias, \( V_{BE}(y) \), there also exists a back-injected hole current density, \( j_{HE}(y) \). This current density is expressed to first order by [5]:

\[
    i_{HE}(y) = \frac{q D_n n_i^2}{N_{DE} L_p} \exp \left[ \frac{V_{BE}(y)}{kT/q} \right].
\]  

(2.3)

Note that equation (2.3) assumes that the emitter thickness is much larger than the diffusion length for holes in the emitter, \( L_p \).

Portions of the feedback mechanism are discussed in [24]. For this dissertation, the relationship for the back-injected hole current density was extended as follows. Taking into account high-level injection effects of the base-emitter junction, equation (2.3) can be replaced by [30]:

\[
    i_{he} = \frac{q D_p n_i^2}{N_{DE} L_p} \left[ 1 + \left( \frac{n_i}{N_{AB}} \right)^2 \exp \left( \frac{V_{BE}}{V_T} \right) \exp \left( \frac{V_{BE}}{V_T} \right) \right].
\]  

(2.4)

Equation (2.4) was obtained by assuming high-level injection conditions exist (increase in minority carrier concentration at base edge of base-emitter junction is of same order as majority carrier concentration). This involves solving for the Fletcher boundary conditions for an n+p junction [30]. Equation (2.4) is similar to equation (2.3), except the back-injected holes have an additional exponential dependence on the base-emitter voltage. This results in an increase in the back-injected hole current during high-level injection. Equation (2.4) is important because without it a critical condition for burnout could be obtained for any parasitic BJT structure. Note that if the back-injected hole current is greater than that supplied by the avalanching mechanism, the parasitic BJT can not generate enough base current to stay turned \( ON \). Thus, the inclusion of equation (2.4) allows for the possibility that a device may be immune to SEB (if the critical condition is pushed so high that high-level injection
Figure 2.6: Four basic components of the feedback mechanism: (a) electron injection; (b) avalanche generated hole current; (c) base current; and (d) the ohmic base-emitter voltage.

There is one remaining current in the feedback mechanism to be described. This is the incremental hole current density which flows laterally through the neutral base region to the ground contact and develops the Ohmic drop necessary to keep the base-emitter junction forward biased. The value of this incremental current density, $j_{HB}(y)$, at any point $y$ is simply the difference between the avalanche-generated hole current density and the back-injected hole current density, which is:

$$j_{HB}(y) = j_{HC}(y) - j_{HE}(y).$$  \hspace{1cm} (2.5)
Note that this current density has units of \([\text{current/square area}]\).

A second order differential equation can be formulated that relates the Ohmic drop to the current density in the neutral base region [24]. First, the incremental lateral base current is just the local incremental base current density:

$$\frac{d}{dy} i_B(y) = j_{HB}(y). \quad (2.6)$$

Note that \(i_B\) has units of \([\text{current/length}]\) and is interpreted as current per gate width. Second, the incremental voltage drop is given by:

$$\frac{d}{dy} V_{BE}(y) = -R_B(y) i_B(y). \quad (2.7)$$

Equations (2.6) and (2.7) constitute a coupled system of first order differential equations. The boundary conditions for this problem are: (1) \(V_{BE}(y_s) = 0\) (this is a ground point and the potential must be zero); and (2) \(i_B(0) = 0\) (this is the integrated hole current density which must be zero at the starting point).

In summary, the components of the feedback mechanism are: (1) electron injection from the emitter to the collector; (2) avalanche generated hole current from the collector into the base region; (3) base current from holes returning to ground through the neutral base region; and (4) base-emitter voltage developed from base current. These components are summarized in Figure 2.6.
2.4 Burnout or Dieout

Equations (2.1) - (2.7) can be solved to obtain a critical condition necessary to initiate burnout [24]. This calculation will be illustrated for a specific device structure. Note that this calculation will involve numerically obtained values of the avalanche multiplication factor, \( M \). This set of equations is solved using a version of the numerical scheme called shooting [31]. The boundary conditions used are: (1) \( V_{BE}(y_s) = 0 \) (this is a ground point and the potential must be zero); and (2) \( i_B(0) = 0 \) (this is the integrated hole current density which must be zero at the starting point). The \( y \)-axis is discretized into 200 intervals. A value for \( V_{BE}(0) \) is initially guessed to be 500 mV. The local hole current density is then found with equation (2.5) through the use of equations (2.1) - (2.4). The hole current density is then integrated using trapezoidal integration to obtain \( i_B \) in equation (2.6). The local voltage drop is then given by equation (2.7). This voltage drop is subtracted from the value at the previous interval. This process continues over all of the intervals until a value of \( V_{BE}(y_s) \) is obtained.

If \( V_{BE}(y_s) = 0 \), the calculation is complete. If \( V_{BE}(y_s) < 0 \), \( V_{BE}(0) \) must be increased by some amount. If \( V_{BE}(y_s) > 0 \), \( V_{BE}(0) \) must be decreased by some amount. \( V_{BE}(0) \) is repeatedly increased or decreased until the boundary condition, \( V_{BE}(y_s) = 0 \), is met (with precision of 0.01 mV). The method of choosing the correct \( V_{BE}(0) \) is automated through a bisection-type algorithm. Once some upper and lower bound is determined for \( V_{BE}(0) \), the interval is repeatedly bisected until the boundary condition is met. In prior work [24], the iteration process was performed manually. At that time it was simply necessary to show solutions to the critical condition; however, for more complete calculations it was necessary to automate this process. That was done for this dissertation. The code used for calculating the critical condition is included in Appendix B.

The critical condition will now be calculated for a typical DMOS structure. The following parameters are used in the calculations: source doping density = \( 2 \times 10^{20} \) cm\(^{-3} \), p-
body doping density = 2 \times 10^{16} \text{ cm}^{-3}, \text{p}^+ \text{ plug doping density} = 2 \times 10^{18} \text{ cm}^{-3}, \text{drain doping density} = 1.1 \times 10^{15} \text{ cm}^{-3}, \text{source diffusion depth} = 1 \mu\text{m}, \text{p body diffusion depth} = 2 \mu\text{m}, \text{p}^+ \text{ plug diffusion depth} = 4 \mu\text{m}, \text{and epitaxial layer thickness} = 22 \mu\text{m}. The device has a nominal breakdown voltage of 300 V. The average doping densities needed in this abrupt junction calculation were obtained from Gaussian-type doping profiles.

The solution to equations (2.1) - (2.7) is shown in Figures 2.7-2.9. The collector bias for this case is 250V. Shown in Figure 2.7 is the incremental hole current density profile in the base region. Note that most of the hole current density occurs far from the ground edge. This is because of the exponential dependence on the base-emitter voltage, which decreases in a linear fashion. The second small hump present in Figure 2.7 is due to the ‘s-shaped’ behavior in the avalanche multiplication factor that will be explained in the next section (the avalanche multiplication factor increases for a decrease in injected electrons on a certain region of the curve). The base current per gate width is shown in Figure 2.8. Since this plot is an integral of that given in Figure 2.7, the initial sharp increase is seen near \( y = 0 \) along with the corresponding saturation. Figures 2.7 and 2.8 are purposely shown on the full scale of the source or emitter length, even though most of the information apparently is contained near \( y = 0 \). A major point to be made is the fact that the parasitic BJT is turned-on only along the cell perimeter. The base-emitter voltage is shown in Figure 2.7. Note the linear drop in voltage over most of the region. This is to be expected with a base current density that is constant over most of the region. Also note the dramatic change in slope occurring at \( y = 5 \mu\text{m} \). This is because the \( \text{p}^+ \text{ plug} \) extends to this point in the device under consideration. The highly conductive \( \text{p}^+ \text{ plug} \) has a very gradual slope in base-emitter voltage, while the \( \text{p body region} \) has a much steeper slope in base-emitter voltage.

These curves represent the critical condition for burnout because any heavy-ion generated perturbation in the system larger than that given in Figures 2.7-2.9 results in
Figure 2.7: Hole current density distribution at the threshold for burnout.

Figure 2.8: Base current density distribution at threshold for burnout.
regeneratively increasing currents within the device, and thus burnout occurs [24]. If the heavy-ion generated perturbation is less than that given in Figures 2.7-2.9, the currents will decay to zero; and burnout does not occur. This point is illustrated in Figure 2.10. In Figure 2.10 the critical condition for some particular device is indicated with dashed lines. Suppose a larger base-emitter voltage is generated at $y=0$, as shown in bold face in Figure 2.10c. If one proceeds to find the corresponding hole current density in the base for this bias level, it will be higher than that given by the critical condition as shown in Figure 2.10a. If the calculations are carried out for the three profiles in Figure 2.10, the base emitter voltage at the ground point would be less than zero. This condition is impossible due to the boundary conditions. The system would be forced to have the base-emitter voltage equal to zero at the ground point. This would have the effect of 'raising' the base-emitter voltage profile as
Figure 2.10: Illustration that critical solution is stable stationary solution to differential equation. The critical solution is shown in dashed lines in each case. The dark lines correspond to a solution whose currents and voltages exceed that of the critical solution. Note in (c) that the boundary condition that $V_{BE} = 0$ at the ground point is less than zero. Forcing this boundary condition (raising curve to that in thin solid line) shows how the system forces an even higher value for $V_{BE}(0)$.

shown in Figure 2.10c. Thus, the system would force the voltage at $y=0$ to increase further, as shown in Figure 2.10c. This illustrates why the critical condition is the stationary stable solution to the differential equation. Note that if a voltage less than the critical condition were developed at $y=0$, then a similar process would take place. The voltages and currents would decrease to zero, rather than regeneratively increase.
CHAPTER 3

AVALANCHE GENERATED HOLES

3.1 Low Current Avalanche Multiplication

The subject of low current avalanche multiplication will be defined to be the treatment of avalanching conditions without consideration of the space charge associated with mobile carriers. This section will discuss the development of the ionization integral which is commonly used to determine the breakdown voltage of a junction. The breakdown voltage is the maximum reverse bias that a junction can withstand with negligible current flow [32].

Avalanche multiplication is the most important mechanism in junction breakdown for lightly doped samples [33]. Carrier generation through the avalanching process is similar in some respects to avalanching of snow down a mountain ledge, which explains the nomenclature. Avalanche multiplication is pictured schematically in Figure 3.1. Figure 3.1 depicts the depletion region of a reverse biased junction. If electrons are injected into the space charge region from the left side, they will be swept to the right edge via the electric field

\[ E \]

Figure 3.1: Concept of avalanche multiplication. As electrons flow to the right under the influence of the electric field, electron-hole pairs are created by impact ionization. The generated holes are not shown.
present. If the electric field is sufficiently high, the electrons may generate electron hole pairs by impact ionization. The generated electrons and holes may proceed to create more electron hole pairs. This explains the increasing electron density gradient from left to right in Figure 3.1. The generated holes are not shown in Figure 3.1 for clarity.

The ionization integral, which determines the breakdown voltage of a p-n junction, will now be developed. The injected electrons, as shown in Figure 3.1, constitute a current \( I_n \). The magnitude of this current increases from left to right in Figure 3.1. Similarly, the generated holes also constitute a current \( I_p \), which increases from right to left in Figure 3.1. The total current at any point in the space charge region must be constant, and it is given by:

\[
I = I_n + I_p. \tag{3.1}
\]

Now, the incremental change in electron density at any point, \( x \), in the space charge region per second equals the number of electron hole pairs generated in the distance \( dx \) per second. An expression which describes this is [33]:

\[
d(n \nu_n) = n \nu_n \alpha_n dx + p \nu_p \alpha_p dx, \tag{3.2}
\]

where \( \nu_n \) and \( \nu_p \) are the velocity of electrons and the velocity of holes, respectively. The parameter \( \alpha_n \) in equation (3.2) is the ionization rate for electrons and is defined to be the number of electron hole pairs generated by an electron per unit distance travelled. Similarly, \( \alpha_p \) is the analogous term for holes. Both \( \alpha_n \) and \( \alpha_p \) are very sensitive to the local electric field. The higher the electric field, the higher the ionization rates. The first term in equation (3.2) represents impact ionization due to electrons and the second term represents impact ionization due to holes. One constraint when solving equation (3.2) is given by equation
(3.1). The other boundary condition is:

\[ I = I_{n}(x_{n}) = M_{n}I_{n}(x_{p}), \quad (3.3) \]

where

\[ M_{n} \equiv \frac{I_{n}(x_{n})}{I_{n}(x_{p})}. \quad (3.4) \]

When equation (3.2) is solved with the constraints given by equations (3.1) and (3.3), one obtains [33]:

\[ 1 - \frac{1}{M_{n}} = \int_{x_{p}}^{x_{n}} \alpha_{n} \exp \left[ - \int_{x_{p}}^{x} (\alpha_{n} - \alpha_{p}) \, dx' \right] \, dx. \quad (3.5) \]

The avalanche breakdown voltage is defined to be the voltage which makes \( M_{n} \) approach infinity (recall the strong electric field dependence on the ionization rates). The ionization integral:

\[ \int_{x_{p}}^{x_{n}} \alpha_{n} \exp \left[ - \int_{x_{p}}^{x} (\alpha_{n} - \alpha_{p}) \, dx' \right] \, dx = 1 \quad (3.6) \]

results when \( M_{n} \) approaches infinity. When equation (3.6) is solved incorporating the electric field dependence on \( \alpha_{n} \) and \( \alpha_{p} \), an estimate of the breakdown voltage of a p-n junction may be obtained.
The topic of avalanche multiplication has been introduced, and the most common application of it has been described. In the power MOSFET burnout calculation, it is necessary to determine a multiplication factor in terms of the number of holes generated through the avalanching mechanism for a given density of injected electrons and not the infinite value used in the ionization integral. Recall that the feedback model requires the density of avalanche generated holes returning from the base collector junction for a specific density of electrons injected (c.f., equation (2.8)). The avalanche multiplication model used in the power MOSFET burnout calculation will be presented in the next section.

3.2 Avalanche Multiplication Model Used in Burnout Calculation

In this section, the highly nonlinear relationships among collector current, electric field distributions, and avalanche multiplication in the collector depletion region of the parasitic BJT in the power MOSFET will be discussed. Numerical methods are used to obtain the avalanche generated hole density returning to the base region for a given electron density injected into the base collector space charge region. This result can not be obtained analytically because of the complicated relationships between the various parameters involved. The one dimensional Poisson equation will be solved across the base collector depletion region taking into account the space charge associated with the mobile carriers.

When the space charge of the mobile carriers is considered, the electric field across the base collector space charge region will be somewhat altered, depending on the density of mobile charge compared to the density of background impurity charge. A qualitative illustration of how the electric field is changed is shown in Figure 3.2 [24]. An idealized impurity profile through the base, collector, and substrate of the parasitic BJT in a typical power MOSFET is shown in Figure 3.2a. The two cases of zero and non-zero current are
Figure 3.2: (a) Idealized abrupt junction, constant doping profiles; (b) Qualitative view of charge distribution at zero current (light lines) and nonzero current (dark lines); and (c) Qualitative view of electric field and ionization rates at zero current (light lines) and nonzero currents (dark lines).

depicted in Figures 3.2b and 3.2c. The light lines correspond to the zero current case, and the heavy lines correspond to the non zero current case. The electric field and ionization rate plots are further labelled with the subscripts 0 and 1 to distinguish between zero and non-zero currents respectively. The total charge density for the non-zero current case, shown in figure 5b, has changed to reflect the electrons in transit across the junction. The total charge density to the left of the metallurgical junction, \(x_m\), is more negative (the electrons add to the total charge), and the total charge density to the right of the metallurgical junction is less positive.
than for the zero current case (the electrons subtract from the total charge).

The change in the total charge density is also reflected in the electric field distribution, shown in Figure 3.2c. Since the total charge density is more negative to the left of $x_m$ for non-zero current, the electric field in this region will have a steeper slope than for the zero current case. This effectively lowers the peak electric field at $x_m$ and moves $x_p$ to the right. Similarly, since the total charge density is less positive to the right of $x_m$ for non-zero current, the electric field in this region will have less of a gradient than for the zero current case. Since the reverse bias for each case is the same, the area under each electric field plot must be equal. This equal area constraint and the lower slope to the right of $x_m$, push the right edge of the electric field, $x_n$, deeper into the collector region. In the example shown in Figure 3.2c, $x_n$, has reached the epi-substrate boundary at which the electric field can penetrate no further. The electric field will assume a non-zero value at the epi-substrate boundary to satisfy the equal area constraint imposed by the Poisson equation. Therefore, two important phenomena occur in the reverse biased base collector junction when non-zero current flows: (1) the peak electric field at the metallurgical junction decreases, and (2) the electric field assumes a non-zero value at the epi-substrate interface. These two consequences significantly affect the avalanche multiplication, as will be shown later.

Also shown in Figure 3.2c is the impact ionization rate, $\alpha$, throughout the depletion region for zero and non-zero current. The functional dependence of $\alpha$ on the electric field will be shown later in Figure 3.4 of this chapter, but qualitatively it is exponentially related to the local electric field. This is why the value of $\alpha$ decreases significantly when the peak electric field drops with increasing current. We would expect the avalanche multiplication rate to significantly decrease with increasing current as well. For the remainder of this discussion $\alpha$ will be used to designate $\alpha_n$, and $\alpha_p$ will be neglected because it is at least an order of magnitude less than $\alpha_n$ over the electric field range of interest (Figure 3.4).
functional relationships between carrier densities, electric field, ionization rate, applied voltage, and the physical geometry of the parasitic BJT must be simultaneously solved to more precisely determine the avalanche multiplication rate.

The equations governing the physics of the base collector space charge region will be presented at this point. The base collector space charge region of the parasitic BJT is shown in Figure 3.3. The primary relationship is of course the Poisson equation, which in one dimension is given by [34]:

$$\frac{d^2 V(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon}.$$  \hspace{1cm} (3.7)

where $V$ is the potential across the space charge region in the $x$ direction, $\rho$ is the total charge density, and $\varepsilon$ is the dielectric constant of silicon. The boundary conditions for equation (3.7) are simply that the potential equals zero at the base edge of the depletion region and equals

![Figure 3.3: Space charge region of reversed biased base-collector in parasitic BJT.](image)
the applied voltage at the collector edge of the depletion region. As previously mentioned, both the space charge due to the depleted impurities and the space charge due to the carriers in transit across the junction will be considered in this calculation. The total charge density is given by:

\[ \rho(x) = q \left[ N_D(x) + p(x) - N_A(x) - n(x) \right], \]  

(3.8)

where \( q \) is the electronic charge, \( N_D(x) \) and \( N_A(x) \) are the donor and acceptor impurity concentrations within the depletion region, and \( p(x) \) and \( n(x) \) are the mobile hole and electron densities across the depletion region.

This model applies to power MOSFETs whose drain to source voltage during the OFF state is typically in the range of 100 V to 500 V [1]. This high drain to source voltage also appears as a reverse bias across the base collector junction of the parasitic BJT. The electric field resulting from these conditions well exceeds the critical field for electron velocity saturation (30 kV/cm) over most of the depletion region. The hole velocity saturates at about 200 kV/cm and reaches 70% of saturation velocity at 50 kV/cm. For this reason, electrons traveling from \( x_p \) to \( x_N \) or holes traveling from \( x_N \) to \( x_p \) will drift at or near their saturation velocity of \( 10^7 \) cm/s over most of the depletion region [28]. This makes use of the approximation that electron and hole saturation velocities are both equal to \( 10^7 \) cm/s. The hole velocity is actually about \( 6 \times 10^6 \) cm/s, but approximating the true carrier velocities by an average velocity over the entire depletion region has led to insignificant errors in avalanche breakdown calculations [35]. This approximation allows the electron current density, \( j_n(x) \), and hole current density, \( j_p(x) \), to be expressed as:

\[ j_n(x) = -q v_{sat} n(x), \]  

(3.9)
Figure 3.4: Impact ionization rate for electrons and holes versus inverse electric field.

\[ \alpha_n \text{(electrons)} \]
\[ \alpha_p \text{(holes)} \]

and

\[ j_p (x) = -q \nu_{\text{sat}} p(x), \quad (3.10) \]

where \( \nu_{\text{sat}} \) is the saturation velocity for the electrons and holes. Because of current continuity, in one dimensional current flow the total collector current density, \( j_c(x) \), must be constant. The total collector current density is given by the sum of equations (3.9) and (3.10), which is:

\[ j_c(x) = -q \nu_{\text{sat}} [ n(x) + p(x) ]. \quad (3.11) \]
Equation (3.11) just states that the sum of the electron and hole densities at any point \( x \) is constant across the depletion region.

The impact ionization rate, \( \alpha \), was defined in the previous section. A plot of \( \alpha \) for electrons and holes versus inverse electric field is shown in Figure 3.4 [33]. The dependence of \( \alpha \) on electric field can be approximated as [24]:

\[
\alpha(x) = A \exp \left[ -\frac{E_i}{E(x)} \right],
\]

where \( E(x) \) is the local electric field and \( A \) and \( E_i \) are fitting parameters. For electrons in transit, \( A \) and \( E_i \) equal 89 \( \mu \)m\(^{-1}\) and 1.2 MV/cm respectively. For holes in transit, \( A \) and \( E_i \) equal 260 \( \mu \)m\(^{-1}\) and 2.0 MV/cm respectively. In view of Figure 3.4, one can see that the impact ionization rate for holes is more than an order of magnitude less than the impact ionization rate for electrons in the electric field range of interest (\( 1/E = 4-8 \times 10^{-6} \) cm/V). For this reason, the impact ionization rate for holes will be neglected in the avalanche multiplication model used in the power MOSFET burnout calculation. Note that a more complicated expression could have been used in place of equation (3.12) (i.e., including an additional \( -E_i/E^2 \) inside the exponential [36]). However, the relationship between \( \alpha_n \) and inverse \( E \) is very close to linear on a log plot (Figure 3.4). If there is any small error due to the second order inverse \( E^2 \) term, the error will be present for all calculations in the model. The overall predictions of the order of magnitude changes in the entire model should not be greatly affected by such error. Neglecting the impact ionization rate for holes, equation (3.2), which describes the number of electron hole pairs generated per second in the distance \( dx \), can be written as [24]:

\[
d(n \nu_n) = n \nu_n \alpha_n dx,
\]
or

\[
\frac{dn(x)}{dx} = n(x) \alpha_n(x). \tag{3.14}
\]

The boundary condition for equation (3.14) is that \( \frac{dn}{dx} = 0 \) at the base edge of the depletion region. This simply means that there is no change in electron density due to avalanching until the interior of the depletion region is reached (electric fields present).

Now that the pertinent physical equations have been presented, the manner in which they are solved will be discussed. Recall that the desired result is the hole concentration at \( x_p, p(x_p) \), as a function of electron concentration at \( x_p, n(x_p) \), or:

\[
M = \frac{p(x_p)}{n(x_p)} \tag{3.15}
\]

There are six arrays of typically 300 points used in the calculation. These arrays are:

1. space charge, \( \rho(x) \)
2. electric field, \( E(x) \)
3. potential, \( V(x) \)
4. ionization rate, \( \alpha(x) \)
5. electron concentration, \( n(x) \)
6. hole concentration, \( p(x) \)

Given the impurity profile, the applied drain to source voltage, \( V_{DS} \), and the electron concentration at \( x_p \), the initial profiles of \( \rho(x), E(x), V(x) \), and \( \alpha(x) \) are calculated. The initial value for \( n(x_p) \) is chosen to reflect a very low current condition, \( i.e., n(x_p) \ll N_{DC} \). The initial profile for \( \rho(x) \) is calculated using equation (3.8) assuming that the electron concentration throughout the depletion region equals the concentration at \( x_p \). This neglects impact ionization, for the moment. The initial electric field profile, \( E(x) \), is found by integrating the charge density, \( \rho(x) \). The initial potential profile, \( V(x) \), is found by integrating the negative electric field profile and dividing...
Figure 3.5: Flowchart showing steps in avalanche curve calculation. The algorithm continues until the desired density of injected electrons is reached (typically about $5xN_D$).
by the dielectric constant of silicon. (See equation (3.7)). The integrations used in calculating $E(x)$ and $V(x)$ were performed using trapezoidal integration starting from $x_p$. Finally, the initial ionization rate profile, $\alpha(x)$, is found using $E(x)$ and equation (3.12).

Next, from $\alpha(x)$ a revised electron concentration, $n(x)$, is found by integrating equation (3.14) using trapezoidal integration starting from $x_p$. Now the hole concentration, $p(x)$, is found using $n(x)$ and equation (3.11). The carrier concentrations, $n(x)$ and $p(x)$, are then used to update the space charge profile, $\rho(x)$, for the next iteration step. At the next iteration step, the position of $x_p$ is updated by an algorithm to reduce the difference between the calculated $V(x_n)$ and the applied $V_{DS}$. The iteration continues until a self-consistent solution for the carrier densities exists simultaneously with the condition $V(x_n) = V_{DS}$. A self-consistent

![Figure 3.6: Avalanche curves for junction with breakdown voltage of 100 V operated at 95 V, 75 V, and 50 V.](image)
solution for the carrier densities occurs when the difference between the revised and unrevised electron concentrations after integrating equation (3.14) is less than 1% of their absolute value. A flowchart summarizing this algorithm is shown in Figure 3.5. The computer code for this calculation is given in Appendix C.

The solution, i.e., the $\rho(x), E(x), V(x), \alpha(x), n(x),$ and $p(x)$ profiles, is then archived. The electron concentration at $x_p$ is then increased by an increment, and the iteration towards self-consistency is resumed. The solution previously archived is used as the initial guess for the next iteration. As the solutions are archived, the particular values for $n(x_p)$ and $p(x_p)$ are stored in a separate file. After many solutions are archived, the functional relationship between $p(x_p)$ and $n(x_p)$ for a given power MOSFET biased at a given $V_{DS}$ is finally obtained.
Figure 3.8: Impact ionization rates corresponding to $n(x_p)/N_D = 0, 0.25, 0.5, 1.0, 1.5, \text{and } 2.5$ on the 95 V avalanche curve.

Typical results from these computations are shown in Figures 3.6-3.10 [24]. Figure 3.6 shows the avalanching characteristics for three different values of $V_{DS}$ in the normalized form of $p(x_p)/N_D$ versus $n(x_p)/N_D$, where $N_D$ is the collector doping concentration. The curves in Figure 3.6 will be referred to as avalanche curves hereafter. Figures 3.7-3.10 show $E(x)$, $\alpha(x)$, $n(x)$, and $p(x)$ respectively for various points along the avalanche curve for $V_{DS} = 180V$.

Avalanche curves were calculated for power MOSFETs operating at 50% to 95% of their rated drain to source breakdown voltage. The breakdown voltages ranged from 100V to 500V. There are always three distinct regions present in each avalanche curve as shown in Figure 3.6. The first region is the distinct hump appearing for values of $n(x_p)/N_D < 1$. The
drop at larger $n/N_D$ corresponds to an initial decrease in the avalanching rate with increasing current. The second region is the valley region or local minimum appearing for values of $n(x_p)/N_D < 1$. This corresponds to a near zero avalanching rate at a current level where the electron density and collector doping density are comparable. The third region of the avalanche curve appears for values of $n(x_p)/N_D > 1$, where the hole concentration increases at approximately the same rate as the electron concentration. Each of these regions will now be discussed in more detail to gain more insight into how the avalanche curve evolves.

The first region of the avalanche curve is best explained by the electric field and ionization rate profiles in Figures 3.7 and 3.8. The calculated electric fields in Figure 3.7 resemble the qualitative description shown in Figure 3.2c. For currents corresponding to
Figure 3.10: Hole densities corresponding to \( n(x_B)/N_D = 0, 0.25, 0.5, 1.0, 1.5, \) and 2.5 on the 95 V avalanche curve.

\( n(x_B)/N_D < 1, \) the peak electric field (at the metallurgical junction) decreases with increasing \( n/N_D. \) Since the area under each electric field profile must be the same because it corresponds to the applied voltage, the electric field assumes a non-zero value at the epi-substrate interface, located at \( x=6 \mu m. \) The calculated ionization rate profiles in Figure 3.8 reflect the changes in the electric field profiles. Initially, as the current increases and the peak electric field decreases, so does the ionization rate. The peak ionization rate occurs at the metallurgical junction, \( x=0, \) which is where the peak electric field occurs. The electric field and ionization rate profiles for \( n(x_B)/N_D = \{0, 0.16, \) and 0.5\} correspond to the first region of the avalanche curve [24].

The valley, or second region, in the avalanche curve is explained by the electric field
and ionization rate profiles for \( n(x_p)/N_D = 1 \). When \( n(x_p)/N_D = 1 \), the peak electric field is in the process of transferring location from the metallurgical junction over to the epi-substrate interface. The electric field is at a relatively low constant value across most of the depletion region for \( n(x_p)/N_D = 1 \). This results in an almost nonexistent ionization rate, which leads to a fairly low avalanche multiplication rate and hence the valley in the avalanche curve [24].

The third region in the avalanche curve corresponds to the asymptotic behavior for values of \( n(x_p)/N_D > 1 \). The profiles for \( n(x_p)/N_D = \{1.5 \text{ and } 2.5\} \) are taken from the third region of the avalanche curve. The peak electric field and the peak ionization rate occur at the epi-substrate interface for this high current portion of the avalanche curve. The electron and hole profiles for this third region, shown in Figures 3.9 and 3.10, provide insight into the asymptotic behavior of the avalanche curve. The electron and hole profiles for two significantly different currents are nearly constant and equal their values at \( x_p \) across the space charge region. Only near the epi-substrate interface do these curves significantly change from their nearly constant level. The electric field and ionization rate profiles are similar to the electron and hole concentration profiles in the sense that they are nearly constant over much of the depletion region and then significantly change at the epi-substrate interface. So when the electron densities are more significant than the background concentration, the hole concentration must rise at nearly the same rate as the electron concentration to keep the total charge density in the space charge region essentially unchanged. This gives rise to the near unity slope of the avalanche curve in the third region [24].

The model behind and the calculation of the avalanche curve has been presented in this section. Because of the highly nonlinear relationships between the total charge density, electric field, potential, and ionization rate across the space charge region, the iterative method used to calculate the avalanche curve requires considerable computation time. Typical computation times for avalanche curves taken out to \( n(x_p)/N_D = 4 \) are about three to
four days when performed on a 25 MHz 80386 based machine with a mathematical coprocessor. Each burnout calculation would take at least this long if the avalanche curve were calculated for each case. This long computation time motivates the idea of curve fitting the avalanche curves to a simple analytic function whose fitting parameters are linked to the breakdown voltage and the applied $V_{DS}$ of the power MOSFET. This method of parameterizing the avalanche curves was performed for this dissertation. Not only did the parameterization decrease the computation time for obtaining the critical condition, but it provided a simple method for incorporating the avalanche curves into the feedback model calculations performed in the last chapter. This will be the topic of the next section.

3.3 Parameterizing the Avalanche Curves

The time-consuming computations required to calculate an avalanche curve for a given device structure and operating condition necessitate one to parameterize these curves. Since each avalanche curve has essentially the same shape, it seems reasonable that one could describe the avalanche curve with a simpler analytical form. This is precisely what has been done.

Each avalanche curve is described by the sum of two relatively simple functions. One function is used to describe the behavior of the avalanche curve for $n(x_p)/N_D < 1$, and the second function describes the behavior of the avalanche curve for $n(x_p)/N_D > 1$. The function representing the lower current levels, $\pi_{LO}(n)$, is given by:

$$\pi_{LO}(n) = A n \exp\left[-\left(n/n_0\right)^k\right]. \tag{3.16}$$

Equation (3.16) describes the lower portion of the avalanche curve well. At low values
Figure 3.11: Components of the parameterization of avalanche curves, $\pi_{\text{LO}}$ and $\pi_{\text{HI}}$. of $n$, the function monotonically increases, and when the exponential term becomes significant the function decreases asymptotically to zero. This behavior can be seen in Figure 3.11, which explicitly shows $\pi_{\text{LO}}(n)$ and the function representing the higher current levels, $\pi_{\text{HI}}(n)$, which is given by:

$$\pi_{\text{HI}}(n) = S \ n_c \left\{ 1 + \left( \frac{n}{n_c} \right)^b \right\}^{1/b} - 1 \right\}. \tag{3.17}$$

For values of $n/n_c \ll 1$, $\pi_{\text{HI}}(n) = 0$, and for values of $n/n_c >> 1$

$$\pi_{\text{HI}}(n) = S \ (n - n_c). \tag{3.18}$$
Equation (3.18) describes a linearly increasing function with a slope of $S$, which is precisely what the avalanche curve looks like for higher current levels. The avalanche curve is then described by the sum of equations (3.16) and (3.17):

$$
\pi(n) = \pi_L(n) + \pi_H(n).
$$  \hspace{2cm} (3.19)

The various parameters appearing in equations (3.16) and (3.17) other than the independent variable, $n$, are: $A$, $n_0$, $k$, $S$, $n_c$, and $b$. These are used to fit equation (3.19) to a given avalanche curve. Equation (3.19) was fit to all of the calculated avalanche curves with good success. Figure 3.12 shows a calculated avalanche curve and the fitted curve from
equation (3.19).

The values for $A$, $n_0$, $k$, $S$, $n_c$, and $b$ were tabulated for all of the calculated avalanche curves. Values of these parameters for a variety of avalanche curves are shown in Table 3.1. These parameters were then linked to structural properties and operating conditions of the MOSFET. It turns out that the parameter $A$ in equation (3.16) is equal to the low current avalanche multiplication factor present in equation (3.5). A physical reason is because the derivative of equation (25) at $n=0$ is equal to $A$, and the slope of the avalanche curve at $n=0$ is the low current avalanche multiplication factor. The remaining parameters were related to a normalized parameter $V_{DS}/V_{BD}$, where $V_{BD}$ is the rated breakdown voltage of the power MOSFET. This enabled an interpolation algorithm to determine the fitting parameters for intermediate operating conditions. The time required to provide the avalanching conditions to the burnout calculation has been shortened from a time period of days to a time period of seconds through the use of equation (3.19).

<table>
<thead>
<tr>
<th>$BV_{DS}$ [V]</th>
<th>$V_{DS}$ [V]</th>
<th>$S$</th>
<th>$n_c$</th>
<th>$k$</th>
<th>$A$</th>
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<tr>
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<td>1.05</td>
<td>0.6</td>
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<tr>
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<tr>
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<td>0.17</td>
<td></td>
</tr>
</tbody>
</table>

Table 3.1: Values for parameterization of avalanche curves
3.4 Summary

An important part of the power MOSFET single event burnout calculation has been described in this paper. This was the avalanching behavior in the base collector space charge region of the parasitic BJT in the power MOSFET. A major component of the burnout calculation, the feedback mechanism, requires the number of avalanche generated holes returning to the parasitic base region for a given number of electrons entering the space charge region from the base region. The feedback mechanism was reviewed to see just what role the avalanching plays in burnout. Before describing the model used for determining the avalanching behavior, low current avalanching was examined. This provided insight to the important physical relations which contribute to avalanching. The avalanche multiplication model used in the power MOSFET burnout calculation was then presented. To obtain the avalanching behavior, the Poisson equation was solved taking the space charge associated with the mobile carriers into account. Numerical methods were necessary due to the highly nonlinear relationships between carrier densities, electric field, ionization rate, and the potential across the depletion region. The avalanche curve, which was a plot of the returning normalized hole density to the entering normalized electron density, was the result of the computations. The avalanche curve had the distinct shape of an initial hump followed by a linearly increasing portion for high current levels. This shape corresponded to the initial lowering of the peak electric field at the metallurgical junction and subsequent transfer to the epi-substrate interface. The characteristic shape of the avalanche curves enables them to be parameterized by two simple analytic functions. This avalanche curve parameterization reduces the computation time required by orders of magnitude. Hopefully, this section has provided some insight into this phenomenon.
CHAPTER 4
USING THE MODEL

In this chapter, the analytical model for SEB that has been developed will be used to calculate some SEB thresholds for a typical power MOSFET device structure. The key structural parameters and operating conditions in the SEB mechanism will be shown. All of the work done for this chapter was performed for this dissertation. The improvements in the numerical methods and enhancements in the models discussed in the last two chapters enable these calculations on realistic device structures to be performed.

4.1 Calculating Some Burnout Thresholds

Now that each part of the model has been developed, the burnout threshold for a particular power MOSFET will be calculated. The burnout threshold will be defined in terms of the linear energy transfer (LET) of the incident ion. For a first order analysis, LET is the stopping power divided by the volume mass density of the target material (i.e. silicon in this case) [18]. The LET will be expressed in units of MeV-cm$^2$/mg for these calculations. The following device parameters are to be used in the calculation:

- source: doping density = $2 \times 10^{20}$ cm$^3$
- p$^+$ body: doping density = $2 \times 10^{16}$ cm$^3$
- p$^+$ plug: doping density = $2 \times 10^{18}$ cm$^3$
- drain: doping density = $2 \times 10^{15}$ cm$^3$

junction depth = 1 μm
junction depth = 2 μm
junction depth = 4 μm
thickness = 22 μm

The length under the source region is 10 μm. These parameters result in a structure with a nominal breakdown voltage of 300 V. The average doping densities needed in this abrupt junction calculation were obtained from Gaussian-type doping profiles.

To express the burnout threshold in terms of LET of the incident ion, it is necessary to compare the magnitude of the current in the plasma filament at time $t_{on}$ with the critical...
condition for burnout given by the feedback mechanism. To find the electron current in the collector given by the feedback mechanism, the collector current density at the threshold for burnout must be integrated over one cell in the DMOS structure. The collector current density at the threshold for burnout for two different lengths of the p+ plug is shown in Figure 4.1. The curve with the lower current density is for a p+ plug which does not extend under the source region, and the curve with the higher current density is for a p+ plug which extends half way under the source region. The higher current density means a higher burnout threshold since the LET of an incident ion must be larger to generate a higher current. A top view of the DMOS structure is shown in Figure 4.2 for a square cell geometry. Recall that an actual DMOS device may incorporate a different cell geometry (i.e., hexagonal), but a

Figure 4.1: Collector current densities at the threshold for burnout for two positions of the p+ plug.
Figure 4.2: Top view of DMOS cell with square geometry.

square geometry is sufficient for this discussion.

The integration of the electron current density in the collector over the DMOS cell is approximated in the following manner. First, the current density is numerically integrated in the y direction of Figure 4.1. This result is then multiplied by the perimeter of the n⁺ source region shown in Figure 4.2. This perimeter will equal 120µm in the following calculations. The current that is calculated in this fashion is defined as the critical current for burnout. In other words, if the ion strike results in a current greater than the critical current, then the transient currents within the parasitic BJT will regeneratively increase until second breakdown sets in. If the ion strike results in an initial current less than the critical current, then the transient currents within the parasitic BJT will die out to zero.

The following algorithm is used to calculate the LET burnout threshold for a given DMOS structure: (1) Given the structural parameters and drain-source voltage, the critical condition is calculated as in Chapter 3; (2) Given the critical condition, the critical electron
current density in the collector is identified; (3) Given the critical collector current density, the critical current is calculated as described above; and (4) Equation A.8 (see Appendix A) at time $t_{on}$ is used to calculate the LET necessary to initiate the critical current. This algorithm is summarized in Figure 4.3. A non-ideal scaling factor, $\gamma$ is introduced at this point. This factor is used to scale part (4) in the above algorithm when comparing to part (3). The scaling factor, $\gamma$ is important because it facilitates the comparison between the current required for burnout and the current supplied by the heavy-ion generated current filament. Furthermore $\gamma$ can be used to fit the analytical model to experimental data. The device structure that will be used in the following calculation has the parameters given at the beginning of this section.

![Figure 4.3: Algorithm used to calculate SEB thresholds. Note that the step requiring the avalanche curve calculation is can be speeded up a great deal with a fit to the avalanche curves as given in Chapter 3.](image-url)
Figure 4.4: Dependence of burnout threshold on drain-source bias and position of p+ plug.

with one addition. The lateral extent of the p+ plug, \( y_e \), where

\[
y_e = y_s - y_p,
\]

(i.e., the length that it extends under the n+ source) will be varied. For example \( y_e = 0 \) \( \mu m \) means that the p+ plug does not extend under the source region and \( y_e = 5 \) \( \mu m \) means that the p+ plug extends 5 \( \mu m \) under the source region.

The LET burnout threshold is calculated as a function of \( y_e \) and \( V_{DS} \) using the algorithm above with \( \gamma = 0.2 \). The results of this calculation are shown in Figure 4.4, where \( y_e \) is varied from 0\( \mu m \) to 8\( \mu m \) and \( V_{DS} \) is varied from 150 V to 290 V. It should be emphasized that this is an example calculation to demonstrate effects of the model and is not intended to be an exact
solution.

The information contained in Figure 4.4 can be helpful in designing a DMOS device to be more resistant to SEB. The LET burnout threshold for a given device structure increases with increasing $y_e$ for a fixed drain-source bias. For an approximate doubling of the drain-source voltage, the threshold increases by approximately 15% to 50%. As one increases the extent that the p+ plug extends under the source (emitter), i.e., increases $y_e$, the total resistance seen in the base region of the parasitic BJT decreases. When incorporated into the feedback mechanism, this necessitates higher current densities in the base region for the critical solution (i.e., the lower resistance requires a higher current to drop a comparable voltage). For a given drain-source voltage, the threshold doubles for a four-fold decrease in base resistance. This suggests that the p+ plug should extend as far as possible below the source region to prevent burnout. The p+ plug can not extend so far as to influence the threshold voltage of the MOSFET, however. The base resistance of the parasitic BJT can also be influenced by the length of the n+ source. As the length of the n+ source is decreased, the base resistance is also decreased. Therefore, the LET burnout threshold increases with shorter n+ source lengths.

4.2 Temperature Dependence of Burnout Threshold

For this dissertation, it was desired to investigate the temperature dependence of the burnout threshold. The temperature dependence of the burnout mechanism can be readily introduced into the feedback mechanism and will now be outlined. In the foregoing discussion, it should be emphasized that the primary component of the burnout mechanism is the base current density flowing in the parasitic BJT. In order for the parasitic BJT to turn on and remain turned on, it must have a source of base current. Unlike 'normal' BJT operation, the base current is not supplied from a device terminal; rather, the base current is supplied through avalanche multiplication in the base-collector space charge region. It has
been shown that the hole current generated in the base-collector space charge region is a function of the doping density and thickness of the collector region, the applied drain-source bias, and the local injected electron density [24]. In the following discussion on the temperature dependence of the burnout mechanism, the focus will be on the base current generated through avalanche multiplication. In other words, the injected electron density will be held 'constant' as a function of temperature, and the change of avalanche generated holes will be monitored as a function of temperature. This is equivalent to accounting for the 2-3mV/°C decrease of base-emitter voltage in the parasitic BJT.

The temperature dependence is included in the aforementioned calculation via the impact ionization rate. The impact ionization rate (number of electron-hole pairs generated per unit path length) decreases with increasing temperature [37]. To first order, this is attributed to the shorter mean free path of the carriers. Recall the relationship given in Chapter 4:

\[
\alpha(x) = A \exp\left[-\frac{E(x)}{E_1}\right].
\] (6.1)

Recall that for a temperature of 300K, \(A\) and \(E_1\) were 89 \(\mu m^{-1}\) and 1.2 MV/cm, respectively. For a temperature of 400 K, \(A\) and \(E_1\) become 78 \(\mu m^{-1}\) and 1.3 MV/cm, respectively [38] (these values correspond to an empirical fit). Since the impact ionization rate is used explicitly in the solution to the Poisson equation, the avalanche-generated hole current density decreases with increasing temperature for the same injected electron current density and applied drain-source bias. A measure of the reduction in hole current density is shown in Figure 4.5. The ratio of the hole density returning to the base at 400 K, \(p_{400}\), and the hole density at 300 K, \(p_{300}\), is plotted as a function of the electron density, \(n\), injected into the base-collector space charge region of the parasitic BJT. The computed avalanche curve for 400 K was simply divided by the avalanche curve at 300 K as a function of normalized injected
electron density. The electron density has been normalized to the doping density in the collector, $N_D$. The shape of the curve in Figure 4.5 is similar to an avalanche curve with the exception of the saturating value at high electron densities. The saturation is because the avalanche curves are in the monotonically increasing portion (absolute difference between avalanche curves is the same in this portion of curves), and the relative difference between the two curves decreases as electron density increases. Note that the hole density at 400 K ranges from 30% to 90% of the hole density at 300 K over much of the operating region. This reduction of the source of base current at higher temperatures is equivalent to an increase of the burnout threshold of the device (i.e., in order to achieve the same level of base current, the electron current density in the collector must increase). The calculated temperature dependence of the burnout threshold will be presented in the next section.

The relationships governing the feedback mechanism can be solved to yield a collector current density distribution at the threshold for burnout, $j_{EC}$, for a given DMOS device.
structure as discussed earlier in Chapter 4 [24]. When the critical collector current density is integrated around one cell of the DMOS structure, a critical collector current for burnout is obtained. The critical collector current for burnout, calculated as a function of drain-source voltage and for ambient temperatures of 300K and 400K, is plotted in Figure 4.6. The calculations were performed as outlined in Figure 4.3. The only differences are that for the 400 K calculation, the appropriate avalanche curves were used, and the burnout threshold is expressed in terms of current necessary to initiate burnout and not LET. The device structure used in these calculations has a nominal breakdown voltage of 190V. The average doping densities in the source, p-body, p+ -plug, and drain region are $10^{21}$ cm$^{-3}$, $2 \times 10^{17}$ cm$^{-3}$, $2 \times 10^{19}$ cm$^{-3}$, and $2 \times 10^{15}$ cm$^{-3}$, respectively. The thickness of the drain region is 13 µm. As shown in Figure 4.6, the SEB threshold increases with increasing temperature and decreasing voltage. Recall that an increase of the critical current corresponds to an increase in the SEB threshold.

![Figure 4.6: Calculated SEB threshold (in terms of current required to initiate burnout) as a function of drain-source bias at temperatures of 400 K and 300 K.](image)
CHAPTER 5

SINGLE-EVENT BURNOUT EXPERIMENTS

In the previous chapters, an analytical model has been developed to help describe the SEB mechanism. For this dissertation, it was deemed necessary to perform various SEB experiments to help establish some validity in the trends exhibited by the analytical model. The experiments that follow were performed to obtain data relating the effects of base resistance variation, supply voltage variation, and temperature variation on the SEB sensitivity. The next chapter will use the data from this chapter to help support the findings in the previous chapters.

This chapter concerns the ground-based experimental testing of the single-event burnout phenomenon. Ground-based testing has been vital to the understanding of the basic mechanism leading to SEB, and it is necessary in order to qualify various power MOSFETs and power BJTs for use in the space radiation environment. In order to perform ground-based testing, a heavy ion source is required. Heavy ion accelerators provide such a facility. At a heavy ion accelerator, there is a highly energetic focussed beam of heavy ions that the device under test (DUT) is subjected to. The energy and species of the heavy ion can be reliably determined so that many different LET values can be obtained. One such heavy ion source is the tandem Van de Graaff accelerator facility at Brookhaven National Laboratories. Another heavy ion source is the 88-inch cyclotron facility at Lawrence Berkeley Laboratories.

This chapter is divided into three parts. In each section, the techniques and some experimental results are presented for different SEB experiments. The first section discusses destructive SEB testing, the second section discusses non-destructive SEB testing, and the third section discusses a temperature controlled SEB experiment.
5.1 Destructive Testing

The simplest SEB test to perform is the destructive test. As the name implies, in this test burnout is allowed to follow its destructive course. This test is useful to absolutely prove SEB for a given device type, bias level, and LET of the incident ion. Following this type of test, there is physical evidence of burnout (the destroyed part). A circuit suitable for performing the destructive test is shown in Figure 5.1 [25]. The resistor shown is to protect the power supply when burnout occurs (the DUT becomes a short circuit). The capacitor is present to provide current to the power transistor during SEB in the event that the current from the power supply is limited. The current transformer is used to monitor the shape of the burnout event. The DUT is biased such that it is blocking a large DC voltage and conducting no appreciable current (other than normal leakage currents). This is the worst-case bias condition for SEB to occur. The DUT is physically de-lidded prior to exposure in the heavy
ion chamber. This allows for a known LET and angle of incidence of the ion beam at the surface of the DUT.

A typical test procedure would go as follows. First, the DUT is positioned such that the heavy ion beam is incident on the center of the chip. The angle of the board holding the DUT can then be adjusted to set the desired angle of incidence of the heavy ion beam. A bias level significantly less than the rated breakdown voltage of the DUT is then applied. The device is exposed to the ion beam until a predetermined fluence is reached (e.g., $10^7$ ions/cm$^2$). Note that if SEB occurs during the first exposure, then the bias level was set too high if the goal was to determine the bias threshold for SEB for a given LET. If SEB does not occur, then the bias level is raised, and the DUT is once again exposed to the heavy ion beam until the given fluence level is reached. This process of increasing the bias level and exposing the DUT for a given fluence is repeated until SEB occurs. The bias threshold for a given LET for the DUT is obtained, and the size of the incremental increases of the bias level determines the error bars on the measurement. Results from a power BJT destructive SEB experiment will now be presented.

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Emitter Junction Depth (μm)</th>
<th>Base Junction Depth (μm)</th>
<th>Epitaxial Layer Thickness (μm)</th>
<th>Rated $V_{CEO}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2N5629</td>
<td>6.35</td>
<td>28.96</td>
<td>46.74</td>
<td>100</td>
</tr>
<tr>
<td>2N6056</td>
<td>6.60</td>
<td>22.86</td>
<td>30.23</td>
<td>80</td>
</tr>
<tr>
<td>2N6059</td>
<td>18.03</td>
<td>21.08</td>
<td>27.94</td>
<td>100</td>
</tr>
<tr>
<td>2N6284</td>
<td>6.10</td>
<td>20.07</td>
<td>32.77</td>
<td>140</td>
</tr>
<tr>
<td>M15003</td>
<td>10.41</td>
<td>34.29</td>
<td>50.29</td>
<td>140</td>
</tr>
<tr>
<td>2N3902</td>
<td>12.45</td>
<td>34.29</td>
<td>108.20</td>
<td>400</td>
</tr>
<tr>
<td>2N3055</td>
<td>60.96</td>
<td>86.61</td>
<td>100.80</td>
<td>60</td>
</tr>
<tr>
<td>2NXXXX</td>
<td>3.05</td>
<td>5.33</td>
<td>24.89</td>
<td>60</td>
</tr>
<tr>
<td>2N4033</td>
<td></td>
<td></td>
<td></td>
<td>80</td>
</tr>
</tbody>
</table>

Table 5.1: Junction depths, epitaxial layer thickness and rated breakdown voltage for power BJTs used in destructive SEB experiment.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Element</th>
<th>Energy [MeV]</th>
<th>LET ([\text{MeV} \cdot \text{cm}^2/\text{mg}])</th>
<th>Range [(\mu\text{m})]</th>
</tr>
</thead>
<tbody>
<tr>
<td>(^{197}\text{Au})</td>
<td>Gold</td>
<td>350</td>
<td>80</td>
<td>25</td>
</tr>
<tr>
<td>(^{127}\text{I})</td>
<td>Iodine</td>
<td>320</td>
<td>60</td>
<td>31</td>
</tr>
<tr>
<td>(^{79}\text{Br})</td>
<td>Bromine</td>
<td>285</td>
<td>37</td>
<td>37</td>
</tr>
<tr>
<td>(^{58}\text{Ni})</td>
<td>Nickel</td>
<td>265</td>
<td>27</td>
<td>42</td>
</tr>
</tbody>
</table>

Table 5.2: Characteristics of heavy ion species used in destructive SEB experiment.

Nine different NPN bipolar device types were characterized using the test setup just described in a simulated cosmic ray environment using heavy ions obtained from the tandem Van de Graaff accelerator facility at Brookhaven National Laboratory (BNL) [25]. The device parameters for the bipolar transistors are shown in Table 5.1. Specific mono-energetic ion species were chosen to span a linear energy transfer (LET) range from 27 to 80 MeV-cm\(^2/\text{mg}\) and penetration depths or ranges in silicon from 42 to 25 \(\mu\text{m}\), respectively. Ion penetration depth is thought to be critical to the test measurement and the burnout sensitivity of the power BJT. Penetration depth has been shown to be relevant in LET threshold measurements of power MOSFETs [39]. These same concepts apply to power BJTs as well. The characteristics of each selected ion are shown in Table 5.2 [25].

The normal test sequence used during SEB characterization went as follows: (1) the device was exposed to a fixed particle fluence, during which the collector current was monitored; (2) if burnout was not observed, the collector voltage was increased by typically 2 V to 10 V, upon which step (1) was repeated; and (3) the test sequence was terminated if burnout was observed or a predetermined collector voltage was reached. However, all test sequences were terminated if the collector voltage reached 334 V, due to voltage constraints of the power source and the voltage ratings of the capacitors used in the test circuit. In some
later experiments, the test voltage was limited to 400 V after some minor modification to the test circuitry was made. All experiments were performed under D.C. bias with the collector voltage of the device initially set lower than the expected voltage needed to induce device burnout – the SEB threshold voltage of the device for a given LET. The DUT was exposed to the selected ion species until a fluence of $1.0 \times 10^6$ ions/cm$^2$ was obtained. The test sequence was only interrupted if burnout was observed (burnout was detected by noticing the sudden large increase in power supply current after the device shorted out).

More than 400 individual runs were recorded at BNL. During these runs, over 40 test devices were exposed to one or more ion species. The four devices which exhibited repeated burnout behavior (2N5629, 2N6056, 2N6059, and MJ15003) are shown in Figure 5.2 [25]. The collector-emitter voltage normalized to the measured collector-emitter open-circuit breakdown voltage, $V_{CEO}$, is plotted against the LET of the incident ion. Each bar represents one single device. The dark shaded region represents the difference between the normalized
voltage at which the device exhibited burnout and the highest normalized voltage that the device did not burnout. Notice that the Darlington pairs, 2N6056 and 2N6059, are more susceptible to burnout than the single devices, 2N5629 and MJ15003. The ratio between the collector-emitter biases that resulted in burnout behavior to the measured $BV_{CEO}$ were in similar ranges as those obtained in high dose-rate burnout in power BJTs [40]. The trends in these data will be explained in the next chapter.

5.2 Non-Destructive Testing

One major shortfall of the above mentioned destructive testing method is that many power transistors may be used to obtain just one data point at one LET and one bias condition. The destructive test can be very expensive in terms of devices. This was the motivation behind the non-destructive testing method [41,42]. The circuit for the non-destructive testing method is shown in Figure 5.3. This circuit is very similar to that of the destructive method (see Figure 5.1), but the resistor is in a different place in the circuit. The resistor limits the current through the DUT such that the local power dissipation remains low enough that

![Figure 5.3: Non-destructive SEB test circuit using a power MOSFET as the device under test.](image-url)
burnout does not occur, in addition to protecting the power supply.

Whenever an ion strike initiates the burnout mechanism (turns on the parasitic BJT, allowing current to flow), the current transformer senses a current pulse. The heavy-ion-generated current pulses are then counted and stored on a computer. In a typical experimental run, the de-lidded DUT is exposed to the ion beam until the predetermined fluence is reached. The number of single events (current pulses) are counted for the entire exposure time. The data are usually presented by dividing the total number of events (units of ions) by the total fluence (units of ions/cm$^2$). The quantity obtained has units of cm$^2$, and it is called the SEB cross-section. The SEB cross-section is often associated with the surface area of the DUT which is sensitive to burnout. The LET of the incident ion is then varied (either by changing ion species, ion energy, or angle of incidence) to obtain the SEB cross-section for the desired range of LET values. The applied bias is the same for each of the data points in the SEB cross-
section versus LET curve.

A typical SEB cross-section versus LET of the incident ion is shown in Figure 5.4 [26]. These data were taken at Brookhaven National Laboratories with heavy ions having LETs of 29, 37, 39, 53, 57, 60, and 82 MeV cm$^2$/mg [43]. The device type is an IRF150 n-channel power MOSFET. The shape of the plot is typical in the sense that a threshold value of LET and an asymptotic SEB cross-section can be estimated. The threshold value of LET determines the minimum LET necessary to initiate burnout at that particular drain-source bias, and the asymptotic SEB cross-section is a measure of the surface area of the device that is vulnerable to SEB.

SEB cross-section data can also be presented in another way. Sometimes it may be desirable or necessary to use a single value of LET when characterizing a device. Each experimental run proceeds as described above by allowing the DUT to be exposed to a given

![Figure 5.5: SEB cross-section versus drain-source bias for an IRF150 n-channel power MOSFET using monoenergetic beam of 380 MeV krypton ions.](image)
fluence. The total number of events is then divided by the total fluence to obtain the SEB cross-section. The applied bias is then varied between experimental runs to obtain a SEB cross-section versus applied bias relationship.

A typical SEB cross-section versus drain-source bias curve is shown in Figure 5.5 for a IRF150 n-channel power MOSFET [38]. These data were obtained at the 88-inch cyclotron facility at Lawrence Berkeley Laboratories using a monoenergetic beam of 380 MeV Kr ions with an LET of 41 MeV cm²/mg [38]. Similar to the previous data, an asymptotic SEB cross-section can be estimated from these data. Also, similar to the threshold LET, a threshold drain-source bias can be estimated from the data. The threshold drain-source bias determines the minimum bias necessary to initiate SEB at that particular LET of the incident ion.

5.3 Temperature Controlled Testing

The non-destructive testing method can be easily changed to investigate the effects of elevated temperature on the SEB mechanism. A thermal controller with a resistive heater is added to the circuit as shown in Figure 5.6 [38]. The resistive heater and temperature sensor

![Figure 5.6: Temperature controlled, non-destructive SEB test circuit.](image-url)
are attached directly to the package of the DUT. It was found that if the system was allowed to stabilize for a few minutes after setting the desired temperature that the temperature across the surface of the chip was uniform (within the accuracy of the probe). This was verified with a thermal probe on the surface of the chip. The experimental procedure for this method is exactly the same as the non-destructive test with the exception of allowing the temperature to stabilize before exposure to the heavy ion beam [38].

Results from a temperature-dependent SEB experiment are presented in Figures 5.7 and 5.8 in the form of SEB cross-section versus drain-source bias for the IR6766 and IRF150

![Figure 5.7: Temperature dependence on the SEB cross-section versus drain-source bias for the IR6766 n-channel power MOSFET. The temperature is varied from 300 K to 373 K. The lines are drawn in to help guide the eye between lowest and highest temperature measurements.](image-url)
Figure 5.8: Temperature dependence on the SEB cross-section versus drain-source bias for the IRF150 n-channel power MOSFET. The temperature is varied from 302 K to 373 K. The lines are drawn in to help guide the eye between lowest and highest temperature measurements.

n-channel power MOSFETs with rated $BV_{DS}$ of 200 V and 150 V, respectively [38]. These data were taken at the 88-inch cyclotron facility at Lawrence Berkeley Laboratories using 380 Mev Kr ions with an LET of 41 MeV cm$^2$/mg. The temperature was varied from 373 K to about 473 K in each set of curves. Note that in each case that the threshold drain-source bias increased with increasing temperature, and that the SEB cross-section decreased with increasing temperature [38]. The physical reasons for these trends will be explained in a later chapter.
CHAPTER 6
VERIFYING THE MODEL

In this chapter, the model will be verified with some of the experimental results presented in the last chapter. This comparison is made in this dissertation to lend some validity to the trends seen in the model. The power BJT destructive SEB experiment, the power MOSFET non-destructive experiment, and the temperature controlled experiment will be used.

6.1 Power BJT Experiment

The burnout susceptibility as a function of base resistance has been shown experimentally for the case of power bipolar junction transistors. Recall that the magnitude of internal base resistance is a key parameter in the feedback mechanism for burnout. As the resistance is increased, the burnout susceptibility of the power BJT is increased. The resistance in the base region is directly proportional to the emitter stripe width, $w_E$. The wider the emitter stripe is the farther the lateral base current must travel before ground is reached, and hence the larger the internal base resistance is. The Gummel number is a measure of the areal doping density in the base region and is obtained by measuring the intercept current of the BJT [44]. The base resistance is inversely proportional to the Gummel number (i.e., the higher the base doping, the lower the resistance). Therefore, a measure of the resistance in the lateral base region can be obtained by dividing the emitter width by the Gummel number. A plot of this ratio for six of the device types is shown in Figure 6.1. Notice that the 2NXXXX, which never exhibited burnout behavior, has the lowest base resistance. The 2N6284, which exhibited burnout for only one part in seven, has the next lowest base resistance. The two Darlington pairs, 2N6056 and 2N6059, have similar base resistances and had similar burnout
Figure 6.1: Experimental dependence of burnout susceptibility as function of internal base resistance. The dark shaded regions correspond to devices which exhibited burnout, and the light regions correspond to devices which did not burnout.

susceptibilities. The two single devices which exhibited burnout, 2N5629 and MJ15003, have similar base resistances and had similar burnout susceptibilities. See Chapter 5, section 1 for the details of these devices.

This is direct experimental support for the dependence of base resistance on the SEB mechanism, as predicted by the model of the SEB mechanism.

6.2 Power MOSFET Experiment

Figure 5.4 also indicates that the LET burnout threshold decreases with increasing drain-source bias for a given device structure with $y_e$ held constant. This is due to the higher electric fields associated with the increased drain-source bias. Higher electric fields increase the impact ionization rate and hence the avalanche-generated hole current that flows to the base region from the collector region of the parasitic BJT. (i.e., more current is generated within the device for the same base-emitter bias) Therefore, when included in the feedback
mechanism, the current required to initiate burnout decreases with increasing drain-source bias. Note that the drain-source bias dependence on the LET burnout threshold is less than the parasitic base resistance dependence. The drain-source bias dependence on the burnout susceptibility of power MOSFETs has been shown experimentally [38]. Figure 2.5 has been repeated and is shown in Figure 6.2. Figure 6.2 shows the single-event burnout cross-section versus the applied drain-source bias for the IRF150 n-channel power MOSFET. Recall, in this experiment the non-destructive test technique was employed and a monoenergetic beam of 41 MeV cm²/mg Kr ions was used to irradiate the device. The cross-sections were obtained by dividing the total number of non-destructive events by the total ion fluence seen by the device [38]. Therefore, the cross-section is a measure of the likelihood that single-event burnout will occur. Note that as the drain-source bias is increased, the single-event burnout
cross-section also increases. This is in agreement with the calculations, and supports the SEB model.

6.3 Temperature Dependent Experiment

The temperature dependence was included in the analytical model in Chapter 4, and a temperature dependent experiment was discussed in Chapter 5. The intent here is to point out that the analytical and experimental results are consistent. The results from the analytical model are repeated in Figure 6.3, where the SEB threshold as a function of drain-source bias is calculated for the temperatures of 300 K and 400 K. The SEB threshold is given in terms of current necessary to trigger the regenerative feedback mechanism. Note that for any drain-source bias, the current required to initiate burnout increases with increasing temperature. Another way to read the results is that for a given critical current (i.e., a given LET of the

![Figure 6.3: Calculated SEB threshold as a function of drain-source bias at temperatures of 400 K and 300 K.](attachment:figure63.png)
incident ion), the drain-source voltage necessary to trigger SEB increases as the temperature increases. The previous two statements say that the vulnerability to SEB decreases with increasing temperature. This is in agreement with typical experimental results, which have been repeated in Figure 6.4 for the IRF150 power MOSFET. Recall that each of the data points in Figure 6.4 was obtained using 380 MeV Kr ions with an LET of 41 MeVcm²/mg. Notice that the critical drain-source voltage increases by approximately 12 V for an increase of 71 degrees.

Figure 6.4: Temperature dependence on the SEB cross-section versus drain-source bias for the IRF150 n-channel power MOSFET. The temperature is varied from 302 K to 373 K. The lines are drawn in to help guide the eye between lowest and highest temperature measurements.
CHAPTER 7

SUMMARY AND CONCLUSIONS

7.1 Summary

The phenomenon of single-event burnout of power transistors has been discussed. This phenomenon is one of the forms of ionizing radiation that naturally occurs in the space radiation environment. As an incident heavy ion traverses the device structure, electron-hole pairs are deposited along its track length. These electron-hole pairs constitute a short-lived current filament which can turn-on the parasitic BJT in the power MOSFET structure or the vertical BJT in the power BJT structure. Depending how hard the BJT is turned on, the BJT currents will either regeneratively increase until second breakdown (hence burnout) sets in, or the currents will decrease to zero leaving the device unharmed. Following SEB, the power transistor is permanently destroyed (a short circuit typically develops across the source-drain terminals).

An analytical model was then developed to help explain the SEB mechanism. The model centers around the operation of the parasitic BJT. It was shown that the feedback mechanism, which relates currents and voltages in the parasitic BJT, could be solved for a critical solution for burnout. If the currents given by the critical solution are exceeded by the heavy ion-generated current source at the turn on time of the parasitic BJT, then currents would regeneratively increase. The simultaneous increasing high currents and voltages trigger second breakdown of the bipolar and finally melt-down of the DMOS structure. If the initial current source does not exceed the currents given by the critical solution, then the transient currents in the parasitic BJT will die out to zero. The components of the feedback mechanism are: (1) electron injection from the emitter across the neutral base region into the
collector; (2) avalanche generated hole current originating in the base collector depletion region and directed towards the neutral base region; (3) hole current flow in the neutral base region; and (4) base-emitter voltage developed by hole current flow (ohmic drop).

The purpose of this model is to lend insight into the key device parameters and operating conditions that determine the single-event burnout vulnerability of a given n-channel power MOSFET. The model indicates that the LET burnout threshold of power transistors increases with decreasing base resistance (either by extending the p+ plug further under the source region, or by decreasing the n+ source length), increases with decreasing drain-source bias, and increases with increasing device operating temperature. In an example calculation the LET burnout threshold doubled when the base resistance was decreased by four-fold; the LET burnout threshold increased by a factor of 15% to 50% with a decrease in the applied drain-source voltage of approximately 50%; and the drain-source bias threshold increased by 10 V to 15 V for a temperature increase of 100 degrees Celcius.

Three different SEB experiments were conducted to investigate the trends that the analytical model predicts. A destructive power BJT SEB experiment was conducted to show the dependence of base resistance on the SEB threshold. A nondestructive power MOSFET experiment was conducted to illustrate the drain-source bias dependence. And finally, a nondestructive temperature-dependent SEB experiment was conducted to explain the temperature dependence in the analytical model. The experimental and analytical trends are found to be in reasonable agreement. The concepts developed from this model can be used to design power transistors with a lower sensitivity to single-event burnout.
7.2 Conclusions

There are several key conclusions that may be made that concern the development of SEB resistant power transistors. The most significant device parameter that influences the SEB susceptibility of the power transistor is the resistance of the base in the parasitic BJT. As shown in Figure 4.4, a four-fold reduction in base resistance resulted in a doubling of the threshold LET. Recall that this reduction in base resistance was accomplished by expanding the p+ plug region for a given cell size. Note that the base resistance could also be decreased by making the overall cell size smaller (this would decrease the length of the n+ region). The significance of a doubling of the threshold LET should be pointed out. The expected integral flux of heavy ions for a typical geosynchronous orbit is repeated from Chapter 1 in Figure 7.1. If the 'Adam's 90% worst-case environment is chosen' (curve labeled 10%), an order

![Figure 7.1: Integral particle flux versus linear energy transfer for a typical geosynchronous orbit (See Chapter 1).]
of magnitude reduction in the integral flux of particles capable of causing burnout may be obtained (depending on what the initial level of LET threshold was). An order of magnitude reduction in integral flux would translate to an increase in device lifetime of approximately 10 times.

The model and experimental data also predict an improvement in the SEB susceptibility with a reduction in the drain-source bias. This of course can be implemented by simply derating the part (i.e., use a 500 V transistor when only a 250 V transistor is needed). This method would work, if one is willing to have more on-state switching losses than necessary. Recall that as the breakdown voltage of a power transistor is increased, the thickness of the epitaxial layer must increase, and the doping density of the epitaxial layer must decrease. Each of these changes increases the on-resistance of the transistor. Using a conservative estimate, a 500 V transistor would have at least twice the on resistance as a 250 V transistor would. Thus, derating the part accomplishes an increase in the SEB threshold at the expense of higher on-state switching losses.

The model and experimental data also suggest that the operating temperature of the power transistor also affects the SEB susceptibility. As the temperature is increased, the SEB threshold increases. The author is not suggesting, however, that one should blindly go and operate the power transistors at elevated temperatures. There are certainly reliability concerns when one contemplates operating any electronic device at elevated temperatures. The trade off between the high temperature reliability issue and the high temperature SEB issue has yet to be carefully addressed.

It is important to point out that any one of several other device parameters could have been used as a variable in determining the SEB threshold. However, one should not simply decide to change device parameters simply to reduce the SEB susceptibility without first
checking how the performance of the power transistor is altered. It is desirable to alter a
device parameter to improve the SEB threshold without altering the device performance. For
example, in other SEB models authors have suggested altering the source (emitter) doping
density in order to improve the SEB threshold [45, 46]. In one case the authors suggest
decreasing the doping density in the emitter [45]. This would in turn reduce the gain of the
parasitic BJT by reducing the emitter injection efficiency. In another case, the authors
suggest increasing the doping density in the emitter until bandgap narrowing in the emitter
region sets in [46]. This also reduces the emitter injection efficiency. In both cases, the
reduction in emitter injection efficiency increases the SEB threshold. The model presented
in this dissertation also predicts such a trend (A reduction in emitter injection efficiency
pushes the onset of the critical condition to higher current levels). This parameter variation
has not been investigated in this dissertation because of the effect it has on the MOSFET
parameters. Recall from Chapter 1 that the channel of the MOSFET is formed by the
difference in diffusion rates between the dopants in the source (emitter) and in the body
(base). If one changes the doping density in the source (emitter), the channel properties will
be significantly altered, as will the threshold voltage. Essentially, if one significantly changes
the doping density in the source (emitter) region, the entire source-body diffusion problem
will need to be re-engineered in order to obtain comparable channel lengths and threshold
voltages. Therefore, altering the doping density of the source (emitter) region is not desirable
a desirable option in most cases.

To re-iterate, changing the base resistance is the best way significantly alter the SEB
threshold. As long as the p+ plug is not expanded such that it influences the channel region,
the MOSFET parameters are unaltered. Also, as long as the MOSFET cells are not so small
that the parasitic resistance between cells due to the parasitic JFET resistance [REF], the
MOSFET parameters should be unaltered (unless the effective channel length is changed by
size and number of cells).
7.3 Areas for Future Investigation

In the course of any project of this scope, there are always areas that merit additional investigation to help further the understanding of the phenomenon. For this work, there are three distinct areas that warrant further studies. They are 2D or 3D device simulations, careful modeling of the parasitic BJT turn-on mechanism, SEB cross-section prediction, and dynamic bias implications. Each of these areas will now be briefly discussed to explicitly show what may be gained from their study.

7.3.1 2D or 3D Device Simulations

As mentioned earlier in Chapter 3, investigation of the SEB mechanism through the use of sophisticated device simulators merits further work. The dynamic aspects of the SEB mechanism were qualitatively argued. Modeling the dynamic aspects of the SEB mechanism with the use of a two-dimensional device simulator such as PICSES (or MEDICI) would result in a much deeper understanding of the turn-on of the parasitic BJT. A device structure such as that shown in Figure 7.2 would be a reasonable starting point for such simulations. The cylindrical cell shape is convenient because that is what can be done on a 2D simulator. If hexagonal or another shape cells need to be simulated, then the 3D simulator must be used. At a more basic level, the simulation of dynamic aspects of the heavy-ion-generated current filament in the structure would show the relationships between axial drift current and radial diffusion (Some work in this area is currently under investigation in [47]).
Figure 7.2: Sample device structure for simulation on 2D code such as PISCES or MEDICI.

7.3.2 Modeling the Parasitic BJT Turn-On

In Chapter 2 the turn-on of the parasitic BJT was briefly mentioned. It was assumed that every ion supplying enough current for triggering the regenerative feedback mechanism was capable of turning on the parasitic BJT. The dynamic aspects of this problem warrant some investigation. If the filament lifetime is comparable to the turn-on time of the parasitic BJT, this is certainly an important issue. The turn-on problem could be addressed with the help
of 2D and 3D simulation tools; however, it may be possible to apply some simple analytical models for preliminary investigation. The analytical model would be centered around a charge storage model of the parasitic BJT. This charge storage model would take into account the charge deposited by the ion strike and couple this to: (1) charge generated through avalanche multiplication; (2) charge necessary to build up in the base-emitter depletion region to support the base-emitter voltage; and (3) and charge (current) necessary to develop the ohmic drop in the neutral base region needed to sustain the base-emitter voltage. A simple RC charging circuit (modeling the resistance and capacitance associated with the base-emitter junction) driven by a dynamic current source (current filament) that takes into account the charges previously mentioned is imagined. This work should at least lend preliminary information as to the possibility of solving the SEB problem through device parameters associated with the turn-on of the parasitic BJT.

7.3.3 SEB Cross-Section Prediction

Recall that throughout the modeling of the SEB mechanism the SEB cross-section was not mentioned. In discussing the SEB threshold, the critical LET and critical $V_{DS}$ were used, but the SEB cross-section was not. However, in the experimental data the SEB cross-section is certainly an interesting quantity. Modeling of the SEB cross-section may be performed in a straightforward manner, if the concept of a critical region on the top surface of a power transistor being equivalent to the SEB cross-section is valid. Figure 7.3 helps to illustrate this point. If an ion generates enough current to cause burnout at the position shown in Figure 7.3a, then the region sensitive to burnout on the surface of the power MOSFET is at least the shaded portion (the current generated will forward bias the parasitic BJT at higher levels at positions further from ground). Similarly, the region sensitive to SEB on the surface of the power MOSFET is at least the shaded portion in Figure 7.3b. The words 'at least the shaded
Figure 7.3: (a) DMOS structure showing heavy ion strike and sensitive surface region at critical condition; (b) same as (a) except for different ion position. The sensitive surface regions are shaded.
region' were used because the regions between the power MOSFET cells may be sensitive to burnout. Also note that total sensitive region would be that shown in Figure 7.3 multiplied by the number of cells in the DMOS structure plus part of or all of the area between the cells. Furthermore, the LET associated with Figure 7.3b would be higher than that of Figure 7.3a (a higher current is necessary to bias the base-emitter voltage to the critical condition with a shorter path – i.e., lower resistance – to ground). Some of the work done pertaining to 2D or 3D device simulators could be useful here.

7.3.4 Dynamic Bias Implications

Since a large drain-source bias is necessary for the feedback mechanism to regeneratively increase the currents within the parasitic BJT (high electric fields are necessary to create the avalanche-generated holes in the base-collector space charge region), one would expect a power MOSFET operated with a dynamic bias to burnout less frequently than one operated with a static bias. This has been shown experimentally when the SEB cross-section was reduced by over two orders of magnitude when the MOSFET operated in a switch mode power supply compared to that when the MOSFET operated with a static bias [43]. The problem with that study was the inability to control the switching frequency, duty cycle, and peak drain-source voltage since the circuit was designed to operate at one frequency, duty cycle, and peak drain-source voltage. To better understand the influence of dynamic bias conditions on the SEB susceptibility of power MOSFETs, it would be interesting to be able to independently control the switching frequency, duty cycle, and the peak drain-source voltage.

Such an experiment would be very similar to the well-established non-destructive SEB test technique that was discussed in Chapter 5, except that instead of the constant DC drain-source bias a switching drain-source bias would be applied. The power MOSFET would still
remain off during heavy ion exposure (i.e., no drain-source current), but the effects of the switching drain-source bias would be isolated. The drain-source bias would have independent control over the switching frequency, duty cycle, and the peak drain-source voltage. A rough sketch of the experimental set-up is shown in Figure 7.4.

It is hypothesized that as the off time of the power MOSFET is reduced, the burnout susceptibility should also reduce. In view of the regenerative feedback portion of the burnout mechanism, when the drain-source voltage is dropped to zero the high electric fields necessary to generated the avalanche hole current are extinguished. The burnout mechanism will also be shut down. If the frequency is increased or the duty cycle is increased for a given frequency, the off time will obviously decrease and one should be able to see a change in the burnout susceptibility. It should also be noted that if the frequency or duty cycle is increased high enough to make the duration of the zero value of drain-source voltage short enough such that the burnout mechanism is not completely shut down, the effects of a dynamic bias on the SEB rate may not be as dramatic.

Figure 7.4: Non-destructive dynamic SEB experimental set-up
APPENDIX A

RADIAL DIFFUSION OF HEAVY ION GENERATED CURRENT FILAMENT

This appendix will discuss the radial time evolution of the initial current source. The discussion of the initial current source and the corresponding assumptions is only a first order analysis, and its intent is to lend basic insight into the radial diffusion of the filament.

The evolution of the initial current source is governed by: (1) the kinetic energy of the incident ion and its stopping power in silicon [48]; (2) the diffusion coefficients and mobilities of carriers within the plasma filament (carriers along the ion track); and (3) the impurity profiles and operating conditions of the parasitic BJT [23]. The kinetic energy and stopping power of the incident ion determine the number of electron-hole-pairs (ehp’s) generated in the silicon. The diffusion coefficients and carrier mobilities within the plasma filament determine the rate at which the ehp’s generated along the ion track will diffuse radially into the silicon. The impurity profiles and operating conditions of the parasitic BJT determine the initial strength of the current source. Each of these three points will now be expanded upon.

The number of ehp’s generated in a given target material due to the passage of a given heavy ion is a function of the energy of the incident ion and species and of the target material. One can relate the kinetic energy of an incident ion to a quantity called its stopping power using a model developed by Ziegler [18]. The stopping power of an ion is a measure of the energy lost by the passing ion and deposited in the target material. Stopping power has units of energy per distance (i.e., MeV/μm). The energy deposited in the target material results in ehp generation. In silicon, the energy required to generate an ehp, \( E_p \), is equal to 3.6 eV [49]. To obtain the number of ehp’s per track length of the incident ion, one simply divides the
stopping power, $S$, by 3.6 eV:

$$N_p = \frac{S}{E_p} \left[ \frac{ehp}{\mu m} \right]$$ \hspace{1cm} (A.1)

where $S$ has the units of eV/\mu m. For example, the stopping power in silicon is 6.3 MeV/\mu m for a 150 MeV iron ion. Application of equation (A.1) yields ehp/\mu m for this incident ion. Note that equation (A.1) assumes that the stopping power is equal to the entrant stopping power and is constant along the track length of the ion. In reality, the stopping power is a continuous function of the ion energy; and if the ion is stopped within the device, the stopping power may vary over two or three orders of magnitude [18]. For ions found in the space environment, the energies are sufficient to pass completely through the device. Furthermore, equation (A.1) could be obtained by integrating the stopping power over the track length of the ion and dividing by the path length to obtain an average stopping power. To first order, this analysis is sufficient.

Initially, the electron-hole pairs are generated along the ion track, creating a steep carrier gradient in the silicon. Carriers will tend to diffuse away from their initial position along the ion track due to this steep gradient. To obtain an analytically tractable model for the time evolution of the generated ehp's, the carrier plasma is approximated as a uniform line source at time $t=0$ that diffuses radially with a constant diffusion coefficient. This constant diffusion coefficient is approximated by [50]:

$$D = \frac{kT}{2q} (\mu_n + \mu_p) = 20 \frac{cm^2}{s}. \hspace{1cm} (A.2)$$

It is also assumed that the radial and axial motion of the carriers are totally decoupled and may then be treated independently. With this assumption, the time evolution of the radial
profiles of the ion-generated electrons, $n_p$, and of the ion-generated holes, $p_p$, can be expressed as [51]:

$$n_p(r,t) = p_p(r,t) = \frac{N_p}{4\pi D_t} \exp\left[-\frac{r^2}{4D_t}\right]$$  \hspace{1cm} (A.3)

In the high-concentration core region of the plasma-filament, the electron and hole distributions are almost precisely congruent because the space charge associated with any deviations would cause high electric fields that would immediately disperse the charge (i.e., the electron distribution is totally screened by the hole distribution and vice versa). Potential differences between the core of the plasma-filament and the outside are supported by the radial deviations of the hole and electron profiles in the fringe region of the filament which generate the electric fields necessary to support the radial potential differences [23].

Equation (A.3) is a Gaussian function in $r$, with a peak concentration occurring at $r=0$. It should be noted that the peak carrier concentrations decrease with time, as one would expect. We can rearrange equation (A.3) to get an expression for the radius of a given concentration, $N_{BCi}$, versus time:

$$r_i(N_{BCi}, t) = \sqrt{4D_t \left[-\ln\left(\frac{4\pi D_t N_{BCi}}{N_p}\right)\right]}.$$  \hspace{1cm} (A.4)

The terms in equation (A.4) are identical to those in equation (A.3) with the exception that $N_{BCi}$ has replaced $n_p$ or $p_p$. In Figure A.1, equation (A.4) is plotted versus time for two radii: $r_b$ which corresponds to the concentration $N_{BCb} = 10^{17}\text{cm}^{-3}$; and $r_c$ which corresponds to the concentration $N_{BCE} = 10^{15}\text{cm}^{-3}$. These concentrations correspond to typical base and collector doping densities in the parasitic BJT. Equation (A.3), for the case of $r=0$, is also plotted in Figure A.1. As shown in Figure A.1, both radii grow to a maximum and then decay to zero, while the peak concentration decays to $N_{BCi}$ when the corresponding radius shrinks.
Figure A.1: Radii $r_b$, corresponding to concentration in plasma filament equal to base doping density, and $r_c$, corresponding to concentration in plasma filament equal to collector doping density, and the peak plasma concentration versus time.

to zero. The importance of these properties of various radii will become apparent when carrier densities that are able to turn on the parasitic BJT are discussed.

Several other interesting and important relationships can be developed using equations (A.3) and (A.4). One relationship that will be useful in determining the current within a core region of radius $r_i$ is the total number of carriers contained within that core per unit core length. The core length is in the same direction as the ion track. Integration of equation (A.3) from 0 to $r_i$ yields:

$$N(r_i) = N_p \left[ 1 - \exp \left( \frac{r_i}{4Dt} \right) \right] = N_p - 4\pi D t N_{BCi}.$$  \hspace{1cm} (A.5)
Another interesting relationship that gives the time at which a particular radius, \( r_i \), vanishes can be found by setting equation (A.4) to zero and solving for \( t \). The result is:

\[
T_i = \frac{N_p}{4\pi D N_{BCi}}.
\]  

Equations (A.3) - (A.6) describe aspects of the time evolution of the heavy-ion-generated electron-hole-pairs. One more issue must be resolved before an expression for the current within the plasma filament can be written. With typical power MOSFET drain-to-source voltage ratings of 50 V to 500 V, and typical distances between drain and source contacts in the tens of microns range, the electric fields throughout much of the collector depletion region will be above the saturation field, \( E_{sat} \) [23]. In silicon, \( E_{sat} = 100 \text{ kV/cm} \) [52]. This causes the holes and electrons to drift at saturation velocity, which is taken to be \( v_{sat} = 10^7 \text{ cm/s} \) for both electrons and holes [52]. Thus, the current within a core region defined by \( r_i \) is simply the product of the saturation velocity and the total charge per unit length. This current is given by:

\[
I_i = q v_{sat} N(r_i).
\]  

Equation (A.7) gives the total current within a core region defined by \( r_p \), which corresponds to a particular carrier concentration level. In light of equations (A.3) - (A.7), the instantaneous current density within a core region is constantly changing. Somewhere between the uniform line source created by the heavy ion strike and the totally diffused plasma filament lies this initial source that acts to turn on the parasitic BJT. The parasitic BJT has a finite turn on time, \( \tau_{on} \). The value of the initial current source at time, \( \tau_{on} \), will be used as the current that drives the parasitic BJT. The resulting current that drives the parasitic
BJT is expressed as:

\[ I_{on} = q \nu_{sat} N(r_c, \tau_{on}). \]  \hspace{1cm} (A.8)
Included in this appendix is the source code that solves for the critical condition. The software is written in the C programming language [53].
/****** crit_vbe() ******/

int crit_vbe(avcrv_def *avcrv_p, npn_def *npn_p)
{
    double dy, m, nxc, px, pxp, ex, p_lo, p_hi, n, vbestep;
    double *a, *nu0, *nuc, *s, *k, *lp;
extern double OVBEMIN, q, VSAT, N1, N12, DN, DP, LP, TP, B;
    int y;
    double umtocm = 1E-04; /* convert microns to cm */
    
    nde = &npn_p->nde;
    ndc = &npn_p->ndc;
    wb = &npn_p->wb;
    na = &npn_p->na;
    yc = &npn_p->yc;
    vcrit = &npn_p->vcrit;
    nxp0 = &npn_p->nxp0;
    ppx0 = &npn_p->pxp0;
    vbe = &npn_p->vbe;
    r = npn_p->r;
    ib = &npn_p->ib;
    jhb = &npn_p->jhb;
    jhe = &npn_p->jhe;
    jhc = &npn_p->jhc;
    jec = &npn_p->jec;
    yy = &npn_p->yy;
    a = &avcrv_p->a;
    nu0 = &avcrv_p->nu0;
    nuc = &avcrv_p->nuc;
    s = &avcrv_p->s;
    k = &avcrv_p->k;

    for (y=0; y<N_YSTEP; y++) {
        ib[y]=0;
        jhb[y]=0;
        jhc[y]=0;
        jhe[y]=0;
        vbe[y]=0;
        jec[y]=0;
        yy[y]=0;
    }

    lp = pow((DP*TP), 0.5);
    dy = (*yc)/N_YSTEP;
    vbe[0] = VBSTART;
for (;;)
{
  ib[0] = 0;
  yy[0] = 0;
  for (y=0; y<(N_YSTEP); y++)
  {
    ex = exp(vbe[y]/VT);
    nxc[y] = q*VSAT*nxc;
    n = nxc/(*ndc);
    p_lo = (*a)*n*exp(-pow((n/(*nu0)),(*k)));
    p_hi = (*s)*(*nuc)*pow((1+pow((n/(*nuc)),B)),(1/B)) - 1;
    m = (p_lo + p_hi)/n;
    pxc = m*nxc;
    jhc[y] = q*VSAT*pxc;
    pxe = (NI2/(*nde))*exp(1+pow((NI/(na[y])),2.0)*ex);
    jhe[y] = (q*DP/LP)*pxe;
    if (y==0)
    {
      (*nxp0) = nxc;
      (*pxp0) = pxc;
    }
    if (jhc[y] == jhe[y])
      jhb[y] = jhc[y] - jhe[y];
    else
    {
      (*vcrit) = STABLE;
      printf("Device intrinsically stable\n");
      return OK;
    }
    ib[y+1] = ib[y] + jhb[y]*dy;
    vbe[y+1] = vbe[y] - 1000*r[y]*ib[y]*dy;
    yy[y+1] = yy[y] + (1E04)*dy;
    jhb[y+1] = jhb[y];
    jhe[y+1] = jhe[y];
    jhc[y+1] = jhc[y];
  } /* loop until all y's exhausted */

  if (fabs(vbe[N_YSTEP]) <= DVBEMIN)
  {
    (*vcrit) = vbe[0];
    return OK;
  } /* quit when boundary value is satisfied */
  vbestep = 0.005 * fabs(vbe[N_YSTEP]);
  if (vbe[N_YSTEP] < 0)
    vbe[0] = vbe[0] - vbestep;
  else
    vbe[0] = vbe[0] + vbestep;
} /* end of for(;;) */
} /* end of crit_vbe() */
APPENDIX C

SOFTWARE ROUTINE FOR SOLUTION TO AVALANCHE CURVES

Included in this appendix is the source code that generates the avalanche curves. The code is written in A Programming Language (APL) [54].
AVALANCHE[" "]

[0] AVALANCHE

[1] " PROMPT USER FOR NA, ND, NO(XP), N+STEP, N, KT, XPMIN,


[3] AV INPUT

[4] " INITIALIZE L, I, F, G VB, VD, K, NO, DNO, KM, DNS, FI, EMIN,

[5] " XP, XN, XXP, NN, XNX, M, AND M1

[6] AV INITIALIZ

[7] CHOOSE:

[8] " PROMPT USER IF DEPLETION APPROXIMATION OR PREVIOUS RUN IS TO BE

[9] " USED FOR THE INITIAL CONDITIONS FOR THE CALCULATIONS

[10] " PLEASE SELECT THE INITIAL CONDITIONS:'

[11] " (1) DEPLETION APPROXIMATION'

[12] " (2) PREVIOUS DATA FILE'

[13] " ASSIGN VARIABLES ACCORDINGLY USING PREVIOUS DATA

[14] AV-START'UP

[15] +L1

[16] L0:

[17] " CALCULATE CHARGE DENSITY, ELECTRIC FIELD, POTENTIAL GRADIENT,

[18] " IONIZATION RATE, ELECTRON CONCENTRATION, AND HOLE CONCENTRATION

[19] " USING THE DEPLETION APPROXIMATION.

[20] AV-DEP'APROX

[21] L1:

[22] " CALCULATE r, E, V, A, N, & P ITERATING ON THE CHARGE DENSITY

[23] AV CALC

[24] " CHECK IF FIRST CONSTRAINT IS SATISFIED (CHECK SECOND ONE IF IT IS)


[26] " CHECK IF SECOND CONSTRAINT IS SATISFIED (JUMP TO L3 IF IT IS)

[27] " L3: DN: M1[N+NP;6]-M[N+NP;6]

[28] " EITHER CONSTRAINT 1 OR CONSTRAINT 2 NOT SATISFIED ***

[29] " SET VALUE OF XP FOR THE NEXT ITERATION

[30] AV FIX XP

[31] " CHECK FOR XP CROSSING XJ'0, ALSO MOVE DATA POINT

[32] " FROM P-SIDE TO THE N-SIDE IF NECESSARY.

[33] AV CHK CROSS

[34] " ITERATE K TIMES

[35] " L1: 0-K K-1

[36] " INCREMENT CARRIER CONCENTRATION AT XP, NO, AND FIX VALUE FOR

[37] " CONSTRAINT 2.

[38] " NO NC+DNC

[39] " DN: 0.00002 NO

[40] " L1

[41] L2:

[42] " SELF-CONSISTANT SOLUTION! -- WRITE TO DISK ***
AV WRITE

* STEP NO(XP)

AV STEP

* CONTINUE FINDING SOLUTIONS UNTIL NO>10*ND

* STEP I: STEP VD

1: I+1

NO=NOO

L=0

* LOV & I<IK

*AV FIX XP[]]

AV FIX XP; PAR; AVNA; AVND

* THIS FUNCTION SETS THE VALUE OF XP FOR THE NEXT ITERATION

PAR=ML[;1]<0

"L1": (XP=0)

AVNA +/-ML[;2]*PAR*1.6E-19+/PAR

"L2"

"L1"

AVNA=0

"L2"

PAR=ML[;1]>0

AVND= +/-ML[;2]*PAR*1.6E-19+/PAR

"L3": AVND<0.01*ND

XP: XP+10000*(AVND,ND)*(VD-/ML[;4])* (AVNA+AVND)* /ML[;3]

"L4"

"L3"

XP: XP-100000000*11.7*6.85E-14*(VD-/ML[;4])*1.6E-19 AVNA* XEPF

"L4"

ML[1;1 6],/ML[;4 5 6],K
AV INPUT[j]

AV INPUT; PAR

THIS FUNCTION ACCEPTS KEYBOARD INPUT TO INITIALIZE VARIOUS
GLOBAL PARAMETERS THAT ARE LOCAL TO THE FUNCTION AVALANCHE

'ENTER NA, ND, NO(XP), N+STEP, (CCM), KT, ∆XPMN (UM)'

PAR " !
NA = PAR[1]
ND = PAR[2]
NO = PAR[3]
NSTEP = PAR[4]
KT = PAR[5]

DXPMN = PAR[7]

'ENTER VD, VD-STEP, VDM, DVD (V), E0 (MV/CM), XEPI (UM), PTS DP'

VDD = PAR[1]
VDSTP = PAR[2]
VDM = PAR[3]
DVD = PAR[4]
A = PAR[5]
EO = 1000000*PAR[6]
XEPI = PAR[7]
NP = PAR[8]

IM = 1:*{PAR[3]-PAR[1]}-PAR[2]

'ENTER DESTINATION FILE FOR MAIN ARRAY, 3 LETTERS, NO EXTENSION'

FILE :

'ENTER DESTINATION FILE FOR M1 ARRAYS, 1 LETTER, NO EXTENSION'

EXAMPLE: A:X.

MORE CHARACTERS WILL BE APPENDED.'

M1FILE :

AV INITIALIZ

THIS FUNCTION Initializes AND SETS UP VARIOUS VARIABLES
LOCAL TO THE FUNCTION AVALANCHE

L = 1; 0

F = 1
G = 2;0

VB = 23080000000000; ND = 0.72414

VD = VDD+F; VDSTP

KD = 100; ND = ND

KD = DNO; NOG = K

KM = 200; NSTEP = ND

DNS = NSTEP KM

FI: FILE, ('00':ND 1E14), ('00':VD), '.DAT'

EMIN IN V/CM

EMIN = -(3.2E 19·NA ND; VD 8.85E 14·11.7·NA+ND)· 2

XP AND XN IN MICRONS. XP < 0. ORIGIN AT X3

XP = 10000·8.85E 14·11.7·EMIN 1.6E 19·NA

XN = XP·NA ND

DXP = -XP·NP

NN = 1+5·NP

DXN = XEPI - NN - 1

M = M1 (((NP+NN), 7); 0
AV DEP*APPROX[1]:

[0] AV DEP*APPROX
[1] THIS FUNCTION ITERATES ON XP TO SOLVE FOR THE CHARGE DENSITY.
[2] ELECTRIC FIELD DISTRIBUTION, POTENTIAL GRADIENT, IONIZATION RATE,
[3] ELECTRON CONCENTRATION, AND HOLE CONCENTRATION USING THE DEPLETION
[4] APPROXIMATION.
[5]
[6]
[7] X VECTOR (FIRST COLUMN)
[8]

[9] M[NP+1;1]=-DXP*:1+NP--NP+1
[11] 
[12] CHARGE DENSITY (SECOND COLUMN)

[15]

[16] ELECTRIC FIELD (THIRD COLUMN)
[17] M[1+NP+NN-1;3]=(M[·NP+NN-1;2]+M[1+·NP+NN-1;2])/2X11.7X8.85E-14
[18] M[1;3]=0
[19] DX*:0.0001*((NP+1)*DXP),(NN-1)*DXN)

[22]

[23] POTENTIAL GRADIENT (FOURTH COLUMN)

[27]

[28] ITERATE XP: CHECK IF \VD\ (VD-\POTENTIAL)
[29] L2\VD\=VD+/M[;4]
[30] XP=XP+10000*ND (VD*/M[;4]) EMINS NA+ND
[31] XN=XN-XP=ND
[32] DXP=XP=NP
[33] M*((NP+NN),7)=0
[34] X1

[35]

[36] L2:

[37] IONIZATION RATE (FIFTH COLUMN)
[38] M[;5]= EO M[;3]=1
[39]
[40] ELECTRON CONCENTRATION (SIXTH COLUMN)
[41] ETA0=-EO EMINS
[42] PAR (-PPAR=/PAR), PAR
[43] PAR (+/PAR=O),PAR
[44] ETA ETA0 XF-XP=M[PAR;1]

[46] M[PAR;6]=-A*XP(·-ETA) 1.5+ETA
[47] M[;6]=0
[48] PAR (+/PAR=O),PAR
[49] PAR (+/PAR=O),PAR
[50] ZETA=ETA0*XP*XN=M[PAR;1]
[51] M[PAR;6]=MN*AP(XN-M[PAR;1]) (·-ZETA) 1.5+ZETA

[53] XN=M[1;10]*M[;6]=0
[55]
[56] HOLE CONCENTRATION (SEVENTH COLUMN)
[58]
[59] COPY X VECTOR AND DENORMALIZED ELECTRON & HOLE CONCENTRATIONS TO M1
[60] M[;1]=M[;1]
\[ \text{AV\-START\-UP}[\text{FILE};\text{TFILE};\text{TND};\text{TVD};\text{SIZE}] \]

1. This function loads the array \( M_1 \) with the contents of the user specified data file.

2. Requirements:
   - 1. The functions \text{AV\-INPUT} and \text{AV\-INITIALIZ} must be run prior to execution.
   - 2. The data filename is assumed to be of the form: \text{AXXYZZZ.DAT} where \( A \) is any letter from A-Z, \( XX = 1E14 \), \( YY = 1D10 \), and \( ZZ = 1E13 \).

3. Get data filename from user
   - 'Enter data filename to be loaded for initial conditions:'
   - 'Is no. 1E16? (Y or N)'
   - Size:

4. Make sure filename corresponds with other parameters
   - \text{TFILE} = \text{FILE}
   - \text{TND} = 1E14
   - \text{TVD} = 10
   - \text{TFILE} = \text{FILE}
   - \text{TND} = 1E15
   - \text{TVD} = 10

5. If filename does not match \( ^{;} \)
   - 'The filename entered does not match with parameters!'
   - ' '
   - \text{LO}
   - \text{LO}

6. Load array \( M_1 \) with contents of file
40)  AV \text{READ}
41) n
42) H UPDATE XP, NP, NN, DNO, NC, DN, K, KT, AND L
43) XP=ML[1;1]
44) NP=ML[1;1]<0
45) NN=ML[1;1]:0
46) S1\times\times\times\times\times\times\times:1=NP/0
47) NP=1
48) NN=NN-1
49) S1:
50) DNO, DNS
51) L4:\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\times\time
AV WRITE[0]

[0] AV WRITE; M1; M1; M1; M1; M1; M1; M1; REC; M1; N; M2; N

[1] " THIS FUNCTION SAVES THE M1 ARRAY ON THE DISK AS WELL
[2] AS WELL AS ADDING THE RECORD CONTAINING N(XP), N(XN),

[4] '

[5] " PREPARE FILENAME FOR M1 ARRAY AND OPEN
[6] " M1FILE=("0""ND", "1E14"), ("0""VD", "10"), ("000""W"", "NO", "10000000000000"), ".

[7] " L1:

[8] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[9] " L1:

[10] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[11] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[12] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[13] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[14] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[15] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[16] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[17] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[18] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[19] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[20] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[21] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[22] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[23] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[24] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[25] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[26] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[27] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[28] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[29] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[30] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[31] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[32] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[33] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[34] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[35] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[36] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[37] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[38] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[39] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

[40] " M1FILE, ("0""ND", "1E15"), ("000""W"", "NO", "10000000000000"), ".

AV WRITE[0]

[0] AV STEP; M1; M1; M1; M1; M1; M1; M1; REC; M1; N

[1] " THIS FUNCTION STEPS NO(XP), AND ADJUSTS K, ANO, KT, AND L

[2] K; KM

[3] DNO; DNS

[4] NO; NO+DNO

[5] KT; KT/(KD+VBD) (NO-0.8"ND")-ND

[6] L; L+1

[7] " AV STEP; M1; M1; M1; M1; M1; M1; M1; REC; M1; N

[8] " THIS FUNCTION STEPS NO(XP), AND ADJUSTS K, ANO, KT, AND L

[9] K; KM

[10] DNO; DNS

[11] NO; NO+DNO

[12] KT; KT/(KD+VBD) (NO-0.8"ND")-ND

[13] L; L+1
AV CHK CROSS:

AV CHK CROSS

THIS FUNCTION CHECKS TO SEE IF THE VALUE FOR XP HAS CROSSED
OVER THE METALLURGICAL JUNCTION, XJ. IN THE PROCESS, A DATA
POINT MAY BE SHIFTED FROM THE P-SIDE TO THE N-SIDE IF NECESSARY.

CHECK IF XP>0

L3: \( (XP>0) \)

L1:

CHECK IF XP=XPMIN

L2: \((\text{-XP})-(\text{NP} \cdot \text{DXPMIN}) \)

CHECK IF NP=1

L3: \((\text{NP}=1) \)

SHIFT DATA POINT FROM P-SIDE TO N-SIDE

NP: NP-1

NN: NN+1

L1

L2:

UPDATE VARIABLES FOR XP=0 AND NP>1

DXP'=-XP\cdot NP

DXN':XEPI\cdot (NN-1)

M[\text{NP+1};1,1]'=\text{DXP}+\text{NP}-\text{NP+1}

M[\text{NP}+1;\text{NN}-1;1]'=\text{DXN} \cdot \text{NN}-1

DXP:0.0001\cdot((\text{NP}+1) \cdot \text{DXP})\cdot((\text{NN}-1) \cdot \text{DXN})

M[;2]'(\text{NP}=(-1.6E'19' \text{NA})),(\text{NN}=1.6E'19' \text{ND}))

L5

L3:

UPDATE VARIABLES FOR NP=1, XP=0, OR XP>0

DXP:DXMIN

DXN'(XEPI'=(XP+DXPMIN))\cdot (NN-1)

M[\text{NP}+1;1]'=\text{XP}+\text{DXP} \cdot ((\text{NP}+1)-1)

M[\text{NP}+1;\text{NN}-1;1]'=M[\text{NP}+1;1]'+\text{DXN} \cdot ((\text{NN}-1) \cdot \text{DXN})

L4: \((XP=0) \)

M[;2]'(\text{NP}=(-1.6E'19' \text{NA})),(\text{NN}=1.6E'19' \text{ND}))

L5

L4:

M[;2]'(\text{NN}+1) \cdot 1.6E'19' \text{ND}

L5:

M[; \text{NN}+\text{NP};6 7]' M[; \text{NN}+\text{NP};6 7]

L5:
AV-CALC[2]:

1. AV-CALC
2. THIS FUNCTION CALCULATES THE CHARGE DENSITY, ELECTRIC FIELD,
3. POTENTIAL GRADIENT, IONIZATION RATE, ELECTRON CONCENTRATION,
5. 
6. L1:
7. CHARGE DENSITY (SECOND COLUMN)
8. \[ M_1[n,1] = m[n,1] + 1.65 \times 10^{-19} M_1[n,7] - M_1[n,6] \]
9. 
10. ELECTRIC FIELD (THIRD COLUMN)
11. \[ M_1[n,2] = \frac{(M_1[n,1] + M_1[n,2]) + 11.7 \times 8.85 \times 10^{-14}}{2} \]
12. 
13. POTENTIAL GRADIENT (FOURTH COLUMN)
14. \[ M_1[n,3] = \frac{\text{DX} \times M_1[n,3]}{M_1[n,3] \times M_1[n,3]} \]
15. 
16. IONIZATION RATE (FIFTH COLUMN)
17. \[ M_1[n,4] = A - \text{BE} \times M_1[n,4] \]
18. 
19. ELECTRON CONCENTRATION (SIXTH COLUMN)
20. \[ M_1[n,5] = 0.5 \times \left( M_1[n+NP,1] + M_1[n+NP,5] \right) \]
21. \[ M_1[n,6] = 10000 \times \text{DX} \times M_1[n,6] \]
22. 
23. HOLE CONCENTRATION (SEVENTH COLUMN)
24. \[ M_1[n,7] = \left( \frac{M_1[n,4]}{M_1[n,6]} \right) - M_1[n,6] \]
25. 
26. ITERATE CHARGE DENSITY
27. \[ L1: (O \times K) \times (-K \times K < 0) \]
28. \[ K = K + (K+1) \times (K = -K+1) \]

\[ \text{AV-READ[3]}' \]

AV-READ; IM; I; RECORD
1. IM: (+M)[1]
2. L11 OPEN FILE, ' D'
3. I ' 0
4. M1 '((NN+NP),7)' = 0
5. LO:
6. RECORD L11, I, 70
7. M1[n+1,3] = READ RECORD
8. I' = I + 1
9. :L0 ' I < IM
10. CLOSE L11
REFERENCES


33. Sze, p. 149.

34. Sze, p. 50.


47. J.R. Brews, University of Arizona, private communication.


