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Evaluation of $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ p-channel HIGFETs for complementary technologies

Martinez, Marino Juan, Ph.D.

The University of Arizona, 1993

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EVALUATION OF $GaAs_XSb_{1-X}/In_YAl_{1-Y}As$ P-CHANNEL HIGFETs FOR COMPLEMENTARY TECHNOLOGIES

by

Marino Juan Martinez

A Dissertation Submitted to the Faculty of the

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As members of the Final Examination Committee, we certify that we have read the dissertation prepared by Marino Juan Martinez

entitled Evaluation of $GaAs_xSb_{1-x}/In_yAl_{1-y}$ P-Channel HIGFETs for Complementary Technologies

and recommend that it be accepted as fulfilling the dissertation requirement for the Degree of Doctor of Philosophy

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Fritz L. Schuermeyer		Nov. 15, 1993 Date
Ronald D. Schrimpf		Nov. 15, 1993 Date
		Date
		Date

Final approval and acceptance of this dissertation is contingent upon the candidate's submission of the final copy of the dissertation to the Graduate College.

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Kenneth F. Galloway
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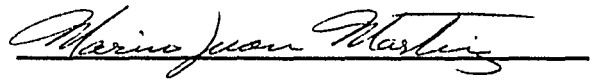
SIGNED: 

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ABSTRACT

This work shows the viability of p-channel $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ HIGFETs for III-V compound-based complementary technologies to compete with silicon CMOS for specialized applications. Monte Carlo simulation was used to establish that even for the most extreme cases of alloy scattering $GaAs_xSb_{1-x}$ on InP has a higher bulk hole mobility than GaAs. Process development demonstrated that H_2O:H_2O_2:H_3PO_4:L-tartaric acid-based etchant solutions provide a reliable etchant with a selectivity of approximately 2:1 of $GaAs_xSb_{1-x}$ over $In_yAl_{1-y}As$. Process development also showed that Ti/Au was the most reliable gate metal for contact to $In_yAl_{1-y}As$ and that care must be taken to avoid letting some common chemical solutions come into contact with $GaAs_xSb_{1-x}$. Experimental devices established that lattice-matched $GaAs_xSb_{1-x}$ channel layers had low gate leakage currents, but had otherwise poor performance. However, experimental devices with strained GaSb-rich $GaAs_xSb_{1-x}$ channels had the lowest recorded gate leakage current for a heterostructure FET yielding a gate turn-on voltage of –3 V and also had transconductance and current drive comparable to the best p-channel HIGFETs of any material systems to date. Finally, SPICE simulations showed that if integrated with n-channel HIGFETs with comparable gate leakage and moderate performance, modestly improved p-channel devices make possible technology with approximately half the delay time of similar CMOS circuits. Although silicon CMOS has enormous advantages over complementary HFETs in terms of robustness and yield which allow very high densities of integration, this work clearly establishes that this infant technology has the capability to challenge the more established CMOS on the basis of speed and power consumption.

1: INTRODUCTION

1.1: MOTIVATION

In recent years, there has been a virtual explosion in the use of silicon–based complementary metal-oxide-semiconductor (CMOS) with applications ranging from wristwatches to application specific integrated circuits (ASICs) for satellite systems. At first, interest in CMOS technology was due to its well-documented properties allowing low static power dissipation. However, it is now recognized that although a logic gate fabricated in CMOS technology can not compete, in terms of sheer speed, with a gate fabricated using bipolar junction transistor (BJT) technology, the low static power dissipation and high noise margin of CMOS gates greatly facilitates the achievement of high levels of integration and high production yields through a high tolerance to processing variations. The benefits of such high density integration include the reduction of chip-to-chip delays and power consumption of output drivers as well as the more obvious savings in weight, volume, and board footprint. These factors combine to produce clock rates and system speeds similar to those of bipolar technologies.

The outstanding performance and costs benefits achieved in silicon-based CMOS have driven interest in complementary heterostructure field effect transistors (HFETs) in recent years. The basic premise behind this interest is to combine the benefits of complementary technology with some of the superior materials properties of compounds from group III and group V of the periodic table of elements (hereafter referred to as III-V compounds) compared to those of silicon. Simulations performed by Kiehl et. al. indicate that complementary heterostructure FET (HFET) technology has the potential of yielding power-delay products 1/8 of those achievable by silicon-CMOS technology [1]. (Such calculations may now be considered conservative in nature since they did not include the performance advantages that heterostructure insulated-gate field-effect transistors (HIGFETs) provide.) Because of the relative cost and difficulty in fabricating complementary HFET technology, the HIGFET technology under study is intended for use in systems where high speed, low power,

and high density integration are at an absolute premium. Examples of such systems are "supercomputers," real-time digital signal processors, and "flash" analog-to-digital converters.

For III-V compounds to be used in implementing a complementary technology, the most desirable properties must be optimized while keeping fabrication as simple as possible. It will be demonstrated in Section 1.2 that, to a first-order, the three most important attributes for devices to be used for complementary digital logic are low gate-leakage current, high transconductance, and high drain current. These requirements drive the selection of a device technology. Of all the available technologies for III-V compound devices, it will be shown that the optimum balance of performance characteristics is achieved by choosing heterostructure insulated gate field effect transistor (HIGFET) technology.

An additional requirement for any complementary technology is that the devices in which charge is transported by holes (p-channel or p-type) and the devices in which charge is transported by electrons (n-channel or n-type) devices must have similar performance, so that they may be combined. While HIGFET technology holds much promise, this objective is not as easily achieved as when using silicon-based technologies. The properties of p- and n-channel silicon MOSFETs are similar enough that they may be combined complementarily by simply using different device sizes (lower mobility of holes dictates that the p-channel devices must be larger) to provide nearly equivalent performance. However, in typical III-V semiconductor compounds there is a vast difference (orders of magnitude) between the mobilities of holes and electrons, with holes having the lower mobility. Since it would be quite impractical to try to make up the difference in mobilities through sizing, the p-channel device performance becomes the most critical part of the problem. That is, it is much more difficult to optimize p-channel devices using III-V compounds than it is to optimize n-channel devices. This is evidenced by the fact that the p-channel devices are the speed-limiting component of present complementary III-V technologies. Nonetheless, it is possible to implement various levels of complementarity, depending on how closely matched the n- and p-channel devices

are.

It will be shown that known materials properties indicate that the best results will be attained by using the compound gallium antimonide (GaSb) for p-channel devices. Accordingly, the focus of this study was p-channel HIGFETs for use in a complementary logic technology and study of the component materials to facilitate the understanding of finished device performance.

1.2: HIGFET TECHNOLOGY ADVANTAGES

Before choosing a logic technology for development, it is necessary to project the performance attributes which are most valuable. An ideal logic gate (e.g., an inverter) would have negligible static input current, very fast switching characteristics, a large logic swing, and large noise margins. Figure 1.1 shows some of these characteristics on a generic voltage transfer curve (VTC). All these requirements reduce to just a few basic device requirements which are detailed below. Other, secondary, requirements such as controllability of threshold voltage and the ability to fabricate good ohmic contacts are neglected in this initial analysis.

If the devices of the candidate technology have insignificant gate currents, they will yield negligible input current resulting in negligible static power dissipation. This also allows a larger logic swing if the devices are directly coupled; a high output connected directly to the gate of another device will not cause that gate to draw significant current. Low gate-leakage also allows the achievement of high noise margins. If the logic transition is halfway between the high output voltage and low input voltage, the larger logic swing of an insulating gate necessarily results in larger noise margins. Such requirements are easily met using silicon MOSFETs, since an insulator separates

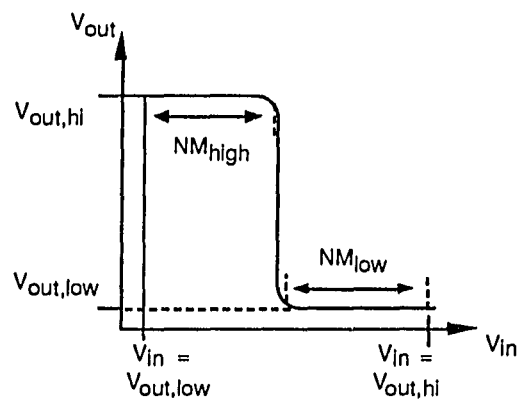

Figure 1.1: Generic voltage transfer curve (VTC).

the gate from the conducting channel. The inability to grow a stable native oxide on III-V compounds and the difficulty in depositing a high-quality insulator that would result in suitable threshold voltages effectively eliminates this option. Therefore, one must look for approaches which minimize gate-leakage-current at relatively high voltages (several volts) without the benefit of a true insulating layer.

It is clear, then, that one of the most important characteristics of any field effect device technology for use as logic is low gate-leakage current. The gate-leakage-current of a technology is often characterized by a gate turn-on voltage, $V_{g(on)}$, which is defined as the gate-to-source voltage at which the gate draws a specific amount of current (e.g., 1 mA). A device with a high turn-on voltage will, in general, have a more insulating gate. The turn-on voltage should not be confused with the threshold voltage, V_t, which defines a gate-to-source voltage at which the conducting channel is fully formed.

The only desired characteristic that is not directly achieved by having an insulating gate is that of high switching speed. In general, switching speed is increased by reducing parasitic capacitances and resistances to reduce time constants associated with capacitive charging, increasing drain current to charge capacitances more quickly, and increasing transconductance, g_m, to, in effect, amplify the gate voltage. Transconductance (units of Siemens (S)) is usually defined by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} . \tag{1.1}$$

Therefore, if parasitics are assumed to be minimized, transconductance and drain current must both be maximized to minimize switching time.

To a first order, then, the technology to be used should ideally have low gate-leakage current, high drain current, and high transconductance. This provides a basis for comparing candidate technologies available using III-V compounds. At present, these technologies fall into four basic categories: junction field effect transistors (JFETs), metal-semiconductor field effect transistors

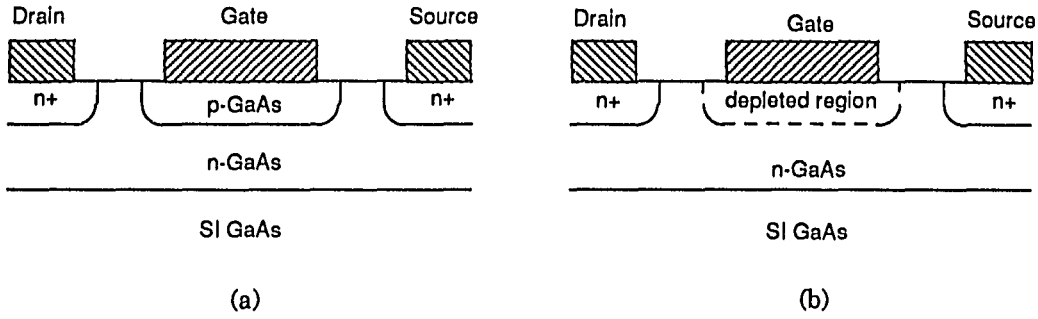

Figure 1.2: a) JFET structure and b) MESFET structure.

(MESFETs), modulation-doped field effect transistors (MODFETs) (this type of device is also known as the two-dimensional electron gas FET (TEGFET), the selectively doped heterojunction transistor (SDHT), and the high electron mobility transistor (HEMT)), and heterostructure insulated gate field effect transistors (HIGFETs). (Heterojunction bipolar transistors (HBTs) are not included as they are primarily an analog technology for much the same reasons BJTs are used mostly for analog applications in silicon-based microelectronics.)

The most mature of these technologies are the JFET and the MESFET. Both technologies operate under the same basic principle: a depleted area controlled by the gate bias modulates the resistivity between the source and drain by changing the depth of the depleted region to alter the size of the conducting channel. The principal difference between JFETs and MESFETs is the method by which the depleted area is produced. For a JFET, it is the depletion region of a p-n junction; for a MESFET, it is the depletion region of a metal-semiconductor, Schottky contact. Although both technologies are quite mature when compared to MODFETs and HIGFETs, they are not as suitable for use in high-density complementary circuits. The basic structures of JFETs and MESFETs are shown in Figure 1.2.

JFETs and MESFETs have two principle weaknesses: low transconductance and high gate-leakage current. The maximum transconductance (normalized for gate width) of these FETs is

limited to about 150 mS/mm for n-channel devices and about 5 mS/mm for p-channel devices. This transconductance is primarily limited by gate-leakage current (which reduces the drain current at high gate bias voltages) and by the relatively low mobility of carriers in the doped channel region. Since transconductance generally increases with increasing gate bias [1] (for $V_g <$ maximum forward gate voltage, $V_{g,on}$), g_m is also limited by the relatively low values of usable gate bias. It is instructive to note that the transconductance of the p-channel device is very limiting compared to that of n-channel devices; this is true in general.

The gate-leakage currents are high chiefly because of the small potential barrier between the gate metal and the channel. As mentioned above, the JFET utilizes a junction barrier and the MESFET a Schottky barrier. Because both structures must have the junctions forward biased when turned "on" (for either p- or n-type devices), the gate voltage is limited to about 0.8 V before significant current begins to flow ($V_{g,on}$ =0.8 V). Even if the entire 0.8 V could be used for logic swing (not usually the case), the noise margins would only be about 0.4 V each. Such small noise margins would require very tight control of processing, and would likely result in very low functional yields. In addition, simulation of advanced (gallium arsenide) complementary circuits by Kiehl et. al. shows that a supply voltage, or logic swing, of at least 2 V is necessary to realize the full potential of such circuits [2]. It is apparent, then, that JFETs and MESFETs are not suitable choices for high-speed complementary integration.

The higher speed and transconductances achieved by MODFETs and HIGFETs make them more attractive for high-speed complementary integration. It will be shown that, when examined more closely, HIGFETs exhibit a clearly superior potential for such integration over MODFETs.

First, let us examine the theory and operation of the MODFET by putting it in historical context. The MODFET belongs to a class of devices that are known as heterojunction devices which derive their name from the fact that part of the active structure includes a junction of two different materials such as gallium arsenide (GaAs) and the alloy of aluminum arsenide (AlAs) and GaAs,

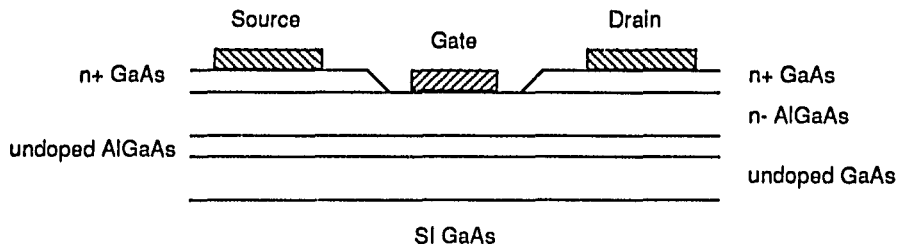

Figure 1.3: Typical recessed-gate MODFET structure.

$Al_xGa_{1-x}As$. The first such device was proposed by Schockley in 1951 [2]; Gubanov developed a theory for heterojunctions in the same year [3, 4]. R.A. Anderson predicted accumulation layers at heterojunction interfaces in 1960 [5] and R.L. Anderson proposed a simple model for heterojunctions in the same year which is still the core of many contemporary models [6]. In 1969, Esaki and Tsu were the first to predict that a two-dimensional electron gas at a hetero-interface should have enhanced mobility [7], but this effect was not actually observed until 1978 by Dingle et. al. [8]. In 1980, Mimura et. al. fabricated the first MODFET [9]. Workers have continued to improve the size and performance of these devices, and this remains an active area of research. A typical MODFET structure is shown in Figure 1.3.

The higher performance of MODFETs is based on two basic principles: a heterojunction can create a quantum well, and ionized impurities are a significant carrier scattering mechanism over a large temperature range. A quantum well for electrons and/or holes results when two materials with different bandgaps are joined in an abrupt heterojunction. If we define the electron affinity, X, of a material as the energy needed to elevate an electron at the bottom of the conduction band to vacuum, then the conduction band discontinuity of a heterojunction of materials 1 and 2 is defined as

$$\Delta E_c = X_1 - X_2 . \tag{1.2}$$

Since the fermi level must be continuous and constant at equilibrium, a quantum well forms at the hetero-interface as the band edges bend to make the level continuous. (An example of an electron

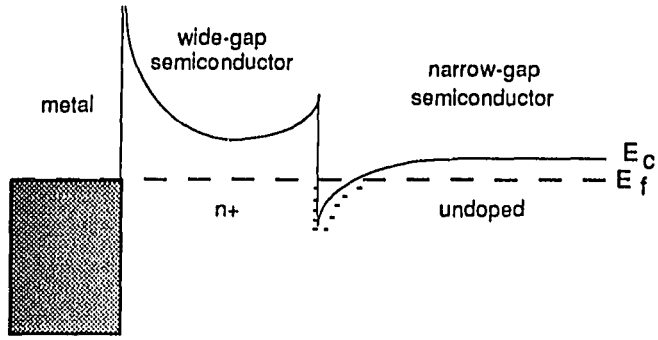

Figure 1.4: Electron quantum well for a MODFET.

quantum well is shown in Figure 1.4.) A quantum well will form on the side of the material with the lower band energy, but whether the well is for holes or electrons depends on the doping of the materials and the relative energies of the valence and conduction band edges of the respective materials.

In the p^--GaAs/n^+-$Al_xGa_{1-x}As$ system, an electron quantum well forms on the GaAs side of the interface. The presence of this quantum well causes the electrons from the donors in the $Al_xGa_{1-x}As$ to move into the well, away from the donor atoms. The shape of the well and the Coulombic attraction to their donor atoms results in the electrons staying very close to the interface in what is referred to as a two-dimensional electron gas (2DEG). To reduce the proximity of the donor atoms to the 2DEG, a thin (typically 60 nm) undoped AlGaAs spacer layer is grown between the n^+-$Al_xGa_{1-x}As$ and the p^--GaAs; this reduces the remote scattering of carriers by the donor atoms. (The density of electrons in the 2DEG is determined by the shape of the well and the position of the fermi level. The energies of electrons within the well are quantized and typical densities are in the 10^{11}-10^{12} cm^{-2} range.)

The net result of such a structure, then, is that charge carriers experience only remote scattering by their associated donor atoms. This increases the mobility of the carriers compared to those in devices with doped channels. The magnitude of improvement in carrier velocities can be significant.

This improvement increases transconductance and drain current, if logic swing and threshold voltages are the same, over those for MESFETs and JFETs. Although MODFETs meet two of our requirements for an appropriate device technology, they fall well short of meeting the requirement for low gate current.

The doping of the barrier layer ($Al_xGa_{1-x}As$) to provide the charge carriers has the additional effect of lowering the barrier for charges between the gate and the channel. This, then, effectively limits the barrier height to the Schottky barrier height (as for MESFETs and JFETs), with an expected increase in gate current. Since low gate current is the single most important parameter for a candidate technology, we must find a more suitable candidate.

To meet this requirement while retaining some of the advantages of MODFETs, we look to the HIGFET, which provides a tradeoff of carrier mobility and gate current. The HIGFET was first proposed in 1983 by Drummond et. al. [10] and has received a great deal of attention since. Work continues on optimizing HIGFETs using the GaAs/$Al_xGa_{1-x}As$ system and investigating alternative materials including alloys of indium arsenide (InAs), GaAs, aluminum antimonide (AlSb), and indium antimonide (InSb) such as $In_xGa_{1-x}As$, $Al_xGa_{1-x}Sb$, $In_{1-x}Al_xSb$, $GaAs_{1-x}Sb_x$, and GaSb.

The HIGFET structure is very similar to that of the MODFET. The chief difference being that the channel, rather than the barrier, is doped in the HIGFET. An example of a HIGFET structure is shown in Figure 1.5. For an n-doped channel layer, the HIGFET structure also provides an electron quantum well where a 2DEG forms. These electrons, however, are subject to direct and remote scattering by their ionized donor atoms. The major advantage of the HIGFET over the other candidate technologies is that it features an undoped, semi-insulating layer between the gate and channel (hence the name). This simple feature results in a barrier potential approximately equal to the Schottky barrier plus the band-edge discontinuity (conduction band for n-channels) at the barrier-channel interface. Workers using such structures have achieved gate turn-on voltages in excess of 3 V [11]. Furthermore, while this structure does exhibit reduced carrier mobility compared

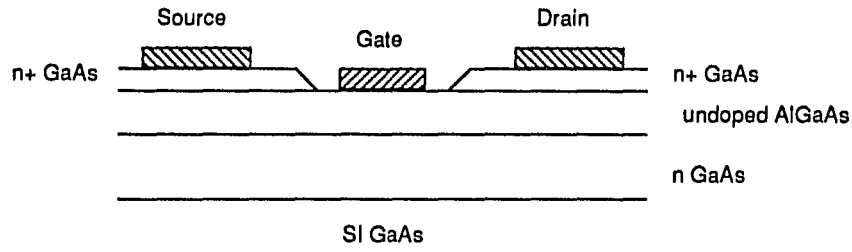

Figure 1.5: Typical recessed-gate HIGFET structure. The undoped AlGaAs layer is a semi-insulating barrier.

to a MODFET structure, it has been shown by Yokoyama that the density of carriers in the 2DEG provides a charge-screening effect that mitigates the effect of the proximity of the donor atoms to the 2DEG [12].

Perhaps even more important than this attribute alone is that this dramatic increase in turn-on voltage may be achieved without paying a large penalty in transconductance or drain current. Indeed, as was explained above, the low gate currents of HIGFETs facilitate the task of achieving satisfactory values for both of these parameters. It is apparent, then, that HIGFET technology is the best candidate for a III-V complementary device technology since it provides the best trade-off between gate current, drain current, and transconductance. The next step is to develop and test devices in the most promising materials systems.

1.3: THE PROMISE OF $GaAs_xSb_{1-x}$ FOR p-HIGFETs

While a complementary technology in final form must, by definition, optimize both n- and p-channel devices, the flexibility of using heterostructures grown by molecular beam epitaxy (MBE) allows us to consider them separately. Because the p-channel devices are the most limiting, for reasons explained above, we shall concentrate primarily on this aspect while still considering the compatibility with candidate n-channel devices.

There are four basic materials choices to be made with respect to HIGFET design. These choices are the channel material, semi-insulator material, Schottky metal, and the ohmic contact metal(s). In order to make these choices properly, it is instructive to examine the operation of an idealized, generic HIGFET more closely. At the most basic level, any field effect transistor is a voltage-controlled resistor. That is, the carriers for drain-to-source conduction are modulated by the voltage applied to the gate which changes the potential of the material in the channel region. The FET appears to be high value resistor when the gate potential keeps carriers out of the channel region and a low value resistor when the gate allows the accumulation of carriers (MOSFET, MODFET, and HIGFET) or permits their presence in the channel (JFET and MESFET).

In the case of the HIGFET, we choose to modulate the channel through a Schottky contact to the semi-insulating side of a heterojunction. The manner in which the modulation occurs in HIGFETs (and MODFETs) is somewhat different from that of other FETs. First, recall that a Schottky barrier has an associated depletion region that extends for some distance, determined by the voltage, from the junction. Second, recall that the energy states in a quantum well are quantized and the occupancy of the states is determined by the Fermi level in the well. Assume also that there are just enough carriers available to fill the available states of the well. Then, as the gate is given a stronger reverse (forward) bias, the depletion region extends to greater (lesser) depth towards the channel and the bands are bent in and around the depletion region, lowering (raising) the fermi level

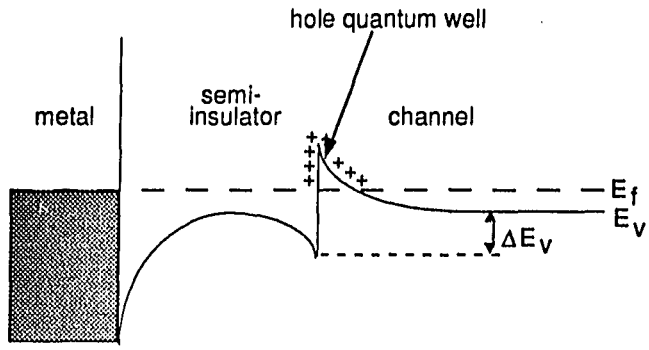

Figure 1.6: Valence band edge discontinuity as a barrier for holes in a quantum well.

with respect to the well bottom. Therefore, the gate bias modulates the fermi level in the quantum well which modulates the 2DEG or 2-D hole gas (2DHG) carrier density.

Examining a band diagram such as Figure 1.6, the number of states available in the well is determined by the width (physical) and the depth (in energy) of the well, with more states in wider and deeper wells. While the width of the well does not change much with different materials, the depth of the well is equal to the band edge discontinuity between the channel and insulator materials. A large discontinuity also increases the barrier between the gate metal and the channel for carriers as shown in Figure 1.6. Therefore, choosing materials with a large band edge discontinuity increases the sheet charge in the 2DEG or 2DHG and decreases the gate current.

Another consideration for any logic device is the velocity of the carriers in the conducting channel; a large number of carriers is of little value if they move too slowly. Below saturation, both drain current and transconductance are directly proportional to the mobility or velocity of the carriers. The best choice for a channel material, then, provides both a large band edge discontinuity with the insulator and a high carrier velocity. (In general, materials with high hole mobilities have lower valence band edge energies than any semi-insulating material that may be used (e.g., AlAs), so the material selections may be optimized separately.) All this implicitly assumes that the material can be grown as a defect-free single crystal.

Scanning a table of properties of semiconductor materials quickly points out which are likely candidates. Many materials such as GaAs and indium phosphide (InP) can be quickly eliminated due to relatively low hole mobilities, and others such as InSb have lattice constants which preclude the growth of reasonably thick layers (greater than 0.5 μm) free of defects on available substrates suitable for device fabrication (chiefly silicon, GaAs, and InP). Still others such as lead sellenide (PbSe) and lead telluride (PbTe) are not the proper crystal type for epitaxial growth. When all these are eliminated, two candidates emerge: germanium (Ge) and GaSb.

From the perspective of materials properties alone, Ge grown on GaAs appears to hold the most promise since it has the highest hole mobility and its valence band edge is at a slightly higher energy than that of GaSb. This promise quickly evaporates, however, when one considers that Ge is a persistent contaminant and doping impurity in semiconductor growth systems and one must go to such extremes as dual-chambered MBE systems to confine the contamination. While it is possible that a metal-organic chemical vapor deposition (MOCVD) system that is cleaned thoroughly and frequently could be used, Ge growth on GaAs is a very difficult and risky proposition at present [13].

This leaves GaSb as the most likely candidate. While GaSb growth does not present the same difficulties as Ge growth, it is not without problems of its own. First and foremost of these is the mismatch in lattice constants between GaSb and InP (the closest matching substrate). This problem can be mitigated by growing instead an alloy of GaAs and GaSb which would provide lattice matching. This would also have the effect of changing the properties of the $GaAs_xSb_{1-x}$ to a weighted average of the properties of GaAs and GaSb which would depend on the fractions of each in the alloy [14]. While this would lessen the benefits of using GaSb, it is a necessary compromise if a defect-free material is desired. Nevertheless, MBE growth of $GaAs_xSb_{1-x}$ is not a trivial matter as composition must be tightly controlled if a defect-free layer of more than a few angstroms thickness are to be grown, and little work has been done in this area.

The second choice to be made is that of Schottky contact metal. Schottky contacts require that

the surface to which the metal makes contact not have a high level of doping so that tunneling current is not significant. Aluminum is typically the metal of choice for p-type Schottky contacts to many III-V compounds (gold may be used as well), but its low melting point make it unsuitable when further high temperature processing is necessary. In these cases, tungsten is an appropriate choice. Therefore, aluminum or gold will be used when feasible, and tungsten will be used when a refractory metal is required.

In contrast to the gate contact, a non-rectifying, or ohmic, contact is desired at the source and drain contacts. A non-ideal ohmic contact increases loss in the device, lowering g_m and drain current. Ohmic contacts are achieved by highly doping the surface at the contact interface and using a metal or metals which will provide further doping at the surface. With this heavy doping, the surface becomes degenerately doped and the majority carriers can easily tunnel through the Schottky barrier. The standard practice for fabricating ohmic contacts on III-V compounds is to deposit a combination of metals, one of which is a fast-diffusing dopant and then alloy the contact so that the dopant is incorporated into the semiconductor [15]. The dominant choice for p-type ohmic contacts in III-V devices is an alloyed gold/zinc/gold (Au/Zn/Au) deposition where zinc is the dopant. Relatively low contact resistances (explained in a later section) are routinely achieved using this method, so we choose to use it as well.

The final material selection to be made is that of the insulator. Except for current flowing between the ohmic contacts and the channel, the insulating material is not a part of the desired current path (the high doping of the insulator during the alloying process allows carriers to easily tunnel through it in the contact regions). Therefore, the material selection is based on two considerations, large band-edge discontinuity for carrier confinement in the quantum well and ability to grow it as a high-quality insulating layer on top of the channel material. Studies of band-edge considerations indicate that the best candidates are $In_xAl_{1-x}As$ and $Al_xAs_{1-x}Sb$ [16]. Of these two, $In_xAl_{1-x}As$ is easier to grow and is more stable ($Al_xAs_{1-x}Sb$ readily disintegrates when exposed

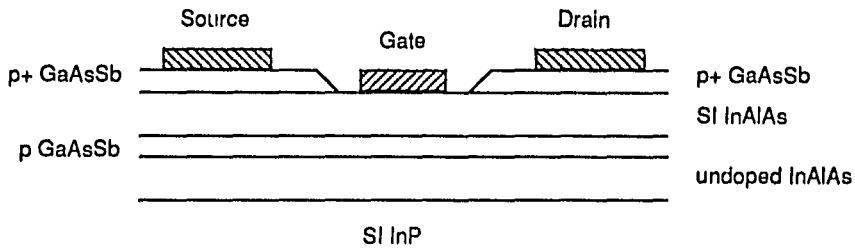

Figure 1.7: Typical recessed-gate p-HIGFET structure. InAlAs is barrier layer.

to air) [13].

When all these selections are put together, a candidate structure emerges which uses the optimum materials based on the best *known* materials parameters. This consists of an aluminum, gold, or tungsten gate on a $In_xAl_{1-x}As$ semi-insulator on a doped $GaAs_ySb_{1-y}$ channel with Au/Zn/Au ohmic contacts. This structure, however, must be grown on some kind of substrate. For growth of quality epitaxial layers, a thick buffer layer is grown first to isolate the active area from the defects surrounding the substrate surface. For isolation purposes, the same material as the gate insulator ($In_xAl_{1-x}As$) is chosen for this layer. The substrate itself is chosen to maximize the mole fraction of GaSb in the channel layer for highest hole mobility. An inspection of the pertinent lattice constants reveals that InP, which is available in semi-insulating form, has the closest lattice constant to GaSb. (A further motivation for choosing this substrate is that some of the best n-channel devices use $In_xGa_{1-x}As$ channels on InP substrates.) A schematic of a recessed-gate, lattice-matched p-HIGFET is shown in Figure 1.7.

The remaining chapters will detail the evaluation of p-channel $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ HIGFETs. Chapter 2 will discuss simulation of bulk hole transport in $GaAs_xSb_{1-x}$ using Monte Carlo techniques to estimate hole mobility and measurement of the valence band-edge discontinuity between $GaAs_xSb_{1-x}$ and $In_yAl_{1-y}As$. Chapter 3 will detail the process development necessary for fabricating devices using these materials. Chapter 4 will cover experimental results for p-channel

HIGFETs, Chapter 5 will evaluate and compare complementary circuits using p-channel HIGFETs, and Chapter 6 will discuss remaining work that is necessary and summarize the results.

2: CHARACTERIZING THE KEY PROPERTIES OF $GaAs_xSb_{1-x}$ AND $In_xAl_{1-x}As$

The discussion of Chapter 1 is self-consistent and sound in theory, however, it relies heavily on using available experimental data to project the performance of idealized (e.g., abrupt heterojunctions and defect-free crystals) materials and structures. In essence, the previous discussion merely points one towards a likely system of materials for further, in-depth, investigation; it is not sufficient grounds for committing to development of a new technology. What is needed, then, is a characterization of the individual materials and materials combinations (heterostructures) to verify or deny their suitability for use in p-HIGFETs. This is particularly true for the proposed materials due to the uncertainty surrounding some of their properties. In particular, the mobility of holes in $GaAs_xSb_{1-x}$ (the chief reason for selection of this material) is not known with sufficient accuracy. Another key parameter for device performance is the actual value of the band-edge discontinuities for a $In_xAl_{1-x}As/GaAs_ySb_{1-y}$ heterojunction so that gate current can be adequately modeled. Therefore, a systematic approach to characterizing these parameters is necessary before it is possible to proceed with reliable device modeling and fabrication.

Of special interest for the purposes of a finished device is the hole drift mobility since this affects the transconductance as well as the magnitude of the drain current. While hole mobility is a very important property, published values for GaSb vary by approximately a factor of two [15, 17-19] and these values are based on material made using chemical vapor deposition (CVD) growth technology of the 1960's rather than material grown by modern MBE techniques. There are no published values of mobility for $GaAs_xSb_{1-x}$.

Therefore, to remedy this lack of theoretical and experimental evidence for proceeding with $GaAs_xSb_{1-x}$ as a channel material, it is essential to address both of these aspects of the problem. This is best accomplished by using Monte Carlo simulation of hole transport in the alloy to give theoretical insight into the relative effects of alloy scattering and using Hall effect measurements to calibrate

the theory experimentally. In fact, much of the theory necessary for a Monte Carlo simulation is also essential for computing the Hall factors for holes in the alloy so that drift mobility can be extracted from the measurements. (This is a non-trivial point since Hall factors for holes in GaAs have been found to be on the order of 2, a much higher value than for electrons due to the predominance of different scattering mechanisms and the interactions of two bands for holes [20].) The simultaneous use of theory and experiment forces a self-consistency upon the results which is important to overcome the uncertainty it is meant to dispel.

Even if we are satisfied that the mobility of holes in $GaAs_xSb_{1-x}$ is suitable for our purposes, it is essential for modeling the gate current of our proposed devices that we have an accurate estimate of the valence band edge discontinuity between $InAl_xAs_{1-x}$ and $GaAs_xSb_{1-x}$. No direct measurement of this discontinuity has been made, although estimates have been made. The most recent estimate of this discontinuity, made by Nakata et. al. [21], was 0.78 eV, a sizeable barrier. This estimate was based on simulation by using the discontinuity as a fitting parameter to match modeled square potential wells to photoluminescence data of quantum wells. The assumptions made in the model call into question the validity of the estimated discontinuity and necessitate the pursuit of a more reliable measurement. Such a measurement is the activation energy method developed by Sugiyama et. al. [22] which is described in Section 2.2.

2.1: MONTE CARLO SIMULATION OF $GaAs_xSb_{1-x}$ AND $In_xAl_{1-x}As$ USING HALL EFFECT CALLIBRATION

Even if reliable values were available, it would not be possible to know directly the hole mobility for an alloy of GaAs and GaSb. The reason for this uncertainty is that carriers in an alloy are subject to an additional scattering mechanism known simply as alloy scattering. (The physics of this mechanism is explored more completely below, but let it suffice here that the scattering is a result of a difference between the constituent compounds of the alloy in the various types of potentials which the carriers see as they move through the alloy.) The question then becomes a matter of how much the mobility is affected by alloy scattering. Another way of stating this is that one needs to know how much of the increased mobility given by the GaSb in the alloy is lost because of alloy scattering. A search of relevant literature does not resolve the matter since various authors have found alloy scattering to be either insignificant [23, 24] or predominant [25].

Monte Carlo simulation of carrier transport itself has a reasonably firm foundation dating back to 1966 when Kurosawa first performed a simulation of electron transport in GaAs [26]. The basic premise of such a simulation is to avoid the approximations necessary to solve the Boltzmann transport equation by using random numbers to simulate the statistical nature of semiconductor transport. Random numbers are used to select scattering mechanisms and the final states of carriers following scattering so that the full complexity of scattering rate relations is retained.

Monte Carlo simulation in this case, however, is complicated by a number of factors. Chief among these is that hole transport in general and the scattering mechanisms for holes in particular have historically received little attention. The more complicated band structure for holes, which will be explored more fully later, also makes the actual programming of the simulation more cumbersome. Finally, it is not immediately apparent how to arrive at appropriate values of the physical parameters necessary for a proper simulation since certain of these (e.g., bandgap) are known to vary

non-linearly with alloy composition. In this case, however, Adachi has shown that most of the important constants vary linearly and the others are not generally very non-linear [14, 27] Therefore, one may choose for simplicity to assume that all necessary physical parameters vary linearly with composition.

Given all the uncertainties associated with it, Monte Carlo simulation typically only provides an approximation to physical reality and a convenient method for simulating the relative effects of variations in material parameters. In addition, it is much more difficult to model actual physical structures using Monte Carlo simulations than it is to simulate idealized bulk materials. Furthermore, the mobility of carriers in a quantum well is not identically that of carriers in bulk material. Carriers residing in a two-dimensional gas scatter with each other more frequently and are confined to a certain region, another form of scattering. However, it has been shown that such carriers also screen each other from ionized impurities, reducing the amount of ionized impurity scattering and giving a net increase in mobility over that in doped bulk material [12]. For these reasons and to provide a verification of the simulations, it is desirable to calibrate the actual mobilities. This is most conveniently accomplished using Hall effect measurements [28].

Hall effect measurements have long been used as a simple means to obtain basic information about semiconductors and other materials. Such measurements can provide the majority carrier type of a material as well as such information as the sheet resistance, active impurity concentration, and a quantity known as the Hall mobility. While all this can be useful to a device designer, what interests us is the capability to measure mobility experimentally. However, the mobility obtained from Hall effect measurements is refered to as the Hall mobility because it is not the same as the drift mobility that is commonly used in semiconductor transport equations [28]. Nevertheless, the quantities are related by a coefficient known as the Hall factor, r_H. Thus μ_{drift} is given by

$$\mu_{drift} = r_H \mu_{Hall} \tag{2.1}$$

If the scattering rates are known as a function of energy, r_H can be calculated from

$$r_H = \frac{\langle \tau \rangle^2}{\langle \tau^2 \rangle}, \tag{2.2}$$

where τ is the energy-dependent relaxation time. Once this factor has been calculated, it can be used to calibrate the mobilities from Monte Carlo simulations.

Using this approach then, it is possible to use Monte Carlo simulation to provide a first-order estimate of drift mobility. This estimate can be refined using the measured mobility from Hall effect measurements. The refined estimate can then be used to extend beyond the fields attainable for Hall effect to those more typical of actual devices. This combination of measured and calculated mobilities provides a much more reliable quantity for the drift mobility in $GaAs_xSb_{1-x}$ than is presently available.

2.1.1: THE MONTE CARLO METHOD

In the following pages, we will examine Monte Carlo simulation of semiconductor carrier transport as it pertains to determining the suitability of $GaAs_xSb_{1-x}$ and $In_xAl_{1-x}As$ for p-channel HIGFETs. The results of such a simulation including all the dominant scattering mechanisms for holes in these materials show that $GaAs_xSb_{1-x}$ and $In_xAl_{1-x}As$ should indeed have useful transport properties for p-channel HIGFETs.

When studying the transport properties of carriers in a semiconductor, it should theoretically be possible to directly calculate the carrier mobilities as well as their complete velocity versus electric field relationships. Such a calculation would be accomplished by using the Boltzmann transport equation which requires analytical expressions for all scattering rates [29]. However, even if such expressions are known, the transport equation cannot be solved analytically without restrictive assumptions and approximations such as a very low electric field. While such an approach can provide valuable insight into the low-field behavior of carriers in a semiconductor, one loses much

generality and any hope of examining the high-field regime. The most common solution to this dilemma is the Monte Carlo method of simulation.

The Monte Carlo method of simulation is one that is often used to simulate statistical processes and derives its name from the use of random numbers to reproduce the distributions of these processes. In the case of semiconductor carrier transport, carriers are allowed to accelerate freely under an applied electric field according to classical laws of motion but random numbers are used to select when a scattering event takes place and what the final state of the carrier is after the collision. The Monte Carlo method is therefore a semiclassical one; free flight is calculated according to classical laws but scattering rates and final state probabilities are determined quantum-mechanically. This method is based on the approach first developed by Kurosawa [26].

In theory, such a collision-by-collision simulation should be very accurate since it can allow the full complexity of band structure and scattering events to be modeled. Such accuracy, however, is not often realized in practice. The most common limitation to full modeling by the Monte Carlo method is that it is computationally intensive, and grows increasingly so as detail is added to the models used, particularly if holes rather than electrons are simulated. For, instance the simulation of one point of a velocity versus field relationship typically requires on the order of 100,000 collisions and billions of iterations. The judicious application of certain approximations, however, greatly relieves some of the computational burden for the simulation without a great loss of accuracy. For example, although the bands of semiconductors are not perfectly parabolic, they are often approximated as such to simplify the energy and wave vector calculations.

The best way to understand how a Monte Carlo simulation works is to step through the algorithm that is used. (We shall assume only single band transport in this example.) Once the algorithm is initialized by the assumptions of values for physical quantities, the first step is to calculate the maximum scattering rate for the simulated conditions for reasons which will be detailed below. This is accomplished quite easily, since scattering varies smoothly with respect to

the carrier momentum vector, **k**, by calculating all the scattering rates for the pertinent scattering mechanisms over a range of expected carrier **k** values and finding the maximum total scattering rate (sum of the rates of all mechanisms), S_{max}. Each free flight time, t_f, is then set equal to the inverse of S_{max}. Once this has been accomplished, the carrier is allowed to accelerate freely under the electric field according to

$$\mathbf{k}(t) = \mathbf{k}_0 + \frac{q\mathbf{F}}{\hbar} t_f \tag{2.3}$$

where $k(t)$ is the time-varying carrier wave vector, k_0 is the initial wave vector, q is the electronic charge, and F is the electric field vector. The actual energy that the particle gains is of course determined by the effective mass of the band in which the carrier resides during the free flight.

Since the scattering rates are a function of the wave number, k, the rates for each mechanism are calculated at the end of the free flight and a random number is generated. The range of the random numbers is scaled to S_{max} and a scattering rate is chosen by dividing the range into bins proportional to the rate for each mechanism and choosing the scattering mechanism in whose bin the random number lays. For example, if there are only two mechanisms and, at a particular k, one of these has a scattering rate half as large as S_{max} and the other has a rate one-quarter of S_{max}, then the first is given a bin which occupies half the range and the second a bin that is one-quarter the range. In this example, the mechanisms have selection probabilities of 50% and 25%, respectively. If none of the mechanisms are chosen (an intentionally frequent occurrence), then the carrier is allowed another free flight; such an event is often referred to as self-scattering.

If a physical scattering mechanism is chosen, then the final state after scattering must be chosen. To do this, one again generates a random number, which is used in a manner similar to that above to determine the final angle of the wave vector according to a derived angular distribution for the chosen scattering mechanism, and the magnitude of the vector is determined by the characteristics of the mechanism. Once the final state has been determined, the carrier is once again allowed a free flight and the process is repeated until enough scattering events have occurred that carrier

velocity is approximately constant. A flow chart for this algorithm is shown in Figure 2.1.

Though the algorithm for this simulation is rather simple, the question naturally arises as to why fixed-length free flights are used rather than computing the flight time by simulating the probability distribution of scattering events. The answer is that this is one of the simplifying approximations made to ease the computational load. This is necessary because the total scattering rate is a complicated function of $\boldsymbol{k}(t)$, making the simulation of the probability distribution difficult. The solution is to make the total scattering rate a constant equal to the maximum scattering rate and introducing a non-physical scattering mechanism (self-scattering) to make up the difference between S_{max} and the actual rate. (To maintain the fidelity of the simulation, "self-scattering" does not change the state of the carrier.) If S_{max} is much larger than the typical scattering rate, then the fixed free-flight intervals are small enough to have little effect on the accuracy of the simulation [30]. That is, the time steps will be fine enough that the probability distribution of the scattering events will be approximately simulated.

2.1.2: VALENCE BAND STRUCTURE AND SCATTERING MECHANISMS

The Monte Carlo simulation is a well-established tool for electron transport problems [30] with the accompanying wealth of supporting work on the optimum expressions for scattering rates and the best values for physical quantities for various materials. The situation for hole transport, however, is quite different. The relatively low mobility of holes as compared to electrons in polar semiconductors has resulted in very little work being done on modeling hole transport in such materials. This is especially important because hole transport is significantly more complex than typical electron transport for reasons detailed below. Despite the small amount of work that has been done on hole transport, that which does exist is relatively thorough and provides a suitable foundation for modeling bulk transport in $GaAs_xSb_{1-x}$ and $In_xAl_{1-x}As$ [14, 25, 27, 31-35].

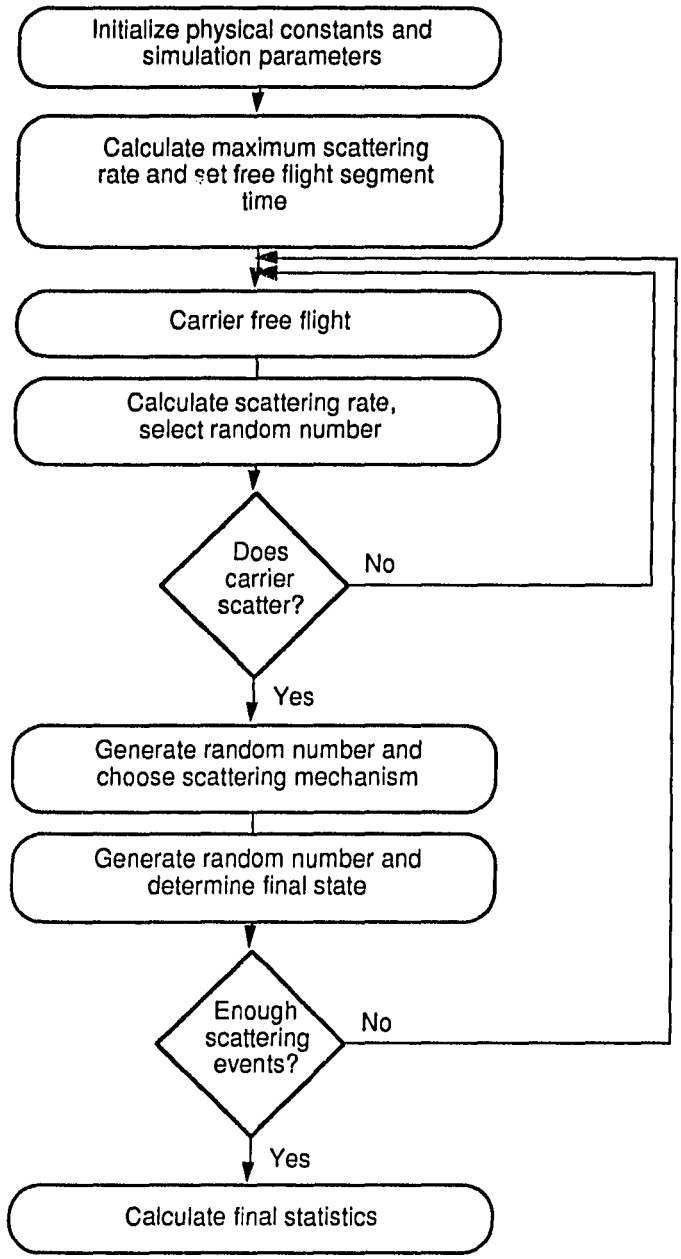

Figure 2.1: Sample algorithm for simulation of semiconductor carrier transport by the Monte Carlo method assuming only one band.

The principle factor which makes valence band transport more complex is that the band for polar semiconductors, including those of interest here, is degenerate at the Γ point (k=0) and though the bands separate at higher k values, they still interact and have different effective masses, as shown in Figure 2.2. Therefore, scattering rates will depend on energy as well as the resident band of the carrier. This is similar to intervalley scattering of electrons in GaAs, but it applies to all scattering mechanisms for all energies. In general, the scattering rate for a particular mechanism is proportional to some power of the effective mass of the band into which the carrier will scatter since this determines the number of available states.

For holes in a semiconductor, there are five important scattering mechanisms: acoustic phonon, non-polar optical phonon, ionized impurity, polar optical phonon, and alloy scattering (only for alloys). The relationships for all these mechanism are calculated by the same procedure. The total scattering rate, $\lambda(\mathbf{k})$, for a particular mechanism is determined by [29]

$$\lambda(\mathbf{k}) = \int W(\mathbf{k},\mathbf{k}')\, dV_{k'}. \tag{2.4}$$

In this equation, $W(k,k')$ is given by the "golden rule" of quantum mechanics,

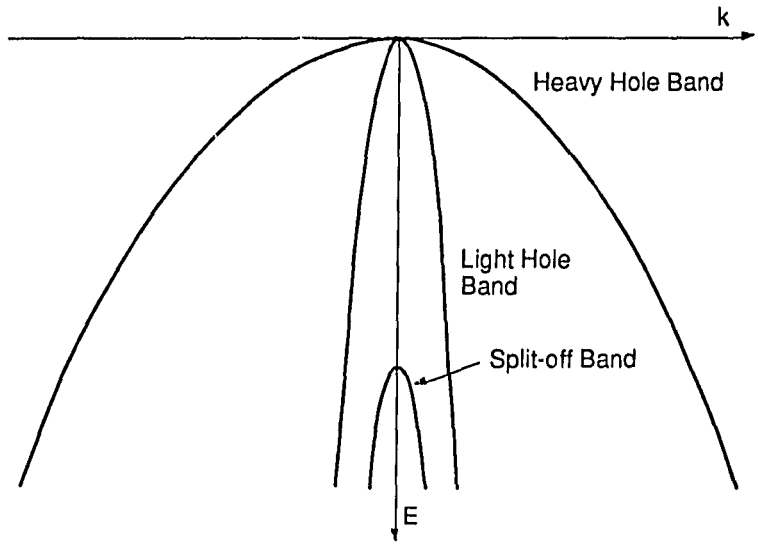

Figure 2.2: A generic valence band diagram.

$$W(\mathbf{k},\mathbf{k}') = \frac{2\pi}{\hbar}|H|^2\,\delta(E'-E) \tag{2.5}$$

where E' and E are the initial and final (with respect to the scattering event) energies and $|H|^2$ is the squared matrix element of the Hamiltonian for the particular mechanism. $|H|^2$ is further specified as

$$|H|^2 = A(\mathbf{k})\,G(\mathbf{k},\mathbf{k}'), \tag{2.6}$$

where $A(k)$ is dependent on the particular scattering mechanism and $G(k,k')$ is the overlap factor,

$$G(\mathbf{k},\mathbf{k}') = \left|\int_{cell} u_{\mathbf{k}}(\mathbf{r})\,u_{\mathbf{k}'}(\mathbf{r})\,d\mathbf{r}\right|^2, \tag{2.7}$$

between the periodic wave functions of the initial and final states, $u_k(r)$ and $u_{k'}(r)$ [29].

In physical terms, acoustic phonon scattering and non-polar optical phonon scattering are caused by the deformation of the lattice (these mechanisms are sometimes referred to as deformation potential scattering) by the vibrations of either type of phonon which locally modulates the band structure in the vicinity of the phonon. The principle difference between these two types of scattering is that, although both involve a change in energy to the carrier during the scattering (an inelastic process), the energy entailed in acoustic phonon scattering is so small that it is usually neglected and it is treated as an elastic mechanism while the energy change for non-polar optical scattering is significant and may not be overlooked.

Costato and Reggiani first calculated scattering rates for these mechanisms in 1973 [33]. The resulting expressions are

$$\lambda_{AC}(k) = \frac{k_B T m_i E_1^2}{4\pi \bar{s}^2 \rho \hbar^3}\left(\frac{m_f}{m_i}\right)^{1/2} k, \qquad \text{and} \tag{2.7}$$

$$\lambda_{NPO}(k) = \frac{(DK)^2 m_f^{3/2}}{2\sqrt{2}\,\pi\rho\hbar^3\,\omega_{LO}}\left(\frac{\hbar^2k^2}{2m_i} \pm \hbar\omega_{LO}\right)^{1/2}\begin{Bmatrix} N_0 \\ N_0+1 \end{Bmatrix}. \tag{2.8}$$

For these equations the upper and lower signs and the factors N_0 and N_0+1 each correspond to phonon absorption and emission, respectively, k_B is the Boltzmann constant, h is the reduced Planck

constant, T is the lattice temperature, k is the wave number of the carrier, ρ is the material density, m_f and m_i are the effective masses of the final and initial bands, respectively, ω_{LO} is the angular frequency of the longitudinal optical phonon of the material, E is a phenomenological deformation potential given by

$$E_1^2 = \left(1/3 + 2/3\left(\frac{s_t}{s_l}\right)^2\right)\left[a^2 + \frac{C_l}{C_t}\left(b^2 + 1/2\, d^2\right)\right] \tag{2.9}$$

where a, b, and d are deformation potentials of the material, s_l and s_t are the longitudinal and transverse speeds of sound and C_l and C_t are the average longitudinal and transverse elastic constants given by

$$C_l = 1/5(3\, c_{11} + 2\, c_{12} + 4\, c_{44}) \tag{2.10}$$

$$C_t = 1/5(c_{11} - c_{12} + 3\, c_{44}), \tag{2.11}$$

where c_{11}, c_{12}, and c_{44} are the crystal elastic constants. N_0 is the optical phonon occupation number given by

$$N_0 = \left(\exp\left[\hbar\,\omega_{LO}/k_B\,T\right] - 1\right)^{-1} \tag{2.12}$$

and $(DK)^2$ is the optical phonon coupling constant given by Conwell [36] as

$$(DK)^2 = 4\left(\omega_{LO}/s_l\right)^2 E_1^2. \tag{2.13}$$

(These equations, as well as those that follow, assume that all bands are parabolic and spherically symmetric, except as noted.)

Ionized impurity scattering is simply the Coulombic interaction between carriers and the ionized impurity atoms in the lattice. This interaction causes the carrier to be deflected from its path. Costato and Reggiani also calculated scattering rates for this mechanism [33], but Brudevoll et. al. made important corrections in 1990 [31]. The correct expression is

$$\lambda_{II}(k) = \frac{3\, e^4\, N_i\, m_f\, F}{32\ \pi \hbar^3\, \varepsilon_0 \varepsilon_r k_i^3 \left(\frac{m_f}{m_i}\right)^{1/2}}, \tag{2.14}$$

where e is the electronic charge, N_i is the impurity density, ε_0 and ε_r are the dielectric constant of

vacuum and the relative dielectric constant of the material, respectively, and F differs for interband and intraband scattering as

$$F^{intra} = \frac{\beta^2 + 2k^2}{k^2}\ln\left(\frac{\beta^2}{\beta^2 + 4k^2}\right) + 4/3\frac{3\beta^4 + 12\beta^2k^2 + 8k^4}{\beta^2\left(\beta^2 + 4k^2\right)} \quad \text{and} \tag{2.15a}$$

$$F^{inter} = \frac{\beta^2 + k_i^2 + k_f^2}{k_i k_f}\ln\left(\frac{\beta^2 + \left(k_i + k_f\right)^2}{\beta^2 + \left(k_i - k_f\right)^2}\right) - 4, \tag{2.15b}$$

where $\beta=(N_i e^2/k_B T\varepsilon_0\varepsilon_r)^{1/2}$ is the inverse charge screening length.

Polar optical phonon scattering is caused in a polar semiconductor such as GaAs when the lattice vibrations of optical phonons create a long-range Coulombic force from the motion of the sublattices. As for ionized impurity scattering, Costato et. al. were also the first to calculate the hole scattering rates for polar optical phonons [32, 34], but corrections were made by Brudevoll et. al. [31]. The corrected expressions are given by

$$\lambda_{PO}(k) = \frac{e^2\omega_{LO}m_f}{4\pi\varepsilon_0\hbar^2}\left(\frac{1}{\varepsilon_\infty} - \frac{1}{\varepsilon_r}\right)\left\{\begin{matrix} N_0 \\ N_0 + 1 \end{matrix}\right\}\frac{\Psi H}{k}, \tag{2.16}$$

where ε_∞ is the relative dielectric constant at high frequencies, Ψ is defined by

$$\Psi = \ln\left|\left(1 + \left(\frac{m_f}{m_i}\right)^{1/2}\right)\Big/\left(1 - \left(\frac{m_f}{m_i}\right)^{1/2}\right)\right|, \tag{2.17}$$

and H differs for interband and intraband scattering as

$$H^{intra} = \frac{1 + 3\Phi\left(\Phi - \Psi^{-1}\right)}{4} \quad \text{and} \tag{2.18a}$$

$$H^{inter} = \frac{3\left[1 - 3\,\Phi\left(\Phi - \Psi^{-1}\right)\right]}{4}, \tag{2.18b}$$

and Φ is defined by

$$\Phi = \left(1 + m_f/m_i\right)/2. \tag{2.19}$$

Alloy scattering, as the name implies, is peculiar to alloys of semiconductors, and, as such has not received much attention until recently. Alloy scattering arises from the fact that an alloy is a

mixture of materials, not a compound, and a carrier moving through the mixture encounters one constituent compound at some instants and another at other times. This constant change also holds for the details of the band structure that the carrier experiences; the carrier moves from one set of potentials to another. It is this change which is the cause of the scattering. Of the scattering mechanisms described here, alloy scattering is the most poorly understood. The currently accepted expression for alloy scattering, given by

$$\lambda_{ALL}(k) = \frac{V_c\, x\,(1-x)\,(\Delta E)^2\, m_f\, k}{2\,\pi\,\hbar^3}\left(\frac{m_f}{m_l}\right)^{1/2} \tag{2.20}$$

where V_c is the volume of the crystal unit cell, x is the mole fraction of one of the constituent compounds, and ΔE is the characteristic potential difference of the alloy known as the alloy potential. This expression is based upon a model of an alloy with randomly distributed compounds and that molecules of one of the compounds create a potential well with respect to the other compound [37]. The physical origins of the alloy potential and its shape and extent are still disputed [24, 38-40] and in practice requires a fit for new materials.

It is apparent from the preceding that reliable physical constants and parameters for the materials to be simulated are imperative if there is to be any hope of accuracy. In the case of most compound and elemental semiconductors, a great deal of work has been done to measure many or all of these parameters such that many of the quantities may be used with a great deal of confidence. The great variety of possible alloys of compounds dictates that one will virtually always be faced with a general paucity of essential data on new combinations. Adachi has shown [14, 27] recently, though, that the quantities central to transport simulation such as effective mass vary linearly or almost linearly with composition, which allows one to calculate physical parameters of an alloy from the properties of its component compounds. Table 2.1 shows the values that were used in the present simulation.

Table 2.1: Material parameters used for Monte Carlo Simulation.

	GaAs	GaSb	InAs	AlAs
m_{hh}/m_0	0.475 [41]	0.330 [42]	0.600 [43]	0.760 [43]
m_{lh}/m_0	0.087 [41]	0.046 [44]	0.027 [43]	0.150 [43]
ρ (g/cm^3)	5.36 [45]	5.61 [46]	5.67 [14]	3.76 [45]
ω_{LO} (rad/s)	5.30×10^{13} [47]	4.52×10^{13} [48]	4.58×10^{13} [48]	7.72×10^{13} [47]
ε_r	13.20 [49]	15.69 [48]	14.60 [14]	10.06 [50]
ε_∞	10.89 [49]	14.44 [48]	12.25 [14]	8.16 [50]
s_l (cm/s)	4.73×10^5 [46]	3.97×10^5 [46]	4.45×10^5 [51]	5.55×10^5 [27]
s_t (cm/s)	3.34×10^5 [46]	2.77×10^5 [46]	2.64×10^5 [51]	3.95×10^5 [27]
C_l (dyn/cm^2)	1.403×10^{12} [52]	1.038×10^{12} [46]	9.975×10^{11} [53]	1.340×10^{12} [27]
C_t (dyn/cm^2)	4.860×10^{11} [52]	3.550×10^{11} [46]	3.136×10^{11} [53]	4.490×10^{12} [27]
a (eV)	10.0 [25]	2.21 [14]	2.50 [54]	15.0 [25]
b (eV)	−1.70 [25]	−3.30 [55]	−1.80 [56]	−1.60 [25]
d (eV)	−4.40 [25]	−8.35 [57]	−3.60 [56]	−3.40 [25]

The reader will find that certain parameters appear to be missing from Table 2.1 such as the effective mass of the split-off band and alloy potentials for the materials. Some of these parameters are not in the table because they are calculated from values that are already included. For example, v_c is calculated from the calculated density of the alloy. In the case of the alloy potential, this parameter is not sufficiently understood to allow it to be anything more than a fitting parameter for an unknown alloy. The effective mass for the split-off band is omitted intentionally because, for all these semiconductors, the band is so energetically distant from the light- and heavy-hole bands that

they are effectively uncoupled under conditions typical for a transistor and the split-off band may be ignored.

It should be noted that though there is more than one published value for many of the parameters above, values were chosen that are either generally accepted for use in modeling, or, if there is no general agreement, fitted data to measured mobilities for the compounds. Using these values, the scattering rates as a function of energy shown in Figures 2.3-2.22 were obtained. These figures show that the much larger density of states in the heavy-hole band results in intraband scattering dominating for holes in that band and holes in the light-hole band having a much higher probability of scattering to the heavy hole band. Note also that ionized impurity scattering has the highest probability at lower energies. (An acceptor density of 10^{17} cm^{-3} was chosen as representative of HIGFET channel doping.)

The scattering mechanism with highest scattering probability does not necessarily affect the carrier mobility the most. The difference is that the different mechanisms affect the carriers in different ways. Ionized impurity scattering, for example, does not have a very great effect because there is no energy lost by the carrier and carriers tend to be deflected by small angles except at very low fields, so little forward mometum tends to be lost. In a Monte Carlo simulation, these differences are accounted for when the final state after scattering is chosen. In general, the algorithm will choose a final k value and an angle, γ, relative to the $\boldsymbol{k}$ vector before scattering. The k value is easily found knowing the initial state of the carrier and what band it will go to, the energy change for the mechanism, and the band structure of the material. γ is found by selecting random numbers to conform to a probability distribution determined by the scattering mechanism.

In the cases of acoustic phonon scattering, alloy scattering, and non-polar optical phonon scattering, the final angle is determined by the overlap factor. This typically results in a loss of forward momentum that reduces the average forward velocity of the carrier. The final angle is therefore chosen by

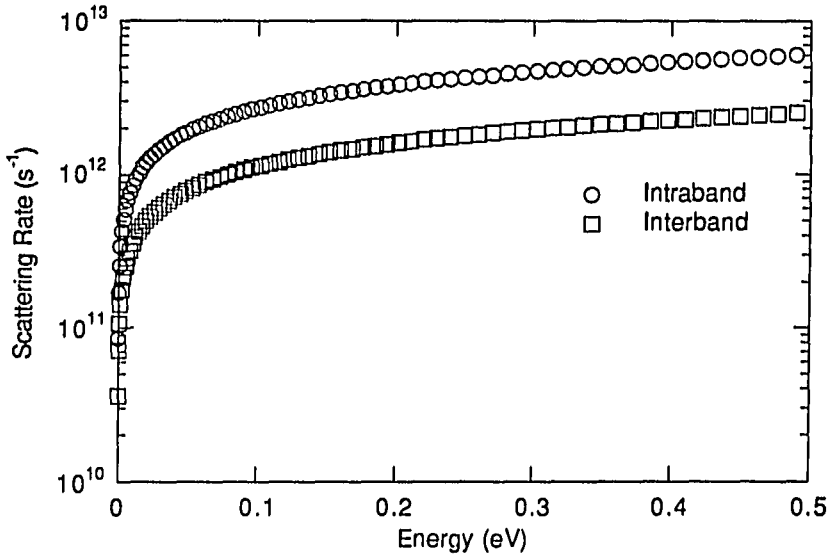

Figure 2.3: Heavy hole acoustic phonon rates for $GaAs_{0.51}Sb_{0.49}$; rates for absorption and emission are equal.

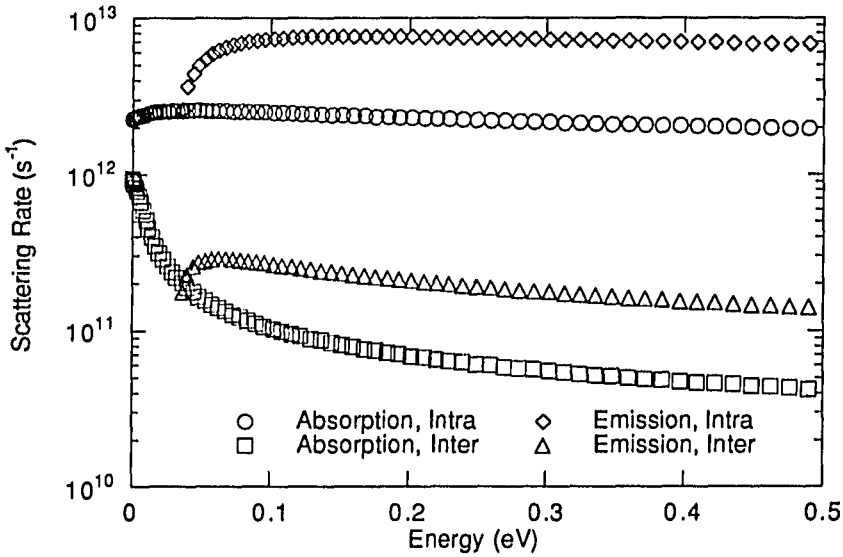

Figure 2.4: Heavy hole scattering rates for polar optical phonons in $GaAs_{0.51}Sb_{0.49}$.

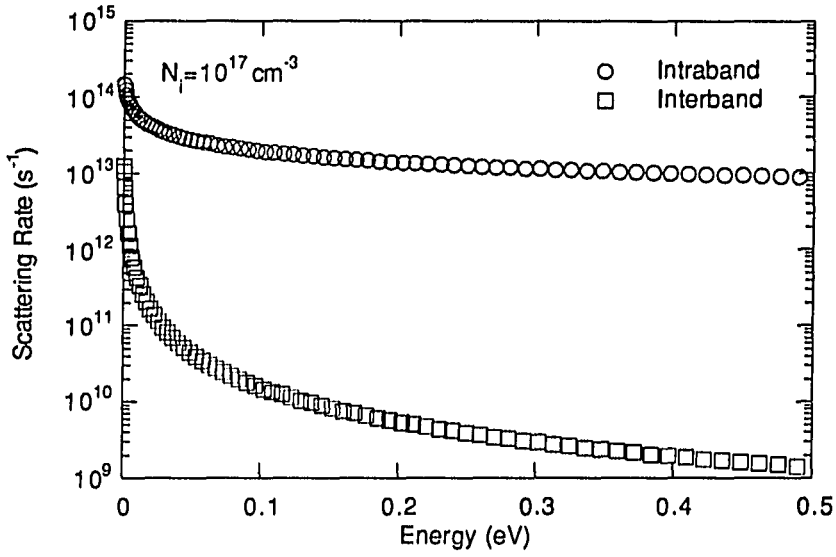

Figure 2.5: Heavy hole ionized impurity scattering rates for $GaAs_{0.51}Sb_{0.49}$.

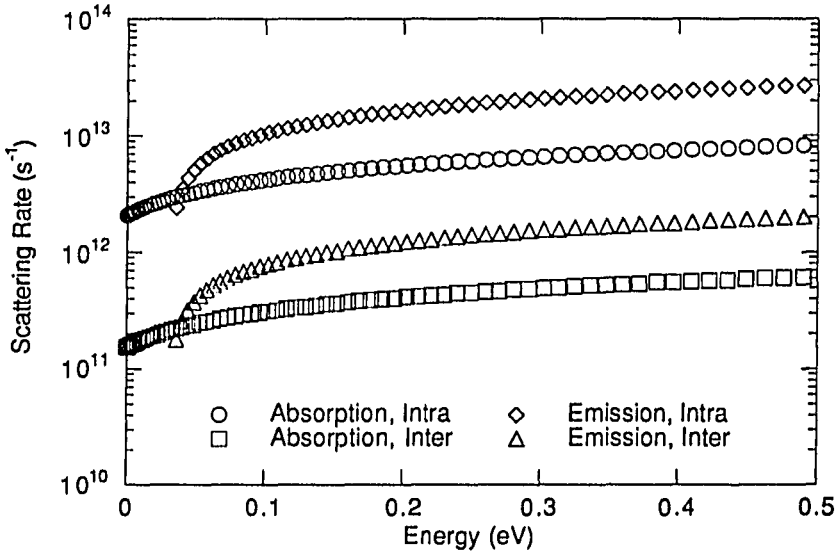

Figure 2.6: Heavy hole scattering rates for non- polar optical phonons in $GaAs_{0.51}Sb_{0.49}$.

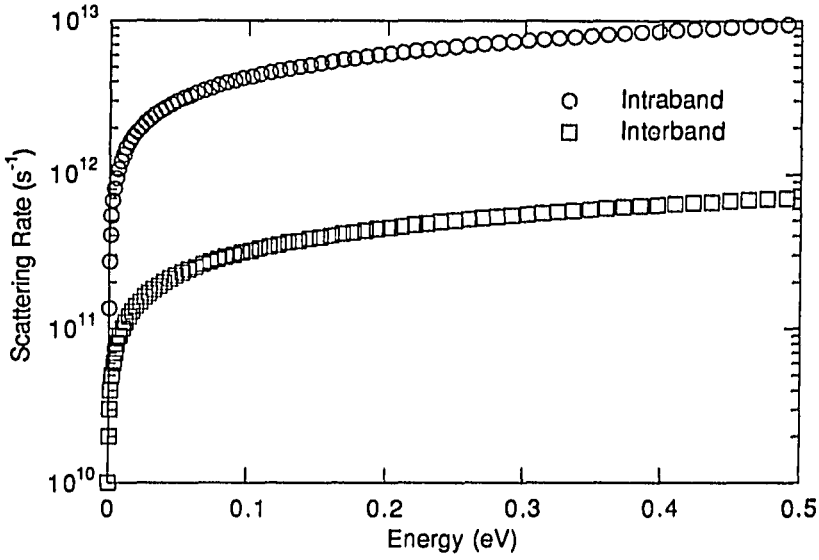

Figure 2.7: Heavy hole alloy scattering rates for $GaAs_{0.51}Sb_{0.49}$.

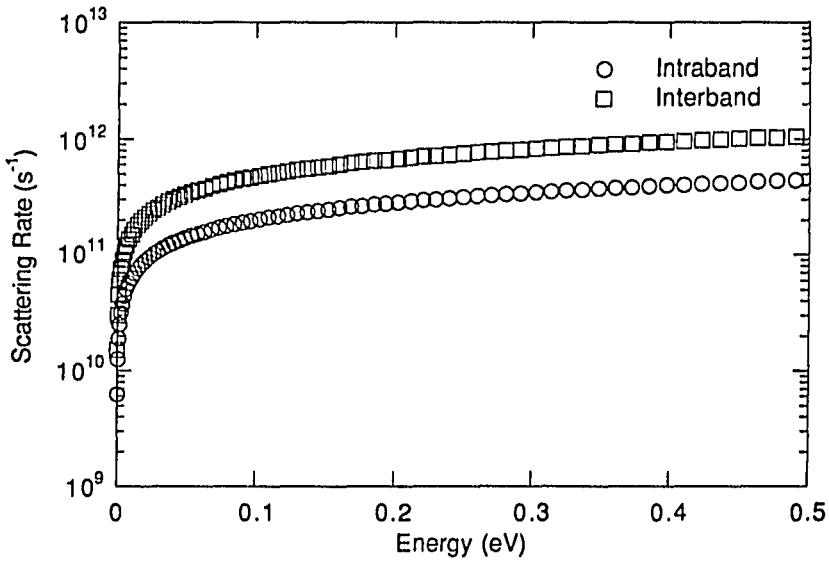

Figure 2.8: Light hole acoustic phonon rates for $GaAs_{0.51}Sb_{0.49}$; rates for absorption and emission are equal.

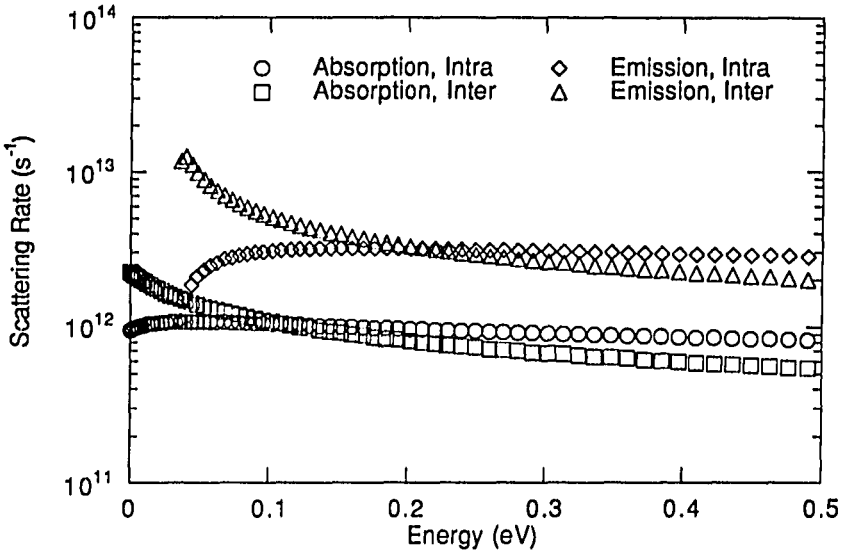

Figure 2.9: Light hole scattering rates for polar optical phonons in $GaAs_{0.51}Sb_{0.49}$.

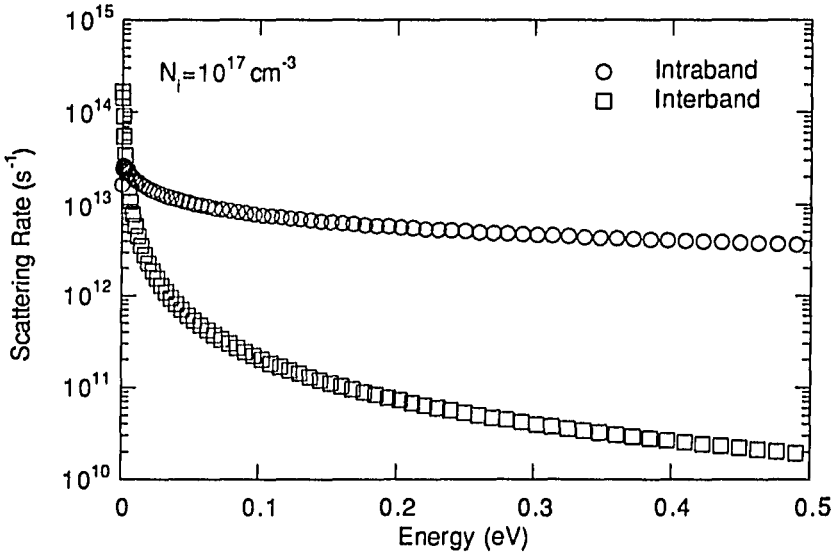

Figure 2.10: Light hole ionized impurity scattering rates for $GaAs_{0.51}Sb_{0.49}$.

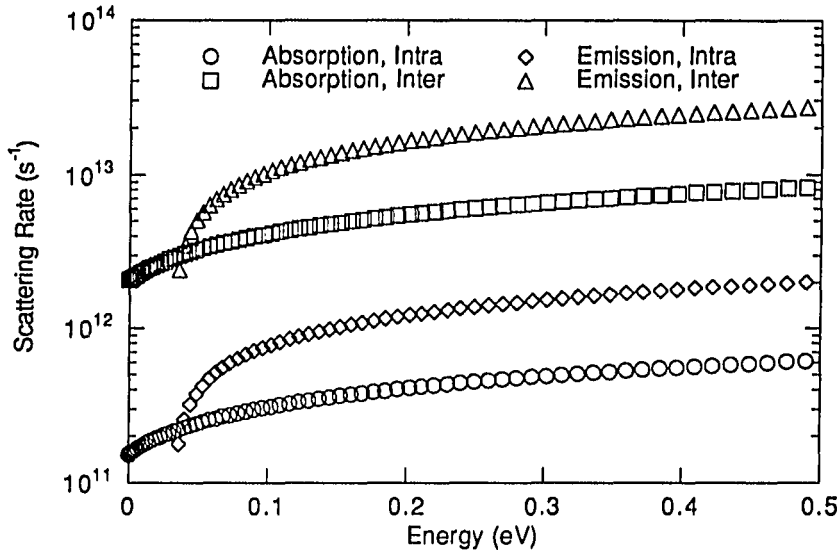

Figure 2.11: Light hole scattering rates for non- polar optical phonons in $GaAs_{0.51}Sb_{0.49}$.

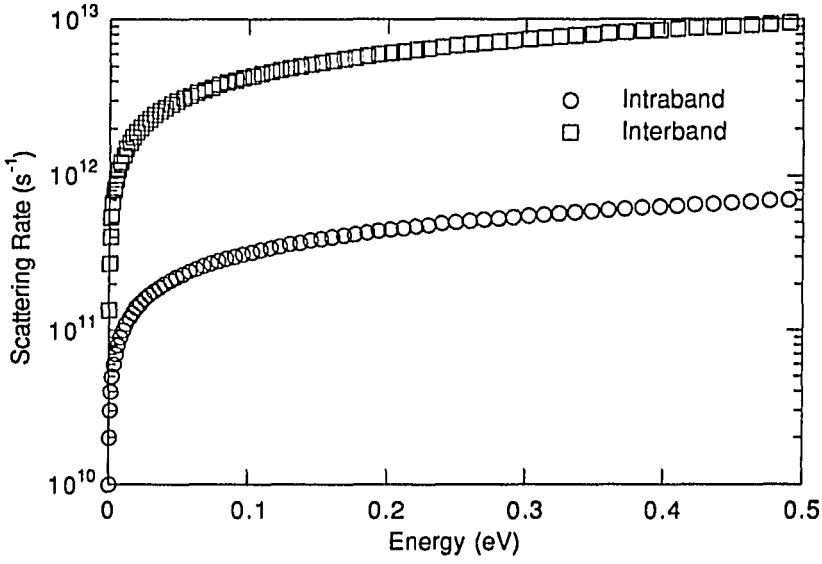

Figure 2.12: Light hole alloy scattering rates for $GaAs_{0.51}Sb_{0.49}$.

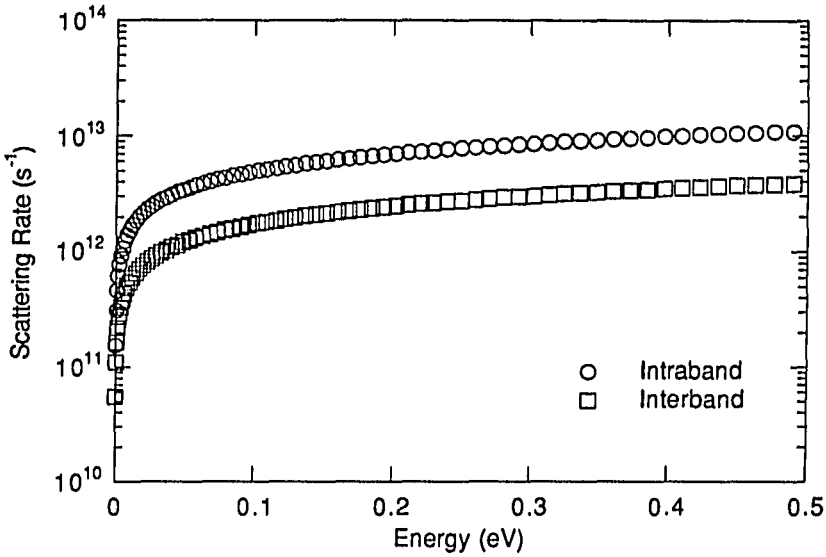

Figure 2.13: Heavy hole acoustic phonon rates for $In_{0.52}Al_{0.48}As$; rates for absorption and emission are equal.

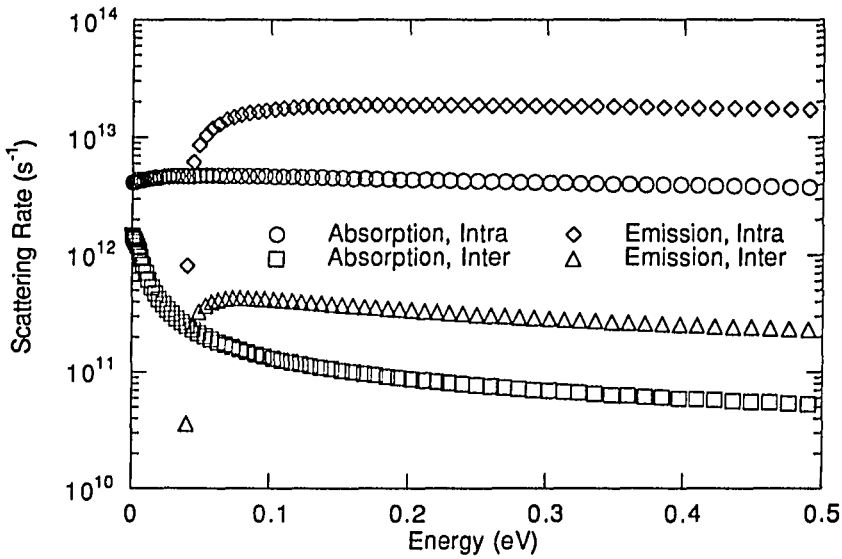

Figure 2.14: Heavy hole scattering rates for polar optical phonons in $In_{0.52}Al_{0.48}As$.

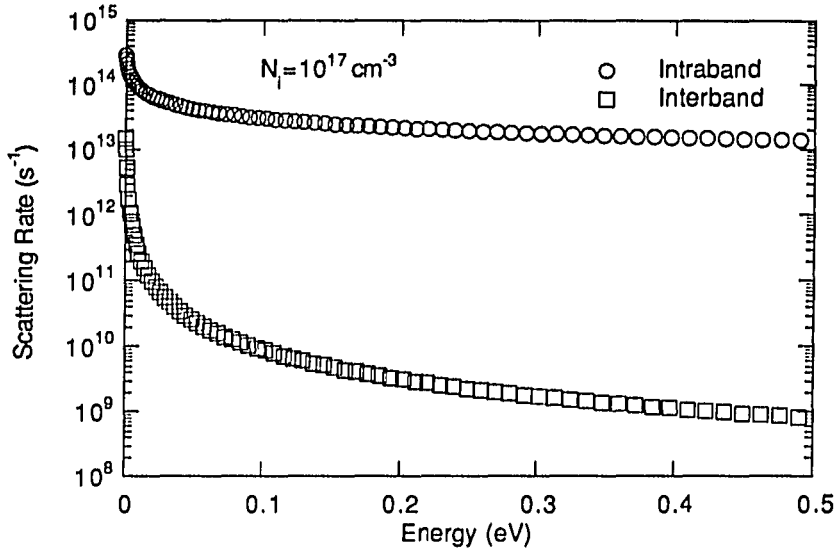

Figure 2.15: Heavy hole ionized impurity scattering rates for $In_{0.52}Al_{0.48}As$.

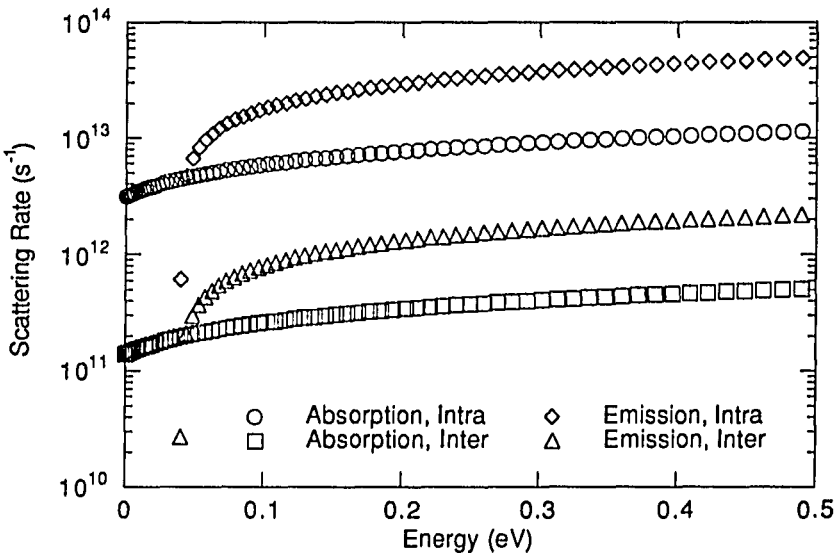

Figure 2.16: Heavy hole scattering rates for non- polar optical phonons in $In_{0.52}Al_{0.48}As$.

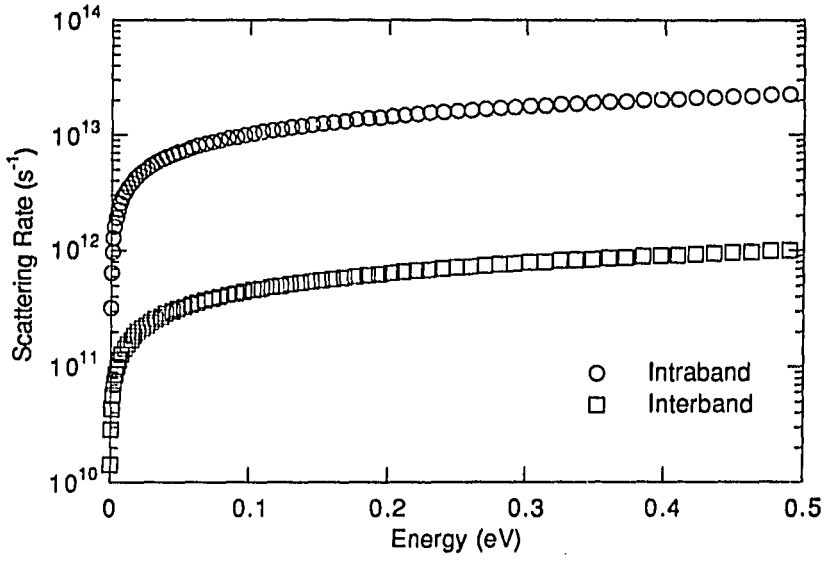

Figure 2.17: Heavy hole alloy scattering rates for $In_{0.52}Al_{0.48}As$.

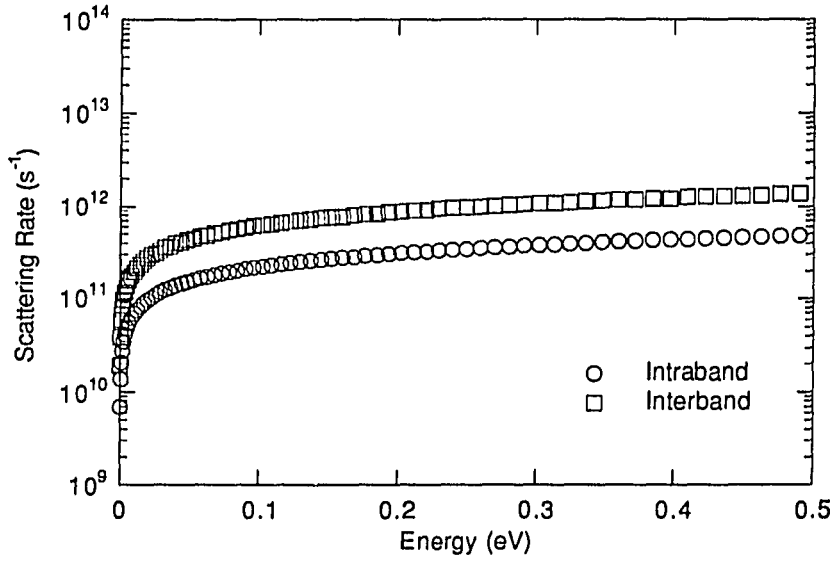

Figure 2.18: Light hole acoustic phonon rates for $In_{0.52}Al_{0.48}As$; rates for absorption and emission are equal.

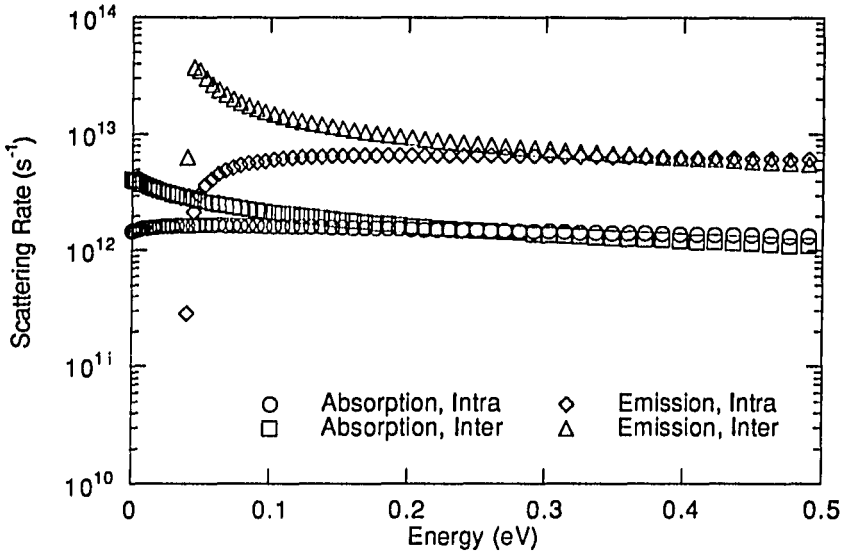

Figure 2.19: Light hole scattering rates for polar optical phonons in $In_{0.52}Al_{0.48}As$.

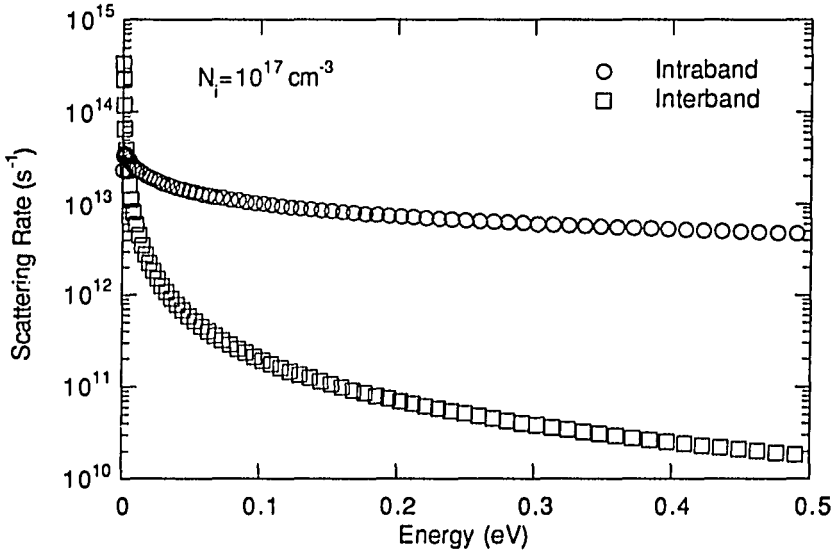

Figure 2.20: Light hole ionized impurity scattering rates for $In_{0.52}Al_{0.48}As$.

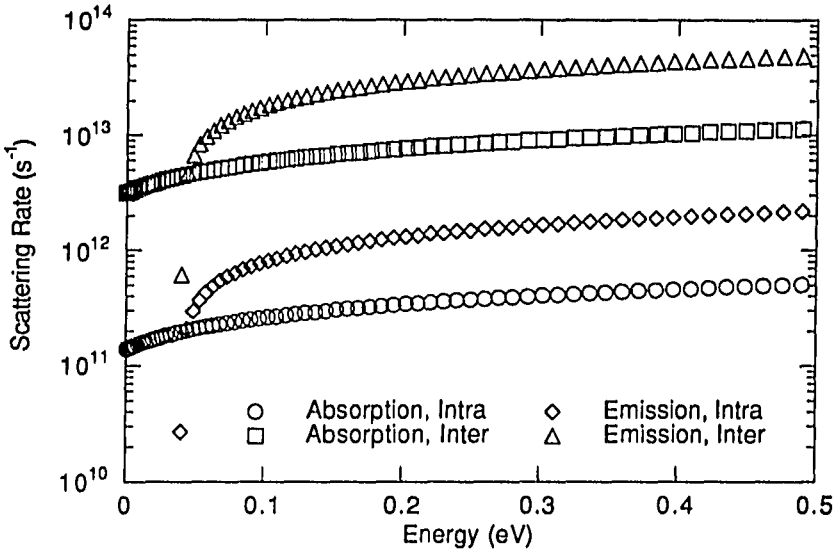

Figure 2.21: Light hole scattering rates for non- polar optical phonons in $In_{0.52}Al_{0.48}As$.

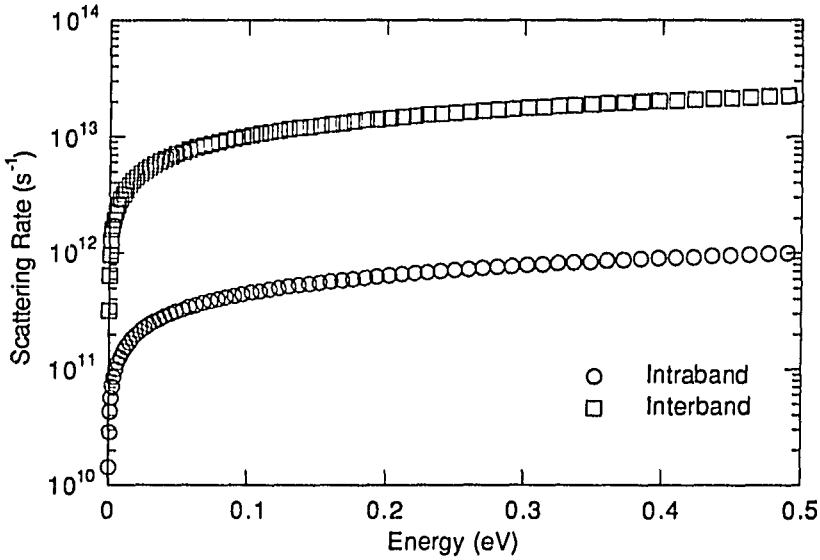

Figure 2.22: Light hole alloy scattering rates for $In_{0.52}Al_{0.48}As$.

$$P^{intra}(\gamma) = \frac{1 + 3\cos^2\gamma}{4} \tag{2.21a}$$

$$P^{inter}(\gamma) = \frac{3\sin^2\gamma}{4}, \tag{2.21b}$$

using the approximations of Wiley [58]. While these approximations are most accurate for moderate- and large-bandgap semiconductors, the primary consequence of applying these approximations to these materials with smaller bandgaps is to underestimate the scattering rates and mobility of light holes. (The azimuthal angle with respect to the intial trajectory is assumed in all cases to be uniformly distributed and is also chosen by a random number.) All these mechanisms lower mobility by allowing backward scattering which tends to negate foward velocity which has built up. In addition, non-polar optical phonon scattering entails an energy loss which reduces velocity every time it occurs.

The final states for polar optical phonon scattering and ionized impurity scattering is different. For these scattering events, γ depends on the overlap factor as well as the magnitude of the vector between the intial and final states (polar optical) or a term which accounts for the coulombic force and charge screening (ionized impurity). The probabilities are given [59] for polar optical scattering by

$$P^{intra}(\gamma) = \frac{1 + 3\cos^2\gamma}{4\left[k_i^2 + k_f^2 - 2k_i k_f \cos\gamma\right]} \tag{2.22a}$$

$$P^{inter}(\gamma) = \frac{\sin^2\gamma}{k_i^2 + k_f^2 - 2k_i k_f \cos\gamma}, \tag{2.22b}$$

and for ionized impurity scattering by

$$P^{intra}(\gamma) = \frac{1 + 3\cos^2\gamma}{\left[1 - \cos\gamma + \beta^2/2k^2\right]^2} \tag{2.23a}$$

$$P^{inter}(\gamma) = \frac{\sin^2 \gamma}{\left[1 + m_f/m_i - 2\left(m_f/m_i\right)^{1/2}\cos\gamma + \beta^2/k_i^2\right]^2}. \qquad (2.23b)$$

The result of these expressions is that, for polar optical scattering, the final states are most likely to be in the forward direction, but there is still a possibility of backward scattering. For ionized impurity scattering, the scattering angle β becomes progressively smaller as the particle energy rises (the particle is deflected less). The consequence of this is that polar optical phonon scattering has a much greater effect on reducing the mobility of holes since it includes energy loss through phonon emission and allows for momentum loss through backward scattering. Therefore the scattering mechanisms that are most effective at reducing mobility, for equal scattering rates, are non-polar optical phonon scattering, polar optical phonon scattering, alloy scattering (depending on alloy potential), acoustic phonon scattering, and ionized impurity scattering, in descending order.

2.1.3: MONTE CARLO SIMULATION RESULTS

When all these factors were put into the simulation, the relationship between carrier velocity and applied electric field was examined. Figures 2.23and 2.24 show this relationship for $GaAs_{0.51}Sb_{0.49}$ and $In_{0.52}Al_{0.48}As$, respectively, for a range of alloy potentials between zero and the difference in energy band gaps assuming a doping level of 10^{17} cm^{-3}. Figure 2.23 demonstrates that $GaAs_{0.51}Sb_{0.49}$ has the potential for higher hole velocity than GaAs [60] and $In_{0.53}Ga_{0.47}As$ [35] for all assumed alloy potentials, and should therefore be a better channel material for p-type devices. Figure 2.24 shows that $In_{0.52}Al_{0.48}As$, has a comparable or better mobility than $Al_{0.5}Ga_{0.5}As$, showing its suitability as a barrier layer rather than a charge transport layer. Superior transport properties for a barrier layer help to reduce losses from parallel conduction in this layer. The effect of doping level on mobility is shown to be relatively small in Figures 2.25 and 2.26. The effect of alloy potential for room temperature and liquid nitrogen temperature is shown in Figures 2.27 and 2.28;

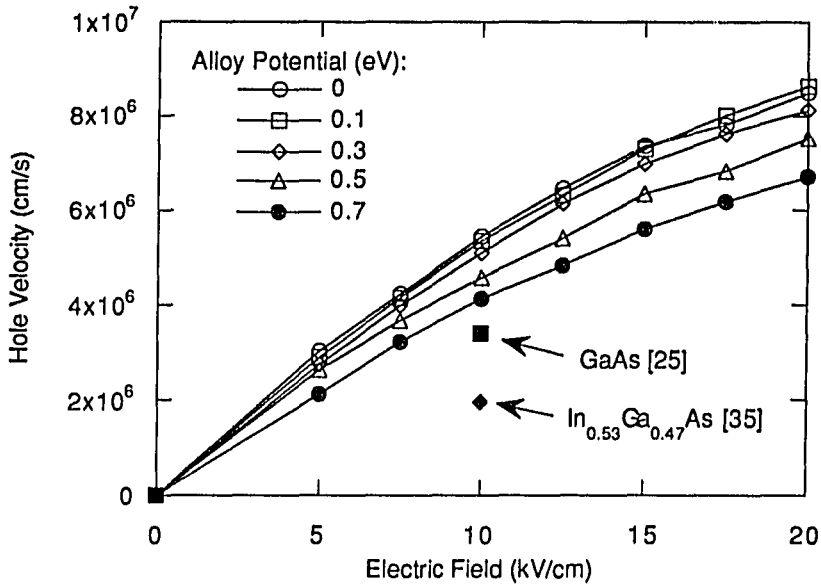

Figure 2.23: Hole velocity versus electric field for $GaAs_{0.51}Sb_{0.49}$.

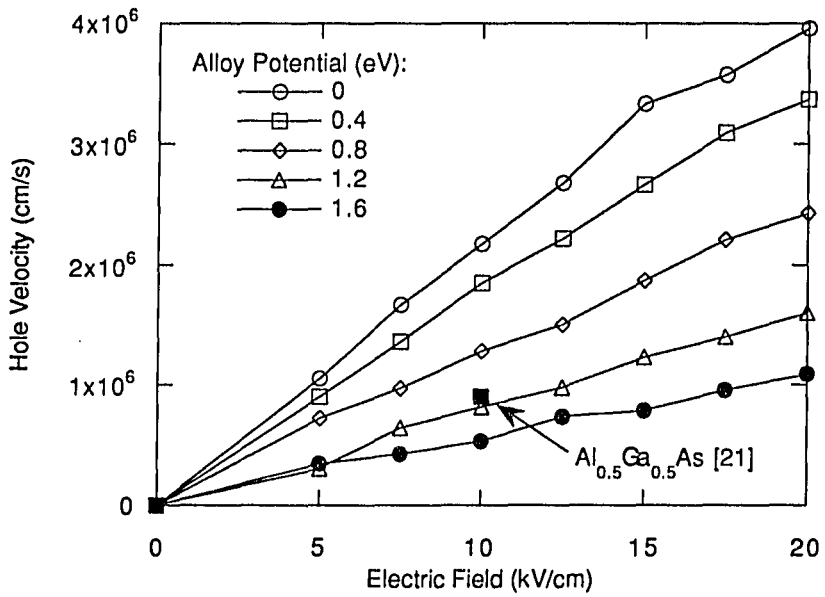

Figure 2.24: Hole velocity versus electric field for $In_{0.52}Al_{0.48}As$.

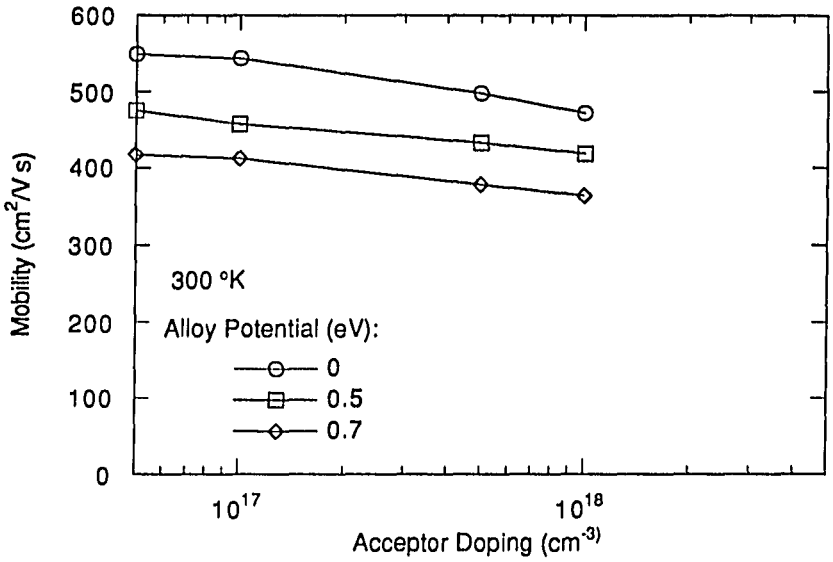

Figure 2.25: Hole mobility versus acceptor doping for $GaAs_{0.51}Sb_{0.49}$.

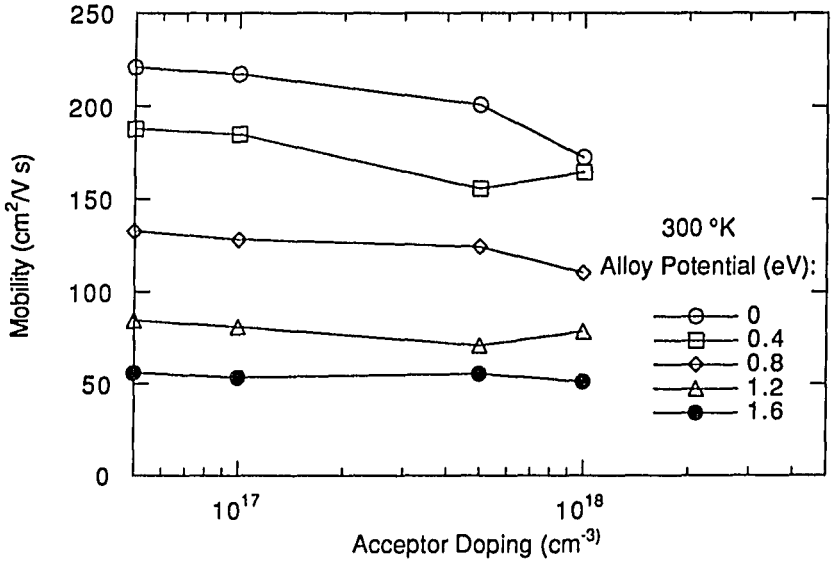

Figure 2.26: Hole mobility versus acceptor doping for $In_{0.52}Al_{0.48}As$.

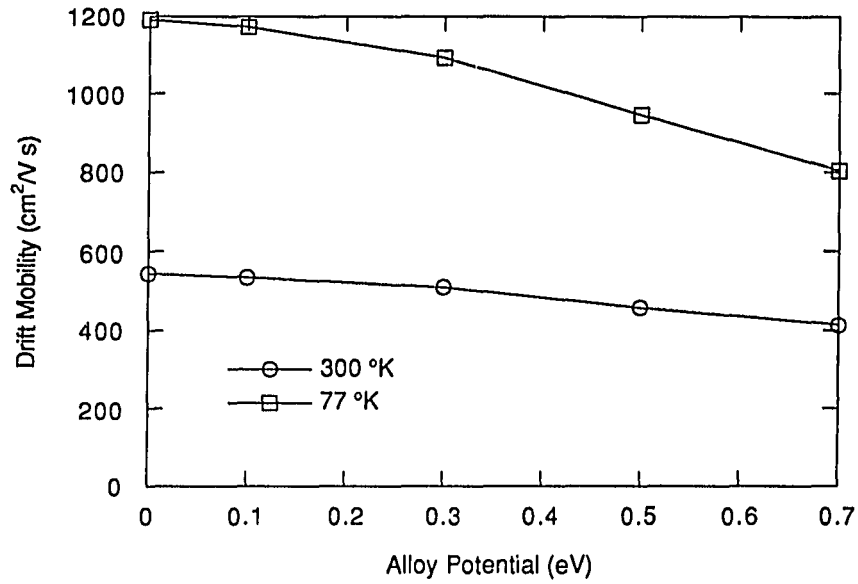

Figure 2.27: Hole mobility versus alloy potential for room temperature and liquid nitrogen temperature for $GaAs_{0.51}Sb_{0.49}$.

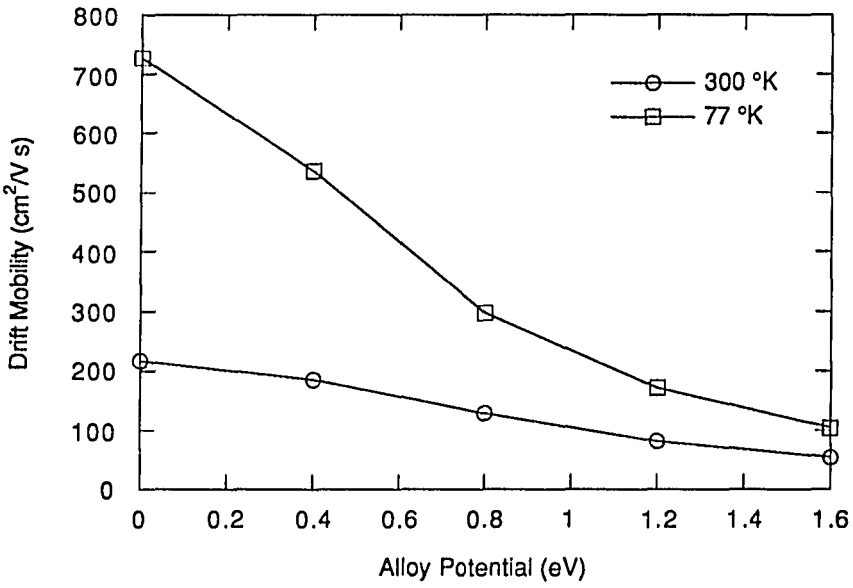

Figure 2.28: Hole mobility versus alloy potential for room temperature and liquid nitrogen temperature for $In_{0.52}Al_{0.48}As$.

the effect of alloy scattering is much more pronounced at the lower temperature.

This Monte Carlo simulation has shown that $GaAs_{0.51}Sb_{0.49}$ and $In_{0.52}Al_{0.48}As$, have hole transport properties superior to the GaAs/$Al_xGa_{1-x}As$ system. This result validates the motivation for pursuing this system to increase transconductance through higher hole mobility in the channel material. However, this result needs to be realized experimentally through high-quality epitaxial layers.

2.2: MEASURING THE $GaAs_XSb_{1-X}/In_YAl_{1-Y}As$ VALENCE BAND-EDGE DISCONTINUITY

Recently, there has been a marked increase in interest in the InAlAs/GaAsSb heterojunction for device applications including both heterojunction bipolar transistors (HBTs) and heterojunction insulated gate field effect transistors (HIGFETs). This interest exists largely because of some anticipated properties of the heterojunction, particularly its valence band edge discontinuity. Based upon their individual properties, a relatively large value has been predicted for this quantity on the order of 0.4 eV [16]. Such a relatively large value (the $Al_{0.3}Ga_{0.7}As$/GaAs system has a discontinuity of only 0.14 eV [61]) would be quite valuable as a barrier for holes in many types of devices. Recently there was an attempt to determine the discontinuity experimentally by using it as a fitting parameter for matching photoluminescence data to a model of a double heterojuntion as a potential well [21]. While such an approach is certainly better than having no experimental evidence, it is preferable to design an experiment to find the discontinuity more directly. This value was measured in a more unambiguous manner by using the activation energy of a single-barrier diode near room temperature.

In this study, one such method has been used and applied to InAlAs/GaAsSb nominally lattice-matched to InP. The method chosen is that used recently by Sugiyama et. al. to determine the conduction band edge discontinuity of InGaAs/GaAsSb lattice-matched to InP [22]. In this method, a single barrier heterojunction diode is grown and the measured activation energy of the diode is extrapolated to equilibrium conditions to find the band-edge discontinuity. This approach has the advantage that very little information of the specific structure need be known (i.e., the results of the measurement are independent of the details of the structure).

In particular, this method takes advantage of the fact that, near room temperature, a single-barrier diode with a barrier width large enough to make tunneling current negligible will be

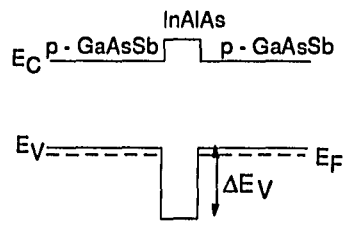

Figure 2.29: Schematic band diagram for single barrier diode.

dominated by thermionic emission current. That is, the current density is given by [62],

$$J = A^* T^2 \exp\left[\frac{-q\,[\,\Delta E_V - (E_V - E_F)\,]}{k_B T}\right]\left(1 - \exp\left[\frac{-q\,V}{k_B T}\right]\right) \qquad (2.22)$$

where A^* is the Richardson constant, E_V-E_F is the Fermi energy level measured from the valence band edge, q is the electronic charge, T is the absolute temperature, V is the applied voltage, and k_B is the Boltzmann constant. Thus, if an Arrhenius plot ($\log[J/(A^*T^2\exp((E_V-E_F)/k_BT)(1-\exp(-qV/k_BT)))]$ versus $1/T$) is made, the activation energy gives ΔE_V for the applied voltage. If thermionic emission is the only carrier transport mechanism, then the resulting discontinuity will be independent of bias. A schematic energy band diagram is shown in Figure 2.29.

As mentioned above, this approach minimizes the number of parameters of the system that must be known in order for a calculation to be made. In contrast to other methods, this approach requires only that the doping density of the diode regions near the barrier and the temperature at which measurements are made be known. Since the activation energy comes from the slope of the Arrhenius plot rather than the absolute values, constants such as diode area and the Richardson constant do not affect the calculated values of the discontinuity. In fact, even the assumed doping density has little effect on the result since it only enters the calculation through the Fermi integral for the quantity E_V-E_F. These attributes make this particular method especially appropriate for materials systems such as this one where many physical parameters are not well-known.

The material used in this study was grown in a modified Varian Gen II MBE chamber and doped

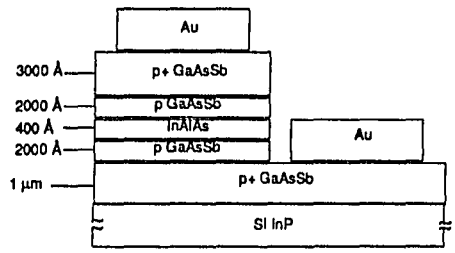

Figure 2.30: Single-barrier diode heterostructure for activation energy measurement of discontinuity.

in situ with beryllium. All growths were performed at the Solid State Electronics Directorate of Wright Laboratory, Wright-Patterson Air Force Base, Ohio by Eric Taylor under the direction of C. Edward Stutz. Material composition was calibrated by x-ray diffraction data, performed by A.K. Rai of Universal Energy Systems, Fairborn, Ohio, and doping densities were calibrated by Hall-effect measurements made by Tim Cooper under the Direction of Dr. David Look, Wright State Univeristy, Fairborn Ohio. The nominally lattice-matched material was etched using a H_3PO_4:H_2O_2–based solution described in Chapter 3, and evaporated Au/Zn/Au was used for ohmic contacts. A schematic of the finished structure is shown in Figure 2.30.

Following fabrication, the diodes were diced and packaged for testing. A sample current-voltage curve of a diode at room temperature is shown in Figure 2.31. The asymmetry of the curve is attributed to the large difference in the current paths.

The test set-up consisted of a Hewlett-Packard HP4145B Semiconductor Parameter Analyzer connected directly to the device under test (DUT). The DUT was, in turn, placed in a Thermotron temperature chamber which was temperature regulated by thermocouple. Currents were measured for applied voltages of 30 mV, 60 mV, and 100 mV at temperatures between 300 K and 400 K. A sample Arrhenius plot is shown in Figure 2.32.

The activation energy was obtained from a least-squares fit of the plot to a straight line. The measured activation energies were found to be quite linear with respect to the applied voltage rather

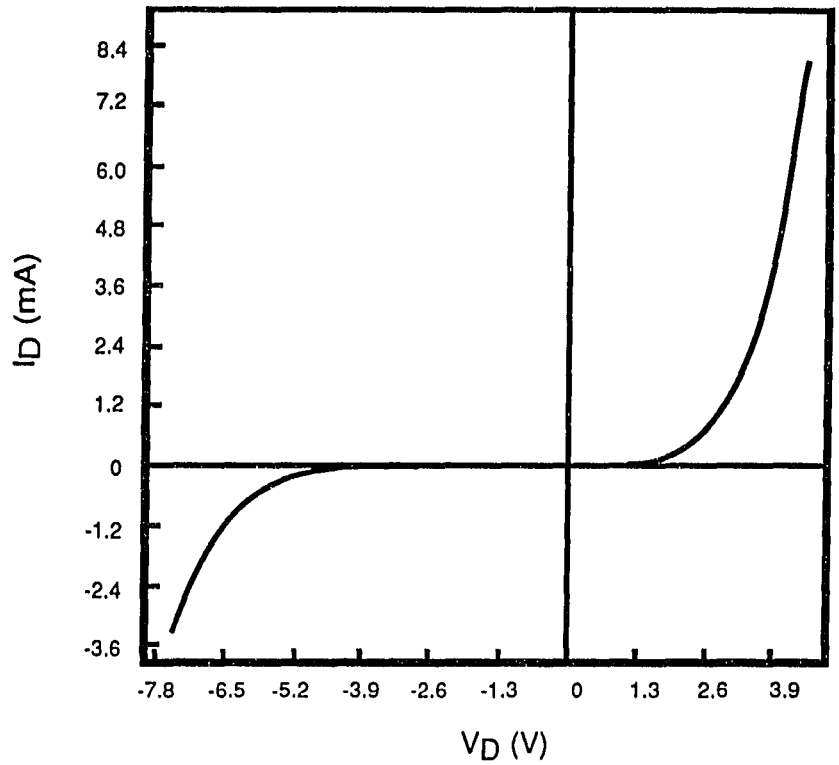

Figure 2.31: Current-voltage characteristics of heterojunction diode.

than constant. While other workers speculate that a Schottky effect is responsible for this bias dependence [22], we have found no evidence to support this theory since there is no rectifying behavior for the ohmic contacts. However, it is possible that a secondary current transport mechanism is active and that this mechanism may be tunneling through the barrier layer via deep levels in the InAlAs. In any case, there is a dependence on bias level which can be removed by extrapolation to zero bias (equilibrium).

The equilibrium valence band edge discontinuity was thus found to be 640±20 meV. Since the gate leakage current of heterojunction field-effect transistors (HFETs) has a negative exponential dependence on this discontinuity, using the GaAsSb/InAlAs heterojunction in place of the GaAs/AlGaAs heterojunction could result in a reduction by many orders of magnitude in this important

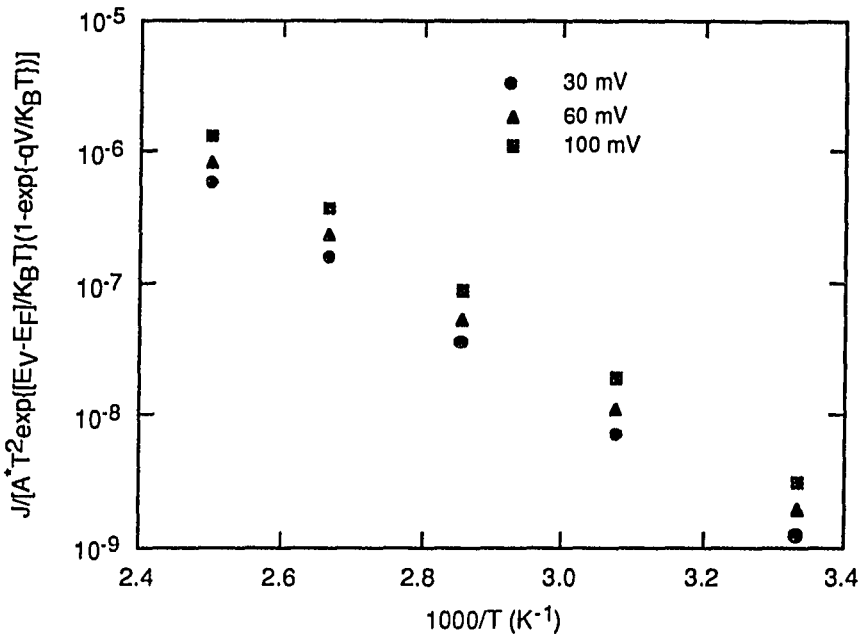

Figure 2.32: Sample Arrhenius plot for heterojunction barrier diode.

device parameter. Indeed, this is the largest known valence band-edge discontinuity that has been measured. An example of an extrapolation to equilibrium is shown in Figure 2.33.

This result compares quite favorably with two independent results from fitting to photoluminescence data [21, 63] and confirms the very low leakage currents found from this heterojunction in HFETs [11], though it is higher than previously predicted values [16].

The results of this study show that, near room temperature, the current does exhibit an exponential dependence on the inverse temperature and the activation energy of this behavior is not strongly dependent on any parameter of the system except the band edge discontinuity. It has further been shown that for small applied voltages, the activation energies have a linear dependence on this voltage which can be extrapolated to an equilibrium value for no applied voltage. It has been established also that the calculated equilibrium value of 640 meV ±20 meV agrees well with modeled values and with experimentally observed trends. It is therefore reasonable to believe that this result

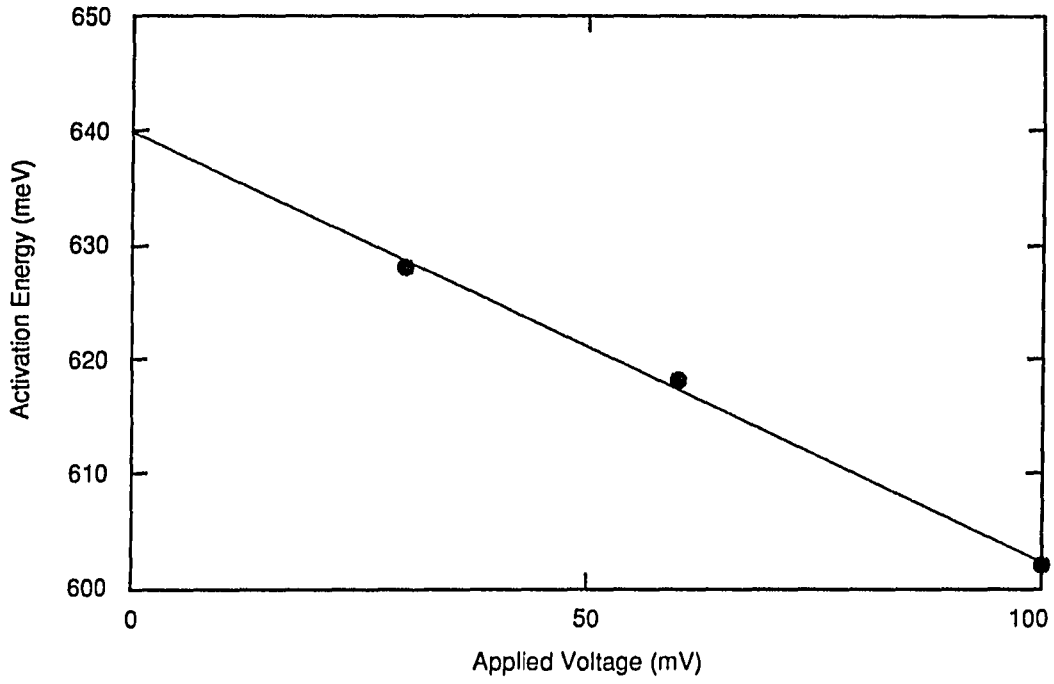

Figure 2.33: Example of extrapolation to equilibrium of activation energy.

can be used with a high degree of confidence by device designers and that it demonstrates the tremendous potential of this heterojunction for use in advanced device design.

3: PROCESS DEVELOPMENT

Even the most promising materials system is not without its difficulties, and the $GaAs_ySb_{1-y}$/$In_xAl_{1-x}As$/InP system is no exception. The chief problem is that of a general lack of information on its electrical, mechanical, and chemical properties. Though the first of these was addressed in part in the Chapter 2, it is necessary to know some of the mechanical and chemical properties, as well as certain of its electrical properties, before it is possible to perform the tests described previously. More specifically, it essential to have a basic set of reliable fabrication processing steps available before it is feasible to create the structures required for those tests as well as finished devices. The minimum requirement is three basic processing steps: mesa isolation etch, ohmic contact formation, and Schottky contact formation.

3.1: PROCESS DEVELOPMENT CONCEPTS FOR $GaAs_xSb_{1-x}$ AND $In_xAl_{1-x}As$ STRUCTURES

For materials such as silicon and gallium arsenide, there are numerous methods for performing such processing, each with its own set of advantages and disadvantages. However, most of these do not transfer directly to other materials systems. For example, though Au/Zn/Au makes p-type ohmic contacts to both GaAs and $GaAs_xSb_{1-x}$, the two materials require different alloying temperatures for the contacts and the addition of the heterojunction with $In_xAl_{1-x}As$ complicates matters further still. While this lack of information does not mean that solutions do not exist, it does mean that a bit of experimentation and optimization is required before a reliable, repeatable process is available to form the desired structures.

Since one of the first steps in most processes is isolation, this is a logical place to begin. For compound semiconductors, there are two standard methods used, mesa and implantation isolation,

both of which assume that the substrate is semi-insulating (a reasonable assumption for either GaAs or InP substrates). Mesa isolation is simply the removal of material that is not semi-insulating between active regions by some type of etching, eliminating any conduction paths. This process naturally leaves the surface of the wafer very non-planar, complicating further processing (this effect may be mitigated by refilling the etched areas with some insulating material, though this adds substantial complexity to the process). Implantation isolation implants some species such as oxygen which create dislocations and traps with states in the banddgap which greatly increase the resistivity of the material between active regions. This method has the advantage of not changing the planarity of the surface, but has the disadvantage of being more complex in its implementation and development and of producing generally inferior isolation.

For initial experiments, mesa isolation was chosen for its relative simplicity and its effectiveness. Having made this choice, it is necessary to choose between wet chemical etching and dry reactive ion etching. In this case, we choose to start with wet chemistry because it is ordinarily easier to realize and to experiment with because of the ease with which new reagents may be tried. This still leaves a great variety of choices for the chemistry. This is because etching solutions are typically a combination of an acid and a base diluted by water designed so that the base oxidizes the exposed semiconductor and the acid removes the oxide. Further variations may be achieved by modifying the ratio of the reagents and water which varies the etch rate and may change a diffusion-limited reaction to a reaction-rate limited reaction or vice-versa. It is clear then that a bewildering number of choices are available given the number of commonly available acids and bases. Indeed, Williams lists a rather large number of standard solutions [64] that only begins to indicate what is possible.

To limit our choices to a number that is more manageable, we must realize that a great deal of work has been done in the GaAs system and some work has been done in the GaSb system and it may be possible to use similar solutions simply by characterizing their behavior in the system of interest. That is, though we know that etch rates will almost certainly be different, as long as the

etchants leave a clean, smooth surface we only need to know what the actual etch rates are in our system. Therefore, two etching solutions were selected for examination: $HF:H_2O_2:H_2O$ and $H_3PO_4:H_2O_2:H_2O$ tartrate. The HF-based solution was selected based upon its reputation in GaAs-based systems for having an etch rate that is not very dependent upon material when mixed in the proper proportions [65]. The H_3PO_4-based solution was selected because it has been shown to be a reliable and repeatable etchant for GaSb [66].

To characterize these etchants in a simple and direct fashion, simple layers of $GaAs_xSb_{1-x}$ and $In_xAl_{1-x}As$ were grown with a range of doping levels representing actual expected levels. Then we etch simple patterns on the samples in solutions mixed in a set series of ratios and for different durations. The range of solution ratios is initially chosen to be a set of two (1:1:8 and 1:1:38 (acid:base:water)) based on commonly used ratios. The range of times is chosen to be 10 s, 30 s and 100 s (if the thickness of the grown layer will allow), with temperature of the solution and time from mixture strictly controlled. The measured etch depths from this combination of experiments should provide a crude but useful picture of the etching characteristics of the solutions including dependence on doping of the material, constancy of the etch rate with etch time, and dependence on composition of the etching solution. This, combined with scanning electron microscopic examination of the etched surfaces, provides a first order estimate of the suitability of the solutions for mesa isolation processing.

Development of an ohmic contact process is a much simpler matter than finding a good etching recipe since the metal system has already been identified (Au/Zn/Au). All that is left, then, is to optimize the alloying step for the equipment being used. In other words, though temperature measurements differ from setup to setup, it is sufficient to find the optimum *indicated* temperature for a given piece of equipment (e.g., a furnace).

To accomplish this, we take samples from a wafer with the appropriate layers to simulate the final structure and pattern the ohmic metal in test structures. For our test structure, we use a

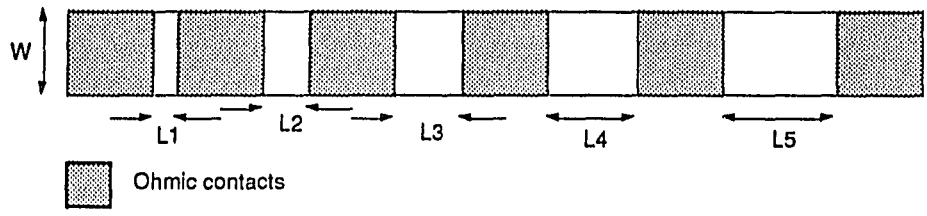

Figure 3.1: Ohmic contact test pattern.

commonly employed pattern in which an isolated strip of material has ohmic contacts of a specific width, w, but separated by increasing distances [67], as shown in Figure 3.1. In such a structure, current must flow between the contacts and the resistance seen by the current is given by

$$R = 2R_c + \frac{R_{sh}}{w} L, \tag{3.1}$$

where R_c is the contact resistance, R_{sh} is the sheet resistance between the contacts and L is the contact spacing (resistance of the measuring equipment must be already accounted for). This gives a linear dependence of R on L. If R is measured with a varying L and R_{sh} is constant, a linear regression to a value of L=0 gives

$$R\,|_{L=0} = 2R_c. \tag{3.2}$$

Measuring the contact resistance, R_c, before and after different alloying steps allows one to find the optimum alloying conditions.

The development of suitable Schottky contacts is often much less straightforward than that of ohmic contacts. The problem here is that the operation of Schottky contacts is very sensitive to the details of the surface to which they make contact. In an ideal case, the Schottky barrier is determined by differences in work function between the metal and semiconductor. However, if the semiconductor has a large number of surface states (as does GaAs), the Fermi level of the semiconductor becomes "pinned" by the surface states, rendering the Schottky barrier virtually independent of the metal used [62]. It is notable that such a barrier is still usable and is indeed used in commercial GaAs MESFETs. Nonetheless, even barriers such as these require careful preparation during fabrication

to insure that a fresh, clean surface is available for the contact. This may require back-sputtering of the wafer just prior to sputtering on metal or a dip in an etchant to remove any surface oxides.

The details, of course, depend upon the composition of the exposed surface. Therefore, it is required that when a new materials system is encountered, that a surface preparation be identified for Schottky contacts. It is not clear what density of surface states is to be expected for $GaAs_xSb_{1-x}$ or $In_xAl_{1-x}As$, but it seems likely that the alloys will behave differently from GaAs. To avoid a lengthy theoretical study at such an early stage, one may simply try a number of surface preparations that are known to work in other systems in hopes that one or more of these will yield satisfactory, though not necessarily optimum, contacts.

In this case, one still needs a figure of merit with which to judge to quality of the contacts. The simplest and perhaps most straightforward figure of merit is the ideality factor, n, as defined by [62]

$$J = J_0 \exp\left[\frac{-q\,(V_{bi} - V)}{nk_BT}\right], \tag{3.3}$$

where J and J_0 are the current density and the reverse saturation current density, respectively, T is temperature, k_B is the Boltzmann constant, q is the electronic charge, V_{bi} is the built-in voltage, and V is the applied junction voltage. (As the name implies, the ideality factor indicates how well the junction approximates an ideal one and the closer n is to one, the better the junction is generally considered to be.) Therefore, n may be found from the slope of the current density versus voltage curve by

$$\ln (J) = \ln (J_0) + qV/nk_BT, \tag{3.4}$$

over a range of voltages, where q/nk_BT is the slope for a semilog plot [67]. Using this, a satisfactory Schottky contact process may be found by selecting the preparation technique that gives n the closest to one.

Candidates selected for these steps include a buffered $HF:H_2O$ dip, a deionized water rinse, and a $H_2O_2:H_2O$ dip followed by a buffered $HF:H_2O$ dip. This selection completes the set of basic process

steps needed for characterization and device fabrication. It must be noted, however, that even minor steps in processing can present unforeseen problems. For example, certain photoresist developers have been found to etch GaSb and Microposit® 1165 photoresist remover has been found to etch $GaAs_xSb_{1-x}$ at an unacceptable rate. While all individual steps in structure processing have been screened for such effects, it is worthwhile to note that using a new process from GaAs technology is not necessarily a simple task. The details of fabrication steps used are given below.

3.2: RECESSED GATE PROCESS

Whatever the motivation for choosing a certain material system, fabrication of devices in a new system requires an inescapable amount of process development before any results may be seen. As a minimum, three basic steps are necessary to fabricate a III-V field effect transistor or virtually any other solid state device. These steps are device isolation, ohmic contact, and a non-ohmic or Schottky contact. If the materials to be used are well-established, it is typically not difficult to find suitable existing fabrication process or parts of processes. However, a process optimized for materials such as GaAs is not likely to be suitable for a different material system because of unexpected chemical interactions or different physical properties such as susceptibility to oxidation.

3.2.1: ISOLATION AND GATE RECESS

Device isolation is typically achieved by one of two methods for compound semiconductors. In the first method, ion implantation, one or more species of ion is implanted between active device areas to create damage or traps and recombination centers. However, for materials with relatively small bandgaps such as $In_xGa_{1-x}As$ or $GaAs_xSb_{1-x}$, isolation better than a few kΩ is seldom achieved.

A much more reliable method is mesa isolation. In this method, areas surrounding devices are etched down to a semi-insulating substrate or buried epitaxial layer, leaving devices on top of mesas. Isolation on the order of MΩs is routinely achieved with this method. A possible drawback of this method, when used for heterostructure FETs, is that the gate finger may lie across the channel layer on the sides of the mesa, which can drastically reduce the breakdown voltage of the device. This effect can be avoided if the etchant used selectively etches the channel material at a faster rate than adjacent layers so that the channel layer is recessed from the rest of the structure on the mesas [68].

The other possible drawback is the resulting non-planarity of the wafer surface which can reduce yield in a production environment. When merely showing the feasibility of a material system or a device technology, this is not a serious limitation since yield is not the primary consideration.

The attributes necessary for a successful isolation etching recipe are that it leave a clean and smooth surface and has a repeatable etch rate. In theory, these attributes may be attainable with either wet chemical etching or dry etching approaches. However, wet chemical etching is usually the first choice due to its relative simplicity and the enormous range of possible etching solutions.

As described earlier, two candidate solutions are $HF:H_2O_2:H_2O$ and $H_3PO_4:H_2O_2:H_2O$:L-tartaric acid. Experiments were initially conducted using solution ratios of 1:1:8 and 1:1:8:0.4, respectively, to compare relative etch rates, etched surface morphologies, and edge profiles of mesas. For these experiments, the solutions etched homogeneous layers of $GaAs_{0.51}Sb_{0.49}$ and $In_{0.52}Al_{0.48}As$ both undoped and p^+. The resulting mesa step heights were measured using a Sloan Dektak IIa profiling tool. For each sample, measurements were taken at three locations and averaged. Etches were performed for 10 s and 100 s to determine linearity of etch rates. Surface morphology was examined by optical and scanning electron microscope. The result of these examinations was that $HF:H_2O_2:H_2O$ was quickly rejected as a candidate, although observed etch rates were very consistent. This solution was found to be sensitive to doping level, complicating the isolation procedure. The solution also left a soft film on the etched surface that was not soluble in water (likely an Sb oxide) and large (1 μm or larger) pieces of debris, making it unsuitable for the process.

The $H_3PO_4:H_2O_2:H_2O$:L-tartaric acid solution produced much better results. In this solution, the L-tartaric acid dissolves Sb oxides on the wafer surface. Etch rates were very reproducible and provided a selectivity of 2:1 for $GaAs_{0.51}Sb_{0.49}$ over $In_{0.52}Al_{0.48}As$ independent of doping. This selectivity results in the $GaAs_{0.51}Sb_{0.49}$ being etched faster than the surrounding material, producing a recess on the mesa sidewall. Furthermore, the etch produces a microscopically smooth and clean surface with sloped mesa edges suitable for good step coverage of metals. The etch rate

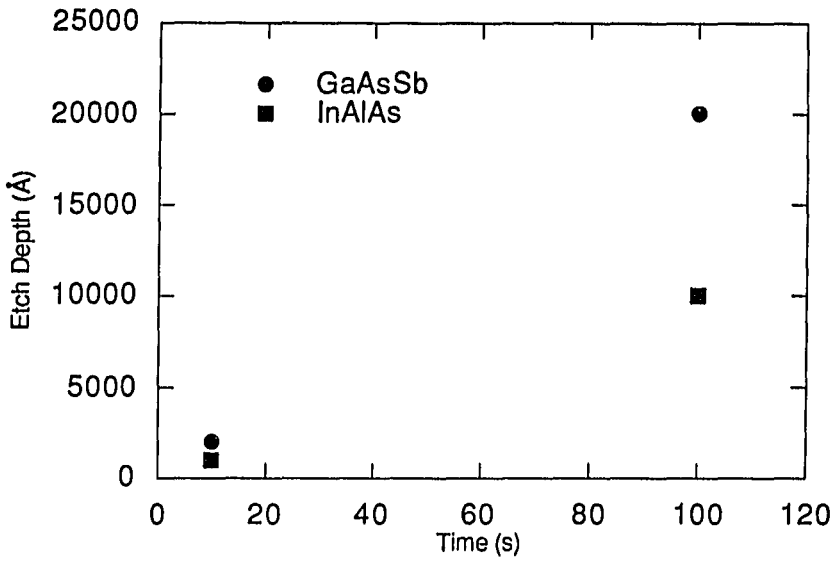

Figure 3.2: Etch depths for $GaAs_{0.51}Sb_{0.49}$ and $In_{0.48}Al_{0.52}As$ in H_3PO_4:H_2O_2:H_2O:L-Tartaric Acid (1:1:8:0.4).

was found to be constant with etch time as shown in Figure 3.2 with etch rates of approximately 200 Å/s for $GaAs_{0.51}Sb_{0.49}$ and 10 nm/s for $In_{0.52}Al_{0.48}As$. These rates are quite suitable for controlling typical mesa etches of 100 nm or more. However, such rapid etch rates are definitely not suitable for a gate recess of 50 nm which is much more critical to device performance. A solution with a lower etch rate is necessary for this step, so a solution with ratios of 1:1:32:0.4 was tested. The etch rates were found to scale with the dilution of the solution and final rates were 5.5 nm/s for $GaAs_{0.51}Sb_{0.49}$ and 2.5 nm/s for $In_{0.52}Al_{0.48}As$ (100 s etch). Etching the solution for double the time resulted in slightly smaller etch rates. Subsequent use of this solution in actual gate recess processes validated the effectiveness of this solution and the measured etch rates. A shelf test was also performed to measure the degradation of the etching solution after being mixed. No change in etch rate was found after 20 additional minutes of waiting with the solution covered; this allows ample time to perform the etch.

3.2.2: OHMIC CONTACT

For non-implanted contact regions, there is basically only one method commonly used for p-type ohmic contacts. That method is evaporated layers of Au/Zn/Au that are alloyed at high temperature to allow Zn to diffuse into the contact region and through the barrier layer so that the resultant degenerate doping allows a good ohmic contact as described earlier. In this system the first Au layer is to promote adhesion to the wafer surface and the top Au layer is simply for high conductivity and for wire bonding, if necessary. Typical thicknesses are 5 nm Au, 20 nm Zn and 250 nm Au.

The question, then, is what is the optimum time and temperature for alloying the contacts? A typical alloying process achieves a minimum contact resistance for a particular temperature/time combination with contact resistance increasing dramatically for higher temperatures and longer times. For GaAs, this combination is 370 °C for 30 s, but alloying contacts to $GaAs_{.51}Sb_{.49}$ this way produces very high contact resistance, indicating that a lower temperature or shorter time is appropriate. Experiments show that contacts to p^+ $GaAs_{0.51}Sb_{0.49}$ are best for an alloy at 250 °C for 30 s, though this does not necessarily apply to the heterostructure device since $In_{0.52}Al_{0.48}As$ is also present. Since 250 °C is easily obtained with a typical bench hot plate, time was used as the variable to produce a simple and efficient alloying process.

In this experiment, the ohmic test pattern of Figure 3.1 was used on actual device structures which occurs 14 times in each die. For the test, 5 die were tested on a wafer at each step and spacings were measured using scanning electron microscopy. The results for all patterns with linear regression correlation coefficients of greater than 0.99 were averaged. The same die were used for all tests. There was a great deal of variation in the contact resistances and lateral diffusion of the Zn was actually visible in the samples with the most pronounced effects for the longer times. Since there was little difference in the actual contact resistance for 50 s alloy versus 30 s alloy, an alloying

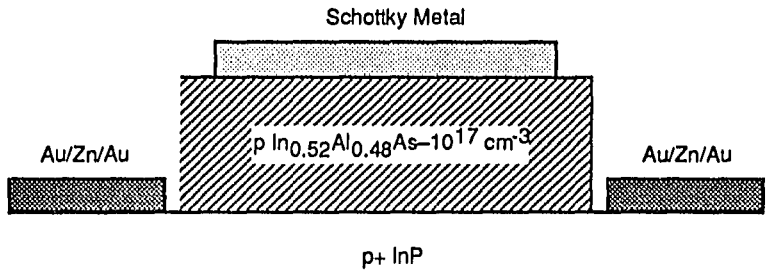

Figure 3.3: Structure for measuring Schottky barrier height to p-$In_{0.52}Al_{0.48}As$.

time of 30 s was chosen to minimize the effects of lateral diffusion.

3.2.3: SCHOTTKY CONTACTS

With the possible exception of the gate recess, the Schottky contact is the most critical step of the device process. A leaky or noisy gate contact will easily ruin an otherwise outstanding transistor. However, the physics of surfaces are a very complicated matter, not well understood for arbitrary materials [65]. Since there are any number of metals that may be used for such contacts, those most commonly used for other semiconductors were selected. Three of the most common are Al, Ti/Au and Au. To examine the actual attributes of p-type Schottky contacts to $In_{0.52}Al_{0.48}As$, an experiment was necessary.

In this experiment, a Schottky diode was fabricated from an $In_{0.52}Al_{0.48}As$ structure as shown in Figure 3.3. Three different pre-metal treatments were used in an attempt to minimize surface states at the interface. Schottky barriers were measured by the common capacitance-voltage method [62] and the ideality factor was calculated from current-voltage characteristics. The resulting Schottky barrier heights and ideality factors are shown in Table 3.1. These results indicate that all the metals have acceptable ideality factors and there is no clear effect on ideality factor by the pre-metal treatment. All metals show relatively high Schottky barriers with Au clearly the

Table 3.1: Schottky barrier heights and ideality factors for candidate metal and cleaning steps.

	Schottky barrier (eV) and (ideality factor)		
Pre-metal treatment	Au	Ti/Au	Al
No Dip	0.836 (1.061)	0.922 (1.032)	0.956 (1.153)
15 s Buffered Oxide Etch (BOE)	0.878 (1.027)	0.932 (1.092)	0.956 (1.074)
15 s BOE and rinse to > 10 MΩ-cm	0.819 (1.217)	0.997 (1.092)	0.987 (1.312)

lowest of the three. Ti/Au was chosen over Al since experience has shown that this system yields much greater reproducibility in gate characteristics. The buffered oxide etch (BOE) dip and water rinse was the obvious choice for pre-metal treatment due to the higher barrier.

3.3: SELF-ALIGNED GATE PROCESS

A self-aligned gate process has much in common with a recessed gate process. The obvious exception is that a different gate process is required. In order to withstand the high temperature of implantation and annealing, the gate must be fabricated from a refractory metal, silicide, or metal alloy such as tungsten (W), tungsten silicide (WSi), or titanium-tungsten (Ti/W). In addition, care must be taken to ensure that the implanted region is kept away from the gate edge, since this can contribute to gate leakage currents [69]. This requires a "T" gate or side spacers on the gate. A T gate approach was chosen because it offers the possibility of self-aligned ohmic metalization.

Since the rest of the device structure is self-aligned to the gate, the order of fabrication steps must be changed so that gate definition is near the beginning. To accomodate the electron beam definition of gate stripes, an alignment key is deposited first which includes special alignment marks for this lithography as well as the standard optical lithography alignment marks. Following the alignment key definition, a refractory metal was deposited on the sample and electron-beam lithography was used to define the foot of the T and a masking metal such as Au was evaporated onto the sample and the excess removed via a lift-off process. The refractory metal was then removed by reactive ion etching (RIE) tailored to selectively etch the refractory metal over the masking metal. In a similar fashion, electron-beam lithography was used to define the top portion of the T aligned to the bottom portion already in place. Use of two electron-beam lithography steps allows great alignment accuracy for the two portions of the gate and gives flexibility to change the dimensions of both the top and bottom of the gate. Once the T gate is formed, all remaining steps use conventional contact lithography starting with isolation of active areas by mesa etching. If implantation of impurities is necessary for ohmic contacts, it may be performed at this point, using the T as a mask for the contact regions and followed by an anneal. Ohmic metalization is then deposited by standard evaporation techniques with the top of the T again acting as a mask, allowing minimum spacing between gate

and source metalization. The final step is a metalization step that places bonding and probing pads and connects them to the ohmic and Schottky contacts. While this process is considerably more complex than the recessed gate process, it allows much greater uniformity and minimizes parasitic losses. The process is depicted schematically in Figure 3.4.

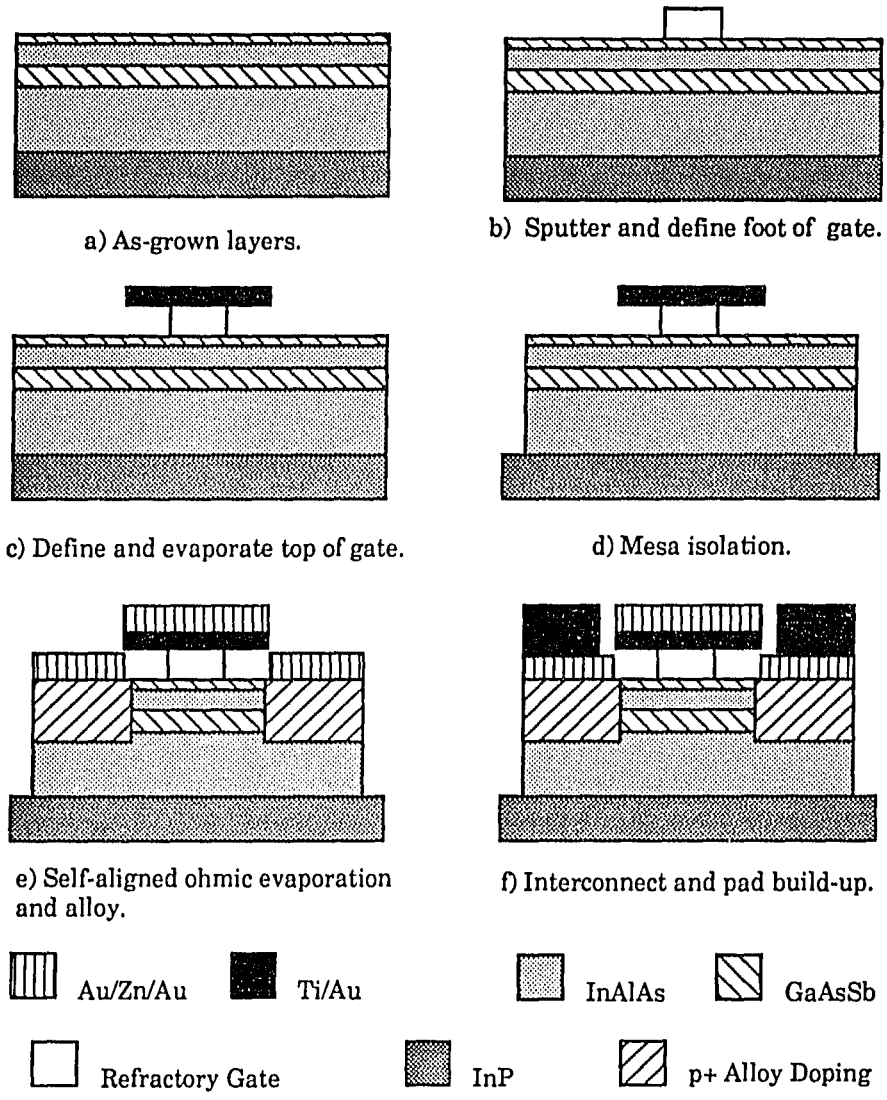

Figure 3.4: Self-aligned gate HIGFET process (an implantation step may be added before mesa isolation).

3.4: PHOTOLITHOGRAPHY

For the most part, basic lithography steps are selected more for the chemistry and temperature profiles they will see than the particular semiconductor materials they are used to define. There are some instances, however, in which the semiconductors themselves can be affected by the lithography process. Lithography of $GaAs_xSb_{1-x}$ is one such instance.

As a routine precaution, samples of $GaAs_xSb_{1-x}$ were immersed in various cleaning and developing solutions to examine the solubility of $GaAs_xSb_{1-x}$. Such a test found that Shipley SAL 101 photoresist developer used for polydimethylglutarimide (PMGI), a photoresist, and Shipley 1165 photoresist stripper, also used for PMGI, etched $GaAs_xSb_{1-x}$. A standard two-level resist process using PMGI was therefore out of the question.

A single-level resist process was then adopted using Shipley 1400-17 photoresist, Shipley 351 developer, and acetone and methanol for stripping and cleaning since none of these were found to etch the material. Devices fabricated using this lithography step, however, showed very high drain to source resistance as though the channel had been virtually removed, though it clearly had not. By closely monitoring electrical behavior during fabrication and varying developing times, the cause of this behavior was narrowed to the 351 developer. Though the nature of the reaction is still not clear, it was quite apparent that the developing solution rendered devices electrically inactive during the developing of the gate pattern. A new lithography process was obviously needed which would not allow 1165 stripper or 351 or SAL 101 developer to come in contact with the wafer.

An existing process was found which fit these requirements by replacing PMGI in the two-level process with polymethlymethacrylate (PMMA) photoresist. This resist is developed by chlorobenzene which, while unpleasant from a personnel safety perspective, does not affect electrical characteristics of $GaAs_xSb_{1-x}$. In this process, PMMA is first spun onto the wafer and baked to remove solvents and allow some planarizing reflow. 1400-17 resist is then spun onto the wafer and

also baked to remove solvents. The sample is then aligned and exposed by an ultraviolet source and developed by spraying 351:H_2O (1:5) onto a spinning wafer. Since this solution does not dissolve PMMA, the developer never comes in contact with the semiconductor. A short oxygen plasma etching step removes residual resist and any mixed interfacial layer that might have formed between the resist layers. This is followed by a blanket exposure by deep ultraviolet light. The sample is then developed by spraying chlorobenzene on the spinning sample. Chlorobenzene does not dissolve 1400-17 and the samples are intentionally overdeveloped in the final step to provide an undercut profile for consistent lift-off of metals. The dimensions in this process, then, are determined by the first exposure and development. Implementation of this process proved to be a crucial breakthrough for device fabrication. A schematic of the process is shown in Figure 3.5.

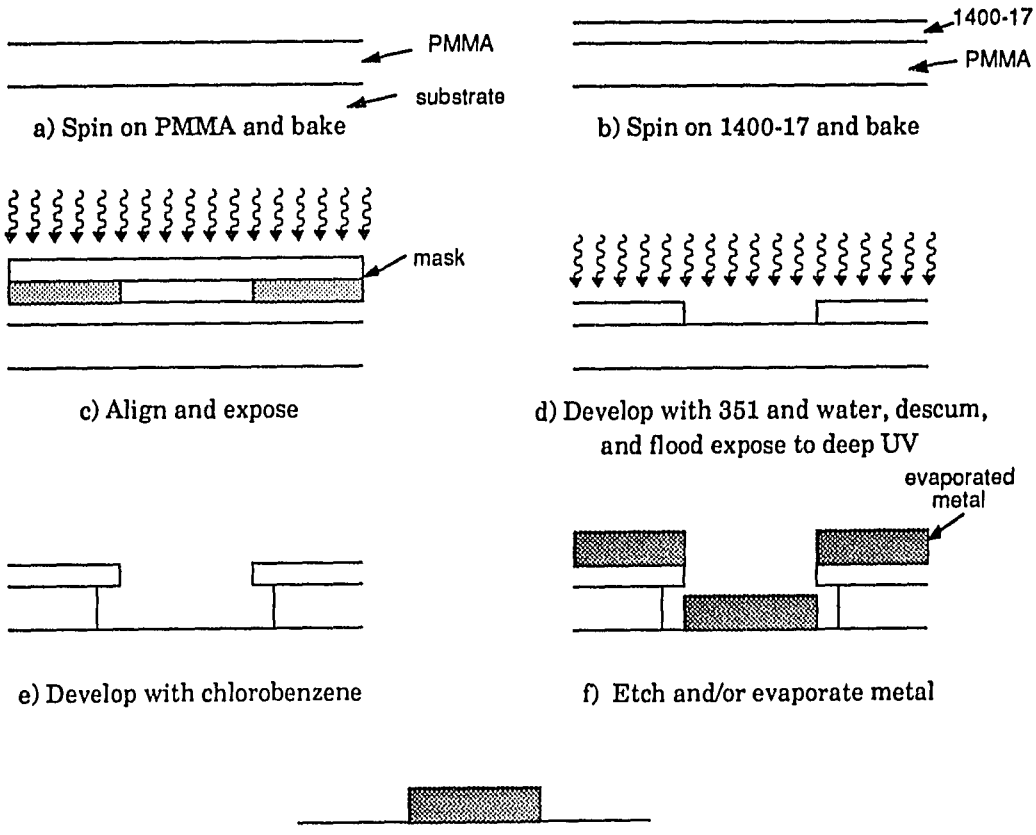

Figure 3.5: Schematic process flow for photolithography.

3.5: PROCESS DEVELOPMENT SUMMARY

In this chapter, processes for fabricating $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ devices were described and developed. First etching steps for isolation and gate recess steps were developed using $H_2O:H_2O_2:H_3PO_4$:L-tartaric acid which was found to have a selectivity of 2:1 for $GaAs_xSb_{1-x}$ over $In_yAl_{1-y}As$. Next, ohmic contacts using the Au/Zn/Au system were optimized for hot-plate anneal at 30 s. Then, Ti/Au was found to be the best approach for producing Schottky contacts to p-$In_yAl_{1-y}As$. Following this development, a process for fabricating self-aligned-gate devices was outlined. Finally the necessary changes in standard photolithography, required by the effects of standard developing chemicals on $GaAs_xSb_{1-x}$, were described including a two-level resist process which uses chlorobenzene as the final developer.

This completes the necessary process development for fabricating devices in a research environment. As stated previously, the processes used here may not be suitable for actual production of commercial devices but they suffice for a feasibility demonstration.

4: EXPERIMENTAL DESIGN AND RESULTS

Having completed the characterization of critical materials parameters and completed basic process development, these need to be implemented in working devices if the true potential of the technology is to be adequately explored. This task may be accomplished in two basic steps: a feasibility demonstration and first-order optimization. That is, one should first fabricate a device in the simplest, most direct fashion possible and extract basic performance parameters from it. One should then explore other fabrication approaches to overcome the principle weaknesses indicated from preliminary testing.

4.1: DESIGNING THE STRUCTURE

Many elements may be manipulated in the design of any compound semiconductor device; this is particularly true for the case of a heterostructure device employing ternary alloys such as the HIGFET under study. The most important variables that can be controlled during epitaxial growth are alloy composition for each layer, layer thicknesses, and doping level and species for each layer. Many device characteristics are affected by more than one variable (e.g., threshold voltage is influenced by all three), so trade-offs must be made.

4.1.1: OPTIMIZING MATERIAL COMPOSITIONS

Alloy composition affects many basic properties of a transistor. As mentioned in Chapter 1, there is a fundamental limit on the range of compositions that may be used, depending on the substrate material chosen – the lattice constant of the substrate. A mismatch between the lattice constant of the grown layer and the underlying layer may be accommodated by strain up to a limit determined

by the layer thickness. Beyond this limit (the critical thickness) dislocation defects relieve the strain and degrade the electrical properties of the material. Matthews and Blakeslee determined a relationship between critical thickness and lattice mismatch [70].

For the buffer layers which lay underneath the active device, electrical properties are not very important, these layers serve to separate the active layers from any surface defects on the starting material. This is generally accomplished by simply growing a relatively thick layer of a semi-insulating material such that defects starting at the original surface do not reach the grown surface. To aid in this, a strained-layer superlattice (SLS) is often grown near the surface of the buffer, because of evidence that such a structure inhibits the vertical progression of defects [13]. For this particular materials system, the SLS is composed of InGaAs and InAlAs since both are relatively easy to control. The remainder of the buffer is lattice-matched since the object is to reduce defects, not create them. Lattice-matching is achieved for the composition of InAlAs, which is semi-insulating when undoped.

The composition of the channel layer is more determined by desired electrical properties than by mechanical considerations. If an arbitrary thickness is desired, to control threshold voltage, for example, lattice-matched $GaAs_{0.51}Sb_{0.49}$ must be used. However, to minimize alloy scattering and maximize Sb content for highest mobility, a strained layer is chosen. For a typical channel thickness of 15-20 nm, the Matthews-Blakeslee relationship allows a composition up to 65% Sb ($GaAs_{0.35}Sb_{0.65}$) for a strained-layer. It should be noted that MBE growth of $GaAs_xSb_{1-x}$ has proven to be difficult. $GaAs_xSb_{1-x}$ is not miscible for the range of compositions that are of interest using equilibrium growth techniques, though the alloy may be forced by a non-equilibrium method like MBE. Transmission electron microscopy (TEM) has shown that such material is not randomly distributed, but appears to have a segregation of one of the constituent compounds; x-ray diffraction measurements display a great deal of dispersion which may also be attributable to clustering of the material [13]. If this is actually the case, the mobility of carriers in the material could be severely degraded

[39]. Furthermore, whereas $Al_xGa_{1-x}As$ composition can be easily controlled by maintaining an As overpressure and simply controlling the Al/Ga ratio, growth of $GaAs_xSb_{1-x}$ requires precise control of all three elements and is sensitive to substrate temperature [13]. A possible solution to this problem is to grow a strained-layer superlattice of GaAs and GaSb for the channel, which would also eliminate problems with alloy scattering.

The barrier layer and the cap-contact layer were chosen to be lattice-matched to minimize the possibility of dislocation defects and because carrier transport properties of these layers are not as critical to device operation.

4.1.2: DETERMINING LAYER THICKNESSES AND DOPING LEVELS

Having decided upon the compositions to be used, the thicknesses and doping levels must be determined for these layers. A typical buffer layer for a GaAs device on GaAs, which is naturally lattice-matched, is approximately 1 μm thick, without the SLS. However, the smallest deviation from lattice-matching composition will result in dislocations for such a thick layer, so the buffer here is reduced to 250 nm, without the SLS. All of the buffer except the top 50 nm is undoped to maintain semi-insulating properties. The topmost layer is lightly doped (10^{16} cm^{-3}) opposite the polarity of the channel layer to aid in pinch-off of the channel through the depletion region of the p-n junction.

The doping level of the channel itself is the most influential determinant of the threshold voltage just as it is for other FET types. The number of carriers in the channel that must be depleted by the potential from the gate establishes the threshold voltage. For $GaAs_xSb_{1-x}$, however, the situation is a bit more complicated than for Si. GaSb has a background acceptor level of approximately 10^{16} cm^{-3} and the most common donor impurity in compound semiconductors, Si, is amphoteric in $GaAs_xSb_{1-x}$, becoming an acceptor for the compositions of interest. Without introducing new impurities into the growth system, then, it is not possible to reduce the net doping level below the

background level. This is important because the large valence band-edge discontinuity creates a deep quantum well that must be empty at zero bias for enhancement-mode operation, and this is difficult to accomplish without very low doping. For the purposes of reproducibility, an acceptor doping level of 10^{17} cm^{-3} using Be was used in most experiments. A possibility for controlling the threshold is to increase doping the buffer layer to deplete the channel from below. The thickness of the channel for strained-layer devices is determined by the critical thickness, but a lattice-matched channel could have a wide range of thicknesses. The thicker the channel, the more difficult it is to deplete, so it is typically kept below 30 nm. Lacking a good quantitative theory for heterostructures, most such determinations are the result of experimental experience (trial and error). All growths and calibrations were performed at the Solid State Electronics Directorate of Wright Laboratory, Wright-Patterson Air Force Base, Ohio as described in section 2.2.

The barrier layer remains undoped, but its thickness determines gate capacitance, threshold voltage, and, indirectly, transconductance. Again, experience has shown that the best trade-off between a thin layer to keep the gate close to the channel for high transconductance and a thick layer allow for a small amount of overetch in processing and eliminate tunneling from the gate is about 30 nm. Because of this trade-off, there is little latitude for controlling threshold voltage by this layer thickness.

The cap layer exists primarily to improve alloyed ohmic contacts without requiring an implantation for the contacts. Therefore, this layer is doped as highly as possible with the acceptor Be resulting in a typical level of 10^{19} cm^{-3}. In principle, this layer could have any of a wide range of thicknesses, but 50 nm was chosen to keep the gate recess etch short yet keep the sheet resistance of the layer low. Composites of the starting structures are shown in Figures 4.1 and 4.2.

p^+ $GaAs_{0.51}Sb_{0.49}$	50 nm	Be: $1x10^{19}$
i $In_{0.52}Al_{0.48}As$	30 nm	
p $GaAs_{0.51}Sb_{0.49}$	25 nm	Be: $4x10^{17}$
n $In_{0.52}Al_{0.48}As$	50 nm	Si: $5x10^{16}$
InGaAs/InAlAs Superlattice	60 nm	
i $In_{0.52}Al_{0.48}As$	200 nm	

Figure 4.1: As-grown lattice-matched transistor structure.

p^+ $GaAs_{0.51}Sb_{0.49}$	50 nm	Be: $1x10^{19}$
i $In_{0.52}Al_{0.48}As$	30 nm	
p $GaAs_{0.35}Sb_{0.65}$	20 nm	Be: $4x10^{17}$
n $In_{0.52}Al_{0.48}As$	50 nm	Si: $5x10^{16}$
InGaAs/InAlAs Superlattice	60 nm	
i $In_{0.52}Al_{0.48}As$	200 nm	

Figure 4.2: As-grown strained-channel transistor structure.

4.2: EXPERIMENTAL APPROACH

Fabrication of an experiemental structure is best accomplished using a recessed-gate structure. In such an approach, all device layers are grown with in-situ doping and the appropriate layers are removed by etching to provide isolation and contact regions. A summary process flow is depicted in Figure 4.3. This process derives its name from the fact that the ohmic contact layer must be removed to provide a Schottky contact region for the gate, recessing the gate metal with respect to the ohmic contact metal. This particular step is also the principle weakness of the method as small variations in etch rate can cause relatively large variations in threshold voltage by placing the gate at different distances from the channel. In addition, insufficient etch depth will result in a poor Schottky contact and a possible drain-source short while excessive etching may remove the semi-insulating layer completely. These weaknesses are acceptable, however, in light of the relative simplicity of the process; no implantations or very high temperature anneals must be developed.

To optimize beyond the initial device results, it is necessary to characterize the performance of these devices. This is routinely accomplished through simple DC testing of devices and test structures using measuring equipment such as the Hewlett-Packard 4145B Semiconductor Parameter Analyzer. The battery of tests would typically yield standard transistor current-voltage curves, gate turn-on voltage, threshold voltage, contact resistance, source resistance, transconductance, and the drain saturation current.

The gate turn-on voltage is measured by connecting drain and source to ground and forward biasing the gate (a negative voltage for p-FETs) until a specified gate current level (e.g., 100 μA) is reached. Since HIGFETs obey a square-law in the saturation region similar to that for MOSFETs [60], with a constant drain voltage sufficient to assure operation in the saturated region, the square root of the drain current is plotted versus gate voltage and the straight line intercept with the voltage axis yields the threshold voltage. Contact resistance is measured as described in the previous

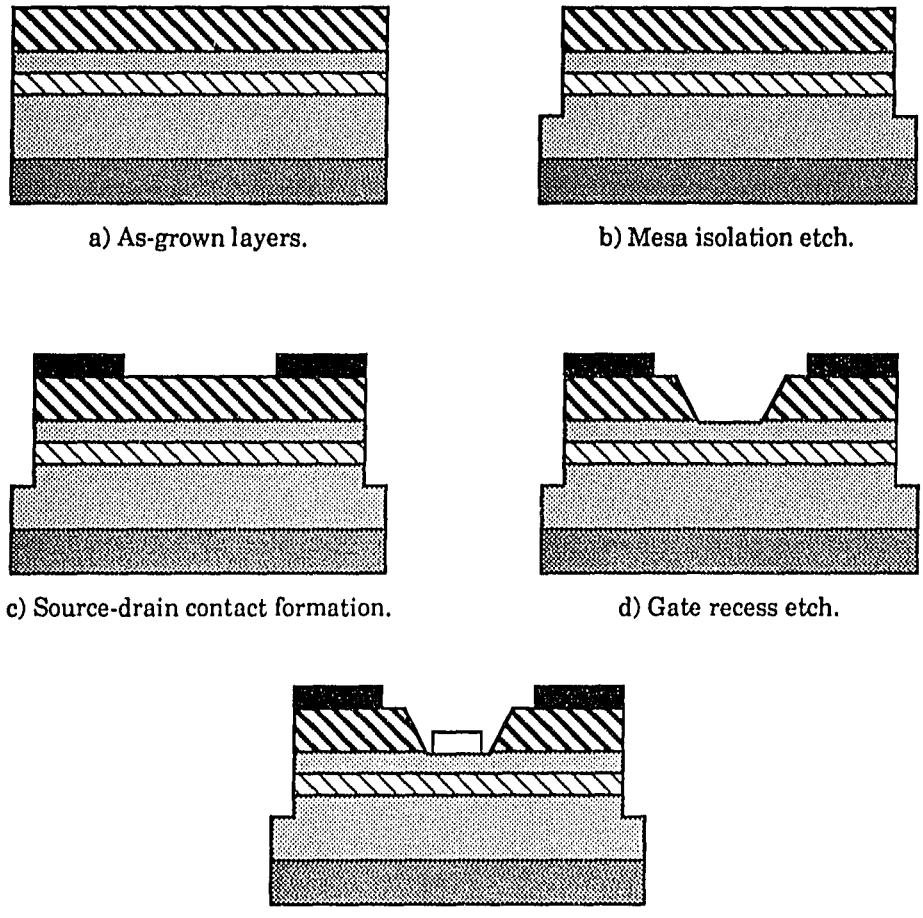

Figure 4.3: Recessed-gate HIGFET process.

section. Source resistance (the resistance between the source metal and the gate, an important parasitic) is measured by forcing current from the drain to source and measuring the gate voltage so the source resistance may be taken from

$$R_{source} = \frac{dI_d}{dV_g}, \quad I_g = 0. \tag{4.1}$$

Transconductance is found from equation (1.1) for a transistor operating in saturation. The maximum drain saturation current is simply the saturation current for a device with the gate biased at the gate turn-on voltage.

These tests help to point out limitations to a device's performance. For instance, a high source resistance will substantially reduce transconductance and drain current and the contact resistance measurement will indicate if this part of the device is the limiting factor. From these results, one may examine fabrication techniques and device structure to correct shortcomings. A full discussion of this topic is reserved for a later chapter when actual device results are examined.

The simplicity of the process notwithstanding, the gate recess process is far from optimum. The requirement of an alignment and etch for the gate step dictate a drain-to-source spacing that is larger than would otherwise be necessary, and the process tends to produce undesirably large variations in device properties, even on the same sample, because of variations in etching and in alignment. The solution to this for a first-order optimization is the same one used for silicon MOSFETs: a self-aligned gate (SAG) process [71].

In this process, the gate is formed first and serves as a mask for the source/drain contact implantation. In order to reduce gate-leakage current [69], a sidewall spacer may be formed on the gates to keep the implanted region from contacting the gate edges. An alternative is to form a "T" gate where the top portion shields the gate edges from the implantation. A summary of the process flow is shown in Figure 4.4. This process has the benefit of eliminating an alignment step and providing minimal source-drain spacing, but has the disadvantage of requiring significant additional process development. A SAG process requires a refractory gate formation process, a sidewall spacer process or "T" gate, and an implantation and anneal process. To take full advantage of the greater planarity of the SAG approach, an implant isolation process would be desirable, though not

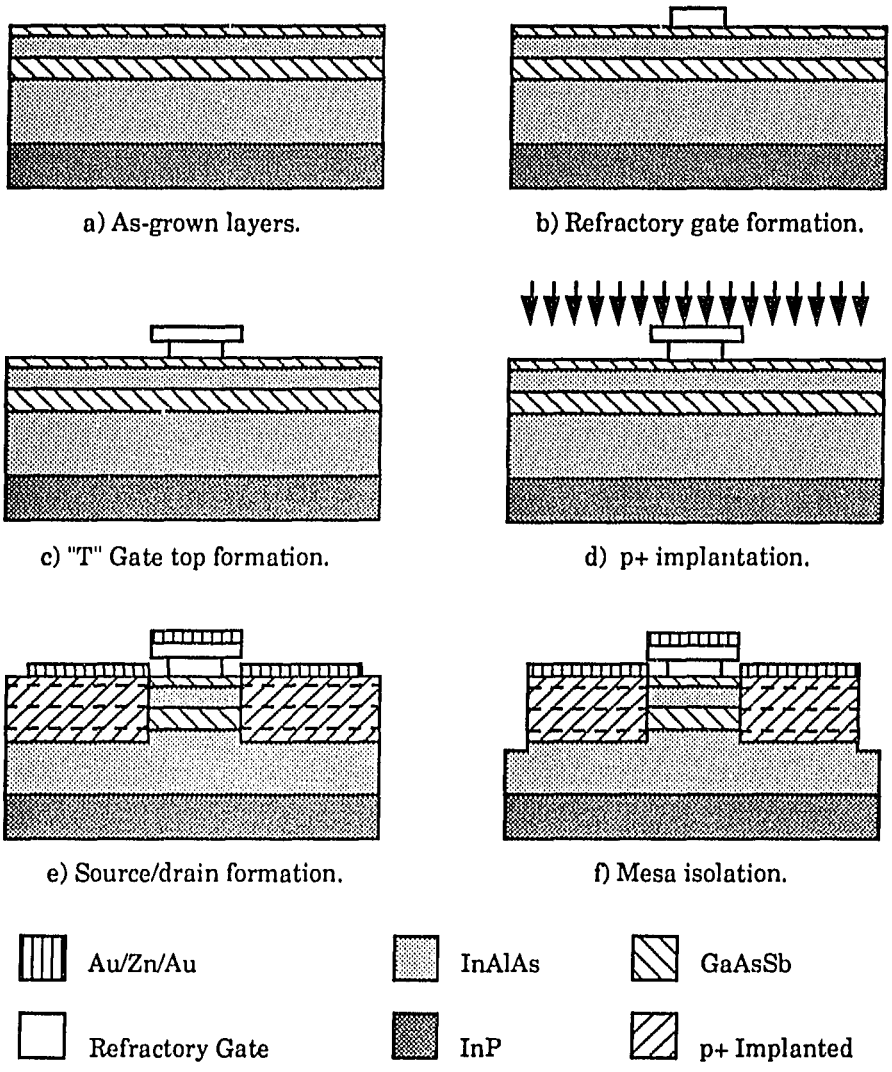

Figure 4.4: Self-aligned gate HIGFET process.

necessary.

Although the use of a SAG process can greatly improve performance, there is no reason one must limit oneself to changes in fabrication techniques for device improvement. For example, one might try using planar doping in the channel instead of uniform doping to further remove carriers from the ionized acceptors and improve mobility. A more drastic modification would be to change the

composition of the $In_xAl_{1-x}As$ and/or the $GaAs_xSb_{1-x}$ away from that needed for lattice-matching to InP. Such materials are often referred to as pseudomorphic materials. While this increases the possibility of dislocations in the material, there are still many reasons to consider such an approach.

The first of these reasons is the most obvious; a higher GaSb concentration in the channel should increase the hole mobility (neglecting alloy scattering). The second reason is quite similar; alloy scattering peaks for alloys with a composition of 50% of each constituent compound. Since the lattice-matching composition to InP is $GaAs_{0.51}Sb_{0.49}$, an increase of the Sb content will lower alloy scattering and raise the mobility even further. The final reason is that strain changes the band structure of solids, especially the valence band, and a non-lattice-matched material will be at least partially strained (not all of the strain will be relieved by dislocations). In particular, strain splits the degeneracy of the light and heavy hole bands causing more holes to occupy the light hole band [72]. This splitting can result in measurably higher hole mobilities, particularly at very low temperatures [73]. The net result is that one expects to achieve higher hole mobilities for pseudomorphic devices.

Of course, these advantages come at the price of an increased possibility of dislocated material. However, for layers thinner than a critical thickness, the lattice mismatch can be accommodated by strain rather than by dislocations [74, 75]. For example, for layers 20 nm thick (a reasonable channel layer thickness) a composition (x) mismatch of up to 15% is possible [70]. That is, it would be possible to use a strained $GaAs_{0.36}Sb_{0.64}$ layer for the channel without worrying about dislocations if this were the case for $GaAs_xSb_{1-x}$ on $In_xAl_{1-x}As$.

Exploration of each of these approaches, combined with a comparison with theoretical predication, will provide a clear picture of the potential performance of these p-HIGFETs. This lays the foundation for the next stage in the development of the technology: integration into a functional complementary technology, a complete research project in its own right.

4.3 EXPERIMENTAL RESULTS

Virtually every combination of the structures described above were grown and fabricated by MBE in a modified Varian Gen II growth chamber on semi-insulating (100) InP substrates supplied by Crystacomm, Inc. Experiments by Stutz et. al. showed that while pauses in growth between layers does not adversely affect the materials in the GaAs/$Al_xGa_{1-x}As$ system, it certainly does in the $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ system [76], so no growth stops were used for any active layers. All compositions were verified by x-ray diffraction measurements [13] and interfaces were shown to be abrupt and smooth by TEM [77]. Doping levels were calibrated by Hall effect measurements. Because experiments indicated that this abruptness might be degraded by anneal steps above approximately 550 °C [76], implantation for contacts was not used. All optical alignments were made with a Carl Zeiss MJB-3 contact aligner using the process described in Section 3.3. Contact resistance measurements were made using a Keithly 450 Automated DC Measurement system which controlled an Electroglas prober to measure 14 ohmic test patterns (Figure 3.1) per die for 5 die per wafer. These measurements were averaged for all die showing correlation of 0.99 or better. All other measurements were made using a Hewlett-Packard HP4145B Semiconductor Parameter Analyzer through an Electroglas prober. All measurements were controlled by a personal computer (PC) as shown in Figure 4.5.

The mask set used had a nominal gate length of 1 μm and contained over 200 transistors per die, either 10 μm wide or 200 μm wide with a source to drain separation of 5 μm. Ohmic test patterns were distributed within the die.

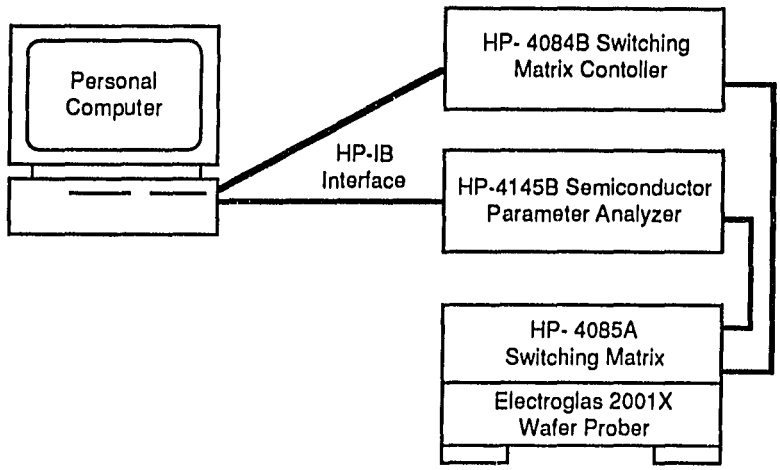

Figure 4.5: DC test measurement system for fully fabricated transistors.

4.3.1: LATTICE-MATCHED DEVICES

The results for lattice-matched devices in general were very poor. The best devices exhibited excellent gate leakage characteristics but very low drain current and, consequently, very low transconductance. The characteristics of a typical device with a channel doping of 4×10^{17} cm^{-3} and channel thickness of 25 nm are shown in Figures 4.6-4.8. Mobilities for this material were very low, on the order of 10 cm^2/Vs, which was verified by Hall measurements of thick epitaxial samples. This low mobility was attributed to a combination of alloy scattering and the clustering of material observed in TEM photomicrographs. The double-channel transistor of Figure 4.9 was fabricated to reduce channel resistance by creating a parallel channel below the standard location, after the work of Chan, et. al. [78]. This structure showed no improvement in characteristics. These transistors are clearly not suitable for high-performance circuits.

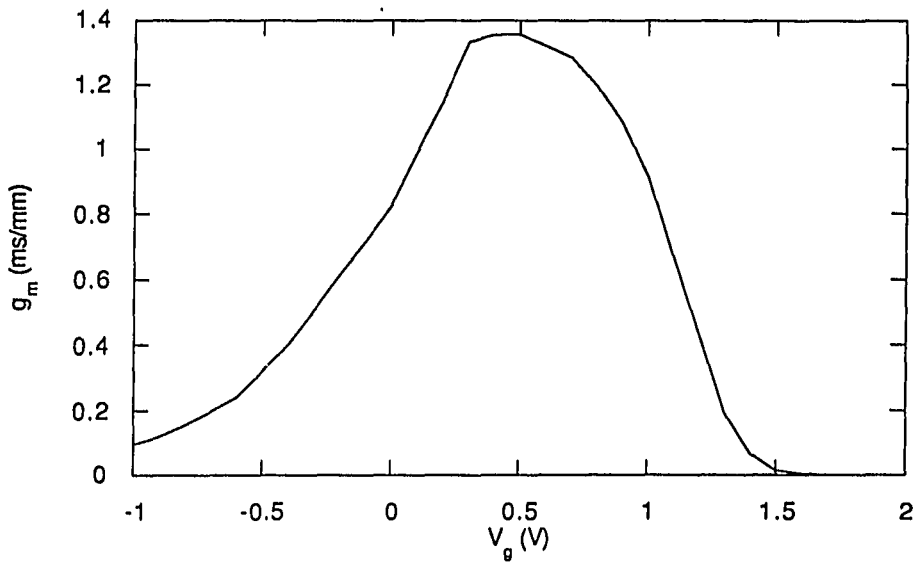

Figure 4.6: Transconductance curve for lattice-matched transistor.

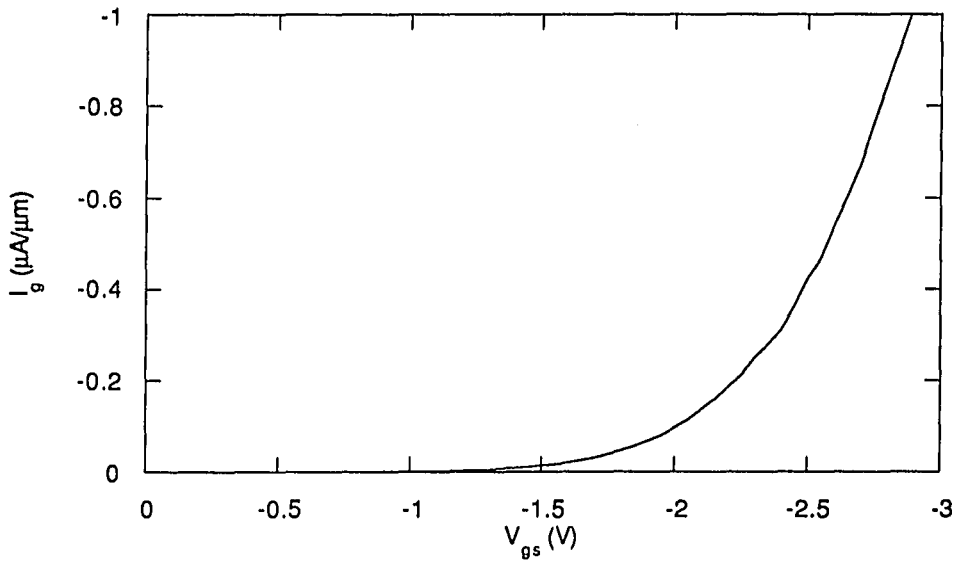

Figure 4.7: Gate turn-on characteristics for lattice-matched transistor.

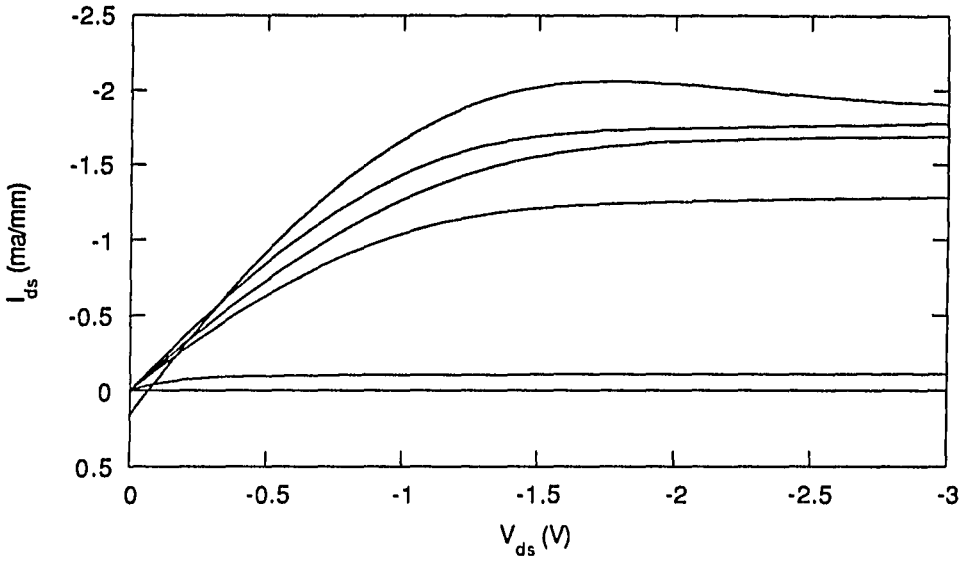

Figure 4.8: Current-voltage characteristics for lattice-matched transistor.

p^+ $GaAs_{0.51}Sb_{0.49}$	500 Å	Be: $1x10^{19}$	
i $In_{0.52}Al_{0.48}As$	300 Å		Barrier #1
p $GaAs_{0.51}Sb_{0.49}$	150 Å	Be: $4x10^{17}$	Channel #1
i $In_{0.52}Al_{0.48}As$	200 Å		Barrier #2
p $GaAs_{0.51}Sb_{0.49}$	150 Å	Be: $4x10^{17}$	Channel #2
n $In_{0.52}Al_{0.48}As$	500 Å	Si: $5x10^{16}$	
InGaAs/InAlAs Superlattice	600 Å		
i $In_{0.52}Al_{0.48}As$	2000 Å		

Figure 4.9: As-grown double-channel transistor structure.

4.3.2: STRAINED-CHANNEL DEVICES

An immediate improvement was seen when the lattice-matched channel was replaced by a strained-layer channel. No evidence (e.g., hysteresis or persistent photoconduction) was found to indicate that the channels had any appreciable amount of dislocation defects. For these devices, a channel composition of 65% GaSb was chosen which dictated a 20 nm channel thickness (1.2% mismatch), the complete structure is shown in Figure 4.10 and the band structure in Figure 4.11. As is readily apparent from Figures 4.12-4.14, these devices exhibited a great improvement in drain current, while retaining outstanding gate properties. The gate turn-on voltage for these devices was approximately -3 V. This represents an effective barrier height of 0.723 eV with an ideality factor of 5.3 corresponding to the heterojunction as part of the barrier (explained further in Chapter 5). This is the highest known gate turn-on voltage for any p-HFET technology and approximately 50% higher that the previous record [79]. The peak extrinsic transconductance was measured at 40 mS/mm, comparable to the best p-HFET fabricated in the $In_xAl_{1-x}As/In_yGa_{1-y}As$ system [79]. The intrinsic transconductance, which removes the effects of source resistance, was calculated by

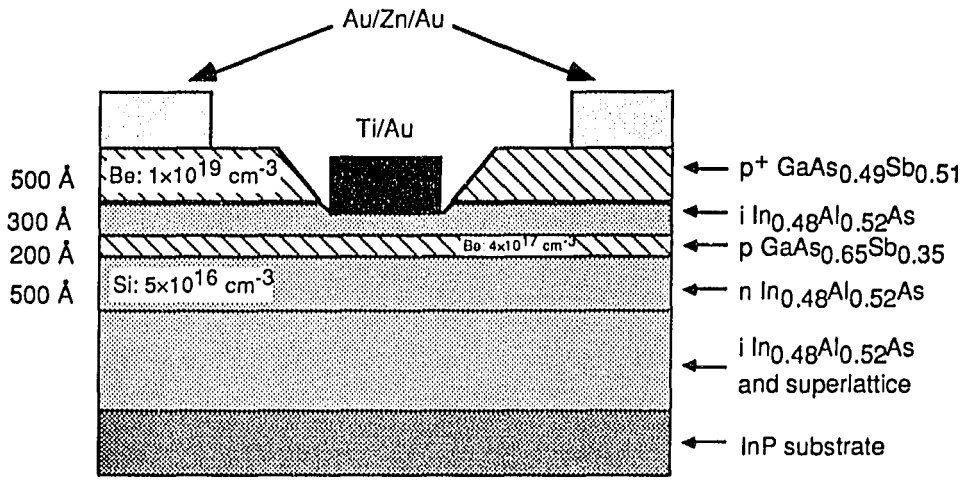

Figure 4.10: Finished structure of strained-channel p-HIGFET.

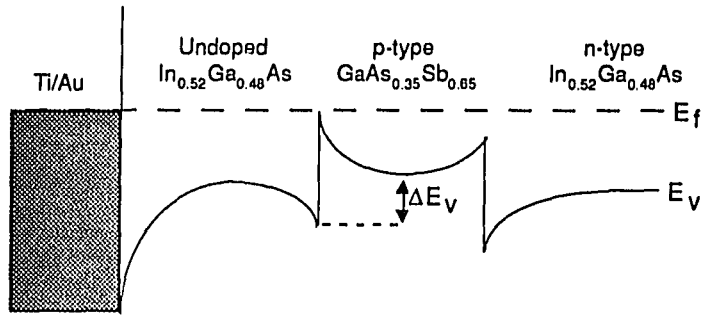

Figure 4.11: Valence band edge diagram for depletion-mode HIGFET with strained channel.

$$g_{m,int} = \frac{g_{m,ext}}{1 - g_{m,ext}R_s} \qquad (4.2)$$

to be 100 mS/mm. The transconductance curve is quite broad, remaining above 30 mS/mm for a gate voltage range of about 1.5 V. This allowed some devices to attain maximum drain currents in excess of 100 mA/mm, an important attribute if the transistors are expected to charge and discharge capacitive loads quickly. Unlike other p-HFETs, these devices also had excellent pinchoff characteristics with $I_{ds(on)}/I_{ds(off)}$ greater than 90,000. No difference was seen in normalized values between the 10 μm and 200 μm-wide transistors. Contact resistance following alloy was 0.97 Ω-cm

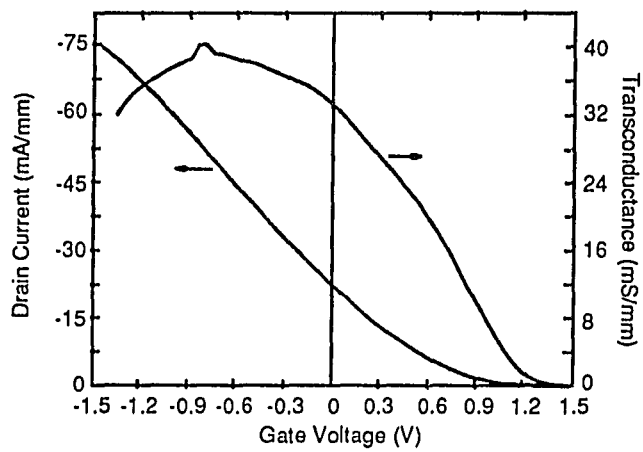

Figure 4.12: Transconductance and drain current curves for strained-channel transistor.

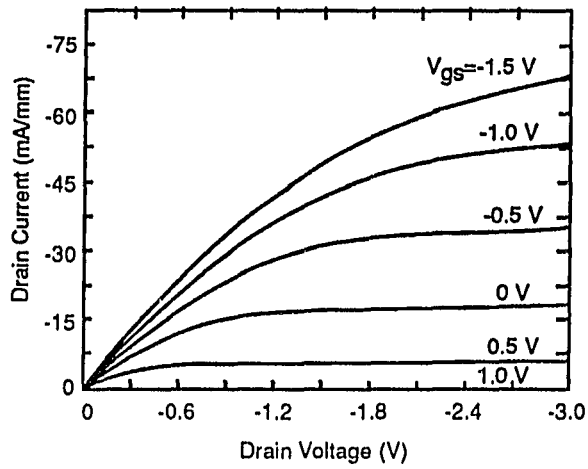

Figure 4.13: Current-voltage characteristics of strained-channel transistor showing excellent pinch-off and low output conductance.

and the source resistance was 100 Ω-mm.

Problems with the alloyed ohmic contacts severely limited yield of these devices. Most transistors on the wafers behaved as short circuits, indicating an excess of lateral diffusion during contact alloy. A closer examination during fabrication revealed that while contact resistance was

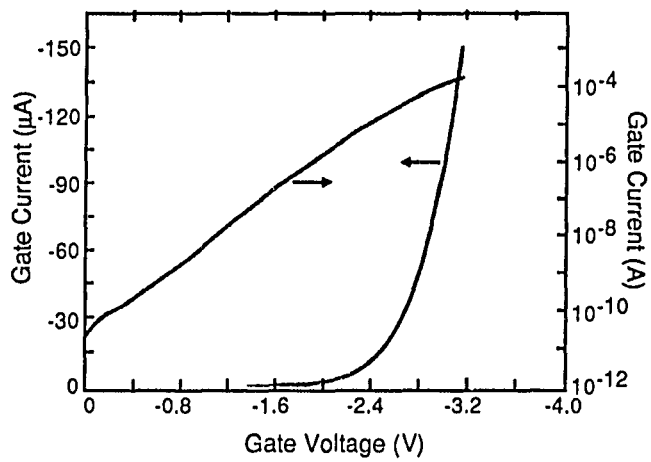

Figure 4.14: Forward gate characteristics of strained-channel transistor.

very uniform prior to the anneal step, this uniformity was lost after the anneal. There can be no doubt that, to be manufacturable, the devices will require a more repeatable and uniform ohmic contact.

However, experimental devices with strained GaSb-rich $GaAs_xSb_{1-x}$ channels had the lowest recorded gate leakage current for a heterostructure FET yielding a gate turn-on voltage of –3 V (a great improvement over the previous record) and also had transconductance and current drive comparable to the best p-channel HIGFETs of any material systems to date. This combination of properties is essential to the success of any complementary technology, but is seen for the first time in these p-channel HIGFETs.

5: PROJECTING THE PERFORMANCE OF COMPLEMENTARY HIGFET TECHNOLOGIES

No matter how good a solid state device appears by itself, the true measure of its worth is its performance in the intended application. Although there are many factors which have led to the dominance of silicon CMOS, particularly the ease and robustness of fabrication processes which allow high integration densities with acceptable yields. This attribute is clearly not one that is yet shared by complemtary HFET technology, as demonstrated in the preceding chapters. However, if one assumes that the processing of complementary HFET circuits can be made similarly robust, one may compare the potential perfomance of such circuits. In the case of a complementary transistor technology, this comes down to measuring the speed and power consumption of inverters and logic gates relative to that of silicon-CMOS, the reigning king of digital circuits.

5.1: MODELING THE TRANSISTORS

The first step in simulating circuits is to develop a suitably accurate model of the transistors which replicates the major features of device behavior. In the case of CMOS devices, a large number of models of varying sophistication are available for circuit simulators such as Berkeley SPICE [80]; such ready-made models are not generally available for HFETs. Nonetheless, since HIGFETs in particular behave in much the same manner as MOSFETs, a gross estimate may be obtained using these models by adjusting parameters such as mobility.

The major feature that is missing in these models is the ability to model the gate current of HIGFETs since MOSFETs have negligible gate currents. The obvious solution, then, is to augment a MOSFET model to add the gate current behavior. Since the gate current mechanism is essentially a combination of Schottky and heterojunction diodes, it is natural enough to understand that gate

current behavior can be mimicked by adding some diodes between the gate and the other terminals. Indeed, Chen et. al. have shown that the behavior of HFET gate currents can be approximated by two series diodes each between the gate and source and between the gate and drain [81].

In this model, one of the diodes represents the Schottky diode and the other represents the heterojunction. The reverse saturation currents and ideality factors for these diodes are extracted from actual current-voltage characteristics of a transistor. The ideality factor of the first diode is found from the semi-log slope at low voltages where the Schottky diode dominates and the reverse saturation current for this case is simply the y-axis intercept. Extracting the ideality factor and reverse saturation current for the second diode is somewhat more complicated. To extract the saturation current, straight lines are fitted to the log plots of both the low current and high current regimes. The crossing of these lines gives the second saturation current. The second ideality factor is found by multiplying the ideality factor found from the slope of the high-current regime by the ratio of two voltages. These voltages are simply the voltage difference between the high-current straight line intercept with an arbitrary current and the low-current line intercept with the same current over the voltage difference between the voltage at the crossing of the two lines and the voltage at the high-current line intercept used above. This method accounts for voltage drops across the first diode in calculating an effective ideality factor.

The resulting parameters from this method are summarized in Table 5.1. Simulation of DC characteristics using Berkeley SPICE version 2.6G showed that the turn-on voltage of -3 V is accurately modeled by this approach as shown in Figure 5.1.

The remainder of the MOSFET parameters were determined by fitting to current-voltage characteristics using a target transconductance of 90 mS/mm and peak drain current target of 120 mA/mm assuming improvements in hole mobilities and ohmic contacts. Parasitic capacitances were calculated based on parallel-plate structures for the gate-to-channel capacitance and gate-to-drain and gate-to-source capacitance were incorporated as junction capacitance for the gate diodes. The

Table 5.1: SPICE 2.6G parameters of gate model diodes for a 1μm × 10μm gate.

Parameter	Diode 1	Diode 2
IS (A)	1.435×10^{-10}	1.425×10^{-13}
N	2.561	5.34
CJ0 (F)	0.589×10^{-15}	0.589×10^{-15}

resulting SPICE MOSFET model parameters to emulate HIGFET gate behavior are summarized in Table 5.2. The n-channel devices were modeled as having the same gate turn-on voltage, but a transconductance of 400 mS/mm and a peak drain current of 200 mA/mm.

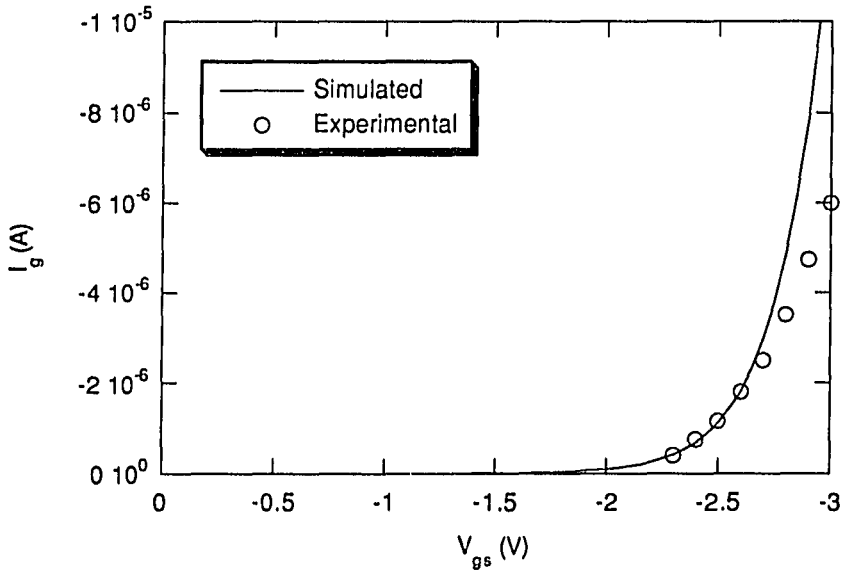

Figure 5.1: Modelled gate turn-on characteristics showing a good approximation to experimental results.

Table 5.2: SPICE 2.6G parameters for HIGFET simulation.

Parameter	p-HIGFET	n-HIGFET
Level	3	3
VTO (V)	-0.6	0.9
RD=RS (Ω)	37.5	10
U0 (cm^2/V s)	180	1000
TOX (m)	9.4×10^{-9}	9.4×10^{-9}
VMAX (cm/s)	1×10^{7}	3×10^{7}
UCRIT (V/m)	1×10^{7}	1×10^{7}
CJ (F/m^2)	0.0367	0.0367

5.2: SPICE SIMULATIONS

To compare performance to silicon CMOS, both DC and transient response were simulated for three different combinations of n- and p-channel aspect ratios and a range of supply voltages. DC transfer curves of inverters were used to determine the threshold voltages needed to maximize both noise margins. Transient speed and power of the inverters were then used to select the best aspect ratios to simulate NAND and NOR gates.

5.2.1: COMPLEMENTARY INVERTERS

Because of the similarity to CMOS devices, the natural starting point for this design was a standard CMOS inverter such as that described by Hodges and Jackson [71]. An alternative architecture has been proposed by Grider et. al. [82] that was simulated as well and is shown with the standard inverter in Figure 5.2. This approach attempts to maximize the speed of the circuit by

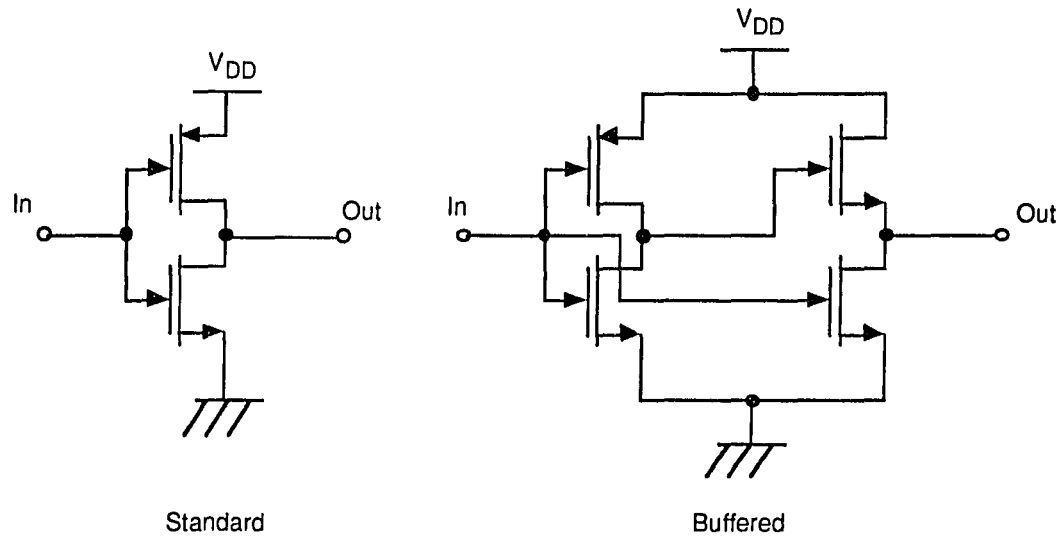

Figure 5.2: Shematic diagrams of simulated inverters. For buffered HIGFET inverter, complementary input stage drives n-channel output stage to improve speed.

using the faster n-channel devices for the output stage of the inverter.

DC transfer curves were generated for V_{DD}=2.0 V and V_{DD}=3.0 V, for both standard and buffered inverters. The resulting curves are shown in Figures 5.3 and 5.4. As for CMOS, the transition for the standard inverter structure between states is quite sharp, and the low gate leakage allows $V_{IL} \approx V_{DD}/2$ and $V_{OL} \approx 0$ and $V_{IH} \approx V_{DD}/2$ and $V_{OH} \approx V_{DD}$. The buffered inverter circuit does not have the same sharp transition because the drain of the pull-up transistor of the output stage is not tied to one of the rails. This floating drain also prevents the output from reaching the supply voltage.

To simulate actual loading conditions for an inverter, the circuit used was a chain of 11 inverters with the results being taken from the response of the 10th inverter. This implementation simulated the response of an inverter being driven by identical inverters and also driving the input of another inverter. The transition time was defined as the elapsed time from the moment the input was within

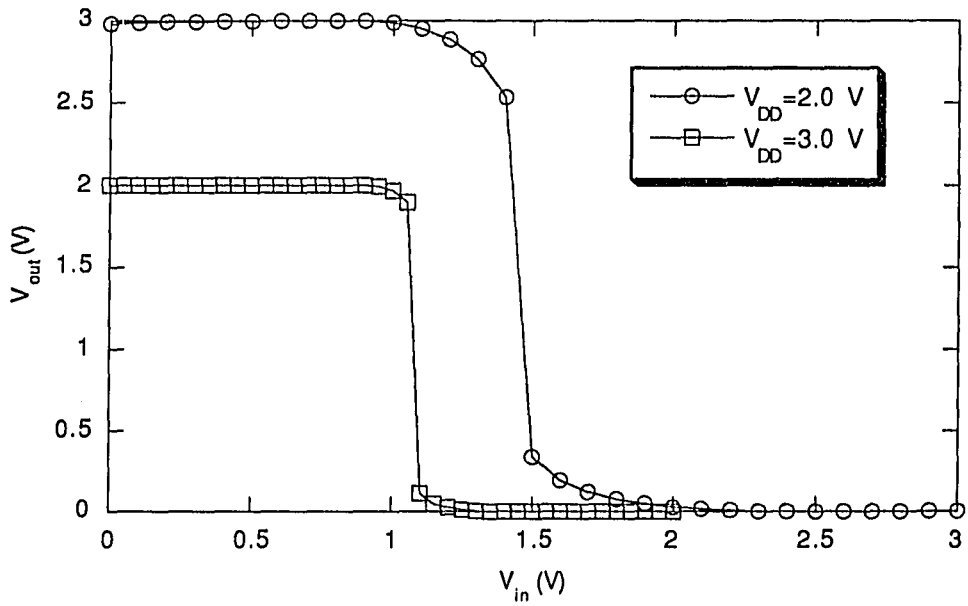

Figure 5.3: DC characteristics of standard inverter for V_{DD}=2.0 V and V_{DD}=3.0 V.

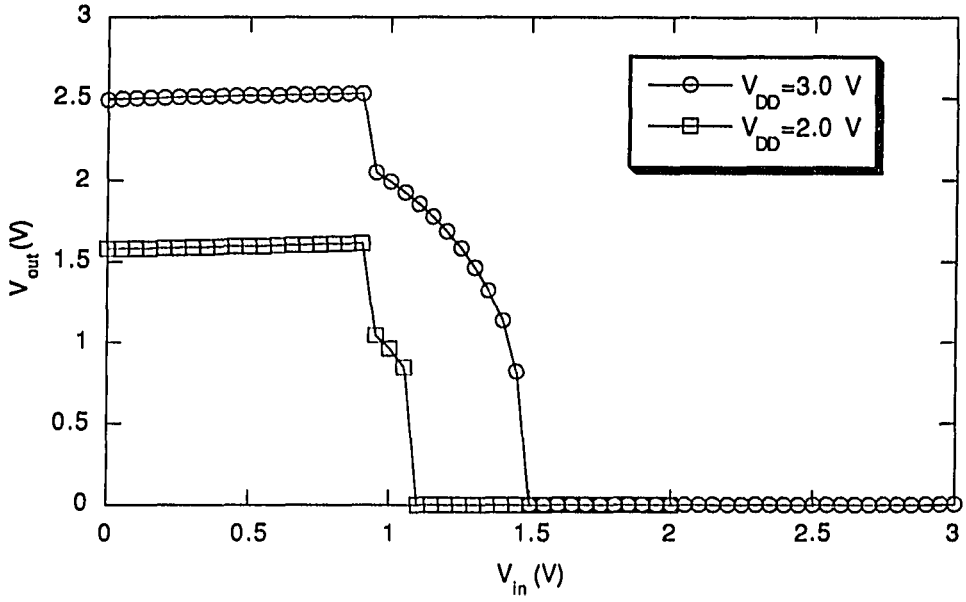

Figure 5.4: DC characteristics of buffered inverter for V_{DD}= 2.0 and V_{DD}=3.0 V.

10% of its final value until the time the output had changed to within 10% of its final value. For example, for the low-to-high transition, $t_{l\text{-}h}$ is from t ($V_{in}=V_{DD}/10$) to t ($V_{out}=9V_{DD}/10$). This transition is shown in Figures 5.5-5.8. Power consumption was calculated for all cases by integrating the product of the supply current and supply voltage and then dividing by the transition time and the results are summarized in Table 5.3. (SPICE was unable to converge for the buffered circuit for V_{DD}=1.5 V for all cases and for V_{DD}=3.0 V when W_p/L_p=5 and W_n/L_n=10, and V_{DD}= 2.0 was not sufficient bias to allow the output stage of the buffer circuit to perform properly, yielding very slow performance.) From these results, it is clear that the difference in performance between the p-type and n-type transistors is not large enough for the buffered inverter circuit to improve inverter performance, and the loss of voltage margin and increased area make this choice even less desirable. It is also apparent that the inverter circuit W_p/L_p=10 and W_n/L_n=5 has the best speed since the

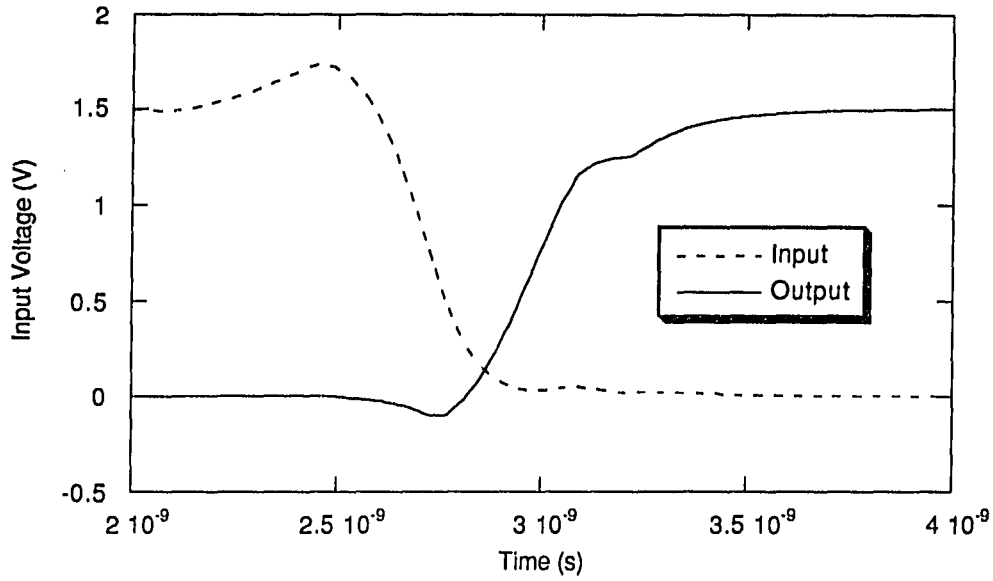

Figure 5.5: Transient behavior of standard inverter cell with W/L ratios of 5 (n-FET) and 10 (p-FET) and V_{DD}=1.5 V.

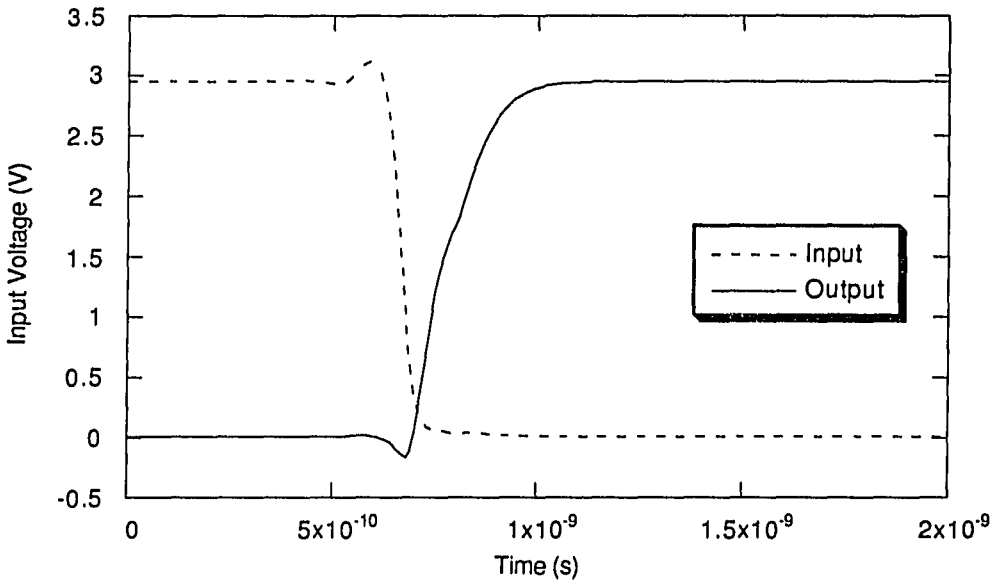

Figure 5.6: Transient behavior of standard inverter cell with W/L ratios of 5 (n-FET) and 5 (p-FET) and V_{DD}=3.0 V.

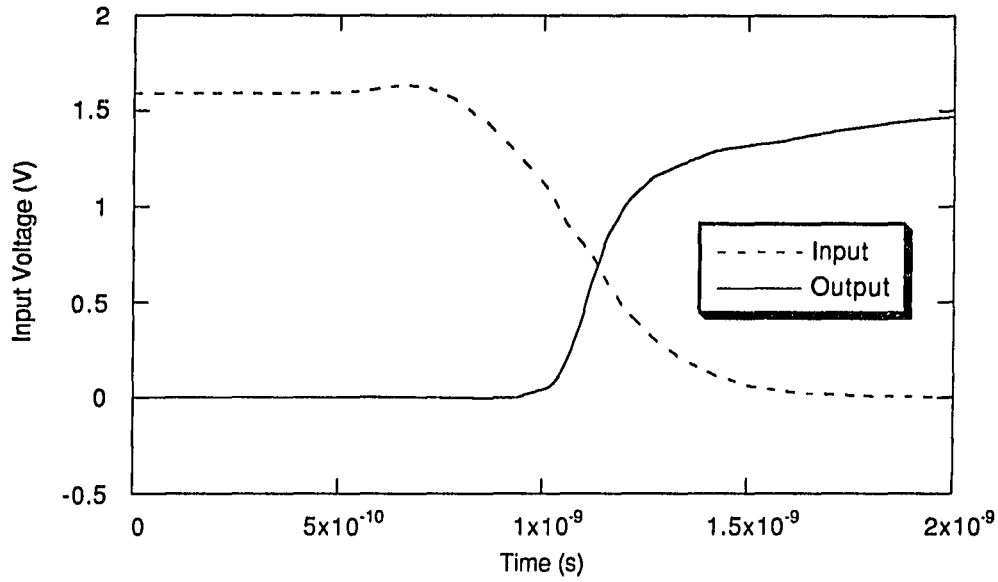

Figure 5.7: Transient behavior of standard inverter cell with W/L ratios of 5 (n-FET) and 10 (p-FET) and V_{DD}=2.5 V.

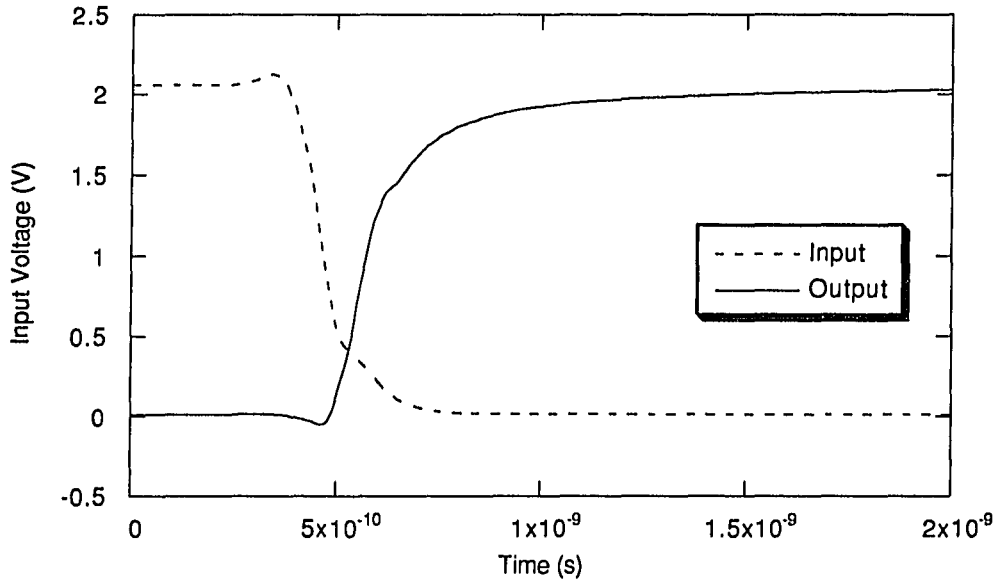

Figure 5.8: Transient behavior of buffered inverter cell with W/L ratios of 5 (n-FET) and 5 (p-FET) and V_{DD}=3.0 V.

Table 5.3: Gate delay and power-delay products for simulated inverter circuits.

		Gate Delay (ps)			Power-Delay Product (fJ)		
		W/L Ratios (n-channel/p-channel), 1 μm gate length					
	V_{DD} (V)	5/10	5/5	10/5	5/10	5/5	10/5
Standard	1.5	445	550	915	59	48.8	68
	2.0	290	360	505	245	117	156
	2.5	185	250	375	368	188	285
	3.0	120	210	315	456	353	383
Buffered	2.5	490	370	335	300	269	189
	3.0	390	305		546	345	

larger p-channel device helps to balance the speed of the n-channel, while $W_p/L_p=5$ and $W_n/L_n=5$ has the best power-delay product since overall currents are lower. The choice of supply voltage is not as clear since there is a clear trade-off between speed and power. This choice will ultimately depend on the intended application (e.g., a battery-powered application will require the lowest power consumption), but $V_{DD}=2.5$ V appears to be a good compromise.

5.2.2: NAND AND NOR GATES

Having chosen the optimal aspect ratios for speed of inverters and discarded the buffered circuit, it is a straightforward extension to design NAND and NOR gates. Again referencing Hodges and Jackson [71], the circuits simulated are shown in Figure 5.9. The transient times and power consumption were calculated in the same fashion as for the complementary inverter; examples of the output voltage versus time are shown in Figures 5.10 and 5.11. In a similar way to the inverter simulation, gates were simulated by monitoring the outputs and inputs to a gate that was sandwiched between two other gates. The simulation had only one input changing state at a time.

The results of these simulations are given in Table 5.4. The large asymmetry in the transients for the NOR gate as compared to the NAND gate is attributed to the fact that the NOR gate has the

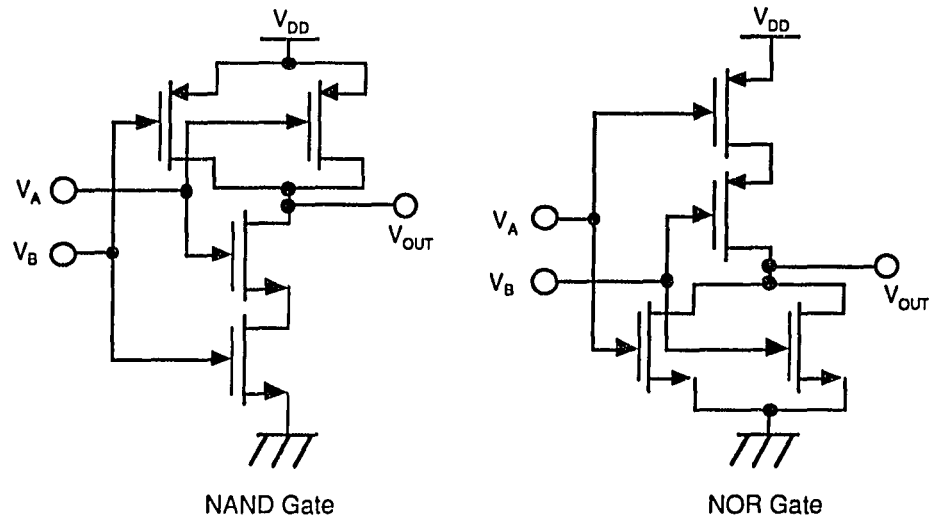

Figure 5.9: Schematic diagrams of NAND and NOR gates used in simulations.

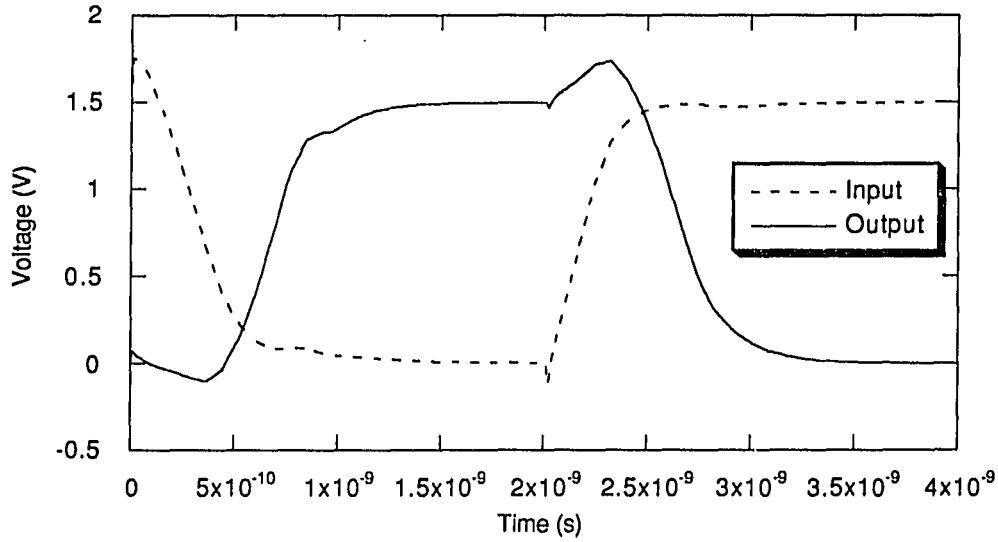

Figure 5.10: Transient characteristics of a NAND gate for V_{DD}=1.5 V.

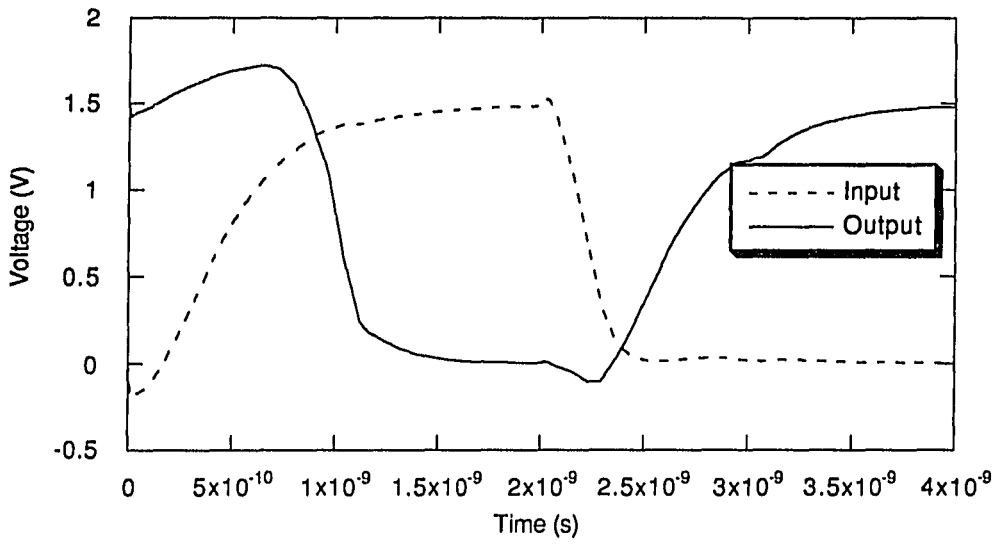

Figure 5.11: Transient characteristics of a NOR gate for V_{DD}=1.5 V.

p-channel devices in series rather than in parallel. This greatly emphasizes the difference in speed between the n- and p-channel devices since the p-channel devices are required to supply charge to the inputs of the next logic gate. The distinct "kink" in the curve of Figure 5.11 occurs at the point that the n-channel devices turn off and the current is completely sourced by the p-channel devices, with a noticeable slowing in the change of the output.

Table 5.4: Transition delays for NAND and NOR gates with W_n/L_n=5 and W_p/L_p=10 for L=1 μm

	NAND		NOR	
V_{DD} (V)	t_{L-H} (ps)	t_{H-L} (ps)	t_{L-H} (ps)	t_{H-L} (ps)
1.5	430	540	930	230
2.0	265	245	595	160
2.5	200	140	465	105
3.0	150	100	360	80

5.2.3: COMPARISON TO CMOS

Comparing to performance figures for silicon CMOS logic, we find that complementary HFET technology, as simulated, compares favorably. Published performance figures for similar device dimensions show that 1μm CMOS inverter ring oscillators achieve delay times of 215-300 ps for V_{DD}=3 V [83-85]. Complementary HFET technology therefore should have approximately twice the speed, with similar power dissipation, and the disparity is expected to be much greater for lower supply voltages [65]. This is a great advantage for battery-operated applications such as digital wireless communications where the highest possible speed is needed, but large power consumption can not be tolerated. This comparison does not include such intangible properties as robustness of a fabrication process or integration density and yield, though these are certainly very important properties to consider for any technology. Nevertheless, it does show that complementary HIGFETs have the potential to compete , at least in terms of performance, with silicon CMOS.

6: DISCUSSION AND SUMMARY

6.1: PRESENT LIMITATIONS OF COMPLEMENTARY HIGFET TECHNOLOGIES

Despite all the advances that have been made recently, much remains to be done before complementary HFET technology is ready for high-volume production. This work has shown that the $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ system is very appropriate for fabricating III-V p-channel transistors with low gate-leakage currents and high transconductance. This is due to the large valence band-edge discontinuity between the two materials and the relatively high hole mobility of $GaAs_xSb_{1-x}$, respectively. The remaining work needed to make complementary HFET technology competetive can be separated into two general categories: materials growth and complementary integration.

6.1.1: MATERIALS GROWTH

The problem to be addressed for material growth is to grow consistent, high-quality $GaAs_xSb_{1-x}$ layers with precise control of layer composition. Cross-sectional transmission electron microscopic analysis has shown that $GaAs_xSb_{1-x}$ tends to form clusters of GaAs and GaSb [77], rather than being randomly distributed, as is commonly assumed for alloys. This tendency is likely related to the well-known observation that GaAs and GaSb are not miscible for compositions of 39% GaSb to 62% GaSb using equilibrium growth techniques such as liquid phase epitaxy [86]. Such clustering is believed to substantially reduce bulk carrier mobility and would explain the observed mobilities [39]. Further experiments with growth temperatures and pressures may solve this problem quickly, but compositional control is more problematic.

Experience has shown that $GaAs_xSb_{1-x}$ growth requires frequent calibrations that are complicated by the broadening of the width of x-ray diffraction peaks from the compositional clustering. Small changes in $GaAs_xSb_{1-x}$ composition could have a great impact in device performance. A first

order effect would be changes in mobility, as evidenced in Chapter 2, which would result in variations in transconductance and drive current. A second order effect would be small changes in the band edge discontinuity resulting from the change in the band gap. This effect would result in subtle changes in gate current. A more serious possibility to consider is that a change in composition could result in a layer that is beyond critical thickness. The ensuing dislocations in such a layer would virtually destroy device performance.

A promising new approach to MBE growth is expected to help achieve precise control of layer composition. In this method, surface desorption is monitored in real-time by mass spectroscopy [87]. The relative desorption of the incident elements indicates the composition of the surface as it is being grown. This data is fed back through automated controls to the element source ovens, allowing real-time correction to give very accurate compositions [87]. Though this technique is still somewhat experimental, it has produced extraordinary control capability.

6.1.2: COMPLEMENTARY INTEGRATION

Finding a satisfactory approach to complementary integration is a much more open-ended matter. The simplest approach would be to fabricate both n- and p-channel transistors with the same $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ structure and use separate ion implantation steps to provide the necessary channel and ohmic contact doping, much as is done for CMOS. This approach has been used successfully in other material systems, most notably $In_xGa_{1-x}As/In_yAl_{1-y}As$ [79]. The drawback of this method for $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ transistors is that the system has a relatively small conduction band-edge discontinuity (about 100 meV) compared to that of the valence band edges. This would result in a great disparity between the gate currents of the two polarities.

An approach that is certainly more complicated involves etch and regrowth of new layers. In this method, device layers are grown for one of the device types and selected areas of the wafer are then

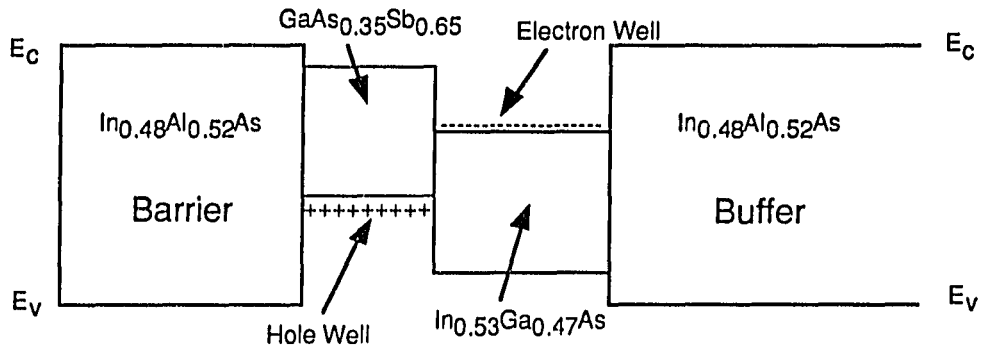

Figure 6.1: Schematic band diagram for staggered complementary heterostructure FETs.

etched away. The unetched portions of the wafer are masked with Si_3N_4, which inhibits crystalline growth. New layers for the second device are then epitaxially grown selectively in the uncovered (etched) areas. While this method does provide a great deal of flexibility for device structures, planarity is difficult to achieve, substantial spacing is required around regrown regions, and regrown layers tend to be of an inferior quality [13]. Such problems currently keep this approach a laboratory curiosity.

A method that is much more practical is known as the staggered complementary heterostructure FET (CHFET) structure [88]. By this technique, band-edge offsets are used to isolate n- and p-channel layers from each other (the band edges are "staggered"). A schematic band diagram in Figure 6.1 shows how the discontinuities would confine electrons in the $In_{0.53}Ga_{0.47}As$ (chosen for high electron mobility) and holes in the $GaAs_{0.35}Sb_{0.65}$ layer. The structure is optimized for p-channel performance since this is usually the limiting factor. The active layer is determined by the type of implantation species used for ohmic contacts. Though unproved experimentally, this approach may provide simplicity of fabrication without substantial loss of performance. Though the problems to be solved to realize true complementary integration are still substantial, there is no shortage of ideas for their solution.

6.2: SUMMARY

This work has shown the viability of p-channel $GaAs_xSb_{1-x}/In_yAl_{1-y}As$ HIGFETs for III-V compound-based complementary technologies to compete with silicon CMOS for specialized applications. Monte Carlo simulation was used to establish that even for the most extreme cases of alloy scattering $GaAs_xSb_{1-x}$ on InP has a higher bulk hole mobility than GaAs. Experimental measurements showed that the $GaAs_{0.49}Sb_{0.51}/In_{0.52}Al_{0.48}As$ system has the highest known valence band-edge discontinuity, a very important property for inhibiting hole currents perpendicular to the interface. Process development demonstrated that $H_2O:H_2O_2:H_3PO_4$:L-tartaric acid-based etchant solutions provide a reliable etchant with a selectivity of approximately 2:1 of $GaAs_xSb_{1-x}$ over $In_yAl_{1-y}As$. Process development also showed that Ti/Au was the most reliable gate metal for contact to $In_yAl_{1-y}As$ and that care must be taken to avoid letting some common chemical solutions come into contact with $GaAs_xSb_{1-x}$. Experimental devices established that lattice-matched $GaAs_xSb_{1-x}$ channel layers had low gate leakage currents, but had otherwise poor performance. However, experimental devices with strained GaSb-rich $GaAs_xSb_{1-x}$ channels had the lowest recorded gate leakage current for a heterostructure FET yielding a gate turn-on voltage of –3 V (a great improvement over the previous record) and also had transconductance and current drive comparable to the best p-channel HIGFETs of any material systems to date. This combination of properties is essential to the success of any complementary technology, but is seen for the first time in these p-channel HIGFETs. Finally, SPICE simulations showed that if integrated with n-channel HIGFETs with comparable gate leakage and moderate performance, modestly improved p-channel devices make possible technology with approximately half the delay time of similar CMOS circuits. Silicon CMOS has enormous advantages over complementary HFETs in terms of robustness and yield which allow very high densities of integration. Although much work remains to develop a robust, manufacturable HFET technology for commercialization, this work clearly establishes that

this infant technology has the capability to challenge the more established CMOS on the basis of speed and power consumption.

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