INFORMATION TO USERS

ELECTRICAL EFFECTS OF CMOS CIRCUIT PACKAGING

by

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To the memory of Zachary William Zell.

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ABSTRACT

Integrated systems are becoming so complex, it is extremely difficult for designers

to simulate full systems, particularly early in the design process. What the designer needs

is a methodology to quickly look at where he/she is going, and determine if there are any

potential packaging related problems. If so, where did the problem originate, and what

can be done about it? The designer wants a quick, easy to use and understand

methodology which consistently yields reasonably accurate results.

This dissertation is limited to CMOS circuits interfacing with metal interconnects.

Of particular interest here is the power and ground bounce, or noise, produced when large

numbers of output drivers switch simultaneously. The high output voltage swing, wide

range between best and worst case device performance, increased density, and high I/O

counts of CMOS integrated circuits make them particularly susceptible to excessive

simultaneous switching noise. A package model suitable for switching noise simulation

is used to develop a simplified methodology for modeling and simulating power

distribution networks in the presence of simultaneous switching outputs. This

methodology is validated with specific circuit examples, and used to investigate

simultaneous switching noise in detail. Of particular interest are the effects of various

parameters on switching noise magnitude. This leads to the derivation and verification of

a simple analytic switching noise formula, and a summary of noise reduction techniques.

Output driver delay and switching noise performance, and parameters that effect performance are examined in detail. The use of damping resistance for switching noise reduction, including the limitations for high current drivers are discussed. An adaptive low noise driver is proposed, which drastically reduces simultaneous switching noise, while still meeting worst case delay specifications. The successful application of the switching noise modeling and simulation methodology in the designs of four released ASICs and two low noise packages are summarized.

Finally, printed wiring board (PWB) electrical properties and general, simplified design guidelines are outlined. Two circuit examples are detailed, one dealing with a signal backplane, and the other a clock distribution network on a multi-layer PWB.

1. <u>INTRODUCTION</u>

Interconnects and packages at all system levels are already major performance bottlenecks.[1][2] Electronic device switching speeds and densities are increasing, while minimum integrated circuit and printed circuit board feature sizes are decreasing.[3][4] As these trends continue, the performance (speed, delay) of systems will become more and more package and interconnect dominated.[5] Of particular interest here is the power and ground bounce or noise produced when large numbers of output drivers switch simultaneously.

There is already quite a bit of excellent work going on toward developing very detailed interconnect models and simulation methods.[6][7][8][9][10][11][12] Accuracy is traded off against model and simulation complexity, making it difficult to handle large circuits. This dissertation presents a simplified methodology for including package and interconnect effects in circuit design and simulation at the chip and board level. The primary focus is on power supply distribution networks, particularly concerning ground and power supply bounce.

The discussion is limited to CMOS circuits interfacing with metal interconnects. The high output voltage swing, wide range between best and worst case device performance , increased density, and high I/O counts of CMOS integrated circuits make them particularly susceptible to excessive simultaneous switching noise. It is important to accurately estimate switching noise as early as possible in the design process, without

either grossly over or underestimating the problem. An underestimation is usually the most serious, since a nonfunctional IC can result. Overestimation can lead to a costly over design of circuits and packages, or to unnecessarily limiting circuit performance. Most common treatments of switching noise deal with derived analytic switching noise expressions, and conclusions drawn from them.[13][14][15][16][17][18][19][20] In this dissertation, a combination of modeling, simulation and analytic analysis is used to look at the problem in detail.

Chapter 2 gives background information explaining the reasoning behind the narrowing of focus to CMOS circuits and metal interconnects, including a discussion of alternative interconnect and circuit technologies. Chapter 3 describes interconnect and package modeling, explaining the tradeoffs of each model type.

Chapter 4 discusses the integrated circuit simultaneous switching output (SSO) noise problem. Various simplifications are discussed, and a methodology is proposed and verified with two circuit examples. This methodology is used to look into simultaneous switching nose in detail, including the effects of numerous parameter and noise prediction limitations. A simple but useful analytic switching noise expression is derived, and noise reduction techniques are summarized.

Chapter 5 is a detailed look at output drivers, focusing on the effects of various parameters on driver switching noise and delay performance. The limitations of source damping resistance noise reduction techniques are discussed. A new driver design is also

proposed which drastically reduces SSO noise, while still meeting worst case delay specifications.

Chapter 6 contains simultaneous switching noise design examples. Four ASIC designs and two package designs utilizing the noise modeling and simulation methodology presented in this dissertation are discussed. The final chapter summarizes the conclusions and results.

Appendix A provides a brief look at printed wiring board (PWB) physical and electrical properties, electrical performance effects, and simple design guidelines. Two signal distribution circuit examples are detailed, one dealing with a signal backplane, and the other a scan clock distribution network on a multi-layer PWB.

2. BACKGROUND

When investigating a topic as broad as electrical packaging and interconnect effects, it is necessary to first narrow the scope somewhat. This dissertation is restricted to CMOS circuits and metal interconnects. The exclusion of other circuit technologies and more exotic interconnect approaches (optical, superconductors etc.) is explained in the following sections.

2.1 Alternate Interconnect Technologies

2.1.1 Optical Interconnects

Optical solutions for interconnections have already been realized for board-to-board and system-to-system applications. What is of interest here is the feasibility of optical interconnects at the board and chip levels. There are many types possible, such as fiber optics, waveguides, unfocused free space broadcasting with detectors placed wherever needed, and focused broadcast using holograms.[21] [22] [23]

Optical approaches have many potential advantages over electrical methods. Crosstalk is greatly reduced because of the inherent non-interaction of different streams of photons.[24] The transmission bandwidth improvement is also significant.[25] Optical interconnects are also relatively insensitive to fanout (lack of capacitive loading effects),

while in electrical interconnects, delay and required power increase with fanout. Non-synchronous switching is greatly reduced, particularly with free space and holographic approaches.[26] One final potential advantage is reduced propagation delay, but one must be careful when considering this. Signals propagate down optical lines at the speed of light divided by n (the index of refraction of the medium). Electrical signals propagate at the speed of light divided by the square root of ϵ_r (effective relative dielectric constant). Materials with ϵ_r in the range of 2.7 to 4 are available. This compares favorably with optical fibers (n=1.5), particularly when a large portion of signal propagation delay is switching, which is common to both optical and electrical approaches. While optical interconnects may minimize the delay associated with propagating signals, additional delays are introduced in the conversion from electrical to optical signals, and again from optical to electrical signals. Moreover, these conversions generally consume undesirable amounts of power.

Optics have other disadvantages. As mentioned above, conversion between electronics and optics must be kept to a minimum. Optics may be limited by the bandwidth of electrical to optical conversion. Materials problems present a serious disadvantage to optics. Optical devices require a material with optical properties ,such as GaAs. The choice is to either use GaAs exclusively, or combine GaAs and Silicon. GaAs on Silicon is not a proven technology, to say the least. Utilizing a separate GaAs chip or a hybrid approach would increase off-chip interconnect complexity and density, thus negating many advantages gained. This would be worthwhile at the board and chip

levels only for selected large fan-out, extremely long, or off board interconnects. Another concern for optical approaches is the lack of maturity of the technology. How are fibers connected reliably to substrates? Free space optical signal distribution may require additional carefully aligned substrates, particularly for focused broadcast. How are these substrates aligned? What extra fabrication steps are needed for various optical interconnects? These are only a few examples of presently unresolved issues.

Although optics have many advantages, the disadvantages outweigh the advantages at this point in time. Since optical interconnects have been little used at the board and chip levels, many unforeseen complications may arise in addition to those mentioned above. A major concern is reliability. There are too many question marks in this relatively immature interconnect technology for extensive use at the board and chip levels in the near future. This is not to say it will not become important in the future, but it needs to be more fully explored first.

2.1.2 Superconductors

Superconductors provide a very intriguing alternative in interconnects. The major advantage over metal interconnects is the negligible series losses.[27] (In metal interconnects these increase as the stripe becomes longer, thinner and narrower.) The longer and thinner the line, the more losses come into play. The phase velocity of superconducting interconnects is independent of frequency up to hundreds of gigahertz,

making them virtually dispersionless.[28] The critical temperature, Tc, has increased

dramatically in recent years to well over liquid nitrogen temperatures (77°K).[29] It is

significant that for the first time we have an overlap in low temperature electronics and

high Tc superconductors, making hybrid systems possible.

The major disadvantage of superconductors is that the technology is still in its

infancy. No one is quite sure what to do with superconductors. New materials are

continually being investigated in the drive to increase Tc and fully understand the

principles behind high Tc superconductivity. What will the material properties be? How

will the materials adhere to boards and substrates? Are processing steps and temperatures

consistent with present processing technology? Reliability is a major concern. The field

is simply too new and changing to be of immediate use in microelectronics. Regular

metal lines must be very long, very small in cross section, or both before superconductors

offer much improvement. Another huge disadvantage is the need for cooling, which

increases power, weight, reliability, space constraints and cost. Without superconductors,

from 2 up to 5 times speed improvement is achieved at 77°K. More important for this

investigation, the mobility of electrons in metal interconnects at 77°K is about 10 times

that at room temperature. This increased conductivity is the main motivation for going to

cryoelectronics. Superconductors do not appear to offer a viable solution to the

interconnect problem in the near future.

2.2 Circuit technologies

There are a variety of technology choices available to the Integrated Circuit (IC) designer, such as Gallium Arsenide, bipolar, CMOS, and BiCMOS (bipolar and CMOS). This choice is crucial since interconnect and package performance and interactions are dependent on the circuit technology used.

2.2.1 Gallium Arsenide

Gallium Arsenide (GaAs) has quite different properties than silicon, and consequently various advantages and disadvantages. GaAs has a larger band gap than silicon, thus GaAs is more insulating (particularly when impurity doping introduces energy states in the middle of the band gap).[30] GaAs is also more radiation resistant, therefore it is desirable for many harsh environment applications.[31] Optical devices are possible in GaAs because of the direct band gap, making it ideal for optical applications.[32] GaAs devices are faster switching and higher bandwidth because the effective mass of electrons in GaAs is less than 10 percent of that in silicon.[33]

These advantages are offset by many disadvantages. There is no proven bipolar technology in GaAs, and no high speed complementary devices because of the very high effective mass of holes. The major disadvantages of GaAs are in the materials and processing areas. It is not nearly as mature a technology as silicon integrated circuits. Schottky barrier Metal Semiconductor Field Effect Transistors (MESFETs) are

predominantly used in GaAs. The lack of a good native oxide for GaAs prevents

fabrication of Metal Oxide Semiconductor (MOS) devices. These factors limit the

number of circuit configurations possible, and also increases power requirements. The

level of integration of GaAs integrated circuits is much lower, thus forcing more

interconnections off chip (and through packages). Finally, circuits implemented in GaAs

are much more costly than silicon.[34]

For very high speed (>1 - 5 GHz) applications, GaAs is very attractive.[35][36][37] For

most other applications, the advantages of GaAs cannot offset its other disadvantages,

particularly the higher cost. Far superior densities can be achieved in silicon. With sub-

nanosecond rise times now common, silicon circuit performance continues to improve. It

is hard to argue with a relatively inexpensive, very mature, improving technology such as

silicon. At some point, the speed and minimum feature size limits of silicon will be

reached, but not in the near future. The conclusion is: Don't use GaAs unless it cannot be

done in silicon.

2.2.2 Silicon

There are three obvious technology choices for high performance digital applications in silicon: bipolar emitter coupled logic (ECL); CMOS and BiCMOS. ECL has higher performance than CMOS, but CMOS is rapidly improving. ECL takes more power and dissipates more heat. Because of this, the level of integration in ECL cannot come close to VLSI CMOS. Most major semiconductor foundries such as National Semiconductor and Motorola are focusing on CMOS, including high performance sub-micron minimum feature size CMOS. CMOS is an extremely mature and improving technology. BiCMOS can incorporate the advantages of both bipolar and CMOS, including off-chip drive capabilities, without much added processing complexity.[38] In addition, it can have lower power dissipation than an equivalent CMOS circuit. This technology is available today and its development is extensive and widespread. CMOS and BiCMOS will be the most widely used technologies for all but the most specialized applications for years to come.[39] Performance limits may be reached as gate lengths approach 0.1 micron, after which new structures such as heterojunctions may take over, but CMOS and BiCMOS will dominate until then.

2.3 Conclusion

System design must take advantage of proven, mature, reliable technologies with high performance capabilities suitable for present and next generation digital systems. The usefulness of other interconnect technologies will depend on how well they can overcome the limitations of metal electrical interconnects, which have definitely not been fully explored. Similarly, CMOS will be the dominant technology for next-generation digital systems.

The techniques and methodology developed here will be applicable to all silicon technologies. Signal interconnect problems such as delay, losses, skew and distortion are common to all technologies to varying degrees. Power distribution networks can suffer voltage perturbations caused by the simultaneous switching of outputs. This is particularly true of CMOS circuits because of the wide variation in device performance over operating condition limits, and continually increasing integrated circuit I/O counts. In addition, CMOS circuits only consume power when switching, which causes large current transients. The choice of a detailed study of power supply distribution was motivated by transient switching problems present in CMOS.

3. <u>MODELING</u>

     The first step in developing a switching noise prediction methodology is to develop models and modeling techniques. The entire power distribution network must be considered, including planes, vias, package pins, traces and bonding wires. The models needed for power distribution may indeed be different than for signal distribution, where reflections and other output waveform distortions are concerns. In this chapter, different interconnect and package models and their characteristics are discussed, without restricting the application to power distribution network simulation.

     For this dissertation, inductance, capacitance and resistance are not considered functions of frequency. It is a common rule of thumb to ignore skin effects up to 100 ps switching times.[40] A common first-order approximation is that the product of bandwidth and rise time is 0.35.[41][42] With 100 picosecond rise time, we note that the bandwidth is 3.5 gigahertz. Thus we conclude that skin effect can be ignored for operating frequencies less than 3.5 gigahertz.

3.1 Board Level Interconnects

3.1.1 Planes

Typical multi-layer boards have three basic types of electrical interconnections: planes, traces and vias. Most power and ground connections are done through internal board planes. For supply distribution with small current drain, wide interconnects may be used. The parasitics of these power distribution board planes are ignored in this paper. It is assumed that the series inductance and resistance of the planes is low compared to the other package sections at the IC level.

3.1.2 Traces

Board traces are generally microstrip, or possible stripline interconnects for internal layers. There are many ways to model and simulate interconnects at the board and chip level. Transmission line parameters provide information for a variety of different models. Treating the interconnects as a distributed parameter transmission line is the most accurate model, but the least efficient with respect to simulation time. A simpler model breaks the line down into a series of lumped RLC (series resistor and inductor, shunt capacitor) segments, or a single lumped RLC. The possible models for use in analysis and/or simulation are listed below in order of increasing complexity. The choice

of model to use is a tradeoff of accuracy vs. ease and speed of computation. The simple lumped capacitor may be sufficient for certain cases, provided accurate capacitance values can be obtained. Other cases may need a more accurate transmission line analysis, or perhaps a treatment intermediate in accuracy and complexity. While modeling and simulating an entire chip or board using a full transmission line treatment has potential for great accuracy, it can be a challenge computationally. A simplified approach could flag potential problem areas for more accurate and detailed treatment.

3.1.2.1 Lumped Capacitor

A single shunt capacitor is the simplest of all models. The delay to a particular switching voltage may be fairly accurately represented in this manner. The general waveshape accuracy, including rise and fall times, is normally severely compromised unless the frequencies are low or the interconnect is very short. Typically, timing analyzers use this simple lumped capacitor model for their line delay estimates.[43]

3.1.2.2 Lumped Lossy Line

A more complex and accurate model is a single series resistor, series inductor, and shunt capacitor. For highly resistive lines (such as polysilicon), the L is often omitted for simplicity. A mostly lossless approximation for metal lines of reasonable length would

omit the resistance. Short lines or discontinuities can be approximated with a single lump of passive elements.[44] [45]

3.1.2.3 Series of Lumped Elements

As lines get longer, analysis and simulation using a single set of lumped elements begin to lose accuracy. The definition of long in this case is the ratio of the physical length to the rise time. The higher the frequency signals involved, the shorter the physical length which is considered as "long". A good rule of thumb is to include a lumped RLC for every section of line for which the delay is one tenth of the signal rise time.[46] [47] Some sources suggest two or three times as many sections as this.[48]
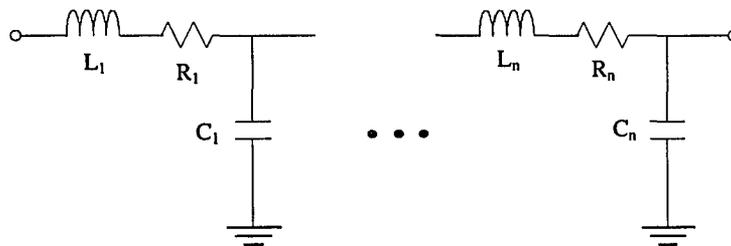
Guideline: Choose n for delay through each section ≤ signal rise time/10

Figure 3.1 Concatenated lumped element segment interconnect model

3.1.2.4 Transmission Line

A transmission line is essentially the extension of a series of lumped sections, with an additional shunt conductance in parallel with the line capacitance. As the section lengths are made infinitely small, we arrive at the transmission line model. The differential equations describing the time varying voltage and current at any point along the line in terms of the distributed circuit coefficients is:[49]

$$\frac{\partial\, v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial\, i(z,t)}{\partial t} \cdots$$

$$\frac{\partial\, i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial\, v(z,t)}{\partial t}$$
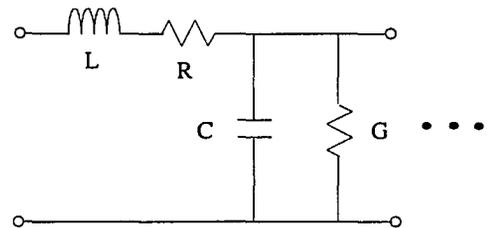
For boards the conductance, G, can be ignored. For silicon substrates, this conductance and frequency effects in general should be considered. The ratio of v to i is the same at all points along the line. This characteristic impedance (Z_0) is complex for a lossy line, while that of a lossless line (R=G=0) is real.

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad \Rightarrow \quad Z_0 = \sqrt{\frac{L}{C}} \quad \text{for lossless lines (R=G=0)}$$

Thus, a lossless line is modeled as a delay and an associated characteristic real

impedance. Typical board Z_0 values are between 35 and 100 ohms.

3.1.2.5 Equivalent Dominant Pole and Excess Phase Model

This model is based on the frequency domain voltage transfer function for a

transmission line network. The transfer function contains hyperbolic trigonometric

functions of the transmission line parameters and the frequency domain variable, s.[50] An

infinite series expansion results in an infinite amount of s domain poles. Approximating

this with a few dominant poles is equivalent to the lumped RLC models discussed above.

A closer approximation is one or two dominant poles with an excess phase term. The

excess phase term is chosen so that the approximating function's magnitude and phase

response closely matches that of the original transfer function. In the time domain, this

approximation corresponds to a lumped section and a pure time delay.

$$T(s) = \frac{1}{1+\frac{s}{p}} \exp(-s\phi) \qquad\qquad (3.1)$$

where p = dominant pole ϕ = excess phase

A model such as this was written for the Saber simulator, which accepts user

defined models and subroutines. Unfortunately, the results were not particularly

encouraging. Just as in the transmission line models discussed above, any model with a pure time delay proved to be very inefficient computationally. In some cases, converging on a solution at all became a problem. Since the goal here was to find a simple, efficient model with reasonable accuracy, this was not pursued any further.

3.1.2.6 Coupled Lines

The next step is to include coupling between lines. The simplest is to consider only adjacent lines. The lines can be capacitively or inductively coupled. A SPICE model has been developed which uses ideal lossless transmission models and cross-coupled inductances and capacitances.[51][52][53][54] An equivalent circuit is derived which consists of ideal linear circuit elements, and lossless TEM transmission lines. Although this results in a circuit suitable for CAD tools such as SPICE, the run times will be prohibitive for large networks of coupled, lossy lines, particularly if coupling is considered for more than the nearest adjacent lines. Accurate estimates of the coupling parameters for such large, complex structures can also be very time consuming.

3.1.3 Vias

For frequencies less than one gigahertz, vias can be modeled with lumped passive elements.[55] Three possible via models are shown below. Typically,

$$L < 0.1 \, nH, \quad and \quad C < 1 \, pF$$

Although each situation must be assessed individually, vias are often of secondary concern because of the relatively small element values.
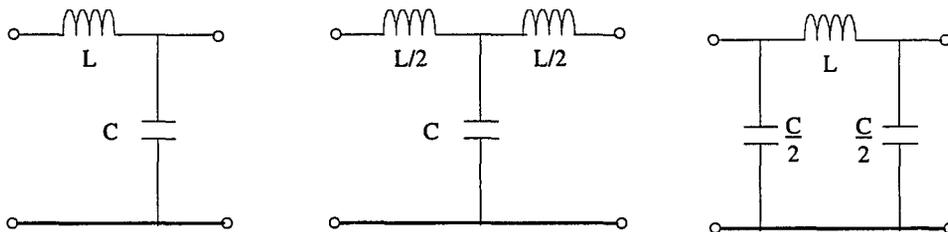
Figure 3.2 Via circuit models

The equivalent circuit models behave approximately the same if:[56]

$$\omega L << Z0 \quad and \quad \omega C << 1$$

For $Z_0 = 50\Omega$, and $\omega = 2\pi*1$ GHz, this means:

$$L << 8 \, nH, \quad and \quad C << 150 \, pF, \qquad \text{which is typically true.}$$

3.2 Package modeling

The next level of interconnection is the package which encases a single IC, a multi-chip module, or a hybrid module. High performance packages generally contain at least one power and one ground plane.

3.2.1 IC package pins, traces and die bonding

The package pins, the package to die bond connection (wire, TAB, etc.), and the pin to bond traces are all important parts of the package and must be modeled. Since pins and bond connections are normally relatively short electrically, as previously discussed, they can typically be modeled as a series resistance and inductance, with perhaps a shunt capacitance. Package traces should be treated similar to board traces as discussed above. The higher the pin count, the larger the package, and therefore the longer the signal traces will usually be from die to pin. This is particularly true for packages with external connections only on the package perimeter (e.g. leadless and leaded chip carriers, dual in line packages, etc.).

Typical pin resistances range from 0.1 to 0.5 ohms.

Typical series inductance values range from 0.1 to 10 nH:[57] [58]

1 mm bond wire .025 mm diameter	0.9 nH
1 mm TAB .05 mm diameter	0.3 - 0.7 nH
Flip Chip .1 mm diameter	0.1 nH

3.2.2 Package Planes

The package planes lower the power distribution series resistance and inductance, at the same time providing additional power supply plane to ground plane capacitance. Since the plate surface area of a power or ground package plane is usually large relative to the thickness and spacing, a simple parallel plate simplification is sufficient for estimating the plane to plane capacitance.

$$C_{parallel\ plate} = \frac{\varepsilon_0 \varepsilon_r A}{d} \quad , \quad A = \text{plane surface area}; \qquad d = \text{plane to plane}$$

spacing

Thus, this capacitance can vary quite a bit from package to package depending on the package size, plane spacing, and inter-plane dielectric. Typical values range from 100 pF to 1 nF.

Although planes reduce series inductance and resistance, they cannot be ignored because of the large power and ground currents which can flow in large IC's. Resistance values can normally be estimated, given material properties and geometries, or they can

be measured. Inductance values can be found with available field solving tools, which

will be discussed later. Typical inductance values are usually less than 2 nH.

3.3 Chip level distribution

The last level of interconnection is the integrated circuit itself. For the most part, chip level interconnects are not considered here. The parasitic element values and associated delays tend to be small when compared to the board and package affects. Another problem is the difficulty in predicting element values before actual chip layout is complete. This makes it hard to include interconnections in chip circuit simulations. If it is absolutely necessary, worst case element estimates can be included. The danger here is an overly pessimistic estimate which results in over designing the system, and underestimating performance capabilities.

Generally, there are multiple, separate power and ground rings and associated pads on the chip. A typical large high performance IC might contain:

"Dirty" power and ground for output drivers.

"Clean" power and ground for the internal logic, and possibly

the input receivers.

Internal clock driver power and ground connections.

Note that these separate power networks are typically connected together in the IC package planes.

Output drivers should be properly placed with respect to associated power and ground pads. For example, simultaneous switching output groups should generally be evenly distributed between the VDD and grounds. It is assumed for this dissertation that

the current is evenly distributed among all of the ground and power pads and pins of interest. If this is not the case, the actual placement of all I/O drivers with respect to power and ground connections must be known to accurately predict switching noise. Non-uniform driver or power pin placement can result in unpredicted, localized noise problems if not accounted for in simulation and modeling.

Integrated circuit substrates can cause noise problems in two ways. P-type integrated circuit substrate ground current mixing can cause crosstalk, but this will not be considered because it is usually minor when compared with inductive and capacitive crosstalk.[59] Direct substrate coupling of ground noise is discussed in Chapter 4.

3.3.1 Electromigration

The number and placement of ground and power pads on an IC depends on two factors. One is the SSO noise requirements, which will be discussed in the next chapter. The second involves electromigration and average DC current levels. Electromigration is the mass transport of metal atoms by momentum exchange with conducting electrons.[60] Metal disappears in certain regions, causing open circuits. The current densities at which reliability problems occur is different for many materials.[61] The number of I/O pads which can be present before a power/ground pad must be placed is based on adhering to process and material electromigration guidelines. Factors which are involved include:

The capacity of the power busses

The switching frequency

The capacitive loading of each output.

The average current in each driver is given by:

$$I_{DC}/driver = VDD * Load\ capacitance * f_{switch} \tag{3.2}$$

As an example, consider an IC power bus which has 100 mA electromigration capacity. Assume the SSOs are driving 50 pF loads worst case, the worst case VDD is 5.5 volts, and the maximum switching frequency is 100 MHz. Note that f_{switch} is 100 MHz/2, since a transition L-H (for VDD bus) or H-L (for ground bus) can occur a maximum of once every other cycle.

$$I_{DC}/driver = 5.5\ volts * 50\ pF * 50\ MHz = 13.75\ mA$$

Thus, only seven such outputs can be placed before a bus pad in order not to violate the worst case electromigration guideline of 100 mA. In general, an average switching frequency of about once every 5 cycles is considered a conservative rule of thumb, which allows the above guideline to be relaxed somewhat from the worst case condition.[62]

3.4 Test Connections

In order to test a raw die or packaged IC, a test fixture of some sort must be attached. We are ultimately interested in the electrical effects of the package on the IC performance. It can be difficult to measure this because the test fixture itself can dominate the testing results. It is not uncommon for a test socket to have a series inductance greater than 4 nH per pin, which is larger than the total for the package pin, plane, traces, vias and bonding.[63] The least intrusive test setup consists of picoprobes and an air bearing die testing table. These active FET probes typically have effective resistances greater than 1 MΩ, and a capacitance of approximately 1 pF. Tester parasitics obviously must be taken into account in order to validate a modeling and simulation methodology. It is possible that the IC may not even function as it was designed while being tested. Simultaneous switching and clock speeds may have to be reduced from normal operation for testing, because of the increased loading of a test fixture.

3.5 Transmission Line Parameter Calculation

Transmission line parameters for board and package traces, vias, leads, bond wires and pads must be found. The quickest way is to use existing derived analytic formulas. For more accuracy, there is software available which calculate electrical parameters from physical data.[64][65][66][67] In general, Poisson's equation is solved for a given geometric cross section of conductors. Once the free charge on the conductors is known, the transmission line parameters (matrices of capacitance and inductance per unit length) are found algebraically.[68] Software of this type from Quantic Labs (Greenfield) and the University of Arizona (MOM, UAC, VAXUAL) was used. Most parameter extractors use transverse electromagnetic (TEM) wave approximations.[69][70] The University of Arizona was also pursuing an interesting simulation approach which does not use the TEM approximation.[71][72] This is a frequency domain simulator which uses network scattering parameters. However, this complexity is not necessary until frequencies are significantly greater than 1 GHz.

3.6 Package Model Examples

Two similar packages are modeled here as examples in sections 3.6.1 and 3.6.2. They are 172 and 256 pin ceramic quad flat pack (CQFP), each with two signal layers, one power plane, and one ground plane. The total power and ground pin allotments for each are shown in sections 3.6.1 and 3.6.2. All of the external power and ground pins are connected to a single pair of package planes. Separate connections are needed at the die for dirty/ring power, clean/core and clock pad power.

Figure 3.3 is a schematic of a generalized package power model. Element values per pin for both packages, and complete package models are given in the following sections. Package trace and plane contributions are based on National Semiconductor modeling results, while the pin and bond wire contributions are based on my calculations and some measurements. National Semiconductor utilized a combination of University of Arizona's UAC and MOM, and Quantic Laboratories Greenfield software tools to obtain these parameter values.[73][74]

It is important to note that clock pads often physically break up dirty power and ground rings along the die periphery. The modeling and simulation methods used here assume a uniform distribution of power/ground connections and switching output drivers. Chip clock pads should be placed carefully. They must not break up the dirty power ring into sections with unbalanced driver I/O pad to power/ground pad ratios or sections with no power and ground pin connections.

BOARD VDD

LP1

RP1

PACKAGE   POWER   PLANE

LP2   LP3   LPCLK   LPCLK

RP2   RP3   RPCLK   RPCLK

RING/DIRTY   CLEAN/CORE   CLOCK PAD 1   CLOCK PAD N
POWER   POWER   POWER   POWER

$C_{PKG\ PLANES}$

RING/DIRTY   CLEAN/CORE   CLOCK PAD 1   CLOCK PAD N
GROUND   GROUND   GROUND   GROUND

RG2   RG3   RGCLK   RGCLK

LG2   LG3   LGCLK   LGCLK

PACKAGE   GROUND   PLANE

RG1

LG1

BOARD
GROUND
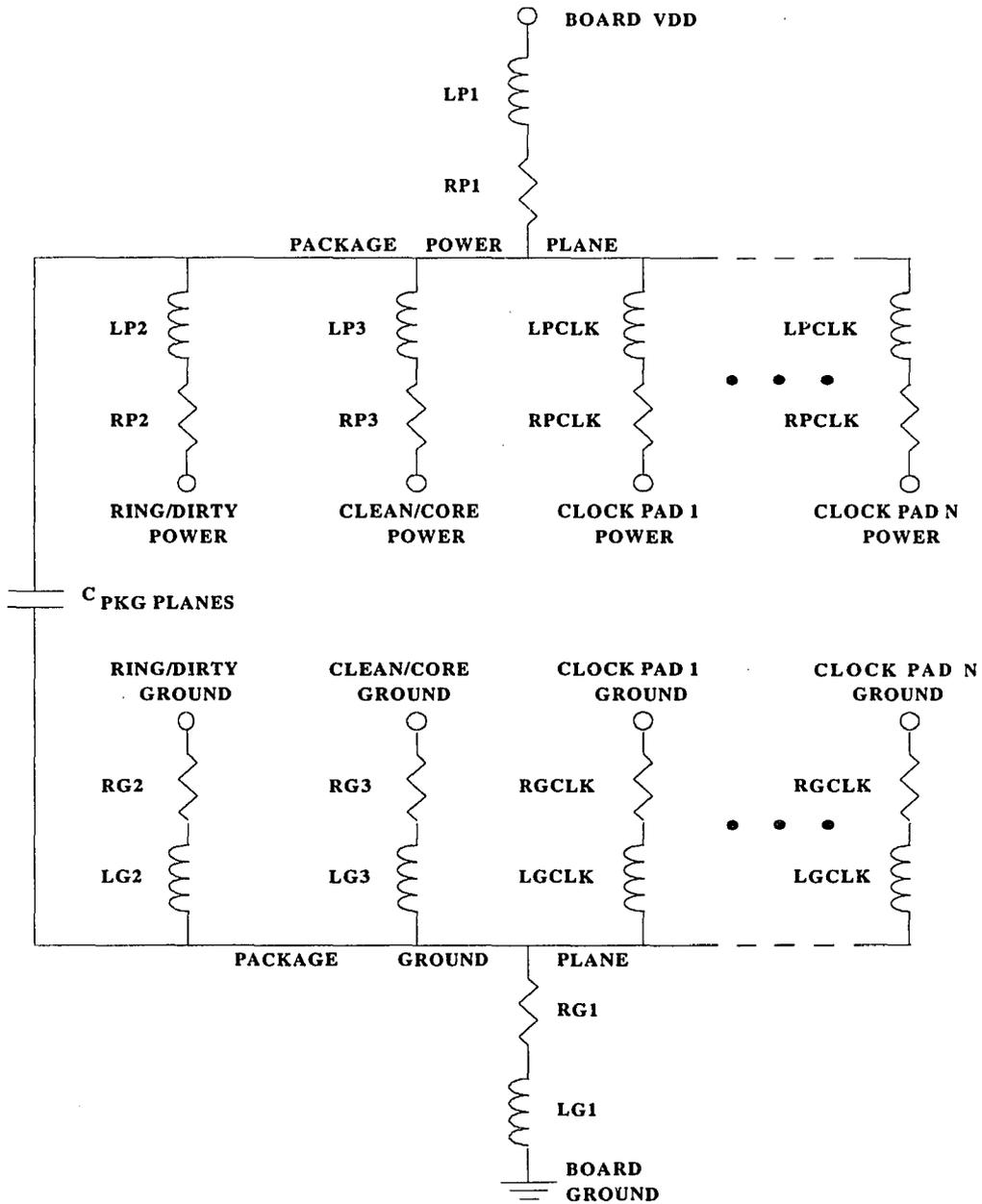
Figure 3.3 - Generalized Package Power Distribution Network Model

3.6.1 256 Pin Ceramic Quad Flat Package (CQFP)

As a specific example, consider a 256 pin package with an allocation of 28 ground pins and 24 power (VDD) pins. A simplified package drawing is shown in Figure 3.4. Assume there are two on chip clock pads. All external power and ground pins are connected to the package planes. The breakdown for package planes to die pads connections is crucial. For this example:

External Pin Power and Ground Allotment

Dirty/ring power	16	
Clean/core power	6	Total power (VDD) connections = 24
Clock pads (2) power	2	

Dirty/ring ground	20	
Clean/core ground	6	Total ground connections = 28
Clock pads (2) ground	2	

Board to Package Plane Element Values

resistance = 0.1 ohms/pin

inductance = 2.15 nH/pin   (includes 1.2 nH lead inductance)

Package Plane to Die Pad Element Values

resistance = 0.1 ohms/pad

inductance = 1.95 nH/pad   (includes 1 nH, 50 mil long bond wire

inductance)

Package Power Plane to Ground Plane capacitance = 315 pF

Figure 3.5 is a schematic for this configuration, including element values. Results of element calculations are:

LP1 = (2.15 nH/pin) / (24 power to plane pins) = 0.09 nH

LG2 = (1.95 nH) / (20 ground plane to die pads) = 0.098 nH

.58 in.

1.46 in.

.092 in.

Ground Plane   Power Plane

Figure 3.4 - 256 Pin CQFP

BOARD VDD

0.09nH

.0042

PACKAGE POWER PLANE

0.122nH

.00625

RING/DIRTY
POWER

0.325nH

.0167

CLEAN/CORE
POWER

1.95nH

.1

CLOCK PAD 1
POWER

1.95nH

.1

CLOCK PAD 2
POWER

315pF

RING/DIRTY
GROUND

.005

0.098nH

CLEAN/CORE
GROUND

.0167

0.325nH

CLOCK PAD 1
GROUND

.1

1.95nH

CLOCK PAD 2
GROUND

.1

1.95nH

PACKAGE GROUND PLANE

.0036

0.077nH

BOARD
GROUND
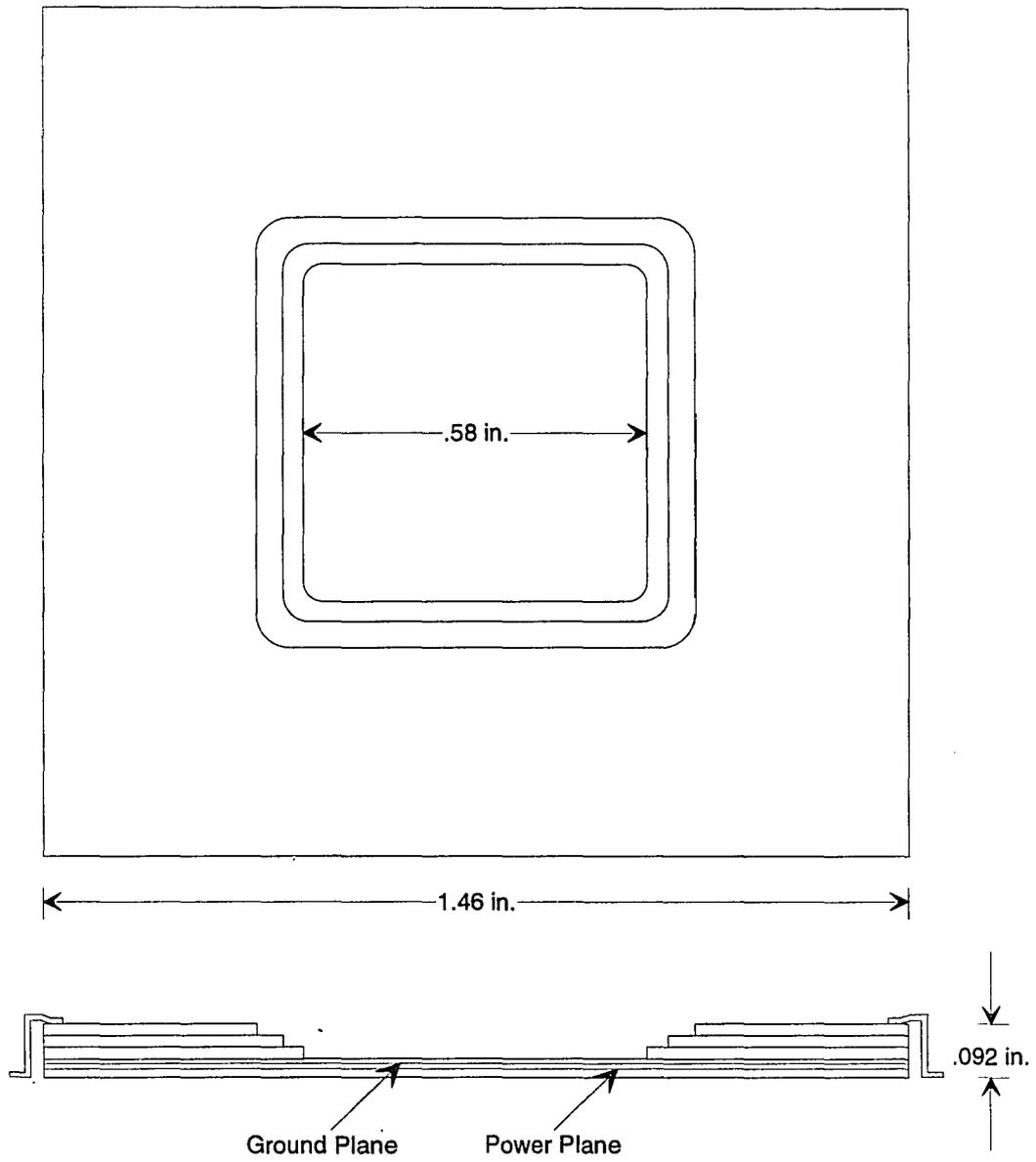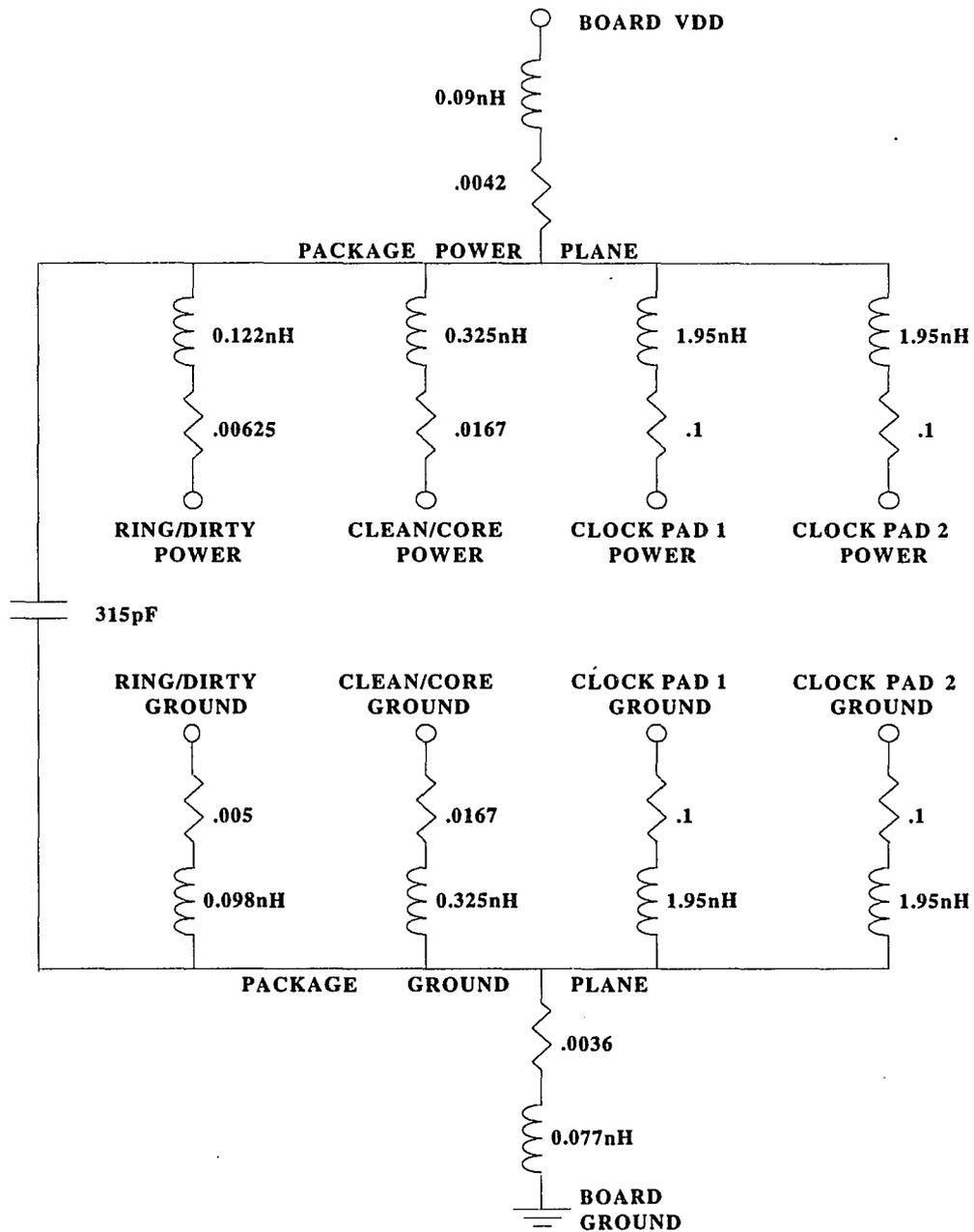
Figure 3.5 - Example of a 256 Pin CQFP Power Distribution Network Model

3.6.2 172 Pin CQFP

As a final example, consider a similar 172 pin package. A simplified package
drawing is shown in Figure 3.6, and the final package model in Figure 3.7.

External Pin Power and Ground Allotment

Dirty/ring power   9

Clean/core power   4   Total power (VDD) connections = 15

Clock pads (2) power 2

Dirty/ring ground   11

Clean/core ground   4   Total ground connections = 17

Clock pads (2) ground   2

Board to Package Plane Element Values

resistance = 0.1 ohms/pin

inductance = 2.0 nH/pin   (includes 1.2 nH lead inductance)

<u>Package Plane to Die Pad Element Values</u>

resistance = 0.1 ohms/pad

inductance = 1.8 nH/pad   (includes 1 nH bond wire

inductance)

Package Power Plane to Ground Plane capacitance = 220 pF

.38 in.

1.15 in.

Power Plane

Ground Plane

.095 in.
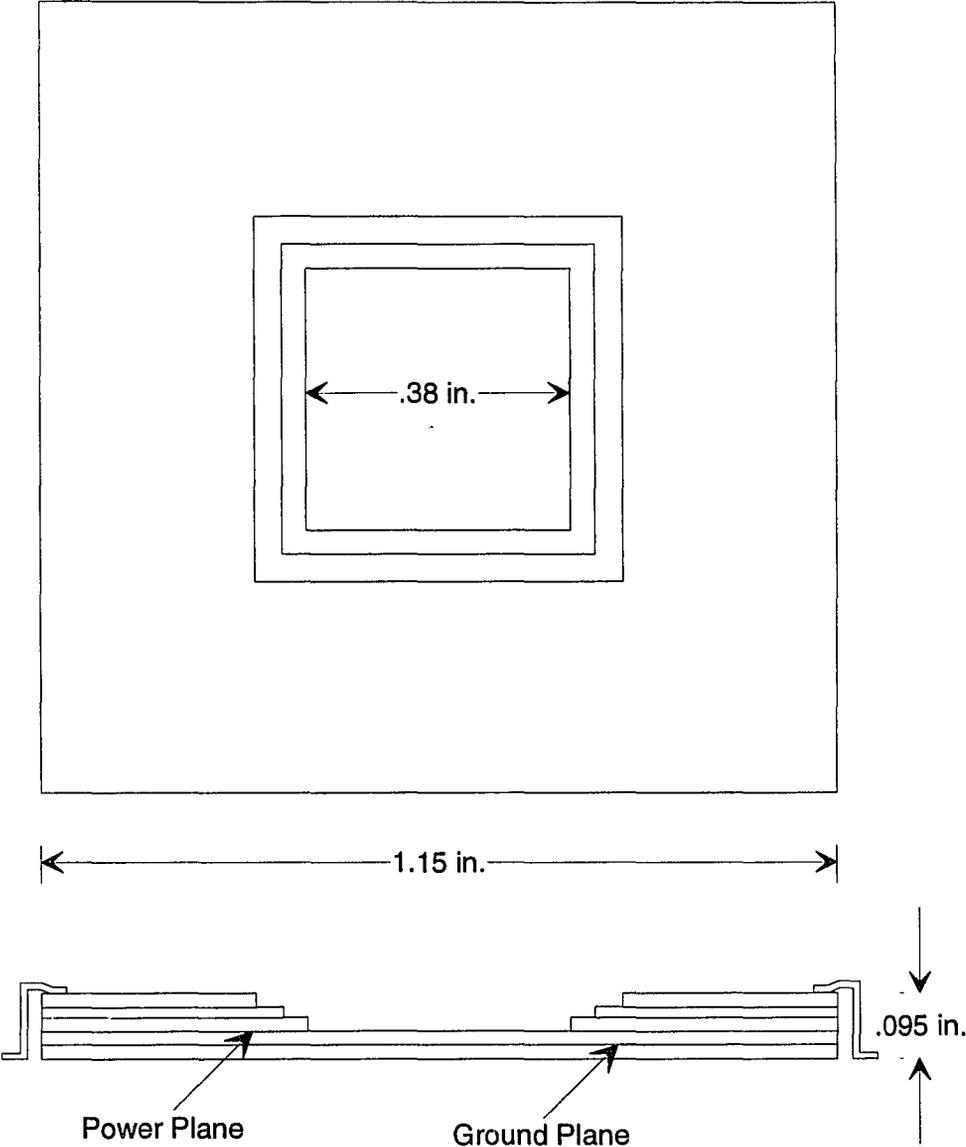
Figure 3.6 - 172 Pin CQFP
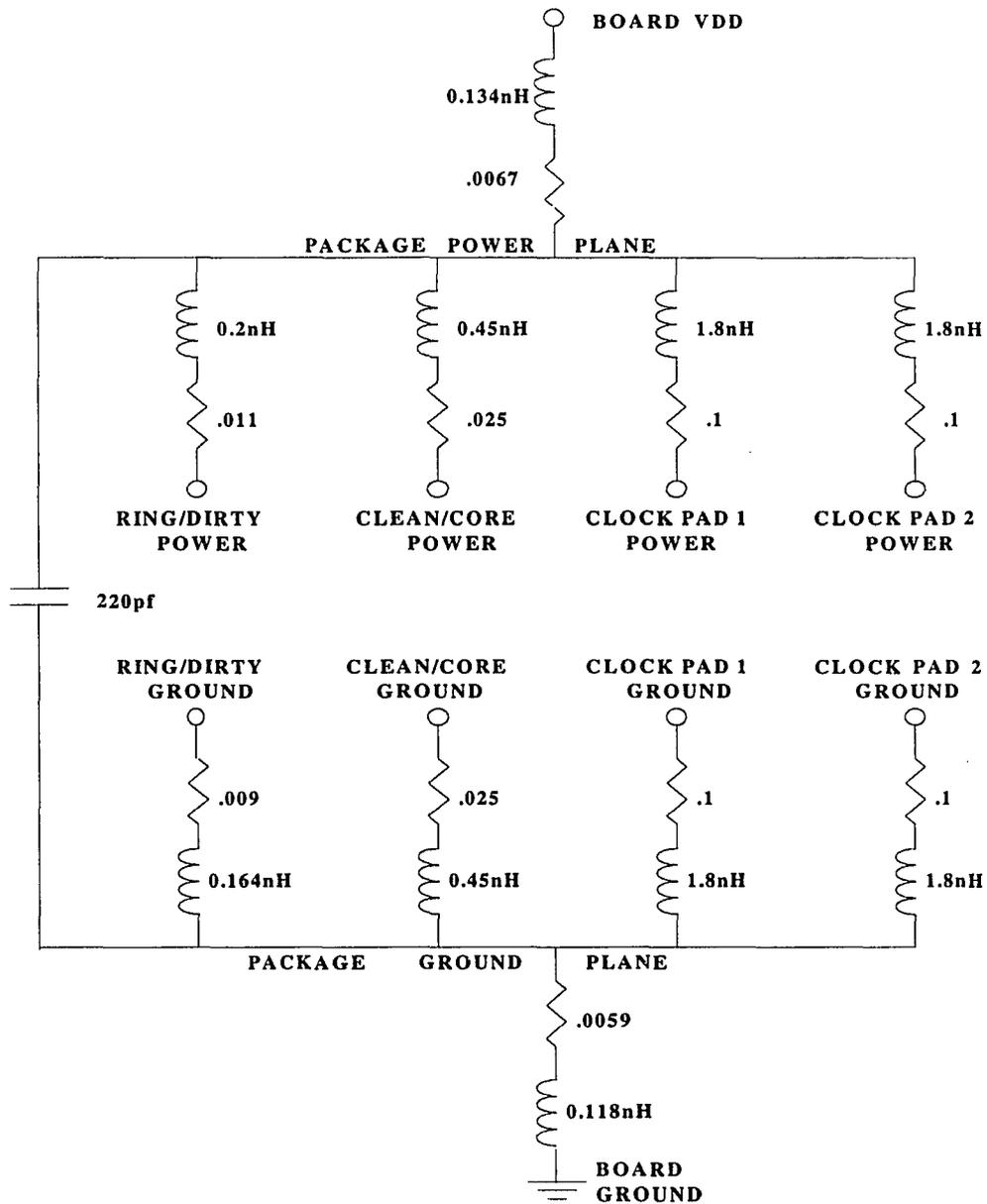
Figure 3.7 - Example of a 172 Pin CQFP Power Distribution Network Model

4. POWER SUPPLY DISTRIBUTION

4.1 Introduction

Ground and power supply bounce are perturbations on the supposedly DC ground and power supply lines feeding an IC. This occurs when a number of output drivers switch simultaneously. Obviously, as the I/O count increases, the more concern there is for ground or power supply bounce. This is particularly true for CMOS circuits. CMOS exhibits a number of properties which potentially contribute to this noise:

The large output voltage swing demands high current drivers to meet system speed requirements.

Output driver performance varies dramatically over temperature, supply and process limits.[75] This means drivers must be over designed to meet performance specifications under worst case conditions.

Decreasing minimum feature size and use of mult-chip modules (MCM) result in increased I/O count, and faster switching times.

It is important to accurately address potential switching noise problems during the IC or MCM design stage. Either underestimating or overestimating a switching noise problem is undesirable. An underestimate is usually the most serious, since a nonfunctional IC can result. An overestimate can mean a costly, over designed power distribution network, package, and IC. Also, limiting a parameter such as output drive to prevent a nonexistent noise problem results in a lower performance IC than is necessary.

Most analysis attempts in the past have concentrated on simplistic circuits and analytic models.[76 77 78 79 80 81 82 83] While analytic models are useful in getting an idea of the magnitude of a potential switching noise problem, there are a number of inherent problems which preclude an extremely accurate analytic estimate. First, analytic solutions generally assume outputs switching exactly simultaneously, which is not likely to be the case in a real circuit.

Second, the output driver MOSFETs are assumed to be characterized by a "square-law" relationship between drain current and drive voltage, $(V_{GS} - V_T)$.[84 85 86 87 88] This is not the case at all for present short channel devices (channel length $\leq$ 1 micron). Figure 4.1 depicts actual measurements, and HSPICE simulations of 0.8 micron National Semiconductor MOSFETs.[89] The fairly constant spacing between the members of the curve family shows clearly that there is not a square law relationship between MOSFET drive voltage and drain current.

Third, the device current waveforms are normally assumed to be triangular in shape, while the actual outputs are not , as shown in Figure 4.2. This figure plots the

switching current and ground bounce for 16 SSOs in a 256 pin package. The maximum

current is usually assumed to be the saturation current, but the current is smaller than this

in practice.[90] The complexity of modern driver circuits, as well as the nonlinear behavior

of actual devices contribute to this behavior. Lastly, the effects of non-switching outputs

are not taken into account, and their loading effect on power and ground lines can be

significant. Fortunately, this loading effect works to our advantage in reducing power and

ground bounce somewhat.
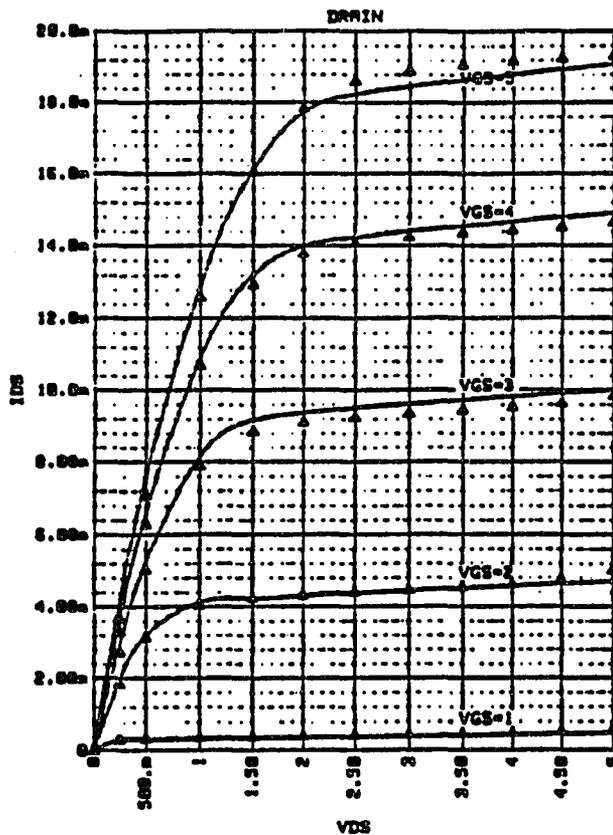
Figure 4.1 - 0.8 Micron MOSFET Device Characteristics
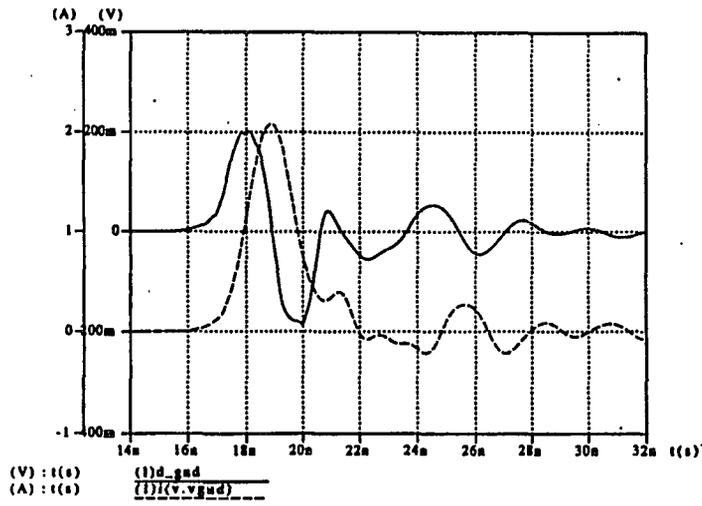
Figure 4.2 - Simulated Output Driver Current (dotted line in amps) and Ground Bounce (solid line) Voltage Waveforms

In this chapter, detailed driver models and extensive simulations are used to investigate SSO noise, and the effects of various parameters on the noise magnitude. First a general simulation methodology is developed for two specific cases for which experimental results are available for correlation and validation. Then this methodology is used to investigate switching noise in detail, including various parameter sensitivities, trends, and to provide improved analytic estimates and noise reduction suggestions.

4.2 Example 1: Custom Data Processing Chip

This particular 132 pin, 1.5 micron CMOS ASIC failed under the following

operating conditions:

Nominal VDD (5v)

Cold temperature (-55C)

Best processing

An entire 16 bit output bus switching simultaneously.

The output drivers were enabled by a direct action (asynchronous), low active,

control signal. Upon enabling, a large underdamped oscillation was observed at the

driver outputs. The problem was finally diagnosed as excessive VDD bounce, turning on

and off the drivers as the asynchronous enable line was misinterpreted. The resulting

VDD line bounce at the IC VDD pad was 3 volts peak to peak, approximately symmetric

around VDD. Figure 4.3 depicts the measured VDD waveform at the packaged die pad.

The measurement was obtained using an air bearing IC probe station with an active FET

picoprobe (input C = 1 pF, R = 1MΩ). The package had no ground or power planes.

Ground and power were each routed through four normal signal leads.

The modeling effort consisted of varying complexities of driver, package and

interconnect models. It was found that detailed transistor level SPICE driver circuit

models were necessary to accurately model and simulate the VDD bounce. Initially, the

surrounding passive network was modeled in great detail, including many minor

parasitics. The element values were found using University of Arizona MOM and UAC software. Figure 4.4 depicts an intermediate complexity model of the power and ground distribution networks. Figure 4.5 is a greatly simplified model which contains only an equivalent lumped series inductance.

A.) Midway along package trace.

B.) Package Bonding Pad

C.) Die bonding pad
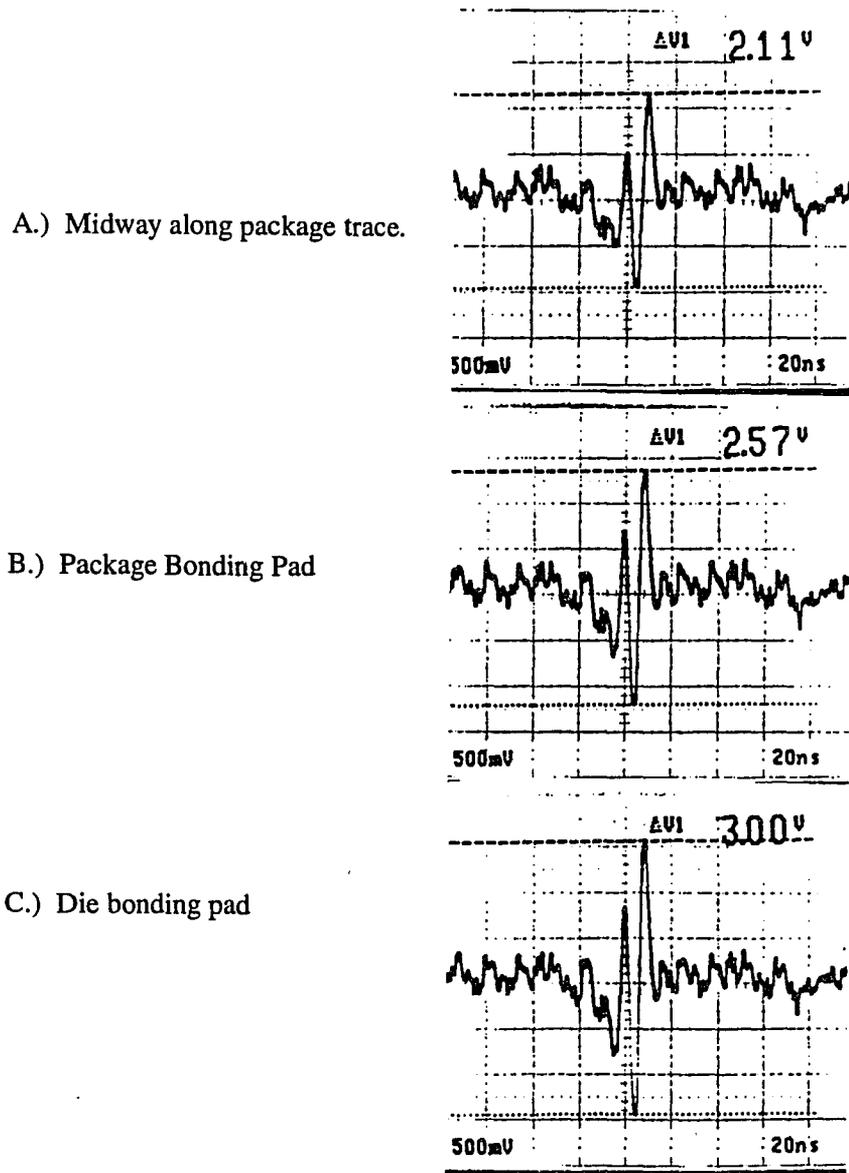
Figure 4.3 - Example 1 ASIC Noise Voltages at Various Package Locations
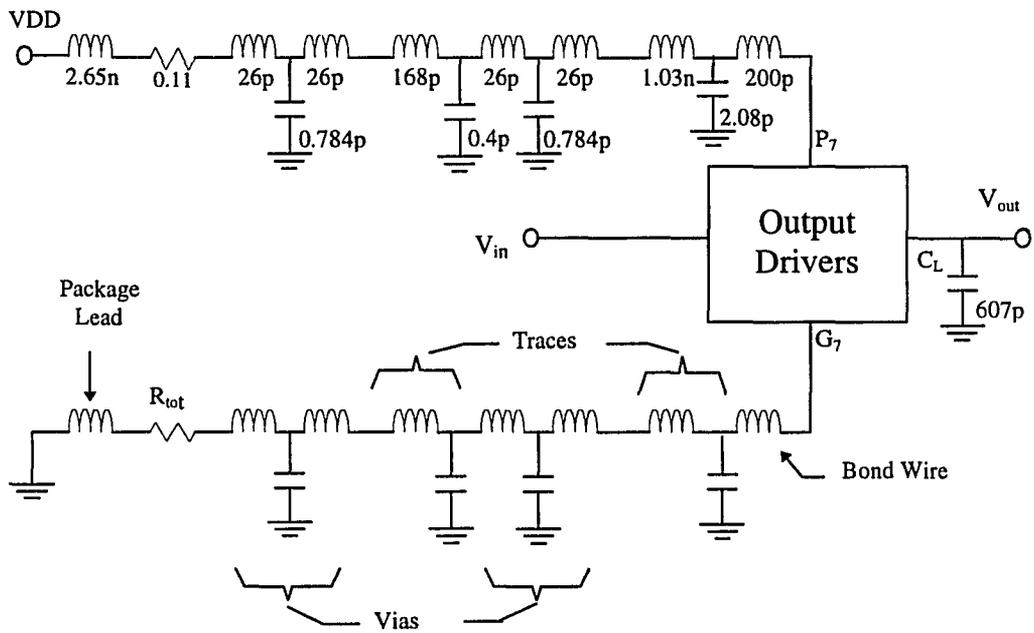
Figure 4.4 - 132 Pin Package Model, Power and Ground = 4 Leads Each

VDD
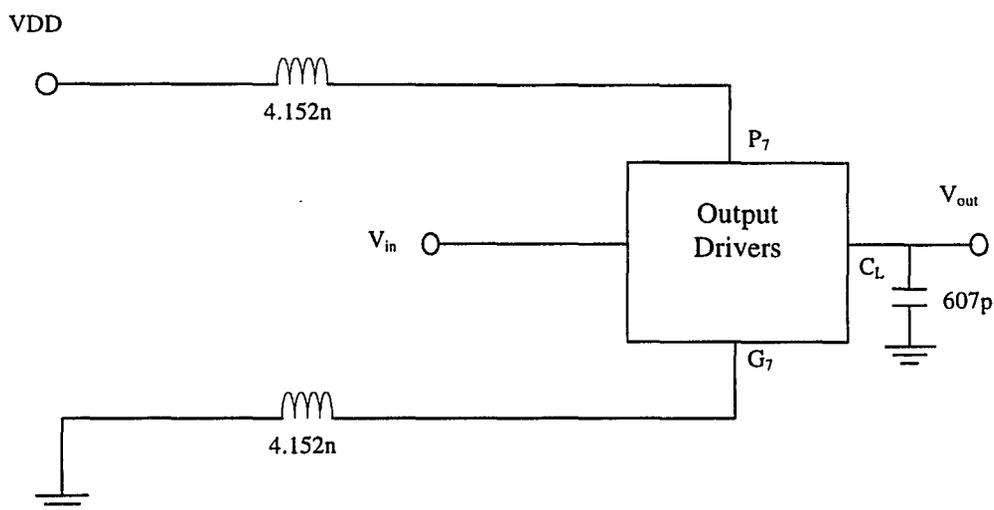
Figure 4.5 - Simplest 132 Pin Package Model (Lumped Inductors)

Figure 4.6 and Figure 4.7 plot the resulting HSPICE/Saber VDD waveforms at

the die pad for the two networks. The oscillations beginning at 15 ns correspond to a H-L

output transition. The oscillations starting at approximately 65 ns are the area of interest,

where the outputs are switching from low to high. Note that the two simulated

waveforms are virtually identical, despite the greatly different package model

complexities. This demonstrates that the driver model and the series inductance are the

dominant contributors to the power noise waveshapes. This simple model is very quick

and easy to set up, since series inductance is the only packaging parameter that needs to

be estimated.

More importantly, the simulated and measured (Figure 4.3 - C) waveforms match reasonably well, particularly in amplitude. The maximum switching noise amplitude is the most critical measure of interest for this investigation. Although other waveform traits can be important, they are much more difficult to accurately simulate and predict than amplitude. Maximum noise level is assumed to give a good measure of the severity of a switching noise waveform, and is the focus for most of this research. For the ground noise case, the maximum positive peak is defined as the maximum noise level. Conversely, in the VDD noise case, the maximum negative or down excursion is of interest, that is VDD_{nom} - VDD_{min} is the maximum VDD switching noise. In this example:

Maximum measured VDD noise (Figure 4.3):   5.0 - 3.55 = 1.45 volts

Maximum Simulated VDD Noise (Figure 4.7):   5.0 - 3.5 = 1.5 volts

The simulated noise maximum is within 3.5% of the measured value with a basically similar waveshape, showing excellent correlation.
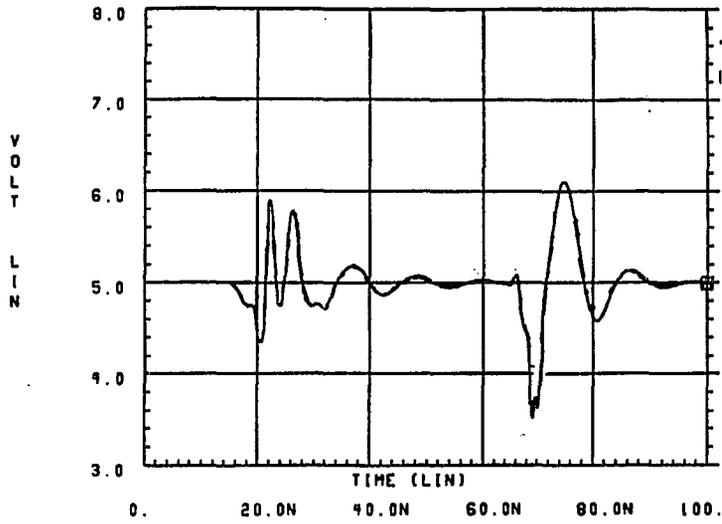
Figure 4.5 - VDD Waveforms for the Complex Network of Figure 4.3
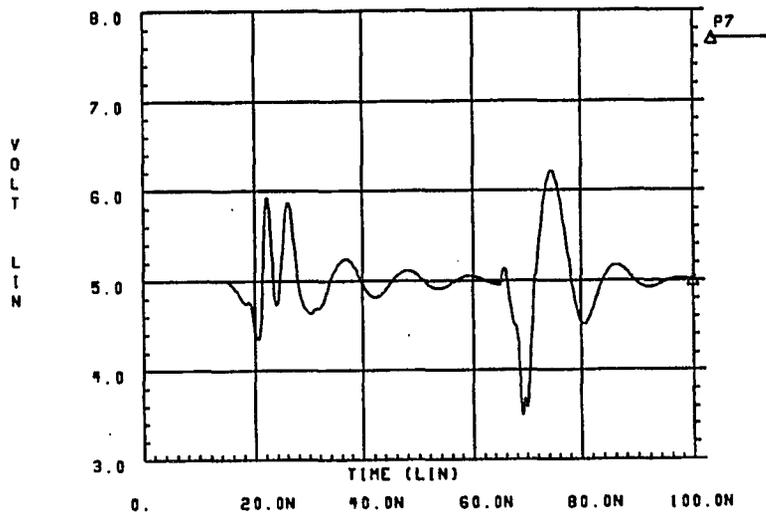
Figure 4.6- VDD Waveforms for the Simple Network of Figure 4.4

4.3 Example Case 2: National Semiconductor 0.8µ Test chip

It is desirable to have more than one example to verify a modeling and simulation methodology. A test chip using a more advanced National Semiconductor 0.8 micron process was fabricated. The test chip contained a variety of driver types with differing drive strengths and configurations, and a controllable switching arrangement. The drivers were much faster and more complex than those in the previous data processing ASIC. There are 26 total outputs, six each of four different drivers, and two stronger clock drivers. Test vectors were created to switch on these drivers in various combinations.

Figure 4.8 shows the simplified test chip package and test setup model used for ground bounce simulations. The model includes the test chip package, tester traces, and the test socket. The package has 80 total external I/O, with 6 allotted for ground, and 6 for VDD.
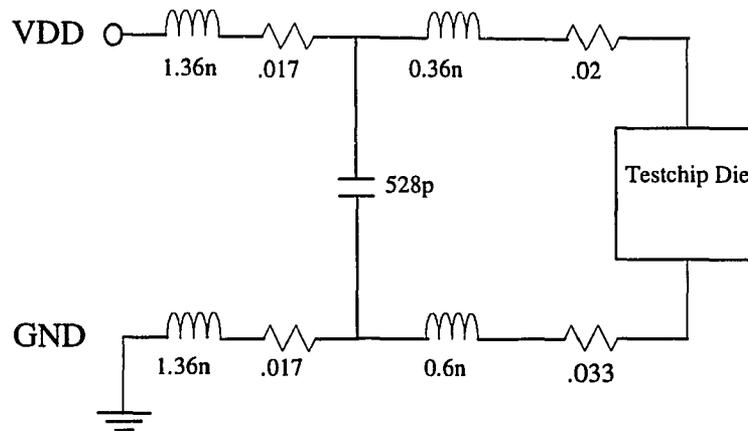
Figure 4.8 - Test Chip Ground and Power Distribution Simulation Model

The test chip test vectors were run with VDD = 5 volts, and room temperature.

Figure 4.9 shows the measured ground bounce at the die for 26 SSOs. The leftmost

positive peak and subsequent ringing is the area of interest. Figure 4.10 is the simulated

ground bounce for the same conditions. Note the different time and voltage scales for

these two figures. The comparisons are shown in Table 4.1.

	Maximum Ground Noise	Oscillation Frequency	Oscillation Damping (τ)
Measurement	1.5 volts	20 MHz	60 ns
Simulation	1.61 volts	45 MHz	15 ns

Table 4.1 - Test Chip Simultaneous Switching Noise Measurement and Simulation
Results
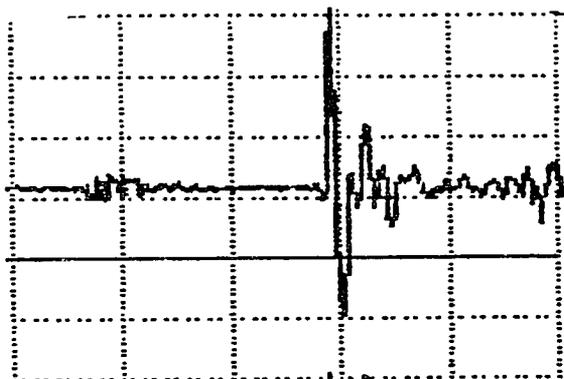
Figure 4.8 - Measured Test Chip Ground Bounce Voltage, 26 I/Os switching, VDD=5V, 25°C, Vertical Scale = 500 mv / div., Horizontal = 100 ns / div.
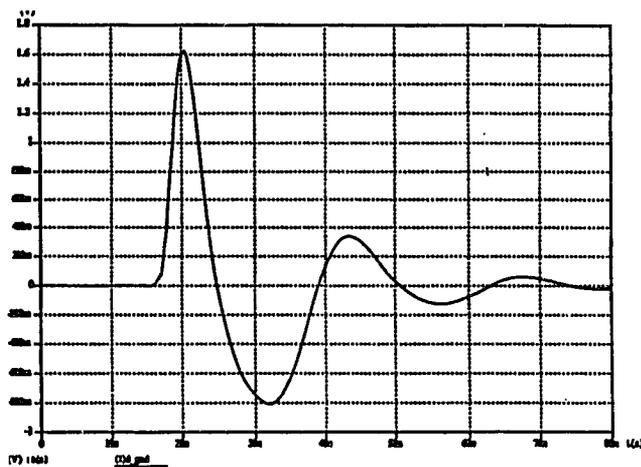
Figure 4.9 - Test Chip Simulated Ground Bounce Voltage, Vertical Scale = 200 mv / div., Horizontal = 10 ns / div.

The simulated ground noise maximum is within 7.5% of the measured value. As stated previously, maximum noise amplitudes are the key results in this investigation. Note that the oscillation frequency and damping are not in close agreement, as was also previously discussed. That is the limitation of the simplified power distribution modeling approach chosen here, and it results from the difficulty in obtaining accurate parasitic element information, as well as from the first level approximations represented by use of only a few lumped elements.

Figure 4.11 shows the maximum amplitude ground bounce simulation results for a variety of simultaneous switching output configurations. The trend lines illustrate reasonably good correlation between measured and simulated performance. The most difficult part of correlating measured and simulated results in this case is the inaccuracy of MOSFET device models. Semiconductor manufacturers have accurately determined worst case and best case models through careful process characterization and measurements. Normally, designers have access to best, typical, and worst parameters for process device models. This is sufficient for designing with performance endpoints in mind. For the purposes of this investigation, this is all we need to determine worst case noise and delay performance. Correlation of measurements and predictions for a specific test case is a different story however. We have no way of knowing exactly which process model to use for an isolated example. It will be somewhere between worst, typical and best, but one of these three must be chosen since that is all we have. For this particular example, test chip characterization showed the process to be fairly typical. When

comparing test results with simulations, the best we can hope for is that the results will be

fairly close in amplitude, with similar trends, as shown here.
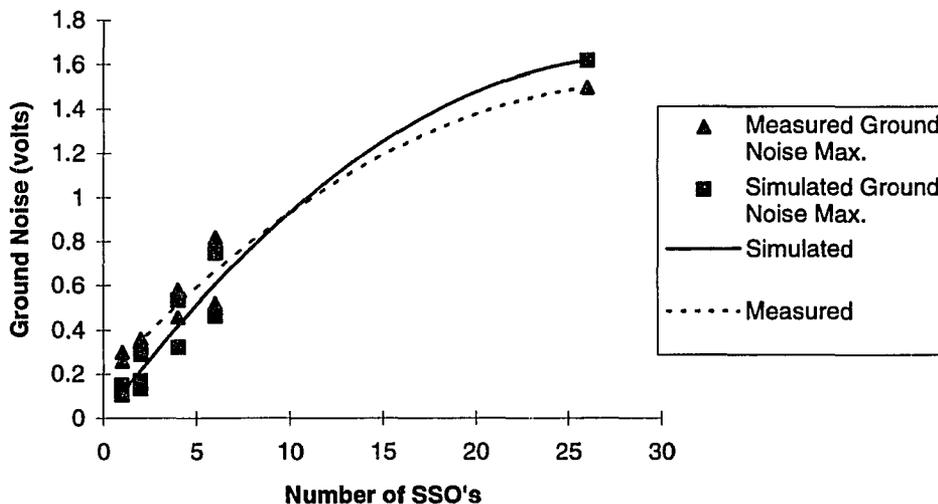
Figure 4.11 - Maximum Test Chip Ground Bounce: Measured vs. Simulated

From the results of the previous two examples, a simple simulation methodology

can be deduced. In both examples, the simulation results are reasonably accurate despite

device model ambiguity. Based on this, we can confidently deduce a simple modeling

and simulation·methodology, and proceed with a detailed simulation investigation of

simultaneous switching noise. The modeling of the power and ground distribution

networks is simplified to its series inductance and if necessary, resistance components.

The resistance component, unless large (ohms), will mainly effect oscillation damping,

but not peak noise amplitudes. The driver, however, should be a detailed transistor level

model which includes the predriver if possible. Determining a satisfactory behavioral
model for the drivers is difficult for two reasons. First, the actual driver output is a very
complex waveform. Second, the output varies a great deal with the number of SSOs, the
temperature, and processing.

4.4   Simultaneous Switching Noise Dependencies on Various Parameters

It is of interest to determine which portions of the IC have an influence on power and ground bounce simulations. Including the remaining I/O which are not members of a particular SSO group can have a significant impact on the power and ground system loading, and therefore on the resulting SSO noise waveforms. The effect of on-chip clock drivers, flip-flops and other logic will depend on the package power and ground distribution system. If there is no separation of power to the I/Os and the core, all of the circuitry on the chip will directly influence SSO noise. A high output, high speed CMOS IC and package which does not have separate core and I/O power distribution is particularly susceptible to on-chip noise problems. For this study, it is assumed that that there is a separation of core and I/O power and ground at the board, or more likely after some package power and ground planes. If this is the case, all core circuits will be only indirectly connected to I/O power and ground, so their loading effect will be ignored when modeling and simulating SSO noise.

Now, let us investigate the dependencies of SSO noise on a variety of parameters. A large number of HSPICE and Saber simulations were performed using the methodology of section 4.3. The package model used is the 256 pin package with internal planes described in Chapter 3. This includes 24 VDD, and 28 Ground pins. A proprietary Delco Electronics CMOS output driver was chosen. This is a non-inverting

driver with staged turn-on output stages to help reduce SSO noise. The following
parameters were varied, with the specified ranges of variation:

- Inclusion of non-switching I/Os

- Number of SSOs, n   1 to 256, by factors of two

- Temperature   -55, 25, 135 °C

- Processing   Best, Typical, Worst

- Output Capacitance Loading 25 to 400 pF

- Power supply (VDD)   4.5 and 5.5 volts

- Series Inductance   0.125 x nominal to 16 x nominal

- Output switching skew   0 to 2 ns

- Power supply capacitance 500 pF to 4 μF

Normal power supply variation is $\pm$ 10% or better. The worst case noise will
occur at maximum VDD, so VDD = 5.5 volts (+10%) was chosen for all simulations,
unless otherwise specified.

In many of the following plots, n will vary from one to 256 by factors of two.
However, the actual maximum n possible for this particular package is 204, which is the
number of signal pins available.

For all the following ground plots, the noise specified is the maximum peak voltage at the die ground connection. The VDD noise specified is the negative difference voltage, or the nominal VDD minus the lowest VDD spike (negative peak). This corresponds to the minimum VDD level as the outputs switch. Unless specified, the load for each output driver is 50 pF for all subsequent simulations Typical driver input and output voltage waveforms are shown in Figure 4.12. Typical ground bounce and VDD bounce voltage waveforms are plotted in Figure 4.1 and Figure 4.14. The maximum peak noise voltage is the salient feature of ground bounce waveforms, while the negative going peak is of primary interest for VDD bounce waveforms. Since both noise peaks are less than 0.3 volts, they are relitively harmless switching noise waveforms.
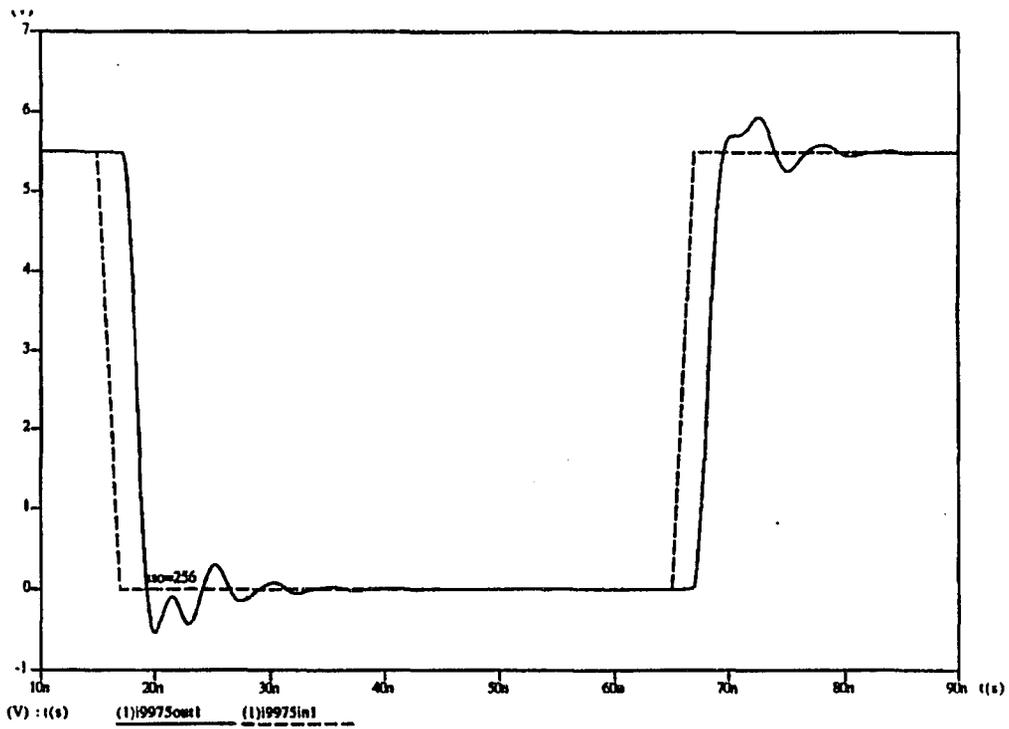
Figure 4.11 - Typical Driver Input (dashed) and Output (solid) Voltage Waveforms
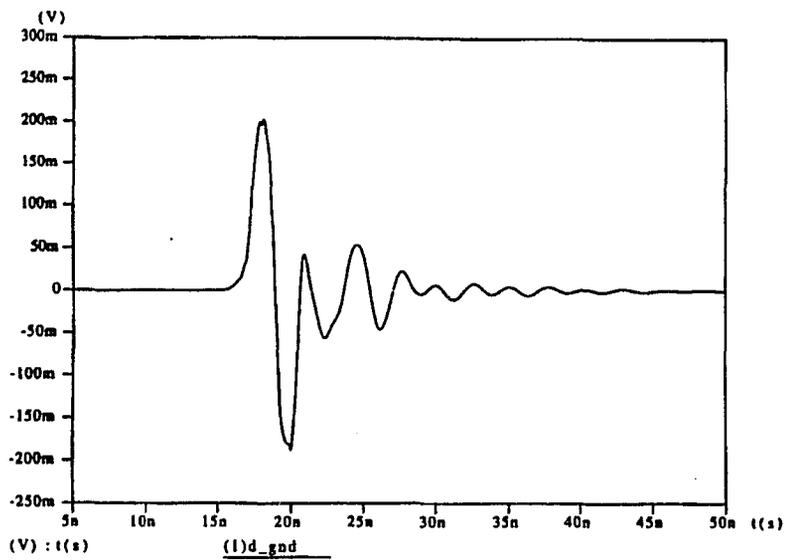
Figure 4.12 - Typical Ground Bounce Voltage Waveform
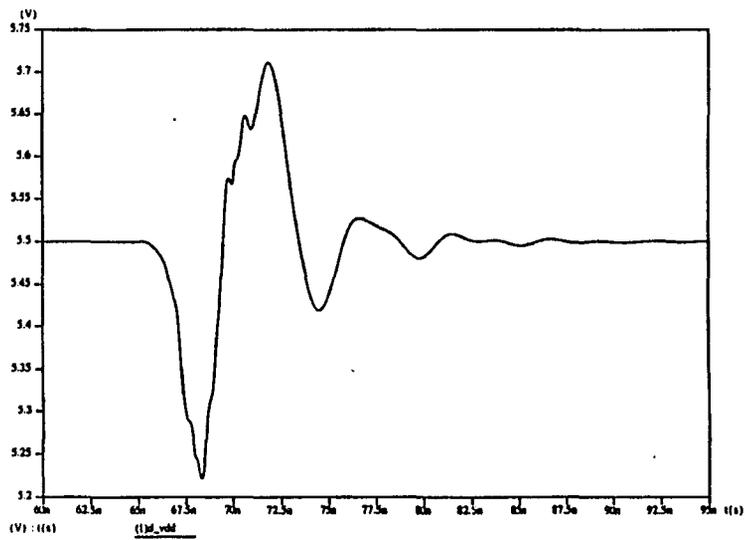
Figure 4.13 - Typical VDD Bounce Waveform

4.4.1 Non-Switching I/Os

As chip I/O counts increase, the potential for a significant number of non-simultaneously switching I/Os (non-SSOs) increases. Is the loading effect of these non-SSOs significant? Again using the methodology of section 4.3, simulation results for 32 SSOs while the number of non-SSOs was varied from 0 to 172 are shown in Table 4.2. The package of interest contains 204 total I/O, therefore the maximum non-SSO count is 172. The ground bounce is reduced by 20 %, and the VDD bounce is reduced by 28% when considering non-SSOs. Clearly, their effect must be considered when estimating Ground and VDD bounce. While non-SSOs help reduce ground noise, it must also be noted that as the number of SSOs increases, the number of non-SSOs decreases.

Non-SSO Count	Ground Noise (volts)	VDD Noise (volts)
0	.254	.308
25	.252	.278
50	.234	.26
100	.219	.233
172	.202	.222

Table 4.2 - Ground and VDD Switching Noise for 32 SSOs, vs. Non-SSO count.

4.4.2 <u>Temperature</u>

Temperature has a large effect on MOSFET performance, and therefore should have a significant influence on switching noise. Simulations were run over a full range of processing and temperatures as the number of SSOs was varied from 1 to 256 by factors of two. Best, typical and worst case National Semiconductor MOSFET processing models were used.[91] The temperatures chosen cover the military range limits of -55°C, 25°C and 135°C. Figure 4.15 shows the best case ground noise for three different temperatures as the number of SSOs is varied from 1 to 256. As expected, temperature has a significant effect on switching noise. The noise is seen to drop by approximately 50% as temperature increases from -55 to 135°C. Figure 4.16 illustrates a similar trend for best case VDD noise. In order to more closely determine the relationship between temperature and switching noise, the data is rearranged to plot noise vs. temperature for different numbers of SSOs (Figure 4.17 and Figure 4.18). Although the relation is slightly nonlinear, a linear approximation is a fairly good first order estimate. Plots of noise vs. temperature and the number of SSOs for typical and worst process are given in section 4.4.3.
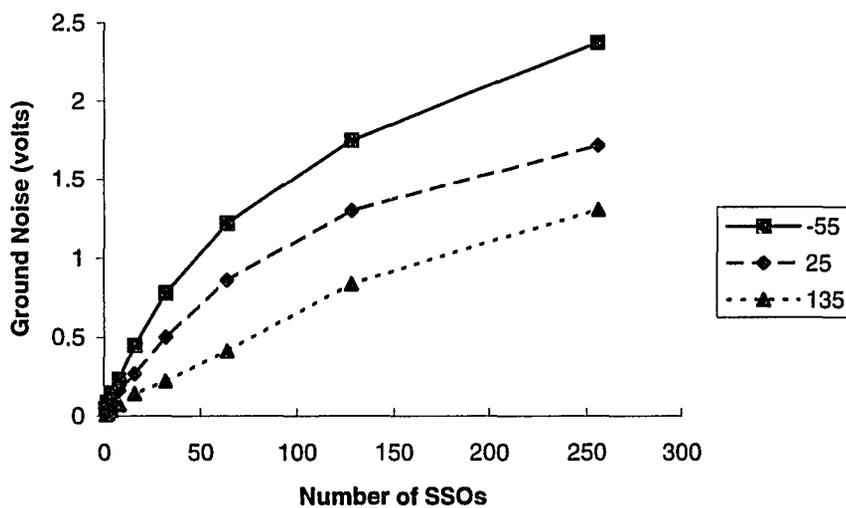
Figure 4.15 - Ground Bounce vs. Number of SSOs, Temperature = -55, 25, 135 °C, Best Process
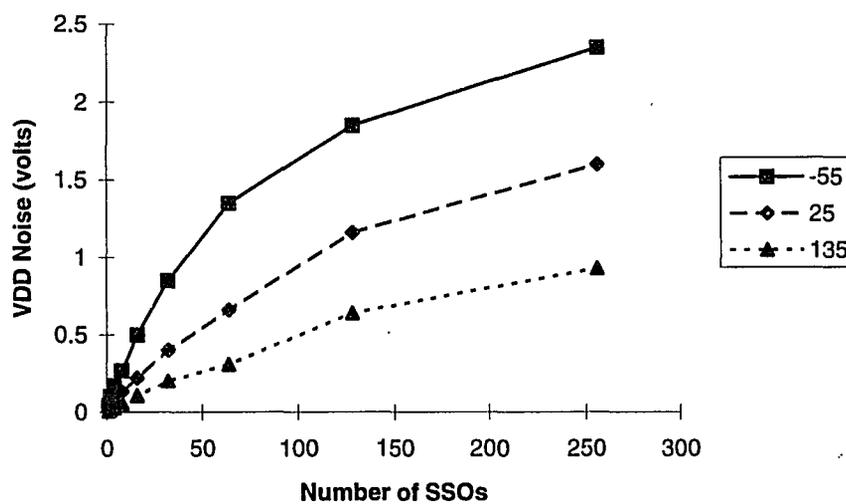
Figure 4.16 - VDD Bounce vs. Number of SSOs, Temperature = -55, 25, 135 °C, Best Process
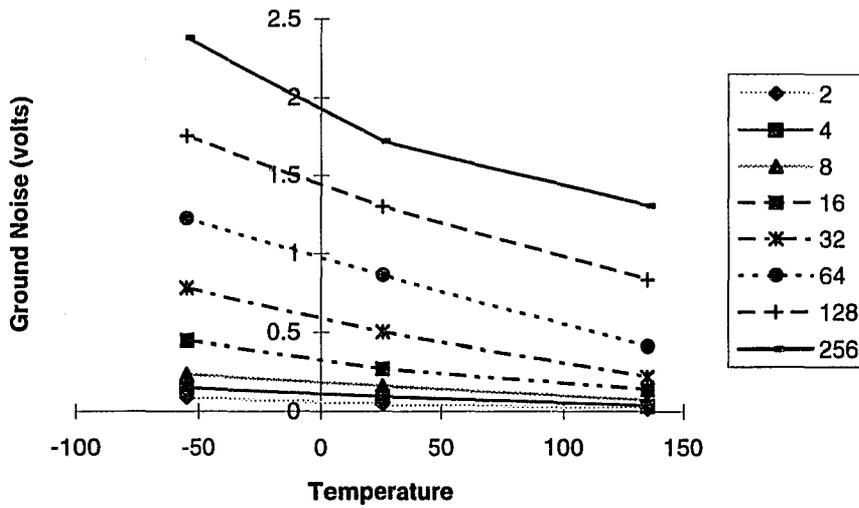
Figure 4.17 - Ground Noise vs. Temperature, SSO = 2 to 256, Best Process
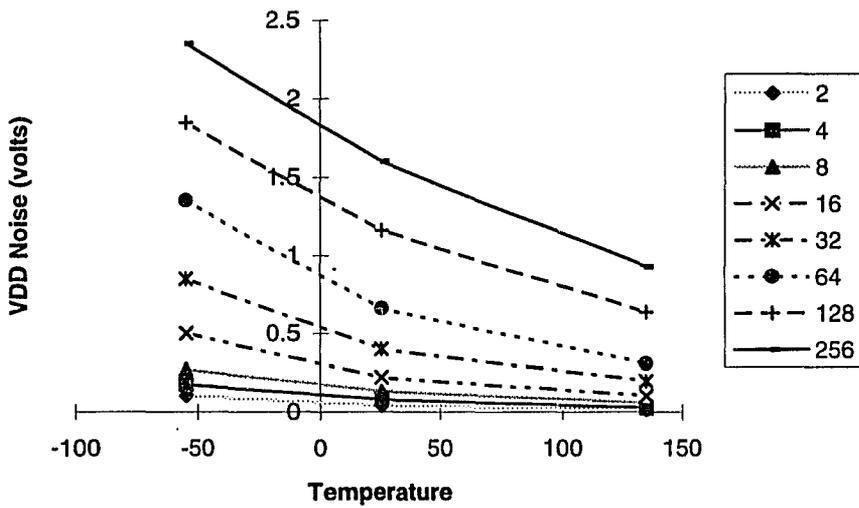
Figure 4.18 - VDD noise vs. Temperature, SSO = 2 to 256, Best Process

Figure 4.19 plots the maximum, best processing current of an NMOSFET as a

function of temperature. The trend here is very similar to that exhibited in the previous

noise vs. temperature plots. This suggests normalizing the switching noise to this

maximum MOSFET drain current, shown for ground noise in Figure 4.20. This is fairly

flat relationship, particularly for lower temperatures, which is the area of higher current,

and therefore of most interest. Thus, if a value of switching noise is determined

(measured or simulated) at room temperature, the worst case noise as far as temperature is

concerned could be estimated fairly well by simply scaling to the change in NMOS

current at the new temperature.
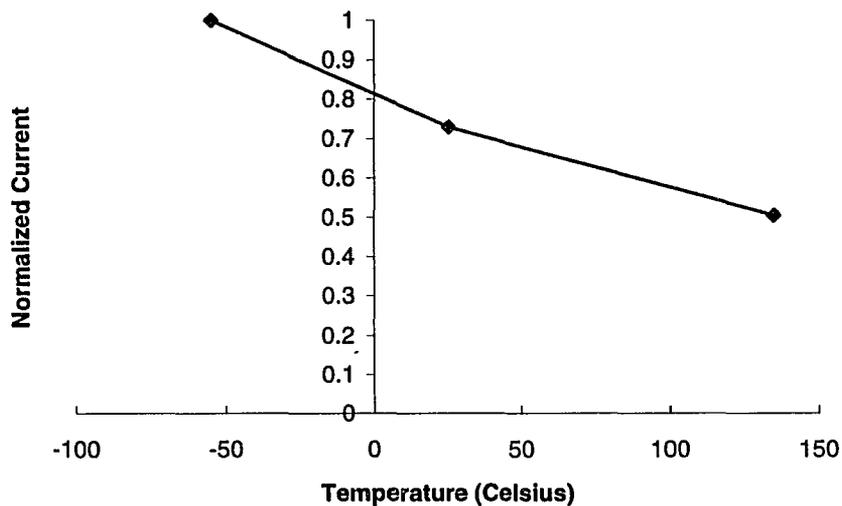
Figure 4.19 - Normalized Best Process NMOS Current vs. Temperature
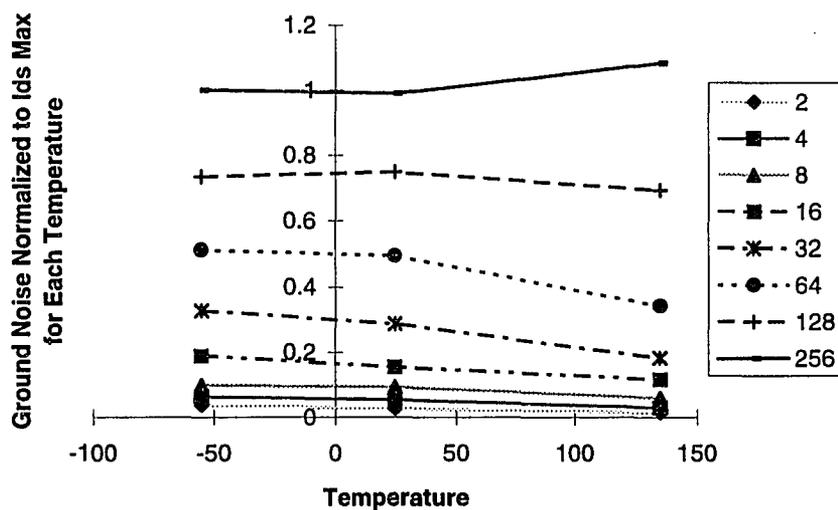
Figure 4.20 - Ground Switching Noise Normalized to Maximum NMOS Current

4.4.3 Processing

Ground and VDD noise for best case processing was discussed in section 4.4.2.

Figure 4.21 through Figure 4.28 plot Ground and VDD bounce vs. temperature and

Number of SSOs, for typical and worst processing. Although the noise amplitudes vary,

the trends are similar to the best processing case. As was expected, the maximum VDD

and ground noise voltages occur for best processing and the lowest temperature, because

that is when the driver MOSFETs have largest currents.
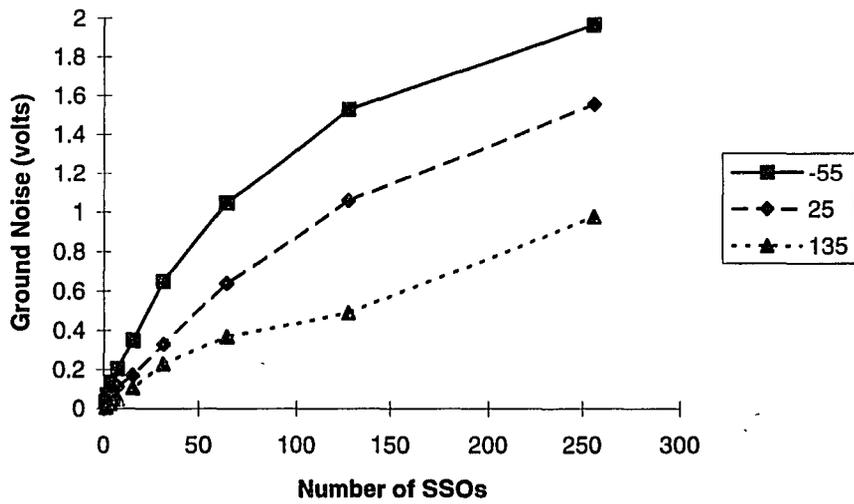
Figure 4.21 - Ground Bounce vs. Number of SSOs, Temperature = -55, 25, 135 °C, Typical Process
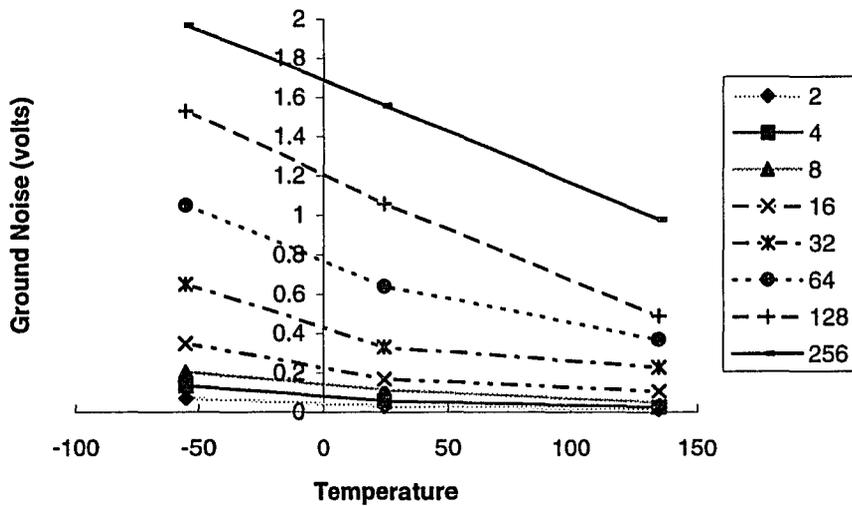
Figure 4.22 - Ground Noise vs. Temperature, SSO = 2 to 256, Typical Process
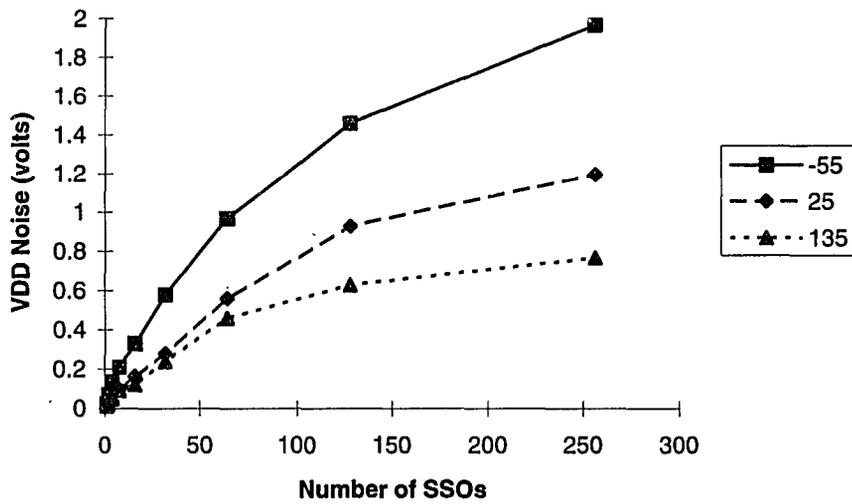
Figure 4.23 - VDD Bounce vs. Number of SSOs, Temperature = -55, 25, 135 °C, Typical Process
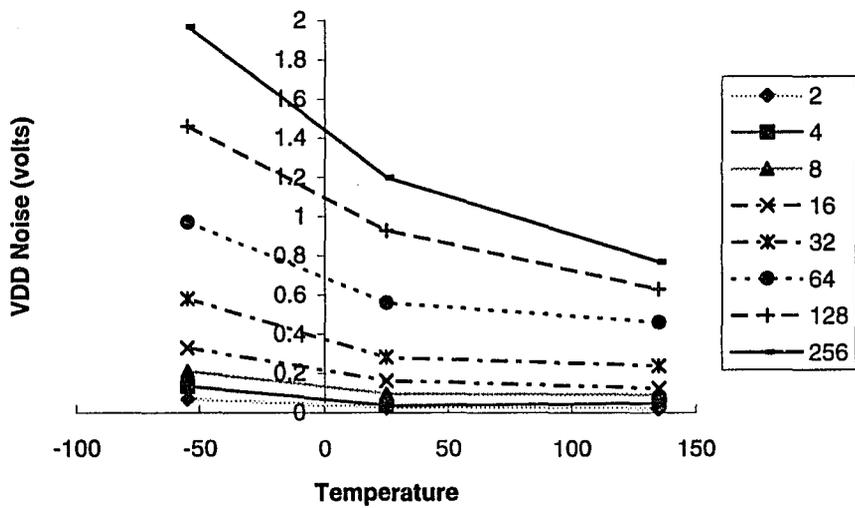
Figure 4.24 - VDD Noise vs. Temperature, SSO = 2 to 256, Typical Process
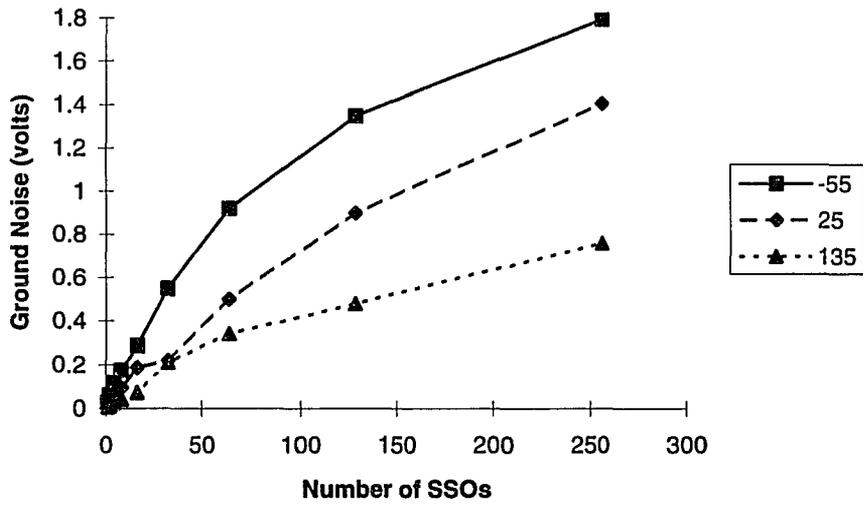
Figure 4.25 - Ground Bounce vs. Number of SSOs, Temperature = -55, 25, 135 °C, Worst Process
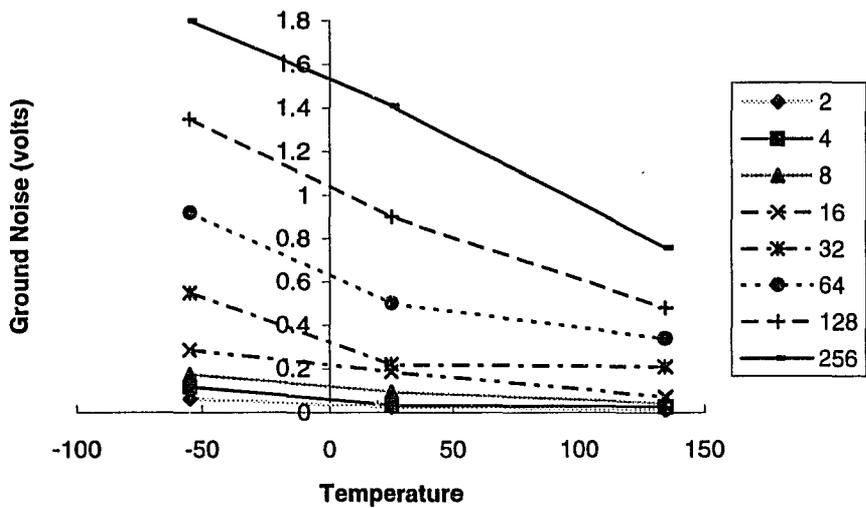
Figure 4.26 - Ground Noise vs. Temperature, SSO = 2 to 256, Worst Process
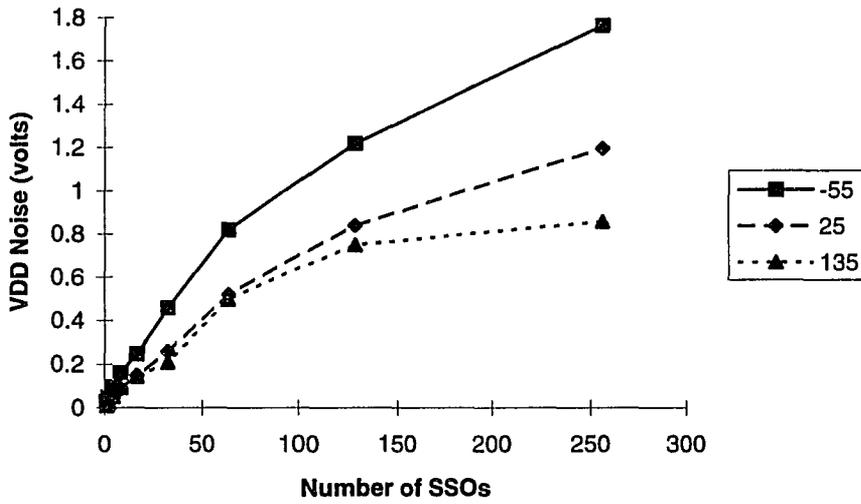
Figure 4.27 - VDD Bounce vs. Number of SSOs, Temperature = -55, 25, 135 °C, Worst
Process
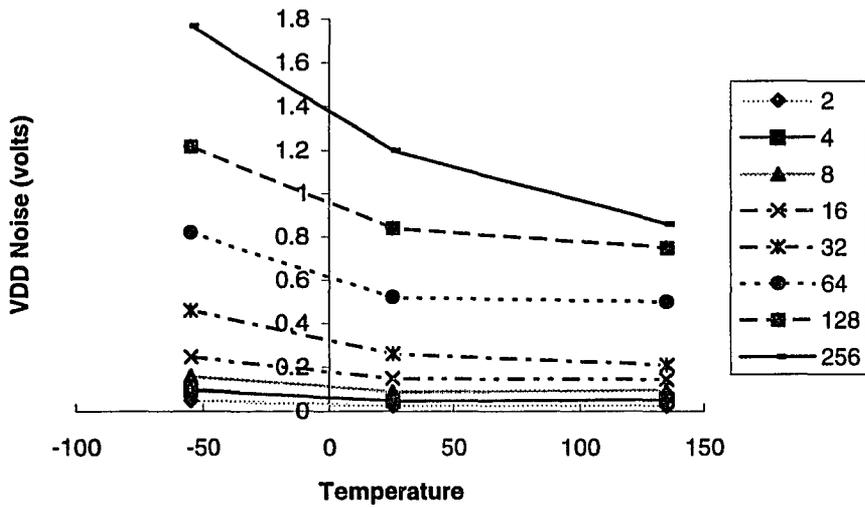
Figure 4.28 - VDD Noise vs. Temperature, SSO = 2 to 256, Worst Process

Processing has a strong effect on MOSFET performance, which implies a significant influence on switching noise. Plotting the previous results in a slightly different manner will illustrate this effect (Figure 4.29 - Figure 4.32). We can look at the maximum switching noise variation at the process extremes by defining:

$$\text{Percent Noise Variation (Process)} = \frac{\text{Best Process Noise - Worst Process Noise}}{\text{Best Process Noise}} \times 100$$

This quantifies the relative effect of process on switching noise. Figure 4.33 through Figure 4.36 show the percent noise variation at the process extremes to be 20 - 40% for this example package and driver circuit. Although significant, this is a somewhat lesser effect than temperature for this case.

It is important to note that this result only applies to this particular National Semiconductor 0.8 micron process. Other National processes, or other semiconductor manufacturer's processes may indeed yield different best to worst variances. This will be illustrated in a later example (see sections 4.4.4 and 4.4.5). The looser the process control, the more difficult the simultaneous noise problem becomes. Circuit performance must be guaranteed under worst case conditions, while noise performance is problematic at the other (best) end of operating conditions. MOSFET temperature effects are also process dependent.
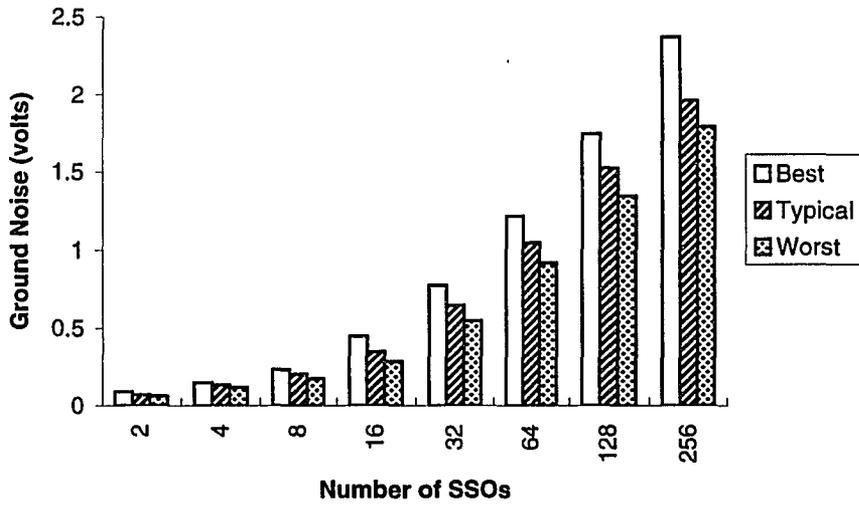
Figure 4.29 - Ground Noise vs. SSOs and Process, Temperature = -55
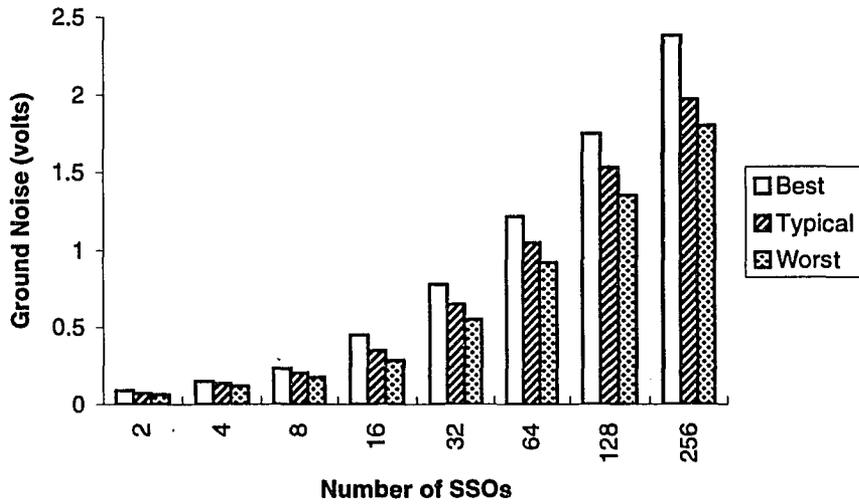
Figure 4.30 - Ground Noise vs. SSOs and Process, Temperature = 25
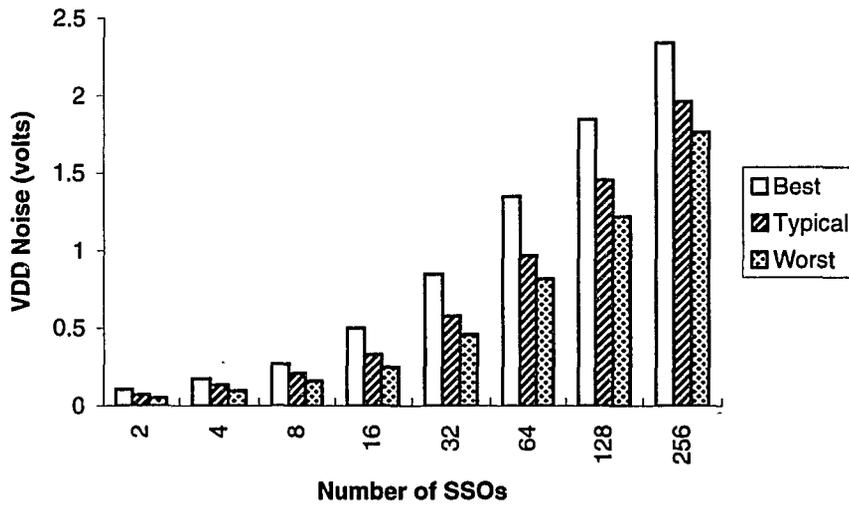
Figure 4.31 - VDD Noise vs. SSOs and Process, Temperature = -55
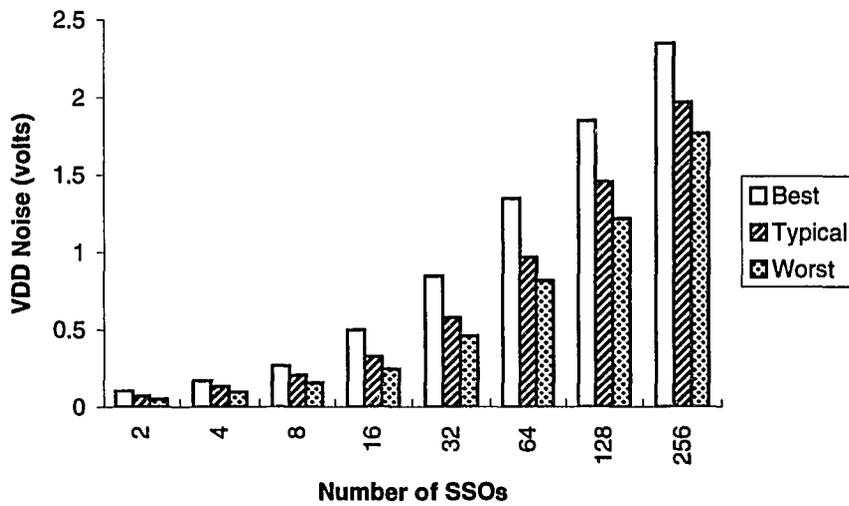
Figure 4.32 - VDD Noise vs. SSOs and Process, Temperature = 25
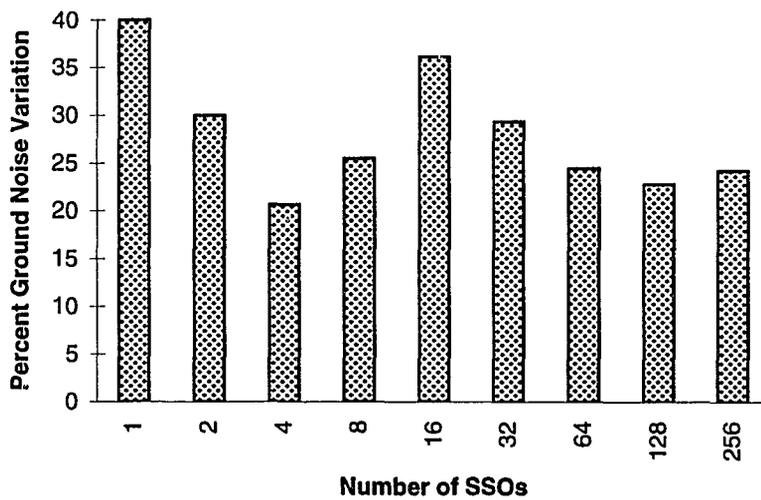
Figure 4.33 - Percent Noise Variation, Best to Worst Process, -55°C
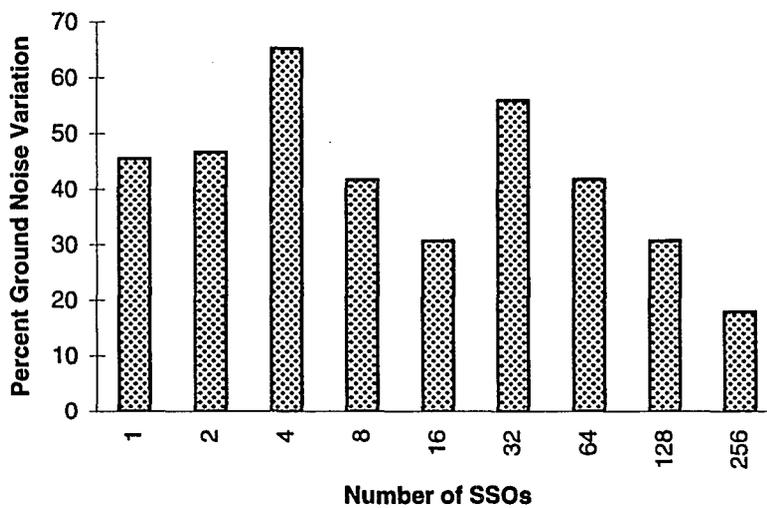
Figure 4.34 - Percent Noise Variation, Best to Worst Process, 25°C
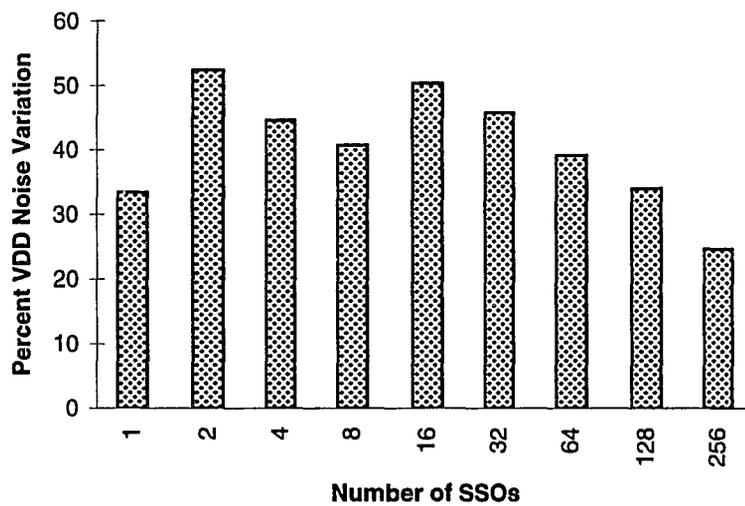
Figure 4.35 - Percent Noise Variation, Best to Worst Process, -55°C
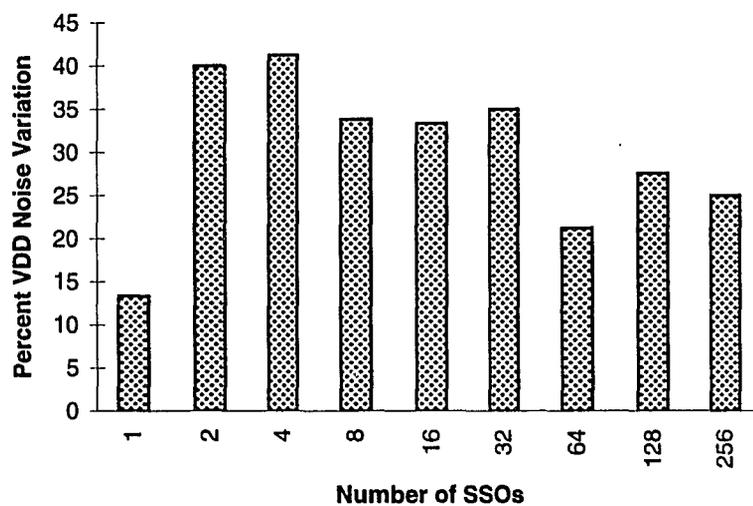
Figure 4.36 - Percent Noise Variation, Best to Worst Process, 25°C

4.4.4 Power Supply Effects

For these next two sections, a somewhat different circuit was simulated. The package and circuits themselves are only slightly different from those used elsewhere in this chapter. The main difference is the use of an older process line, with larger differences between best case and worst case parameters. This is not significant in illustrating the effects on sections 4.4.4 and 4.4.5, but it is important not to compare exact noise results from these two sections with those obtained elsewhere.

Table 4.3 summarizes maximum ground noise effects for the eight permutations of the following parameters:

VDD   4.5, 5.5 volts

Processing   Best, Worst

Temperature   -55°C, 135°C

The ground noise is normalized to the worst case value (VDD = 5.5, best process, -55°C). All cases include 16 switching outputs, and 112 non-switching outputs, representing a data or address bus switching in a 160 pin package, with 128 total signal pins, 16 ground pins and 16 VDD pins.

VDD,Temp., Process	Normalized Ground Noise	Delta VDD	Delta Process	Delta Temp.	Average Estimate	Error
5.5,-55,Best	1					
5.5,-55,Worst	0.461		0.461		0.512	0.9
5.5,135,Best	0.673			0.673	0.701	0.96
5.5,135,Worst	0.353		0.525	0.766	0.358	0.988
4.5,-55,Best	0.665	0.665			0.693	0.96
4.5,-55,Worst	0.35	0.758	0.526		0.354	0.988
4.5,135,Best	0.45	0.668		0.676	0.485	0.927
4.5,135,Worst	0.242	0.684	0.538	0.692	0.248	0.977
Ave Effect		0.693	0.512	0.701		

Table 4.3 - Average Endpoint Power Supply, Process and Temperature Effects

The focus of this section, the effect of only changing VDD from 5.5 to 4.5 volts (standard ±10% supply specification), is reflected in the Delta VDD column. On the average, the ground noise is reduced to 69.3% over the range of VDD. This result is a bit deceiving, since the operating range of all inputs is also reduced with VDD. For TTL level inputs, the maximum low input specification is constant at 0.8 volts, but the switching point for CMOS circuits is approximately VDD/2. Thus, as VDD changes from 5.5 to 4.5 volts, the switching point changes from 2.75 volts to 2.25 volts. Therefore, absolute CMOS circuit noise immunity is lowered as VDD decreases, reducing the lower noise benefit for low VDD.

4.4.5 Combining Temperature, Processing, and VDD Level Effects

From the previous noise voltage results, it is obvious that the effects of temperature, processing and supply voltage are cumulative. Could the effect of these together with voltage be predicted knowing only the individual effects of each? Table 4.3 summarizes maximum ground noise voltage as VDD, process and temperature are varied to their various endpoints. The effects of varying a single parameter are shown in the three columns titled Delta VDD, Process or Temperature. The average of all four cases is shown below each column. Note that there is little variation of the individual values, and they are all within approximately 10% of the average.

The simplest possible noise prediction method would be to simply multiply the average individual parameter effects for a given change in operating conditions, with the maximum noise point as a reference. The Average Estimate column is the estimated result using the previously calculated average parameter effects, multiplying them where appropriate. The error column is simply the actual result divided by the estimate. The estimate is always too large, but seldom by as much as 10%. As previously discussed, it is safer to overestimate the noise, as long as the overestimate is not excessive. We can also slightly revise our approximation, knowing the general tendency to overestimate when considering cumulative effects. Decreasing each estimate by 5% results in an error of less than 5% for all endpoints. This illustrates the simple, cumulative nature of these three major noise effect parameters (VDD, process and temperature). The methodology

enables accurate noise estimates at different operating points to be predicted from a single switching noise simulation.

4.4.6 The Number of Simultaneously Switching Outputs

Many of the plots presented already include noise vs. the number of SSOs, showing the expected higher noise with increases SSO count. It is well documented elsewhere that switching noise increases at a less than linear rate with the number of SSOs, or inductance. The examples here have also shown that noise does not increase linearly with SSOs, but at a slower rate. However, although the increase has been shown to be less than linear, the decrease in rate is not as severe as concluded in many other treatments of switching noise in the literature.[92 93 94 95 96]

Much of this decrease has been attributed to the negative feedback effect of ground noise, that is, as the ground noise increases, the effective gate drive on the output transistor decreases, thereby reducing the noise. The non-square law behavior of short channel MOSFETs previously discussed results in less dramatic decreases in MOSFET drain current caused by ground noise induced gate drive reduction. This partially accounts for the somewhat different results here. Another factor contributing to the less pronounced drop-off in switching noise with SSOs is the favorable non-SSO loading effect (section 4.4.1). Non-SSO loading decreases with increased SSO count, simply

because the number of non-SSOs decreases directly with increasing SSOs. This will only be observed if non-SSOs are considered in switching noise modeling.

Many of the previous noise maxima are well above one volt, introducing another issue in noise estimation. Are the effects of various parameters changed as the amplitudes become excessive, perhaps when the maxima become a significant fraction of the VDD supply voltage? Two families of simulations were run, each varying series ground and VDD line inductance from nominal values, but with different nominal inductance values. The switching noise was normalized to the noise voltage at Lnom = 16. Figure 4.37 and Figure 4.38 show clearly that the higher nominal inductance case, and thus the higher absolute noise maxima, shows a more pronounced drop-off as inductance and noise increase, for both VDD and ground switching noise. This dependence on absolute noise voltage level further complicates noise estimation without detailed simulation. A good practice is to determine switching noise trends and parameter dependencies while ensuring the maximum noise voltages never exceed 1.5 volts. This will result in accurate noise predictions for voltages below 1.5 volts, at the expense of possible overestimation of higher switching noise situations. If switching noise predictions are above 1.5 volts, system performance is clearly marginal and needs redesign, so some overestimation is not a big concern. Accuracy is more important in a realistic switching noise operating range, below 1.5 volts.
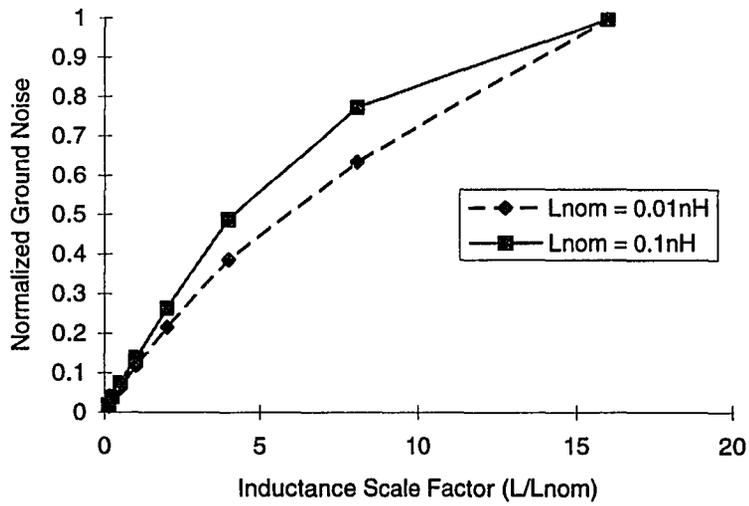
Figure 4.37 - Ground Noise as Inductance is Scaled
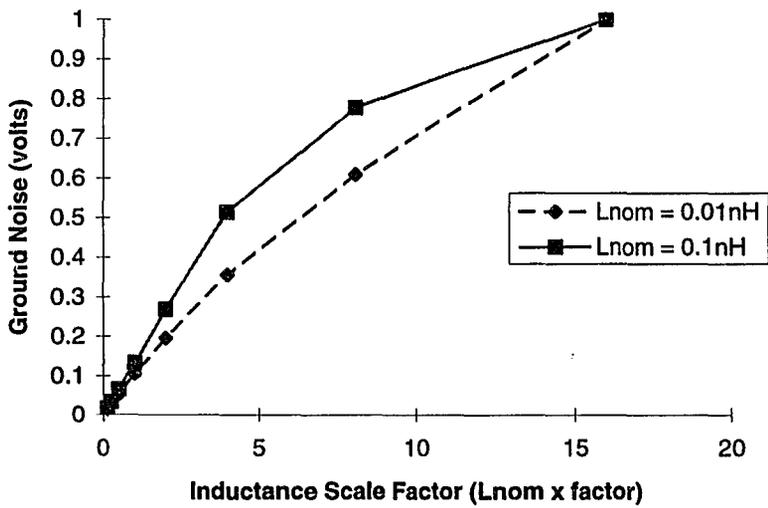
Figure 4.38 - VDD Noise as Inductance is Scaled

4.4.7 Series Inductance

The voltage across an inductor is proportional to di/dt, and inductance, L. Since the number of SSOs determines di/dt, it would seem that the effect of varying inductance would be identical to varying the number of SSOs. It has been shown that switching noise is not linear with SSOs for a variety of reasons, and the inductance should affect the noise in the same manner. A simple driver and package circuit was simulated to investigate this relationship for both VDD and ground switching noise. The switching noise for scaling SSOs and inductance equally is shown in Figure 4.39 and Figure 4.40. Although not identical, scaling inductance and SSOs is extremely, close, probably well under the errors already introduced by the different approximations in this analysis. The assumption that inductance scaling can be treated in the same way as SSO scaling for noise estimation is a very good one, as one would expect. Note that scaling series inductance is essentially varying the number of external pins allotted to power and ground, since that directly alters the effective inductance of the power distribution network.
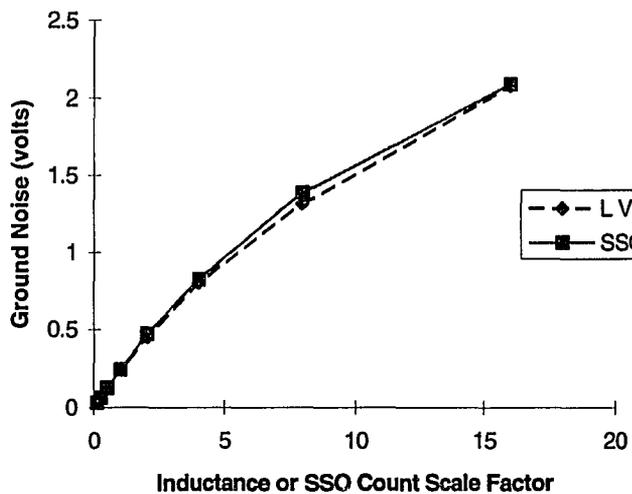
Figure 4.39 - Ground Noise vs. Equal Inductance and SSO Count Scaling
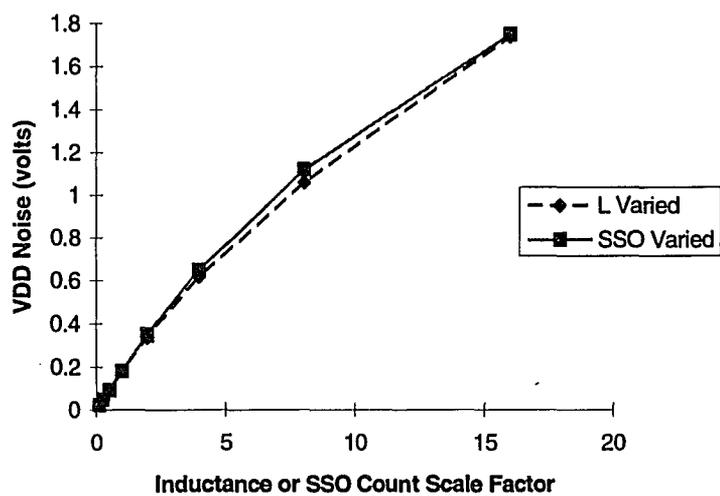
Figure 4.40 - VDD Noise vs. Equal Inductance and SSO Count Scaling

4.4.8 Power Supply Capacitance Effects

An obvious, and commonly proposed, switching noise improvement is the addition of package and/or chip capacitors between VDD and ground. Locations of these two types of capacitors are shown in the simplified schematic of Figure 4.41. L_{P1} and L_{G1} represent the total inductance from the board to the internal package planes. L_{P2} and L_{G2} contain the total inductance from the internal planes to the die pads.
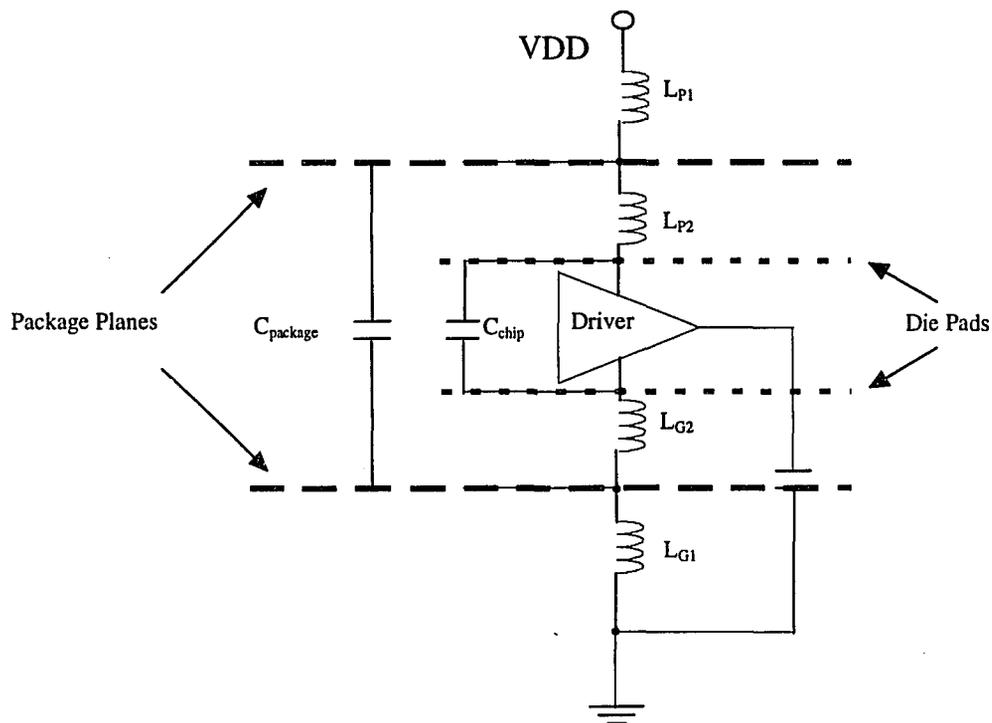
Figure 4.41 - Package and Chip Bypass Capacitor Locations

Figure 4.42 plots normalized switching noise vs. package bypass capacitance

($C_{package}$), as capacitance is varied from 1 nF to 4 μF. The switching noise is normalized

to the noise voltage for zero bypass capacitance. This particular case is for 16 SSOs,

VDD = 5.5, -55°C, and best processing. Note that increasing the package bypass

capacitance beyond a certain point (~1μF in this case) does not further decrease the

maximum switching noise. The region of lower capacitance ($C_{bypass} \leq$ 16 nF) is also of

interest. (Figure 4.43). Although the noise is reduced by about 20%, the capacitance is

increased more than an order of magnitude from 0.5 nF to 16 nF. Thus, switching noise

has a weak dependence on package bypass capacitance, and the maximum noise

reduction is approximately 35%.
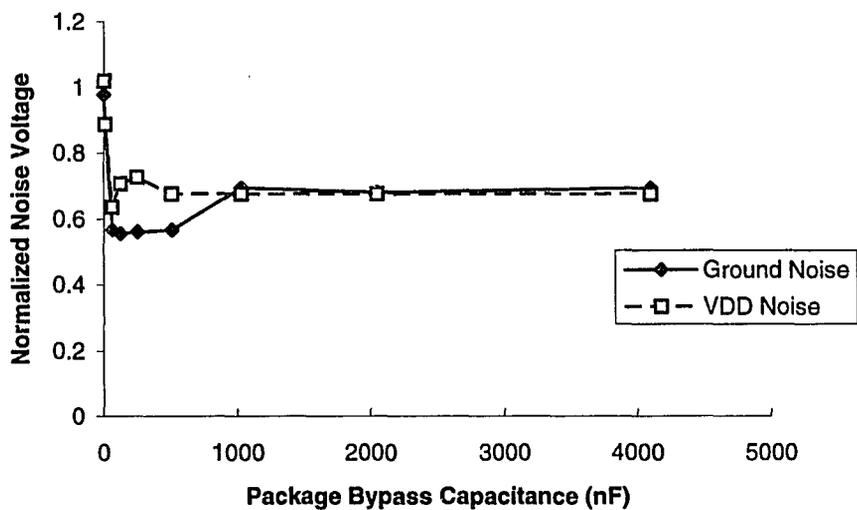
Figure 4.42 - Ground Noise vs. Package Bypass Capacitance (1 nF to 4 μF)
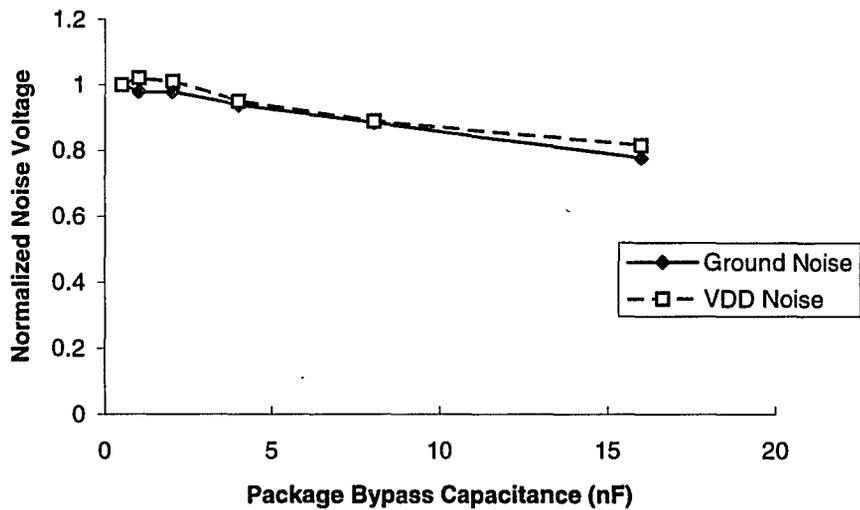
Figure 4.43 - Ground Noise vs. Package Bypass Capacitance (0.5 to 16 nF)

We can understand a bit more by looking at the current paths with these capacitors in place. The normal current path from the board through the IC package for a low-to-high output driver transition is illustrated in Figure 4.44. The switching noise is caused by large di/dt through the parasitic VDD connection inductances L_{P1} and L_{P2}. Figure 4.45 shows the current contribution from a package bypass capacitor for a low-to-high transition of an output driver. Focusing on VDD noise, this portion of the output load charging current does not pass through L_{P1}, but it still does travel through the plane to pad inductance, L_{P2}. This is the reason there is a limit to how much package bypass capacitance can reduce switching noise.

At the ground side, note that an additional ground current has been introduced through L_{G1} in completing the loop through the bypass capacitor. This extra ground noise may or may not be a concern, depending on other output drivers which could be switching high-to -low and producing significant ground current. Also, predrivers may be sizable and thus produce appreciable switching current. This is why it is advantageous to include detailed predriver as well as driver circuit models in switching noise simulations.

How much capacitance can be achieved with the intrinsic VDD plane to ground plane capacitance in the package? As an example, the approximate capacitance between two planes with area 4 x 4 centimeters, spacing 0.01 inches (0.0254 centimeters), and dielectric material with $\varepsilon_r = 10$ is C = 557 pF.

Unless the package is significantly larger than this already sizable example, it is difficult to get the plane to plane capacitance larger than a few nanofarads, since all we have to work with is spacing and ε_r, which is already quite large. This means that most of the additional capacitance must come from a dedicated package capacitor, with care taken not to introduce significant inductance in its own connections to the internal package planes.
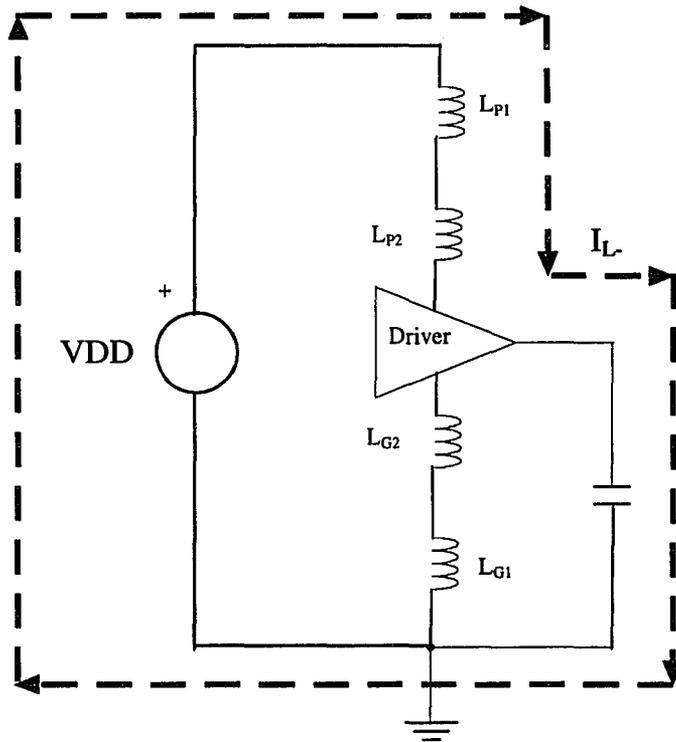
Figure 4.44 - Normal Output Driver I_{L-H} Charging Current Path
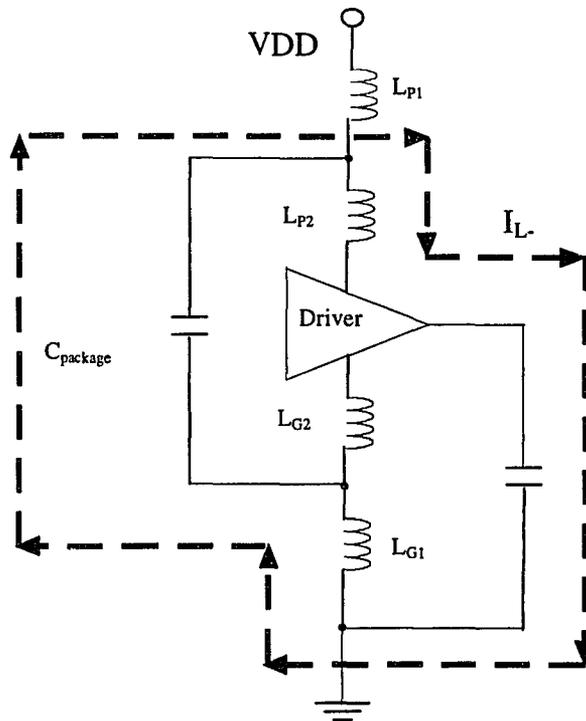
Figure 4.45 - Package Bypass Capacitor: Output Driver I_{L-H} Charging Current Path

Figure 4.46 shows a similar current path for a low-to-high output driver transition, this time for a capacitor connected at the chip. Now the charging current from the capacitor completely avoids the parasitic VDD inductances L_{P1} and L_{P2}. Once again, this is at the expense of additional ground noise current, this time through both parasitic ground inductors L_{G1} and L_{G2}. It is interesting to note that each of the current paths discussed for driving external loads contains exactly two parasitic inductances.
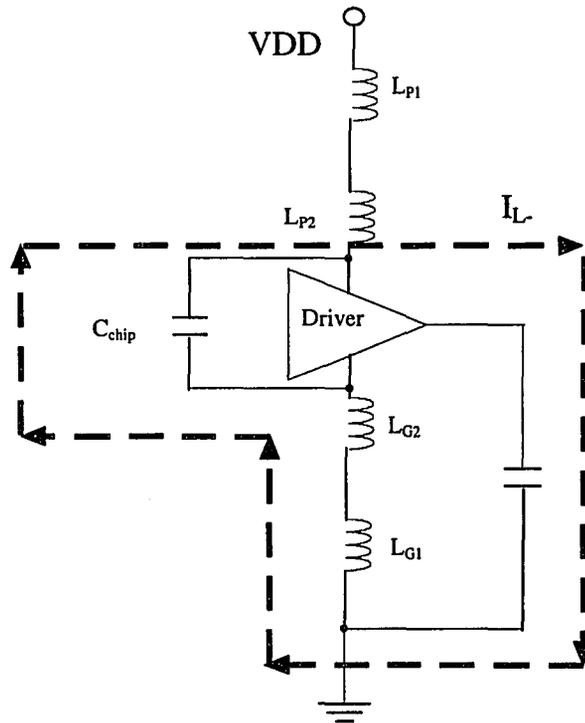
Figure 4.46 - On-Chip Bypass Capacitor: Output Driver I_{L-H} Charging Current Path

The situation is quite different when considering internal gate switching, because the internal load is referenced to internal ground. The normal low-to-high charging path through the IC package is shown in Figure 4.47. The switching current now travels through all of the parasitic package inductances, because of the internal die ground reference. This means that di/dt noise can be introduced on the ground and VDD lines, regardless of the switching transition direction. The situation is helped somewhat by increasing capacitance in the package, across the internal package planes (Figure 4.48). Now the bypass capacitor current path includes only the portions between the package planes and the die, in other words, the bond wires, bonding pads and vias, and the planes themselves. Best of all is the case where extra capacitance is added right at the die (Figure 4.49). Now the current contribution from the additional capacitor does not pass through the package at all. This reduces the overall current through the parasitic inductances, thus reducing the switching noise caused by internal gates.
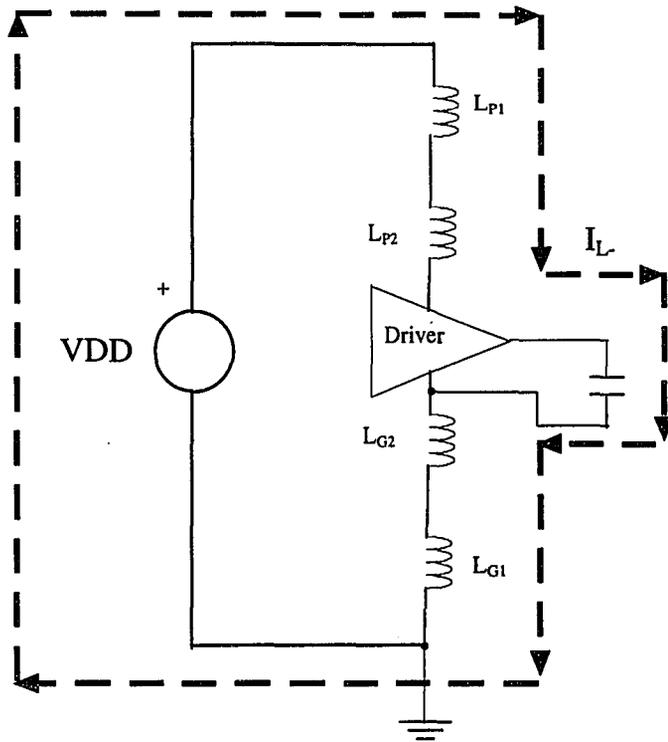
Figure 4.47 - Normal Internal Driver I_{L-H} Charging Current Path
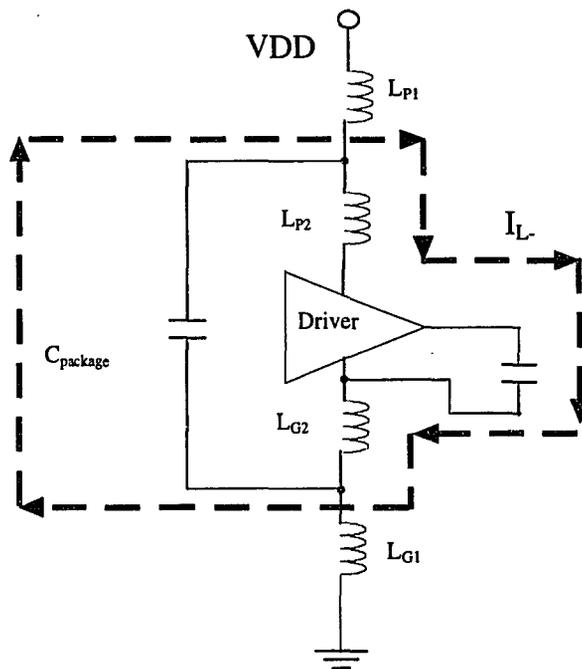
Figure 4.48 - Package Bypass Capacitor: Internal Driver I_{L-H} Charge Current Path
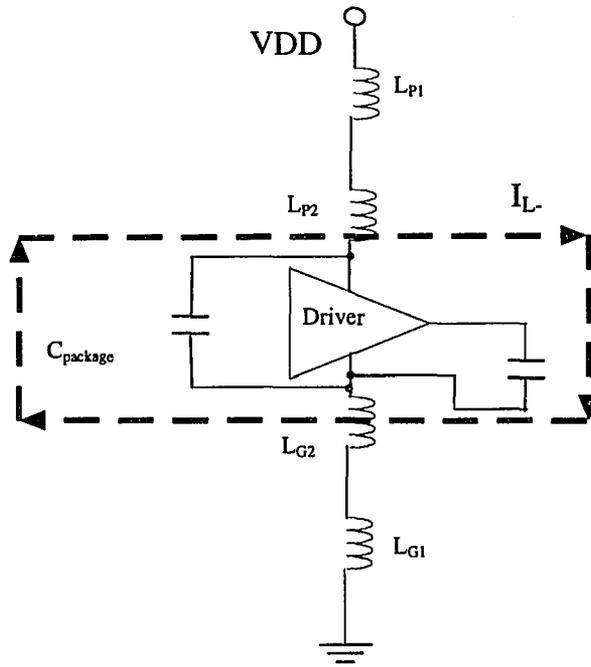
Figure 4.49 - On-Chip Bypass Capacitor: Internal Driver I_{L-H} Charging Current Path

How feasible is it to add substantial capacitance directly at the die? This is most applicable for multi-chip modules (MCM), where a capacitor can be placed on the substrate close to the IC in question.[97][98] Even then, the capacitor is not directly at the chip, and the power and ground path parasitics in the die to substrate connection will be included in any capacitor charge path. This is not perfect, but these parasitics, particularly the inductance, are smaller than a normal single die package.

There are a few options for adding capacitance on the chip. A close attached capacitor is a thin film capacitor placed on the active surface of the die.[99] This is connected to the die ground and power pads with very short wires, resulting in series inductance $\leq$ .6 nH and series resistance $\leq$ 0.05 ohms.[100] Note that 0.6 nH is still a large inductance when considering switching noise.

Another on-chip decoupling option is to employ unused area under power and ground bus metalization, and unused cell area for power-ground capacitors. For a typical chip, this can produce a power-ground decoupling capacitor of about 30 to 40 nanofarads. Internal gate switching noise is reduced by a factor of 3 to 5, and SSO noise reductions of approximately 20% have been reported.[101] As expected, on-chip decoupling dramatically reduces internal gate switching noise, but not SSO switching noise.

4.4.9 Load Capacitance Effects

Output driver load capacitance has a large effect on delay, but what is the effect

on switching noise? If we assume that the output driver will be turned on to roughly

maximum current when switching begins, and remain in that state for most of the

switching, then load capacitance should have only a small effect on di/dt noise. This is

shown to be the case in Figure 4.50 (ground noise) and Figure 4.51 (VDD noise). Both

plots have 16 SSOs, and the results are normalized to the value at -55°C and $C_{LOAD} = 25$

pF. The maximum ground noise increases by about 20% and the VDD noise by about

40%, when there is an increase in C_{LOAD} of more than an order of magnitude (25 pF to

400 pF). VDD noise did not increase for larger load capacitance, while ground noise

actually decreased slightly for such unrealistically large loads. The particular drivers used

in these simulations were designed for a 50 pF nominal, 300 pF maximum load. The

actual effect of load capacitance is not likely to be changed dramatically by the actual

driver design, but the load at which the noise maximum levels off will be a function of

driver size.
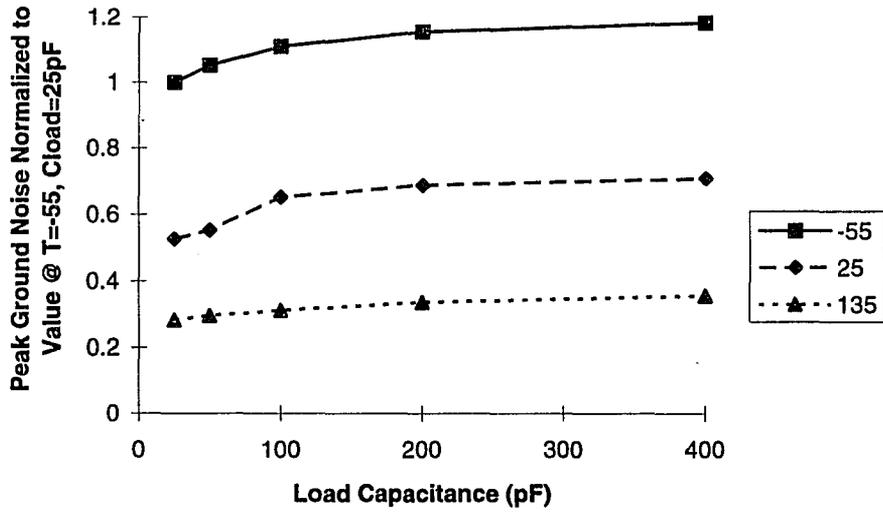
Figure 4.50 - Normalized Ground Noise vs. Load Capacitance
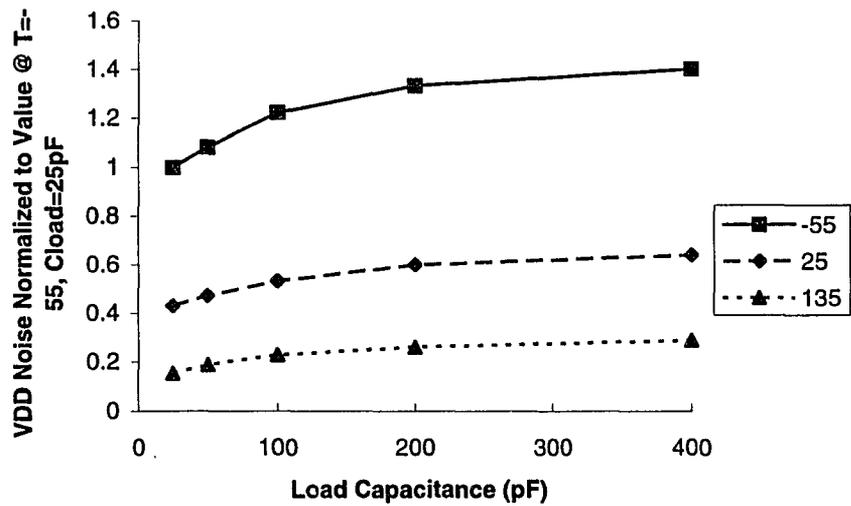
Figure 4.51 - Normalized VDD Noise vs. Load Capacitance

4.4.10 <u>Output Switching Skew</u>

As previously mentioned, most investigations of switching noise assume that all

outputs switch at identically the same time. This is not the case in practice, so it is

interesting to look at just how much the skew between SSOs affects di/dt noise. The

following conditions and assumptions were made in this section:

Best Processing

Four equally spaced and populated output switching groups

In Figure 4.52, the skew refers to the difference in nanoseconds between each

switching group. For example, for 64 total SSOs, 0.25 ns skew, we have 4 groups of 16

SSOs each, separated serially by 0.25 ns, for a total switching time difference of 0.75 ns

between the first and the last group.

Numerous simulations were done for different conditions, and different size

switching groups. Since the trends were very similar, only one set of plots for ground and

VDD noise are shown here. Plots at three different temperatures (-55, 25 and 135°C) are

shown in each graph, each with 64 total SSOs (Figure 4.52 and Figure 4.53).

The results are normalized to the maximum noise magnitude at -55°C, zero skew.

Both plots show the dramatic effect of relatively small skews. A skew of 0.5 ns between

each of the four switching groups (for a total skew of 1.5 ns) decreases the noise to 60%

of its zero skew level. It should be noted that some skew will be naturally present, while

additional skew can be purposely introduced for noise reduction. Of course, this carries

with it a reduction of system speed performance. Inherent switching skew on the order of 0.2 ns has been reported.[102]

These particular drivers are designed to have worst case delays of 4.85 ns for 50 pF load capacitance. Thus, the 1.5 ns delay added for skew noise reduction is less than 33% of the delay specification. Designing a slightly stronger driver and skewing the SSOs may result in significantly lower switching noise, while maintaining the overall 4.85 ns delay requirement. This case only serves as a example of the effects of skew, the exact numbers and requirements must be determined for each application and design. It should be noted, however, that there may be applications where it is advantageous to trade off small reductions in speed for a considerably larger reduction of noise. Such a tradeoff should not be overlooked.
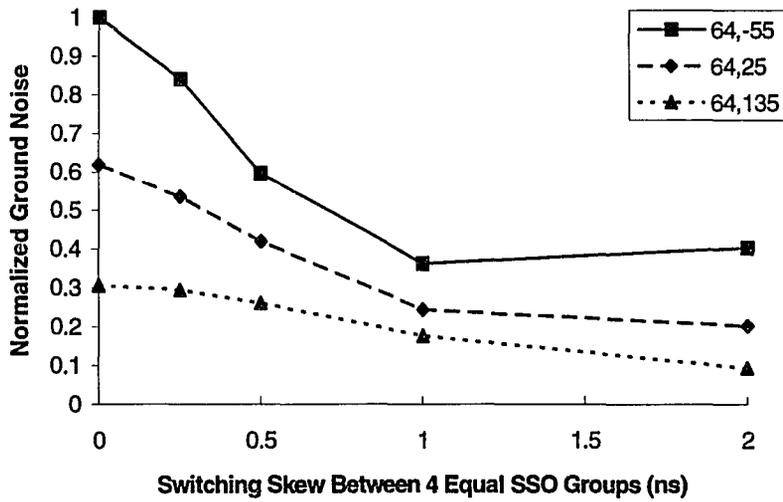
Figure 4.52 - Normalized Ground Noise vs. Output Switching Skew
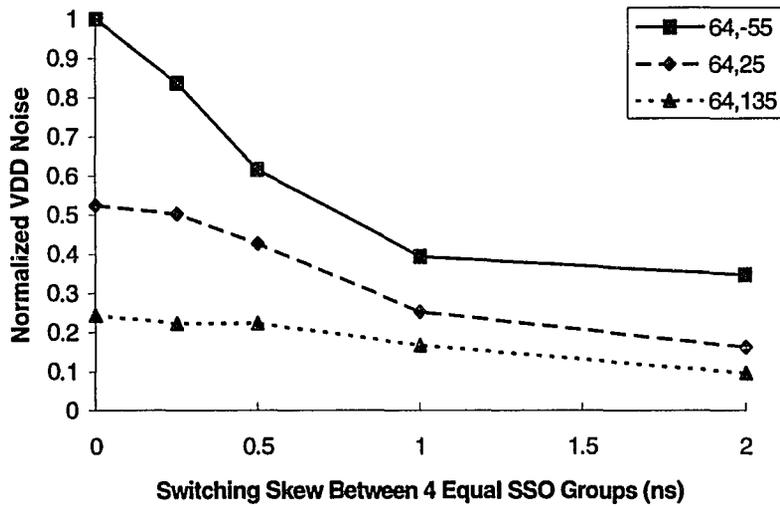
Figure 4.53 - Normalized VDD Noise vs. Output Switching Skew

Because of the R, L, and C, circuit on the ground or VDD path, switching

waveforms follow an underdamped oscillatory behavior with a damping coefficient of

$\frac{R}{2L}$, and a period which decreases with time.[103] [104] The quasi-period, or first (maximum)

period, of the underdamped current is:[105]

$$T = 2\pi \sqrt{\frac{LC}{\sqrt{1 - \frac{R^2 C}{4L}}}}$$

Consider two groups of simultaneously switching outputs, one group skewed ΔT

from the other. As ΔT is increased, a ground switching noise global minimum will occur,

followed by several local minima.[106] The global minimum for commonly used packages

and typical drive speeds is on the order of 1-2 ns.[107] This behavior can be seen in Figure

4.52, -55°C ground noise results, where the ground switching noise reaches a shallow

minimum at a delay of approximately 1 ns.

The oscillation damping and quasi-period depend on package parasitics, and

output driver characteristics. Accurate estimates of these parameters are difficult to

obtain, particularly early in the design process, making it difficult to predict noise minima

vs. delay locations. Additionally, this analysis assumes that grouped outputs switch

exactly simultaneously, and switching noise current waveforms precisely follow an

underdamped oscillatory behavior. In practice, the switching noise minima will be

shallower than predicted by this simple R,L,C model. It should be noted that the

simulations presented here do not include accurate IC parasitics, or the small random switching skew that will be present in actual hardware.

4.5 Analytic solution

As mentioned earlier, there are a number of analytic treatments of SSO noise in the literature. They generally start with the square law MOSFET current expression:

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad (4.1)$$

Actual and simulated 0.8μ device curves shown in Figure 4.1 illustrate fairly constant spacing between members of the device curve family, suggesting an exponent close to one, rather than two (Actually, the exponent on the V_{GS}-V_T term may be greater than one, but other parameters may vary with increased V_{GS}-V_T also, counteracting this).

One particular derivation produces a variety of useful expressions, starting with a square law MOSFET device assumption.[108] The final expression for the ground noise is:

$$V_n = (V_{in} - V_T) + \frac{T}{nkL}\left[1 - \sqrt{1 + 2(V_{in} - V_T)\frac{nkL}{T}}\right] \qquad (4.2)$$

A similar derivation can be performed with n = 1:

$$I_{Dmax} = n\frac{k}{2}(V_{GS} - V_T)(1 + \lambda V_{DS}) = n\frac{k'}{2}(V_{GS} - V_T) \qquad (4.3)$$

where $k' = k(1 + \lambda V_{DD})$ and

n is the number of simultaneously switching outputs.

For short channel length devices, the channel length modulation term λ should not be omitted.

$$V_{GS} = \left(V_{in} - V_n \right)$$

V_n = ground noise voltage

For an inductor,

$$V_n = L \frac{di}{dt}$$ L = effective ground path inductance to the output

drivers.

For this rough estimate of ground noise, assume a ramp ground current waveform,

$$V_n = L \frac{I_{Dmax}}{t_f}$$

where t_f = the time it takes for the current to decrease from $0.9 I_{max}$ to $0.1 I_{max}$.

Combining the above expressions, we have

$$V_n = \frac{n}{n + \dfrac{2t_f}{k'L}} \left(V_{in} - V_T \right) \tag{4.4}$$

This expression does not account for the previous derating effects mentioned

earlier, namely non-SSO and skewed switching. Adding in an overall reduction

coefficient yields:

$$V_n = C_{red} \frac{1}{1 + \dfrac{2t_f}{nk'L}} \left(V_{in} - V_T \right) \tag{4.5}$$

As expected, the noise is nonlinearly related to the inductance, and the number of

simultaneously switching outputs. The effects of changing n and L are identical, as

demonstrated in section 4.4.7.

Designers are interested in determining how many I/Os can switch

simultaneously, or how many ground and power pins are needed for a certain application.

This is very difficult to resolve, since the number of SSOs and package pins necessary are

functions of the package, output drivers, and maximum allowable switching noise.

Rearranging Equation 4.5 results in a useful expression for the product of inductance and

number of simultaneous switching outputs.

$$Ln = \frac{2t_f}{k'} \frac{V_n}{C_{red}(V_{in} - V_T) - V_n}$$ (4.6)

The Ln product determines the switching noise for a given output driver. Equation 4.6

can be used to trade of driver size, inductance per package pin, package power and

ground allotments, and simultaneous switching requirements for a desired maximum

noise voltage.

It is interesting to compare results from Equation 4.5 to actual maximum noise

simulations. For a given temperature, $\frac{2t_f}{k'L} = C_1$, a constant. Let us first estimate C_{red},

then calculate a C_1 value for a specific case, namely VDD = 5.5; -55°C; and best

processing, to see if the maximum noise values can be effectively approximated by a

function of this type. The non-SSO portion of C_{red} is difficult to condense down to a

single number over the range of SSOs, since this effect changes with the number of non-

SSOs, but 0.85 (a 15% reduction) is a reasonable compromise. Skew, which is included

in the simulation model used here (1/3 ns), should cause approximately a 25% reduction

based on section 4.4.10. Thus, $C_{red} = (0.85)\ (0.75) = 0.64$.

Based on simulations, the output fall time, t_f, is approximately 0.8 ns, and the

series inductance is 0.15 nH for this package, leaving only k to find. A zero order

estimate of k is

$$k = \mu_n C_{ox} \frac{w}{l}$$

where $\qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

For this process and design, $\mu_n = 575\ cm^2/vs$; $t_{ox} = 1.4\ E\text{-}8\ m$; $w = 530$ microns, 1

$= 0.98$ microns,[109] giving k = 0.23. Therefore,

$$C_l = \frac{2t_f}{k'L} = 46.38$$

Figure 4.54, which plots Equation 4.5 and the simulation results, shows that this

leads to a gross overestimate of the ground noise, in error by as much as 100% in some

instances. This attempt used a very crude approximation of the NMOS k, without any

parasitic effects. Now, we will find a more accurate k by including channel length

modulation, and, calculating the effective channel length and effective mobility. Two

parameters we use are the mobility degradation factor theta, and l_d, the lateral diffusion

of the source and drain into the channel.[110]

$$l_{eff} = l - 2l_d$$

$$\mu_{eff} = \frac{\mu_0}{1 + Theta(Vgs - Vth)}$$

. For this process, l_d = .125 microns, theta = 0.466 1/v, V_{th} = 0.623, and λ = 0.173 1/v.[111]

The calculation for λ was fairly lengthy, involving numerous analytic formulas,[112] and SPICE parameters from reference 109, and is not included here for brevity. Now,

$$k = \mu_{eff} C_{ox} \frac{w}{l_{eff}}(1 + \lambda Vds) = 0.111, \quad and$$

$$C_1 = \frac{2t_r}{k'L} = 96.1$$

Figure 4.55 shows this to be an excellent match with simulations, except for very high numbers of simultaneously switching outputs. In this approximation, a constant 0.85 non-SSO degradation factor was used, but this effect diminishes considerably as the number of SSOs increases, resulting in the poorer match at high SSO counts.
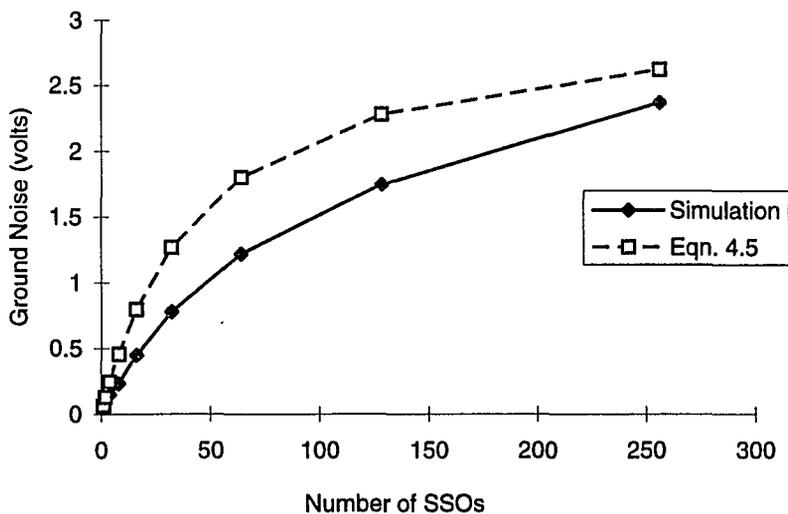
Figure 4.54 - Ground Noise Simulation/Equation 4.5 Comparison, Simple NMOS k Approximation, -55°C, Best Processing
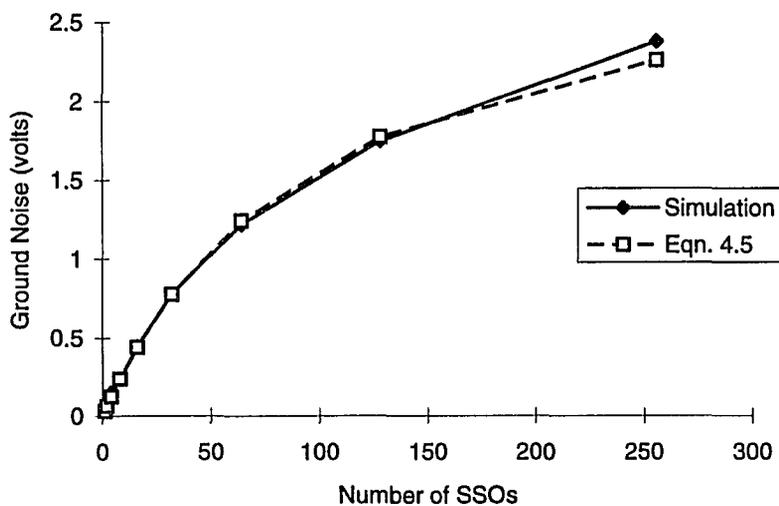
Figure 4.55 - Ground Noise Simulation/Equation 4.5 Comparison, Better NMOS k Approximation, -5C, Best Processing

This analysis was extended to five other operating points: 25°C, best Processing (Figure 4.56); -55 and 25°C, typical processing (Figure 4.57 and Figure 4.58); -55 and 25°C, worst processing (Figure 4.59 and Figure 4.60). The Saber simulation results in Table 4.4 were used for fall time estimates. Only ground noise was considered here, however this could easily be extended to include VDD noise by using PMOS transistor characteristics.

The match for all cases is reasonably good. The error was always less than 20%, usually well under, which is very impressive considering the complexity of the circuit, and the simplicity of the analytic estimate. This demonstrates the validity of the original assumption of non-square-law short channel MOSFETs, but it also illustrates the danger in using an analytic formula for more than a rough estimate. In this case, and likely for others as well, there was some trial and error necessary in determining the level of detail necessary for the parameters in Equation 4.5. For a new situation, it would be unwise to use a first estimate as anything more than a crude estimate, until more detailed simulations were performed as validation and refinement. In particular, the output rise and fall times, and reduction factor, C_{red}, would be difficult to estimate without knowing and simulating the actual drivers in use. This will certainly be the case if new drivers are being designed with the goal of lowering switching noise. Nonetheless, a formula such as Equation 4.5 can be very useful for assessing hypothetical situations and alternatives.

VDD=5.5 SSO = 64	Best T = -55	Best T = 25	Typical T = -55	Typical T = 25	Worst T = -55	Worst T = 25
Rise Time (ns)	1.14	1.61	1.33	1.9	1.5	2.01
Fall Time (ns)	0.8	1.25	1.08	1.56	1.18	1.71

Table 4.4 - Saber Simulated Driver Rise and Fall Times
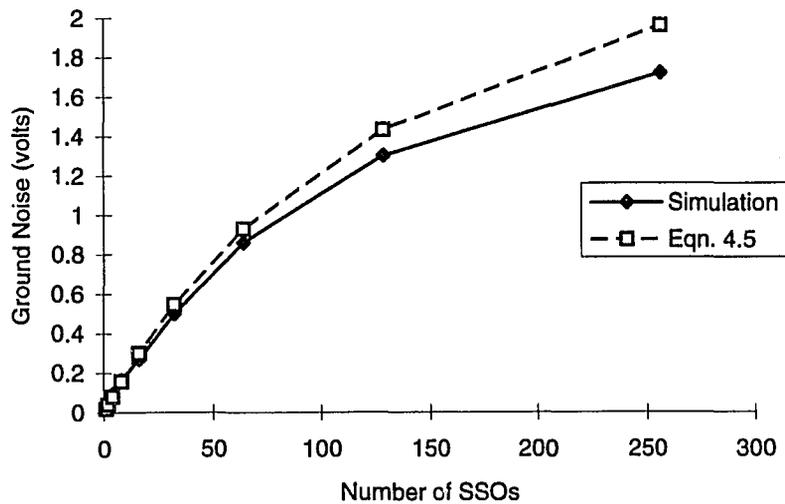
Figure 4.56 - Simulation/Equation 4.5 Comparison, 25°C, Best Processing
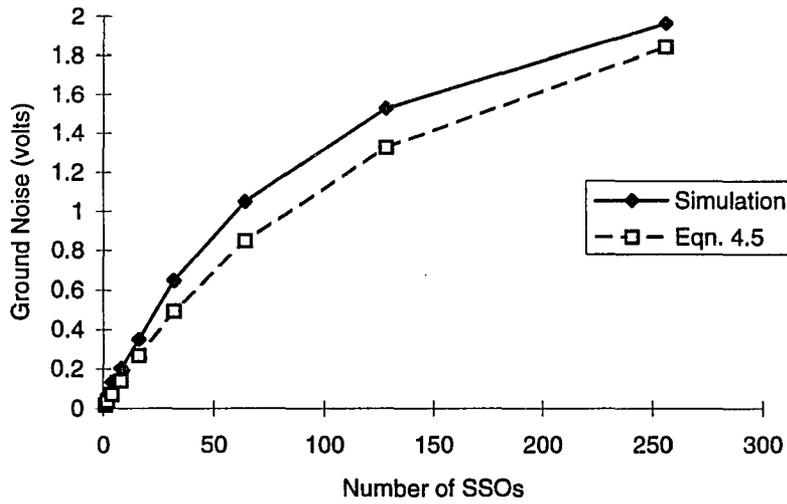
Figure 4.57 - Simulation/Equation 4.5 Comparison, -55°C, Typical Processing
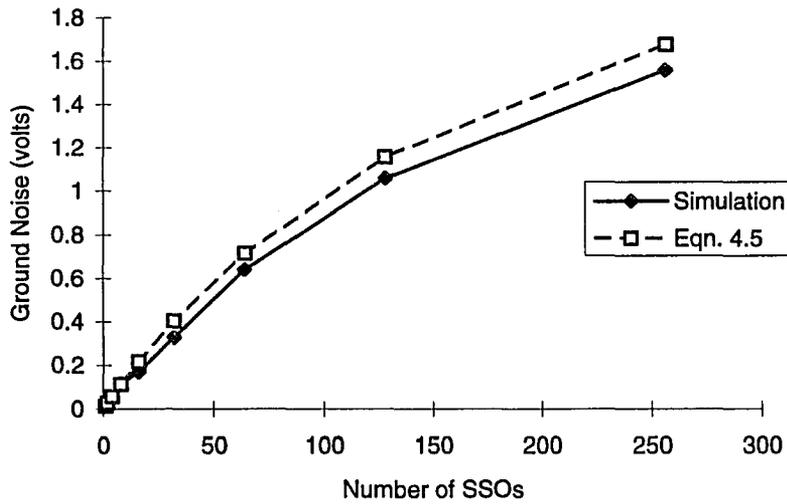
Figure 4.58 - Simulation/Equation 4.5 Comparison, 25°C, Typical Processing
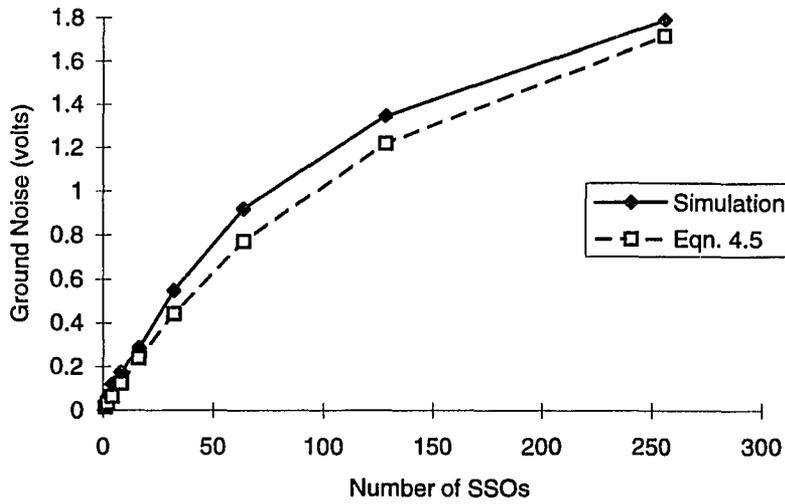
Figure 4.59 - Simulation/Equation 4.5 Comparison, -55°C, Worst Processing
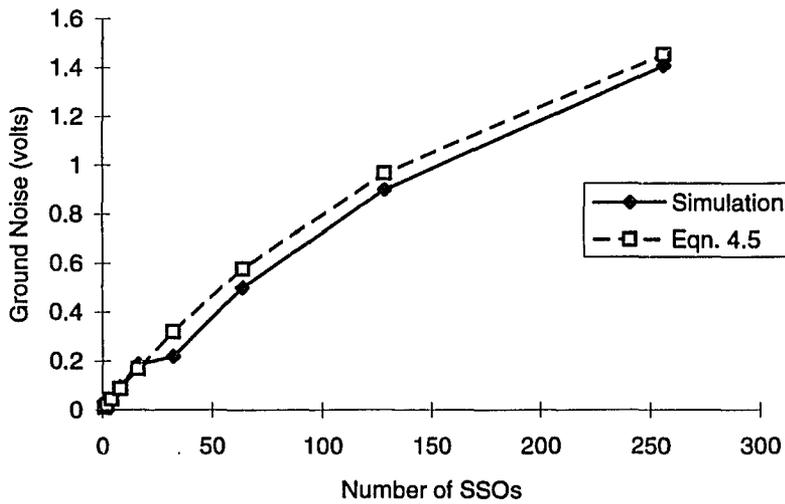
Figure 4.60 - Simulation/Equation 4.5 Comparison, 25°C, Worst Processing

4.6 Noise Coupling

Can noise be coupled from one section of the IC to another? This is possible through the substrate, or via the package ground and power planes. Figure 4.61 shows a simplistic model of the ground switching noise, V_{NOISE}, coupling through the p-type substrate in an n-well process to an adjacent or nearby quiet driver ($V_{COUPLED}$). At a given frequency, this is a simple divider circuit:

$$\frac{V_{COUPLED}}{V_{NOISE}} = \frac{R_{QUIET} + 2\pi fL}{R_{COUPLED} + R_{QUIET} + 2\pi fL} \qquad \text{Equation 4.7}$$

Consider an example circuit, with L = 0.535 nH, R_{QUIET} = 0.073 Ω, and rise and fall times of approximately 1 ns. Using a common first order approximation, we have

$$\text{Bandwidth}_{HERTZ} = \frac{0.35}{t_r} = 350 \text{ MHz}$$
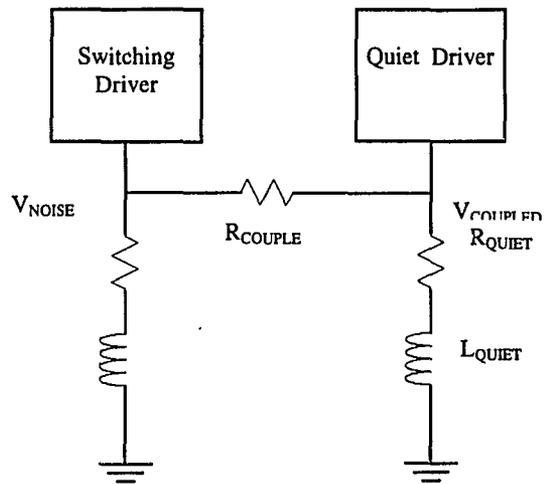
Figure 4.61 - Substrate Noise Coupling Model for Adjacent Drivers

Now, from Equation 4.8, we can find the coupling for a given R_{COUPLE}, or

calculate an R_{COUPLE} for a desired coupling ratio. Table 4.5 details selected coupling

values and R_{COUPLE} for this example.

Coupling (%)	R_{COUPLE} (Ω)
1	124
5	24
10	11.3
20	5

$$\frac{V_{COUPLED}}{V_{NOISE}} = \frac{R_{QUIET} + 2\pi fL}{R_{COUPLED} + R_{QUIET} + 2\pi fL} = \frac{1.25}{1.25 + R_{COUPLE}}$$

Table 4.5 - Coupling Percentage vs. Coupling Resistance

Reasonable estimates for R_{COUPLE} can be found by looking at a cross section of a typical p-substrate die (Figure 4.62). The resistivity of the epitaxial layer is 3 orders of magnitude larger than the substrate, so the coupling path of lowest resistance will be straight down through the epi layer, across the substrate and up through the epi layer to the next device. Given the thickness of this layer, we have:

$$R = \frac{0.03}{A} \text{ ohms} \qquad \text{where A is the cross sectional area (cm}^2\text{).}$$

From Table 4.5, an R_{COUPLE} of 124 ohms corresponds to only 1% noise coupling. Since we must go through the epi layer twice, and include any contact resistance, which is approximately 10 Ω in this case,[113] R_{epi} is greater than 50 Ω and coupling can be effectively ignored. An R_{epi} equal to 50 Ω implies effective epi active area 600μ x 600μ, which is an extremely large effective area. The conclusion is that noise coupling to adjacent devices through the substrate is a secondary effect at best, especially considering that the resistance of the long p^+ substrate has not even been included.
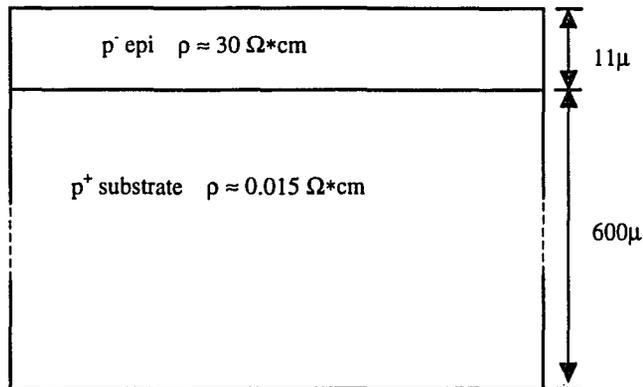
Figure 4.62 - Substrate Cross Section

What about substrate coupling of the I/O driver (dirty) power and ground ring itself to internal (clean) power and ground network? It is common to have on-chip rings for these various powers and grounds, which are then connected to the various devices. In an n-well process, the p-type substrate is connected to one of the IC grounds, usually the clean ground. These different ground rings therefore have a parasitic connection path through the substrate. The coupling path is from the ground metalization on top of the substrate, through the epi layer (and possibly a p^+ epi contact), across the substrate, and back through the epi layer to the other ground metalization.

Another obvious coupling path is through the package planes. Figure 3.3 shows a typical IC package with power distribution planes. The different IC grounds are common

from the board to the package ground plane, after which they are separated. Part of the generated ground switching noise will be caused by the board to package ground plane inductance (L_{G1}), and therefore be present at the plane. This noise is directly coupled into the clean ground, and to any other clock driver grounds on the IC.

A specific simulation example will best illustrate the relative importance of these coupling mechanisms. The design details are based on a new custom Delco Electronics ASIC. The package of Figure 3.7 was designed for this application. An n-well process such as that shown in Figure 4.62 was chosen. The conducting path cross sectional areas for clean and dirty ground were found using layout extraction tools:[114]

Total Clean/Core ground conduction path area:

341,070 square microns

Total Dirty ground conduction path area:

475,900 square microns

Total internal clock driver ground path area:

18,865 square microns

Using the epi layer depth of 11 microns, and the resistivity of 30 ohm*centimeters, we have:

Clean ground to Substrate resistance = 12 ohms

Dirty ground to substrate resistance = 8 ohms

Clock ground to substrate resistance = 212 ohms

The resistance of the substrate itself will be very small in comparison. Figure 4.63 shows the distance from the dirty ring ground to a worst case clean ground connection at the center of the 320 mils square die. The average distance from each of the four ring sides is approximately 180 mils, and the average cross sectional area of the triangular conduction path shown is 150 mils. Accounting for all four ring sides, the total substrate conduction path resistance is 0.07 ohms.

Ring Width = 10 mils

Dirty Ground Ring

Worst Case Clean
Ground
Connection

substrate ρ = 0.015 Ω*cm.

320 mils
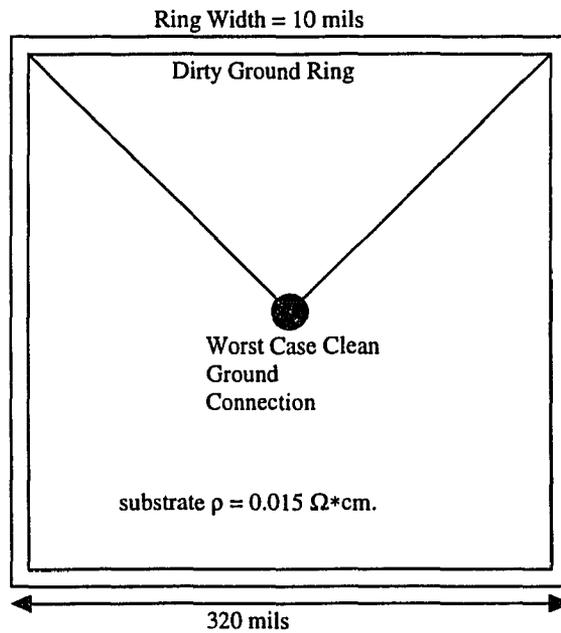
Figure 4.63 - Example of Die Substrate Connection Path from Dirty to Clean Ground

This particular IC has a 16 bit data bus, a 16 bit address bus, and five additional asynchronous enables which can switch simultaneously, for a total of 37. The package model of Figure 3.7 was used, with the addition of the calculated dirty and clean ground resistances connected in series between dirty and clean ground. Substrate coupling to the grounds of the ASIC's two internal clock drivers is not considered here, because of their significantly higher resistance values of 212 ohms. Substrate path resistance was not included, because of the small value calculated above. Contacts will also add a bit more resistance, but are not considered here.

Figure 4.64 shows the percent coupling from the I/O driver ground (dirty ground) to the internal IC clean ground, vs. the total substrate coupling resistance. The total coupling resistance is defined as the resistance from dirty ground to the substrate plus the clean ground to substrate resistance. The substrate coupling has minimal effect for $R_{COUPLE} > 7$, where the coupling is approximately 50%. This clean ground noise in this region is therefore mainly caused by package plane noise coupling, as discussed above. For this particular package, we have a total coupling resistance, $R_{COUPLE} = 12 + 8 = 20$ ohms, which means the substrate will have little effect on the noise coupling into clean ground. A similar analysis and simulation should be done for different design case, since the results will depend on the specific I/O drivers, package, and semiconductor process. Note however that the numbers used here are taken from an actual design case, and should be representative of most typical relatively high speed CMOS designs. The coupling caused by package planes could be quite different depending on the number and

arrangement of planes in a specific package, but substrate coupling is unlikely to be radically different. A package with higher series inductance and resistance in the ground lines would yield more substrate coupling. Such a package would be unsatisfactory for high speed CMOS designs from a switching noise standpoint, so it should not be chosen in the first place.
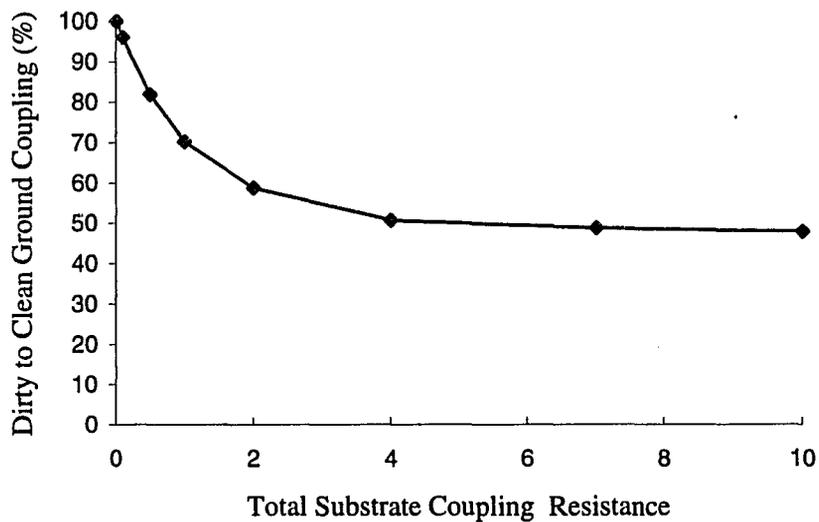
Figure 4.64 - Dirty to Clean Ground Switching Noise Coupling vs. Total Substrate Coupling Resistance

4.7 Internal Clock Driver Noise

Internal clock drivers are needed to drive the numerous on-chip and synchronous elements. There may be more than one clock regime, and therefore more than one clock driver necessary on a single integrated circuit. These drivers may need to be extremely large to handle their loads under worst case conditions. They can cause large switching noise spikes, depending on their ground and power interconnections. It is common to have separate power and ground pads for each clock driver for isolation, either from the board or from a common package plane. The parasitic inductance of a single die connection can be fairly large.

4.8 Combining Switching Noise From Different Sources

The switching order of clock drivers, internal synchronous registers, and simultaneously switching outputs is key when considering how to predict their combined switching noise. An internal clock driver will be the first to switch, followed by the internal registers and the output drivers, which are both driven by the clock. An output driver circuit will normally have several levels of logic and predrivers before the final output MOSFETs. For first order approximations, it seems safe to assume that the main noise spikes from a clock driver will have died out by the time the large output devices turn on. Internal logic switching will normally occur before the I/O drivers. When considering internal register simultaneous switching, an estimate of approximately 20% switching in one direction at one time is reasonable. Skew between different registers will also be present, but the magnitude will be difficult to determine before actual layout.

Because of the oscillatory nature of most ground and VDD bounce, it is extremely difficult to predict exactly how they will combine. The simplest approach is to simulate I/O, clock, and internal logic separately, and use conservative worst case goals to account for some coupling from the other switching noise sources. It is important to realize that devices, drivers etc. in different clocking regimes must be assumed to be simultaneously switching for worst case noise estimates, since they can switch at any time relative to each other. This adds to the complication of combining noise from different sources. Output drivers should be the highest priority, of course.

4.9 Hints To Lower Simultaneous Switching Noise

What can be done to minimize ground and power bounce caused by simultaneous switching outputs? From the previous results, several things stand out. Unfortunately, most steps taken to minimize this noise are not extremely effective. For example, lowering inductance is an obvious tactic. But we have already shown that there is a less than a linear relationship between inductance and SSO noise. This is true with virtually every noise reduction method. Basically, there is no way to easily reduce SSO noise. The tradeoff in performance, cost and complexity is usually expensive.

Most of the inductance comes from the IC package itself. Power and ground planes are a necessity, as are low inductance pins and bonding techniques. TAB connections are lower inductance than bonding wires, but not by a wide margin. Increasing the number of power and ground pins and pads effectively lowers inductance. This is the most common method for reducing inductance, and is the only thing available to the designer if a particular package type is mandated. Once again, this is expensive, because these power distribution pins are no longer available for signals, thus forcing a bigger package for a given number of signal I/O.

IC package design is extremely important. PGA packages and flip chips are attractive, because they reduce the length of connection paths Double bonding is not a very effective technique, since the adjacent bond wires are highly coupled. Package

power and ground planes with short paths to pins and bonding pads are essential to reduce inductance.

The next obvious step is to reduce the number of SSOs as much as possible. This lowers the overall ground and/or VDD current, and also increases the number of non-SSOs. In the event that this is not possible, introducing some switching skew has been shown to significantly reduce switching noise with a relatively small operating speed penalty.

The strengths of the drivers necessary for a particular application are very important. By increasing the necessary delay, rise and fall times as much as possible, the di/dt will be minimized. Choosing a semiconductor process with minimum difference between best and worst cases will help reduce the driver sizes, and therefore the maximum currents during best case conditions.

Lastly, power supply capacitance has been shown to be of limited help. Care must be taken not to reduce noise in one location, at the expense of increasing noise in another. Multi-chip and hybrid modules show the most promise for improvements using power distribution network capacitance. The following chapter will discuss driver effects in detail, including some ideas to dramatically reduce switching noise with careful driver design.

4.10 Methodology Summary

Switching noise modeling and simulation is an evolutionary process. Initially,

first estimates of system simultaneous switching requirements, and preliminary predriver,

driver and package designs are needed. Accurate package inductance estimates, obtained

by a combination of field solvers and measurements, are essential. The package model

can be simplified to its series inductance and resistance components, and any package

ground plane to VDD plane capacitance. Detailed transistor level predriver, driver and

MOSFET device models must be used to accurately estimate switching noise.

Initial simulations varying process, temperature and voltage provide information

on the magnitude of delay and noise variation over the operating range. This operating

point data is useful in later noise predictions. Next, simulations varying the numbers of

non-switching I/Os and output switching skew will assess their switching noise reduction

effects.

Enough information will now have been gathered to utilize the analytic switching

noise expressions developed in section 4.5. The designer can trade off parameters such as

package inductance, the number of simultaneous switching outputs, and skew noise

reduction to reach a desired maximum switching noise level. As the design changes, it is

only necessary to perform a single noise simulation at one operating point. It was shown

that noise levels at other operating points can be accurately predicted using the previously

determined operating range data.

Damping resistor effects require realistic worst case capacitive load estimates to accurately trade switching noise reductions against delay increases. The simulations can be refined when information such as parasitic IC damping resistance, better package inductance estimates, and bypassing capacitor details become available as the design progresses. If the output driver design changes drastically, the modeling and simulation methodology should be started again, since the previously obtained data and trends may be incorrect.

5. LOW NOISE DRIVER DESIGN

5.1 Basic CMOS Output Drivers

Figure 5.1 depicts a simple, two-stage CMOS output driver. Basically, the output stage must charge up the output capacitance. When the output stage is switching from one state to another, there is a through current and a charge or discharge current. The initial rise (and maximum di/dt) of the total switching current is mainly controlled by the through current, which is primarily independent of load capacitance.[115] Since the switching noise is directly proportional to di/dt, this explains the weak dependence of switching noise on output loading capacitance discussed in Chapter 4.
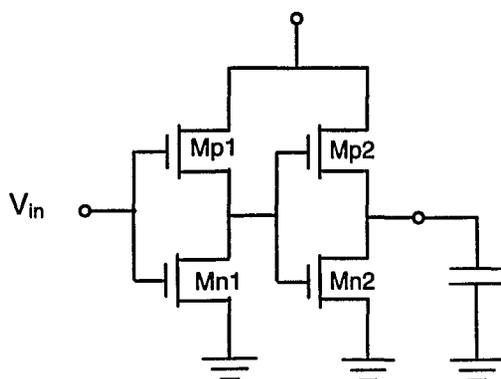
Example Device Sizing:

Predriver
Mn1 = 0.8μ x 108μ
Mp1 = 0.8μ x 216μ

Output Stage
Mn2 = 0.98μ x 530μ
Mp2 = 0.98μ x 987μ

Figure 5.1 - Simple CMOS Output Driver

The rise times of output drivers decrease with decreasing device geometries. Thus, reducing the device minimum feature size will cause an increase in switching noise for a given number of simultaneous switching outputs. A large problem to overcome is the need to over design CMOS output drivers to work under worst case conditions. A driver must meet delay specifications when VDD is low (10% usually), temperature is a maximum (up to 135 C), and under worst case processing. Each of these effects alone can reduce the output current capability by as much as 50%. In order to meet minimum drive capability requirements when all three parameters are worst case, a driver will have significantly more current capability than is necessary under best case conditions. The simultaneous switching criteria must be met under these best case conditions, which can be difficult.

5.1.1 I/O Cell Delay

Delay in CMOS circuits is defined as the time from the input crossing VDD/2, to the output crossing VDD/2, for either inverting or noninverting output drivers. For simplicity and clarity of all delay simulations, switching noise was not taken into account (i.e. no package model is included). Actual switching noise will directly depend on the specific package used. Once a package is chosen, noise and delays should be modeled and simulated to investigate more exact cumulative effects.

Output driver delays are affected by a number of parameters. Load capacitance is one of the first that comes to mind. The output delay is a sum of the driver switching delay, and the time to charge the load capacitance. That is:

$$t_d = t_{switch} + kC_{load} \quad \text{where } k = (VDD/2)/I_{driver}$$

which is a straight line with slope k as C_{load} is varied.

The effects of temperature, processing and VDD on switching noise were discussed in Chapter 4. From the above expression, it can be seen that both terms of t_d are affected as process, temperature and VDD are varied. What happens to the delay as these parameters are varied? The circuit of Figure 5.1 was simulated as temperature, VDD and process were varied. The processing parameters represent National Semiconductor's 0.8 micron process.

Table 5.1 summarizes the variation in delay for one parameter over the limits of the remaining two. High-to-low and low-to-high delays were both considered in this summary. It can be seen that temperature is the dominant parameter when considering delay. Note that the variation is defined as:

Percent variation = (max-min/max) x 100

Parameter	Parameter Limits	Delay Variation (%)
Temperature	135 > T > -55	$43 < \Delta t_d < 51$
Voltage (VDD)	4.5 < VDD < 5.5	$9 < \Delta t_d < 16$
Processing	Worst - Typical - Best	$15 < \Delta t_d < 26$

Table 5.1 - Single Parameter Variation Effects on Delay

5.1.2 Switching Noise

Table 5.2 summarizes a similar analysis of VDD and Ground switching noise for this simple driver as T, VDD, and process are varied. The package model of Figure 5.2 replaced the ideal VDD and ground connections of the previous simulations. Once again, temperature is the most dominant parameter. Note however, that the noise voltage variation is much larger over the chosen parameter space than the delay variation, by more than a factor of 3. This is also a larger variation than that shown in Chapter 4, but those were very complex low noise drivers, while here we have very simple 4 transistor drivers.

Parameter	Parameter Limits	VDD Noise Variation (%)	Ground Noise Variation (%)
Temperature (°C)	$135 > T > -55$	$75 < V_{noise} < 82$	$74 < V_{noise} < 78$
Voltage (VDD)	$4.5 < VDD < 5.5$	$26 < V_{noise} < 37$	$21 < V_{noise} < 38$
Processing	Worst-Typical-Best	$9 < V_{noise} < 29$	$17 < V_{noise} < 35$

Table 5.2 - Single Parameter Effects on Switching Noise
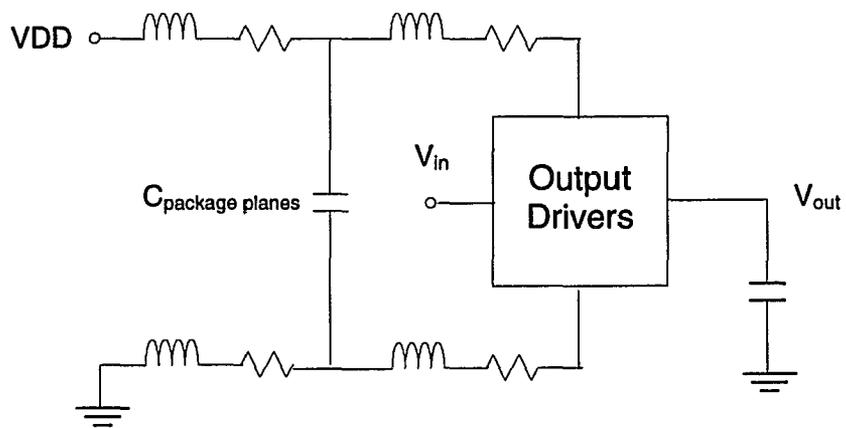
Figure 5.2 - Power and Ground Connection Package Model

5.1.3 Predriver and Driver Sizing

5.1.3.1 Delay effects

Driver size is another obvious factor affecting output delays and switching. As size is increased, one would expect delay to decrease at the expense of higher switching noise. High to low delay vs. driver size is plotted as the solid curve in Figure 5.3, with constant predriver size. This shows delay increasing as driver size is reduced, but also increasing again as driver size is raised from nominal. This increased delay as driver size is increased is caused by the added load the predriver must drive. The delay increased as drivers are decreased is not as pronounced as one might expect, because although the output drive strength is lessened, the load on the predriver is also smaller. As driver size becomes excessive, this dominates the overall delay. This suggests that an optimum driver to predriver size ratio exists for a given technology and driver design. Note that at the left side of the plot, a scale factor of 0.1 means the driver is actually smaller than the predriver, which is unrealistic. Note that in this and all following plotted simulation results, nominal sizes are those stated in Figure 5.1

Predriver strength (i.e. size) can also have a significant effect on both simultaneous switching noise and delay. Delay decreases monotonically with increasing predriver size as driver size is kept constant (Figure 5.3). Not surprisingly, the effect is not nearly as strong as with driver strength. The final curve in Figure 5.3 shows delay as

predriver and driver sizes are changed together. The driver to predriver size ratio is kept

constant at approximately 5 to 1, as in Figure 5.1.

Another way to look at sizing effects on delay is to plot delay vs. total driver plus

predriver sizes, or gate lengths (Figure 5.4). For a given total gate size, the minimum

delay is achieved when the driver and predriver stages are scaled together. This also

suggests that our chosen relative sizing between the stages is close to optimum. Both

plots discussed were for worst case delay conditions, or VDD = 4.5, 135°C and worst

processing. The trends were very similar for all other permutations of these operating

parameters, so they are not shown here.
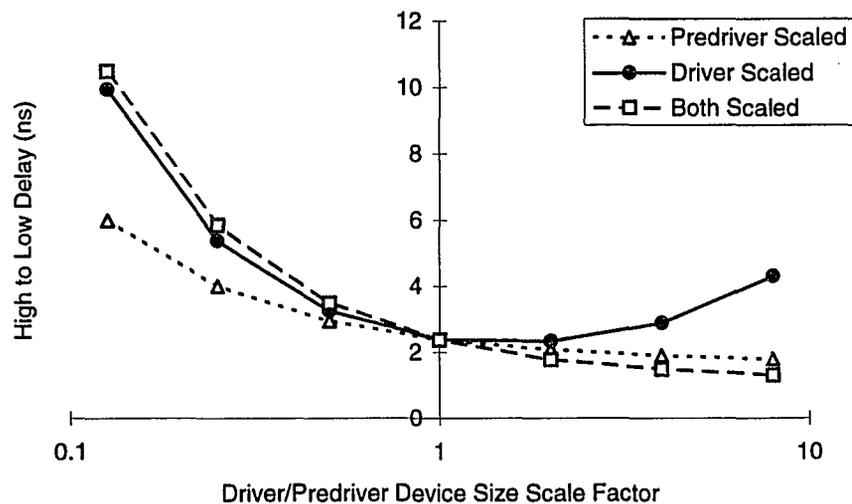
Figure 5.3 - Worst Case High-to-Low Output Delay vs. Driver and Predriver Size
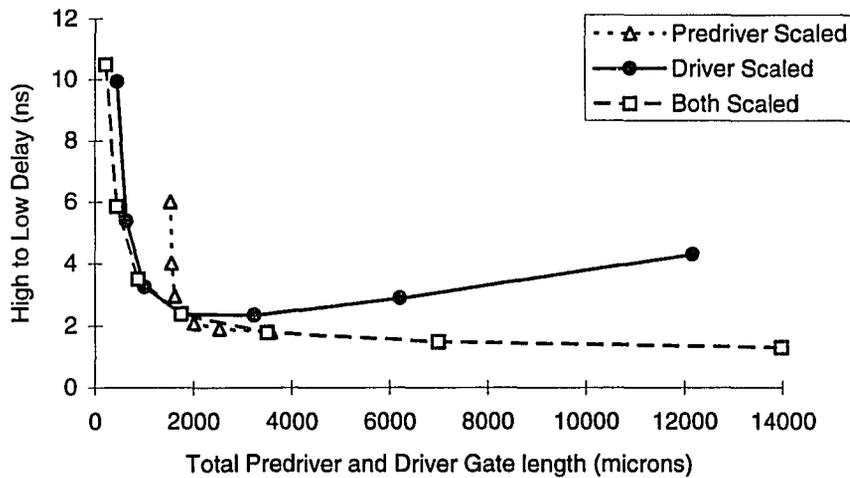
Figure 5.4 - Worst Case H-L Output Delay vs. Total Driver and Predriver Size

5.1.3.2 Switching Noise Effects

We would certainly expect that switching noise would be a strong function of

driver size, similar to that for the number of SSOs. Worst case switching noise (VDD =

5.5, -55°C, best processing) is shown in Figure 5.5. As before, driver and predriver sizes

are scaled separately, and together. Simulation trends and waveshapes are once again

very similar for different operating conditions, so only the most interesting, worst case is

shown here. Predictably, the effect is maximum as the stages are scaled together,

followed by driver only scaling, and finally predriver scaling. It may be a bit surprising

that predrivers have almost as much influence on noise as drivers.

This brings up another concern. The predrivers for high current output drivers are themselves quite large. In the previous chapters, we concentrated on output driver induced noise, that is VDD noise on output L-H transitions, and Ground noise on H-L transitions. Given the inverting nature of typical stages, predrivers switch the opposite direction as the outputs. For example, for a H-L output transition, the NMOS driver di/dt causes ground noise, while the PMOS predriver switches L-H resulting in VDD noise. Since the drivers are normally significantly larger, this has been ignored up to this point. In extreme cases where predrivers are as large as or larger than the drivers themselves, their contribution to switching noise become as important as those from the drivers. It seems unlikely for this to actually occur, since predrivers should always be significantly smaller than drivers, so it is noted here but not pursued further.
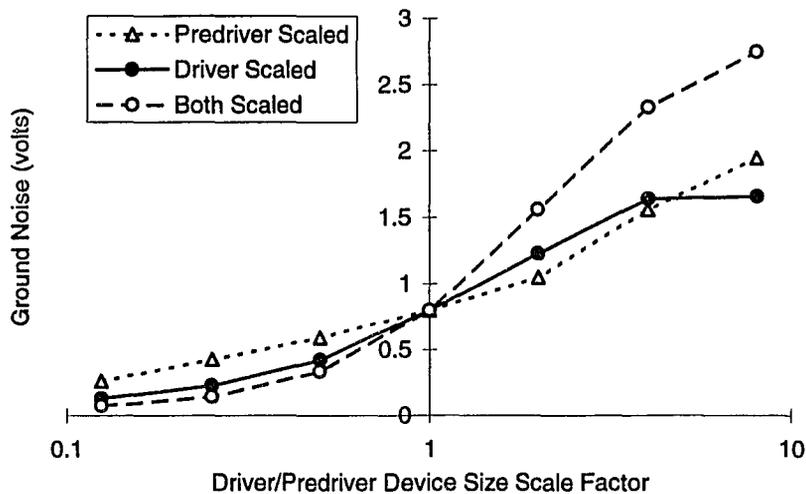
Figure 5.5 - Worst Case Ground Switching Noise vs. Driver and Predriver Size

We desire a driver for which both switching noise and delay are minimized. How these two are weighed will vary with application. Perhaps the most practical way to look at sizing effects is to plot worst case delay vs. worst case switching noise for a given MOSFET sizing. This allows us to weigh delay vs. switching noise for a given design at voltage, temperature and processing extremes (Figure 5.6). The "scorpion tail" should be ignored, since it corresponds to unrealistically large drivers. For a given delay, the lowest ground noise is achieved when the drivers and predrivers are scaled together. As before, this means the chosen nominal size ratio is near optimum. This also suggests an output driver design methodology. The stage scaling ratio need only be optimized for one set of operating conditions. Then, the stages can be scaled together to achieve desired worst case delay and or switching noise targets.
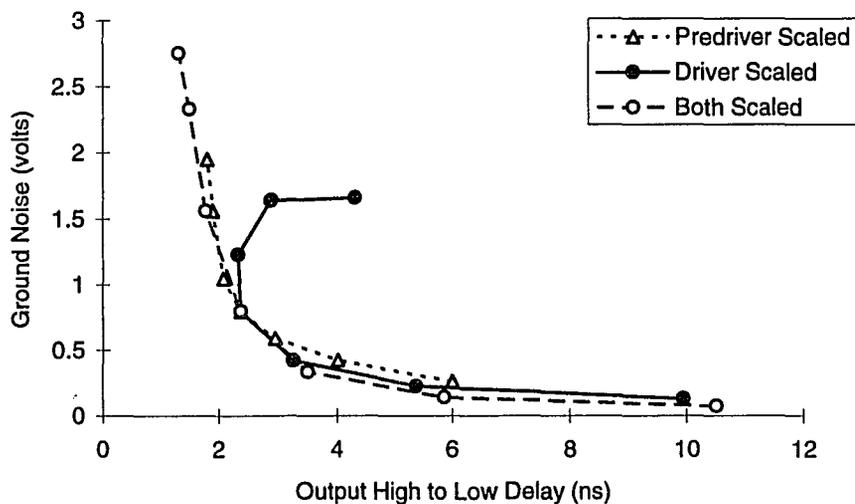
Figure 5.6 - Worst Case Ground Noise vs. Worst Case H-L Delay

5.2 Damping Resistance

It has been shown that the addition of source damping resistance, as in Figure 5.7, can significantly reduce the switching noise by up to 75 percent. [116] [117] For relatively small drivers, the small increases in delay could be easily compensated for with an increase in output driver size of less than 15 percent.[118] The situation is quite different for larger drivers, with maximum saturation currents greater than 100 mA. Best case drive strength requirements in this range are not uncommon for outputs which drive long lines and multiple loads, such as address and data busses.

Typical damping resistances range from 10 to 100 ohms. A driver with a saturation current of 100 mA would result in an IR drop of 10 volts across a 100 ohm damping resistor. This is unrealistic, therefore the damping resistance would simply limit the output stage current. This will lower the switching noise, but the penalty in delay may be large. Additionally, increasing the driver size will have only a minor effect on the delay, since the current is already limited by the damping resistance. Note that there will be some parasitic contact and interconnect damping resistance already present in a typical IC, typically on the order of 5-10 ohms.[119]

The tradeoff of noise and high-to-low delay as damping resistance is varied for a driver with a maximum saturation current of 120 mA is shown in Figure 5.8. The delay penalty for reduced noise is high, particularly if noise reductions greater than 50% are desired. Figure 5.9 plots high to low delay and ground noise for 50 an 100 ohm damping

resistances, as the driver and predriver sizes are scaled. The maximum noise and minimum delay are both limited for a given damping regardless of how large the output stage is, because of switching current limiting. As driver size as reduced, noise reduction is achieved with a heavy penalty in delay, as expected. In summary, the effectiveness of adding damping resistance is greatly reduced for high current output drivers.
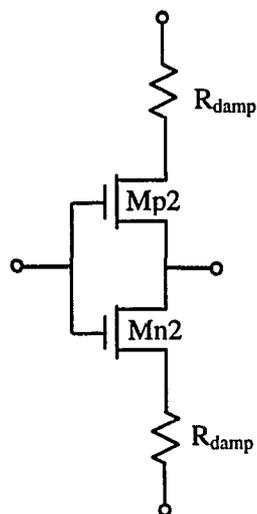
Figure 5.7 - CMOS Output Stage with Source Damping Resistors.
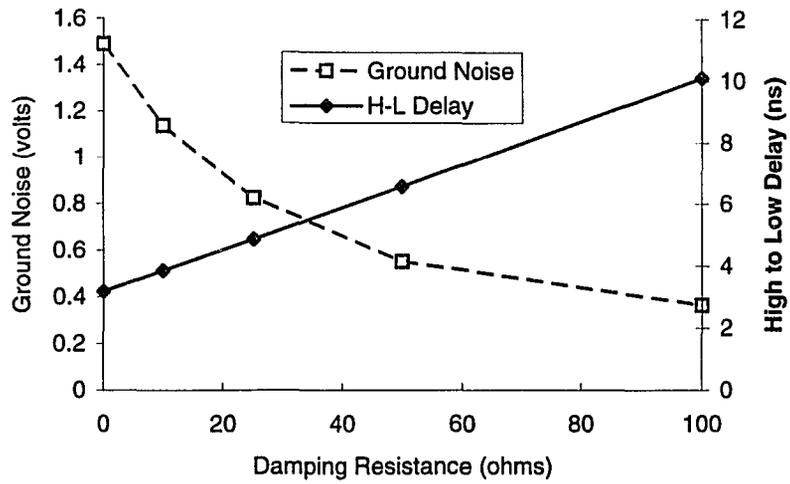
Figure 5.8 - Ground Noise and H-L Delay vs. Source Damping Resistance.
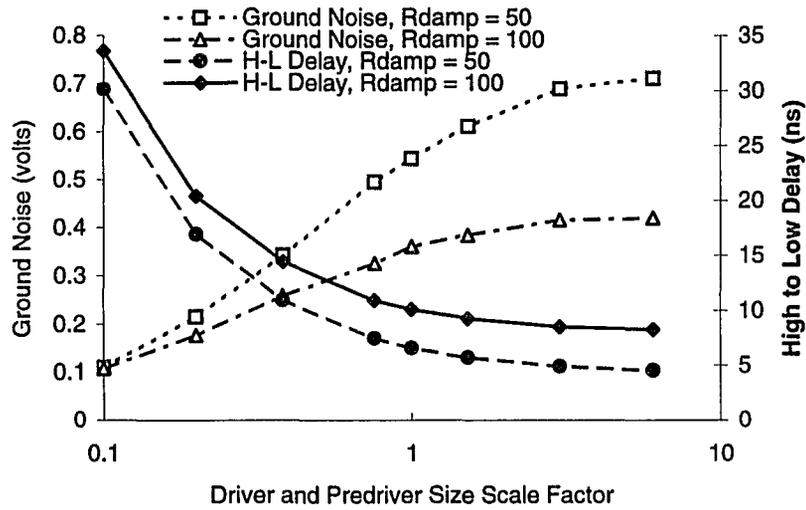
Figure 5.9 - Ground Noise and H-L Delay vs. Predriver and Driver Size Scale Factor for $R_{damp} = 50$ and 100 Ohms.

5.3 Adaptive CMOS Output Driver Design

It is imperative that a driver meet the maximum delay requirements for a given application under worst case conditions. From a switching noise standpoint, it would be ideal if the same driver could also minimize its drive strength when conditions are not worst case. One way to approach this problem is to design a driver which can sense conditions or performance, and then adjust the drive strength accordingly.

A closed ring of 2n-1 inverters (Figure 5.10) will oscillate at a frequency which varies with temperature, processing and voltage.[120] Table 5.3 details the normalized oscillation frequency of the single stage CMOS inverter ring as these parameters are varied. The oscillation frequency is normalized to the frequency at -55°C, VDD = 5.5 volts, and best process. Is ring oscillation frequency a direct indicator of IC performance? Consider an output driver with multiple parallel output stages, each separately enabled (Figure 5.11). If ring oscillator frequency is a reasonable performance indicator, then output driver stage enabling criteria could be based on a measure of this frequency. The higher the frequency, the "better" the IC is performing. Therefore, fewer output stages need to be selected to meet the maximum output delay specification. This minimizes the switching noise by controlling the output drive capability.
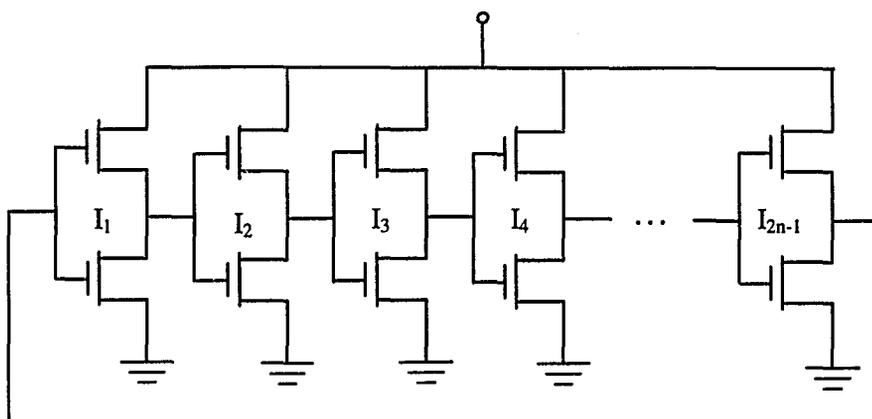
Figure 5.10 - Ring Oscillator

			Ring Freq.
TEMP.	VOLTAGE	PROC.	Normalized
-55	5.5	Best	1
-55	5.5	Typical	0.7770449
-55	5.5	Worst	0.7216359
-55	4.5	Best	0.8891821
-55	4.5	Typical	0.6662269
-55	4.5	Worst	0.5976253
25	5.5	Best	0.6807388
25	5.5	Typical	0.5277045
25	5.5	Worst	0.4854881
25	4.5	Best	0.6108179
25	4.5	Typical	0.4577836
25	4.5	Worst	0.4023747
135	5.5	Best	0.4591029
135	5.5	Typical	0.3469657
135	5.5	Worst	0.323219
135	4.5	Best	0.4023747
135	4.5	Typical	0.3047493
135	4.5	Worst	0.2770449

Table 5.3 - Normalized Ring Oscillation Frequency vs. Temperature, VDD, Processing
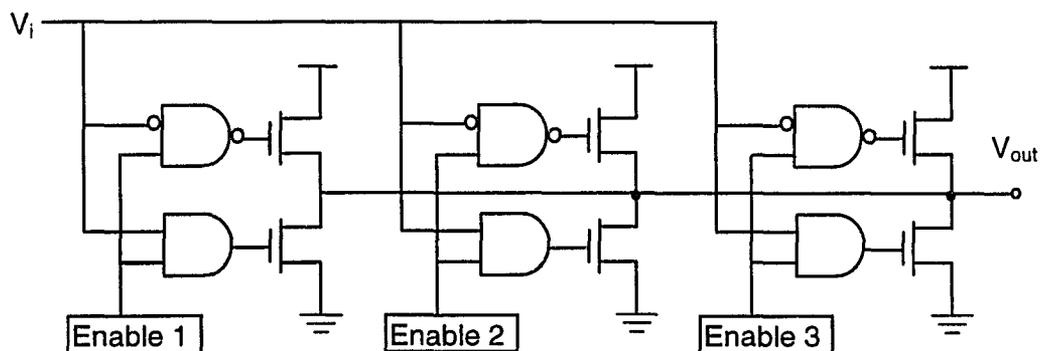
Example Sizing for Each Output Stage:

$Mp = 0.98\mu \times 329\mu$ $Mn = 0.98\mu \times 177\mu$

Figure 5.11 - Three Stage Programmable Strength Driver

The relationships between ring oscillation frequency and both delay and switching noise are of interest here. The circuit of Figure 5.11 with all three stages enabled was simulated while varying T, VDD and process. Figure 5.12 and Figure 5.13 depict output driver delay as process, temperature and VDD are varied. They show that ring oscillation frequency is an excellent, though nonlinear, relative measure of output delays. This is not surprising, since the oscillation frequency is directly dependent on the ring inverter delays.

Ground and VDD switching noise correlation with oscillation is plotted in Figure 5.14 and Figure 5.15. While not nearly as close as the delay case, the correlation is good, with R^2 values between 0.83 and 0.94 for the nonlinear trendlines shown. Therefore, ring

oscillation frequency is a good parameter for estimating relative switching noise performance, and a good measure of overall IC performance.

The magnitude of the CMOS output driver design problem is easily seen by plotting ground switching noise vs. high-to-low delay (Figure 5.16), and VDD noise vs. low-to-high delay (Figure 5.17) over the entire process, temperature and voltage ranges. The strong dependencies of both over the operating space are multiplied together, forming a very non-linear relationship. Both VDD and ground switching noise vs. delay plots can be approximated very well with the same trend line:

$$Noise = \frac{1.1}{Delay^2}$$

This illustrates the high worst case noise penalty paid for a desired reduction in worst case delay.
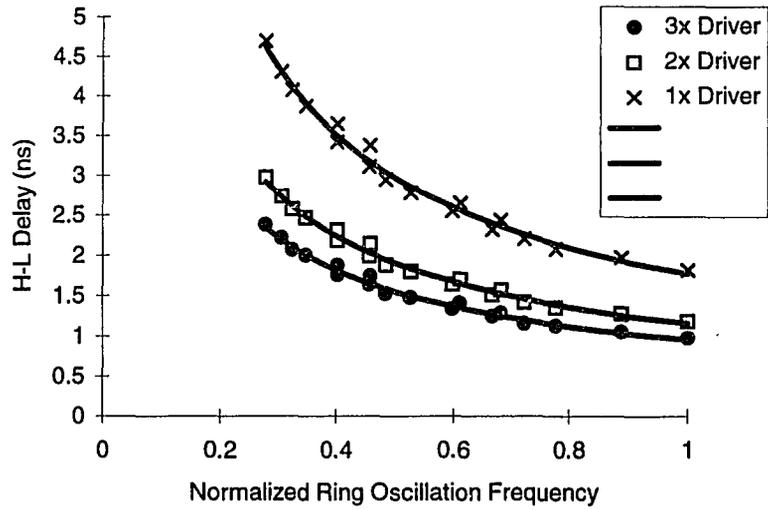
Figure 5.12 - High-to-Low Output Delay vs. Ring Oscillation Frequency
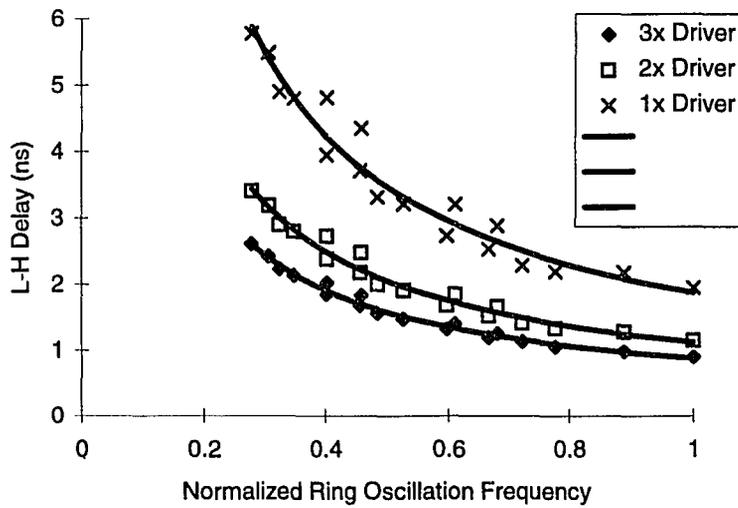
Figure 5.13 - Low-to-High Output Delay vs. Ring Oscillation Frequency
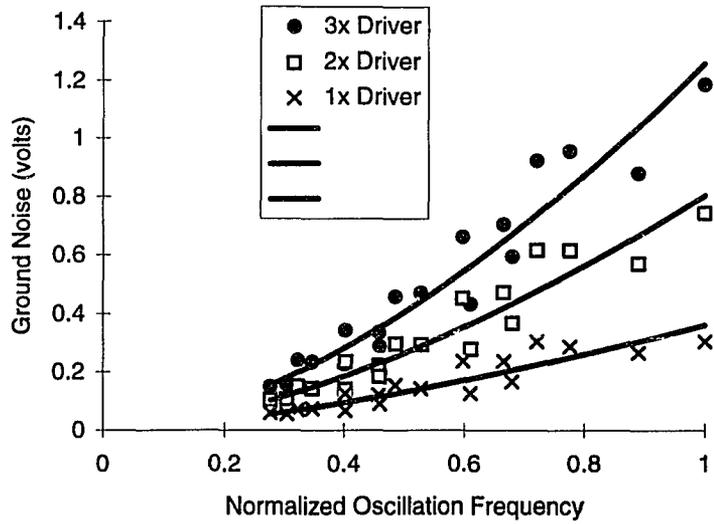
Figure 5.14 - Ground Switching Noise vs. Ring Oscillation Frequency
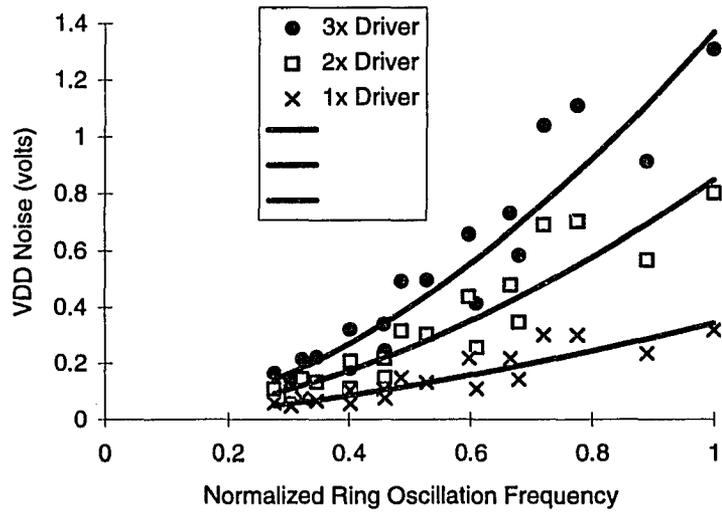
Figure 5.15 - VDD Switching Noise vs. Ring Oscillation Frequency
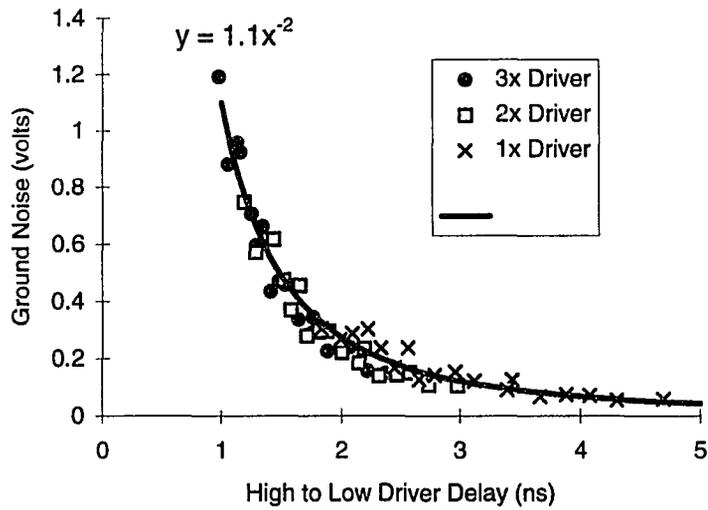
Figure 5.16 - Worst Case Ground Switching Noise Vs. H-L Delay
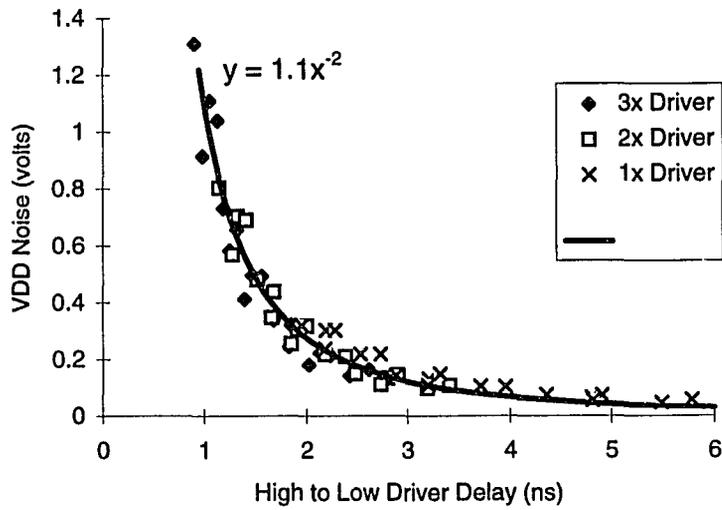
Figure 5.17 - Worst Case VDD Switching Noise Vs. L-H Delay

All three stages of Figure 5.11 were enabled for the previous plots. How much can we gain by intelligently enabling these stages according to ring oscillation frequency? Using the previous results, a driver stage enabling strategy can be deduced. Suppose we wish to have a worst case delay of approximately 3 ns, and thus choose to enable the three stages in the following manner:

$$\text{Normalized } F_{ring} \leq 0.35 \qquad \Rightarrow \quad \text{Stage 1 enabled}$$

$$0.35 < \text{Normalized } F_{ring} < 0.55 \qquad \Rightarrow \quad \text{Stage 1 and 2 enabled}$$

$$0.55 \leq \text{Normalized } F_{ring} \qquad \Rightarrow \quad \text{Stage 1, 2 and 3 enabled}$$

The delay results are shown in Figure 5.18 and Figure 5.19, and switching noise results in Figure 5.20 and Figure 5.21. The superiority of this new design can be seen by comparing the VDD noise vs. low-to-high delay for this new driver (Figure 5.22) against the old case (Figure 5.17). With a maximum delay of 3.2 ns, we have marginally met our delay specification of 3 ns. Our maximum switching noise is now 0.32 volts. The switching noise is banded, and significantly lower under best case conditions than a conventional driver. By merely intelligently switching output stages, the maximum noise is now only 25% of its original value. The price for this was a worst case increase in maximum delay from 2.61ns to 3.2 ns. As impressive as the performance increase was in this example, there is still room for further improvement. In this illustration of the concept of an adaptive driver, there was no attempt to design a complex, low noise output

driver stage. In addition, only three stages were considered here. Increasing the number

and relative sizes of stages should lead to additional improvement.

There is an area of caution which should be noted, concerning the enabling of

stages. It is not desirable for the enabling of stages to occur continually. Hysteresis

would prevent a situation where the oscillation frequency was on a border, and therefore

causing driver stages to be turned on and off rapidly. The enabling logic should also only

be active at predetermined times or intervals to prevent inopportune output stage changes.

Different driver modes could be employed, such as calibration and normal operation.

Output stage enabling changes could only occur during calibration sequences while

drivers are inoperative.
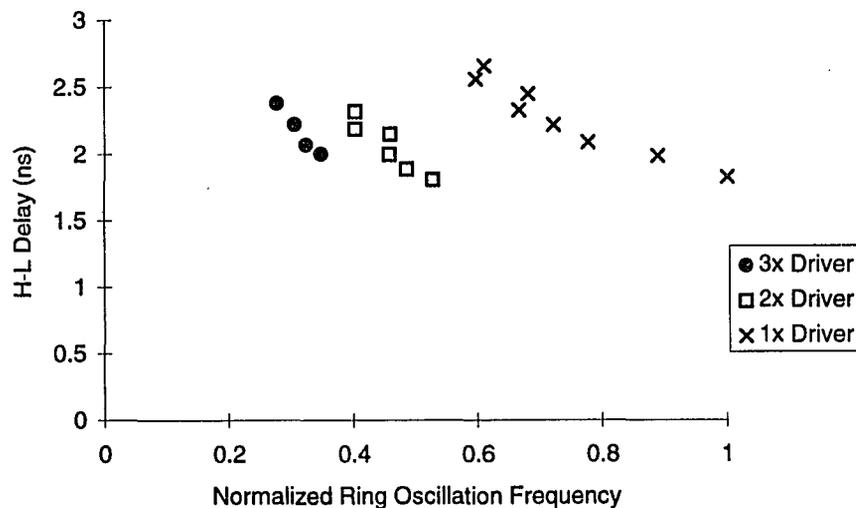
Figure 5.18 - Adaptive Driver H-L Delay vs. Ring Oscillation Frequency
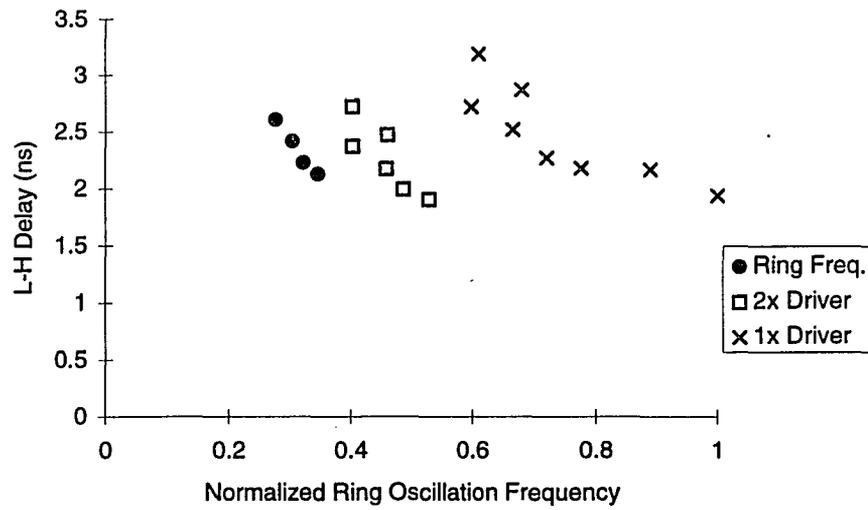
Figure 5.19 - Adaptive Driver L-H Delay vs. Ring Oscillation Frequency
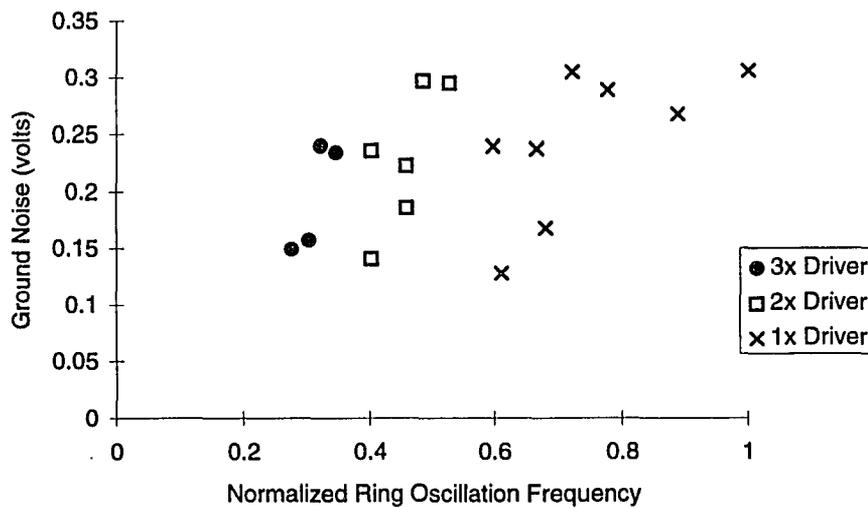
Figure 5.20 - Adaptive Driver Ground Switching Noise vs. Ring Oscillation Frequency
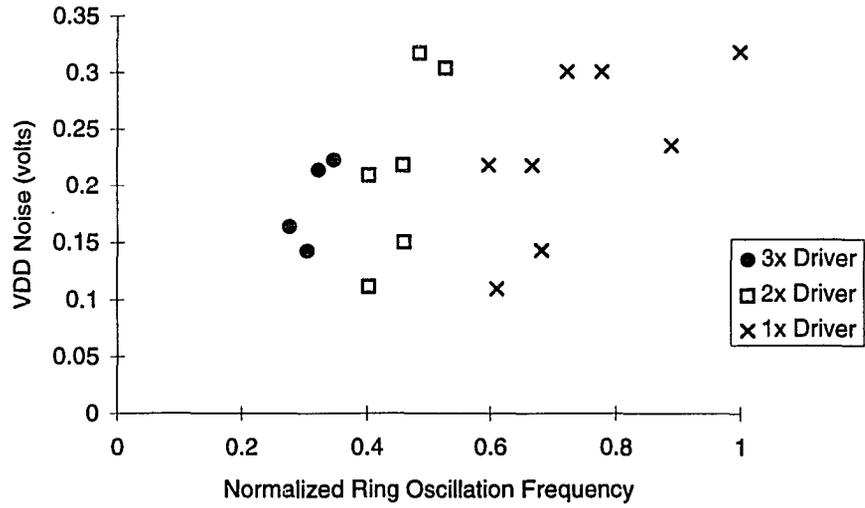
Figure 5.21 - Adaptive Driver VDD Switching Noise vs. Ring Oscillation Frequency
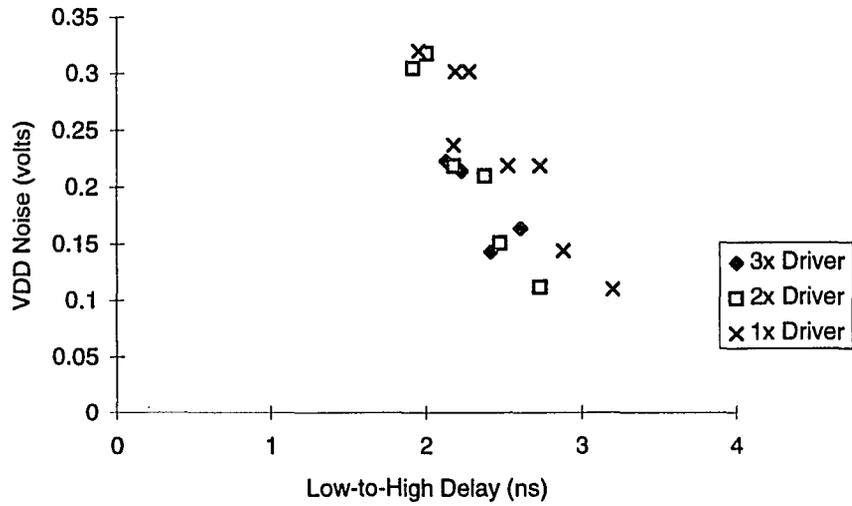
Figure 5.22 - Adaptive Driver Worst Case VDD Noise vs. L-H Delay

Fabrication process tolerances prevent the direct and precise matching of off-chip driver impedances to the impedances of driven transmission lines. An adaptive circuit has been described in the literature, which adjusts the output impedance of a reference driver to that of a reference transmission line and generates a control voltage for adjusting the output impedances of the other drivers on the same chip to the same impedance.[121] [122] A simulated ten-to-one reduction in impedance mismatch has been reported.[123] This suggests an interesting match with the adaptive switching noise drivers described in this dissertation The combination of adaptive output drive control and adaptive impedance matching could form the basis for optimal, intelligent driver designs.

6. SWITCHING NOISE METHODOLOGY DESIGN CASES

6.1 Switching Noise Examples

The simultaneous switching noise modeling and simulation methodology developed in this dissertation has been successfully used in the design of two low switching noise packages, and four different Delco Electronics application specific integrated circuits (ASICs). The ASICs were designed using a silicon compilation methodology, with full custom register blocks, and four different full custom output driver types. The proprietary nature of the ASIC designs precludes more than a cursory look at the switching noise predictions. The two packages are described in more detail in sections 3.6.1 and 3.6.2.

The packages and output drivers were designed, assessed and refined for noise performance based on the methodology presented here. All chip designs were modeled and simulated for noise performance before layout, and before final release for fabrication. The output drivers were divided into four equal switching groups, with a combined inherent and designed skew of 1 ns between groups.

<u>Design A</u>:

172 Pin Ceramic Quad Plat Pack

Maximum SSO count = 37

Simulation Results:

Maximum ground switching noise	0.8 volts
Maximum VDD switching noise	0.63 volts

<u>Design B</u>:

172 Pin Ceramic Quad Plat Pack

Maximum SSO count = 45

Simulation Results:

Maximum ground switching noise	0.50 volts
Maximum VDD switching noise	0.52 volts

<u>Design C</u>:

256 Pin Ceramic Quad Plat Pack

Maximum SSO count = 95

Simulation Results:

Maximum ground switching noise	0.71 volts
Maximum VDD switching noise	0.65 volts

<u>Design D</u>:

256 Pin Ceramic Quad Plat Pack

Maximum SSO count = 110

Simulation Results:

Maximum ground switching noise   0.70 volts

Maximum VDD switching noise   0.72 volts

Each ASIC has a completely different makeup of output driver types and strengths. For this reason, the maximum noise voltages per driver may vary from case to case.

The previous generation of similar Delco Electronics ASICs had experienced a number of switching noise failures. All four ASICs described above easily met the worst case switching noise goal of less than one volt. There have been no reported simultaneous switching noise related failures in worst case testing or in the field.

7. SUMMARY

The main focus of this research has been on CMOS simultaneously switching output (SSO) induced ground and power supply noise. A treatment of interconnect and package modeling led to a simple, generic package model for switching noise purposes. A simplified methodology for modeling and simulating power distribution networks in the presence of numerous SSOs was presented, and validated with two specific circuit examples. A detailed discussion of switching noise followed, particularly focusing on various parameter effects and trends. This led to the derivation and verification of a simple analytic switching noise formula, and a summary of noise reduction techniques.

Output drivers were then investigated, starting with how different parameters affect delay and switching noise performance. The limitations of source damping resistance noise reduction for high current drivers were discussed. An adaptive low noise driver was proposed, with suggestions for further improvements.

Simple printed wiring board properties and general design guidelines were outlined. Finally, several design examples were reviewed. Two specific signal distribution examples were given, demonstrating modeling, simulation and interpretation techniques. The successful application of the switching noise modeling and simulation methodology to the designs of four released ASICs and two low noise packages was summarized.

7.1 Methodology Summary

Integrated systems are becoming so complex, it is extremely difficult for designers

to simulate full systems, particularly early in the design process. What the designer needs

is a methodology to quickly look at where he/she is going, and determine if there are any

potential packaging related problems. If so, where did the problem originate, and what

can be done about it? The designer wants a quick, easy to use and understand

methodology which consistently yields reasonably accurate results. Such a methodology

has been presemted here.

Switching noise modeling and simulation is an evolutionary process. Initially,

first estimates of system simultaneous switching requirements, and preliminary predriver,

driver and package designs are needed. Accurate package inductance estimates, obtained

by a combination of field solvers and measurements, are essential. The package model

can be simplified to its series inductance and resistance components, and any package

ground plane to VDD plane capacitance. Detailed transistor level predriver, driver and

MOSFET device models must be used to accurately estimate switching noise.

Initial simulations varying process, temperature and voltage provide information

on the magnitude of delay and noise variation over the operating range. This operating

point data is useful in later noise predictions. Next, simulations varying the numbers of

non-switching I/Os and output switching skew will assess their switching noise reduction

effects.

Enough information will now have been gathered to utilize the analytic switching noise expressions developed in Chapter 4. The designer can trade off parameters such as package inductance, the number of simultaneous switching outputs, and skew noise reduction to reach a desired maximum switching noise level. As the design changes, it is only necessary to perform a single noise simulation at one operating point. It was shown that noise levels at other operating points can be accurately predicted using the previously determined operating range data.

Damping resistor effects require realistic worst case capacitive load estimates to accurately trade switching noise reductions against delay increases. The simulations can be refined when information such as parasitic IC damping resistance, better package inductance estimates, and bypassing capacitor details becomesa available as the design progresses. If the output driver design changes drastically, the modeling and simulation methodology should be started again, since the previously obtained data and trends may be incorrect.

7.2 Contributions

This dissertation provides the designer with some insight into switching noise, and some easy to use tools for noise prediction and design. These are summarized in the following list of important contributions.

A methodology for modeling and simulation of simultaneous switching ground and power supply noise was proposed and validated.

Simple analytic expressions for simultaneous switching noise based on the non-square law drain current vs. drive voltage behavior of short channel MOSFETs were developed, including cautions about usage.

The effects of numerous parameters on simultaneous switching noise were identified and quantified. These parameters include processing, temperature, supply voltage, the number of simultaneously switching and non-switching I/Os, package inductance, switching skew, load and bypass capacitance, and substrate coupling

The effects of numerous parameters on driver switching noise and delay performance were identified and quantified, including predriver and driver sizing, and source damping resistance.

An adaptive. low noise driver design was developed, which reduced noise by a factor of four, with a delay increase penalty of approximately 25%.

A. APPENDIX: SIGNAL INTERCONNECTS

A.1 Basic Printed Wiring Board Electrical Guidelines

The purpose of this section is to give designers some indications of potential

pitfalls in high speed printed wiring board (PWB) designs. Primarily electrical issues are

addressed here. The goal is to prevent as many problems as possible in the design stage

and minimize costly and time consuming redesigns. This section will use many simple

analytic formulas which are approximations only. Only general trends and guidelines are

considered here. Specific troublesome cases should be analyzed in detail using available

transmission line calculator software tools.[124] [125] [126] [127] [128] There are a number of fine

treatments of parameter extraction tools, and detailed analysis theory and techniques in

the literature. [129] [130] [131]

The guidelines are meant to apply to digital CMOS circuits up to approximately

100 MHz operating frequency, and sub-nanosecond rise times. Clock speeds

significantly higher than this will need special treatment. These guidelines are generic in

nature. They are not intended to be an exhaustive set, but rather a checklist of things to

consider. Therefore, there will be problems unique to each specific design which may not

be addressed here fully, if at all. Some of the guidelines point out potential problem

areas. It the designer's responsibility to follow up and evaluate these. It does not

eliminate the need for normal careful analysis and design practices.

A.1.1 Overview

There are four basic areas of PWB design over which we have control:

1. The board and its physical properties

2. Parts placement or layout

3. Power and ground distribution

4. Trace Routing

All of these are related, and should be used to achieve our overall goal. That is, to minimize delay and crosstalk while maintaining board signal integrity. Each of these areas will be discussed in a bit more detail in the following sections.

One other key to success cannot be stressed enough. Although this particular document addresses electrical performance of PWB's, other aspects must not be ignored in the design process. Nothing is more important than continually maintaining a close working relationship with all areas involved with the board. Although the electrical designer is the first and primary one interested in the electrical aspects of a particular PWB, it is critical that he/she be constantly in contact with the layout, manufacturing, parts, and mechanical groups from the beginning. For high performance PWB's, it is unacceptable for each portion to be done separately. All aspects of the PWB must be considered throughout the design: performance, manufacturing, testing and reliability.

A.1.2 Board (Physical) Properties:

From an electrical standpoint, the physical properties of a board determine the characteristic impedance (Z_0) of interconnections. This includes planes and traces. Assuming lossless lines, Z_0 is real.

For lossless lines:[132]

$$C = \varepsilon W/d = \text{Capacitance per unit length}$$

$$L = \varepsilon\mu/C = \text{Inductance per unit length}$$

$$v_p = \sqrt{LC} = \text{signal propagation velocity}$$

$$Z_0 = \sqrt{\frac{L}{C}} \qquad \text{where } L, C = \text{trace inductance and capacitance per unit length}$$

The board properties we have some control over are:

trace widths

trace to trace spacing

layer spacing

ground and power plane locations

insulator dielectric (e_r)

It is difficult to drastically change Z_0 for a given board due to the weak dependence of Z_0 on all of the above parameters. Typical board trace impedances are in the range of 50 to 100 ohms.

C (and hence v_p) is proportional to $\sqrt{e_r}$, which means Z0 is proportional to $\dfrac{1}{\sqrt{e_r}}$

Specifically, $v_p = \dfrac{\text{speed of light}}{\sqrt{e_r}} = \dfrac{3 \times 10^8}{\sqrt{e_r}} \quad \dfrac{\text{meters}}{\text{second}}$

Thus, lowering the dielectric constant will result in somewhat decreased signal propagation delays, smaller crosstalk coupling capacitance, and higher impedance, easier to drive traces (transmission lines). Insulators with high dielectric constant (higher than four or five) should be avoided if possible.

A.1.2.1 Trace to Plane Spacing:

Decreasing the trace to plane spacing decreases L and increases C, therefore decreasing Z_0. The above expressions show L directly proportional and C inversely proportional to spacing. Therefore, according to the above approximations, Z_0 is proportional to spacing. However, analysis using two dimensional field solvers shows this to not be the case for traces, at least for typical board geometries. Trace Z_0 is proportional to the nth root of the spacing, where n is greater than or equal to 2. Thus, we again have a weak dependence of Z_0 and C on layer spacing. Tight tolerance on layer to layer spacing is expensive, so using spacing for extremely accurate impedance controlling is usually not practical.

Capacitance between the power and ground planes is inversely proportional to the plane to plane spacing. Power and ground planes should be arranged in pairs on adjacent layers to maximize this capacitance.

A.1.2.2 <u>Trace Width</u>

Z_0, C and L also depend weakly on trace width. Again, this is approximately a square root dependence. Controlling impedance of signal traces by varying their widths is not recommended, since tight tolerances are difficult to control.

Both trace width and trace thickness have an effect on resistance. Resistance is not normally high enough to be a concern for signal interconnects at the board level. For a one ounce copper (1.4 mils thick), 6 mil wide trace, R is less than 0.1 ohms/inch. This ignores skin effect, a valid assumption up to about 1 GHz. Power and ground should be distributed through planes, with connections made directly through vias. If any power and ground connections absolutely require a trace of substantial length, these should be made as wide as possible to minimize inductance and resistance.

A.1.3 PWB Design

A.1.3.1 Parts Placement

Typically, layout of parts is done mostly by hand, or it is an iterative process combining automated and hand layout. Unless one is in the business of designing numerous boards on aggressive schedules, the amount of extra time required by hand placement is not normally an issue. High speed designs are much more likely to work with some intelligent human intervention. Many of the layout concerns are obvious, but they should be mentioned anyway.

The first key task is smart partitioning, both at the system and the board level.

Minimize the number of off board nets required, particularly critical high speed signals.

Keep parts with many common nets in close proximity.

Keep parts with off-board I/O close to the connector, within one inch or less if possible.

Partition high speed portions together for minimum trace lengths. Separate them from other sections for reduced crosstalk.

Place high speed portions close to the board connector.

Separate analog and digital circuitry.

A.1.3.2 Power and Ground

Power and ground distribution is an extremely important issue. A good rule of thumb is to allot 10% of board I/O to power, 10% for ground. All boards should have at least one pair of power and ground planes. Place power and ground plane pairs on directly adjacent layers. Check that plane continuity is not broken up by through holes. Watch for areas on the board which are isolated in this way. Mixed analog/digital boards should have separate power and ground planes for the analog and digital portions, or the planes can be segmented.

Do not allow power or ground to be connected to any chip with traces of appreciable length. Via connections from the planes should be direct, or as close as possible to the chip power and ground pins. Traces should be no longer than 100 mils.

Decoupling capacitors for the board should be placed close as possible to the board power and ground connectors. As an estimate, approximate the total capacitive load for on-board chips. For 5% VDD variation, multiply this capacitance by 20. This is the total board decoupling capacitance required. Split this up among capacitors placed at power and ground board I/O pairs. This capacitance will probably be in the range of 10 to 50 μF. Board decoupling capacitors should be aluminum or tantalum electrolytic types with a series resistance and inductive impedance of less than one ohm. This typically means an inductance less than 10 nH for each capacitor. As an example, for six parallel board decoupling capacitors and a maximum board operating frequency of 100 MHz,

inductive impedance is about one ohm. Inductive impedance is calculated at the maximum frequency of operation.

$$Z = 2 \pi f L$$

Since there are six leads, we have

$$Z = 2 \pi \, 100e6 \, (10 \, nH / 6) = 1 \, ohm$$

Each chip should have RF-grade decoupling capacitors. Chip decoupling caps should be located directly at chip power pins. Again, trace lengths must be absolutely minimized (100 mils maximum).

A.1.3.3 <u>Signal Distribution</u>

When considering packaging and interconnect effects on signal propagation, there are two basic issues. First, a signal can be degraded by problems in its own interconnection network. Leads, board and package traces, vias, connectors, contacts and bond wires can all cause waveform delays and distortions through reflections, losses, frequency effects etc. Secondly, crosstalk problems can occur through interaction with other signals whose traces are in close physical proximity. In this section, the concentration is mainly on non-crosstalk issues.

Most commonly used circuit simulators are time domain based. Time domain differential equations describing a network are formed and solved. The solution usually involves various linearizations to reduce the problem to a system of algebraic equations

for a particular time point. Once convergence requirements are met, the simulator moves ahead in time and repeats the process. It should be noted that convergence parameters within these simulators (absolute and relative tolerances) can have a large affect on output waveforms. It was my experience that extreme caution must be exercised when evaluating results, particularly for interconnect networks. Convergence tolerances need to be varied to be certain that resulting waveform characteristics such as ringing are not simulator artifacts. It is good practice to tighten the simulation error tolerances until very little difference is observed in the waveforms. Most of this work was done on simulators such as HSPICE, Saber, and PSPICE. Saber was a particularly valuable tool. It allows user defined models to be inserted, and it has mixed mode simulation capabilities.

A.1.3.3.1 Trace Routing

Trace routing is one of the most difficult tasks in designing high frequency boards. Automatic routing of entire boards will not generally work. We need some restrictions or rules to prevent excessive delays, crosstalk, and signal distortion. How much do we want to restrict ourselves? Enforcing many rigid rules may prevent problems, but it can limit density, or inhibit auto routing. First, a few definitions which may be useful in this section:

Typical board signal propagation time is about 0.2 nanoseconds per inch of trace.

Use the expression at the beginning of this section to estimate this for a

particular board. This is wave propagation delay only, and does not

include rise time, loading, or signal distortion delays.

Long trace definition:

Traces with one way propagation delays of greater than one tenth the

signal rise time are subject to transmission line reflection effects, and are

considered long. In the literature, the definition of a long line varies from

source to source. The suggested critical propagation delay to rise time

ratio ranges from approximately one to one tenth.[133] [134]

To calculate the bandwidth of a particular signal, the following first order

approximation can be used:[135] [136]

$$\text{Bandwidth (Hz)} = \frac{0.35}{\text{minimum rise time } (t_r)}$$

$$\text{Reflection coefficient} = \frac{\text{value of reflected wave at point of reflection}}{\text{value of incident wave at point of reflection}}$$

$$= \frac{Z_{load} - Z_0}{Z_{load} + Z_0}$$

Many of the following guidelines may seem obvious, but the designer must be

aware of these potential problems and establish specific routing priorities to avoid them.

Suggested digital net routing priorities:

clocks

direct action (asynchronous) signals

high speed buses

other high speed signals with critical timing

Lengths of critical nets must be kept to a minimum. Use the above criteria for long traces as a guideline. Delays due to long nets must be factored into timing analyses. Jumps between layers results in via and Z_0 discontinuities. These should be minimized for long traces. Stubs on multiple destination signals should be kept short (less than 1 inch). Ninety degree corners on signal traces is not a big concern for frequencies less than a few gigahertz.

The designer should identify all signals which are sensitive to crosstalk, and pay particular attention to their routing. Direct action signals are the most obvious examples. Here are some techniques to help minimize crosstalk:

No signals should run parallel on the same or adjacent layers for more than two inches (less for sensitive signals).

Place signals sensitive to crosstalk on layers close to (adjacent) ground planes to minimize Z_0.

Surround sensitive signals with parallel ground traces.

Mixed analog and digital board guidelines:

Analog and digital sections should be completely separate, with separate

power and grounds.

Analog and digital traces should never be intermixed. Analog traces

should be routed over their own power and ground planes (or plane

segments).

For CMOS designs, the value of Z_0 is not extremely important. Board Z_0 ranges

between 50 and 100 ohms typically. Typical I/O driver output R is 15 to 20 ohms.

CMOS loads are high impedance and capacitive, which means a reflection coefficient of

approximately one. This can result in overshoot and ringing unless some type of limiting

is used. Most newer parts have input protection, and many have bi-directional I/O for

test. These input protection networks and the large output driver diode loading, both

serve to effectively limit the overshoot and ringing. Nets containing parts without input

protection networks should be considered candidates for a detailed transmission line

analysis. Quad Design XTK™ (crosstalk), University of Arizona tools, Saber, and SPICE

are all analog simulators which are recommended for this analysis. Refer to data books

for information on input networks.

There are two approaches for clock routing, each with its own advantages and

disadvantages. Star (or tree) routing has potentially shorter traces, with less skew

between the clocks at different destinations.[137] [138] [139] [140] This method can have problems

such as large Z_0 discontinuities, noise pulses, and distortion. Alternatively, a serpentine routing scheme with short (less than 1 inch) stub connections can minimize reflections at the expense of increased skew and delay. Detailed analog simulation of board clock distribution networks is absolutely necessary for high speed boards. The extra time taken here will result in less troubleshooting and redesign later on.

On-card clocks and resets must not be the same as off board clocks and resets. They should be buffered at the board interface.

A.2 Signal Distribution Examples

A.2.1 Communications Backplane

This example demonstrates the differences in results for different model

complexities. Each application may require a different level of models, based on clock

speed, rise time, driver type, etc. The information desired may also have an effect on the

interconnect model complexities. For example, if simple delay estimates are of primary

interest, then there may be no need to break up the interconnect into many very short

lumped segments, much less a use a full transmission line model. As long as severe

ringing and/or reflections are not present, the precise waveshape is not crucial, as long as

the delay estimates are fairly accurate.

This example analyzes signal distribution on a densely populated backplane. The

backplane and associated transceivers are designed to operate with an output swing of

only one volt.[141] The backplane consisted of 32 equally spaced card slots. Low output

capacitance, controlled slew rate drivers are used. The bus operating frequency is 40

MHz.

The simulation model block diagram is shown in Figure A.1. The complexity of

each block model was varied and the simulation results compared. The two centimeter

backplane and four centimeter PWB transmission line segments were originally modeled

as transmission lines. Later, these models were simplified to five lumped RLC segments,

and finally as a single lumped RLC. The connector, package and termination resistor

models are shown in Figure A.2, Figure A.3, and Figure A.4. A proprietary, transistor level transceiver model was used. Information concerning the backplane, PWBs and transceivers was provided by TRW Electronic Systems Group.[142]
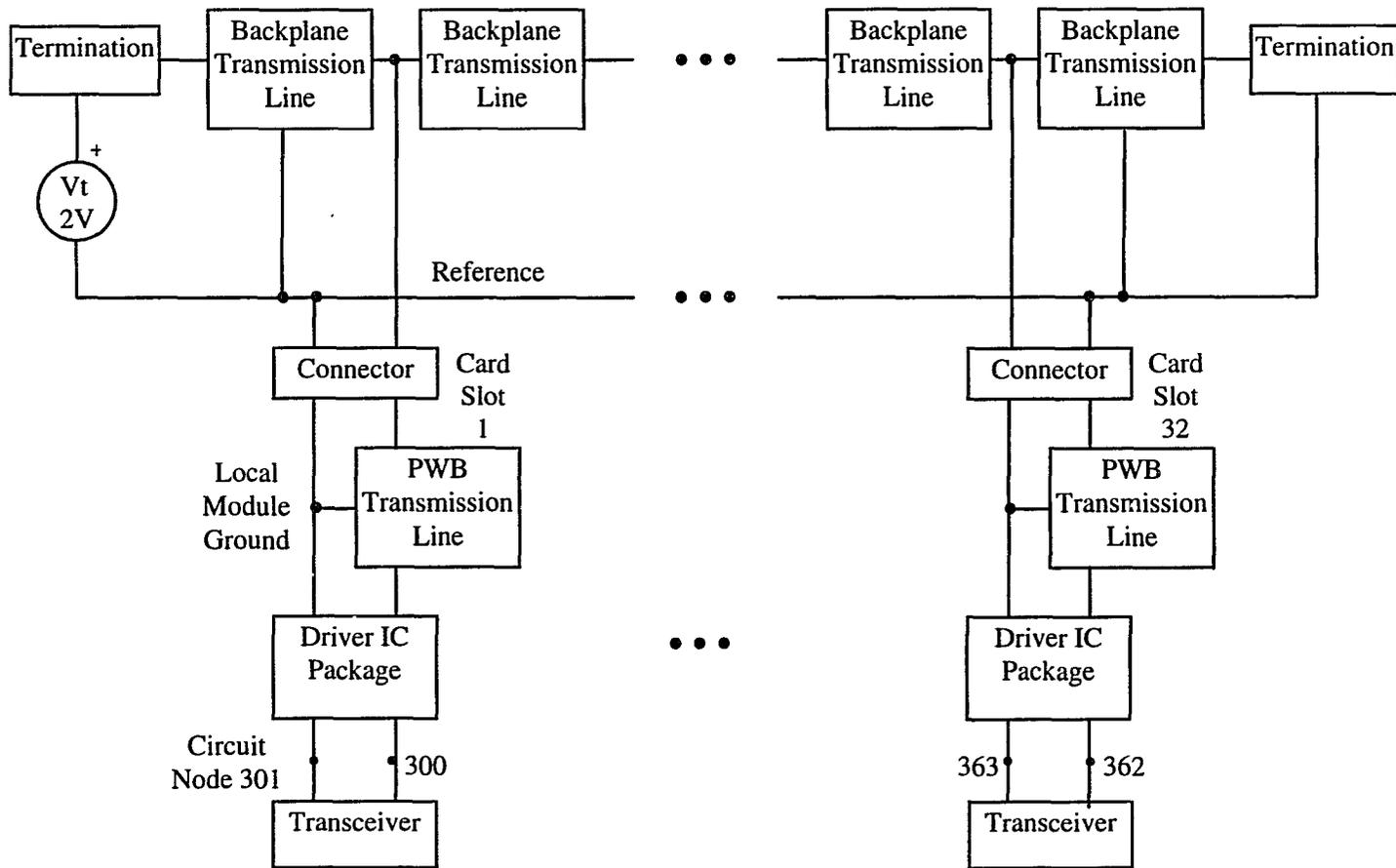
Figure A.1 - 32 Slot Backplane Model

Connector
Backplane
Thru-Hole | Connector Pin Set | Flex Cable | Module Pad and Via

a. Complex

b. Simple Single Lump
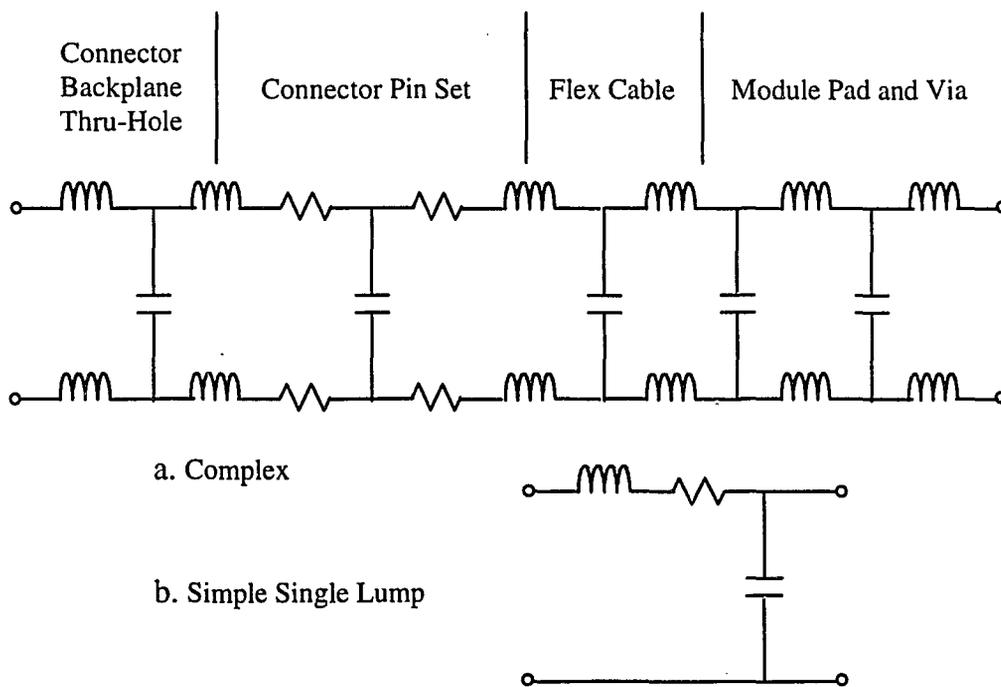
Figure A.2 - Lumped Element Backplane Connector Models

Module Via and
Transceiver Pad | Package

a. Complex

b. Simple Single Lump
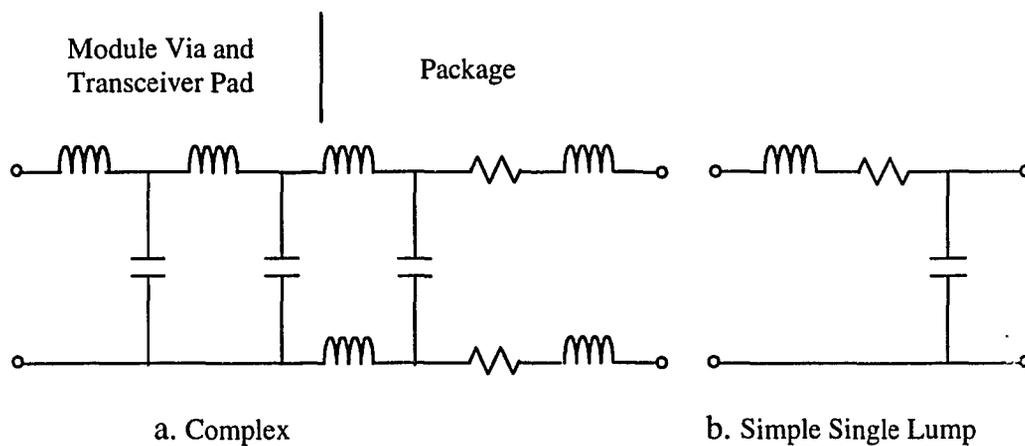
Figure A.3 - Transceiver Package Model

Backplane Thru-Hole | Resistor Lead | Resistor | Resistor Lead

Backplane ground
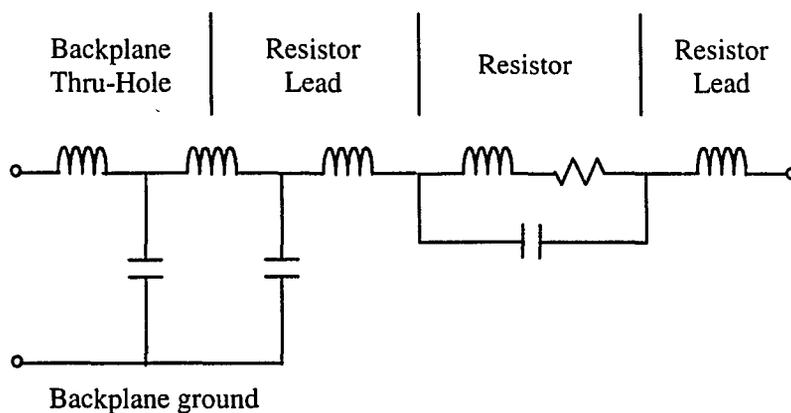
Figure A.4 - Termination Resistor Model

The bus was driven with a 40 nanosecond wide, inverted pulse from slot number 17 in the middle of the backplane. Voltages waveforms at the end of the backplane for three different models are shown in Figure A.5 and Figure A.6. Model level one contains full transmission line models for the backplane and printed wiring daughter board, and complex connector, package and termination resistor models. Level two substitutes five lumped RLC segments for the transmission line models. Model level Three contains a single lumped RLC transmission line model, the simplest connector and package models shown in Figure A.2 and Figure A.3, and a series resistance termination resistor model.

Figure A.5 shows the voltage at slot one (circuit node 300) for level one (solid curve) and level two (dotted curve) simulation models. The different model

complexities have little effect on simulation results in this case. Similarly, level three

model simulation results (solid curve) are plotted with level one model results (dotted

curve) in Figure A.6. It can be seen that the level one model is beginning to compromise

the waveforms, but the results are still close. This can be used to check our long line

definition. Assuming the signal rose time is approximately two nanoseconds, and the

time delay on the backplane is two nanoseconds per foot, a trace greater than 3

centimeters would be considered long. The four centimeter PWB traces in this example

are over this limit, as can be seen in Figure A.6.
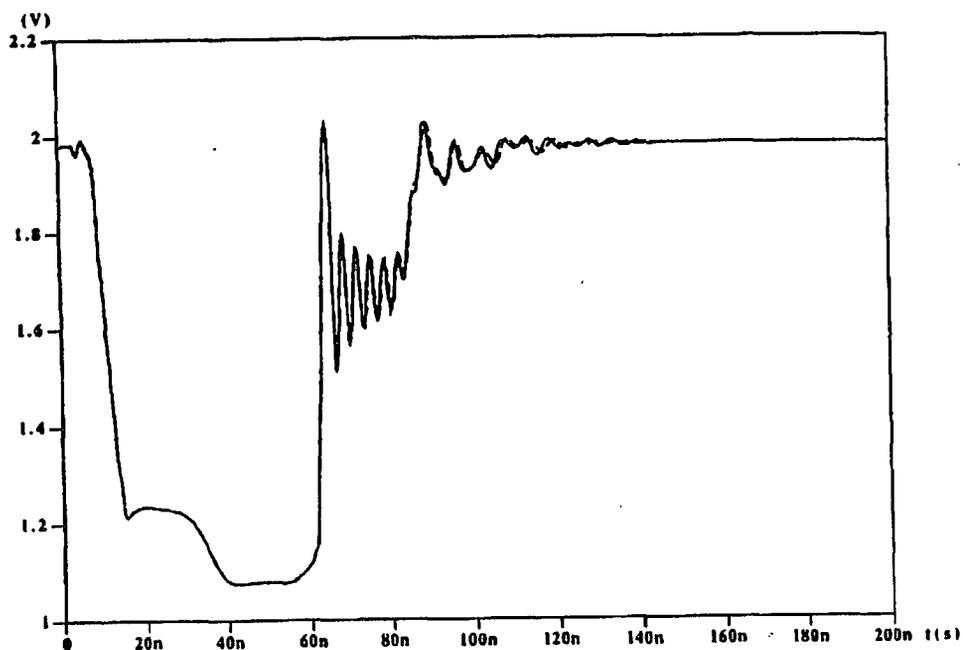
Figure A.5 - Slot One Transceiver Input Waveforms Voltage using Level One (Solid
Curve) and Level Two (Dotted Curve) Simulation Models. The
Backplane is Driven from Slot 17.
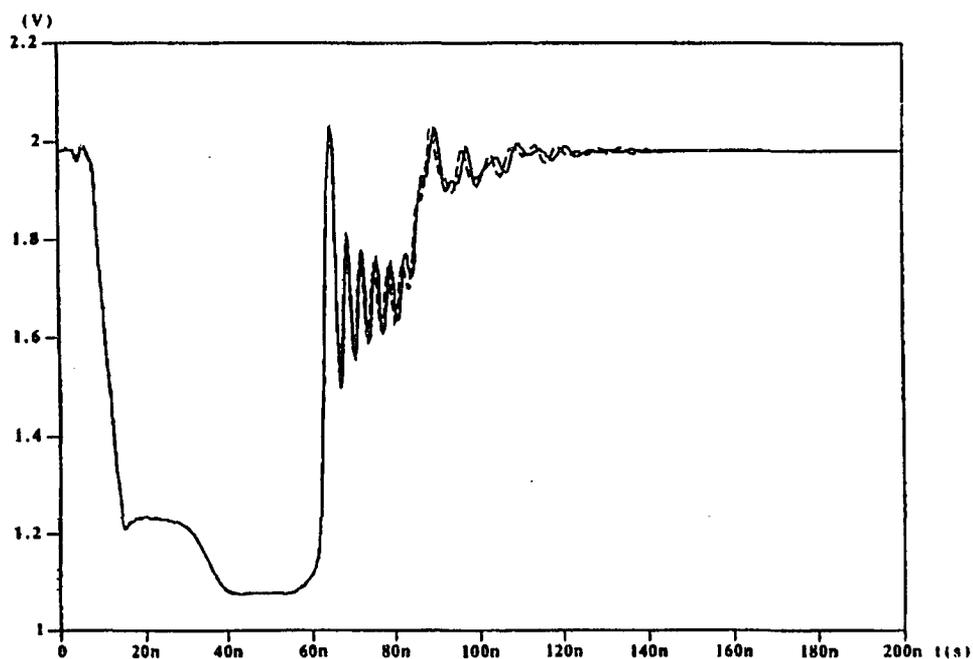
Figure A.6 - Slot One Transceiver Input Waveforms Voltage using Level One (Solid
Curve) and Level Three (Dotted Curve) Simulation Models. The
Backplane is Driven from Slot 17.

A.2.2 Clock Distribution on a Multi-Layer PWB

As a final example, consider a scan clock distribution network on a multi-layer PWB. A nominal one megahertz clock is distributed to 12 custom ASICs for scan testing. Let us examine the feasibility of operating at a higher scan clock frequency. The board has 12 metal layers, including a ground plane on layer 6 and a power plane on layer 7. The one ounce copper interconnect traces are five mils wide by 1.4 mils thick. The board metal layer spacing is 6 mils, and the dielectric is epoxy/glass ($\varepsilon_r = 4.6$).

Twelve 132 pin Ceramic Quad Flat Pack ASICs are located on layer one, as seen in Figure A.7. The scan test clock path is shown in Figure A.8. Transmission line parameters for the traces labeled 1 through 16 were found using the University of Arizona electrical parameter extraction tools UAC and MOM 1.1. Detailed transistor level input receiver models and a behavioral clock driver model were used for the simulation. With a clock rise time of approximately seven nanoseconds, we define the critical trace length as 10.7 centimeters. All interconnect sections are less than eight centimeters, thus they all are modeled as single lumped LC segments.
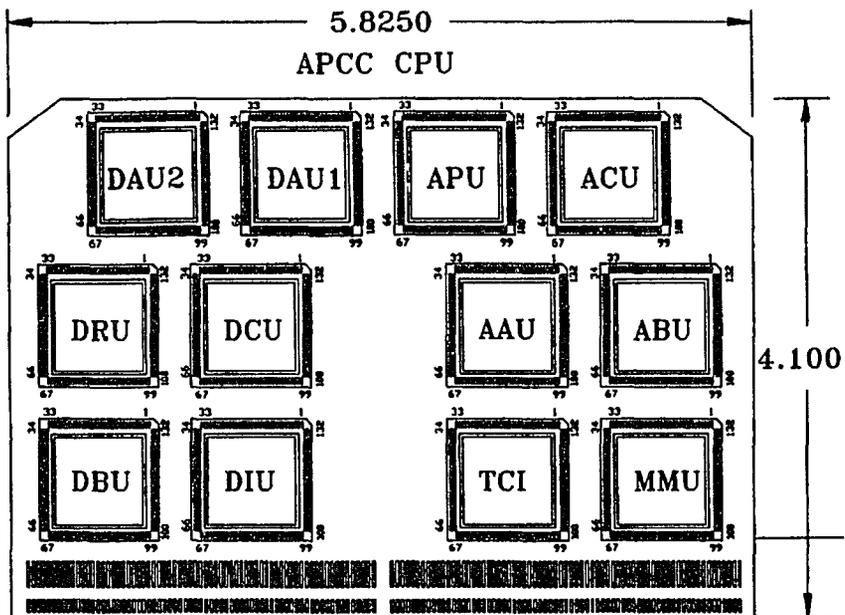
Figure A.7 - Multi-Layer CPU Printed Wiring Board.

APCC SCAN CLOCK PATH
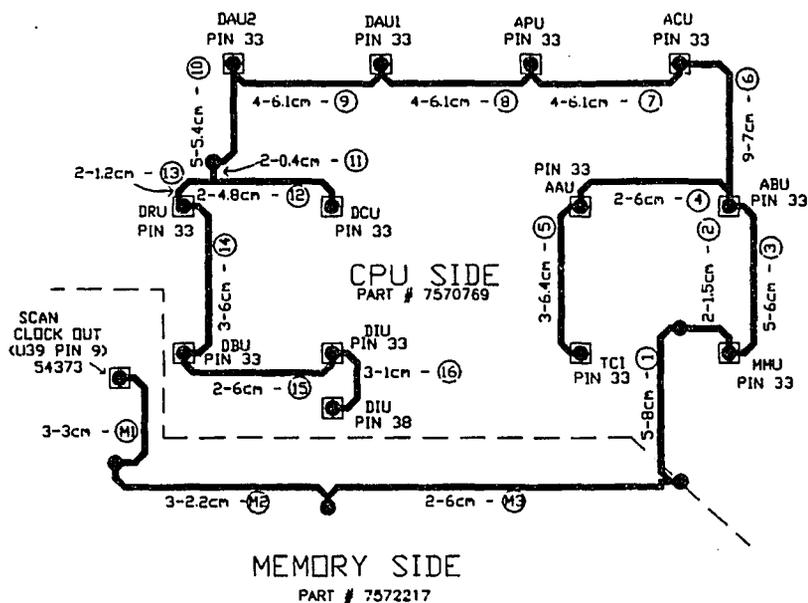
Figure A.8 - Scan Clock Path.

A 10 MHz clock was driven from the Scan Clock Out pin at the lower left of Figure A.8. Figure A.9 compares measured and simulated clock waveforms at the TCI chip scan clock input, pin 33. An active FET picoprobe mounted on an air bearing IC probe station was used in the measurements. The clock waveform is already quite distorted at the end of this stub. The match between the simulated and measured voltage signals is reasonable. The waveshapes are similar, however the simulated peak voltage is approximately 30% higher than the measured peak.

As we move further along the scan clock path, the clock signal becomes further distorted. Figure A.10 compares measured and simulated clock signals at DAU2 ASIC pin 33, and Figure A.11 shows the clock at DBU pin 33, near the end of the distribution path. Again, the match between simulation and measured data is reasonable, with similar waveshapes and peak amplitudes within 20%. Based on the measurements and simulations, we can conclude that scan clock operation at 10 MHz is marginal at best.

A1 1.30 V PHASE 360 DEG

500mV 100mV 25.0ns

(V)

3

2.5

2

1.5

1

500m

0

-500m

.1

-1.5

0 25n 50n 75n 100n 125n 150n 175n 200n 225n 250n 275n 300n t(s)
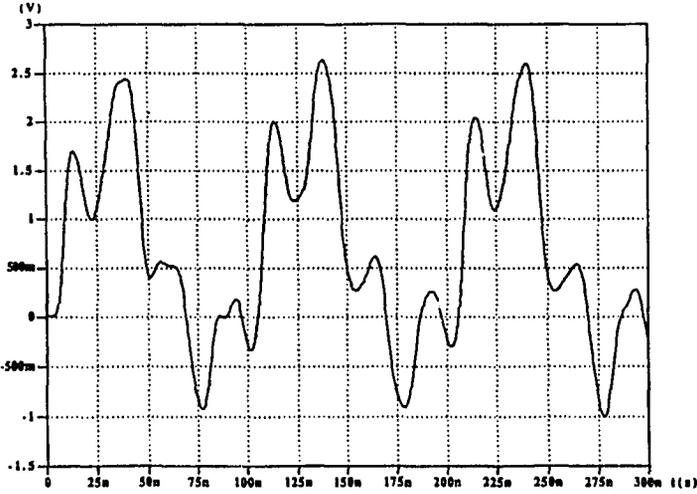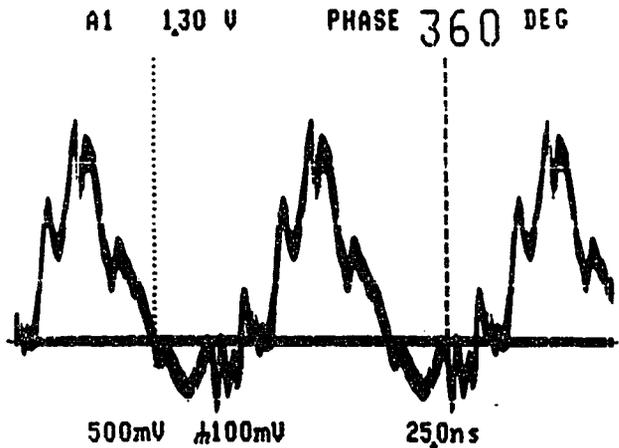
Figure A.9 - Measured and Simulated TCI 10 MHz Scan Clock Input Voltage.
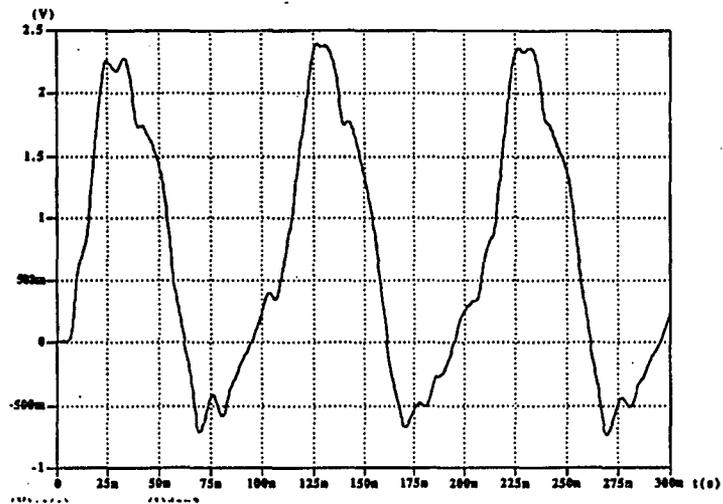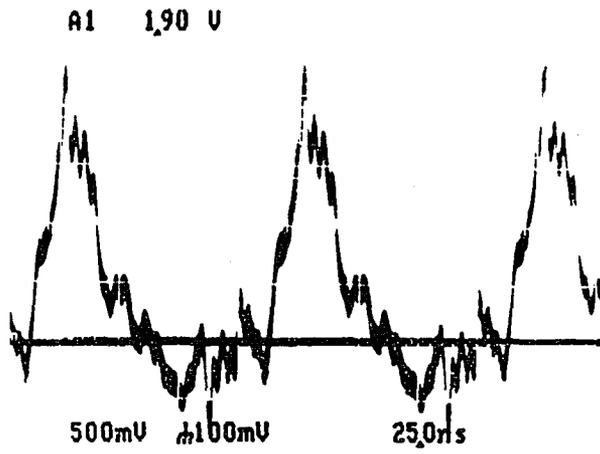
Figure A.10 - Measured and Simulated DAU2 10 MHz Scan Clock Input Voltage.

A1   0.86 V

500mV   100mV   25.0ns
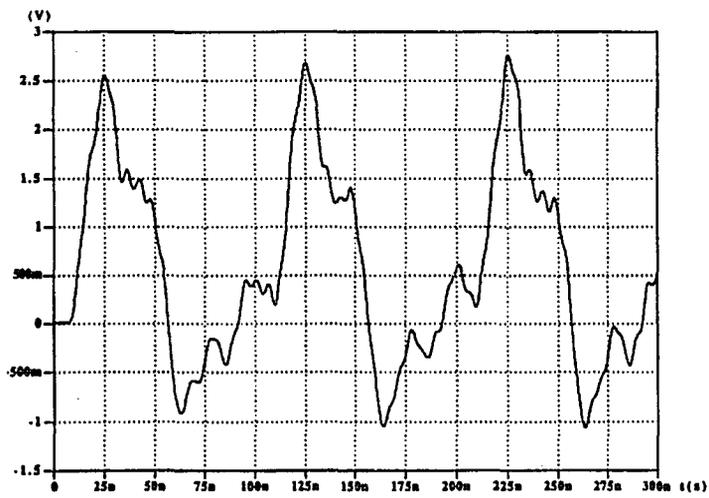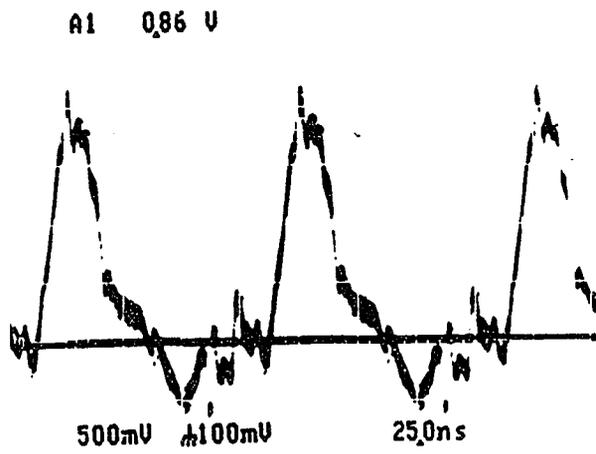
Figure A.11 - Measured and Simulated DBU 10 MHz Scan Clock Input Voltage.

Increasing the number of lumped segments in each transmission line model did little to improve the match between measured and simulated data in this example (results not shown). This illustrates the difficulty in accurately simulating signal propagation in a complex system. More accurate PWB models are necessary for a more accurate treatment. For example, nominal board, metalization and dielectric dimensions and properties rather than measurements were used for parameter calculations. Additionally, a transistor level driver model could increase accuracy. Given the distortion present in the clock waveform and the complexity of the distribution, this example is an excellent candidate for a more detailed treatment using one of the available transmission line calculators.

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