Integrated Switching DC-DC Converters with Hybrid Control Schemes

By

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AUTOBIOGRAPHY

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ABSTRACT

In the modern world of technology, highly sophisticated electronic systems such as multiprocessor modules and system-on-chips (**SoCs**) pave the way for future's information technology breakthroughs. However, rapid growth on complexity and functions in such systems has also been a harbinger for the power increase, which tends to severely limit system miniaturization, efficiency, reliability and lifetime. Power management techniques have thus been introduced to mitigate this urgent power crisis. Switching power converters are considered to be the best candidate due to their high efficiency and voltage conversion flexibility. Moreover, switching power converter systems are highly nonlinear, discontinuous in time, and variable. This makes it viable over a wide operating range, under various load and line disturbances. However, only one control scheme like pulse width modulation (PWM) cannot optimize the whole system in different scenarios. Hybrid control schemes are thus employed in the power converters to operate jointly and seamlessly for performance optimization during all operation periods of start-up, steady state and dynamic voltage/load transient state.

In this dissertation, three different switching power converter topologies, along with different hybrid control schemes are studied. **First**, an integrated switching buck converter with a dual-mode control scheme is proposed. A pulse-train (PT) control, employing a combination of four different pulse control patterns, is proposed to achieve optimal regulation performance under various operation scenarios. Meanwhile, a high-frequency pulse-width modulation (PWM) control is adopted to ensure low output ripples and avoid digital limit cycling in the steady state. **Second**, an integrated buck-boost converter with a tri-mode digital control is presented. It employs adaptive step-up/down voltage conversion to enable a wide range of output voltage.

This is beneficial to ever-increasing dynamic voltage scaling (DVS) enabled, modern power-efficient VLSI systems. Dynamic voltage scaling **(DVS)** is such a technology which adaptively adjusts the supply voltage and operation frequency according to instantaneous power and performance demand, such that a system is constantly operated at the lowest possible power level without compromising its performance. **Third**, a digital integrated single-inductor multiple-output (SIMO) converter, tailored for DVS-enabled multicore systems is addressed. With a multi-mode control algorithm, DVS tracking speed and line/load regulation are significantly improved, while the converter still retains low cross regulation.

All three integrated CMOS DC-DC converters have been designed and fabricated successfully, demonstrating the techniques proposed in this research. The measurements results illustrate superior line and load regulation performances and dynamic response in all these designs. The approaches presented in this dissertation are evidently viable for realizing compact and high efficient DC-DC converters.

CHAPTER 1 INTRODUCTION

1.1 Motivation

In recent years, the development of advanced VLSI systems poses new challenges on power supply designs. Such a supply is expected to have fast transient performance to immediately response to sudden load changes of multi-mode systems. In addition, it should maintain low ripple voltage all the time for clean power delivery to all circuit modules and devices. A switching power converter is considered as one of the best candidates due to its high efficiency and voltage conversion flexibility. However, for a conventional PWM controlled switching converter, certain drawbacks exist for these new applications.

For a voltage-programming PWM converter, due to the existence of the complex poles in the loop gain transfer function, it is very difficult to design the compensation network to achieve a wide loop-gain bandwidth and thus fast response [Ki-98].

For a current-programming PWM converter, although it has two separated poles in transfer function and wider loop-gain bandwidth, special current sensing circuit is required and ramp compensation has to be made to avoid sub-harmonic oscillation [Ki-98b].

Dynamic voltage scaling (**DVS**) is considered as the most effective low-power operation technique in modern VLSI circuit designs [Burd-00] [Kwon-03]. One most challenging issue in DVS is to design "untraditional" variable power supplies [Calhoun-06] [Nowka-02]. Such a supply is usually implemented by a switching DC-DC converter because of high efficiency and flexible voltage conversion.

Most popular DVS systems employ an external variable-output DC-DC converter. However, as the scale of VLSI system increases, single dynamic DC-DC converter can hardly

minimize system power consumption, especially when processor cores or functional modules require their peak power at different times. Hence, multiple voltage level operations are highly demanded. These ideas are also encouraged by ITRS in Executive Summary [ITRS-09]. Recent researches maximize power control flexibility by using multiple and variable power supplies. Compared to the other DVS techniques, this new technique can further reduce the power by 20% or more [Iyer-02].

In a portable device, such as cell phone, MP3 player, PDA, or Laptop, different DC supply voltage levels suitable for different components are included. In modern electrical and electronic technology, voltage scheduling with multiple and variable supply voltage optimization draw great interests, because multiple and variable supply optimization is the single most effective wave to reduce power consumption of circuits, especially digital circuit.

1.2 Research Goals and Contributions

The goal of this research is to design and implement low-voltage high-efficiency DC-DC converters with hybrid control schemes for power reduction techniques and multiple-supply and variable supply systems. Many system and circuit-level techniques were developed to enhance the performance of DC-DC converters. Several key research contributions are highlighted below:

1) Developed a switching buck converter with dual-mode pulse-train and PWM control, which enjoys the flexibility of operating in either the high-frequency PWM mode for low output ripple voltage or the pulse train mode for fast load transient response. [Luo-07][Luo-08b][Luo-09].

2) Developed a digital tri-mode controlled variable-output buck-boost power converter for DVS-enabled integrated systems. Three voltage and current control modes operate jointly and seamlessly to optimize the converter's performance at

start-up, steady state and dynamic voltage/load transient state, respectively. [Luo-08a].

3) Developed a digital single-inductor multiple-output (SIMO) step-up/down power converter with multiple control schemes for DVS-enabled multicore systems.

4) Successfully fabricated a CMOS integrated switching dc-dc converter with dual-mode pulse-train/PWM control. The output ripple voltage is reduced to ±12.5 mV in PMW mode and the load transient response is shorter than 345 ns with 100% load current change from 50 to 100 mA. The maximum efficiency is 91% [Luo-07][Luo-08b][Luo-09].

5) Successfully fabricated a digital tri-mode controlled variable-output buck-boost power converter for DVS-enabled integrated systems. The converter precisely provides an adjustable power output within a voltage range from 0.9 to 3.0 V and a power range from 11 to 800 mW. Maximum efficiency of 96.5 % is measured at 0.9-V output and 45-mW load power [Luo-08a].

1.3 Dissertation Organization

The rest of the dissertation is organized as follows. Chapter 2 addresses fundamental knowledge and design considerations of DC-DC converter designs. Basic DC-DC converter architectures and control topologies like PWM, hysteretic control, digital control are analyzed. Multiple-voltage scheduling (MVS) and dynamic voltage scaling (DVS) techniques are then discussed for both digital and analog VLSI systems. Prior arts on SIMO converter are discussed. Existing DC-DC conversion solutions are also compared, and inductor based switching converters are finally chosen for implementing the power management systems in this research.

Chapter 3 presents an integrated switching buck converter with a dual-mode control scheme. A pulse-train (PT) control, employing a combination of four different pulse control patterns, is proposed to achieve optimal regulation performance under various operation scenarios. Meanwhile, a high-frequency pulse-width modulation (PWM) control is adopted to ensure low output ripples and avoid digital limit cycling in the steady state. The converter was designed and fabricated with a 0.35-μm digital CMOS N-well process. Experimental results are shown to verify the validity of the designs.

In Chapter 4, an integrated buck-boost converter with a tri-mode digital control is presented. It employs adaptive step-up/down voltage conversion to enable a wide range of output voltage. This is beneficial to ever-increasing dynamic voltage scaling (DVS) enabled, modern power-efficient VLSI systems. Three voltage and current control modes operate jointly and seamlessly to optimize the converter's performance at start-up, steady state and dynamic voltage/load transient state, respectively. To avoid latch-ups and large leakage current, a compact automatic substrate switching circuit (ASSC) is introduced, which is compatible with low-cost single-well digital CMOS process. The converter was designed and fabricated with a standard 0.35-μm digital CMOS N-well process. Experimental results are presented to show the performance of the converter.

Chapter 5 presents a digital integrated single-inductor multiple-input multiple-output (SI-MIMO) converter, tailored for DVS-enabled multicore systems. In this design, each power output employs a step-up/down voltage conversion, thereby enabling a wide range of variable output voltage. This is beneficial to dynamic voltage scaling (DVS) techniques that are in high demand by low-power multicore systems. With a multi-mode control algorithm, DVS tracking speed and line/load regulation are significantly improved, while the converter still retains low

cross regulation. Designed with a 180-nm digital CMOS process, the converter precisely provides three independently variable power outputs from 0.9 to 3.0 V, with a total power range from 33 to 900 mW.

Chapter 6 provides conclusions and future work on single inductor multiple-input multiple-output (SI-MIMO) power converter design and the thermal sensing and thermal shutdown circuit design.

CHAPTER 2 DC-DC CONVERTER FOR LOW-POWER EMBEDDED SYSTEMS

2.1 Introduction on DC-DC Converter

Microprocessors are often used in systems where the energy to operate the device is provided by a rechargeable battery. One example of such a system is a portable computer. The voltage regulation tolerance for the microprocessor is often smaller than the voltage variation of the battery, since the battery voltage can vary due to a number of reasons including temperature, state of charge, battery current, and aging. Therefore a voltage regulator is used to process the widely varying battery voltage and provide the well-regulated power supply voltage that the microprocessor requires.

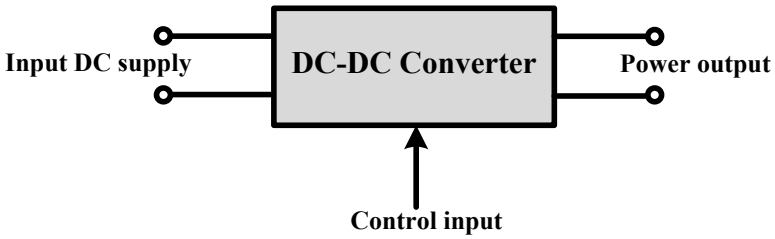


Figure 2.1.1 System schematic of DC-DC converter.

It is desirable for the voltage regulator to be as efficient as possible to maximize the battery operation time and minimize the amount of heat generated by the portable device. It is also desirable to keep the weight and size of the voltage regulator as low and small as possible.

For these reasons, a DC-DC converter type of voltage regulator is often used. A switching converter uses switches and energy storage elements to efficiently convert power from one form to another. In this case, the power conversion needed is a voltage conversion from the battery voltage to the μP power supply voltage. A switching converter that performs this type of

function is called a DC-DC converter [Erickson-01]. The abbreviation "DC" stands for "Direct Current" and implies a voltage or current waveform that is constant with time, as opposed to an "Alternating Current" or "AC" waveform that changes polarity with time. A DC-DC converter can convert one DC voltage to another DC voltage, as shown in Figure 2.1.1.

2.1.1 DC-DC Converter Specifications

DC-DC converters are characterized to quantify their ability to transform an input supply voltage into desires voltage levels as required by the loads. It is desire to have a DC-DC converter that has the minimum power loss thus has the maximum efficiency, at the same time, the output voltage is still well regulated under all operation conditions: start-up, steady-state, and line/load regulations. Several basic DC-DC converter specifications are explained in the following subsections.

1. **Power efficiency (η)**: The efficiency of a DC-DC converter is defined as the ratio of the output power delivered to the load (P_{load}) and the input power drawn from the power source (P_{in}), and is given by

$$\eta = \frac{P_{load}}{P_{in}} = \frac{P_{load}}{P_{load} + P_{loss}} . \tag{2.1}$$

   Where P_{loss} represents the power loss of the whole system. DC-DC converters are always designed to minimize the power loss and therefore achieve high efficiency.

2. **Line regulation**: Line regulation is the capability to maintain a constant output voltage level on the output channel of a power supply despite changes to the input voltage level. Line regulation is expressed as percentage of change in the output voltage relative to the change in the input line voltage.

$$line\_regulation = \frac{V_{out}\big|_{V_{in\_\max}} - V_{out}\big|_{V_{in\_\min}}}{V_{in\_\max} - V_{in\_\min}} \times 100\% = \frac{\Delta V_{out}}{\Delta V_{in}} . \quad (2.2)$$

3. **Load regulation**: Load regulation is a measure of the ability of an output channel to remain constant given changes in the load. Variations in the load result in changes in the output current. This variation is expressed as a percentage of range per amp of output load and is synonymous with a series resistance.

$$load\_regulation = \frac{V_{out}\big|_{i_{load\_\max}} - V_{out}\big|_{i_{load}\min}}{i_{load\_\max} - i_{load\_\min}} \times 100\% = \frac{\Delta V_{out}}{\Delta i_{load}} . \quad (2.3)$$

4. **Thermal coefficient**: thermal coefficient refers to the ability of a power converter to maintain the output voltage under variation of thermal conditions,

$$TC(V_{out}) = \frac{\Delta V_{out}}{\Delta T} , \quad (2.4)$$

5. **Continuous conduction mode (CCM)**: Continuous-conduction-mode (CCM) means the averaged load current I_{load} is large and the inductor current I_L never goes to zero between switching cycles, as shown in Figure 2.1.2.

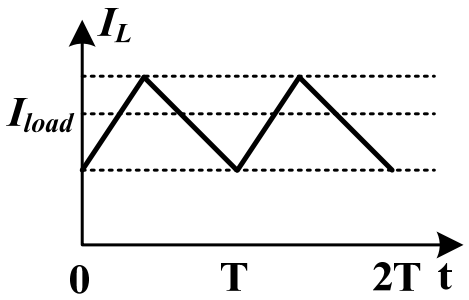


Figure 2.1.2 Inductor current in CCM.

6. **Discontinuous conduction mode (DCM):** As shown in Figure 2.1.3, in discontinuous-conduction-mode (DCM), the current goes to zero during part of the switching cycle. In buck derived converters the major effect is that when it changes from CCM to DCM, it goes from a second order system to first order system.

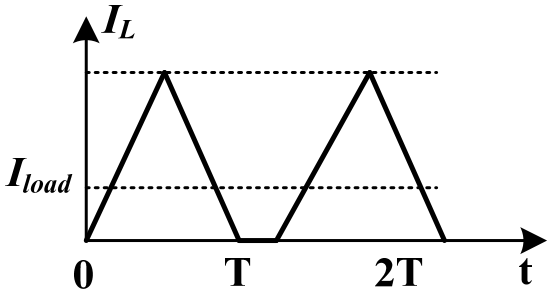


Figure 2.1.3 Inductor current in DCM.

7. **Pulse-width modulation (PWM): PWM** means that the converter operates at a fixed switching frequency. The DC-DC converter is regulated by varying the duty ratio rather the switching period.
8. **Pulse-frequency modulation (PFM)**: **PFM** means the converter operates with a variable switching frequency. This operation mode is helpful when the system has light load for high efficiency.

2.1.2 DC-DC Converter Circuits

A. Linear Regulator

A linear regulator takes an input DC power supply and produces a controlled output DC power supply by dissipating some power. There are two basic topologies of linear regulator:

- The series regulator

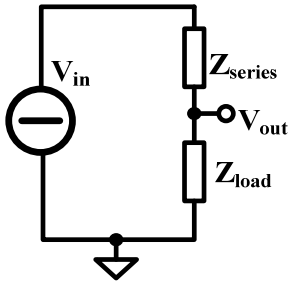


Figure 2.1.4 Schematic of a series regulator.

The series regulator is used if the input power supply is low impedance, which is the most common case. As shown in Figure 2.1.4. Here, the load Z_{load} and Z_{series} is in series. Neither Z_{load} and Z_{series} need to be linear elements, however, it can be seen that the current through Z_{load} and Z_{series} are the same. As we know, with stable (DC) conditions, the efficiency can be seen to be:

$$\eta_{series} = \frac{V_{load}}{V_{in}}, \tag{2.5}$$

where η_{series} represent the efficiency, V_{load} is the voltage across Z_{load}, and V_{in} is the input voltage. Note that the efficiency is only affected by V_{in} and V_{load}, the current I is irrelevant.

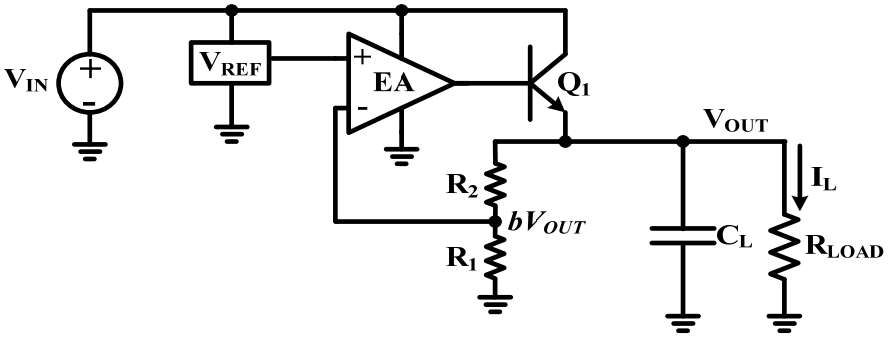


Figure 2.1.5 Schematic of a series voltage regulator.

The simplest way to implement a series regulator is a resistor divider, however, they have their limitations. Using a resistor to drop voltage makes the output dependent on output load current (load regulation) and also on the input voltage (line regulation). We need some control

system to measure the output and vary Z_{series} such that the output is invariant with input voltage and load current (voltage regulator) or invariant with input voltage and load voltage (current regulator).

A series voltage regulator is shown in Figure 2.1.5, it is based on an active device (such as a bipolar junction transistor, or MOS transistor) operating in its "linear region". the power transistor Q_1 is made to act like a variable resistor, continuously adjusting a voltage divider network to maintain a constant output voltage, and a feedback network compares the output voltage V_{OUT} to the reference voltage V_{REF} in order to adjust the input to the transistor, thus keeping the output voltage reasonably constant.

All linear regulators require an input voltage at least some minimum amount higher than the desired output voltage. That minimum amount is called the drop-out voltage. For example, a common low power regulator has an output voltage of 3V, but can only maintain this if the input voltage remains above about 3.3V. Its drop-out voltage is therefore 3.3V−3V = 0.3V. When the supply voltage is less than about 0.3V above the desired output voltage, as is the case in low-voltage microprocessor power supplies, so-called low dropout regulators (LDOs) must be used. The efficiency of the linear regulator is low because the transistor is acting like a resistor and the dropout voltage is always there.

- The shunt regulator

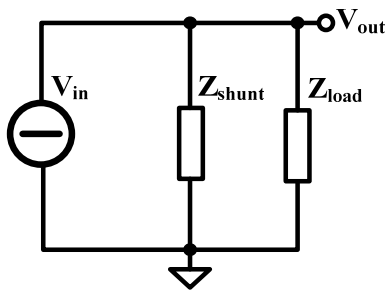


Figure 2.1.6 Schematic of a shunt regulator.

The shunt regulator is used if the input power supply is high impedance. Here Z_{load} and Z_{shunt} are in parallel. The voltage across Z_{load} and Z_{shunt} are the same. Under stable (DC) conditions, the efficiency can be seen to be:

$$\eta_{shunt} = \frac{I_{load}}{I_{in}}, \tag{2.6}$$

where η_{shunt} represent the efficiency, I_{load} is the current through Z_{load}, and I_{in} is the input current (sum of I_{load} and I_{shunt}). Note that the efficiency drops to zero as the current through the load drops to zero.

A common example of shunt regulation would be to use a zener diode as Z_{shunt}, the input current would be supplied from a high impedance source such as a charge-pump or from a series element, such as a depletion FET, a current mirror output or a high value resistor.

B. Switched-Capacitor Power Converter (Charge Pump)

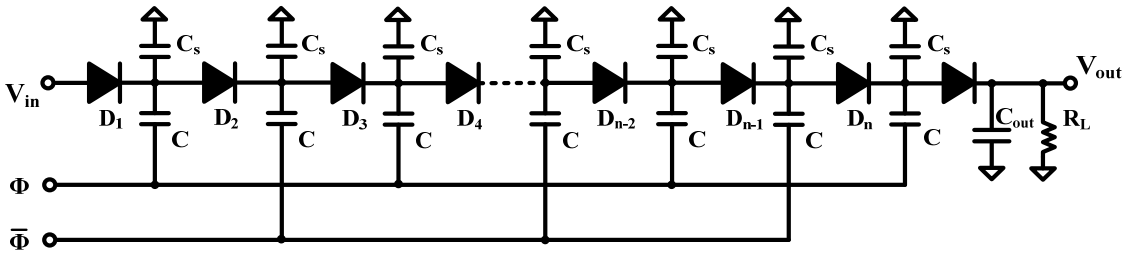


Figure 2.1.7 Schematic of Dickson charge pump.

With the proliferation of battery-operated portable devices and emerging self-powered sensing and biomedical applications, integrated power electronics attracts ever-increasing attentions for power-efficient VLSI designs. A clean and stable on-chip power line is paramount to operation performance and battery run-time. Nowadays, most integrated power supplies are implemented with three major types of DC-DC conversion circuits: switch mode power converter (or switching converter in short), switched-capacitor (SC) power converter (or charge

pump for open-loop design) and linear regulator. For those applications that require voltage(s) higher than the supply voltage, such as LCD drivers, EEPROMs and electrostatic actuator drivers, boost switching converter and SC power converter are usually the best solutions.

A power stage, usually referred as charge pump, is the most important part for a SC power converter. The original idea of designing a charge pump was first proposed by Cockcroft and Walton in [Cockroft-32]. The circuit was used to generate steady potentials near 800,000 volts in connection with studying on the atomic structure of matter. In this design, multiple capacitors can be connected in either series or parallel, by controlling the power switches in between. The circuit structure is quite simple. However, in practice, the circuit suffers low efficiency due to large on-chip stray capacitance. In addition, the output impedance of the circuit increases rapidly with the number of the stages. In order to overcome these limitations, a new charge pump circuit was proposed by Dickson in [Dickson-76]. Compared to Cockcroft-Walton voltage multiplier, Dickson charge pump is more efficient and its driving capability is independent of the number of multiplier stages.

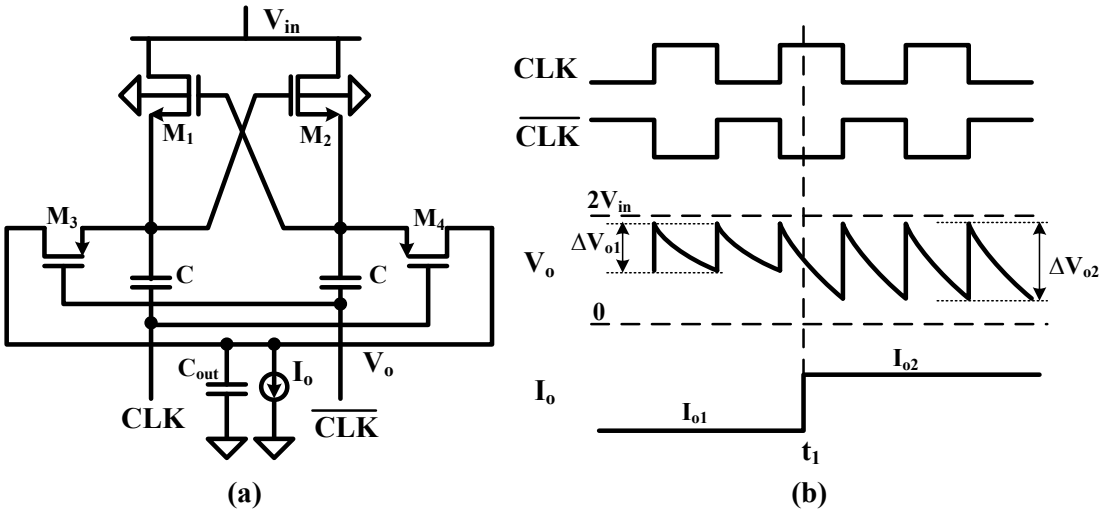


Figure 2.1.8 (a) Schematic of a cross-coupled voltage doubler, (b) major waveforms in voltage doubler.

Another cross-coupled charge pump is illustrated in Figure 2.1.8(a) [Ma-08a]. The operation of the circuit is mainly managed by a pair of non-overlapping, complementary clocks *CLK* and $\overline{CLK}$ as shown in Fig. 2.1.8(b). The transistors M_1 and M_2 are successively switched on and off in order to charge capacitors C_1 and C_2 to V_{IN}. After a few clock cycles, the voltage on the top plates of the capacitors will be (V_{IN} + V_{DD}), where V_{DD} represents the amplitude of the clocks. Then the switches M_3 and M_4 are periodically turned ON and OFF to charge the output to a value of (V_{IN} + V_{DD}). If V_{IN} = V_{DD} then the output doubles the supply voltage. Hence,

$$V_{OUT} = 2V_{DD}. \tag{2.7}$$

C. Switch Mode DC-DC Converter

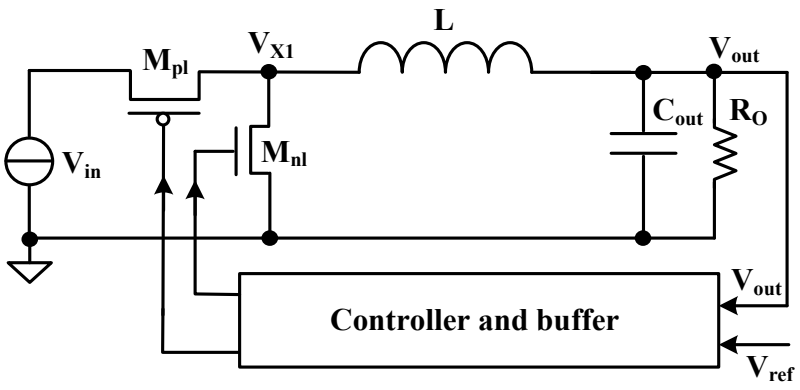


Figure 2.1.9 Schematic of a switch mode buck converter.

A switch mode power converter switches a power transistor between saturation (full on) and cutoff (completely off) with a variable duty cycle whose average is the desired output voltage, as shown in Figure 2.1.9. The resulting rectangular waveform is low-pass filtered with an inductor and capacitor. The main advantage of this method is greater efficiency because the switching transistor dissipates little power in the saturated state and the off state compared to the semiconducting state (active region). Other advantages include smaller size and lighter weight (from the elimination of low frequency transformers which have a high weight) and lower heat

generation due to higher efficiency. Disadvantages include greater complexity, the generation of high amplitude, high frequency energy that the low-pass filter must block to avoid electromagnetic interference (EMI), and a ripple voltage at the switching frequency and the harmonic frequencies thereof.

2.1.3 Switch Mode DC-DC Converter Topology

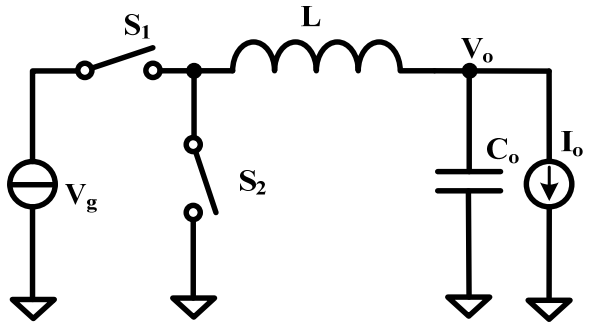


Figure 2.1.10 Switched mode DC-DC converter topologies: buck converter.

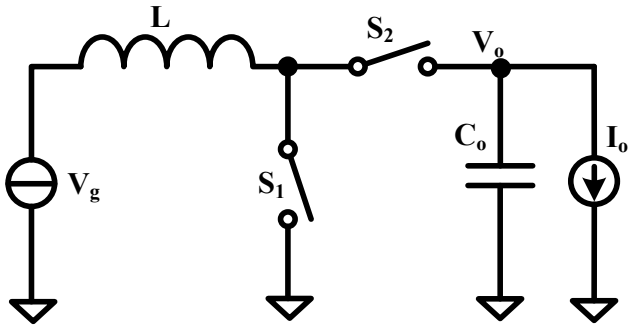


Figure 2.1.11 Switched mode DC-DC converter topologies: boost converter.

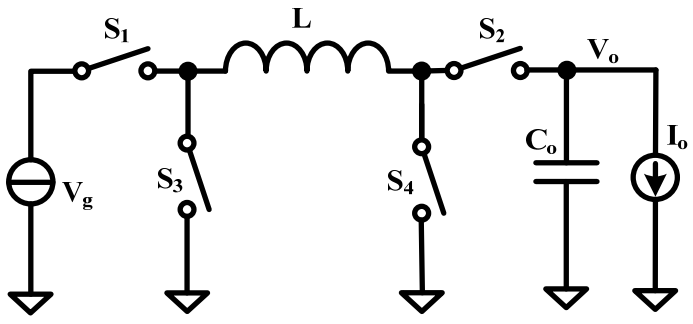


Figure 2.1.12 Switched mode DC-DC converter topologies: buck-boost converter.

There are three major topologies in the switching DC-DC converters. Those are categorized as buck, boost, and buck-boost converters. First, the buck converter realizes the step-down voltage conversion: the output voltage is lower than the input voltage. Second, the boost converter realizes the step-up voltage conversion: the desired output voltage is higher than the input voltage. Lastly, the buck-boost converter, which is also called as flyback converter, is realizes both step-up and step-down voltage conversions.

The operation principles of those three types of converter are given as follow. First, Figure 2.1.10 shows a circuit diagram of the buck converter. The energy is transferred only when S_1 is ON and S_2 is OFF. Hence, the average output voltage in this topology is,

$$\frac{V_o}{V_g}_{buck} = \frac{t_{on}}{T} = D, \tag{2.8}$$

where D is the duty-ratio, t_{on} is switching-ON period, and T is the one switching period.

For the boost converter shown in Figure 2.1.11, the average inductor voltage over the complete cycle is zero,

$$V_g \cdot t_{on} - (V_o - V_g) \cdot t_{off} = 0, \tag{2.9}$$

hence,

$$V_g \cdot DT - (V_o - V_g) \cdot (1-D)T = 0. \tag{2.10}$$

Then the conversion ratio can be calculated as

$$\frac{V_o}{V_g}_{boost} = \frac{1}{1-D}. \tag{2.11}$$

Figure 2.1.12 shows a circuit diagram of the non-inverting buck-boost regulator. Using the similar idea of the boost regulator, we get

$$V_g \cdot DT - V_o \cdot (1-D)T = 0. \tag{2.12}$$

And the input to output voltage ratio is,

$$\frac{V_o}{V_{g\ buck-boost}} = \frac{D}{1-D}. \tag{2.13}$$

2.2 Control Methodology in Switch Mode DC-DC Converter

In ideal case, the input-output voltage ratio is directly followed by the duty ratio as shown in Equation (2.12). However, in a realistic case, the real input-output voltage conversion does not exactly depend only on the ideal duty ratio value due to following reasons. First, switch (MOS transistor) has a finite turn-on resistance value and produces a voltage drop across the switch. Second, this voltage drop is varied by the different load condition with average current level changes. Third, the inductor has the effective series resistance which builds another voltage drop. All of these increase the dependency of output voltage on load. Fortunately, the closed-loop regulation technique proposed recently can significantly reduce this dependency.

2.2.1 Voltage-Mode PWM Control

Based on the information used to control the converter, voltage mode or current mode control methods can be applied. Voltage mode control uses only output voltage information to control the converter. Current mode control uses both the output voltage and the inductor current information to control the converter. The details about voltage mode and current mode control will be discussed in the following sections.

A schematic of analog voltage mode PWM (pulse width modulation) controlled buck converter is shown in Figure 2.2.1. The output stage consists of a filtering capacitor C_o and a (resistive) load R_o. The output voltage V_o is attenuated by the resistor string R_3 and R_4, and is fed back to the error amplifier and compared with a reference voltage V_{ref} to determine the trip point

of the PWM comparator and generate the error voltage V_e. Then, a comparator stage quantizes V_e with the reference of the fixed frequency ramp signal. PWM modulator generates the PWM signal that has a duty ratio proportional to the V_e.

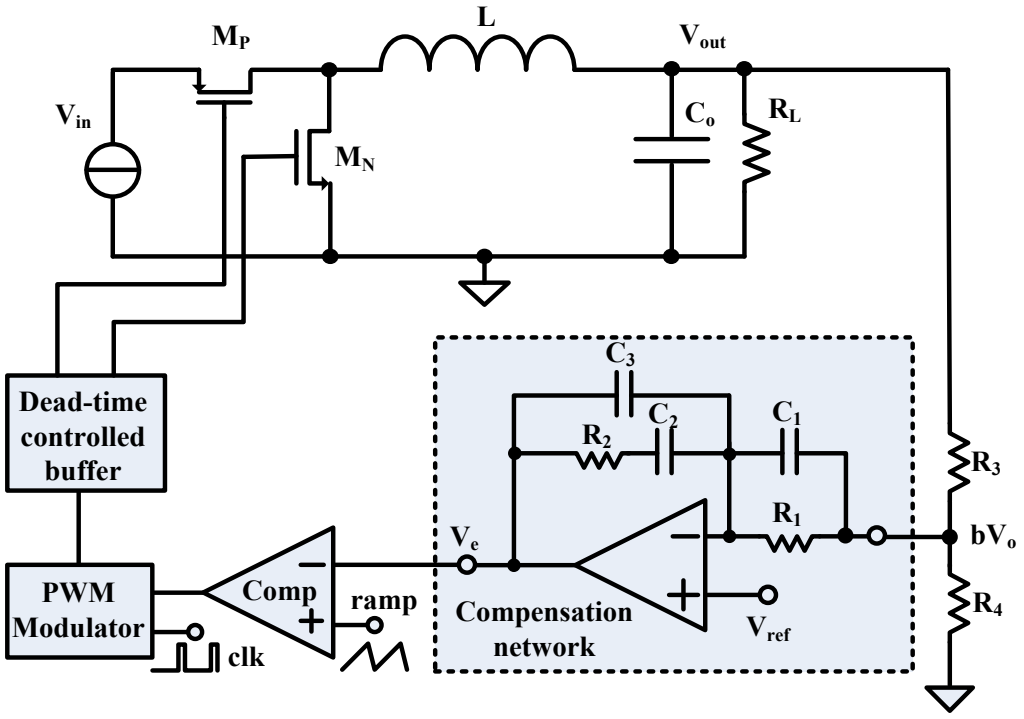


Figure 2.2.1 Schematic of conventional voltage mode PWM controlled buck converter.

In a voltage mode PWM converter, due to the existence of the low-frequency complex poles in the loop gain transfer function, it is very difficult to design the compensation network for a wide loop-gain bandwidth.

2.2.2 Current-Mode PWM Control

Another popular control technique for switch mode DC-DC converter is the current mode control as shown in Figure 2.2.2. Instead of comparing the error voltage, V_e, to an externally generated ramp signal, the V_e is now compared to the inductor current signal. The basic operation of the current mode control can be shown in the waveforms of the V_{RF} and control signal (Figure 2.2.3): During the switching signal ON, the inductor current builds up linearly.

When inductor current-sensed voltage V_{RF} reaches to the V_e, the comparator sends a reset signal to the PWM modulator and turns switching signal OFF. Now the inductor current decreases linearly so does the V_{RF}. Until the reset is performed from the system CLK, the switching signal stays OFF. Finally this switching ON/OFF action performs the output regulation. For example, when inductor suddenly carries higher currents, a V_{RF} will increase with stiffer slope during the period DT. This will turn the switch OFF earlier resulting narrower D.

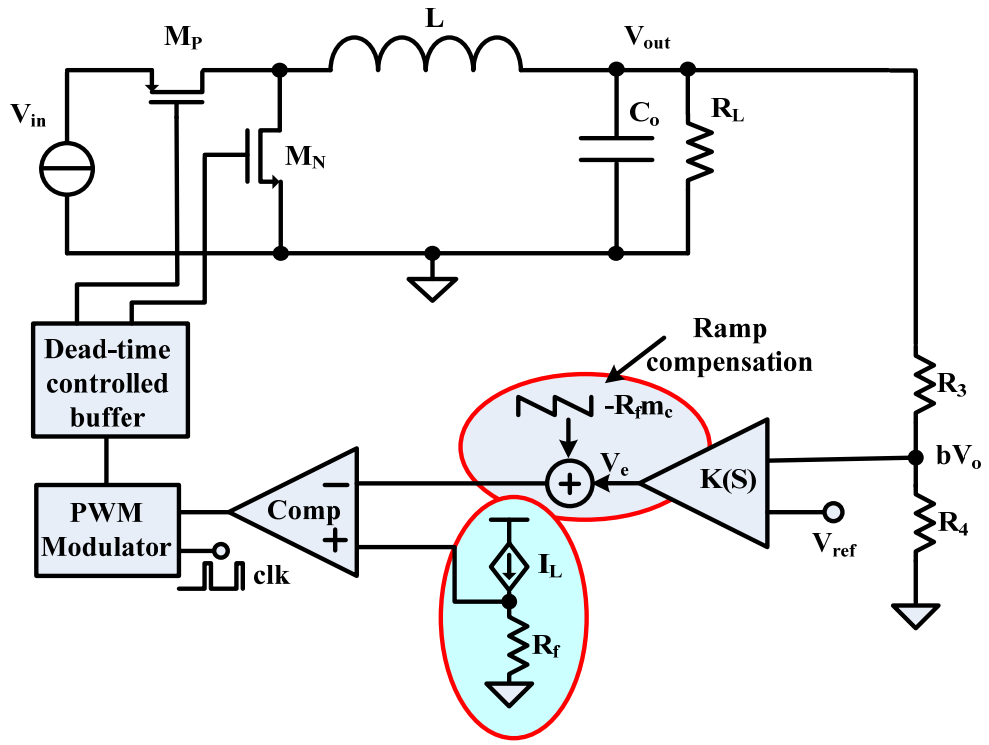


Figure 2.2.2 Schematic of conventional current mode PWM controlled buck converter.

Comparing the current mode control with voltage mode control, we can see that, in current mode control, the inductor current follows the current command almost instantaneously. In a simple and approximate model, it removes the inductor pole from the loop. This makes the power stage transfer function to the first order shape. Therefore, faster transient response can be obtained with current mode control with a simpler compensation network. Furthermore, a current

limit protection can be easily implemented by limiting the maximum level of error voltage, V_e, hence the inductor current i_L.

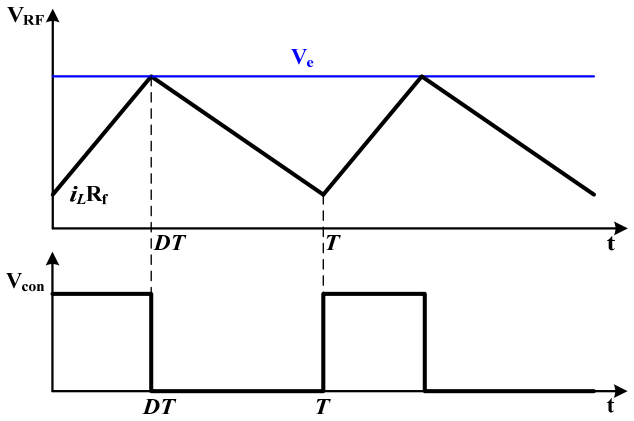


Figure 2.2.3 Waveforms of the control signals in current mode control.

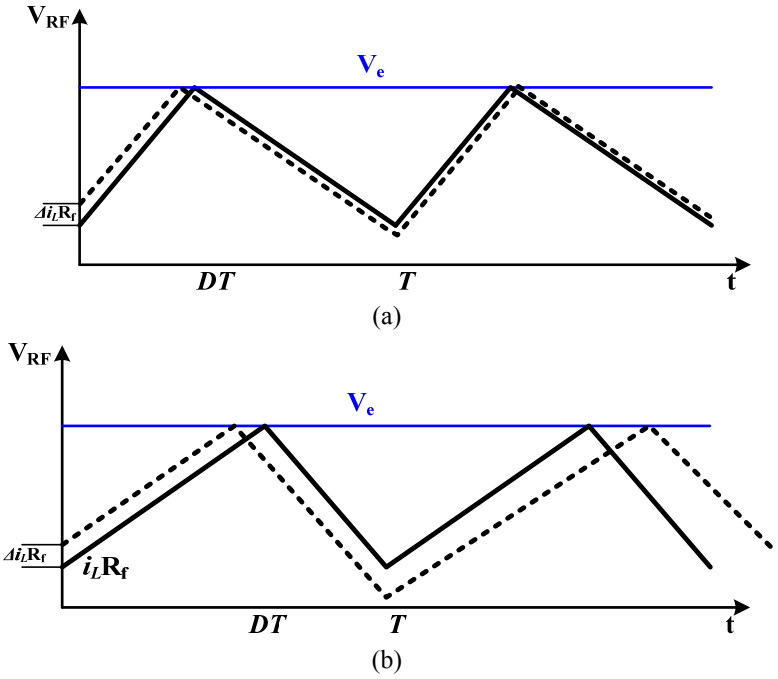


Figure 2.2.4 Effect of small disturbances with current mode control: (a) D<0.5 (b) D>0.5.

But sub-harmonic oscillation occurred in the fixed frequency current mode control working in CCM mode when the duty ratio D is larger than 0.5 [Ki-98b]. This sub-harmonic oscillation is shown in Figure 2.2.4. When D > 0.5, the small disturbance ΔI_L rapidly increases in

subsequent cycles and this indicates the instability. In Figure 2.2.4 (a), where D < 0.5, the small disturbance, $\Delta I_L R_f$, dies away along with time, t, resulting stable condition. On the other hand, In Figure 2.2.4 (b), where D > 0.5, $\Delta I_L R_f$ is continued to amplify along with time, t. This problem can be solved with extra compensation ramp signal added to the control signals [Ki-98b], as shown in Figure 2.2.5.

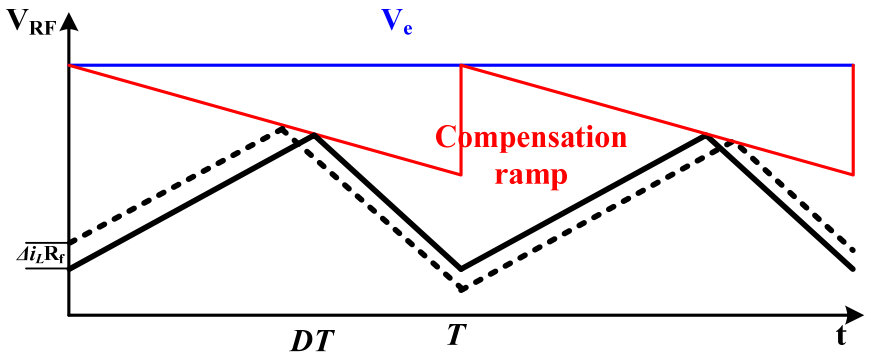


Figure 2.2.5 Extra compensation ramp is added for sub-harmonic oscillation.

2.2.3 Hysteresis Control (Band-Band Control)

Hysteretic voltage-mode control, also known as band-band control or ripple voltage control is well known for its fast response for line and load transients. Moreover, hysteretic switching converters have been shown to have unconditional stability under all operation conditions [Su-08]. Figure 2.2.6 shows the block diagram of a conventional hysteresis voltage mode control. If the output voltage V_{out} is lower than the low-voltage band V_{low}, the hysteretic comparator turns on the pMOS power switch M_p, and turns off the nMOS M_n, charging up the output capacitor C_o through the inductor L, and the output voltage V_{out} increases. When the V_{out} is higher than the higher band V_{high}, M_p will be turned off, and M_n will be turned on to make V_{out} drop into the band. If the change of the input voltage V_{in} or the load current I_{load} causes V_{out} to be outside of the band limited by V_{high} and V_{low}, the hysteretic comparator will make the gate drive

signals to charge or discharge continuously (that is, full or zero duty cycle) to steer back to within the band as quickly as possible. Thus, the output voltage V_{out} is corrected as fast as the output filter (C and L) allows and, incidentally, the converter is unconditionally stable.

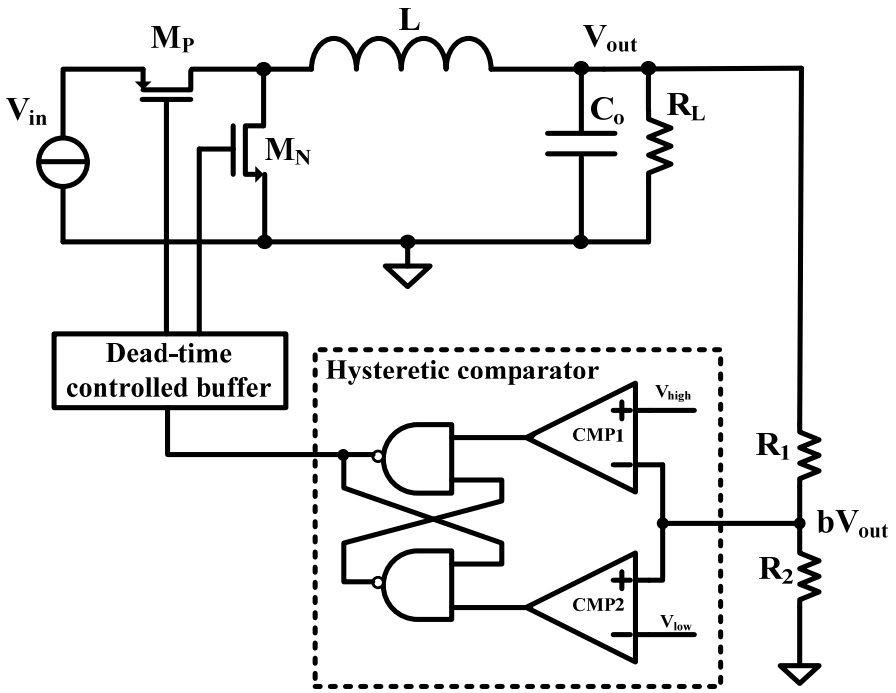


Figure 2.2.6 Block diagram of the voltage mode hysteresis controlled buck converter.

There are also some disadvantages of the voltage mode hysteresis control. As discussed above, the control signal can go 100% duty cycle and zero duty cycles, the inductor current could rise beyond the current limit of the power switches during large signal transient responses, for example, during the start-up period. Second, the switching frequency varies with all of the design parameters of the converter, such as C_o, L, R_o……

2.2.4 Analog Control and Digital Control

Digital controlled DC-DC converters enjoy growing popularity due to their low power, immunity to analog component variations, compatibility with digital systems, and faster design process. They have the potential to implement sophisticated control schemes and to accurately

match duty cycles in interleaved converters. Figure 2.2.7 gives a block diagram of a digital voltage mode control. Some salient features of the digital controlled power system are listed below:

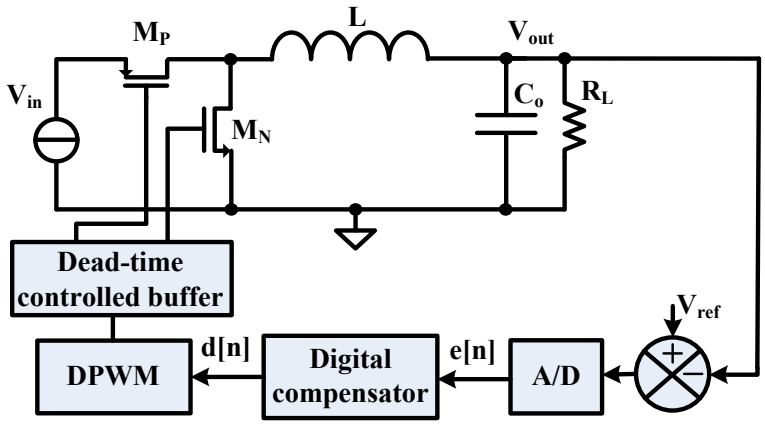


Figure 2.2.7 Block diagram of digital voltage mode control.

1. **Advanced Control Strategies:** Digital controllers enable the use of advanced control methods which can improve the converter performance in a number of ways. First, the feedback and feedforward control laws can be adaptively tuned to optimize system performance. Second, adaptive mode control can be used to maximize efficiency over a wide range of loading conditions and component tolerances. Finally, other performance-enhancing functions can be easily programmed in a digital controller.
2. **Communication with Host System:** A digital controlled power management system can facilitate communication with the digital processing system easily. This can effectively improve the power efficiency, transient performance, and fault handling.
3. **Synthesizability and Programmability:** A large portion of the digital controller circuitry is synthesizable. Existing CAD tools can be used to reduce design effort, facilitate portability to new process, and hence decrease the time-to-market.

4. **Insensitivity to Component Variation and Noise:** Analog controllers suffer from component tolerance variation and drift due to ambient conditions and aging. In a digital system, it is sensitive only at its front-end, where an analog system suffers potential problems throughout.
5. **Reduced Power and Area:** As a result of the dramatic scaling of digital technology, digital power management controllers could offer reduced power and die area in battery-powered hand-held applications.

There is also one important disadvantage of the digital voltage mode control: quantization and limit cycling, which has been studied in [Peterchev-03]. Limit cycling refers to steady-state oscillations of the output voltage V_o. It may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop. It is an undesired effect which will increase the output ripple voltage and also increase the power consumption of the controller. Obviously, steady-state limit cycling becomes very undesirable when it leads to large, unpredicted output voltage variations. Furthermore, since the limit cycle amplitude and frequency are hard to predict, it is difficult to analyze and compensate for the resulting V_{out} noise and the electro-magnetic interference (EMI) produced by the converter.

2.3 Power Reduction and Efficiency Enhancement

2.3.1 Dynamic Voltage Scaling (DVS)

As an essential part of any electronic system, power management has been identified as "**Grand Challenge**" by ITRS [ITRS-09]. Traditionally, it involves efficient energy conversion from a source (battery, solar panel, fuel cell, etc.) to well regulated voltage and current levels required by the load. Two factors, conversion efficiency and quality of regulation, have driven the evolution of power management. As illustrated in Figure 2.3.1, beginning with linear

regulators, it has resulted today in highly sophisticated, multi-mode, synchronous switching DC-DC converters, with over 90% efficiency. As power converter efficiency reaches its limit and system power dissipation keeps roaring up with complexity, research has turned towards integrated power management over the entire IC system. One most popular and effective way to achieve this is to employ the dynamic voltage scaling (**DVS**) techniques [Chang-97] [Choi-07] [Kuroda-98] [Kuroda-00] [Nguyen-03] [Usami-08] [Yan-05].

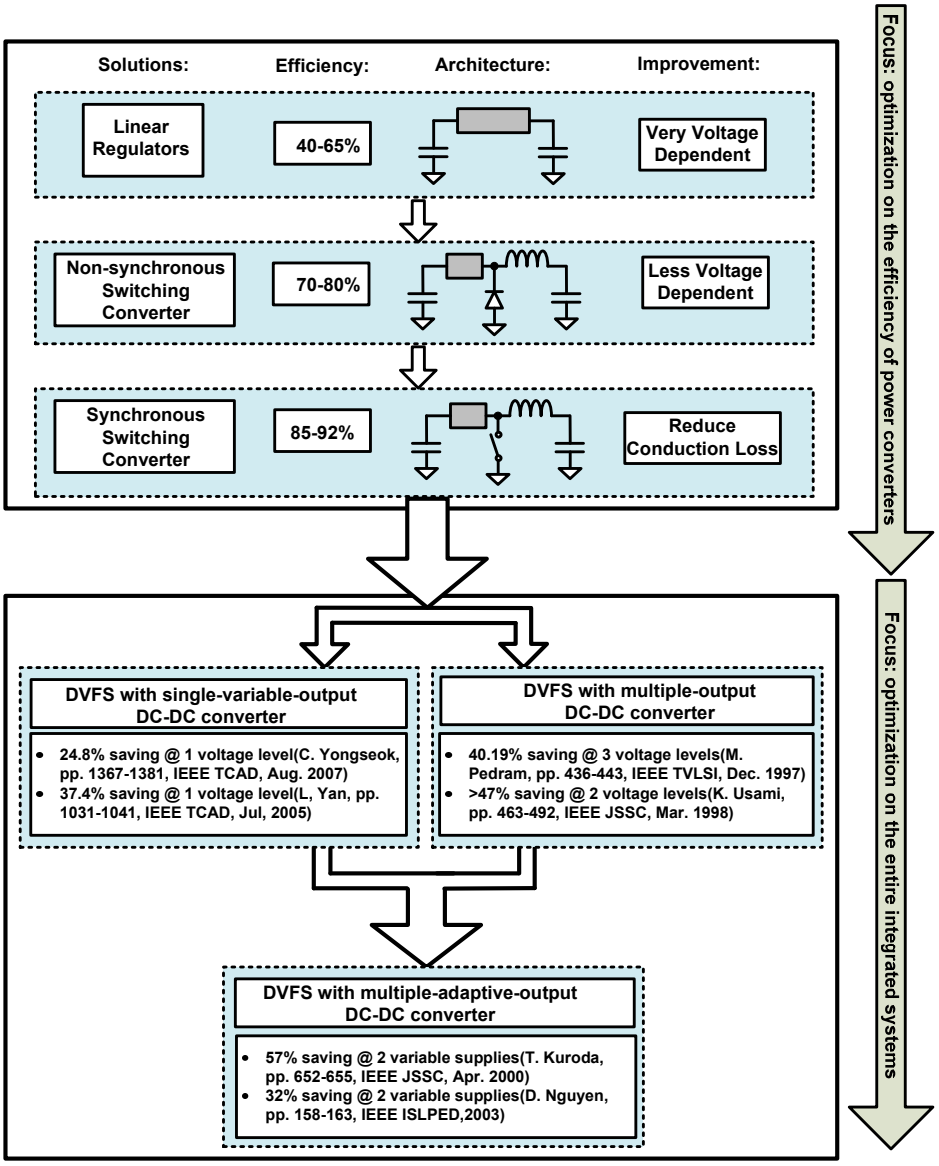


Figure 2.3.1 Evolution of power converters and power management ICs.

For examples, with a variable power supply, power dissipation could be reduced by 24.8% in an embedded CPU system [Choi-07] and by 37.4% in a distributed real-time embedded system [Yan-05]. With 3 discrete supply levels, 40.19% power was saved in pipelined data paths [Chang-97]. More than 47% power saving was obtained in a media processor powered with two voltage levels [Usami-08]. The most significant results were obtained when the power supplies offered multiple-and-variable voltage levels, which provide the largest control freedom to DVS. 57% and 32% of power savings were reported in a MPEG04 Codec chip [Kuroda-98] and ISCAS85 benchmark circuits [Nguyen-03], respectively. However, although these system-level techniques can reduce power significantly, they require fine-grained, advanced, sophisticated power management architectures and controls, most of which, unfortunately, are not commercially available.

2.3.2 Multiple Output Power Converters

Meanwhile, in a portable device, such as cell phone, MP3 player, PDA, or Laptop, some different DC supply voltage levels suitable for different components are included. In modern electrical and electronic technology, voltage scheduling with multiple supply voltage V_{DD} optimization draw great interests, because multiple V_{DD} optimization is the single most effective way to reduce power consumption of circuits, especially digital circuit. Figure 2.3.3a shows a multiple supply voltage system needs multiple DC-DC converters. And in the most recent technology of Organic Light-Emitting Diode (OLED) display, Active-Matrix (AM) OLED panels need a different sophisticated voltage supply for each color (Red, Green, or Blue) to optimize display efficiency and display quality with brightness, contrast, and vividness. All of the above-mentioned typical needs from real applications pose a challenge to DC-DC switching

converter designers: from a single input power supply, usually a battery, several outputs with different voltage levels are regulated, as shown in Figure 2.3.3b.

Before the 1900s, a very first implementation was to use a separate DC-DC converter for each output. This is a straightforward and timesaving method with many available commercial chips. On the other hand, it causes too many bulky power devices as inductors, capacitors, and control ICs. Hence, the cost for implementation of one and mass-production is apparently expensive.

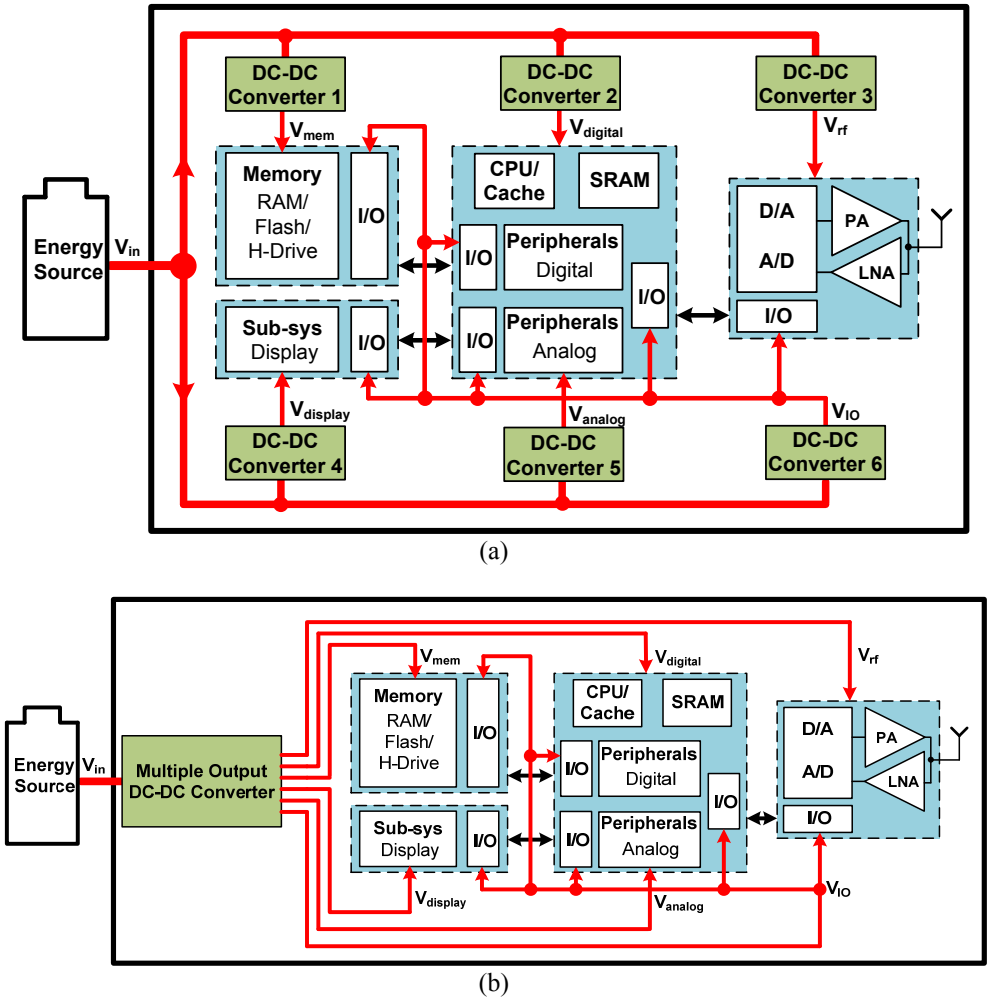


Figure 2.3.2 A VLSI system that has six supply voltage levels: (a) needs six DC-DC converters, and (b) needs one six-output DC-DC converter.

To overcome the problems, from the 1900s until now, many designers have developed their researches on Multiple-Output ICs, where there is only one control IC to control several outputs. This approach can reduce remarkably the Printed Circuit Board (PCB) areas, and from that, reduce the implementation cost. However, DC-DC converters of this type still require one energy-storage component, usually an inductor, for each output. That results in costs of PCB place for inductors and of inductors themselves. That is not to mention the control ICs are not fully optimized, such as the number of integrated power switches.

It is, therefore, desirable to develop compact DC-DC converters that are possible for Multiple-Output, small in size, with fewer IC pins, fewer off-chip inductors, and fewer on-chip power switches, while keeping EMI and cross couplings due to the reduction of magnetic components at an acceptable level. Single Inductor Multiple Output (SIMO) DC-DC converter shows up as a most suitable and cost-effective solution.

2.3.3 Single-Inductor Multiple-Output (SIMO) DC-DC Converter

Conventional implementation of a DC-DC converter that has N output voltages may consist of N independent converters, or employ a transformer that has N secondary windings to distribute energy into the various outputs (isolated multiple-output converter)[Erickson-01]. The first method requires too many components, including controllers and power devices, and this will increase the system cost. The second method does not allow individual outputs to be precisely controlled and has a big limitation for the applications of multiple voltage supply scaling. In addition, leakage inductance and cross coupling among windings cause a serious cross-regulation problem. Moreover, both methods require at least N inductors or windings, which may be too bulky and costly. In [Dancy-00], a multiple-output architecture was proposed

which combines the control loops of N converters into a single one. Multiple inductors are still needed and the reduction in external components is very small.

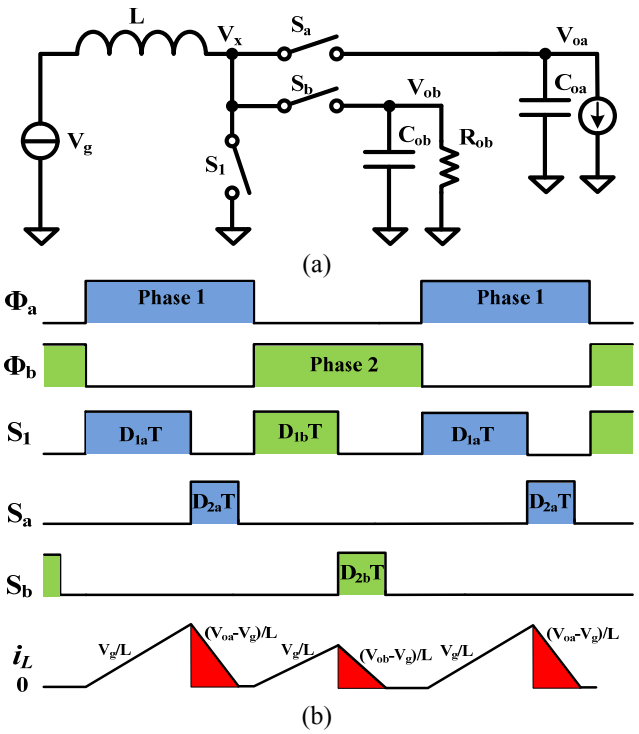


Figure 2.3.3 SIDO boost/boost converter working in DCM using time multiplexing in [Ma-03a]: (a) power stage, and (b) timing diagram.

Among existing multiple-output power supply implementations, single-inductor multiple-output (SIMO) switching converter is a very cost-effective solution. Inductors are expensive and bulky elements in switching converters. For a considerable saving in cost, weight and size, it is natural to investigate the possibility of using fewer inductors and power switches to fulfill the task without compromising the performances. The invention of SIMO switching converters nicely fit this need. With only one single inductor, it provides multiple, independently regulated outputs successfully.

To overcome the problems mentioned above, a single-inductor dual-output (SIDO) boost/boost converter was proposed in [Ma-03a] by Dr. Ma. Figure 2.3.5 shows the converter

structure and timing diagram. Only one inductor is required for providing two different output voltages. Using a novel time-multiplexing (TM) control scheme, the converter only need one controller loop to regulate all outputs. Compared with other designs, both on-chip and off-chip components are reduced significantly, while low cross-regulation is maintained at the same time.

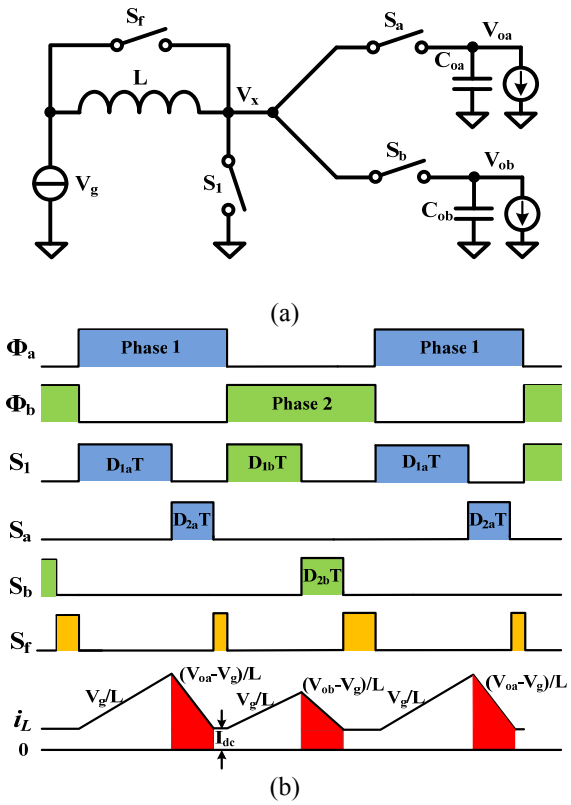


Figure 2.3.4 SIDO boost/boost converters working in PCCM using freewheel switching in [Ma-02a]: (a) power stage, and (b) timing diagram.

Traditional single-output DC-DC converters can work in DCM (discontinuous conduction mode) at light load for high efficiency, while it operates in CCM (continuous conduction mode) at heavy load to supply more power. However, this cannot be applied to a SIMO converter. With the inductor L being shared by all outputs, it is easy to cause cross regulation among the sub-converters of a SIMO converter when it goes into CCM mode. Hence, the SIDO converter in [Ma-03a] will suffer cross regulation when it goes to CCM.

The pseudo-continuous conduction mode (PCCM) is thus proposed in [Ma-02a] by Dr. Ma. As shown in Figure 2.3.6 (b), in this working mode, the floor of the inductor current is raised by a DC level of I_{dc}. Here, I_{dc} can be adjusted according to the load and current ripple requirements. When the converter is having heavy loads, I_{dc} can be increased to allow more power to be delivered to the outputs. Current ripple can be much reduced, since a larger inductor can be used in PCCM. This eliminates the power constraints in the DCM case, while retaining relatively small current ripple and voltage ripples.

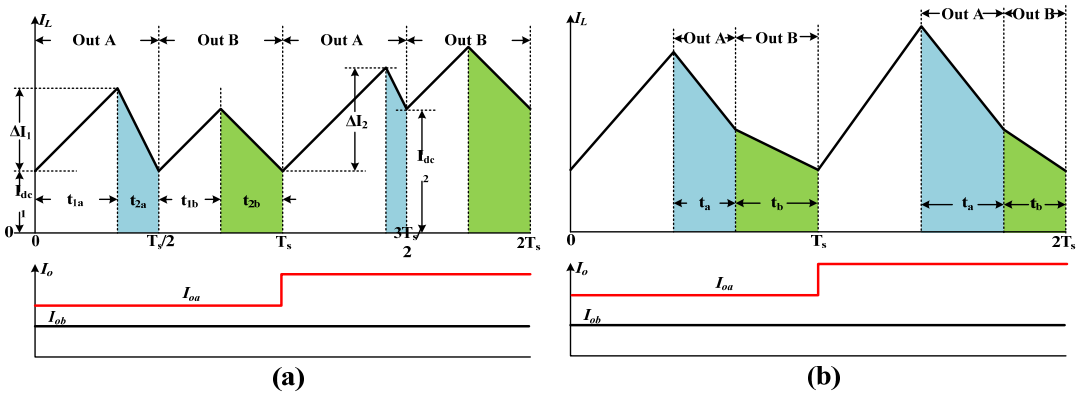


Figure 2.3.5 Cross regulation in SIMO converters.

In [H-P. Le-07], Le *et al.* present a SIMO converter architecture which employs an ordered power-distributive control (OPDC). This converter regulates four main positive boost outputs and one dependent negative output developed by a charge pump. In [Bonizzoni-07], Bonizzoni *et al.* present a SIDO buck converter, which uses PWM control and dynamically biases the power transistors to the highest voltage.

Certain severe drawbacks exist in the aforementioned designs. Cross regulation is a unique and critical stability issue in multiple-output converters, where each output should be independently regulated. If the output voltage of a sub-converter is affected by the load change of another, cross regulation occurs. In the worst case, the entire converter may become unstable

(Figure 2.3.7). The design in [H-P. Le-07] employs a control similar to that shown in Figure 2.3.7(b), where each of the five outputs is energized after a global charge of the inductor. This control undergoes severe cross regulation when one of the loads has a sudden power demand. The SIDO buck converter presented in [Bonizzoni-07] uses a PWM control strategy, where the error voltage from the first output is used to determine the total energy to be delivered. The error voltage corresponding to the second output is then used to appropriately allocate this energy. Such a control scheme will also undergo severe cross regulation, as a large dynamic change in one output will affect the energy delivered to the other.

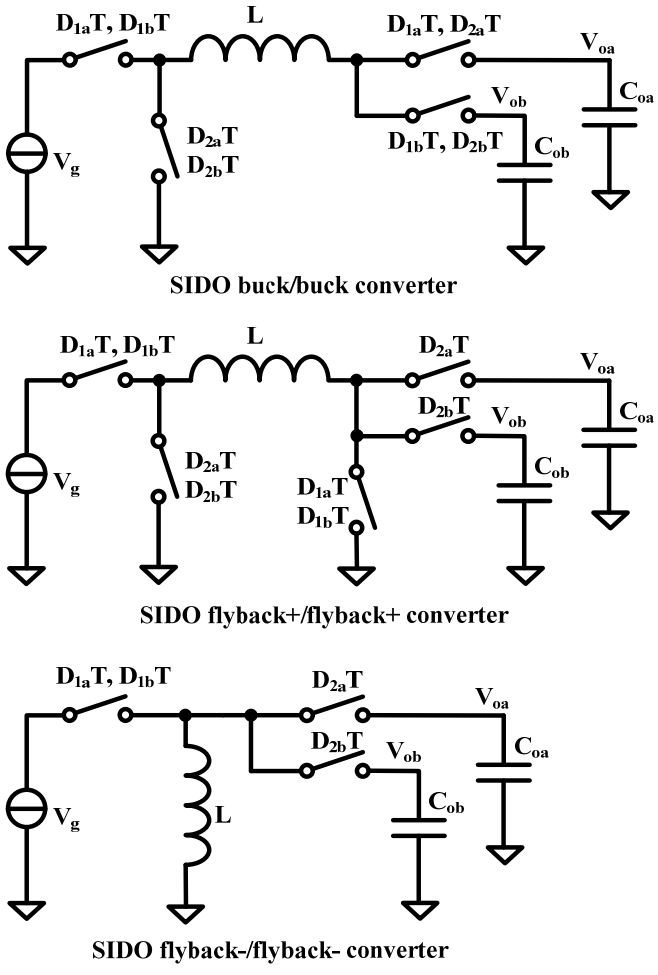


Figure 2.3.6 Architecture extensions on SIDO switching converters: SIDO same-type converter.

In fact, the extension on the proposed SIDO converters is very flexible and it can be applied for all kinds of DC-DC conversions [Ki-01]. In Figure 2.3.8, Figure 2.3.9, and Figure 2.3.10, we demonstrate this idea with dual-output implementations (SIDO). Based on the conversion manner, the SIMO converters can be classified into three groups. Figure 2.3.8 shows the SIMO same-type converters, which achieving the same type of DC-DC conversion at each output. We label the SIMO converters that have positive and negative outputs as SIMO bipolar converters, shown in Figure 2.3.9. For those achieving different type DC-DC conversions with the same polarity, we name them as SIMO mixed-type converters, as shown in Figure 2.3.10.

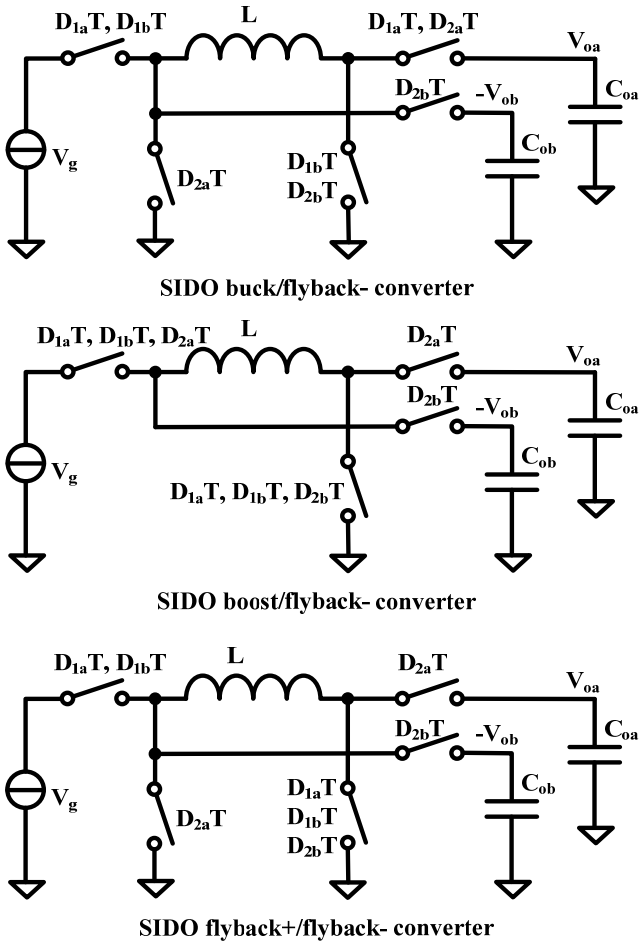


Figure 2.3.7 Architecture extensions on SIDO switching converters: SIDO bipolar converter.

It is obvious that the SIMO converters can be extended to give N+M outputs in general. Table 2.1 summarizes the topology features of all second-order SIMO converters with N+M outputs. Compared with conventional designs, bulky magnetic components are minimized to be one, The number of power devices is also reduced, which will be more significant as the number of output increases.

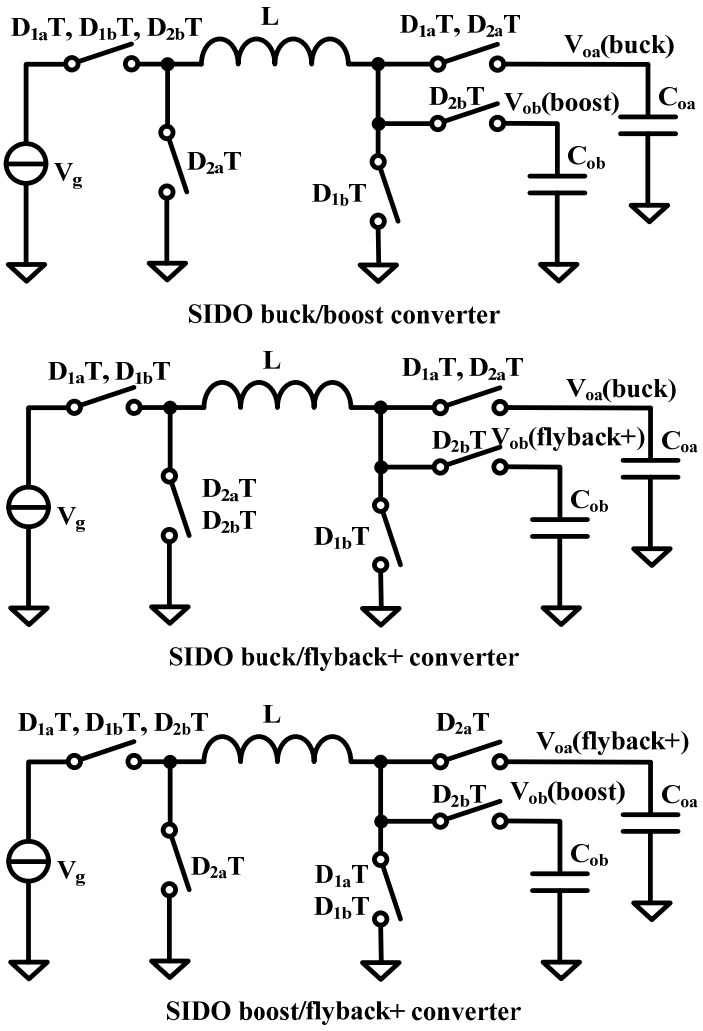


Figure 2.3.8 Architecture extensions on SIDO switching converters: SIDO mixed-type converter.

Table 2.1 SIMO converters with N+M outputs

Type	Name	Type of outputs	Number of inductors	Number of power devices
Conventional designs		positive or/and negative	N+M	≥ 2N+2M(4N+2M for N flyback+ outputs)
SIMO single-type converters	Buck	positive	1	N+M+2
	Boost	positive	1	N+M+1
	Flyback	negative	1	N+M+1
	Flyback+	positive	1	N+M+3
SIMO bipolar converters	Buck(N)/flyback(M)	bipolar	1	N+M+3
	Boost(N)/flyback(M)	bipolar	1	N+M+2
	Flyback+(N)/flyback(M)	bipolar	1	N+M+3
SIMO mixed-type converters	Buck(N)/boost(M)	positive	1	N+M+3
	Buck(N)/flyback+(M)	positive	1	N+M+3
	Boost(N)/flyback+(M)	positive	1	N+M+3

CHAPTER 3 AN INTEGRATED SWITCHING DC-DC CONVERTER WITH DUAL-MODE PULSE-TRAIN/PWM CONTROL

This chapter presents an integrated switching buck converter with a dual-mode control scheme. A pulse-train (PT) control, employing a combination of four different pulse control patterns, is proposed to achieve optimal regulation performance under various operation scenarios. Meanwhile, a high-frequency pulse-width modulation (PWM) control is adopted to ensure low output ripples and avoid digital limit cycling in the steady state. The converter was designed and fabricated with a 0.35-μm digital CMOS N-well process. The entire die area, including on-chip pads and power devices, is 1.31 mm2. Experimental results show that, in the steady state, the output voltage is well regulated at 1.5 V with ±12.5-mV ripples in the PWM mode, with a nominal input supply voltage of 3.3 V. The measured maximum efficiency is 91%, and the efficiency stays above 70% within a 500-mW power range. In transient measurements, with a 100% load step change from 50 mA to 100 mA, the output voltage of the converter settles within 345 ns due to the fast response of the PT control, with a maximum voltage variation of 164 mV. The converter functions well when the input supply voltage frequently varies between 2.2 V and 3.3 V, with a line regulation of 29.1 mV/V.

3.1 Review of Prior Arts

Advances on high-performance VLSI systems impose new challenges on power supply designs. Such a supply is expected to have fast transient response to frequent load changes due to the nature of multi-mode system operations [Ma-04] [Song-07]. Meanwhile, it should maintain low ripple voltage for clean power delivery.

Switching power converter is considered as the best candidate to implement such power supplies due to its high efficiency and voltage conversion flexibility. However, for conventional pulse-width modulation (PWM) switching converters, there are certain drawbacks for these new applications. In a voltage-programming PWM converter, due to the existence of the low-frequency complex poles in the loop gain transfer function, it is very difficult to design the compensation network for a wide loop-gain bandwidth [Ki-98a]. In a current-programming PWM converter, although there are two separated real poles in the loop-gain transfer function, special current sensing circuit is required and ramp compensation has to be adopted to avoid sub-harmonic oscillation [Ki-98b]. A pulse-frequency modulation (PFM) is usually helpful to the efficiency at light load. However, its random switching noise spectrum is hard to predict, increasing design difficulty in communication and other noise-sensitive devices. It would be very desirable if a new control scheme can be proposed to overcome all the aforementioned drawbacks in the prior arts.

To improve the transient performance, a new digital control technique named pulse-train (PT) control was introduced in [Ferdowsi-05]. As illustrated in Figure 3.1.1, the converter is regulated with two different types of digital pulses – power pulse and sense pulse. When the output voltage V_o is higher than the reference voltage V_{ref}, low-power "sense pulses" are used such that less power will be delivered to V_o. On the other hand, when V_o is lower than V_{ref}, high

power “power pulses” are employed and more power is delivered to V_o. However, a closer look at the control scheme reveals the following concerns: if the power pulses are chosen very long, severe over-damping behaviors would occur at V_o. Meanwhile, if the sense pulses are chosen too short, it may cause under-damping behaviors. Even in the steady state, the large quantization errors cause very noisy ripples at V_o. In either case, a single power/sense pulse pattern can hardly optimize the converter in both steady-state and dynamic transient operations.

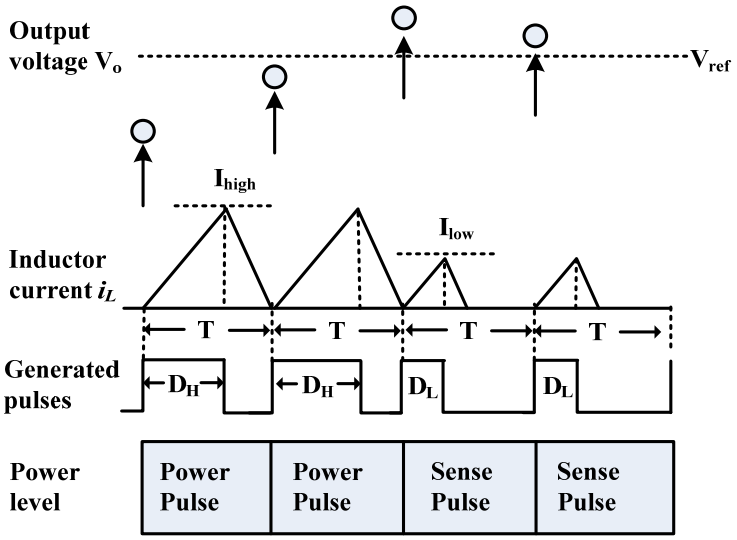


Figure 3.1.1 Pulse-train control scheme in [Ferdowsi].

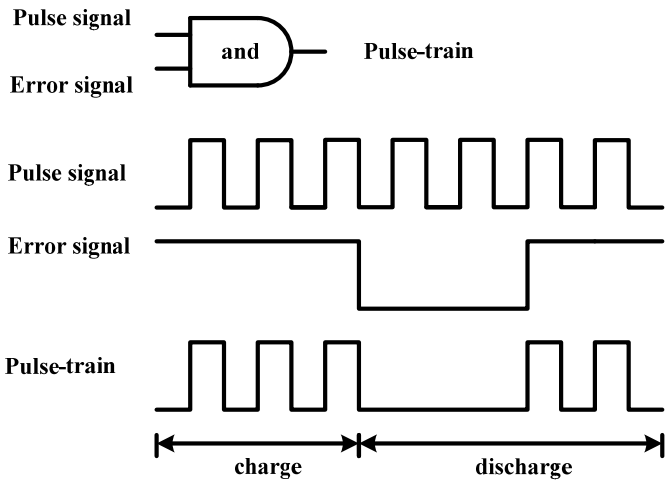


Figure 3.1.2 The PT control scheme proposed in [Zhang-04].

Even earlier, a similar pulse control technique was purposed by one of our authors in [Zhang-04], as shown in Figure 3.1.2. In the paper, a converter's duty ratio signal was modulated by high-frequency pulses, instead of a constant control voltage. The high-frequency switching actions improve the damping performance, but the uniform pulse pattern does not suffice to all the complex transient operations. In addition, since no inductor current is considered in the control loop, load transient response is relatively slow.

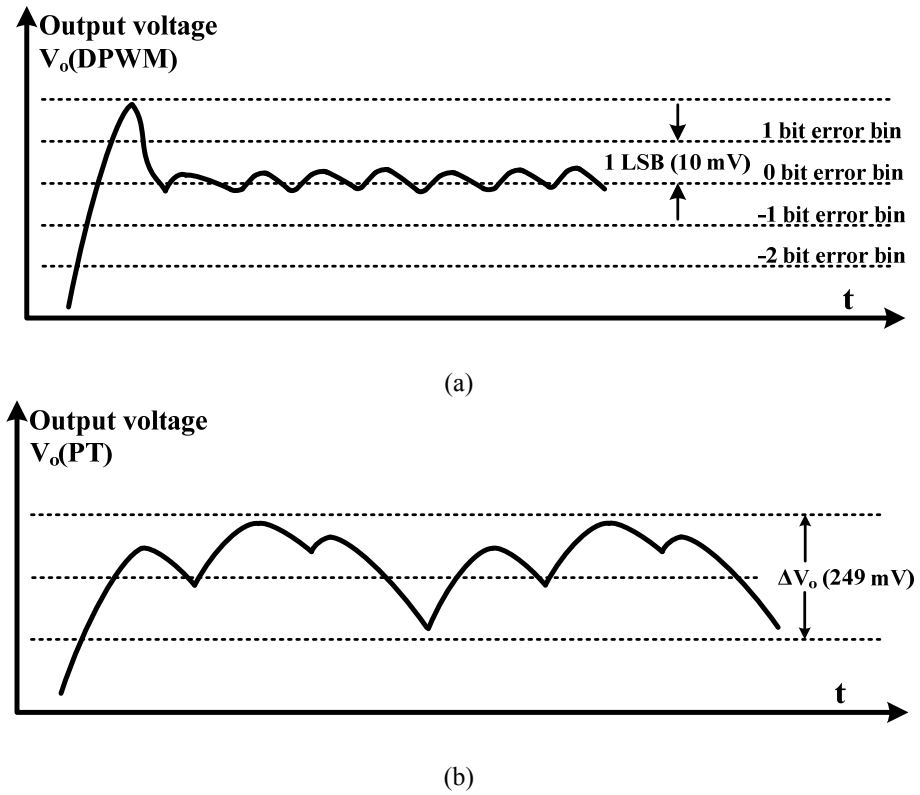


Figure 3.1.3 Limit cycle problems at the output voltage of V_o in (a) a DPWM switching converter [Peterchev-03], and (b) a PT switching converter [Ferdowsi-05].

In addition, both of the above designs suffer from limit cycle problem due to the nature of digital control [Peterchev-03]. Limit cycles refer to steady-state oscillations of the output voltage V_o. It may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop. For a PT control based converter, the amplitude of quantizers has to be big enough such that each pulse could carry sufficient amount of power to the output V_o

(even for the sense pulse in [Ferdowsi-05]. Hence, the PT controls usually face much more severe limit cycling (Figure 3.1.3(b)) than the traditional DPWM controls (Figure 3.1.3(a)). For examples, a DPWM converter can regulate the output V_o within a tolerance of 1 LSB of a 11-bit ADC, leading to 10 mV quantization error [Intel-02]. However, with 1 power pulse and 1 sense pulse pattern, a PT control converter has a ripple voltage of 249 mV [Ferdowsi-05]! Even when multiple power and sense pulses are introduced, due to the tradeoff between quantization error and transient speed, the ripple voltage cannot be improved (Figure 3.1.4).

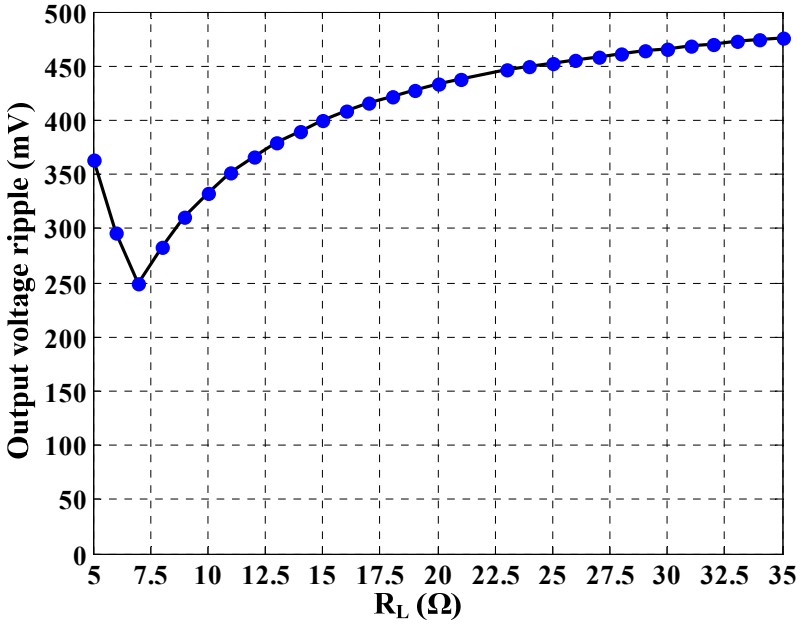


Figure 3.1. 4 Optimal output ripple voltage versus load resistance, with multiple power and sense pulse options in [Ferdowsi-05].

Obviously, steady-state limit cycling becomes very undesirable when it leads to large, unpredicted output voltage variations. Furthermore, since the limit cycle amplitude and frequency are hard to predict, it is difficult to analyze and compensate for the resulting V_{out} noise and the electro-magnetic interference (EMI) produced by the converter.

3.2 The Proposed Dual-Mode PT/PWM Control

3.2.1 Control Scheme

Figure 3.2.1 illustrates the operation of the proposed dual-mode PT/PWM control scheme. In this design, the modes of operation are highly determined by the output voltage V_o of the converter. The entire output voltage range is divided into five operation zones. **A, B, C, D** and **E** represent typical operation points in the five zones, respectively. Accordingly, four different reference voltage levels $V_{ref\_[i]}$ (i=1, 2, 3, 4) are defined for the zones.

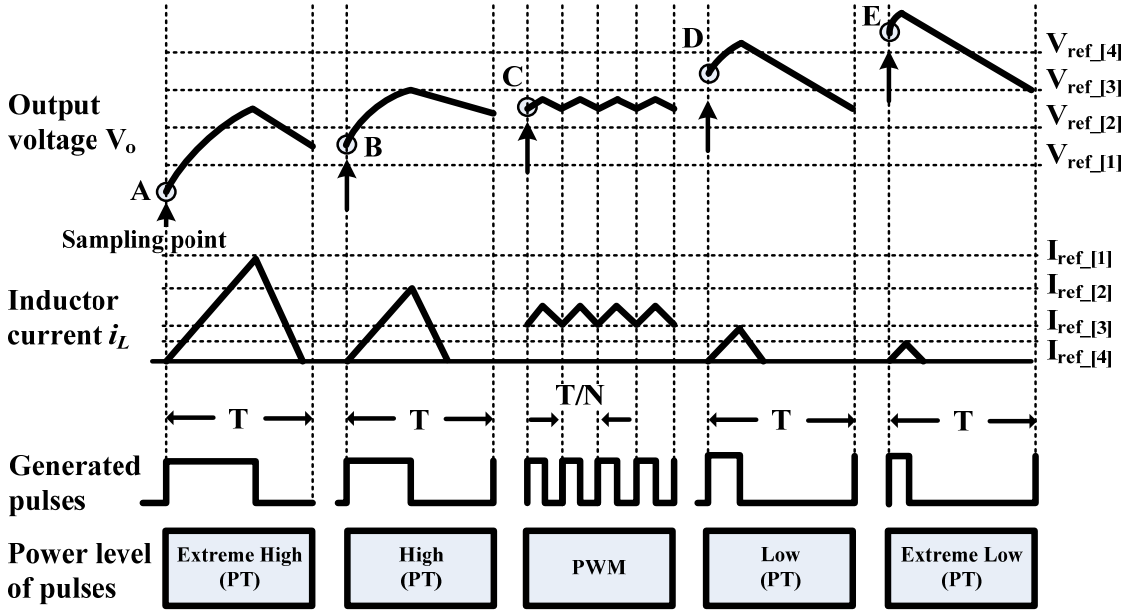


Figure 3.2.1 The proposed dual-mode PT/PWM control scheme.

At the point of **A**, the output voltage V_o is much lower than the desired regulation level $V_{ref\_[1]}$. This represents a deep power-hungry operation scenario. Hence, a large amount of power is needed to charge up the capacitor at V_o immediately. The controller assigns a large-duration pulse to provide sufficient inductor current for charging, which also defines the duty ratio of the converter. The power carried by this pulse is categorized as “Extreme High”.

At the point of **B**, the output voltage V_o is still considered as "low", but is much closer to the desired level than A, where the inequality $V_{ref\_[1]}<V_o<V_{ref\_[2]}$ holds. To avoid overshooting, a shorter duration "High" power pulse is employed to charge up the capacitor at V_o moderately.

At the point of **C**, the output voltage V_o is in a relatively accurate regulation range, with a valid inequality of $V_{ref\_[2]}<V_o<V_{ref\_[3]}$. An analog PWM control takes over the control. Because the PWM control can adjust the duty ratio continuously, different from the PT control, it enjoys infinite regulation resolution. To further reduce the ripple voltage, we operate the converter in continuous -conduction mode (CCM), at a much higher switching frequency (N/T) than the PT control scenarios. Here, 1/T represents the switching frequency of the converter in the PT control mode.

At the point of **D**, the output voltage V_o is too high to be in the PWM regulation zone, with $V_{ref\_[3]}<V_o<V_{ref\_[4]}$. The PT control takes in charge and a "Low" power pulse is assigned. Because the equivalent duty ratio is lower than the PWM one, it causes V_o to drop.

If V_o is much higher than the desired level $V_{ref\_[4]}$ (at the point of **E**), an "Extreme Low" power pulse will be employed with an even smaller duty ratio than that at **D**, which allows V_o to drop even faster. The difference between the scenarios of **D** and **E** is that the power level of the assigned pulse in **D** is higher than the one in E to avoid over-discharging at V_o.

It should be noted that the four patterns of the PT control all operate at a fixed frequency of 1/T or its multiples. This ensures the converter to maintain a discrete and predictable noise spectrum.

3.2.2 System Stability

A. System Stability in PT Mode

In the PT mode, the proposed converter operates in discontinuous conduction mode (DCM). Within one switching period between nT and (n+1) T, the energy difference is equal to

$$\Delta E_{in} = \Delta E_L + \Delta E_{CL} + \Delta E_{RL}, \tag{3.1}$$

where ΔE_{in} is the amount of energy change from the power supply, ΔE_L, ΔE_{CL} and ΔE_{RL} are the energy changes of the inductor L, the output capacitor C_L and the load R_L, respectively.

Because the converter stays in DCM mode, ΔE_L is equal to zero since the inductor L de-energizes at the end of each switching period. Meanwhile, ΔE_{RL} can be computed as

$$\Delta E_{RL} = \frac{1}{R_L} \cdot \int_{nT}^{(n+1)T} V_o^{\,2} dt \approx \frac{T}{2R_L}(V_{o,(n+1)T}^2 + V_{o,nT}^2). \tag{3.2}$$

Moreover, the energy stored in a capacitor at the end of each switching period can be written as

$$E_{CL,(n+1)T} = \frac{1}{2} C_L V_{o,(n+1)T}^2, \qquad E_{CL,nT} = \frac{1}{2} C_L V_{o,nT}^2. \tag{3.3}$$

By combining (3.2) and (3.3), we have

$$\Delta E_{RL} \approx \frac{T}{R_L C_L}(E_{CL,(n+1)T} + E_{CL,nT}). \tag{3.4}$$

From (3.2) and (3.4), the energy stored at the output capacitor at the end of each switching period can be calculated as

$$E_{CL,(n+1)T} = \left(\frac{T}{R_L C_L} + 1\right)^{-1} \cdot \Delta E_{in} + M \cdot E_{CL,nT}, \tag{3.5}$$

where

$$M = \left(1 - \frac{T}{R_L C_L}\right) \Big/ \left(1 + \frac{T}{R_L C_L}\right) < 1. \tag{3.6}$$

In (3.5), M is positive because the switching period of the converter is usually much shorter than the time constant determined by the product of R_L and C_L. Because M is always less

than 1, the converter is stable under any pattern of high- or low-power pulses in the proposed closed-loop system.

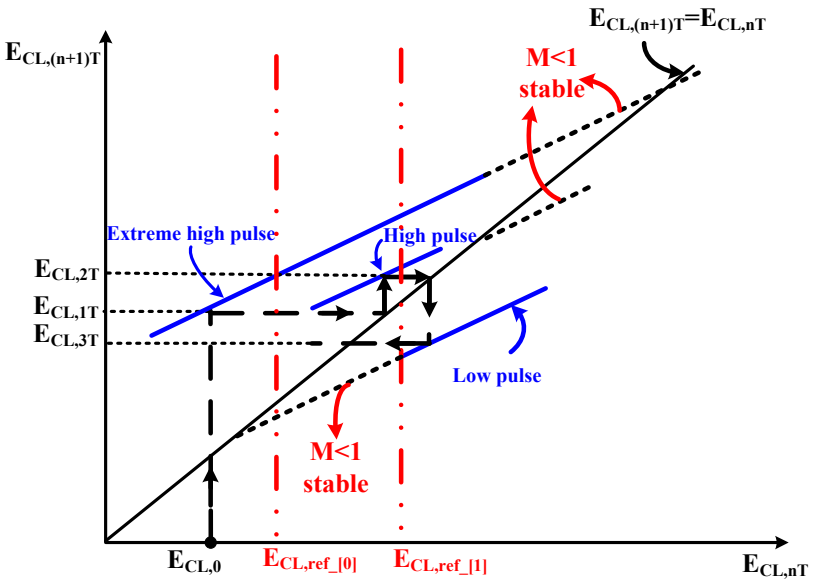


Figure 3.2.2 Sequential flow of the PT pulse control.

Based on (3.5) and the control inequalities, the time evolution of the sequence of the PT control in a closed-loop system is illustrated in Figure 3.2.2. In this figure, for example, based on the initial value of the output voltage V_o, an "Extreme high" pulse is generated first. As V_o rises up, a "High" pulse is then assigned, followed by a "Low" pulse when V_o is higher than the desired level. Because M is smaller than 1, the system is stabilized around the desired voltage level. Analog PWM control then takes into effect to achieve fine voltage regulation.

B. System Stability in PWM Mode

In PWM mode, the flow diagram of the closed-loop buck regulator can be derived by applying the generalized control law to the linearized power circuit. This control law determines how transfer function T(s), the Laplace transformed control variable, varies as a function of key

circuit parameters. For a second-order system, such as the buck converter with one input voltage, it can be expressed as:

$$T(s) = -F_1(s)i_L(s) - F_2(s)V_o(s) + Q_1(s)V_{in}(s)\,. \tag{3.7}$$

That is, the inductor current variable, the output voltage variable, and the input voltage variable, can each individually contribute to the system control variable. For a voltage mode PWM controlled buck converter [Ki-98a], there is no current feedback, i.e. $F_1(s) = 0$. There is also no feedforward control in this design, $Q_1(s) = 0$ too. And finally, note that in this case, $F_2(s)$ includes the reference and feedback summing components. This generalized control law can then be made specific to our voltage-mode controlled buck regulator, where the feedback summing point is the differential input to the error Amplifier. With the state-space averaging method, the transfer function T(s) is:

$$T(s) = A(s)\cdot H(s) = A(s)b\frac{1}{D}\frac{V_o}{V_m}\cdot\frac{1+\dfrac{s}{\omega_z}}{1+\dfrac{1}{Q}\dfrac{s}{\omega_o}+\left(\dfrac{s}{\omega_o}\right)^2}, \tag{3.8}$$

where A(s) is the gain of the error amplifier, which consists of the op-amp and the compensation network which consists of the op-amp and the compensation network, H(s) is the control-to-output transfer function, b is the scaling factor; V_m is the peak-to-peak voltage of the ramp signal. And

$$\omega_z = \frac{1}{C_L R_{ESR}}, \omega_o = \frac{1}{\sqrt{LC_L}}, Q = R_L\sqrt{\frac{C_L}{L}}\,. \tag{3.9}$$

The strategy of compensation is to ensure that the converter would be stable for all possible load changes. By using the pole-zero compensation network shown in Figure 3.2.3, the corresponding transfer function, assuming an infinity gain of the op-amp, is

$$A(s) = \frac{1 + sR_2C_2}{s(C_1 + C_2)R_1[1 + s(C_1 \parallel C_2)R_2]} = \frac{1 + \dfrac{s}{2\pi f_{z\_ea}}}{s(C_1 + C_2)R_1(1 + \dfrac{s}{2\pi f_{p\_ea}})}, \tag{3.10}$$

which has a first pole at origin, a zero at $-1/R_2C_2$, and a second pole at $-1/R_2(C_1||C_2)$. The zero is at a lower frequency in magnitude than the second pole.

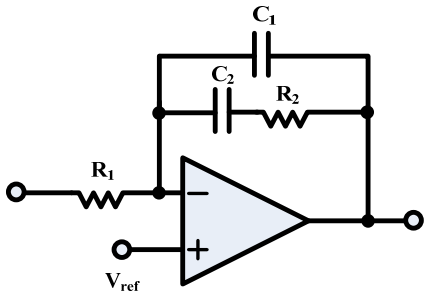


Figure 3.2.3 Error amplifier with pole-zero compensation.

The control-to-output transfer function H(s) changes as R_L changes, and combines with A(s) to give the overall loop gain T(s). To ensure stability in the worst case, the zero f_{z_ea} introduced by C_2 and R_2 is placed at the complex pole in (3.8). The high-frequency pole f_{p_ea} of the compensation network caused by C_1, C_2 and R_2 is placed at the frequency of the zero $f_z=\omega_z/2\pi$ in the control-to-output response curve caused by the ESR of the output filtering capacitor. Hence, the values of the components are given by

$$C_1 = \frac{1}{2\pi f_{z\_ea} R_2}, \tag{3.11}$$

$$C_2 = \frac{1}{2\pi f_{xo} R_2}, \tag{3.12}$$

$$R_2 = A_{xo} R_1. \tag{3.13}$$

where A_{xo} is the gain of the compensation network at the crossover frequency of the loop gain, and f_{xo} is the crossover frequency which is related to the bandwidth of the converter.

3.2.3 Output Ripple Voltage in PT Mode

A. Output Ripple Voltage in PT Mode

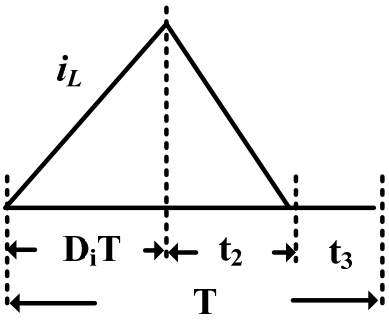


Figure 3.2.4 One switching period in PT mode.

Output ripple voltage can be analyzed using the circuit differential equations. Figure 3.2.4 depicts one switching period in PT mode, and the converter is working at DCM mode. During the intervals t_2 and t_3, the output filtering capacitor discharges through the load and the output voltage decreases. Assuming that the output voltage is at its desired level $V_o=V_{ref\_[i]}$, the change of the output voltage can be written as:

$$\Delta V_{CL(-)} \cong -\frac{V_{ref\_[i]}}{R_L C_L}(t_2+t_3) = -\frac{V_{ref\_[i]}}{R_L C_L}(1-D_i)T\,. \tag{3.14}$$

During interval D_iT, the output filtering capacitor charges through the inductor, hence the output voltage increases. Assuming that the inductor current increase linearly and the output voltage variation is small, the increase of the output voltage during on time D_iT can be obtained solving the differential equations and is equal to

$$\Delta V_{CL(+)} \cong A\left(e^{-\frac{D_iT}{R_L C_L}}-1\right)-\frac{R_L}{L}(V_{in}-V_{ref\_[i]})D_iT\,, \tag{3.15}$$

where

$$A = \frac{V_{ref\_[i]}}{R_L C_L} + \frac{D_i T}{2LC_L}(V_{in} - V_{ref\_[i]}). \tag{3.16}$$

The total changes of the output voltage in PT mode is the summation of the above two extracted values and can be estimated as

$$\begin{aligned}\Delta V_{CL} \cong \Delta V_{CL(-)} + \Delta V_{CL(+)} &= \left(\frac{V_{ref\_[i]}}{R_L C_L} + \frac{D_i T}{2LC_L}(V_{in} - V_{ref\_[i]})\right) e^{\frac{D_i T}{R_L C_L}} \\ &+ V_{ref\_[i]}\left(\frac{R_L}{L} + \frac{1}{2LC_L} + \frac{1}{R_L C_L} - \frac{2}{R_L C_L D_i T}\right) D_i T - \left(\frac{R_L}{L} + \frac{D_i T}{2LC_L}\right) V_{in}\end{aligned} \tag{3.17}$$

(3.17) depicts how different circuit parameters involve in the generation of output ripple voltage ripple in PT mode.

B. Output Ripple Voltage in PWM Mode

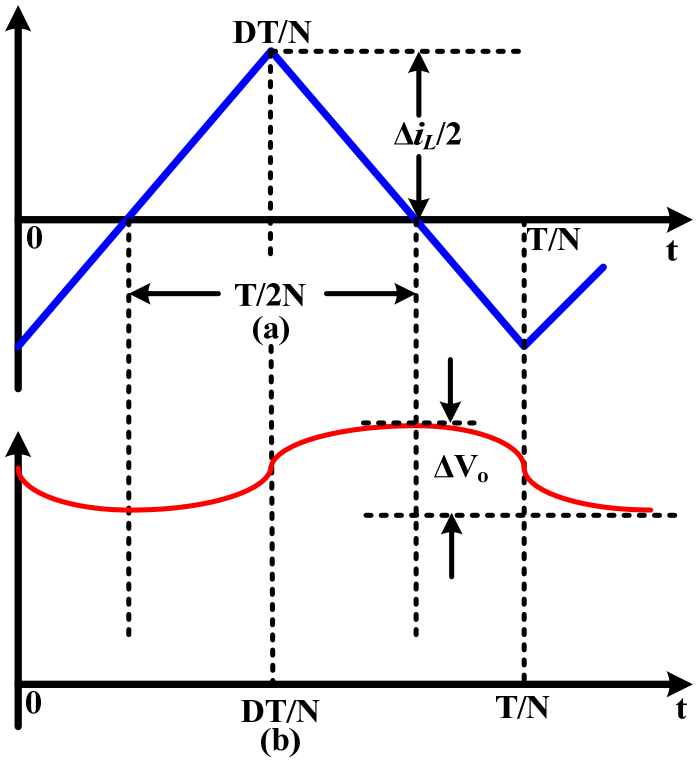


Figure 3.2.5 (a) Output capacitor current i_{CL}, and (b) output ripple voltage ΔV_o.

Output ripple voltage in PWM mode can be calculated using output filtering capacitor current. Figure 3.2.5 shows the output filtering capacitor current i_{CL} and output voltage ripple ΔV_o in one switching period. As we can see, i_{CL} is given by

$$i_{CL} = i_L - i_{RL}, \tag{3.18}$$

where i_{RL} is the current flow into output load. When i_{CL} is positive, the output capacitor is charging, since the charge is defined as $Q=C_L V_o$, we can define the output ripple voltage ΔV_o as

$$\Delta V_o = \frac{\Delta Q}{C_L}, \tag{3.19}$$

Where ΔQ is the area of the triangle above the time axis as shown in Figure 3.2.5(a). From Figure 3.2.5(a), we can get

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2N} \cdot \left(\frac{\Delta i_L}{2} \right) = \frac{\Delta i_L}{8Nf_s}, \tag{3.20}$$

where N is ratio of the switching frequency in PWM mode and in PT mode. f_s is the switching frequency in PT mode. The peak-to-peak inductor current ripple Δi_L of a buck converter is given in [Erickson] as

$$\Delta i_L = \frac{V_o (1-D) T}{NL}, \tag{3.21}$$

D is the duty ratio in PWM mode. And the output ripple can be calculated as

$$\Delta V_o = \frac{\Delta Q}{C_L} = \frac{\Delta i_L}{8Nf_s C_L} = \frac{V_o (1-D)}{8LC_L (Nf_s)^2}. \tag{3.22}$$

If the ESR (Equivalent Series Resistor) of the output capacitor is also considered, (14) can be modified as

$$\Delta V_o = \frac{\Delta i_L}{C_L} \cdot \sqrt{\left(\frac{1}{8Nf_s} \right)^2 + (ESR \cdot C_L)^2} = \frac{V_o (1-D)}{LC_L Nf_s} \sqrt{\left(\frac{1}{8Nf_s} \right)^2 + (ESR \cdot C_L)^2}. \tag{3.23}$$

Compare with PT mode, the ripple voltage in PWM mode becomes much smaller due to the accurate duty ratio and an assigned much faster switching frequency.

3.3 System Design & Circuit Implementations

3.3.1 Closed-Loop System Architecture

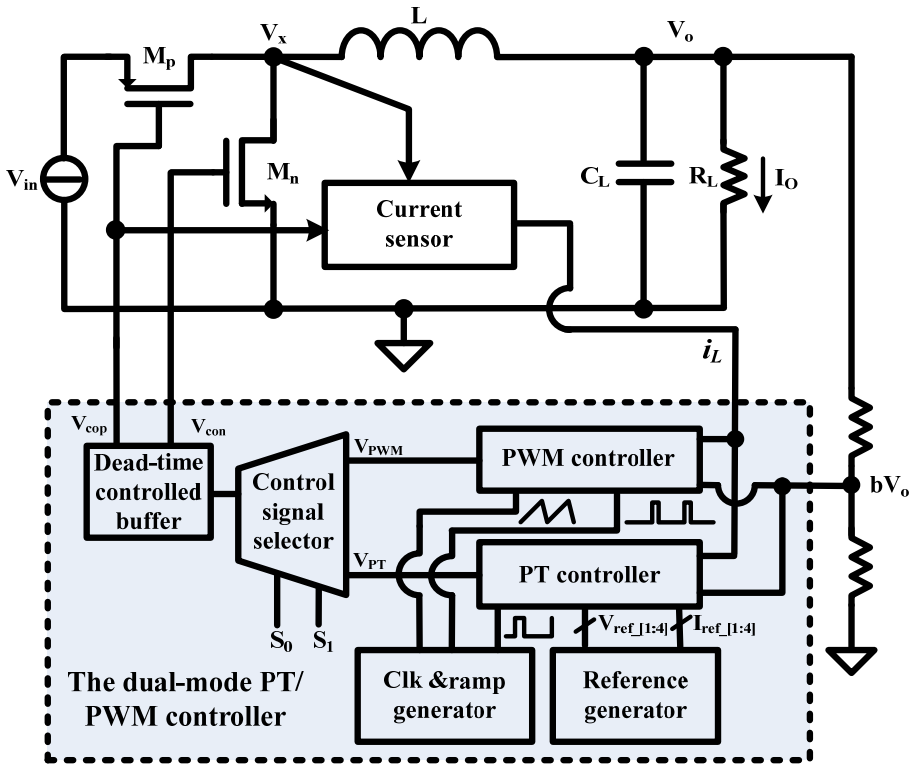


Figure 3.3.1 Block diagram of the proposed converter.

Figure 3.3.1 shows the entire system block diagram of the proposed converter. The design enjoys the flexibility of operating in either the high-frequency PWM mode or the PT mode, which is adaptable to load dynamics. In the PWM mode, the error amplifier generates a duty ratio at higher switching frequency for low ripple voltages. In the PT mode, based on the load power demand and real-time V_o, an optimal power-train pattern will be assigned for prompt and smooth dynamics.

3.3.2 The PT Controller

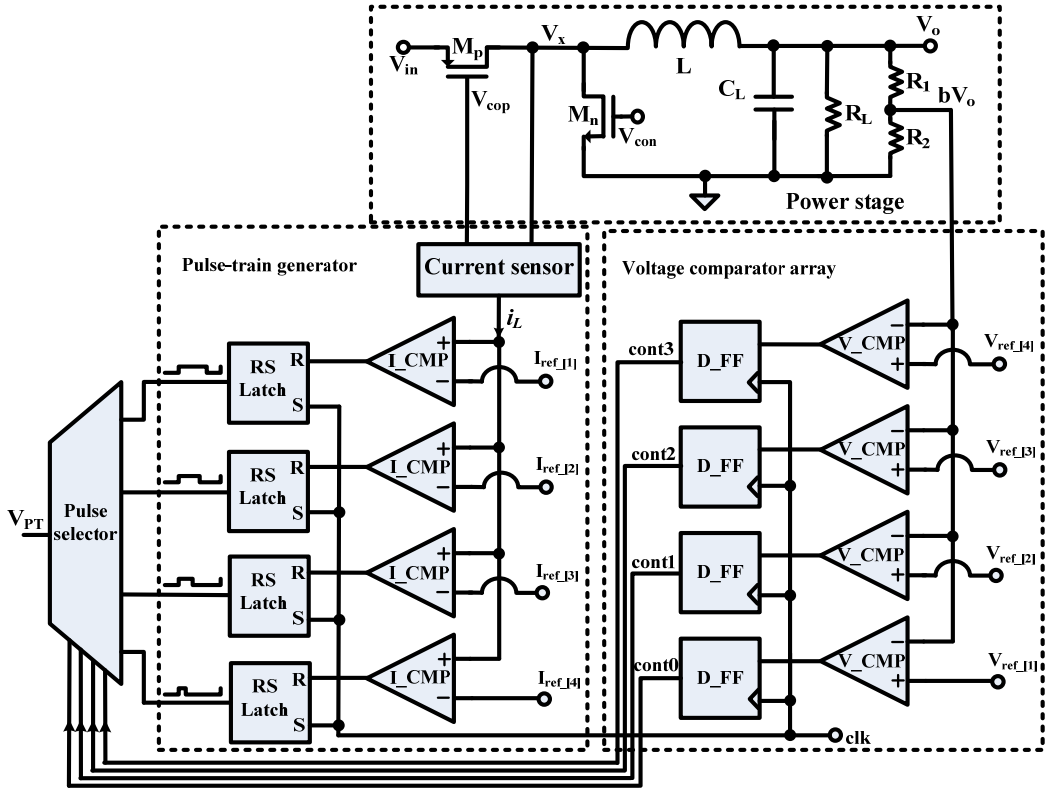


Figure 3.3.2 Schematic of the PT controller.

The circuit schematic of the proposed PT controller is shown in Figure 3.3.2. The voltage comparator array compares the output voltage V_o with four predefined reference voltage levels $V_{ref\_[i]}$ (i=1, 2, 3, 4), and then generates four synchronized control signals for the pulse selector. The PT pattern is then selected based on the instantaneous inductor current i_L sensed by a current sensor. The inductor current based control significantly improves transient response and regulation accuracy, compared to our preliminary simulation work [Luo-07].

To ensure low power dissipation from the controller, a self-biased comparator is implemented with the focus on low power and fast speed, as depicted in Figure 3.3.3. The circuit directly benefits the entire comparator array used in Figure 3.3.2.

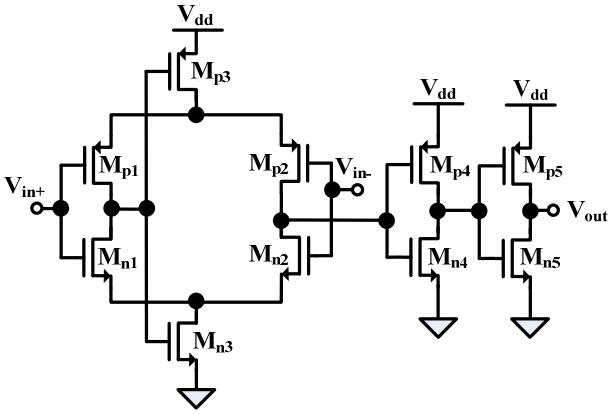


Figure 3.3.3 Schematic of the comparator.

3.3.3 Transistor-Scaling Current Sensor

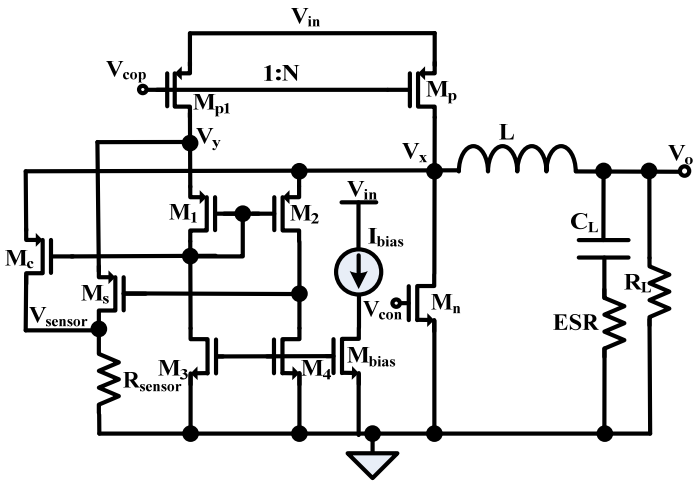
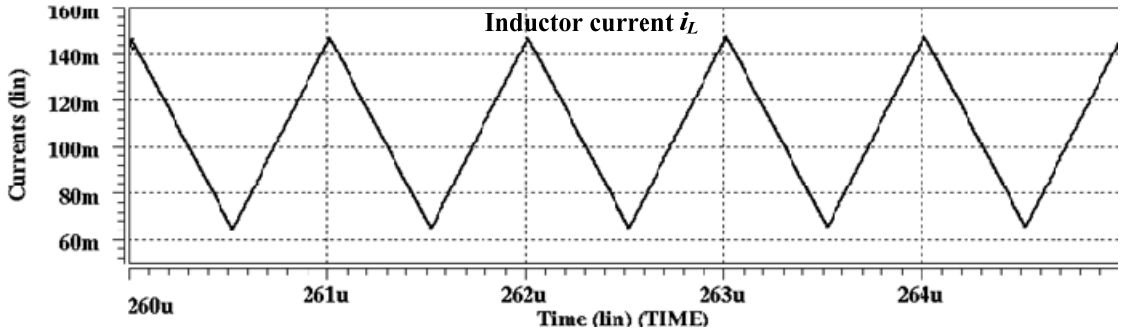


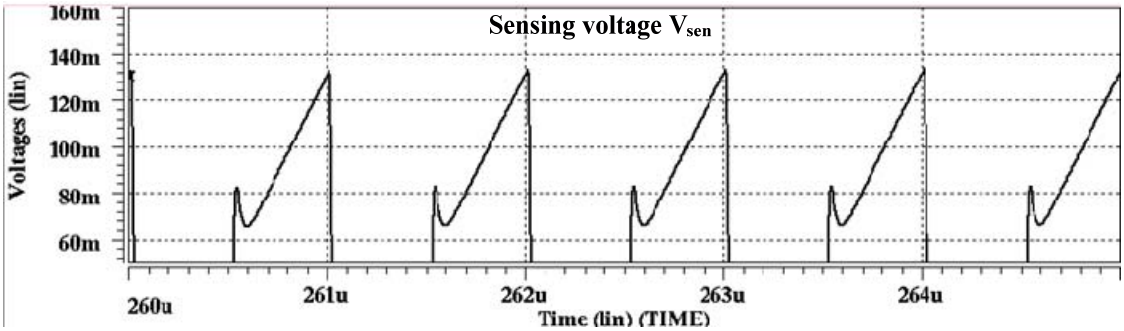
Figure 3.3.4 Current sensor with transistor scaling.

To generate the correct pulse patterns, a current sensor is designed to monitor the instantaneous inductor current i_L. In each operation region, the controller computes the peak current level $I_{ref\_[i]}$ (i=1, 2, 3, 4), by evaluating the real-time inductor current i_L. Tailored for low-voltage low-power designs, we adopt a PMOS current sensing circuit based on transistor scaling techniques [Ma-03b]. As shown in Figure 3.3.4, the transistors M_1~M_4 form a voltage mirror and force the drain voltages of M_p and M_{p1} to be equal. Here, M_p is the PMOS power transistor in the

power stage, while M_{p1} is the sensing PMOS transistor that is N times smaller than M_p. Because the two transistors operate at the same DC operation conditions, the inductor current i_L, which flows through M_p, is scaled down by N times in M_{p1}. As a result, the power consumption of the current sensor is N-time lower than using sensing resistors, which contributes high efficiency at light load. In this design, the scaling factor N is 1000.



(a)



(b)

Figure 3.3.5 (a) Simulated inductor current i_L, and (b) sensing voltage V_{sen}.

To evaluate the current sensing performance, Figure 3.3.5 shows simulated sensing voltage with reference to the inductor current i_L. The sensing voltage is linearly proportional to i_L. In this design, we have $i_{sen} : i_L = 1 : 1000$ and R_{sen}=1KΩ. Accordingly, power consumption of the current sensing circuit is reduced by 50 times, compared to the case of using 50-mΩ sensing resistor. The sensing accuracy is 90.7%.

3.3.4 Clock & Ramp Generator

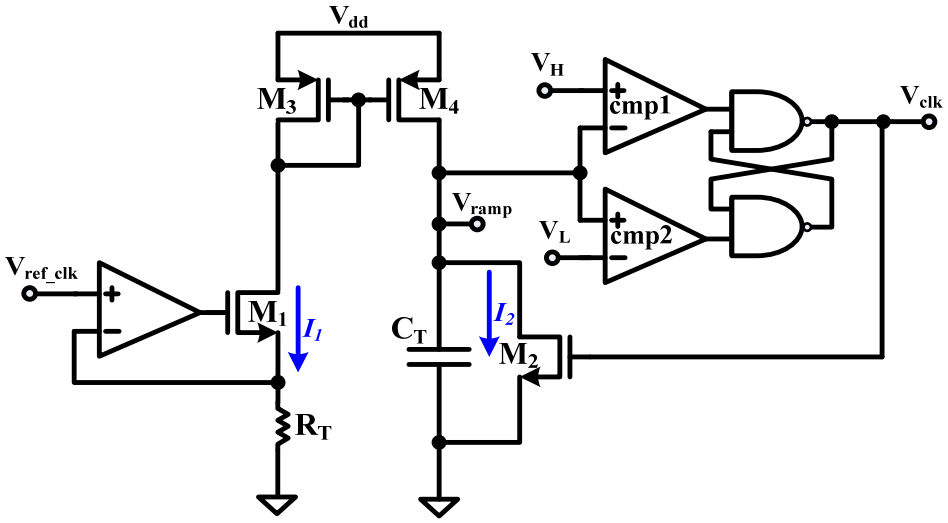


Figure 3.3.6 Schematic of the clock and ramp generator.

A clock and ramp generator is used to generate the clock and ramp signals for the PWM control and synchronize the PT control signals, respectively. As shown in Figure 3.3.6, it consists of a voltage-to-current (V-to-I) converter and a hysteretic comparator. A reference voltage V_{ref_clk} and resistor R_T are used to control the charging current of the capacitor C_T and thus determine the clock frequency. When the ramp signal V_{ramp} reaches V_H, the comparator is reset to turn on the transistor M_2 (acts as a switch) and discharge the capacitor C_T. Normally, the discharging current is much larger than the charging current. The ramp signal drops until it reaches V_L and the comparator changes state and the transistor M_2 turns off. Therefore, the clock frequency and the slope of the ramp are synchronized with each other. And the frequency of the clock and ramp signal is

$$f_s = \frac{V_{ref\_clk}}{R_T C_T (V_H - V_L)}. \tag{3.24}$$

3.3.5 Dead-Time Controlled Buffer

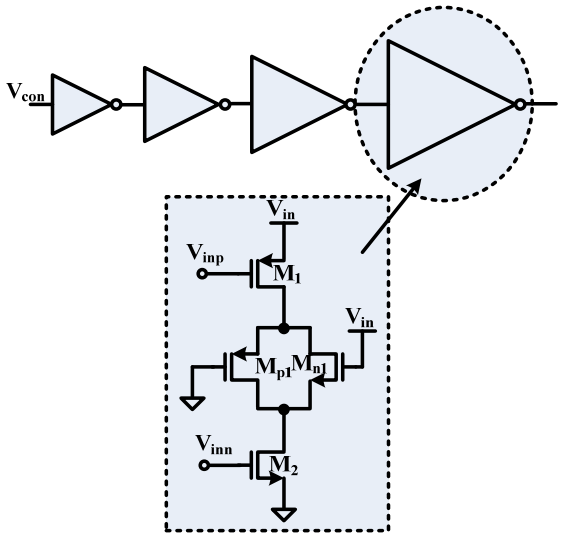
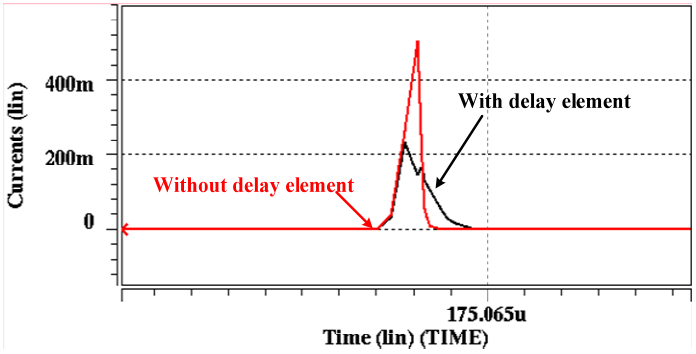
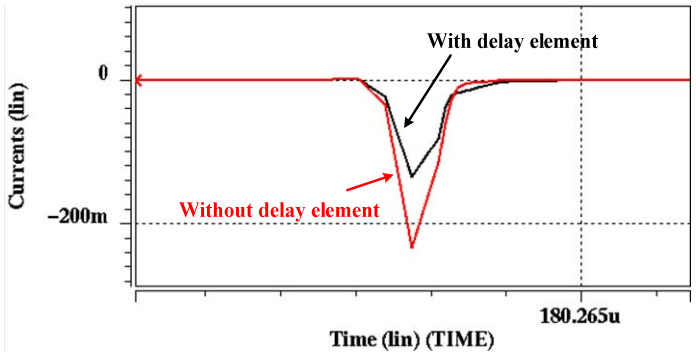


Figure 3.3.7 Block diagram of the dead-time controlled buffer.

For a power transistor, the major power losses include conduction loss and switching loss. The conduction loss of the switching converter is inverse propositional to the on- resistances on the power transistors. We prefer larger power transistors to achieve lower on-resistances and lower power losses. Hence the nMOS power transistor M_n in Figure 3.3.7 should not be turned on when the pMOS M_p is conducting to avoid large shoot-through current that would seriously degrade the efficiency of the converter and cause large glitches in the inductor current and output voltage. The dead-time controlled buffer is then needed. As shown in Figure 3.3.7, by adding a resistor in the driving inverter, the pMOS M_1 can be turned off prior to the turn-on of the nMOS M_2 during the "1" to "0" transition, the shoot-through current of the buffer can be greatly reduced. A similar mechanism applies to the "0" to "1" transition. The resistor is realized by M_{n1} and M_{p1} as shown in Figure 3.3.7.



(a)



(b)

Figure 3.3.8 Simulated current in the inverter with & without delay element: (a) current in nMOS transistor, and (b) current in pMOS transistor.

Figure 3.3.8 shows the simulated currents in the buffer with and without delay elements. As we can see, with the delay elements, both the nMOS and pMOS shoot-through currents are greatly reduced.

3.4 Experimental Verifications

The proposed converter was designed and fabricated with a 0.35-μm digital CMOS N-well process. Figure 3.4.1 shows the chip micrograph. The entire silicon area is 1.31 mm^2, including all the on-chip pads and power transistors. For the power stage, we choose the inductor and the capacitor values as 10 μH and 10 μF, respectively. The ESR of the capacitor is 350 mΩ.

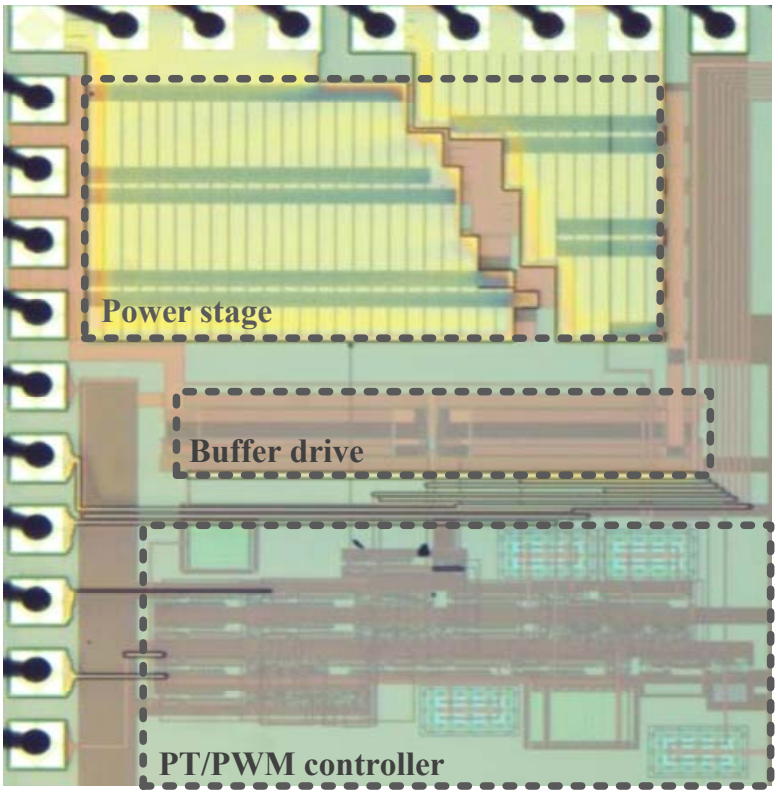


Figure 3.4.1 Chip micrograph.

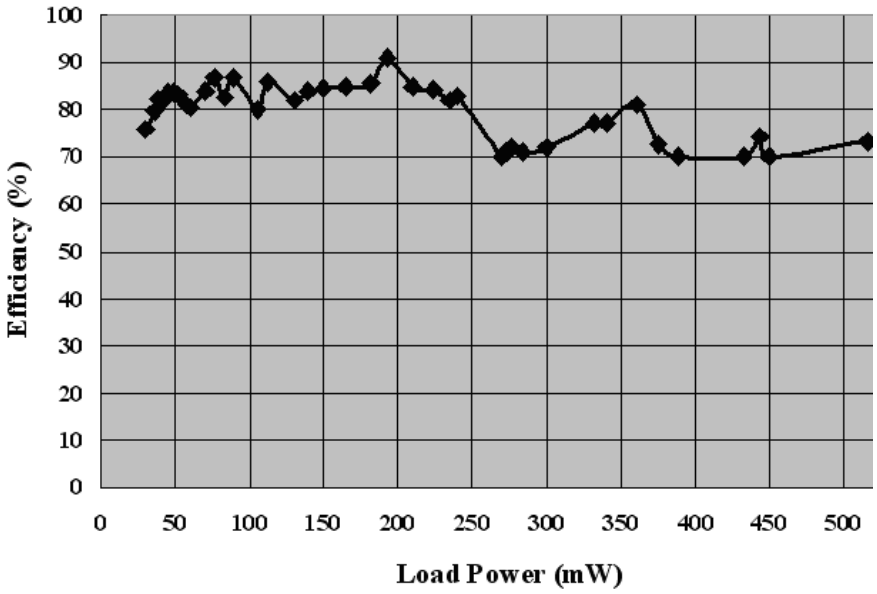


Figure 3.4.2 Measured efficiency of the converter.

Under the nominal operation condition, the output of the converter is well-regulated at 1.5 V with a maximum power of 517 mW and an input voltage of 3.3 V. The switching frequency ranges from 200 to 550 kHz in the PT mode and from 1 to 2.5 MHz in the PWM mode. Figure 3.4.2 shows the plot of the measured efficiency. It remains above 70% in a power range of 20 to 517 mW, with a maximum value of 91% at 193 mW.

3.4.1 Measurement Results in the PT Mode

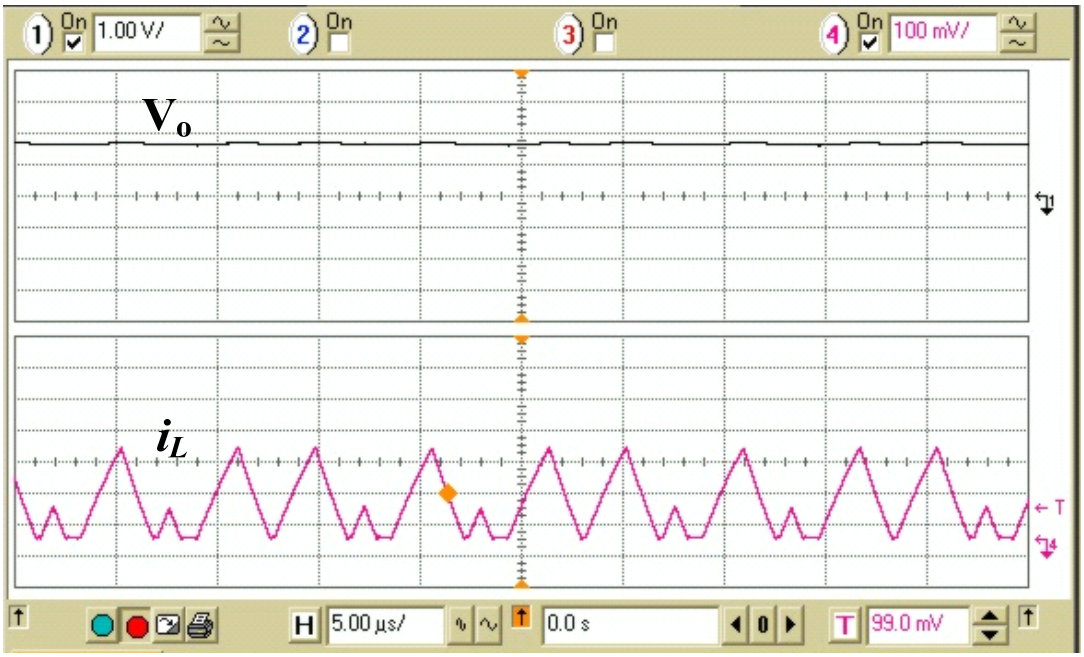


Figure 3.4.3 Measured steady-state V_o and i_L at the PT mode.

Figure 3.4.3 shows the measured steady-state output voltage V_o and inductor current i_L in the PT mode. Observation on i_L reveals that large and small pulses are assigned alternately to regulate V_o at 1.5 V. A close-up view of Figure 3.4.3 tells that V_o is well controlled with ±50 mV peak-to-peak ripple voltages at a switching frequency of 250 kHz in Figure 3.4.4. The advantages of the PT control are reflected in the load transient measurement in Figure 3.4.5. Here, V_R represents the load control voltage. When V_R steps down from "1" to "0", the

equivalent load current steps up from 50 to 100 mA. In this measurement, the settling time of V_o is shorter than 345 ns and the overshoot and undershoot voltages are 166 and 145 mV, respectively.

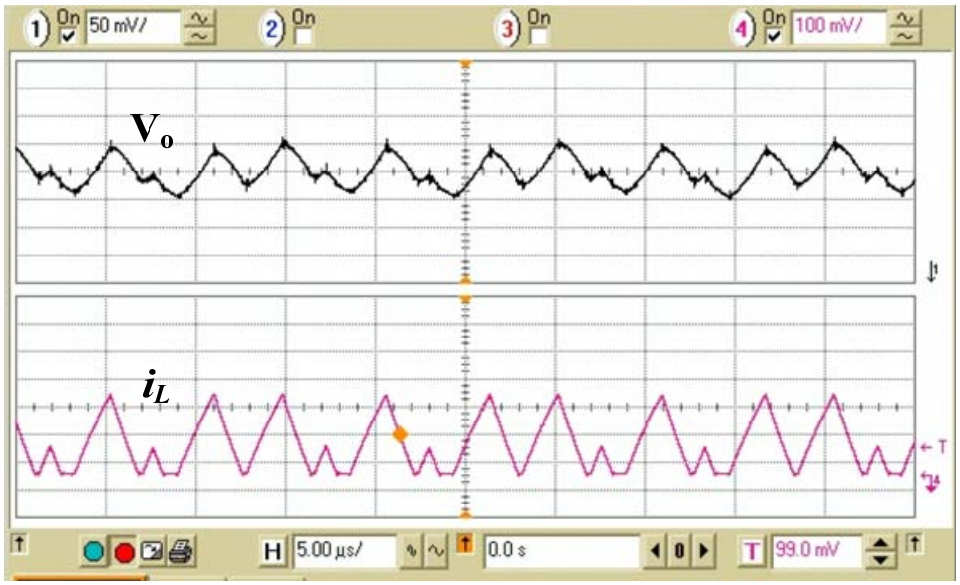


Figure 3.4.4 Measured ripple voltage with reference to i_L at the PT mode.

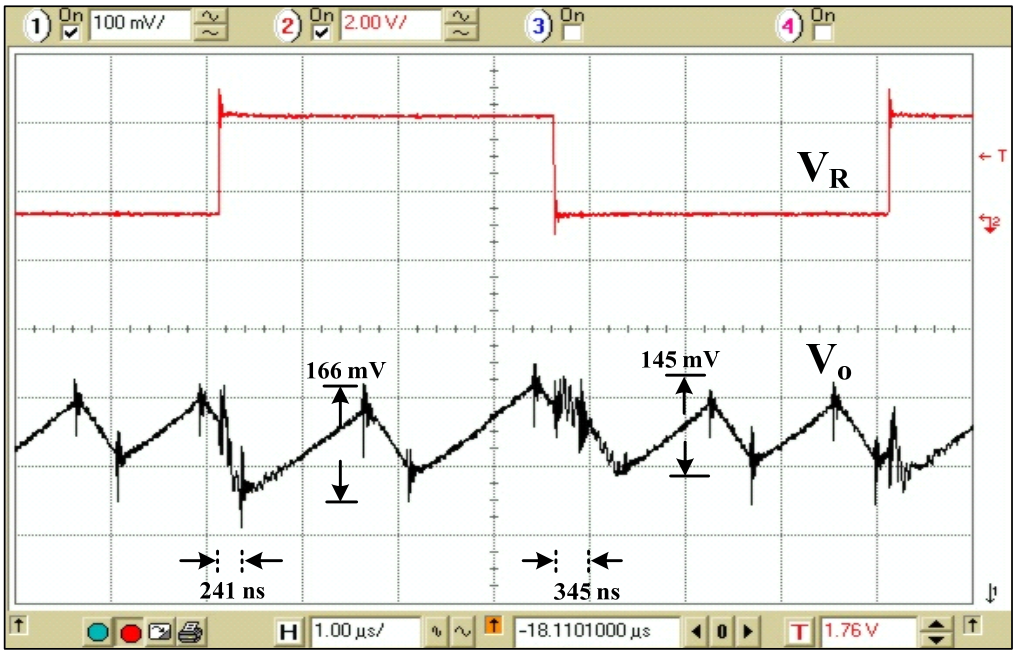
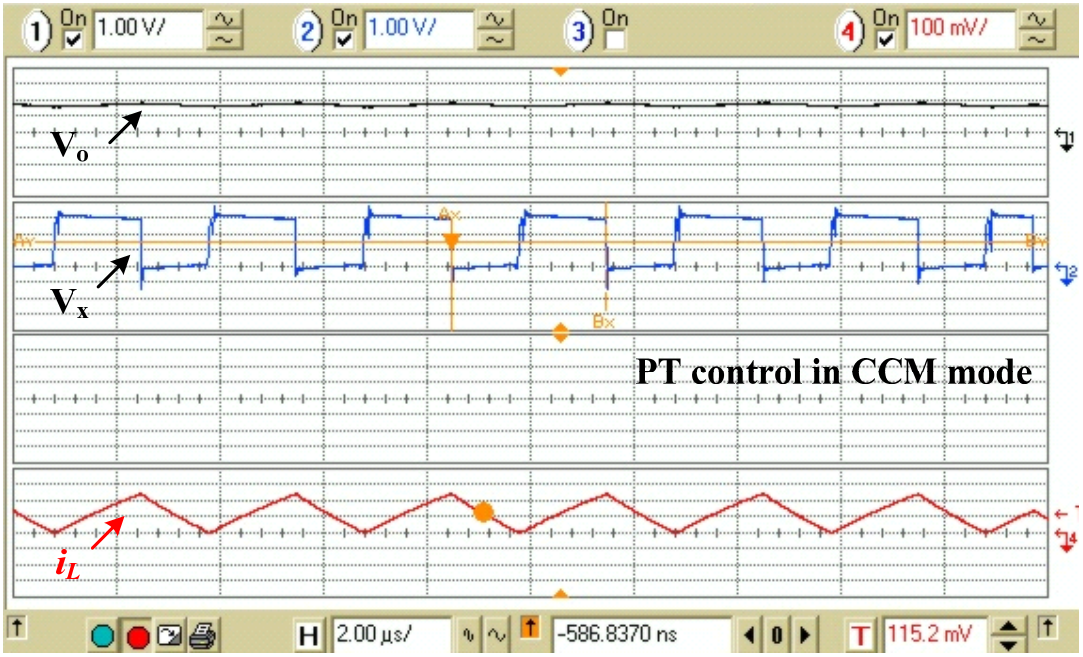
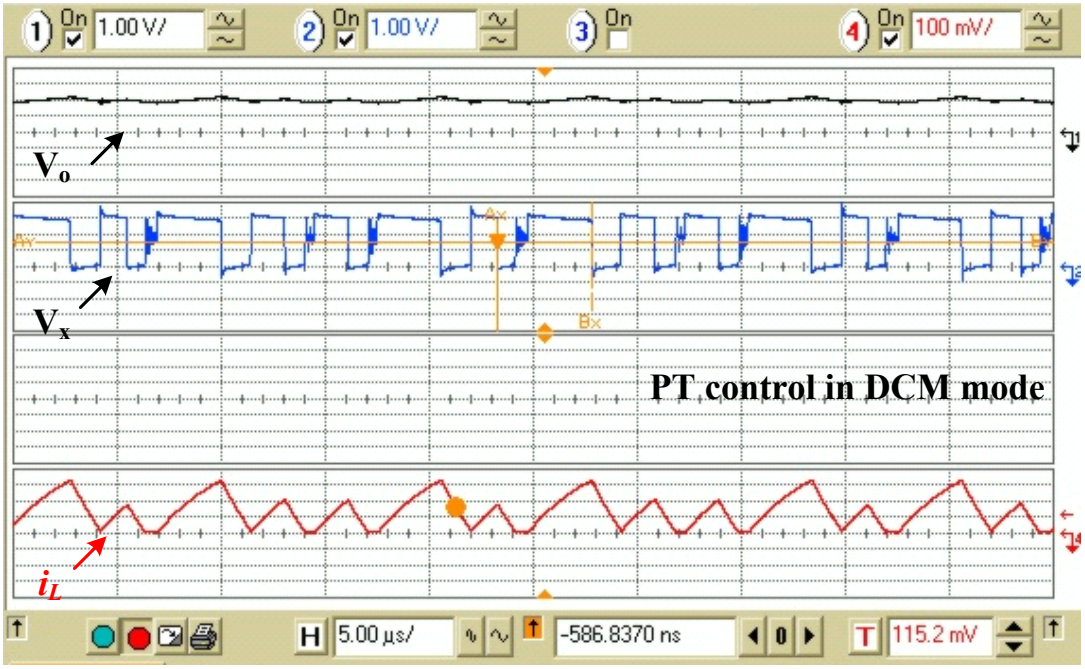


Figure 3.4.5 Measured load transient response at the PT mode: (upper) load current i_O switching between 50 mA and 100 mA, (lower) output V_o.



(a)



(b)

Figure 3.4.6 Measured V_o, V_x, and i_L at the PT control: (a) CCM mode, and (b) DCM mode.

The PT control can regulate the output in both CCM (continuous conduction mode) at heavy load and DCM (discontinuous conduction mode) at light load. Figure 3.4.6(a) and (b)

illustrate the measured output voltage V_o, the voltage at node V_x, and the inductor current i_L in CCM and DCM, respectively.

3.4.2 Measurement Results in the PWM Mode

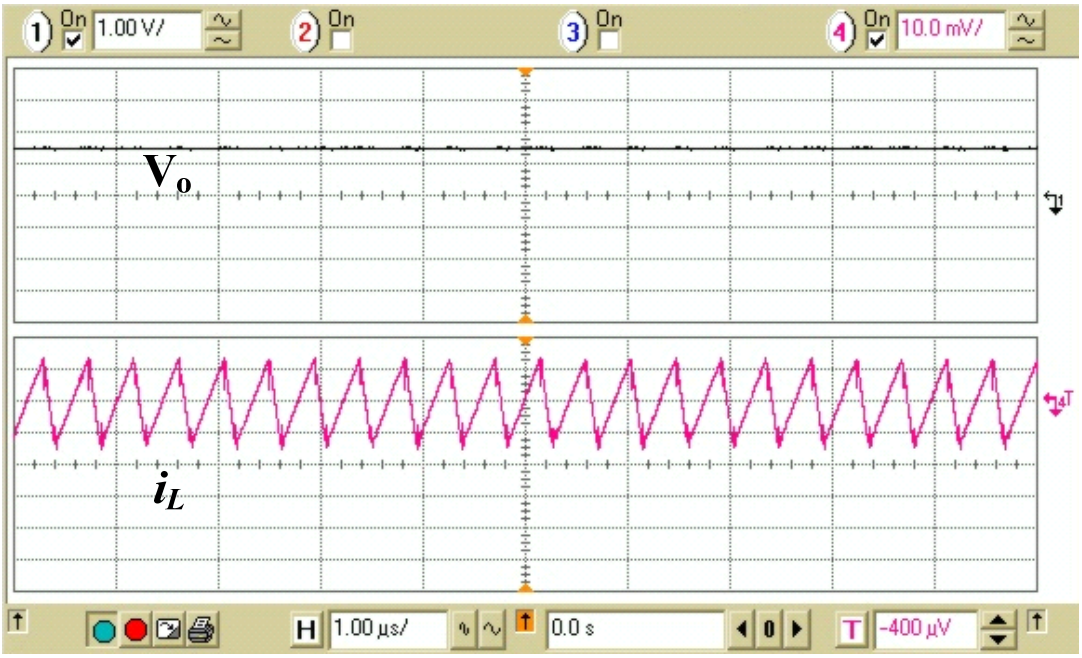


Figure 3.4.7 Measured steady-state V_o and i_L at the PWM mode.

Meanwhile, the measurements in the PWM mode were also performed. Figure 3.4.7 shows the measured steady-state output voltage V_o and the inductor current i_L, respectively. A closer look at the output ripple voltage and the inductor current is shown in Figure 3.4.8. Due to the infinite analog duty ratio resolution, the CCM operation mode and the higher switching frequency, the ripple at V_o is reduced from ±50 mV in the PT mode to ±12.5 mV in the PWM mode.

Figure 3.4.9 shows the load transient measurement in the PWM mode. With the same 100% load transient measurement set-up in Figure 3.4.5, the settling time of the output voltage V_o is 10.2 µs for step-up load change and 7.8 µs for step-down load transient. The corresponding

maximum voltage variations are 116.5 mV and 169.4 mV, respectively. With a line regulation of 29.1 mV/V, the converter functions robustly, even when the supply voltage varies between 2.2 V and 3.3 V abruptly.

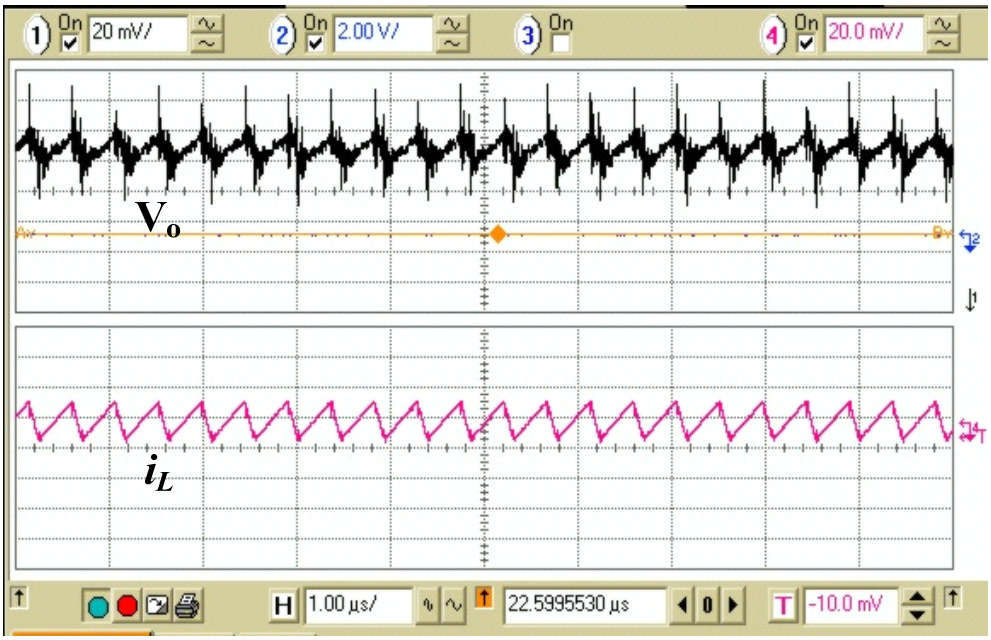


Figure 3.4.8 Measured ripple voltage with reference to i_L at the PWM mode.

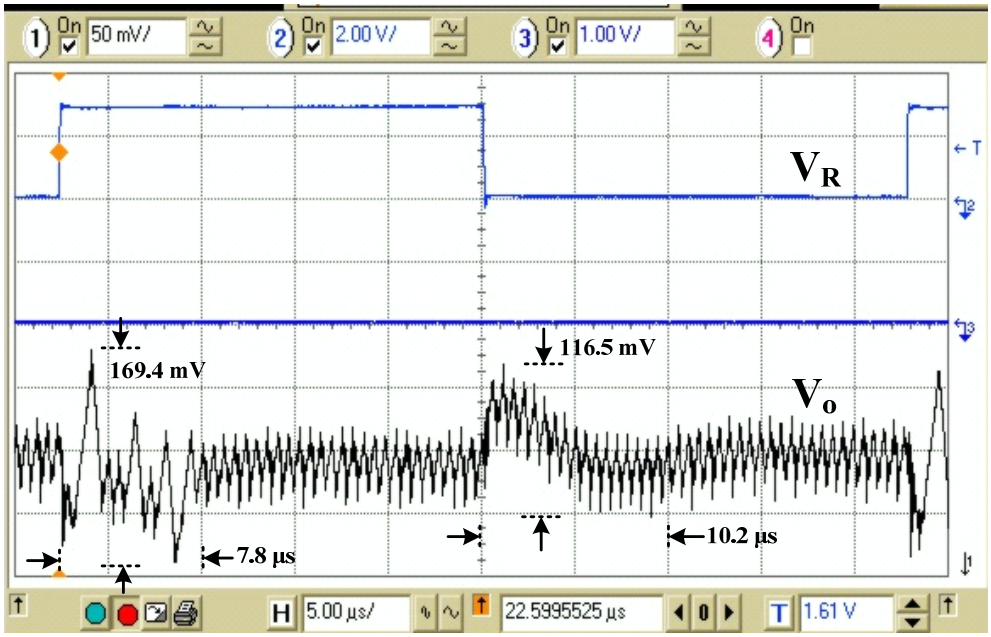


Figure 3.4.9 Measured load transient response at the PWM mode: (upper) load current i_O switching between 50 and 100 mA, (lower) output voltage V_o.

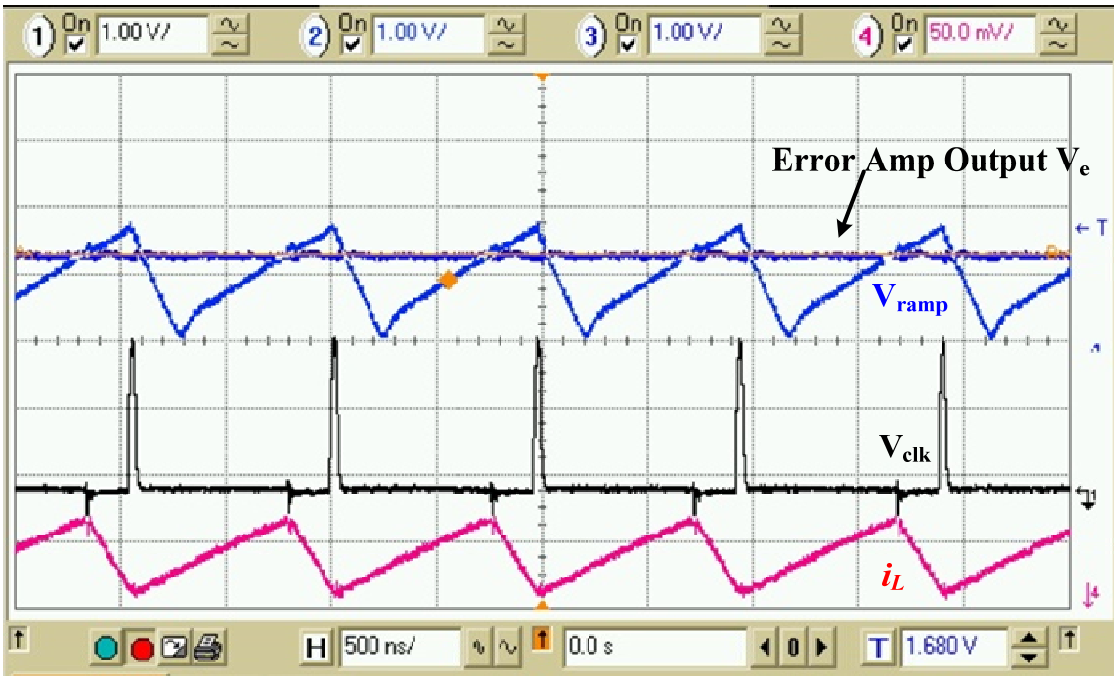


Figure 3.4.10 Measured error amplifier output V_e, ramp signal V_{ramp}, clock signal V_{clk}, and inductor current i_L at the PWM mode.

Figure 3.4.10 shows the measured error amplifier output V_e, ramp signal V_{ramp}, clock signal V_{clk}, and the corresponding inductor current i_L. The error amplifier output V_e is compared with the ramp signal V_{ramp}, and the duty ratio D is generated at a much higher switching frequency to control the switching actions of the power transistor M_n and M_p.

3.5 Conclusions

A new switching power converter IC design with a dual-mode PT/PWM control is presented. With the proposed architecture and control scheme, the performances on ripple voltage and transient response of the converter are both improved. The results on both the PT and PWM controls successfully verify the proposed design ideas. It provides an effective solution to high performance power converter designs.

CHAPTER 4 DESIGN OF DIGITAL TRI-MODE ADAPTIVE-OUTPUT BUCK-BOOST POWER CONVERTER FOR POWER-EFFICIENT INTEGRATED SYSTEMS

An integrated buck-boost converter with a tri-mode digital control is presented. It employs adaptive step-up/down voltage conversion to enable a wide range of output voltage. This is beneficial to ever-increasing dynamic voltage scaling (DVS) enabled, modern power-efficient VLSI systems. Three voltage and current control modes operate jointly and seamlessly to optimize the converter's performance at start-up, steady state and dynamic voltage/load transient state, respectively. To avoid latch-ups and large leakage current, a compact automatic substrate switching circuit (ASSC) is introduced, which is compatible with low-cost single-well digital CMOS process.

The converter was designed and fabricated with a standard 0.35-μm digital CMOS N-well process. The entire die area is 1.3 mm^2. With a 2.5-V input power supply, the converter precisely provides an adjustable power output within a voltage range from 0.9 to 3.0 V and a power range from 11 to 800 mW. Maximum efficiency of 96.5 % is measured at 0.9-V output and 45-mW load power, while the efficiency remains above 50% over the entire 800-mW power range. Load transient response is shorter than 600 ns when the load current experiences step changes from 45 to 90 mA. DVS tracking speed is 37 μs/V for 1.0-V output step change. The robust controls and circuit designs ensure the system to function well, even when the input power source frequently fluctuates between 1.6 and 3.3 V, with a line regulation of 20.4 mV/V. The ASSC consumes only 88-μW static power.

4.1 Design Challenges and Motivations

In the modern world of technology, highly sophisticated electronic systems such as multiprocessor modules and system-on-a-chips (SOCs) pave the way for future's information technology breakthroughs. However, rapid growth on complexity and functions in such a system has also been a harbinger for the increase in power consumption, which tends to severely limit system miniaturization, efficiency, robustness and lifetime. Efficient power management techniques have therefore been introduced to mitigate this urgent power crisis. Dynamic voltage scaling **(DVS)** is such an algorithm which adaptively modifies the supply voltage and corresponding operation frequencies, such that a system can be constantly operated at the lowest possible power level without compromising the performance. It is considered as one of the most efficient power operation techniques in contemporary VLSI system designs, and has been effectively exploited in many commercial low-power processor designs [Burd-00] [Calhoun-06] [Kwon-03] [Nowka-02].

One of the most challenging issues in implementing DVS algorithms is the requirement on the "untraditional" power supplies, which need to provide a variable output based on the instant power demands [Kim-01] [Ma-04] [Ma-06a] [Weiser-94]. Usually, such supplies are implemented using switching DC-DC converters, because of their high efficiency and flexible voltage conversion. However, compared to conventional fixed-output switching converters, these new types of converters face unprecedented design challenges. **Firstly**, in the traditional DC-DC converters themselves, stabilization and compensation have been difficult issues. In adaptive switching converters, these issues become even more complex due to the frequent variations at the output voltage and the load current. **Secondly**, in order to adapt to high-speed operations in VLSI systems, the output voltage/load transient response has to be significantly improved from

the order of milliseconds, which is the current range, to the order of microseconds or shorter. This requirement is to prevent latency and computing errors that occur during voltage changes. **Thirdly**, while maintaining high-efficiency is vital to all power converters, it becomes even more challenging in adaptive converters due to much a wider output power and voltage range. **Fourthly**, to maximize the effectiveness and flexibility of DVS techniques, a buck-boost converter is preferred over buck or boost converter, as it can provide voltages that are either higher or lower than the main power source. Such inherent flexibility can lead to large power savings when used in conjunction with DVS techniques. Unfortunately, in contrast to the buck or boost converters, the buck-boost converter has isolated charging and discharging paths in the power stage, leading to difficulties in start-up and DVS dynamic periods [Erickson-01]. **Last**, the variable step-up/down output voltage makes substrate biasing difficult and costly. For example, in an N-well CMOS process, the pMOS substrates are biased at the highest on-chip voltage to avoid large current leakage or latch-ups. However, as will be discussed, such a voltage does not exist at any fixed circuit nodes of the proposed converter. This dilemma can be overcome by using the twin or tri-well processes, but leads to much higher fabrication cost.

In this design, we propose a variable-output buck-boost converter with an integrated digital tri-mode control and an automatic substrate switching circuit (**ASSC**) technique to overcome the difficulties discussed earlier. Detailed design strategies and theoretical analysis of the digital tri-mode control are discussed. Moreover, systematic design consideration and optimization are also provided. The rest of the chapter is organized as follows. Section 4.2 elaborates the proposed digital tri-mode control in the adaptive converter. Some key system design issues are also discussed. In Section 4.3, we introduce the detailed closed-loop system

design and its circuit implementations. Section 4.4 verifies the circuit functionality and control validity with experimental results. Finally, we summarize this work in Section 4.5.

4.2 Digital Tri-Mode Control Scheme

4.2.1 Power-Scalable Digital Sliding Mode Control

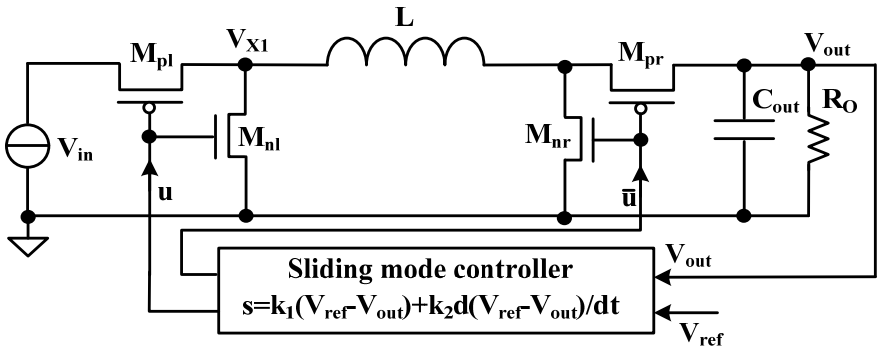


Figure 4.2.1 Analog sliding mode controller with a buck-boost converter.

Sliding mode controls were initially introduced for the robust control of variable structure systems [Utkin-92] [Utkin-99] [Perruquetti-02]. The basic principle of sliding mode control is to design a certain sliding surface, in the control law, which will direct the trajectory of the state variables towards a desired origin. Figure 4.2.1 shows the block diagram of an analog sliding controller integrated along with a buck-boost converter. Currently, most existing sliding mode control designs involve complicated analog implementations [Bilalovic-83] [Perruquetti-02] [Utkin-92] [Utkin-99] [Venkataramanan-85]. One such implementation in [Bilalovic-83] used seven op-amps, along with numerous resistors and capacitors, as shown in Figure 4.2.2. Such a realization exhibits many drawbacks, which are as follows: the nature of the analog operation makes the controller very sensitive to switching noises. Meanwhile, the cascaded amplifier stages severely limit the frequency bandwidth, resulting in a sluggish transient behavior.

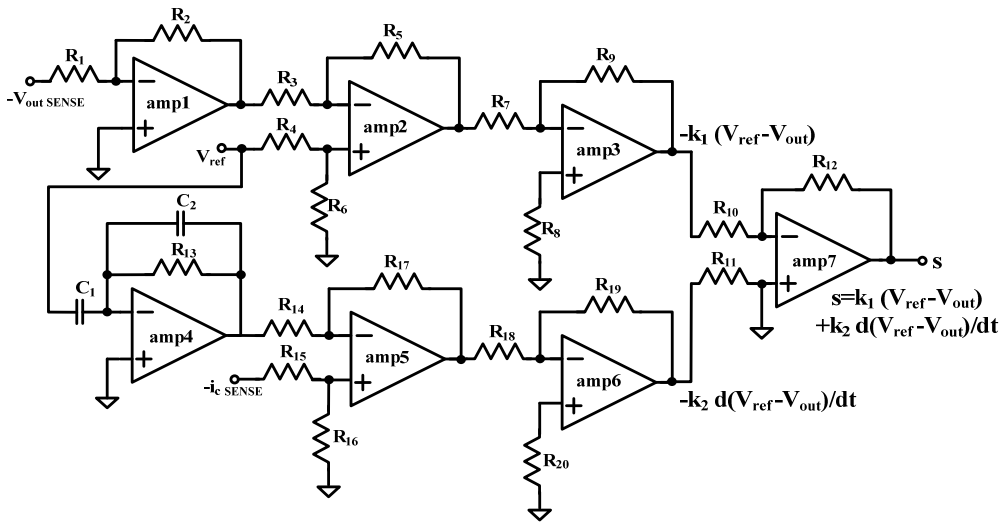


Figure 4.2.2 One implementation of the analog sliding mode controller in [Bilalovic-83].

A digital implementation was reported in [Kim-01], but could only achieve a step-down conversion in a buck converter topology. For our purposes, the digital control scheme is very desirable; as such a realization can be inherently immune to noise and has the potential for a compact IC implementation. More importantly, if the controller could be directly powered by the variable output V_{out}, its power consumption becomes scalable to V_{out}. This is extremely helpful in maintaining high efficiency, especially in low-power DVS operations.

Unlike analog implementation that regulates the voltage, digital control regulate the frequency or the delay of the reference circuits. Therefore, the controlled variable is the frequency f_{out} and f_{ref}, instead of the voltage V_{out} and V_{ref}. Then the sliding control requires the information on the frequency error $(f_{ref} - f_{out})$ and its derivative $d(f_{ref} - f_{out})/dt$ which is not directly available.

The straightforward approach to estimate $d(f_{ref} - f_{out})/dt$ would be to measure the difference in frequency between the present and previous samples. However, this requires a very high resolution in detecting frequency, because the sampling rate has to be greater than the

system dynamics by a sufficient amount to avoid instability due to the loop delay, and therefore the change in frequency during each sampling period is very small.

A better approach is instead to derive the slide rule in a way that the frequency derivative df_{out}/dt can be represent as other control variables. Since buck-boost converter is preferred for maximizing the effectiveness and flexibility of DVS techniques, our analysis below will base on the buck-boost converter.

In order to derive operating principle of the digital sliding mode control, the state-space description of the buck-boost converter under sliding mode control, is first discussed. The control variables are not only the output voltage error, but also the voltage error dynamics. As shown in Figure 4.2.1, the voltage error x_1 and the voltage error dynamics x_2 can be expressed as

$$\begin{cases} x_1 = V_{ref} - V_{out} \\ x_2 = \dot{x}_1 = -\dfrac{dV_{out}}{dt} \end{cases}, \tag{4.1}$$

where V_{ref}, V_{out} are the reference voltage and output voltage.

For a buck-boost converter, it follows

$$-\frac{dV_{out}}{dt} = -\frac{i_{cout}}{C_{out}} = \frac{1}{C_{out}}\left(i_O - \frac{V_{in}}{V_{ref}+V_{in}}\cdot i_L\right), \tag{4.2}$$

where C_{out}, i_{cout}, i_O, and i_L are the output filtering capacitor, the current flowing through C_{out}, load current and inductor current respectively. The sliding surface of the sliding controller is chosen to be a linear combination of x_1 and x_2, i.e.,

$$s = k_1x_1 + k_2x_2 = k_1(V_{ref} - V_{out}) - k_2\frac{dV_{out}}{dt}k_1 = (V_{ref} - V_{out}) + \frac{k_2}{C_{out}}\left(i_O - \frac{V_{in}}{V_{ref}+V_{in}}\cdot i_L\right), \tag{4.3}$$

where k_1 and k_2 represents the sliding coefficients. If we choose $k_2=C_{out}$, $k_1=k_v$ and $V_{in}/(V_{ref}+V_{in})=k_i$, the sliding rule s becomes

$$s = k_v(V_{ref} - V_{out}) + i_O - k_i \cdot i_L . \tag{4.4}$$

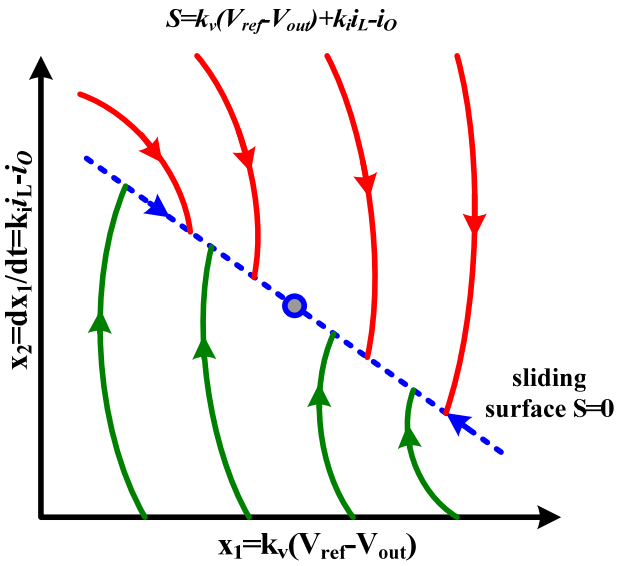


Figure 4.2.3 Phase plane plot of the sliding rule.

Note that k_i is variable to different V_{out} (V_{ref}) for optimized sliding control state. By enforcing s=0, a sliding surface with gradient k_1/k_2 can be obtained. The purpose of the sliding surface is to serve as a boundary to split the phase plane into two regions, as shown in Figure 4.2.3. Each of these regions is specified with a switching state to direct the phase trajectory towards the sliding surface. It is only when the phase trajectory reaches and track the sliding surface towards the origin that the system is considered to be stable. To ensure that the trajectory is maintained on the sliding surface, the existence condition, which is derived from *Lyapunov*'s second method [Slotine-91] to determine asymptotic stability, must be obeyed:

$$s \cdot \dot{s}\big|_{s\to 0} < 0 \ . \tag{4.5}$$

Then, from (3) and (5), the condition for sliding mode control to exist is

$$\dot{s} = \begin{cases} k_1\dot{x}_1 + k_2\dot{x}_2 < 0 & for \quad 0 < s < \varepsilon \\ k_1\dot{x}_1 + k_2\dot{x}_2 > 0 & for -\varepsilon < s < 0 \end{cases}, \tag{4.6}$$

where ε is an arbitrarily small positive quantity. It can be observed that at steady state, the output and reference voltage error is relatively small, and

$$\dot{s} \approx -k_i \cdot \frac{di_L}{dt}. \tag{4.7}$$

If the phase trajectory is at any arbitrary position above the sliding surface(s=0), 0<s< ε, from (4.6) and (4.7), we know that di_L/dt>0, and the inductor current i_L will increase to ensure the trajectory is directed towards the sliding surface, and the state control signal u for power switch M_{pl} and M_{nl} will be 0 and $\bar{u}$ = 1−u for M_{pr} and M_{nr} will be 1; if s<0, the phase trajectory will be at any point below the sliding surface, di_L/dt<0, and with u=1 and $\bar{u}$ =0, i_L will decrease. This forms the basis of the sliding-mode control law.

Ideally, the converter will switch at infinite frequency with its phase trajectory tracking along the sliding surface when it enters the sliding mode. However, because of the presence of non-ideal switching actions, the discontinuity in the feedback control will produce a particular dynamic behavior in the vicinity of the sliding surface trajectory known as chattering [Perruquetti-02] [Utkin-92] [Utkin-99].

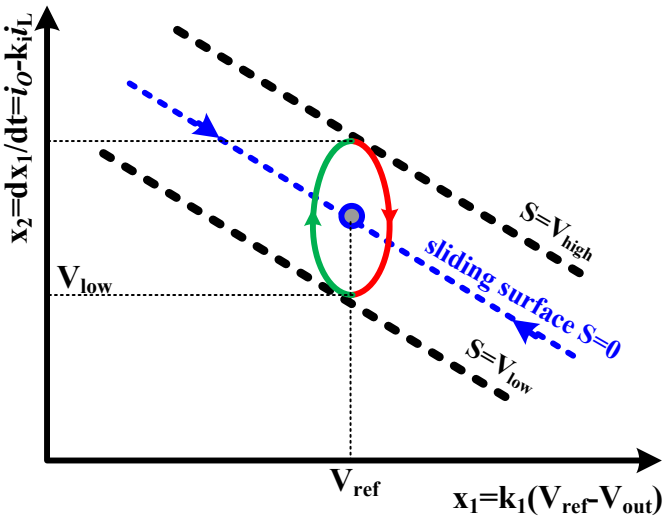


Figure 4.2.4 The phase plane of the limit cycle.

In order to avoid the chattering, and self-oscillating, a hysteresis band is introduced into the control law with the boundary conditions s=V_{high} and s= V_{low}. The hysteresis will control the switching frequency and the output ripple voltage of the converter, and the sliding surface will split into two lines and the steady state becomes a limit cycle formed between these two lines, as shown in Figure 4.2.4.

From (4.4), instead of considering (V_{ref}−V_{out}) and the derivative dV_{out}/dt , the controller detects and processes the signals of V_{out}, V_{ref}, $i_{L,}$ and i_O to maximize control effectiveness and boost transient speed. And the digital sliding rule becomes very simple: the control decision is made simply by the voltage error between the output voltage and reference voltage combined with the current error between the load current and the inductor current. Complicated frequency derivative df_{out}/dt is avoided.

In order to easily implement the control rules in a digital system, we map the original voltage and current signals ($V_{ref,}$ $V_{out,}$ $i_{L,}$and i_O) to corresponding digital signals in the frequency domain. This is supported by the delay-voltage equation, ubiquitous in CMOS digital circuit designs [Rabaey-03]:

$$f_{out} = \frac{\beta(V_{out} - V_{th})^2}{2k \cdot n_{stages} \cdot C_{load} V_{out}}, \tag{4.8}$$

where k and β are process parameters, n_{stages} is the number of delay buffer stages and C_{load} is the load capacitor for one delay cell. The frequency domain variables for current i_L and i_o can be represented in a similar manner. As a result, the sliding rule in (4.4) is transformed as

$$s_D = k_{fv}(f_{ref} - f_{out}) + f_{io} - k_{fi} \cdot f_{i_L}. \tag{4.9}$$

To be addressed in Section 4.3, because the delay times and noise margins in digital logic gates are much shorter or larger than those in analog op-amps, this transformation makes the

controller much faster and more robust. Furthermore, most of the circuits in this controller would be powered by the adaptive V_{out} instead of the fixed V_{in}. When the converter powers light load with a low voltage according to DVS schemes, power consumption of the proposed controller scales down with V_{out}. This keeps the efficiency of the converter high in low-power range, which cannot be achieved in analog designs.

4.2.2 Tri-Band Hysteresis Current-Mode Start-Up Control

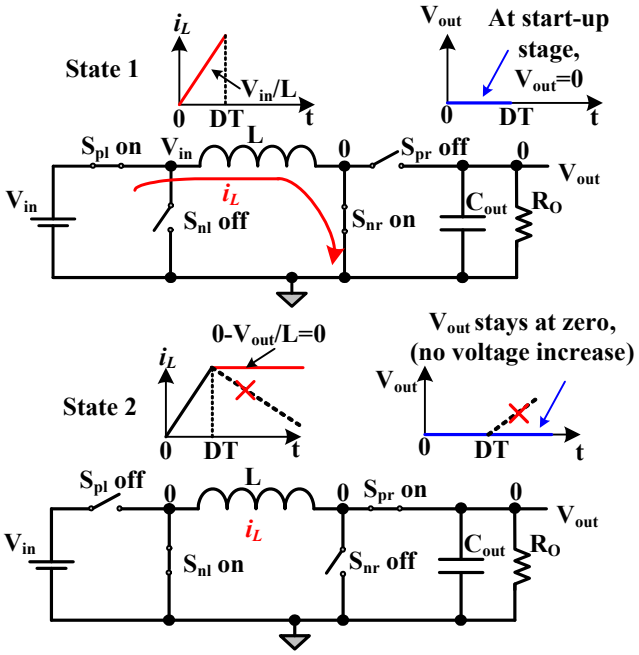


Figure 4.2.5 Start-up issue in buck-boost converter.

Although a buck converter starts up easily, a buck-boost converter requires extra control mechanism even for the step-down conversion. Such an issue can be illustrated in Figure 4.2.5. Initially, V_{out} is relaxed at zero. Although it operates well in State 1, the inductor current i_L cannot decrease in State 2, because the voltage across the inductor L is very low in this period. Although the error amplifier in the controller usually generates a large duty ratio (close to 1) for State 1 and significantly charges up the inductor L, most of the charges stored in the inductor L

cannot flow to the output load, because the remaining discharging period is too short. Therefore, while i_L keeps increasing, the output voltage V_{out} remains to be low. As these charging and discharging actions repeat, the high inductor current i_L may damage power devices permanently.

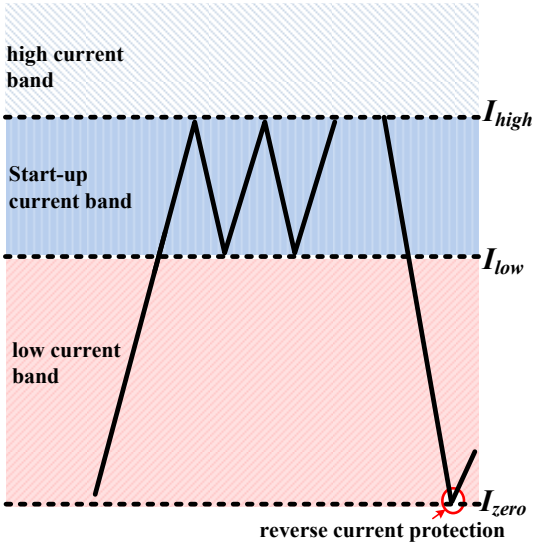


Figure 4.2.6 Tri-band current-mode start-up scheme.

A tri-band hysteresis current-mode start-up scheme is thus adopted. The operation region of the converter is divided into three current bands: low current band, start-up current band and high current band, as shown in Figure 4.2.6. In this design, we employ a current sensing circuit to detect i_L continuously. When i_L is higher than I_{high}, i_L is considered to be dangerously high to damage the power devices. The converter then terminates the State 1 and stops i_L from rising up. State 2 is then initialized. A negative voltage across L makes i_L decease. However, i_L should not drop too low to avoid a very slow start-up response. Hence, once it hits I_{low}, another State 1 will be initialized to increase i_L. Therefore, the inductor current i_L bounces back and forth within the start-up current band just as the output voltage behaves in a classic hysteresis voltage control. We thus call this control as *hysteresis current-mode control*. The block diagram of the proposed current-mode start-up scheme is also shown in Figure 4.2.7.

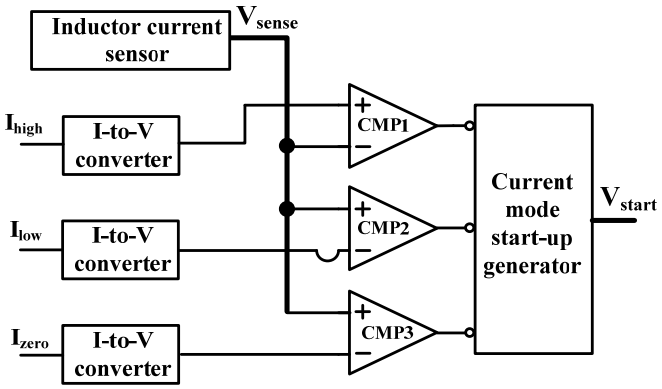


Figure 4.2.7 Block diagram of tri-band current-mode start-up scheme.

Over-current protection and zero-current protection are very important in power supply design for safety reasons. One of the benefits of this proposed current-mode start-up control is the in-cycle current limiting. The three current bands not only ensure the start-up operation, but also guarantee that the inductor current i_L is not too high to damage the power devices or too low to slow down the transient speed. In addition, in case that i_L hits zero by accidence, in order to avoid the reverse current to degrade the efficiency, the converter automatically switches to discontinuous conduction mode (**DCM**). All the power switches are turned off in this mode.

For a buck-boost converter, based on the inductor voltage-second balance rule, we have

$$DT \cdot V_{in} = (1-D)T \cdot V_{out}. \tag{4.10}$$

Hence, the voltage conversion ratio is computed as

$$M = \frac{V_{out}}{V_{in}} = \frac{D}{1-D}, \tag{4.11}$$

where D is the duty ratio and T represents the switching cycle.

To identify the current band boundaries in the control, we simplify the analysis by assuming the power loss from the power stage and the controller is ignorable, which is usually valid for high-efficiency designs. Hence,

$$P_{in} = V_{in} \cdot DI_L = P_{out} = \frac{V_{out}^2}{R_O}, \tag{4.12}$$

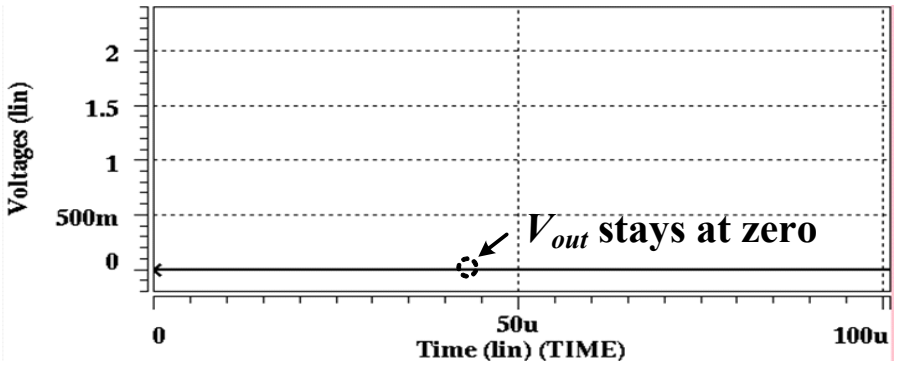
where R_O is the output load, and I_L is the average value of the inductor current i_L, from (10) and (11), we have

$$I_L = \frac{V_{out}^2}{V_{in} R_O D} = \frac{V_{out}}{(1-D)R_O}. \tag{4.13}$$

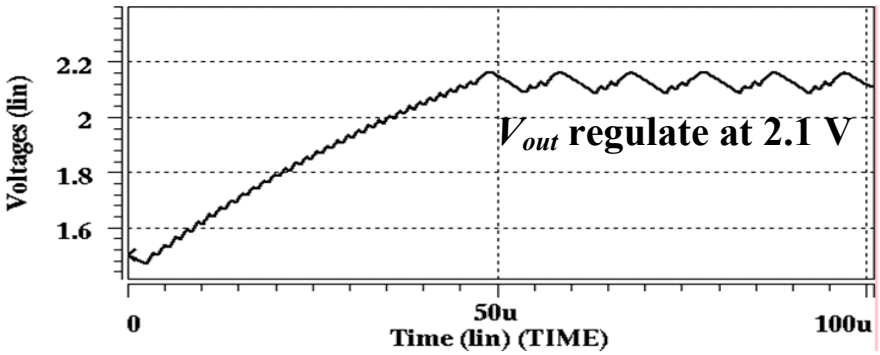
Then I_{high} and I_{low} can be calculated as:

$$I_{high} = I_L + \frac{\Delta i_L}{2} = \frac{V_{out}}{R_O(1-D)} + \frac{1}{2}\left[\frac{V_{out}}{L}(1-D)T\right], \tag{4.14}$$

$$I_{low} = I_L - \frac{\Delta i_L}{2} = \frac{V_{out}}{R_O(1-D)} - \frac{1}{2}\left[\frac{V_{out}}{L}(1-D)T\right]. \tag{4.15}$$



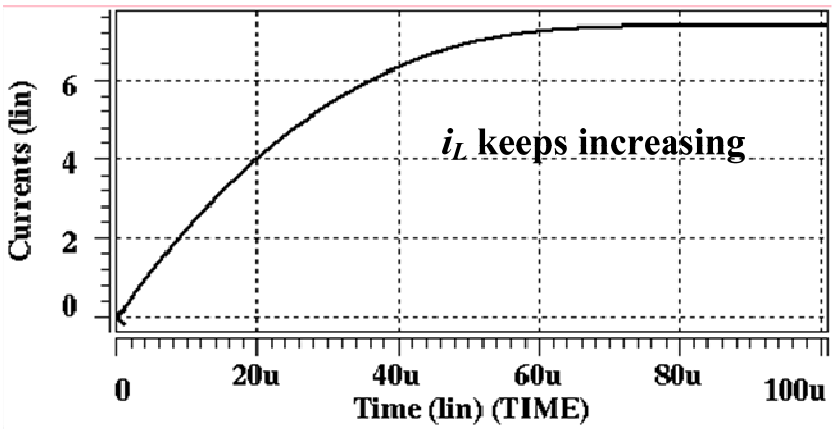
(a)



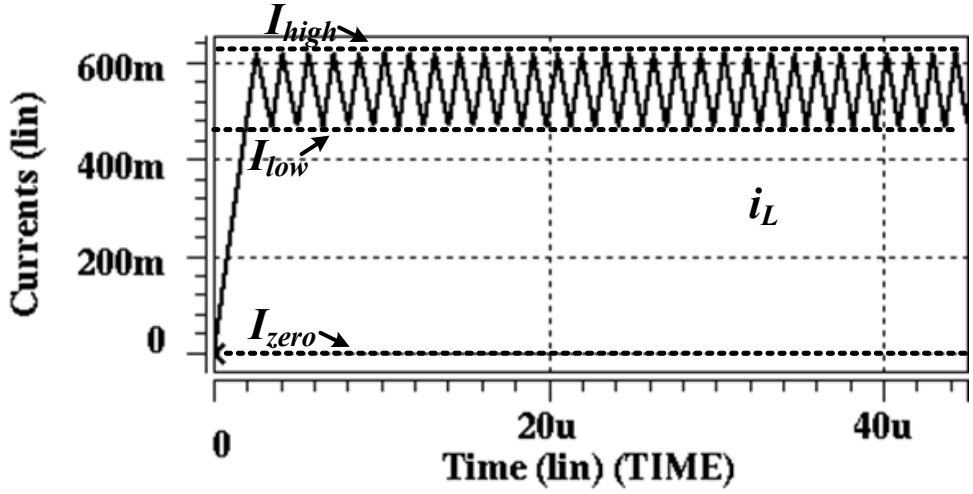
(b)

Figure 4.2.8 Simulated output voltage V_{out}, (a) without start-up control, and (b) with the proposed tri-band current-mode start-up control.

Figure 4.2.8 and Figure 4.2.9 illustrate the effectiveness of the tri-band current-mode start-up control. The simulation results show that, without any start-up control, the output voltage V_{out} of a buck-boost converter could not be charged up effectively (Figure 4.2.8a). Meanwhile, i_L continues increasing to an unacceptably high level (Figure 4.2.9a). With the proposed control scheme, V_{out} is charged up to the desired level successfully (Figure 4.2.8b) and the inductor current i_L is well controlled within the well-defined current bands (Figure 4.2.9b).



(a)



(b)

Figure 4.2.9 Simulated inductor i_L, (a) without start-up control, and (b) with the proposed tri-band current-mode start-up control.

4.2.3 Adaptive Digital Hysteresis Control

When V_{out} experiences very large dynamics and is out of sliding mode voltage band, an adaptive digital hysteresis voltage-mode control takes into effect. In this design, we choose V_{low} and V_{high} to be 3-bit LSB below and above the reference level, respectively. Instead of regulating V_{out} along the sliding surface, the controller immediately turns off (on) the charging path, forcing V_{out} to drop (rise) back to the sliding mode range in the fastest manner.

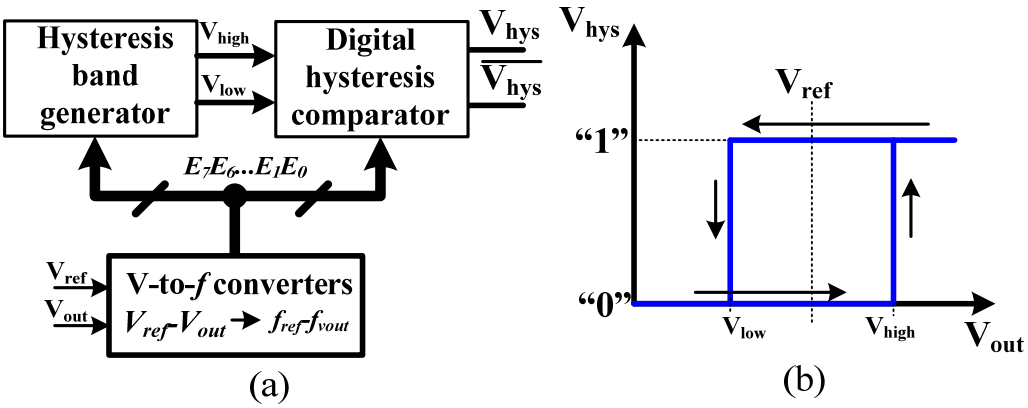


Figure 4.2.10 (a) Block diagram, and (b) control mechanism of digital hysteresis voltage-mode control.

Figure 4.2.10 illustrates the block diagram of the digital hysteresis control and its control mechanism. The V-to-*f* converters detect the regulation error between V_{out} and V_{ref}, and outputs corresponding 8-bit digital error signals $E_7...E_0$. The hysteresis band generator then adaptively generates the upper and lower limits (V_{high} and V_{low}) of the hysteresis control window. Meanwhile, the output of a digital hysteresis comparator V_{hys} is also triggered when V_{out} exceeds V_{high} and V_{low}. Here, we assume that in the hysteresis voltage-mode, the output voltage ripple ΔV_{out} is dominated by the equivalent series resistance (ESR) of the filtering capacitor C_{out}. The hysteresis control can then be utilized to adaptively control the current ripple, which will be expressed as

$$\Delta i_L = \frac{\Delta V_{out}}{ESR} = \frac{V_{high} - V_{low}}{ESR}. \tag{4.16}$$

This reflects an attractive feature that the current ripple and thus the switching noises can be adaptively controlled by adjusting the hysteresis window.

4.3 System Architecture & Circuit Implementations

4.3.1 Closed-Loop System Architecture

Figure 4.3.1 shows the closed-loop system block diagram and timing diagram of the design, respectively. In the start-up period, a current-mode hysteresis start-up controller adaptively strikes a balance between the charging speed and the peak inductor current. In steady state, a modified digital sliding-mode controller provides robust transient control and accurate regulation, with scalable power consumption for high efficiency. In large transient scenarios, an adaptive hysteresis controller offers fast transient regulation with the capability of adaptively controlling the current ripple.

The power stage of the converter in Figure 4.3.1 usually operates in two states. During State 1 (charging state), both M_{pl} and M_{nr} are on. The voltage across the inductor L is equal to V_{in}. The inductor is charged up with a slope of V_{in}/L until DT expires. Here D is the duty ratio determined by the controller. During State 2 (discharging state), M_{pl} and M_{nr} are switched off, whereas M_{nl} and M_{pr} are turned on. The voltage across the inductor L is then equal to $-V_{out}$. The inductor is discharged with a negative slope of $-V_{out}$/L. The current is delivered into C_{out} and R_O in this state. From (2), the voltage conversion ratio is calculated as: $M=V_{out}/V_{in}=D/(1-D)$. Obviously, when D is higher than 1/2, a step-up conversion is achieved. Otherwise, the converter functions as a step-down converter. At very light load, the inductor current decreases and the converter can seamlessly go into DCM operation for power saving.

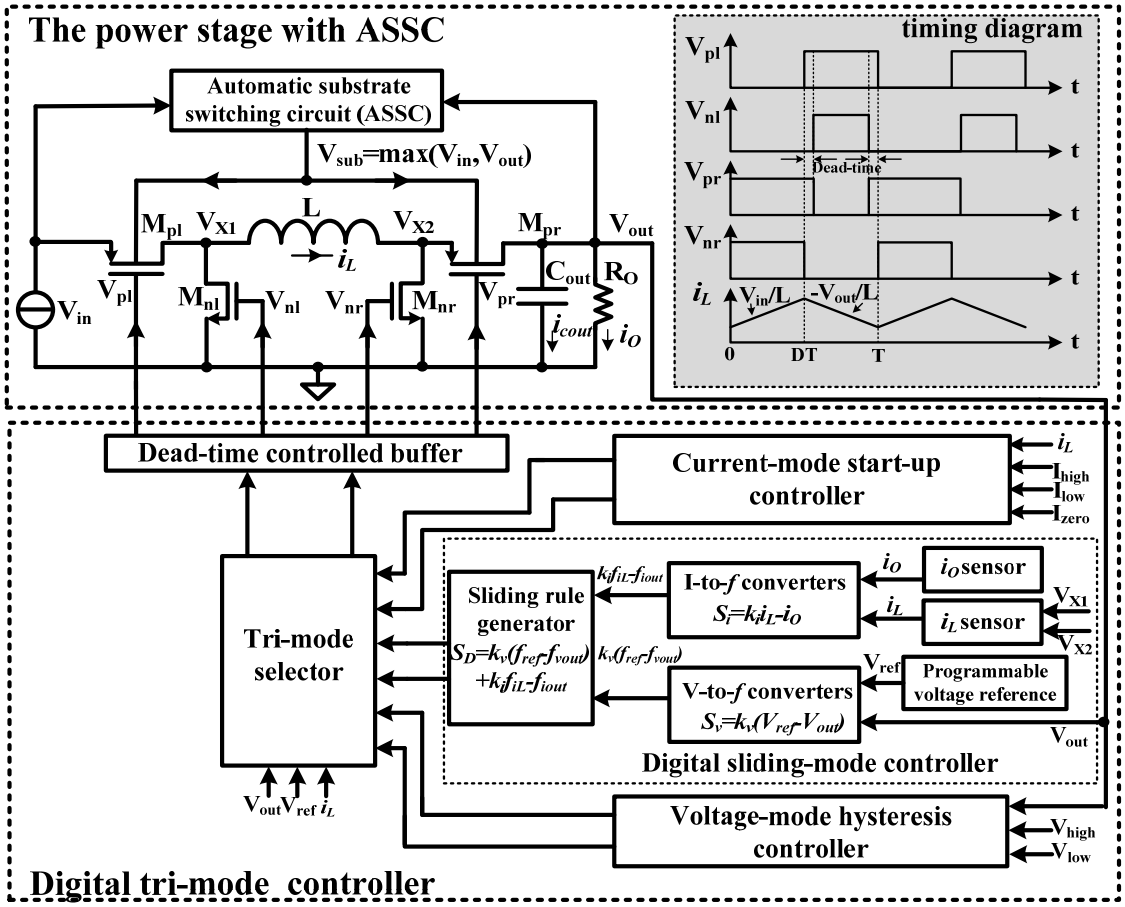


Figure 4.3.1 Block diagram of the proposed buck-boost converter.

4.3.2 Automatic Substrate Switching Circuit (ASSC)

In CMOS fabrication technologies, single-well (either N-well or P-well) process costs much less than twin or tri-well CMOS or BiCMOS processes. Figure 4.3.2 shows the cross section of one n-well CMOS process. V_{B1} is the n-well biasing voltage for pMOS transistor substrate and V_{B2} is the p-substrate biasing voltage for nMOS transistor. To prevent the conduction of the parasitic PN junction diodes (such as D_1 and D_2) and avoid latch-up, V_{B1} should be connected to the highest voltage of the chip, which is the supply voltage in most cases. Similarly, V_{B2} should be connected to the lowest voltage of the chip, which is usually the ground.

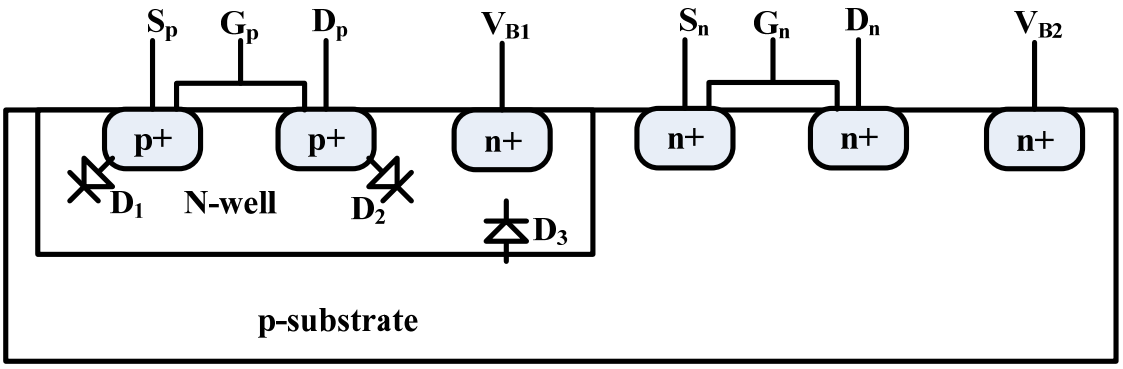


Figure 4.3.2 Cross section of n-well CMOS process.

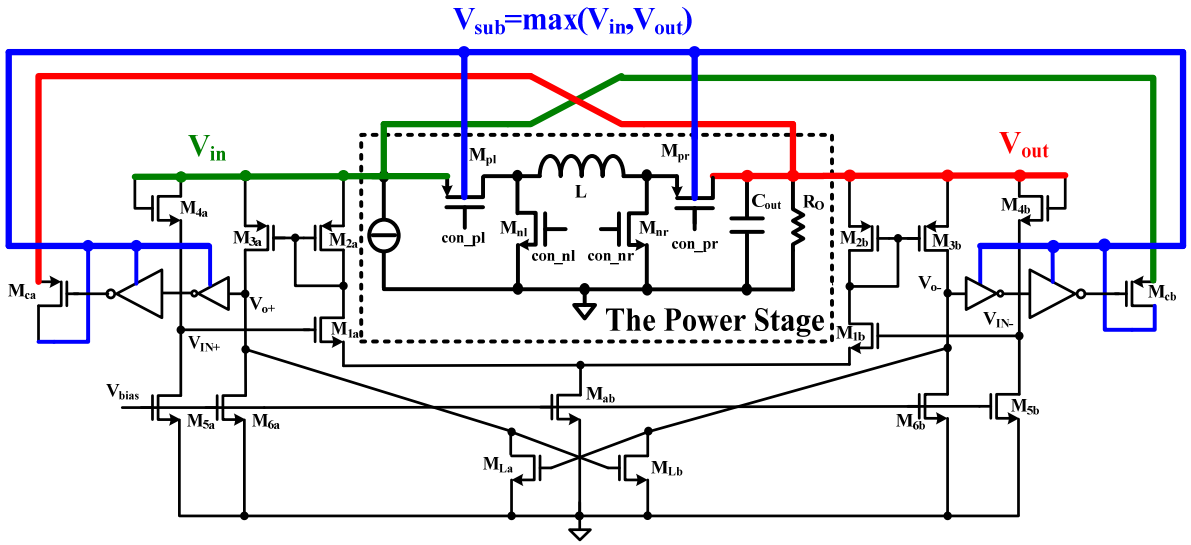


Figure 4.3.3 Schematic of automatic substrate switching circuit.

As the fabrication technology enters the nano-era, leakage current becomes a serious problem, especially when the substrate voltage is improperly handled. This is especially critical for the systems adopting variable power supplies such as DVS-enabled systems. Given that the power transistors are usually bulky, this leakage can cause large power loss, and thus degrades the efficiency. More seriously, potential latch-ups can cause fatal damages on silicon chips. Hence, extreme caution should be given when the substrate biasing voltage is variable. As shown in Figure 4.3.3, in this design, the large pMOS power transistors M_{pl} and M_{pr} are indeed facing

these problems, because V_{out} can be either higher or lower than V_{in} depending on different voltage conversion manners and the substrates of those power transistors should not be constantly connected to either V_{in} or V_{out}.

To solve this problem and keep the design compatible with low-cost fabrication process, we propose an automatic substrate switching circuit (**ASSC**). Figure 4.3.3 shows the schematic of the proposed circuit. The ASSC compares V_{in} to V_{out} and automatically selects the higher one to bias the pMOS substrates. When V_{in} and V_{out} differ with a large voltage margin, this voltage difference will be amplified between V_{o+} and V_{o-}. If V_{in} is larger, V_{o+} will be high. M_{ca} will be off and M_{cb} will be on, connecting V_{in} to the output. Hence, the output voltage will be V_{in}. Otherwise, M_{cb} will be off and M_{ca} will be on and connect V_{out} to the output. As a result, V_{sub} will always take the higher voltage between V_{in} and V_{out}. Here, M_{ca} and M_{cb} are two large pMOS transistors with M_{ca} source powered by V_{out} and M_{cb} source powered by V_{in}.

When V_{in} and V_{out} are very close, M_{ca} and M_{cb} might work in the saturation region, which causes a voltage drop over the drain and source. Thus, V_{sub} will be much lower than the desired level. In order to completely turn on/off M_{ca} and M_{cb}, two buffers and M_{La} and M_{Lb} are inserted. M_{La} and M_{Lb} act as a latch to drive V_{o+} and V_{o-} either to ground or supply. The buffers powered by V_{sub} can help speed up the switching speed of M_{ca} and M_{cb}.

4.3.3 Self-Biased Current Sensor

During the current-mode start-up state, instant current sensing of the inductor current i_L is critical. Current sensor circuits are thus needed. Traditional implementations of current sensing employ either current sensing resistors [Forghani-02] or integrators [Ma-04] [Midya-01]. However, it is very difficult to integrate a low resistance but high power rating resistor accurately on-chip. The approach involving integrators requires complicated analog circuits and dual-rail

power supplies [Ma-04] [Midya-01]. In addition, both approaches consume relatively large power to affect the power efficiency.

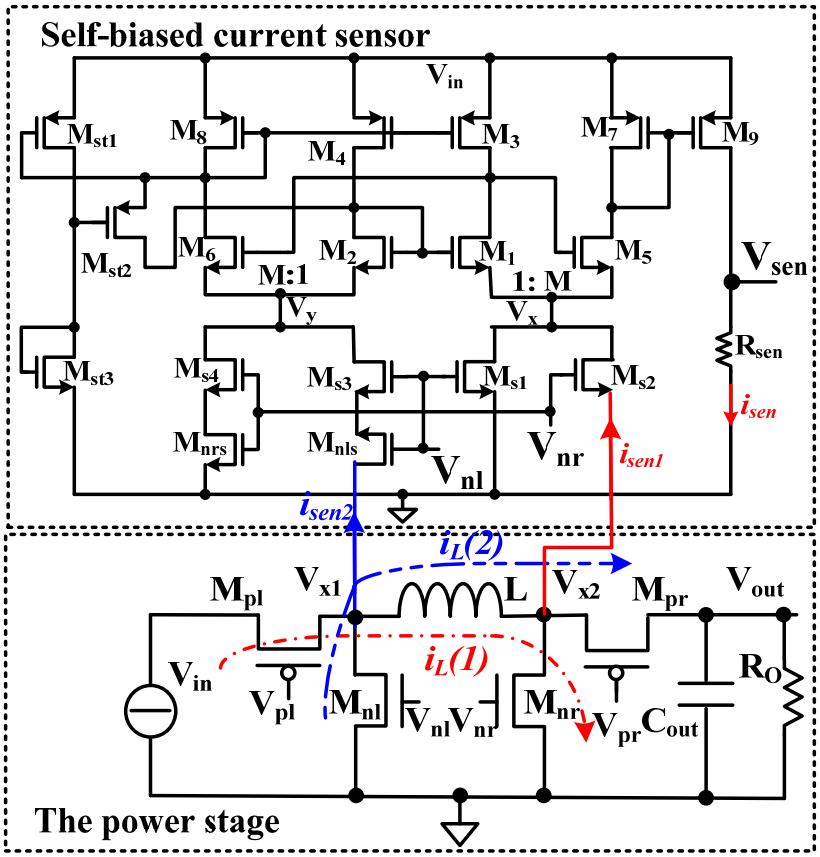


Figure 4.3.4 Schematic of the self-biased transistor-scaling current sensor.

Tailored for low-power VLSI implementations, we propose a self-biased current sensing circuit based on transistor scaling techniques [Ki-98c] [Ma-02a] [Ma-03a]. As shown in Figure 4.3.4, in State 1, both M_{pl} and M_{nr} in the power stage are on. The inductor is charged up. In the sensing circuit, the switches M_{nl}, M_{nls}, M_{s1}, and M_{s3} are all off, while M_{nr}, M_{nrs}, M_{s2}, and M_{s4} are all on. By turning on the switch M_{s2}, V_x is connected to ground through M_{s2}. i_L flows through M_{nr}, and according to the ratio of the transistors, we have $I_{Ms2}=I_{Ms1}=I_{Mnrs}=i_L/N$, and $I_{Mnr}=i_L(N+1)/N$, such that V_y is forced to be the same as V_x, and current sensing of M_{nr} can be

achieved. At the same time, with $(W/L)_3=(W/L)_4$, $I_{M3}=I_{M4}$ are injected into M_1 and M_2. Now M_1, M_2: M_5, M_6=1: M, such that M_1+M_5 are matched to M_2+M_6, and current (M+1) I_{M1} is injected into nodes V_x and V_y, which will also forces V_y to be equal to V_x, and the current ratio I_{dx}: I_{dy} is

$$[i_L + (M+1)\cdot I_{M1}] : [(M+1)\cdot I_{M1}] = N:1, \tag{4.17}$$

so that $I_{M1}=i_L/[(M+1)(N-1)]$. The sensed current is mirrored by M_9 that can be scaled with the ratio of $(W/L)_9/(W/L)_7$, and a sensed voltage proportional to the inductor current is developed across the sensing resistor R_{sen}, the final sensing current is

$$i_{sen} = \frac{(W/L)_9}{(W/L)_7}\cdot\frac{M}{M+1}\cdot\frac{1}{N-1}\cdot i_L, \tag{4.18}$$

and the power consumption is

$$P_{sen} = i_{sen}^2\cdot R_{sen} = \left(\frac{(W/L)_9}{(W/L)_7}\cdot\frac{M}{M+1}\cdot\frac{i_L}{N-1}\right)^2\cdot R_{sen}. \tag{4.19}$$

If the ratio N is very large, power consumption of the current sensing circuit can be reduced significantly, compared to the case of using sensing resistors, while still maintaining a much better sensing resolution. The inductor current sensing during the discharging phase-State 2 operates in a similar manner. It should be noted that the self-biased current sensor has two metastable states, and a start-up circuit is thus needed.

To evaluate the current sensing performance, Figure 4.3.5 shows simulated sensing voltage with reference to the inductor current i_L. The sensing voltage is linearly proportional to i_L. In this design, we have $i_{sen} : i_L = 1 : 3000$ and R_{sen}=3KΩ. Accordingly, power consumption of the current sensing circuit is reduced by 150 times, compared to the case of using 50-mΩ sensing resistor. The sensing accuracy is 98.4%.

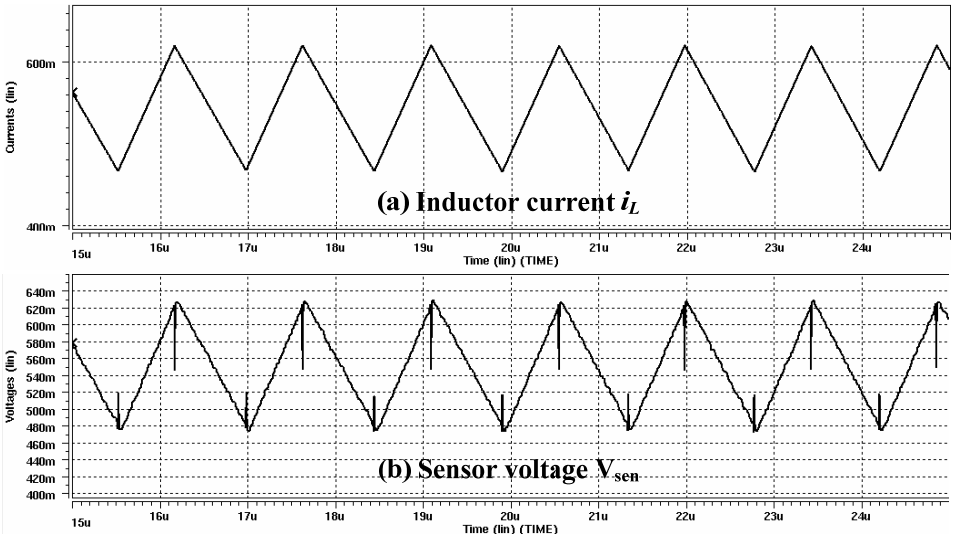


Figure 4.3.5 Simulated self-biased current sensor waveforms: (a) inductor current, and (b) sensing voltage.

4.3.4 Ring Oscillator Based V-to-f Converter

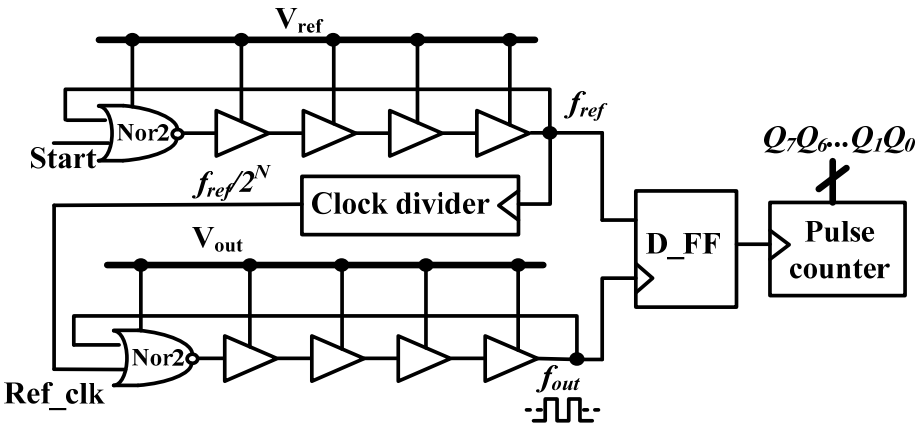


Figure 4.3.6 Schematic of the ring oscillator based V-to-*f* converter.

The output signal of the converter is analog. In order to implement the digital control, an analog to digital (A/D) converter is required. Traditional A/D converter is not preferred, because it occupies large silicon area, consumes substantial power and is very sensitive to noise. Recently, ring-oscillator and delay-line A/D converters have been reported in literature [Kim-01] [Ma-06b]

[Zhang-04]. Compared with the traditional ones, these designs are more area and power efficient, since both of them utilize basic digital logic gates as building blocks.

Compared to the delay-line based design, ring oscillator based A/D converter is even more area efficient because the delay elements are re-utilized even within a single switching cycle. To detect the regulation error between the output V_{out} and the desired reference voltage V_{ref}, two identical ring oscillator A/D converters are used as the V-to-*f* converter, as shown in Figure 4.3.6. The ring oscillator A/D converter consists of one NOR gate, four delay cells and one pulse counter. Each delay cell simply includes two inverters. The pulse counter is an asynchronous positive edge triggered N-bit counter. Note that the NOR gate and the delay cells are powered by V_{out}, which is the output of the SC power converter. When the "Start" signal is HIGH, the loop remains at a static state and the outputs of delays cells keep LOW. When the "Start" signal goes LOW, the loop oscillates and a series of pulses are generated at V_{ADC} with an oscillating frequency of f_{out}. By examining $Q_{N-1}...Q_0$ at the output of the counter, the voltage V_{out} is presented in form of f_{out}, as (4.8).

The upper ring oscillator, powered by V_{ref}, generates a clock signal with a frequency of f_{ref}. This clock passes through a clock divider and generates another clock signal Ref_clk with a frequency equal to $f_{ref}/2N$, where N is the number of bits in the clock divider. Ref_clk is then used as the Start signal of the second ring oscillator powered by the power converter's output voltage V_{out}. When Ref_clk is LOW, the second oscillator oscillates with a frequency of f_{out}, which drives the pulse counter to count the number of pulses in a fixed time period. Finally, the pulse counter outputs N-bit binary signals $Q_{N-1}…Q_0$. Based on $Q_{N-1}…Q_0$, the frequency difference $f_{ref} - f_{out}$ can be computed to implement the sliding control rule.

- If $V_{out} < V_{ref}$, then $Q_{N-1}...Q_0 <$ *'10 ... 0'*;

- If $V_{out} = V_{ref}$, then $Q_{N-1}...Q_0 =$ *'10 ... 0'*;
- If $V_{out} > V_{ref}$, then $Q_{N-1}...Q_0 >$ '10 … 0'.

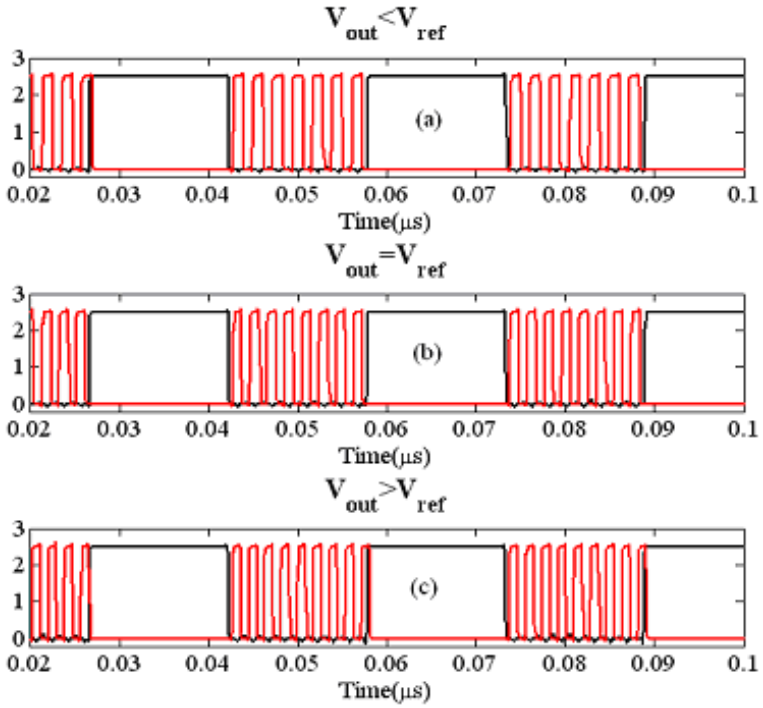


Figure 4.3.7 Simulated V-to-*f* converter, when (a) $V_{out} < V_{ref}$, (b) $V_{out} = V_{ref}$, and (c) $V_{out} > V_{ref}$.

Based on the value of $Q_{N-1}...Q_0$, the range of V_{out} can be determined and then the controller uses the information to regulate V_{out} at V_{ref}. Figure 4.3.7 demonstrates the simulated results with N = 4. In Figure4.3.7(a), when the reference clock is LOW, 7 pulses are counted during the interval. Therefore, $Q_3Q_2Q_1Q_0$ = '0111', which is smaller than '1000'. This agrees well with the statement. Similar analysis can be done when $V_{out} = V_{ref}$ and $V_{out} > V_{ref}$, where '1000' and '1001' pulses are found from Figure4.3.7 (b) and Figure4.3.7(c), respectively.

4.3.5 I-to-f Converters

The difference between the inductor current i_L and the output current i_o is calculated by the I-to-*f* converters circuit, as shown in Figure 4.3.8. Two identical I-to-*f* converters are used

here, in the upper *I*-to-*f* converter, the inductor current i_L flowing into M_1 is mirrored and scaled to M_2, M_3, M_4 and M_7 depending on the transistor ratio, M_5 and M_6 work as switches to charge and discharge the capacitor C_1. When the control signal reaches V_{high}, the hysteresis comparator changes state and the SR-Latch output will become high, which turns M_9 on and switches M_8 off, forcing M_5 off and M_6 on. The capacitor C_1 is then discharged. As a result, the control signal drops until it reaches the V_{low}, and the comparators will flip the state again and charge the capacitor C_1. In this design, the clock frequency is linearly proportioned to i_L, achieving the I-to-*f* conversion. The clock signal drives an 8-bit pulse counter, converting pulse signal into N-bit binary signals $Q_{N-1}...Q_0$. Similarly, the lower I-to-*f* converter in Figure 4.3.8 generates N-bit digital signals of output current.

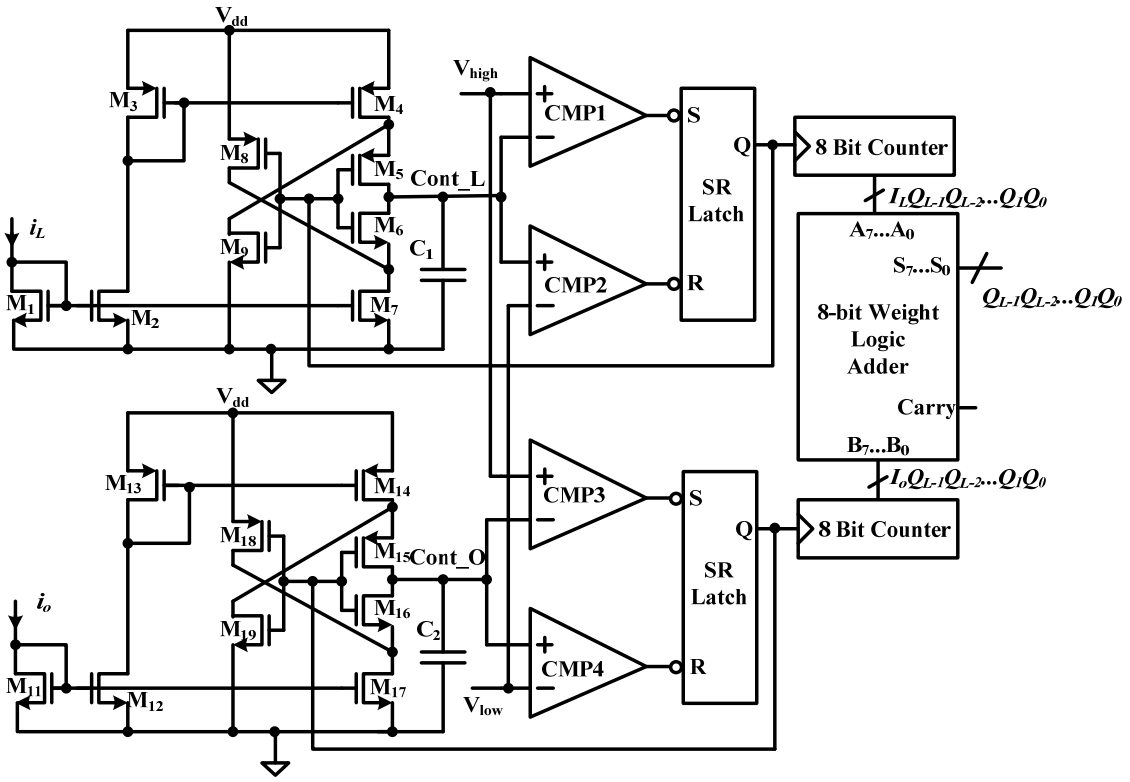


Figure 4.3.8 Schematic of the I-to-*f* converters.

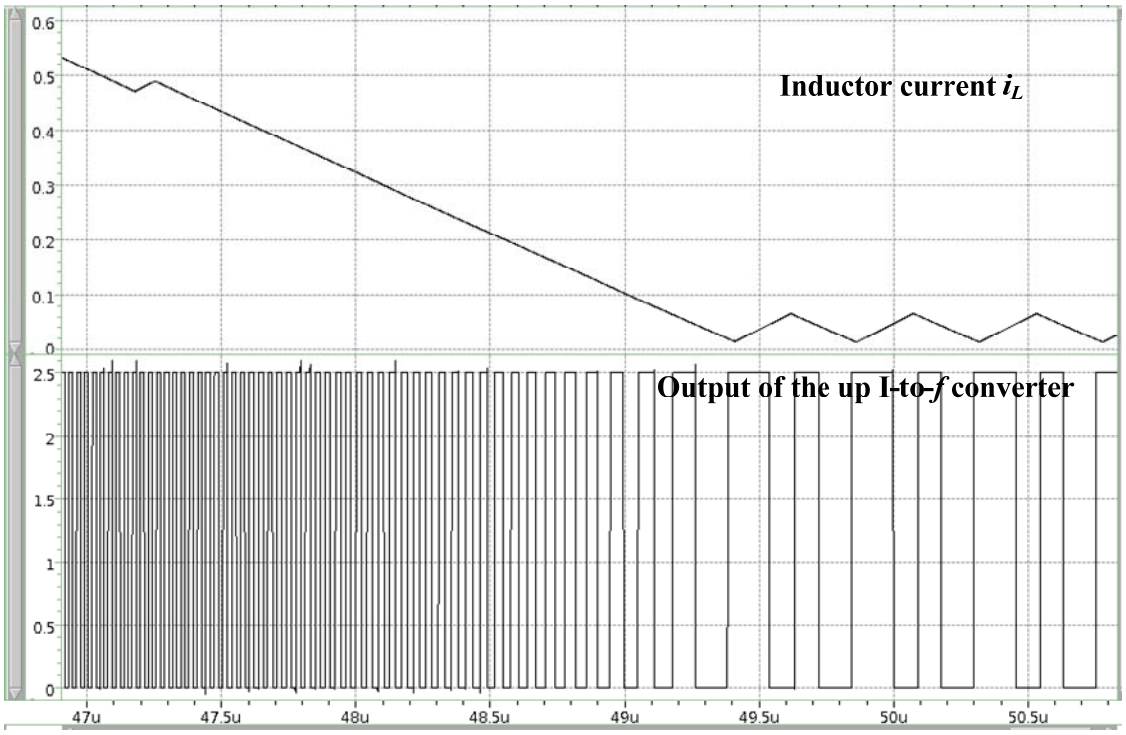


Figure 4.3.9 Simulation result of the clock frequency linearly proportioned to i_L.

Figure 4.3.9 is the simulation result shows the linear relation between the clock frequency and inductor current i_L. As we can see, when i_L drops, the corresponding clock frequency drops linearly, which verified our design.

4.3.6 Programmable Voltage Reference Generators

Figure 4.3.10 shows the schematic of the programmable voltage reference generator. Control signals $Q_2Q_1Q_0$ determine the actual reference level to be used based on the DVS voltage demand. An error amplifier controls the pMOS pass transistor with respect to the reference from an 8-to-1 decoder array. The low dropout regulator (LDO) then generates a voltage reference which powers the V-to-*f* converters in Section 4.3.4. Since the load of the LDO is very low (the supply input of the reference ring oscillator), this LDO design is simple and standard, consuming very small silicon and power.

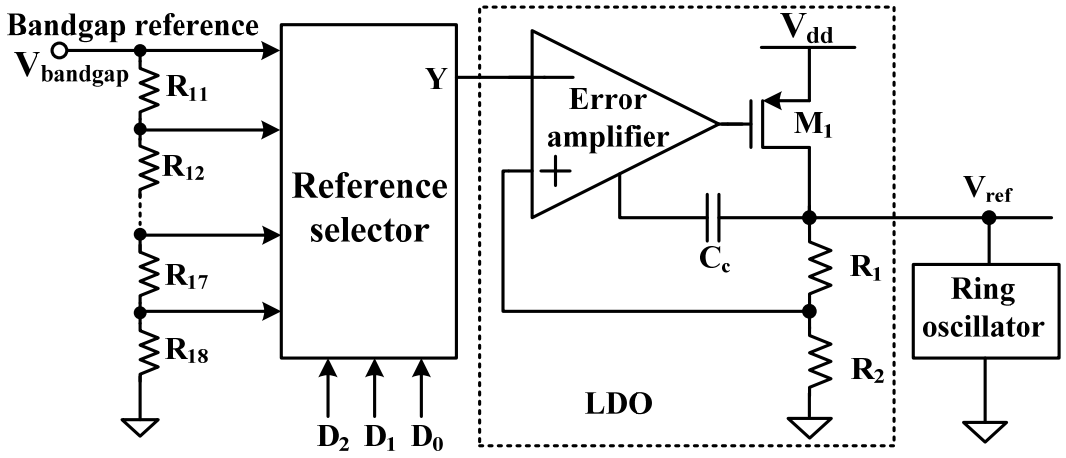


Figure 4.3.10 Schematic of programmable voltage reference generator.

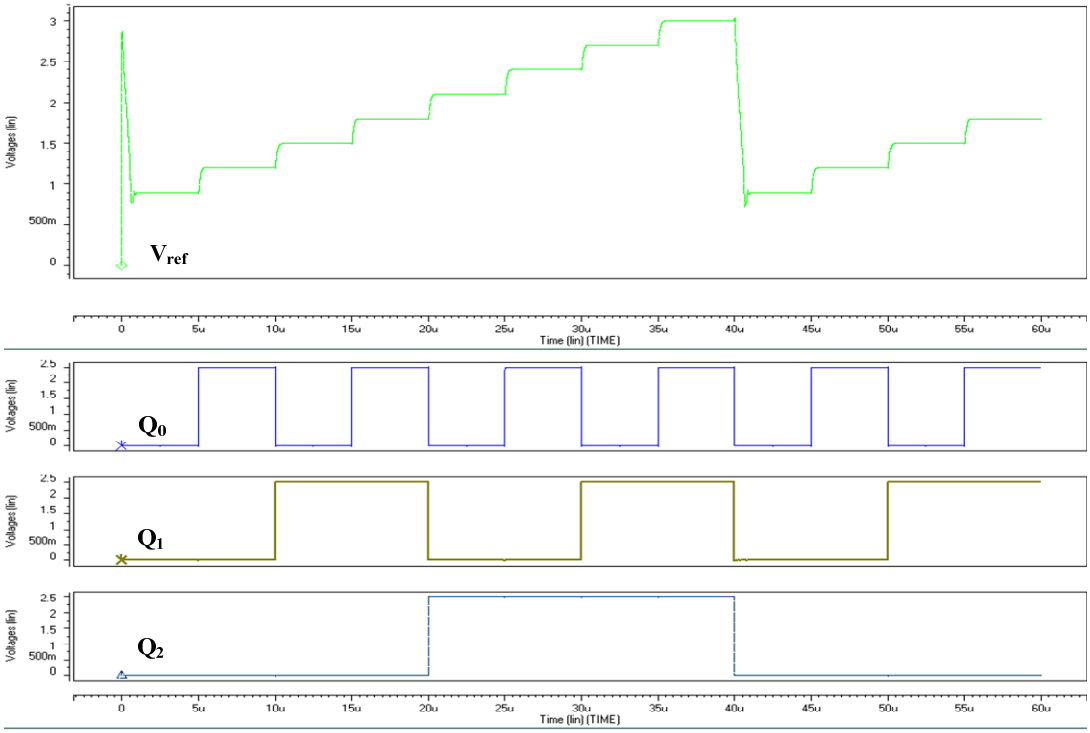


Figure 4.3.11 Simulation result of programmable voltage reference generator.

The simulated output of the programmable voltage reference generator is shown at Figure 4.3.11. When we sweep control signals $D_2D_1D_0$ from "000" to "111", the output V_{ref} changes from 0.9 V to 3V at 0.3 V step.

4.4 Experimental Verifications

4.4.1 Steady-State Measurements

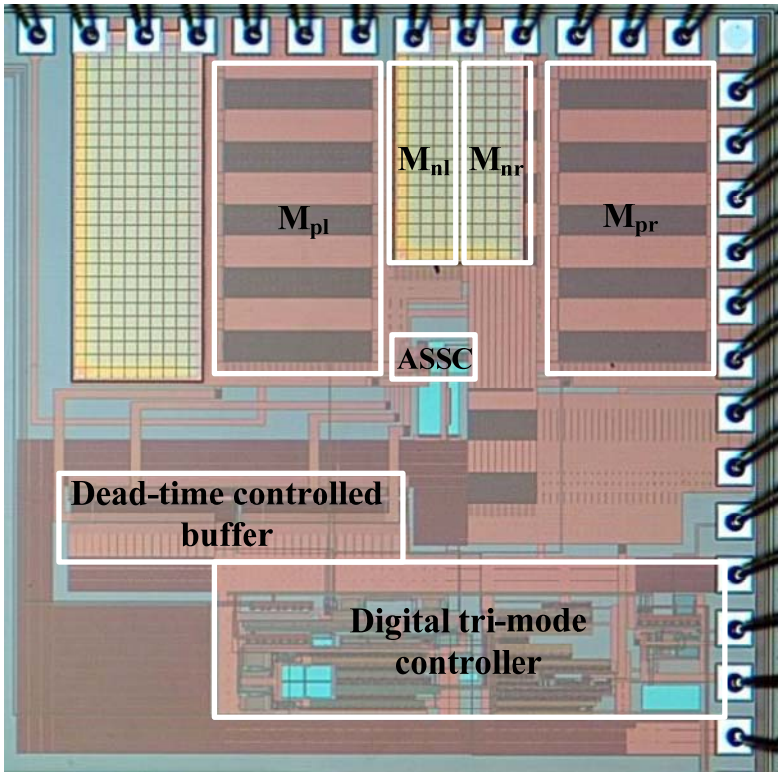


Figure 4.4.1 Chip micrograph.

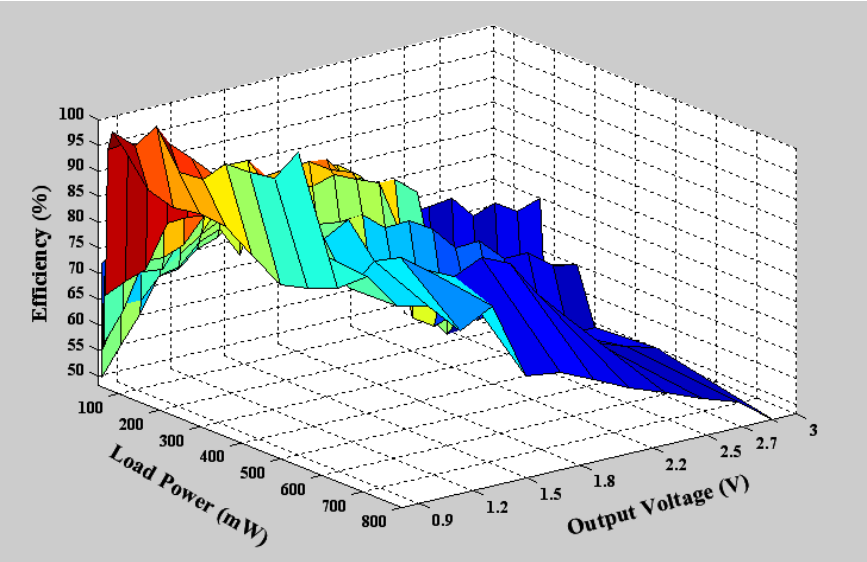
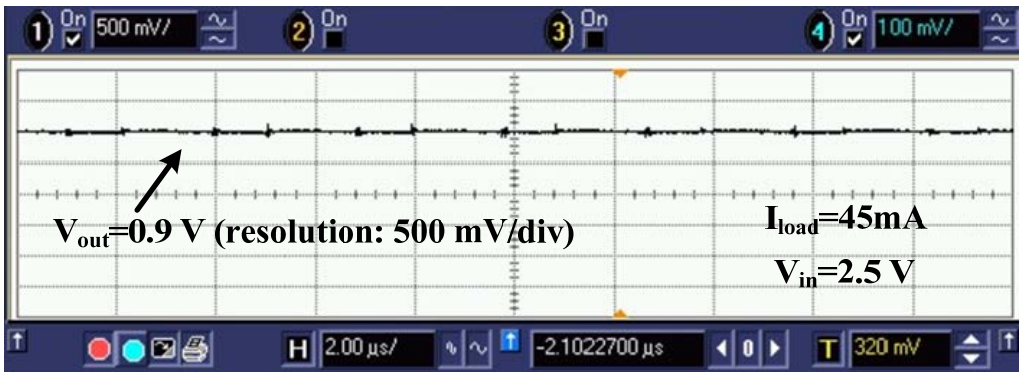


Figure 4.4.2 Measured efficiency versus output voltage and load power.

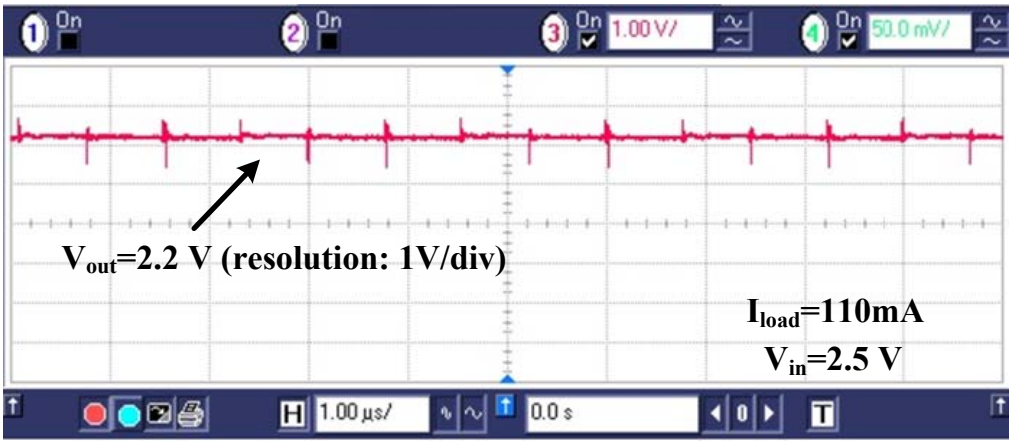
The proposed converter was designed and fabricated with TSMC 0.35μm digital N-well CMOS process. Figure 4.4.1 shows the chip micrograph of the entire system. The active die area is 1.3 mm^2, while the controller occupies 0.63 mm^2 silicon. In this design, we choose the inductor and filtering capacitor values as 10 μH and 10 μF, respectively, where the ESR of the capacitor is 350 mΩ. The converter provides a well-regulated output variable from 0.9 to 3.0 V. With a line regulation of 20.4 mV/V, the converter robustly functions when the supply voltage frequently varies between 1.6 and 3.3V.

The measured power efficiency of the converter is shown in Figure 4.4.2. It remains above 50% in the entire operating power range from 11 to 800 mW and a voltage range of 0.9 to 3.0 V. Because this proposed adaptively step-up/down converter is optimized for low power application, at 1.6V supply voltage, the maximum efficiency is measured as 96.5% at 0.9-V output and 45-mW load power.

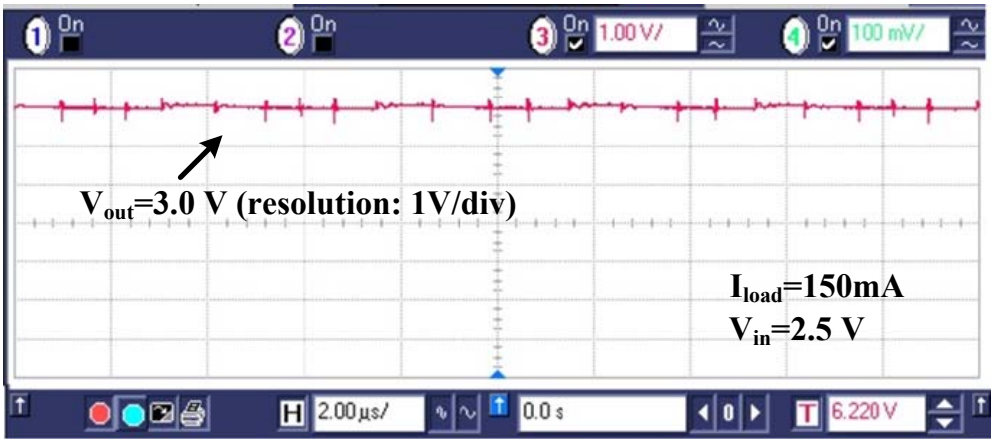
Figure 4.4.3 shows the measured steady-state power output, regulated at different preferred levels. With a nominal supply voltage V_{in} of 2.5 V, Figure 4.4.3a achieved the regulated output V_{out} at the lower bound of the regulation: 0.9V, while Figure 4.4.3c demonstrated the regulated output V_{out} at the higher bound of the regulation – 3.0V. For these two cases, the converter performs step-down and step-up conversion, respectively. Note that this converter can continuously provide output power at any level between the two bounds. Figure 4.4.3b shows the case when V_{out} is regulated at 1.8 V as an example. With all the cases, the peak-to-peak ripple voltage is controlled below ±10 mV, due to the effectiveness of digital sliding control. Figure 4.4.4 shows one typical ripple performance of the converter with reference to the inductor current i_L.



(a)



(b)



(c)

Figure 4.4.3 Steady-state V_{out} at (a) 0.9 V for step-down conversion, (b) 2.2 V for step-down conversion, and (c) 3.0 V for step-up conversion.

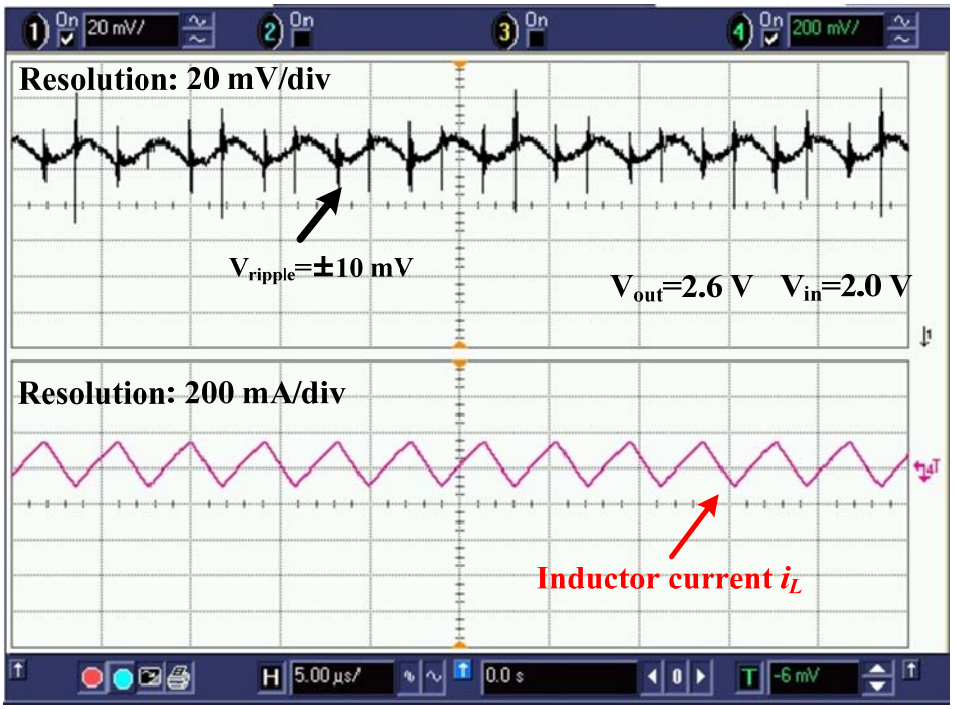


Figure 4.4.4 Measured output ripple voltage (upper) and inductor current i_L (lower).

4.4.2 Automatic Substrate Switching Circuit Measurements

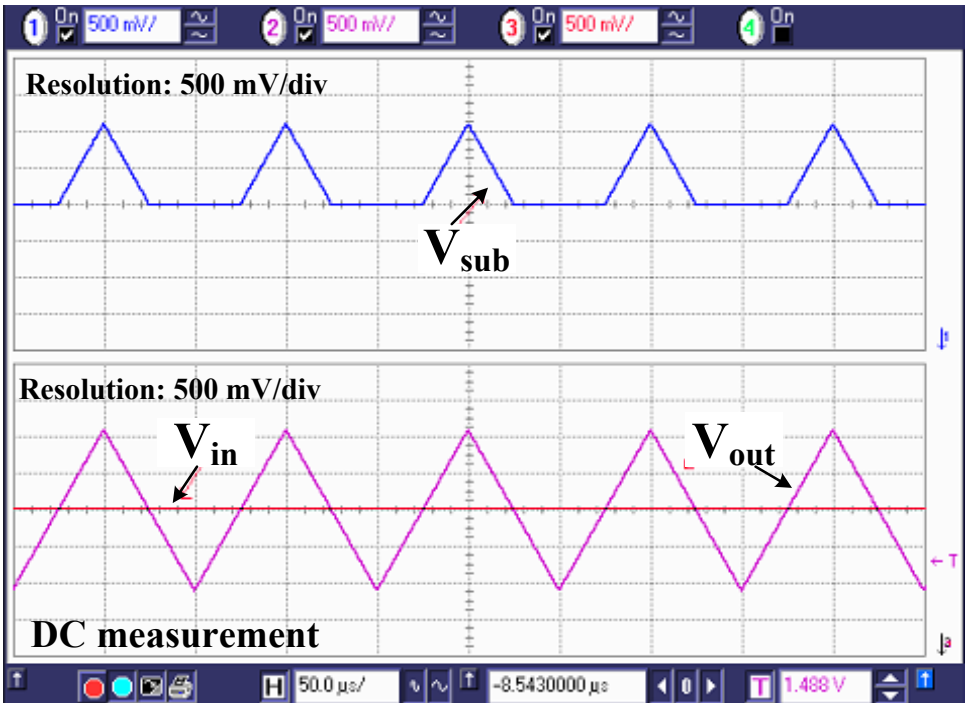


Figure 4.4.5 Measured DC performance of the ASSC.

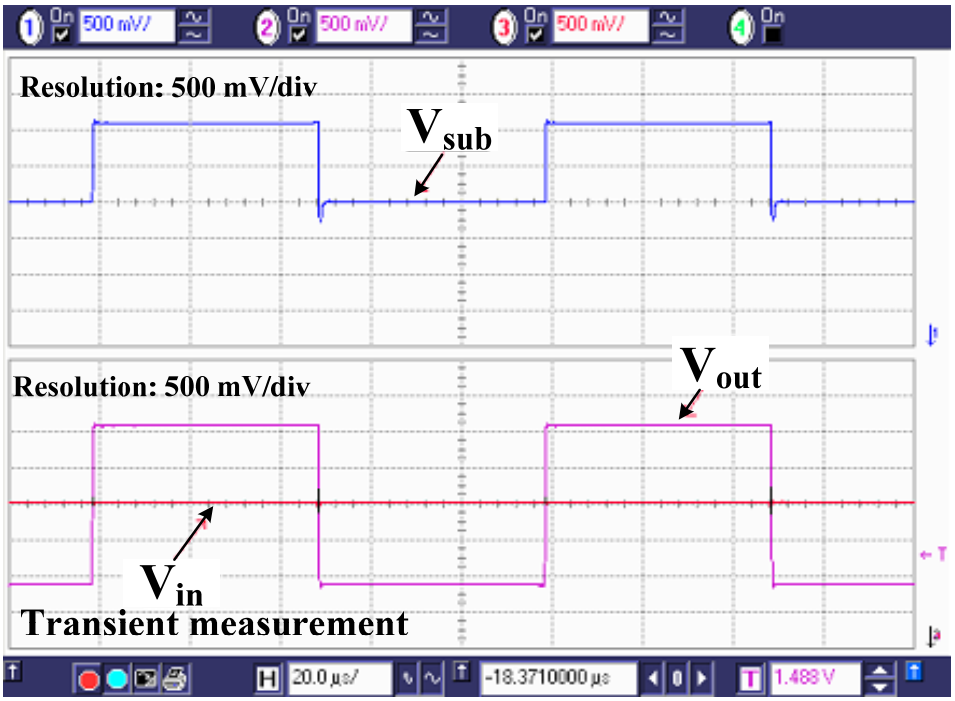


Figure 4.4.6 Measured transient performance of the ASSC.

The ASSC circuit was also individually tested. It only occupies 0.017 mm^2 area and consumes only 88 µW power. Experiment results are shown in Figure 4.4.5 and Figure 4.4.6. In DC measurement (Figure 4.4.5), V_{in} is fixed at 2.2 V, while V_{out} sweeps periodically from 1.1 to 3.3 V as a triangular wave. The higher voltage is always chosen for V_{sub}. In transient measurement (Figure 4.4.6), a square wave is used for stricter set-up. The maximum switching speed of 2.2 V/µs is obtained.

4.4.3 DVS /Load Transient Measurements

Figure 4.4.7 shows the dynamic voltage tracking performance for DVS applications. With V_{in} at 2.5V, V_{ref} suddenly steps up and down between 1.2 to 2.2 V. It takes the converter 37 µs and 150 µs to trace a 1-V step-down and to a step-up change, respectively.

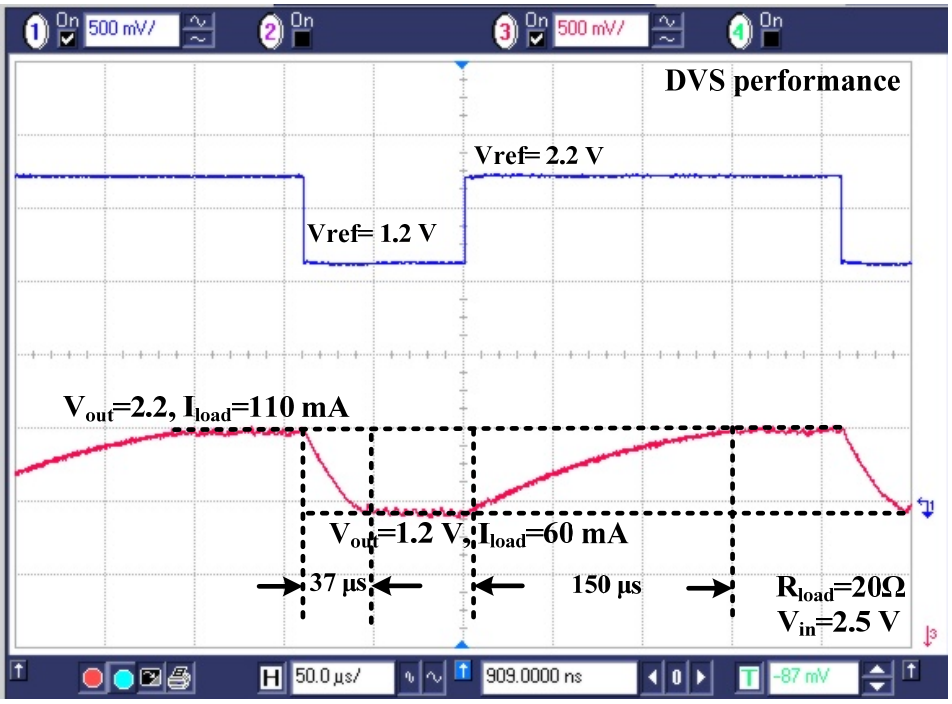


Figure 4.4.7 Measured dynamic performance for DVS: (upper) V_{ref} steps down from 2.2 to 1.2 V, (lower) measured V_{out}.

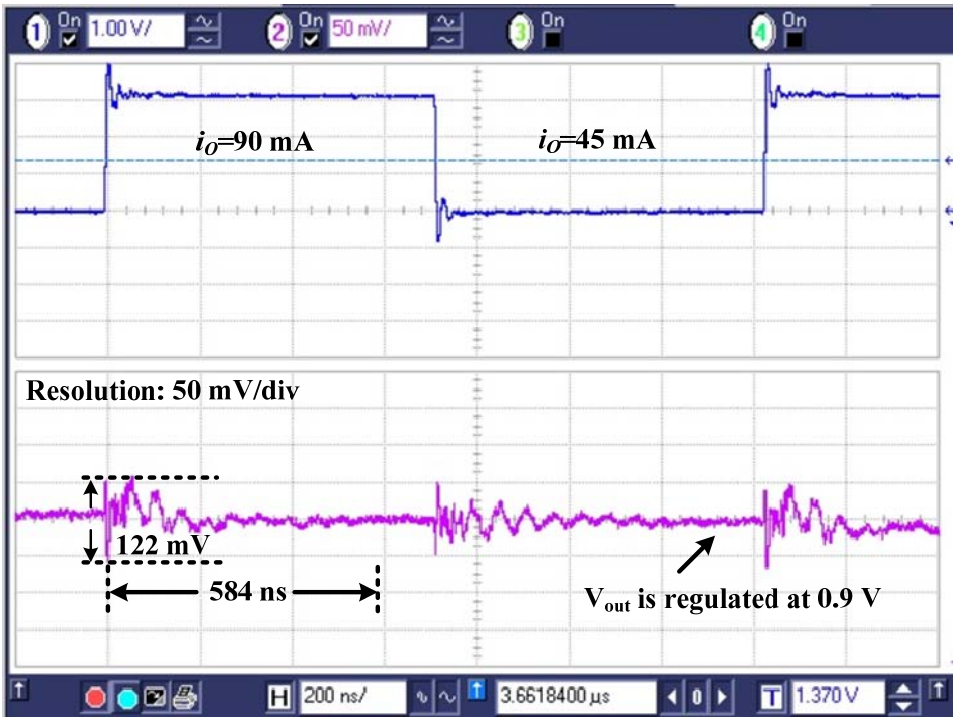


Figure 4.4.8 Measured load transient response: (upper) load current i_O steps up and down between 45 and 90 mA, (lower) measured output voltage V_{out}.

Figure 4.4.8 shows the measured load transient performance. A 100% load current i_O steps up and down between 45 to 90 mA in the upper trace to model the worst case load change in real applications. A close-up look at output voltage V_{out} in the lower trace demonstrates a smooth and stable transient performance. The output voltage variation is controlled below 110 mV with a settling time of less than 600 ns.

Table 4. 1 Performance comparison with prior arts

Designs		[Namgoong]	[Kim-01]	[Hiraki]	[Ma-04]	[Chui]	[Ma-06a]	**This work**
Steady-State Performance	Conversion manners	step down	step down	step down	step down	step down	step down	step-up step-down
	V_{out} (V)	1.5~3.5	1.1~2.3	1.3~2.2	0.9~2.5	0.2~3.0	0.8~2.2	0.9~3.0
	V_{in} (V)	5V	2.5V	2.7~3.3	2.9~3.9	3.3V	3.0V	1.6~3.3
	Efficiency (max)	93%	95%	87%	93.7%	92%	92%	96.5%
	Power range (mW)	200	350	300	450	625	484	800
Dynamic Performance	Load response(μs)	N/A	10	N/A	40	50	N/A	0.6
	Tracking speed (μs/V)	~ 6000	80	2000	13.75	50	9.5	37
Fabrication Information	Total area (mm^2)	13.66	1.43	0.42*	2.31	3.78	3.01	1.3
	Controller area (mm^2)	N/A	0.35	N/A	0.54	0.78	0.55	0.63
	CMOS process(μm)	0.8	0.25	0.2	0.5	0.6	0.35	0.35

* 7 series regulators are not counted.

Finally, Table 4.1 compares this work with prior arts. The comparison focuses on the three most important design aspects: the steady-state operation, the dynamic transient and the fabrication information. The use of step-up/down conversion topology allows this work to achieve the most flexible input/output voltage conversion. The proposed TBTM control and circuit designs make the converter robust to large input voltage variations with high efficiency in the largest power range. The effectiveness of both sliding and hysteresis controls contribute to the fastest load response and very competitive DVS transient in this design. The design is also proven to be area and cost efficient based on the process and silicon area data. Note that all the

prior arts are limited to step-down conversion only, because of the control difficulties and single-well CMOS process. ASSC technique simply removes the process constraint with simple and low cost implementation.

4.5 Conclusions

In this chapter, we propose a new integrated adaptive buck-boost power supply with digital sliding-mode digital control and automatic substrate switching technique. The digital sliding-mode controller allows the converter to operate with fast start-up, load and DVS transients and superior line and load regulations. The converter precisely provides a variable and adjustable power supply voltage, ranging from 0.9 to 3.0 V and from 11 to 800 mW. It operates robustly even when the input supply varies from 1.6 to 3.3 V. The design provides a competitive solution to the new-generation, robust and adaptive power supply designs.

CHAPTER 5 DIGITAL SIMO STEP-UP/DOWN POWER CONVERTER FOR DVS-ENABLED MULTICORE SYETEMS

This chapter presents a digital integrated single-inductor multiple-output (SIMO) converter, tailored for DVS-enabled multicore systems. In this design, each power output employs a step-up/down voltage conversion, thereby enabling a wide range of variable output voltage. This is beneficial to dynamic voltage scaling (DVS) techniques that are in high demand by low-power multicore systems. With a multi-mode control algorithm, DVS tracking speed and line/load regulation are significantly improved, while the converter still retains low cross regulation. Designed with a 180-nm digital CMOS process, the converter precisely provides three independently variable power outputs from 0.9 to 3.0 V, with a total power range from 33 to 900 mW. A very fast load transient response of 3.25 μs is achieved, in response to a 67.5-mA full-step load current change. The converter can operate robustly at any input supply level from 2.0 to 3.3 V, leading to a superior line regulation of 4.6 mV/V. The design provides a cost-effective solution to robust, fast-transient, DVS-compatible, on-chip power supplies.

5.1 Design Motivations

Driven by the technologies of superscalar pipelining, cache coherency, simultaneous multithreading (SMT) and so on, the emergence of sophisticated multicore platforms has led to their establishment as the preferred architectures in a plethora of advanced applications. Such applications tend to demand large throughputs at high efficiencies, causing these multicore data processors to operate using massively paralleled and pipelined structures. The result of catering to such demands, while simultaneously satisfying the requirements of highly on-chip silicon integration, has led to very high power densities and sharp thermal gradients. Under critical conditions of extremely heavy workload, a multicore system can even enter into situations of thermal runaway and may eventually break down [Isci-06]. Therefore, this urgent power crisis has been identified as a long-term **Grand Challenge** by *ITRS* [ITRS-09].

In order to achieve optimal operation performance in these power-hungry systems, equally advanced power management techniques are urgently required. One such technique is dynamic voltage scaling (DVS) [Burd-00] [Calhoun-06] [Kwon-03] [Ma-04] [Ma-06a] [Nowka-02] [Weiser-94], in which variable power is delivered to each processor core based on its instantaneous workload. This technique is refined to tune in on voltages and frequencies of operation that allow all processes in the multicore system to complete 'just-in-time', thereby eliminating any slack periods. Hence, DVS techniques require underlying hardware, such as DC-DC converters, to adjust and deliver the desired power. As these techniques minimize power dissipation under the presumption of exploiting multiple or variable power sources, such an implementation would traditionally require many individual power converters. This leads to a bulky architecture, due to the use of large inductors that introduce serious EMI noise and large power switches that lead to significant silicon cost.

In order to overcome these drawbacks, this chapter presents a digital integrated single-inductor multiple-output (SIMO) step-up/down power converter. Such a converter seamlessly lends itself for efficient power management of DVS-enabled multicore applications, through the use of a digital hybrid control schemes. In this novel control scheme, the outputs of the SIMO converter are controlled based on the instantaneous static power demands and dynamic power changes sensed by digital power sensing and processing modules. With each output capable of providing a well-regulated and variable voltage to individual cores, exact load power demands can be satisfied with high power efficiency. The multi-mode control algorithm also provides prompt DVS tracking response and significantly enhances line/load regulations, while still retaining low cross regulation. Such a synergetic control algorithm, coupled with the advantages of a cost-effective SIMO converter structure, provides an ideal power management solution for a multicore platform. The rest of the chapter is organized as follows. The proposed digital multi-mode control scheme is elaborated in Section 5.2, along with a detailed discussion about the SIMO power stage design, the whole closed-loop system design, and parallel start-up techniques. The detailed circuit implementations are discussed in Section 5.3. Section 5.4 verifies the circuit functionality and control. Finally, we summarize this work in Section 5.5.

5.2 System Architecture & Control Algorithms

5.2.1 Closed-Loop System Architecture

Figure 5.2.1 shows the block diagram of the closed-loop system architecture of our proposed single inductor triple-output power converter. It features a step-up/down power stage with multiple-and-variable-outputs and a feedback controller with embedded software control algorithms.

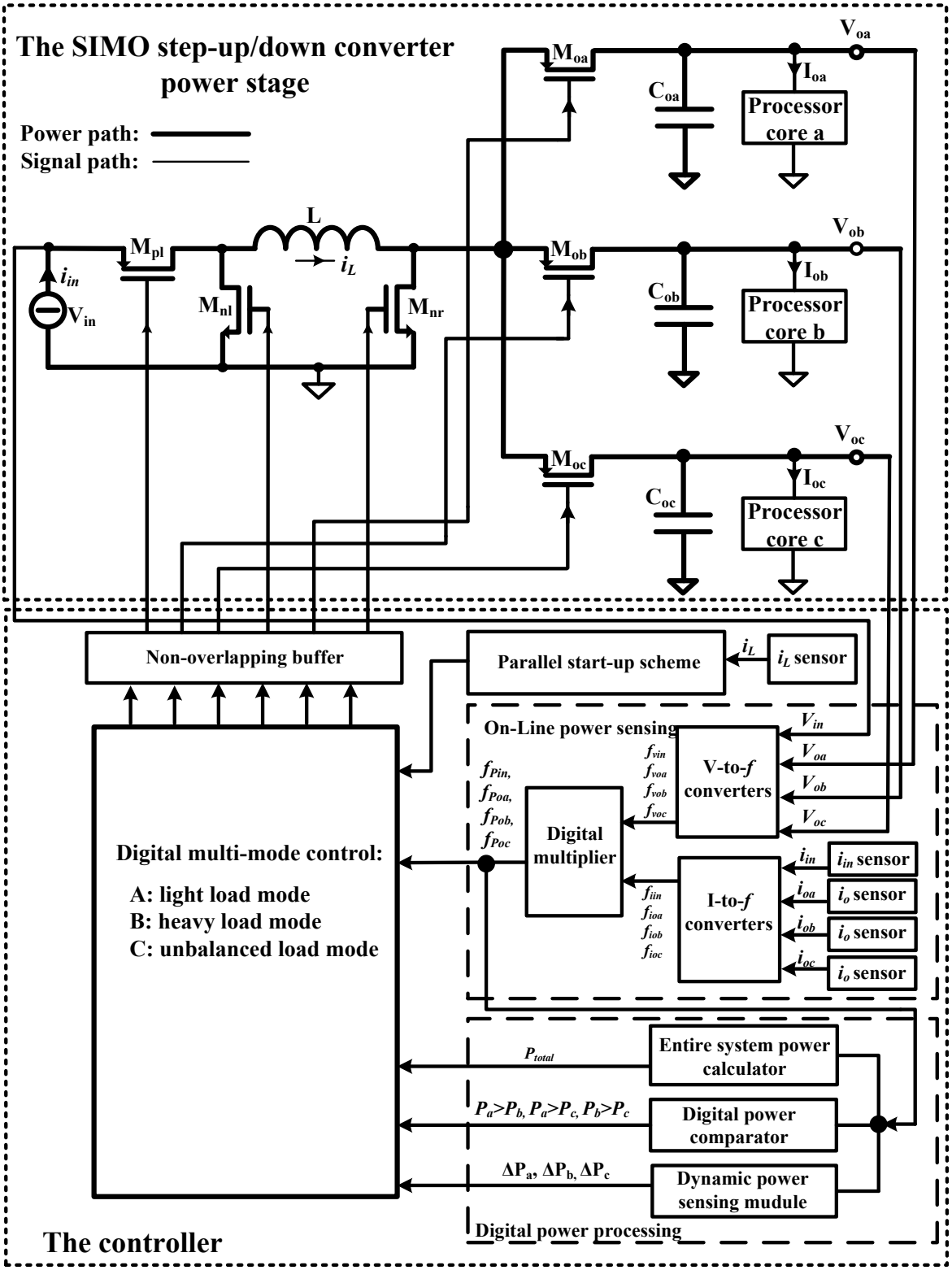


Figure 5.2.1 System block diagram of the proposed design.

For the design of the power stage, as depicted in Figure 5.2.1, this work inherits the cost-effective feature of a SIMO converter: in order to regulate three outputs, only one inductor is needed. The number of power switches is also reduced by 50%. More importantly, in contrast to existing SIMO designs [Bonizzoni-07] [H-P. Le-07] [Ma-02a] [Ma-03a], each output is variable with step-up/down DC-DC conversion. According to a research conducted at CMU, the use of multiple and variable power supplies can maximize the DVS control flexibility and achieve the largest possible power saving. Compared to the DVS techniques that employ a single variable supply [Burd-00] [Calhoun-06] [Kwon-03] [Ma-04] [Ma-06a] [Nowka-02] [Weiser-94] or multiple static power supplies [Bonizzoni-07] [Chang-97] [Dancy-00] [Goodman-98] [H-P. Le-07] [Ishihara-01] [Johnson-97] [Ma-02a][Ma-03a] [Usami-08] [Yeh-01], this technique can further reduce power consumption by more than 20% [Iyer-02].

The circuit operation of the power stage can be explained in two states. During State 1 (the charge state), both transistors M_{pl} and M_{nr} are turned on, and the voltage across the inductor L becomes equal to V_{in}. The inductor is charged up with a slope of V_{in}/L until DT expires. Here D is the duty ratio determined by the controller. During State 2 (the discharge state), the transistors M_{pl} and M_{nr} are switched off. Depending on the operation modes determined by the controller, M_{nl} and one of the output transistors (M_{oa}, M_{ob}, and M_{oc}) are turned on. The voltage across the inductor then becomes $-V_{oi,i=[a,b,c]}$. The inductor then discharges with a negative slope of $-V_{oi,i=[a,b,c]}/L$, thereby delivering power to one or two or even all of the outputs. The voltage conversion ratio is calculated as: $M_{oi,i=[a,b,c]}=V_{oi,i=[a,b,c]}/V_{in}=D/(1-D)$. When D is greater than 1/2, a step-up conversion is achieved. Otherwise, the converter functions as a step-down power converter.

For the design of the controller, software-defined hybrid control schemes work jointly with the power stage to ensure efficient operation of the multicore system under all possible operation scenarios. During the start-up period, a parallel start-up mode is adopted, wherein the power stage is automatically reconfigured into a buck topology. Power is delivered simultaneously to all three outputs, thereby speeding up the entire start-up process. In the steady state, on-line power sensors continuously monitor the instantaneous power demands of the processor cores present at each output as well as the input power at the power source. The sensed power is then processed to determine the total power demand, along with the priority of power delivery to each of the outputs. The digital multi-mode controller then utilizes the sensed and processed information to decide on the power delivery schemes. It then appropriately controls the power stage and thus the amount of power delivered to each core in the system, leading to an efficient, fast and robust system operation.

5.2.2 Parallel Start-Up Control Scheme

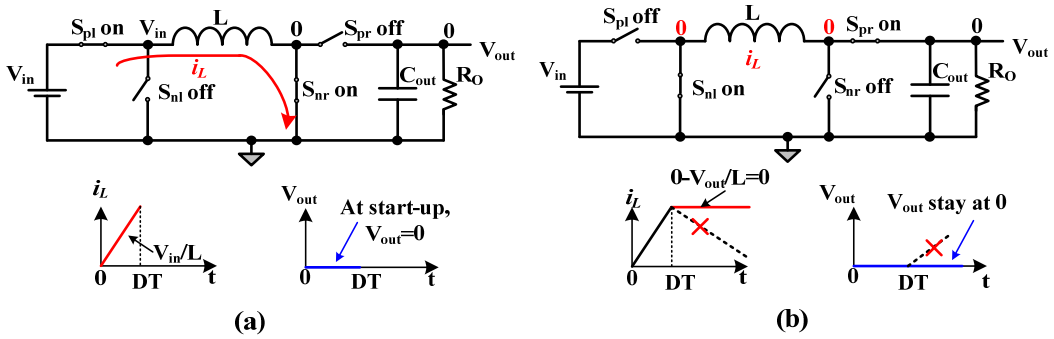


Figure 5.2.2 Start-up issue in a step-up/down converter: (a) State 1, and (b) State 2.

Although a step-up/down power converter offers a much wider voltage range than its buck or boost counterparts, it requires an extra control mechanism to start up. Such an issue is illustrated in Figure 5.2.2. Initially, since V_{out} is relaxed at zero volts, the inductor, in State 1 (Figure 5.2.2(a)), charges up well. However, in State 2 (Figure 5.2.2(b)), it cannot be discharged

due to the low voltage across its terminals. Although the error amplifier in the controller generates a large duty ratio in State 1, thereby significantly charging up the inductor, most of the charge cannot flow to the output load, as the remaining discharge period is too short. Therefore, while i_L keeps increasing, V_{out} remains low. As these charge and discharge actions repeat, the large inductor current i_L may eventually damage power devices permanently.

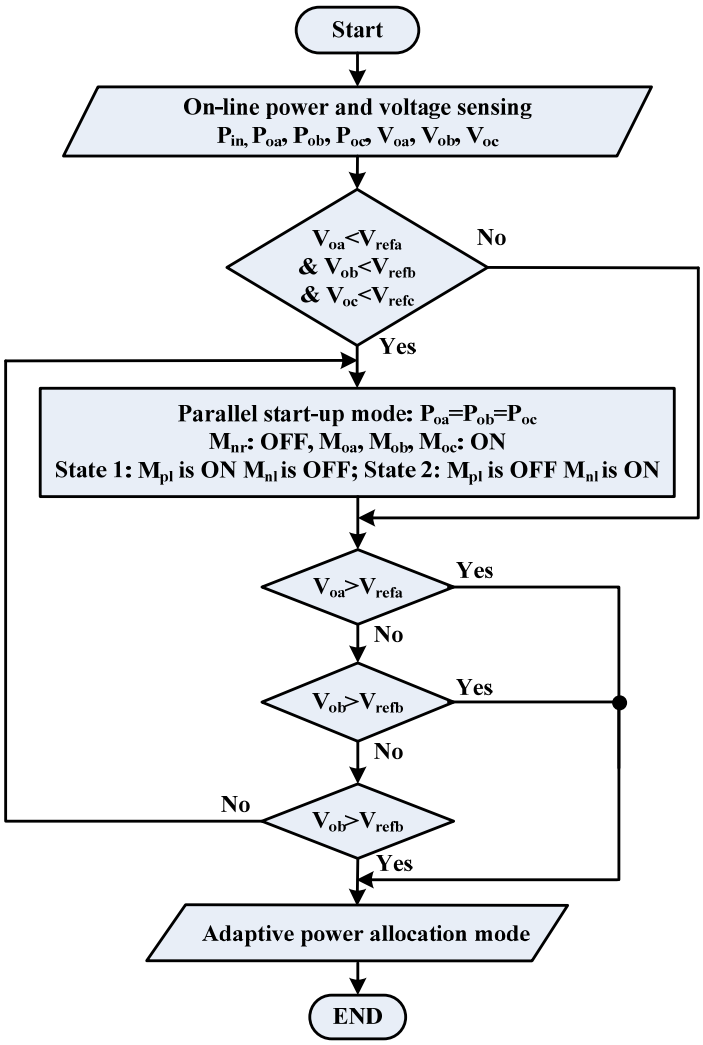


Figure 5.2.3 Flow chart of the parallel start-up control scheme.

In order to overcome this drawback, a parallel start-up scheme is adopted, the flowchart of which is shown in Figure 5.2.3 and the corresponding timing diagram is shown in Figure 5.2.4. When the system is initially powered on, the voltages levels of all the outputs are zero. This state is

sensed by the on-line power sensing and voltage sensing circuits. Once the multi-modes controller learns that each output voltage is much lower than its reference value, it configures the power stage to operate in the start-up mode. In this mode, the transistor M_{nr} is turned off, while the transistors M_{oa}, M_{ob}, and M_{oc} are turned on. The power stage now resembles a parallel SIMO buck converter, which does not face any start-up problems. In this configuration, power is delivered to all three outputs equally. As all the outputs are charged up, if any one of them reaches its desired regulation voltage value, the controller exits the start-up mode and the multi-modes controller takes over.

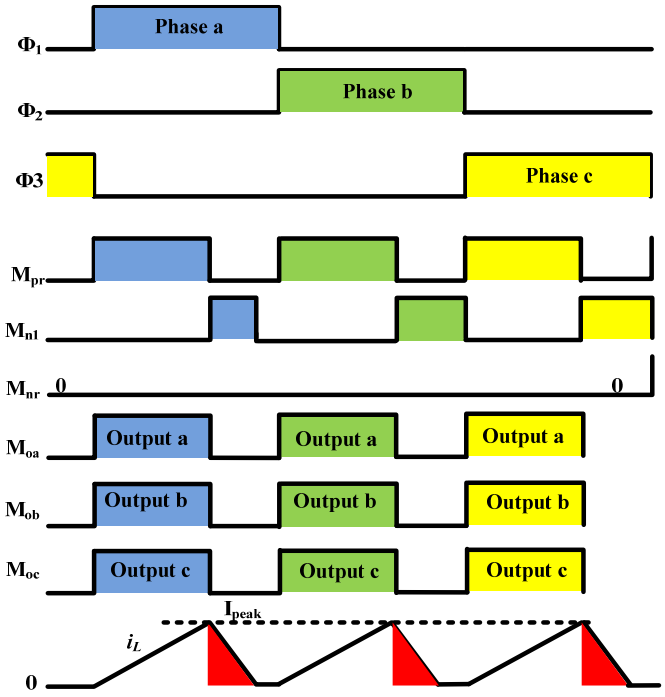


Figure 5.2.4 Timing diagram of the parallel start-up scheme.

5.2.3 Software-Defined Multi-Modes Control Scheme

As mentioned earlier, cross regulation is a critical stability issue in multiple-output converters. To avoid it and minimize system response time, power demands from all processor cores should be instantaneously monitored and accurately measured. On-line digital power

sensing and processing techniques are thus used to accurately measure the instantaneous static and dynamic power of the whole system. The details are to be addressed in Section 5.3.2. With the aid of on-line power sensing and processing, a digital multi-mode control scheme is proposed, the control scheme contributes to adaptive, prompt and optimal regulation under different operation scenarios. Figure 5.2.5~Figure 5.2.7 illustrates the control schemes under different operation scenarios. Three major operation scenarios are discussed here.

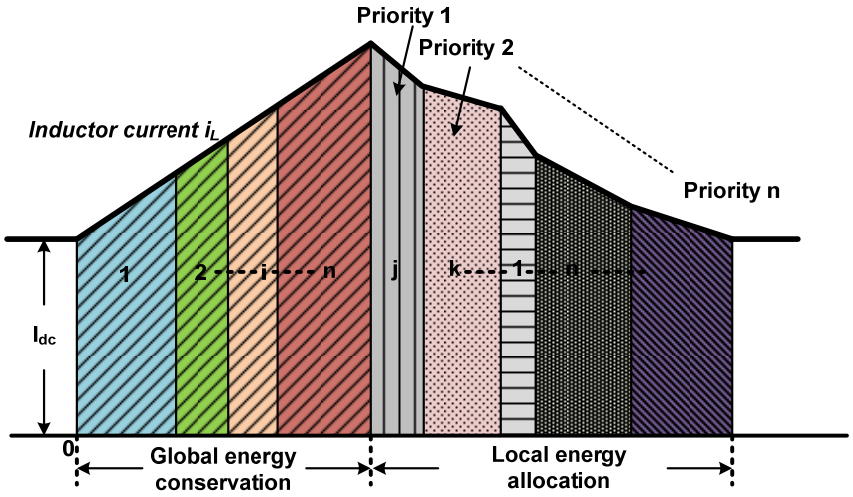


Figure 5.2.5 Inductor current at light load mode.

In **Light load mode** (Figure 5.2.5), when all the loads are light, the inductor is charged only once in a global switching cycle, with the energy of total load demands (global power estimate). This energy is then accurately discharged to each load, one at a time (local allocation) as shown in the current flow in Figure 5.2.5. Switching power and noise will be reduced due to less frequent switching actions.

In **Heavy load mode** (Figure 5.2.6), when all the loads are heavy, the use of the previous scheme would lead to high peak currents and noise spikes. Instead, the inductor is charged and

discharged based on individual load demands, according to the regulation priority that is determined online.

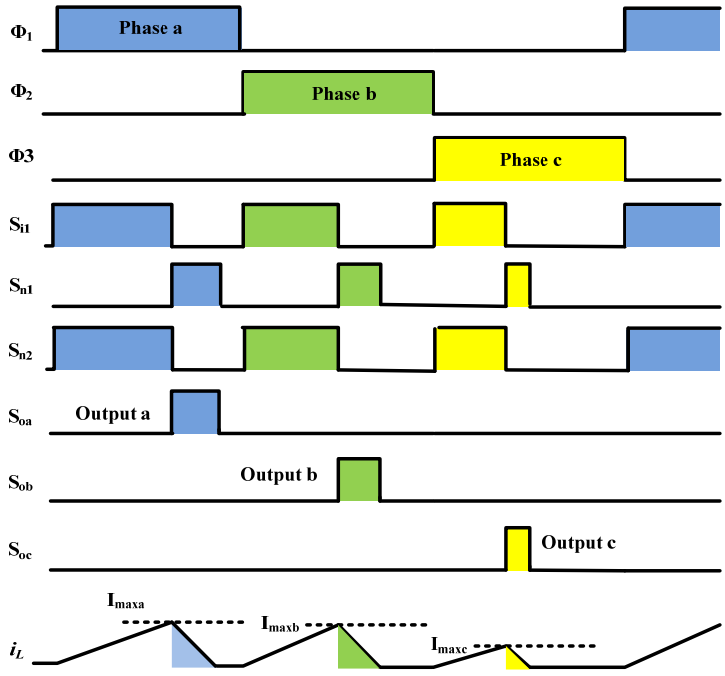


Figure 5.2.6 Timing diagram at heavy load mode.

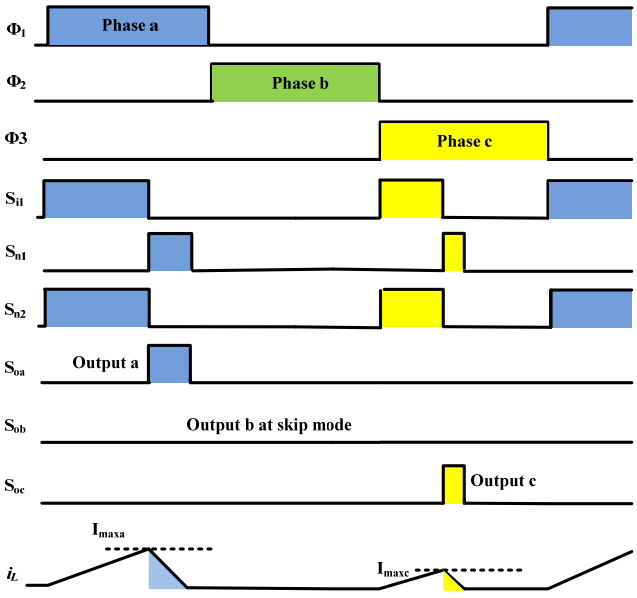


Figure 5.2.7 Timing diagram at unbalanced power demand mode.

Figure 5.2.7 shows the **unbalanced power demand mode**, where loads *a* and *c* are heavy but loads *b* is light. Under this situation, the regulation only focuses on power delivery for loads *a* and *c*. This skipping operation on *b* reduces the switching power loss and noise, and improves the response times to the more power demanding loads *a* and *c*.

5.3 Circuit Implementations

5.3.1 Process and Temperature Independent Ring Oscillator Based ADC

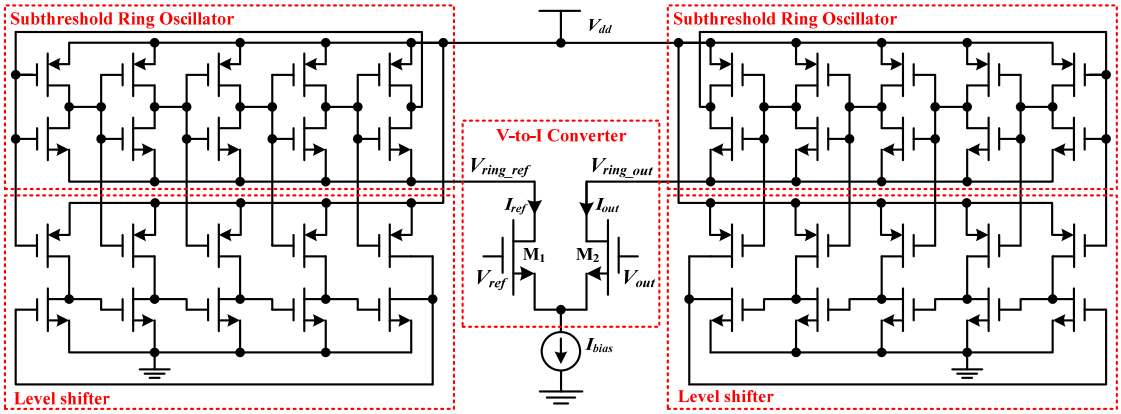


Figure 5.3.1 Schematic of the process and temperature independent ring oscillator based ADC.

Figure 5.3.1 shows the process and temperature independent sub-threshold ring-oscillator based ADC. A differential V-to-I converter is employed to amplify the output voltage V_{out} and the reference voltage V_{ref}, and then convert them into the corresponding current signals I_{ref} and I_{out}. In order to achieve a higher closed-loop gain and thus a finer regulation resolution, large trans-conductance is preferred in the input stage of the V-to-I converter. The differential circuit topology has the advantages of canceling even-order harmonics as well as temperature and process variations. In addition, wide common-mode input range and supply-independent current biasing are adopted to enhance circuit robustness to supply (V_{in}) and output (V_{out}) variations. As results, the voltage error between the output voltage V_{out} and the reference voltage V_{ref} is converted to the current difference,

$$\Delta I = I_{out} - I_{ref} = g_m (V_{vout} - V_{ref}) = g_m \cdot v_e \,. \tag{5.1}$$

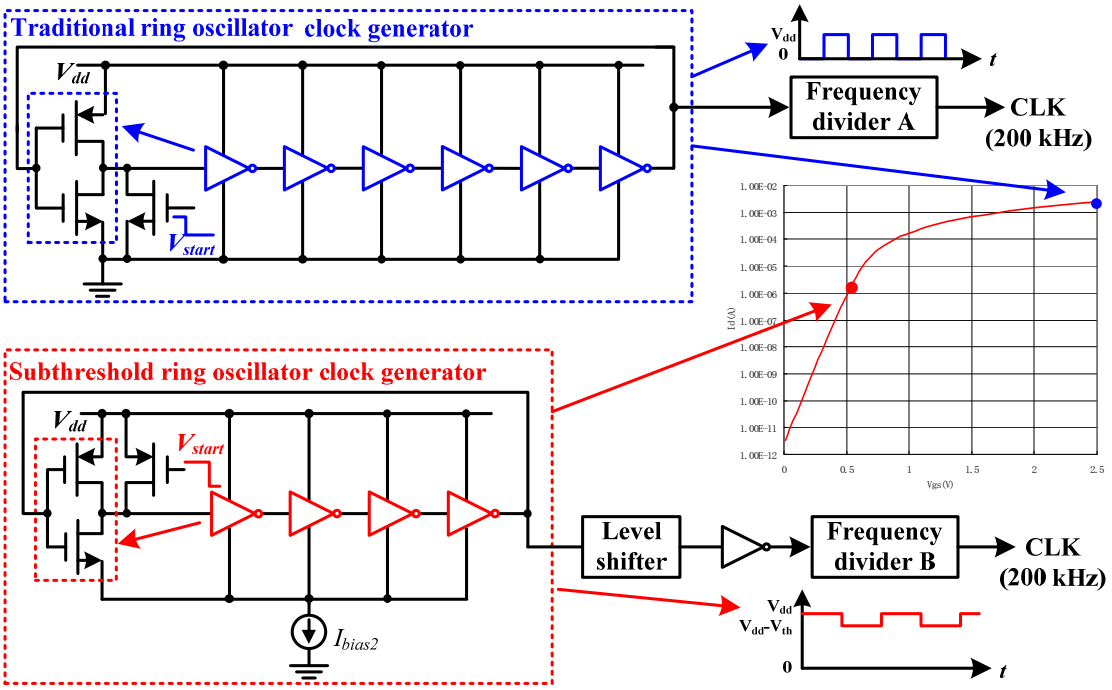


Figure 5.3.2 Traditional and the proposed ring oscillator clock generators.

I_{ref} and I_{out} are used to bias two ring oscillators. With the different biasing currents, the oscillation frequency of each oscillator varies accordingly. Note that, the biasing current here is designed very low to operate the oscillators in the subthreshold region. Compared to traditional ring oscillator with a full voltage swing of V_{in}, the voltage swing of the subthreshold ring oscillator is around or even below a MOSFET threshold voltage (V_{th}), which allows the oscillators to save significant switching power. Our experimental results show that the power consumption drops significantly from 2.13 mW in traditional ring oscillator clock generator to only 70 μW in our subthreshold-region design, when the oscillation frequency is set at 200 kHz.

As a MOS transistor operates in the subthreshold region, its unity-gain frequency, f_T, can be defined as [Rabaey-03]

$$f_T = \frac{1}{2\pi} \frac{I_D}{V_T} \frac{1}{WLC_{js}} \,. \tag{5.2}$$

Similarly, the oscillation frequency of each oscillator also shows a linear dependence on the biasing current:

$$f_{osc} = k_{ro} \cdot I_{bias} + b \,. \tag{5.3}$$

The linear relationship between the oscillation frequency and the biasing current makes the detected voltage error also linearly proportional to the oscillation frequency. This is proven by

$$\Delta f = f_{out} - f_{ref} = k_{ro}(I_{out} - I_{ref}) = k_{ro}\Delta I = k_{ro} \cdot g_m \cdot v_e \,. \tag{5.4}$$

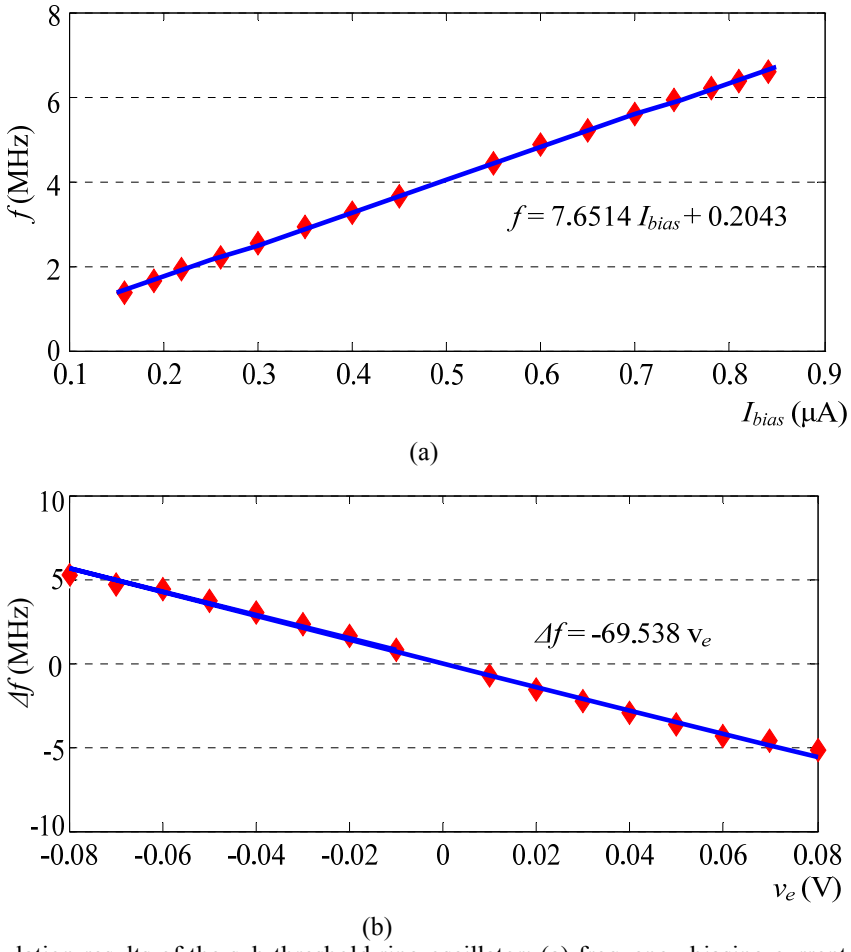


Figure 5.3.3 Simulation results of the sub-threshold ring oscillator: (a) frequency-biasing current dependency, and (b) frequency-voltage error dependency.

The linear frequency-error relation greatly simplifies the system modeling and circuit designs. Our experimental results in Figure 5.3.3 clearly prove these linear frequency dependencies.

5.3.2 On-Line Power Sensing and Processing

The on-line power sensing and processing circuits are integral parts of the software-defined multi-modes control. As illustrated in Figure 5.3.4, the power sensors that make up the on-line power sensing module consists of current and voltage sensing circuits, along with a digital multiplier. To determine the instantaneous power demands, as shown in Figure 5.3.4, the sensed output voltages and currents are converted into corresponding frequency values. Voltage-to-frequency (V-to-*f*) conversion is achieved using a ring oscillator, while the current conversion is achieved by using transistor scaling based current sensor followed by subsequent current-to-frequency (I-to-*f*) conversion. These frequency values are utilized by the digital multiplier to obtain the instantaneous power demand of each output.

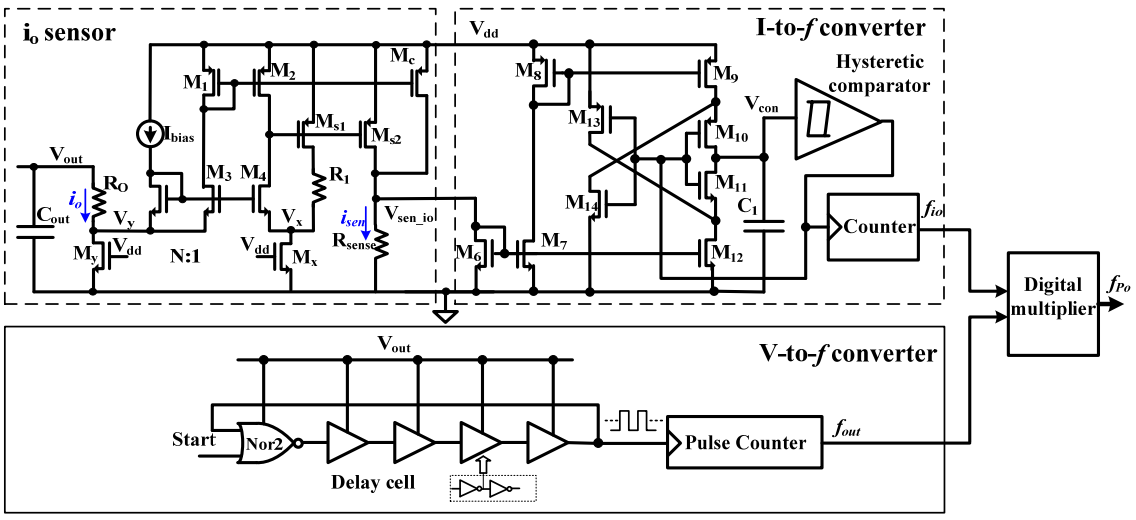


Figure 5.3.4 Schematic of a power sensor.

To generate the correct power information, a current sensor is designed to monitor the instantaneous load current i_o(Figure 5.3.4). Instead of employing a traditional series sensing resistor, the on-line transistor current scaling technique is employed [Ki-98c] [Luo-09]. The transistors M_1~M_4 form a voltage mirror, thereby forcing the drain voltages of M_y and M_x to be equal. Here, M_y is the power transistor at the load, while M_x is the sensing transistor that is N times smaller than M_y. Since the two transistors operate at the same DC conditions, the load current i_o, which flows through M_y, is scaled down by N times in M_x. As a result, the power consumption of the current sensor is N-times lower when compared to using sensing resistors. The sensing current is then copied to the I-to-*f* converter which is also shown in Figure 5.3.4. The sensing current flowing into M_6 is mirrored and scaled to M_7, M_8, M_9 and M_{12} depending on the transistor ratio. M_{10} and M_{11} work as switches to charge and discharge the capacitor C_1. When the control signal V_{con} reaches threshold voltage V_{high}, the hysteretic comparator output flips, which turns forces M_{10} off and M_{11} on. The capacitor C_1 is then discharged. As a result, the control signal drops until it reaches V_{low}, and the comparators will flip the state again and charge the capacitor C_1. Obviously, the larger the load current, the faster C_1 is charged up, leading to a larger number at the counter output. A digital multiplier then multiplies the detected current and voltage for power information.

The sensed instantaneous power demands are then processed as follows. The total system power is computed first. It is from this total power demand, along with the individual power demand of each core, that the multi-modes controller starts to determine the duty ratios to be employed in each power switches at the power stage. Simultaneously, the power processor determines the transients and dynamics of the multicore system, with the aid of the dynamic power sensor. This sensor identifies dynamic changes present at each core, by comparing the

instantaneous and the previous power demands at each output of the converter. Based on this, a digital power comparator is employed to assign a priority scheme for power delivery. If each of the outputs continues to remain at steady state, then the digital power comparator assigns the highest priority to the output that has the largest power demand. If a transient is identified at any of the outputs, then this output is assigned with the highest priority, even if its power demand is not the largest. Based on this priority scheme, the total power and the instantaneous power demands and system dynamics, the multi-modes controller identifies the operation mode and suitably controls the power stage, leading to the most efficient operation of the step-up/down power converter.

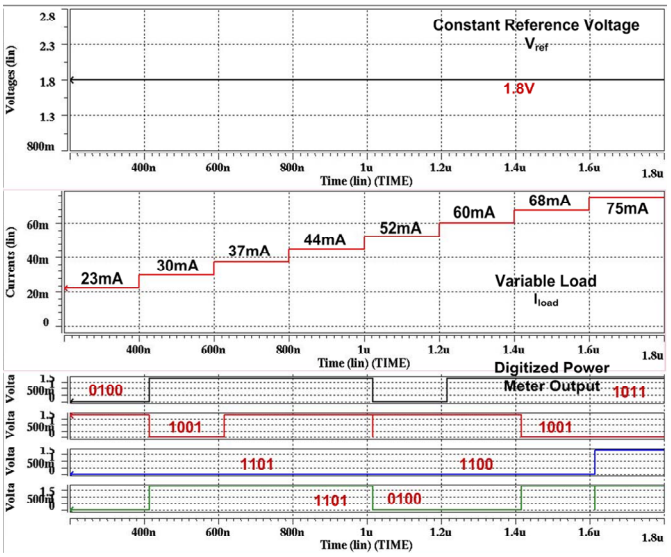


Figure 5.3.5 Simulated digital power sensing and processing technique outputs: with constant reference voltage V_{ref}.

Figure 5.3.5, Figure 5.3.6. and Figure 5.3.7 illustrate the effectiveness of the on-line digital power sensing and processing technique. Figure 5.3.5 depicts the response of the digital power meter when the reference voltage is fixed at a particular value, while the load current is increased from 23 to 75 mA gradually, with a step of 7 mA. It is seen that the output of the power meter immediately responds to the change in an accurate manner. Figure 5.3.6 illustrates the case were the reference voltage is decreased from 3 down to 0.9V, with a step of 0.3V, while

keeping the load current constant. Once again, the power sensing is prompt and accurate. The total digitized power output is also shown in Figure 5.3.7.

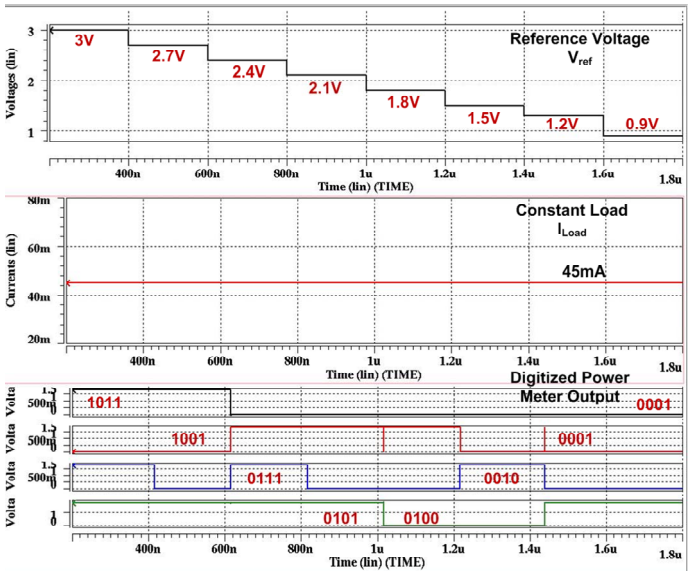


Figure 5.3.6 Simulated digital power sensing and processing technique outputs: with constant load current I_{load}.

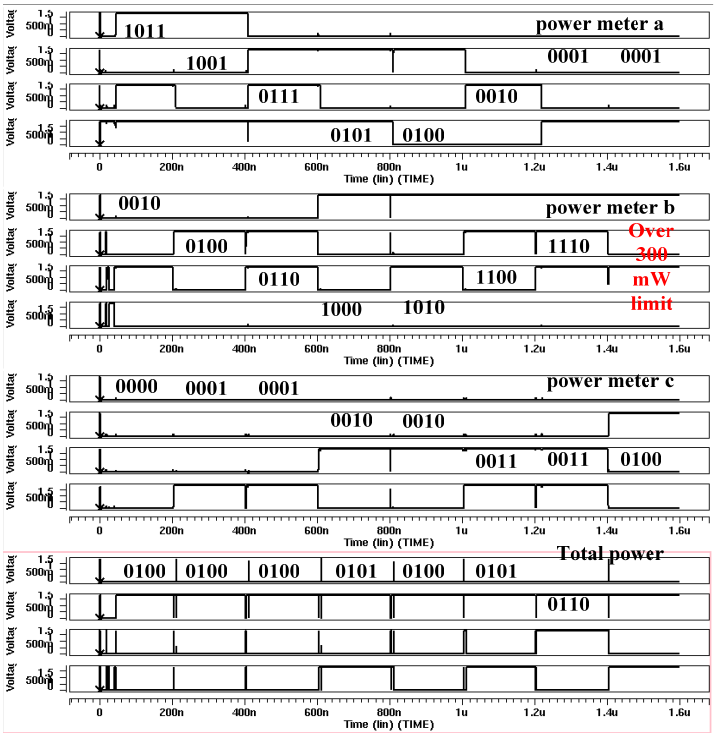


Figure 5.3.7 Simulated digital power sensing and processing technique outputs: total power demand.

5.4 Performance Verifications

5.4.1 Steady-State Performance

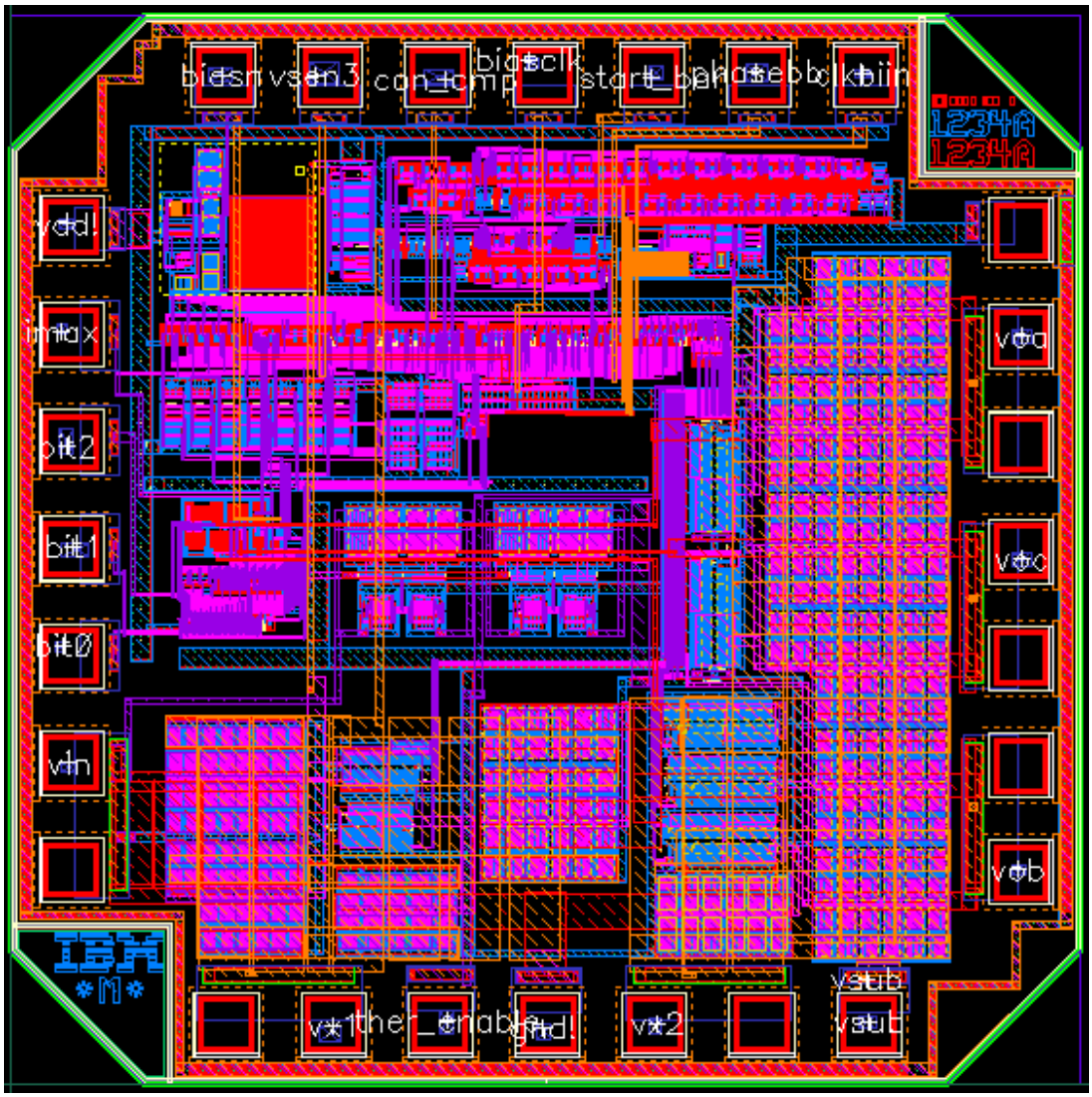


Figure 5.4. 1 Chip layout.

The proposed converter is designed with a 180-nm CMOS process, and has been sent for fabrication. Figure 5.4.1 shows the layout of the entire system. We have chosen the respective inductor and filtering capacitor values as 10 μH and 10 μF, where the ESR of the capacitor is 350 mΩ. The converter provides three well-regulated outputs that are variable from 0.9 to 3.0 V and a total power from 33 mW to 900 mW. The maximum efficiency is 80.9% when three outputs

regulated at 1.2V, 1.8V, and 2.4V, respectively, with a total power 850 mW. With a line regulation of 4.6 mV/V, the converter functions robustly when the supply voltage frequently varies between 1.8 and 3.3V. The switching frequency is 2 MHz at heavy load and 500 kHz at light load. All the results reported here are based on fully transistor level HSPICE post-layout simulations with BSIM 3 Level 49 transistor models.

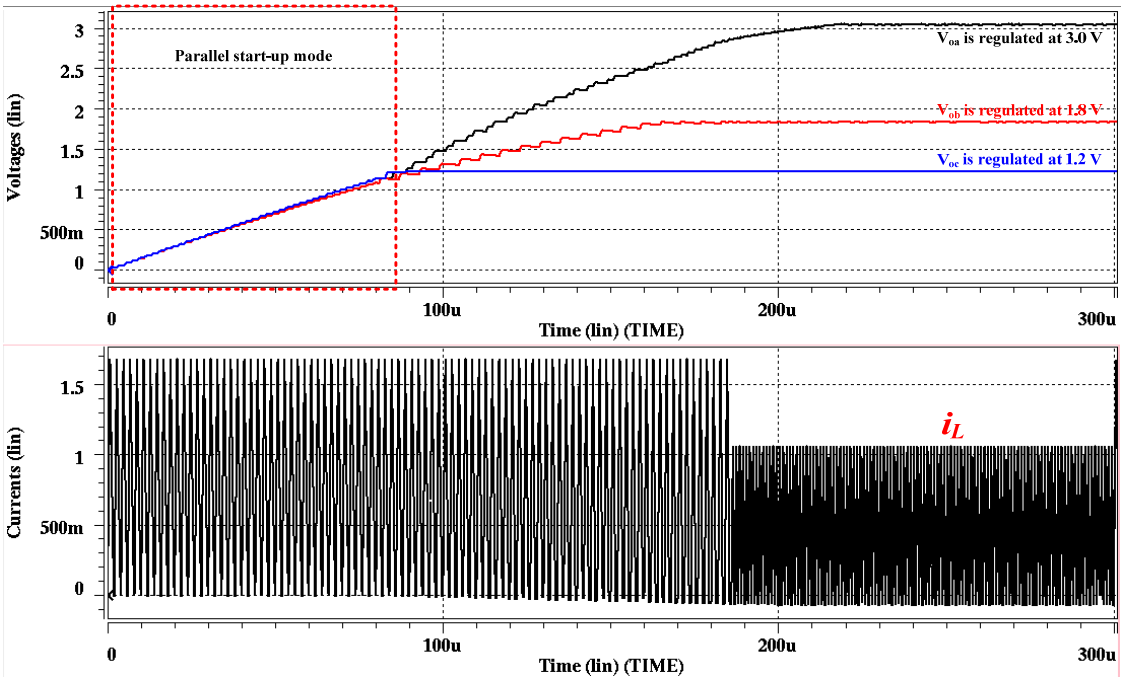


Figure 5.4.2 Simulated steady-state three output voltages (top), and inductor current i_L (bottom).

Figure 5.4.2 shows the simulated three steady-state power outputs, and the inductor current i_L. With a nominal supply voltage V_{in} of 2.5 V, V_{oc} achieved the regulated output at the lower bound of the regulation: 0.9V, while V_{oa} demonstrated the regulated output at the higher bound of the regulation: 3.0V. For these two outputs, the converter performs step-down and step-up conversion, respectively. V_{ob} is regulated at 1.8 V as an example. Note that each output can be independently adjusted to any level from 0.9V to 3.0V, based on the real-time power demand. As shown in Fig. 5.4.2, during the parallel buck start-up mode, the inductor current is maximized to

achieve a faster transient speed, which then goes back to normal operation during the steady-state.

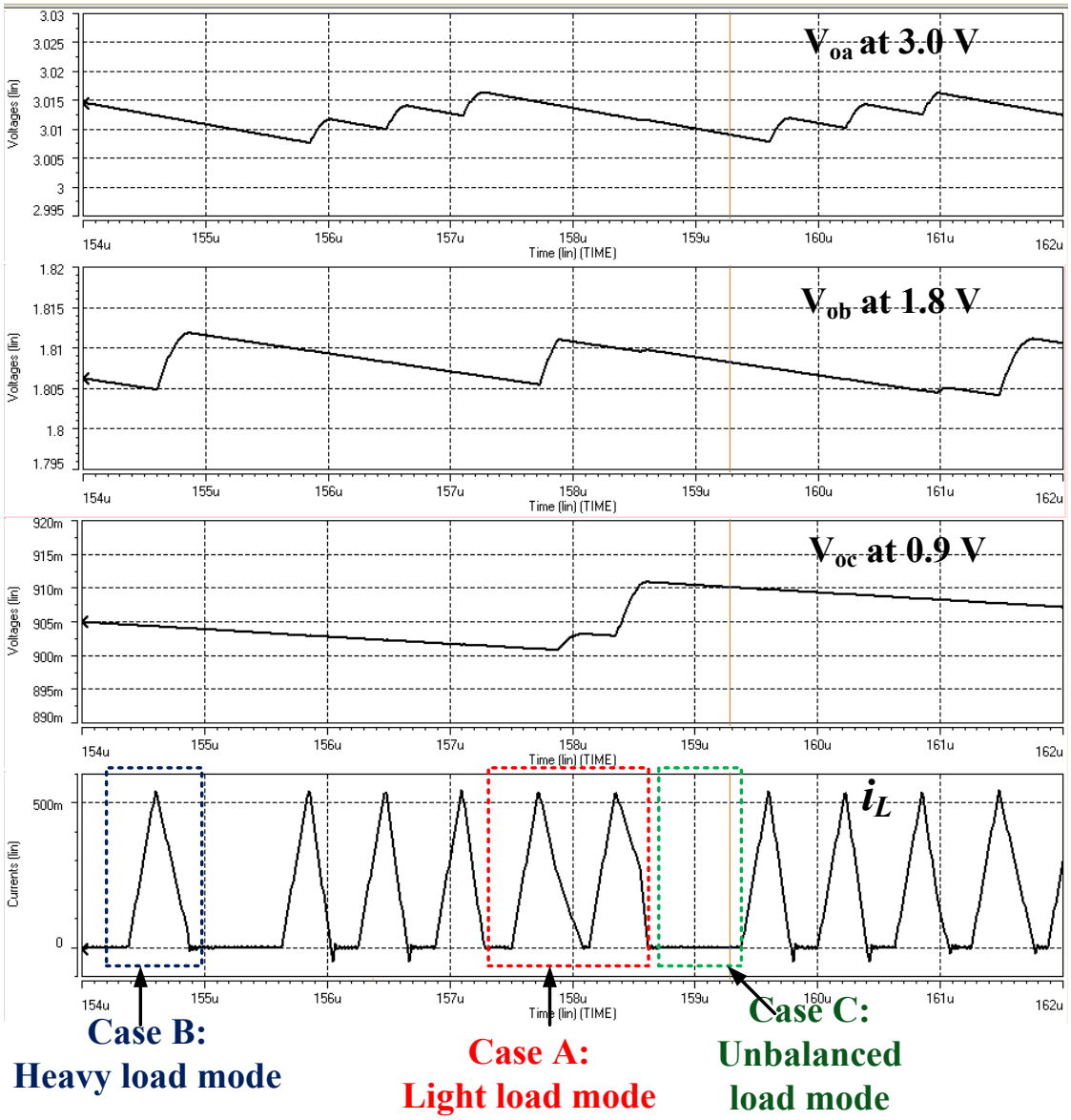


Figure 5.4.3 Simulated output ripple voltages at different control modes.

At it can be seen from Figure 5.4.3, within the entire output voltage range, the peak-to-peak ripple voltages of all three outputs are controlled below 10 mV, due to the accurate multi-modes control. Meanwhile, the inductor current waveform (i_L) clearly verified the control ideas proposed

in Section 5.2. Under different operation conditions, different modes are selected by the controller: time multiplexing mode at heavy load, charge once and deliver all mode at the light load, and the skip mode. Figure 5.4.4 shows the simulated control signals when V_{oa} is at the buck-boost mode with heavy load, V_{ob} is at boost mode with light load and V_{oc} is at buck mode with light load.

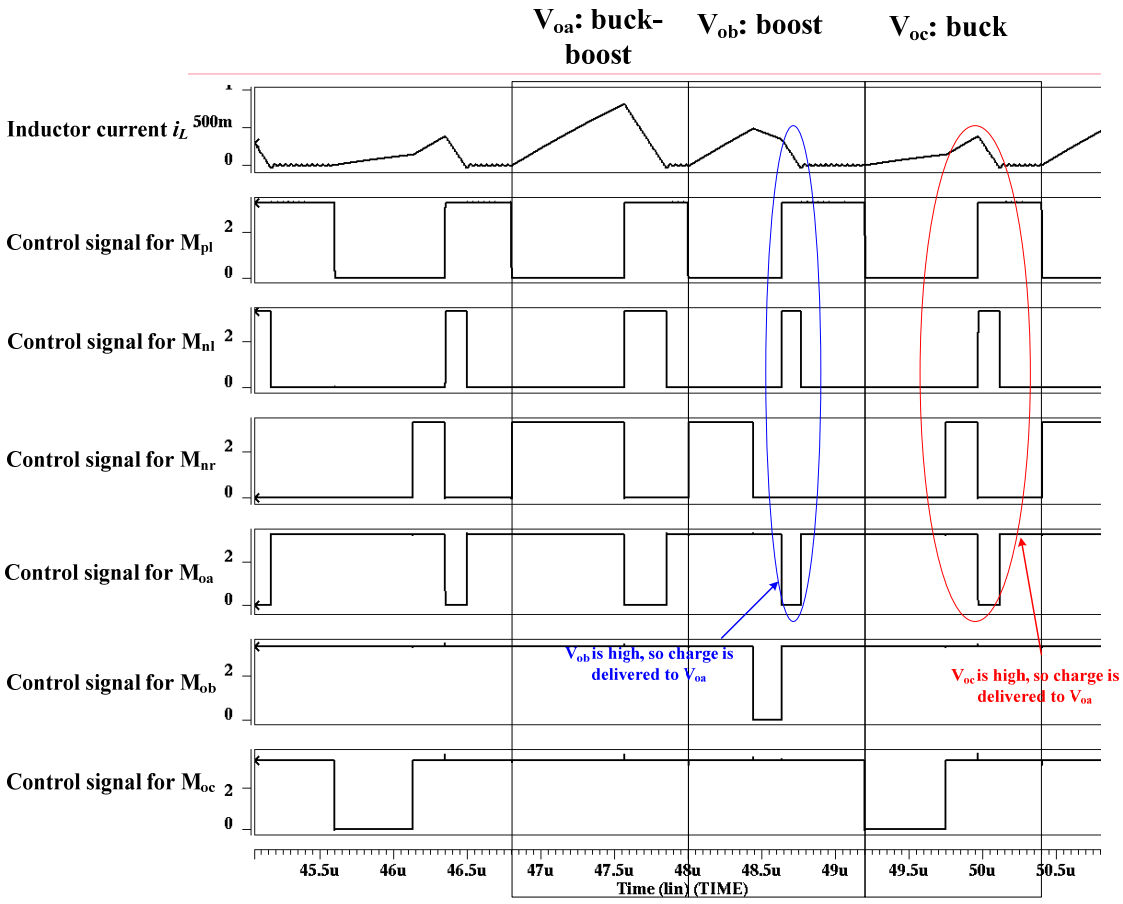


Figure 5.4.4 Simulated control signals.

5.4.2 Dynamic Transient Performance

Figure 5.4.5 shows the load transient performance test. At the output V_{oa}, sudden load changes take place from 0 mA to 67.5 mA at the instant of 120 μs and from 67.5 mA to 0 mA at the instant of 200 μs, modeling the worst case of load changes in the real applications. The closed-up view of the lower trace shows a smooth and stable transient performance. The output voltage

variation at all outputs is controlled below 20 mV with a settling time of 3.25 µs. The other two outputs V_{ob} and V_{oc} are kept at the desired regulated voltage level. Minimum cross regulation is observed.

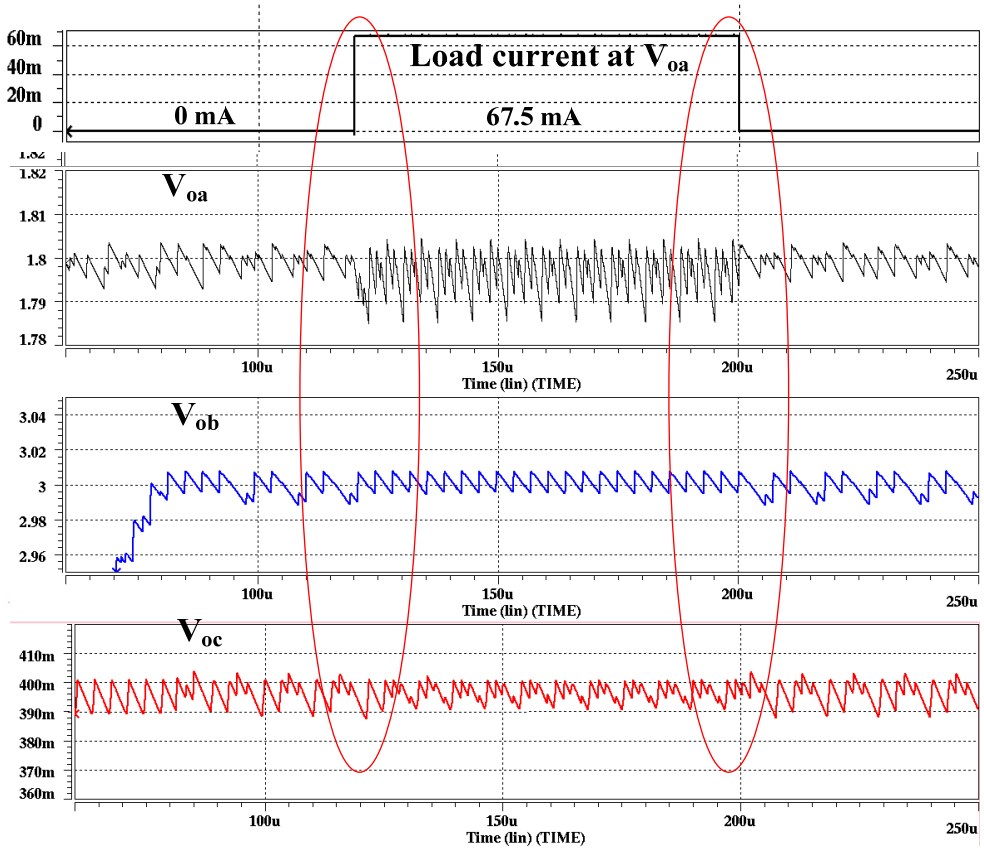


Figure 5.4.5 Load transient performance test.

Figure 5.4.6 shows both start-up and dynamic voltage tracking performance for DVS applications. At the instant of 0 µs, the converter is relaxed. All the output voltages stay at zero. Once started, the converter initializes the parallel start-up scheme to charge up all the outputs simultaneously. Once the first desired output level (1.2V) is reached, each of the three outputs are regulated separately. Multi-mode control scheme takes over the complete system regulation after the instant of 190 µs. The outputs settle at 1.2V, 1.8V and 3.0V, respectively. At the instant of 300 µs, DVS system control signals are detected, requiring both V_{ob} and V_{oc} to suddenly step up from

1.8V to 2.4V and from 1.2V to 1.8V, respectively. It only takes the converter 95 μs to trace all the DVS voltage changes and settle at the newly defined levels, while V_{oa} is still regulated at 3.0V, with very little cross regulation.

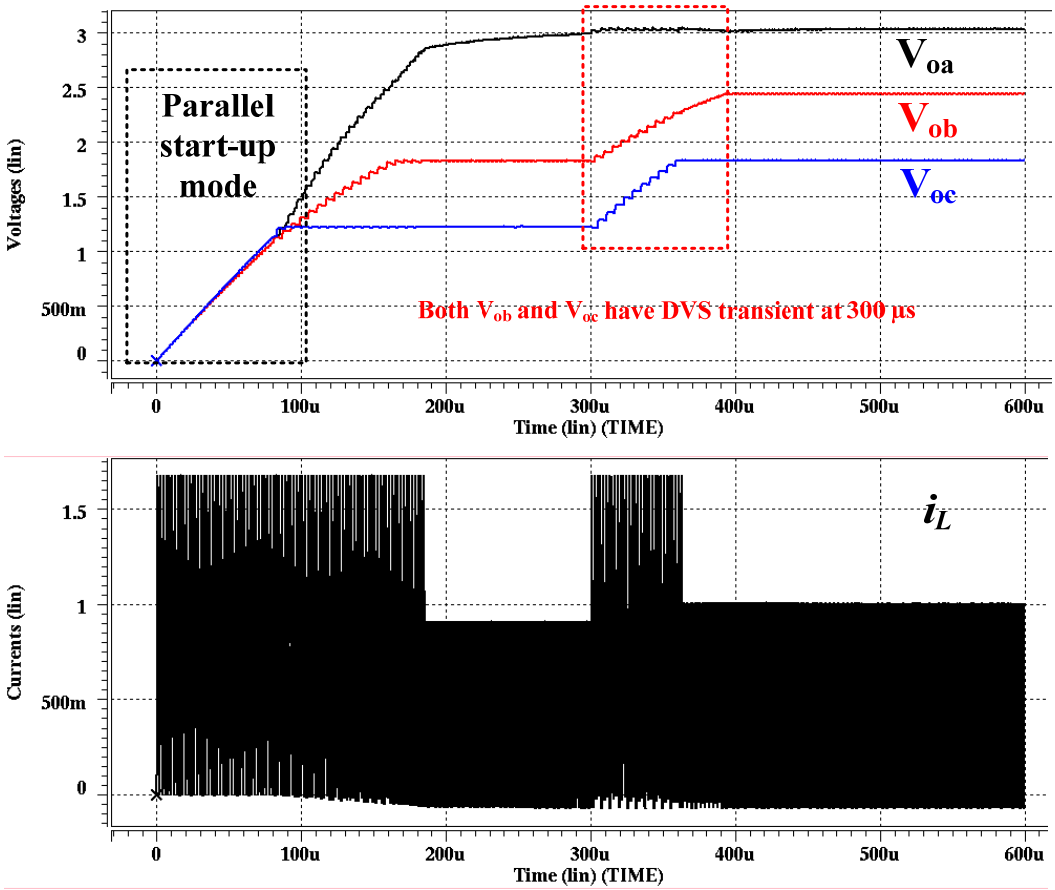


Figure 5.4.6 Start-up and DVS transient performance test.

Figure 5.4.7 shows the line regulation performance. With three output regulated at 2.75V, 1.8V, 1.2V, the converter is powered by an input source V_{in} that frequently switches between 2.0 and 3.3 V. Thanks to the multi-mode control scheme, all the three outputs exhibit less than 1% undershoot voltage. With a total 6 mV output voltage variation, the line regulation of 4.6 mV/V is measured.

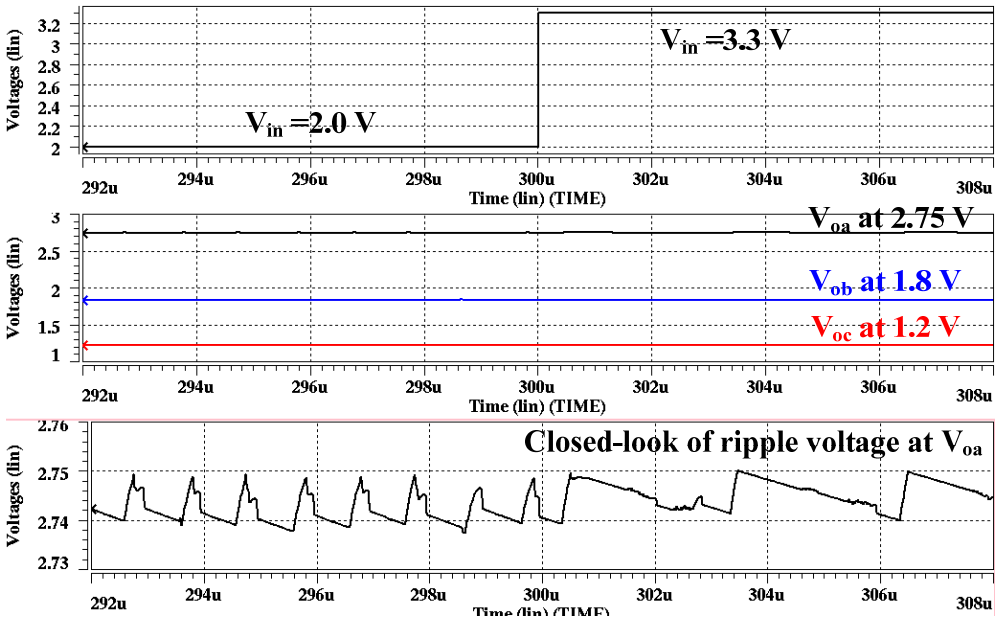


Figure 5.4.7 Line regulation performance test: V_{in} (top), regulated outputs (middle), and a close-up view at V_{oa}(bottom).

5.5 Conclusions

In this chapter, we propose a new integrated adaptive SIMO step- up/down DC-DC converter for DVS-enabled multicore system applications. The software-defined multi-modes control allows the converter to operate with superior line, load and DVS transient regulations, while keeping the cross regulation at a very small value. The design provides a competitive solution to the new-generation, high-performance, on-chip adaptive power supply designs.

CHAPTER 6 CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

As power issue has been identified as one Grand Challenge by ITRS [ITRS-09], dynamic voltage scaling (DVS) and/or dynamic thermal management (DTM) have emerged to enable more power-efficient operation and to ensure thermal safety in recent years. Most popular DVS systems employ an external variable-output DC-DC converter. However, as the scale of VLSI system increases, single dynamic DC-DC converter can hardly minimize system power consumption, especially when processor cores or functional modules require their peak power at different times. Hence, multiple voltage level operations are highly demanded. This dissertation introduced DC-DC converter designs that make all these techniques realizable.

Three different DC-DC converter topologies with multiple control schemes were introduced that provide high-efficient well-regulated DVS-enabled power sources. First, a buck converter with dual-mode pulse-train/PWM control is proposed for both fine output regulation and fast transient response; second, a digital tri-mode controlled buck-boost converter is discussed with automatic substrate switching circuit (ASSC) for DVS applications; then we introduced a software-defined single-inductor multiple-output (SIMO) step-up/down power converter with multi-modes control for multicore systems. All three designs involve hybrid control schemes for optimize the whole system in all operation scenarios: start-up, steady-state, and line/load dynamics.

Several control techniques and circuit-level design techniques have been presented to optimize the system performance, reduce the size, cost and energy dissipation of the low-voltage and low power DC-DC converters. Experimental results on these three integrated DC-DC

converter prototypes have successfully demonstrated these design techniques. The approach presented in this dissertation is evidently viable for realizing compact and high efficient DC-DC converters.

6.2 Summary of Research Contributions

In this dissertation, low-voltage high-efficiency DC-DC converters with hybrid control schemes discussed. This included the development and demonstration of the system-level and circuit-level design techniques to increase the utility of DC-DC converter in DVS applications and multiple-supply and variable supply systems. Several key research contributions are highlighted below:

The goal of this research is to design and implement power systems and develop circuit-level techniques to enhance the performance of DC-DC converters. Several key research contributions are highlighted below:

1) Developed a switching buck converter with dual-mode pulse-train and PWM control, which enjoys the flexibility of operating in either the high-frequency PWM mode for low output ripple voltage or the pulse train mode for fast load transient response. [Luo-07][Luo-08b][Luo-09].

2) Developed a digital tri-mode controlled variable-output buck-boost power converter for DVS-enabled integrated systems. Three voltage and current control modes operate jointly and seamlessly to optimize the converter's performance at start-up, steady state and dynamic voltage/load transient state, respectively. [Luo-08a].

3) Developed a software-defined single-inductor multiple-output (SIMO) step-up/down power converter with multi-modes control scheme for DVS-enabled multicore systems.

4) Successfully fabricated a CMOS integrated switching dc-dc converter with dual-mode pulse-train/PWM control. The output ripple voltage is reduced to ±12.5 mV in PMW mode and the load transient response is shorter than 345 ns with 100% load current change from 50 to 100 mA. The maximum efficiency is 91% [Luo-07] [Luo-08b][Luo-09].

5) Successfully fabricated a digital tri-mode controlled variable-output buck-boost power converter for DVS-enabled integrated systems. The converter precisely provides an adjustable power output within a voltage range from 0.9 to 3.0 V and a power range from 11 to 800 mW. Maximum efficiency of 96.5 % is measured at 0.9-V output and 45-mW load power [Luo-08a].

6.3 Future Work

6.3.1 Reconfigurable SI-MIMO Power Converter

A. SI-MIMO Power Stage

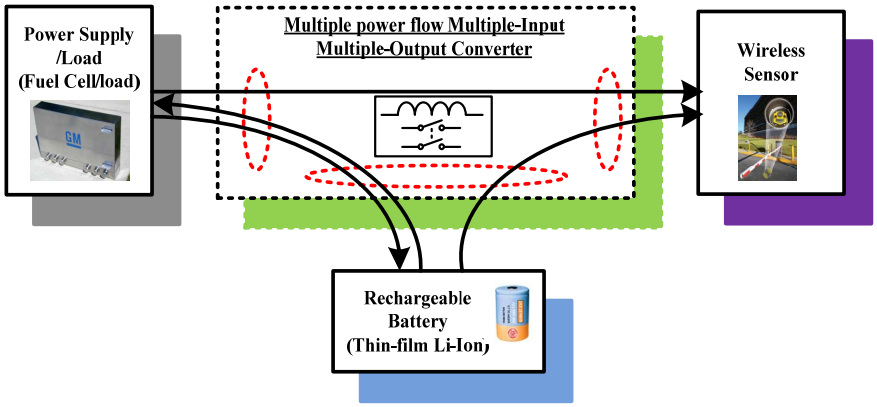


Figure 6.3.1 A multiple input multiple output system.

In order to overcome the drawbacks addressed in Section 2.3.3 and allow multiple-power-source and bidirectional-power-flow functions, the aforementioned architecture still needs to be modified. For example, as shown in Figure 6.3.1, in a portable device, rechargeable batteries are usually used as an offline power source. A power management system is needed to deliver power from either an external DC source of from a rechargeable battery to the equipment. When the external power source is available, it provides regulated power for output loads and charges the batteries (normal power flow). When the external power sources are unavailable, the batteries then become the power source to power all the loads (reverse power flow).

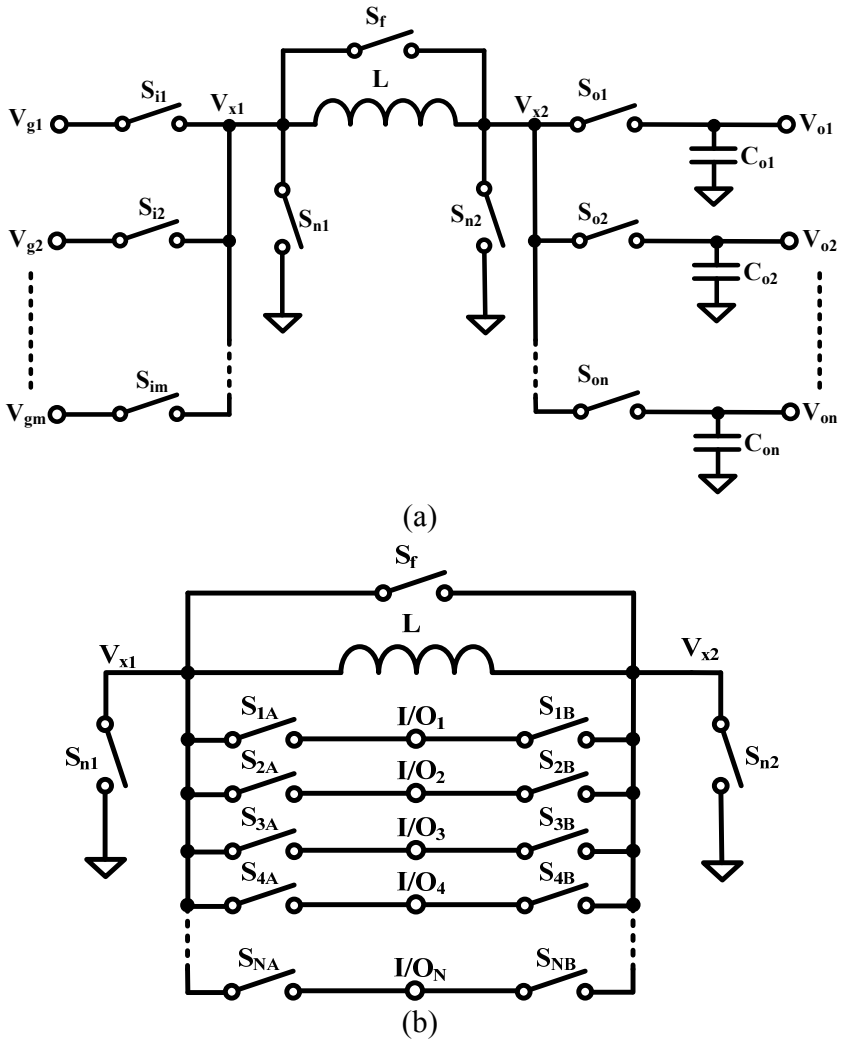


Figure 6.3.2 (a) the proposed step-up/down SIMIMO converter, and (b) a generic topology.

Accordingly, the design should accommodate bidirectional power flows and multiple inputs. By combining the multiple-output architectures discussed above, we thus propose a single-inductor multiple-input multiple-output (SI-MIMO) power stage. The schematic of the circuit is shown in Figure 6.3.2. In Figure 6.3.2(a), we propose a step-up/down SI-MIMO converter architecture to maximize the freedom of achieve both step-up and step-down conversions from both power flow directions. Figure 6.3.2(b) shows a clear demonstration that each power port can serve as either input (for power source) or output (for power load).

The system is highly reconfigurable, and can easily be implemented with buck (Figure 6.3.3), boost (Figure 6.3.4), buck-boost (Figure 6.3.5), or even bi-directional conversion, as shown in Figure 6.3.6, we use dual input and dual output converter as an example. One possible operation is depicted by the timing diagram shown in Figure 6.3.7.

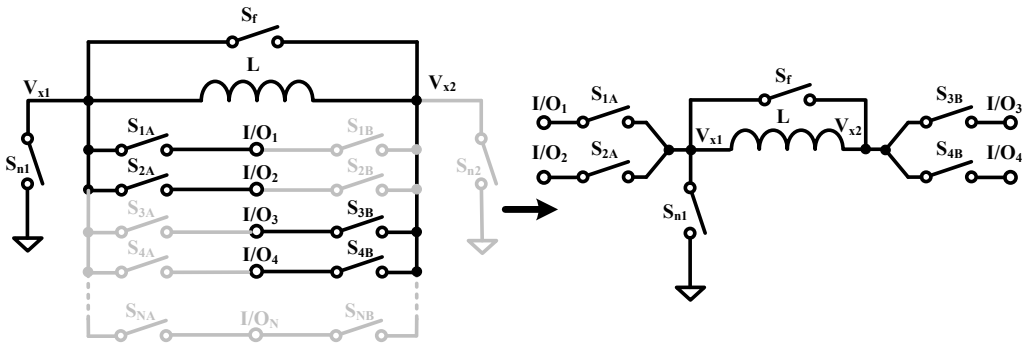


Figure 6.3.3 Extension of the proposed SI-MOMO converter power stage: achieving SI-DIDO buck converter.

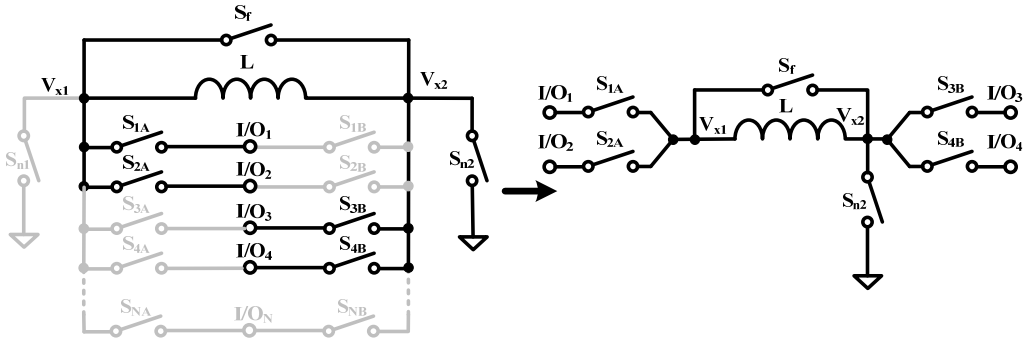


Figure 6.3.4 Extension of the proposed SI-MOMO converter power stage: achieving SI-DIDO boost converter.

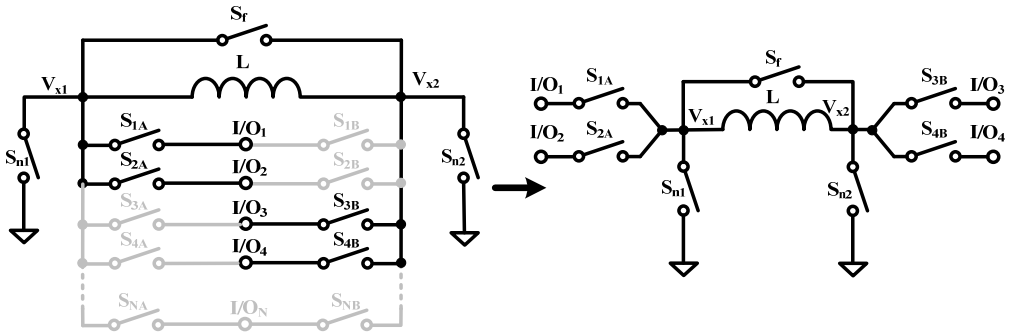


Figure 6.3.5 Extension of the proposed SI-MOMO converter power stage: achieving SI-DIDO buck-boost converter.

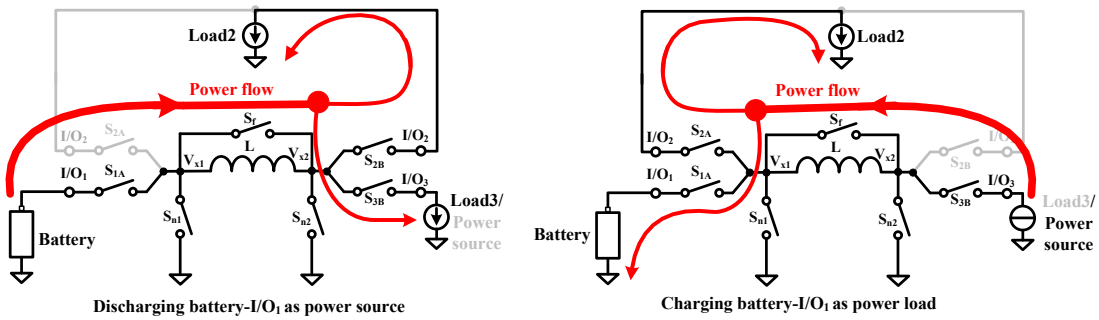


Figure 6.3.6 Extension of the proposed SI-MOMO converter power stage: achieving bi-directional SI-DIDO converter.

One problem exists in SIMIMO converter lies in that the regulation time allocated to each output are much shorter than a conventional single output converter as shown in Figure 6.3.8, if the number of the outputs are high. If a sudden load change occurs at one output, the converter will wait until the corresponding regulation phase becomes effective and then enables the response. This, in general, will slow down the transient response. To enhance the transient performance without adding extra inductive components, we are investigating the effectiveness of introducing a switched-capacitor (SC) power path. Similar to its switching converter counterparts, this SC path is also reconfigurable and can be adaptively switched to the most power-hungry loads to avoid the large voltage drop caused by the slow transient response. Figure 6.3.9 illustrates one possible architecture of the proposed power stage. We will continue on our

design and simulation to verify and evaluate the performances of the proposed power stage architecture in the next task period.

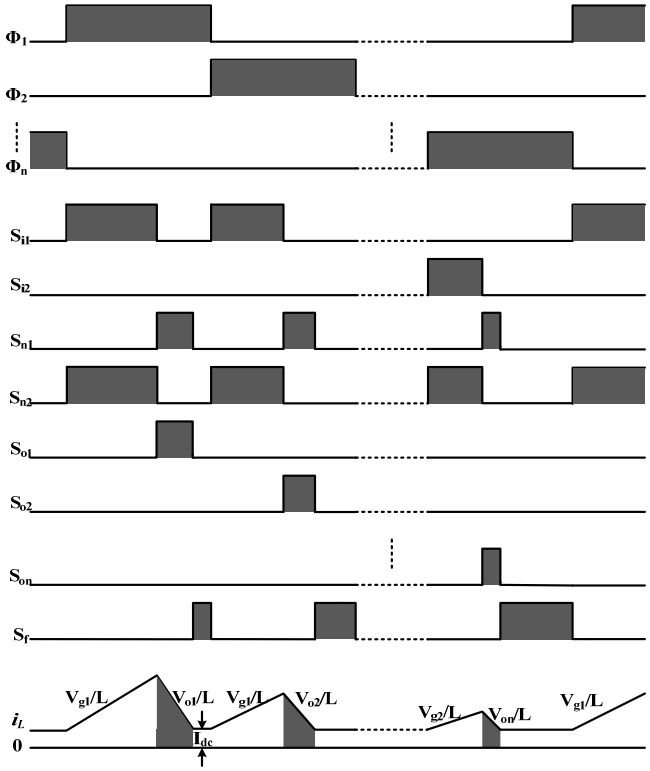


Figure 6.3.7 One timing diagram of the SIMIMO converter.

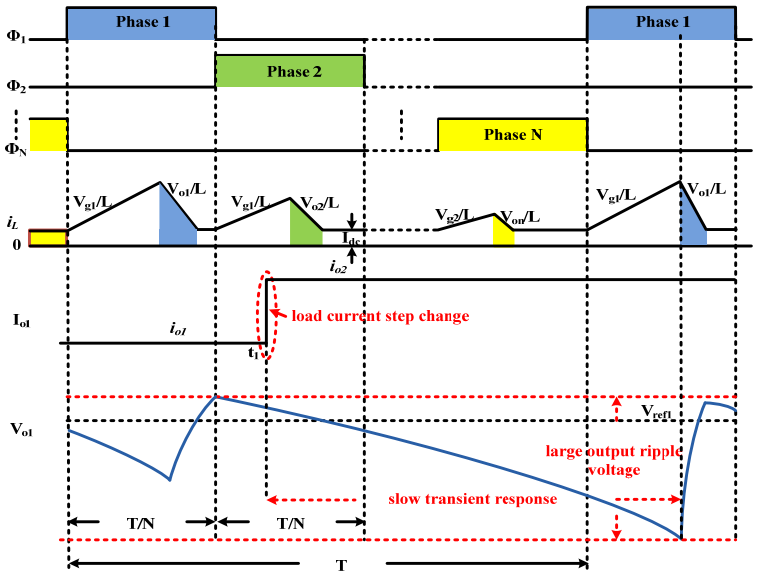


Figure 6.3.8 A potential drawback of the proposed SIMIMO converter.

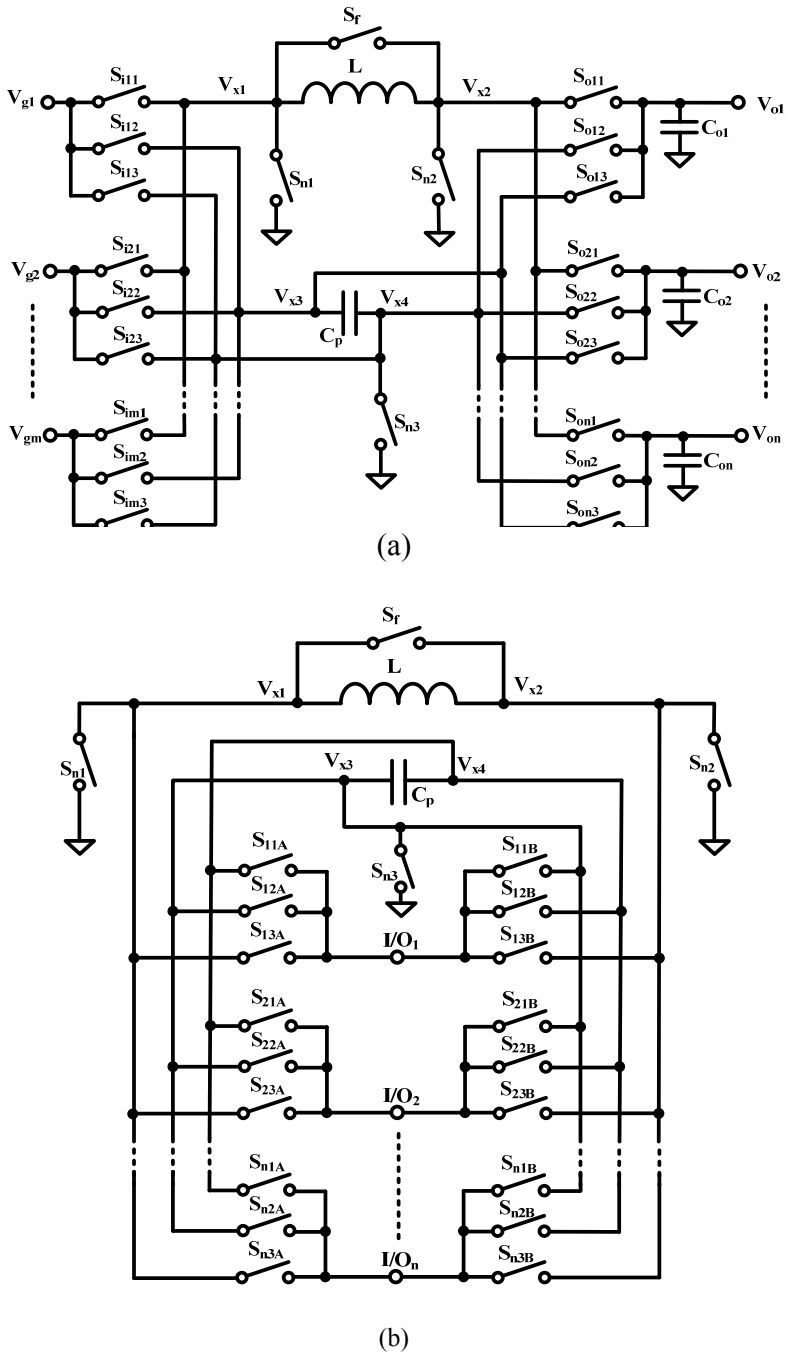


Figure 6.3.9 (a) The proposed step-up/down SI-MIMO converter with SC power path, and (b) a generic topology.

B. Bi-Directional Power Path Performance

Bi-direction power flow is also tested. When the system faces a sudden and large load transient, the input power is not sufficient for this dramatically change, the output voltage will

drop below the desired level. As shown in Figure 6.3.10, when V_{oa} has a sudden big load change, V_{in} is not enough for the change, all three output has large dynamic changes, the voltage violation is among 200 mV or even drop below the desired level.

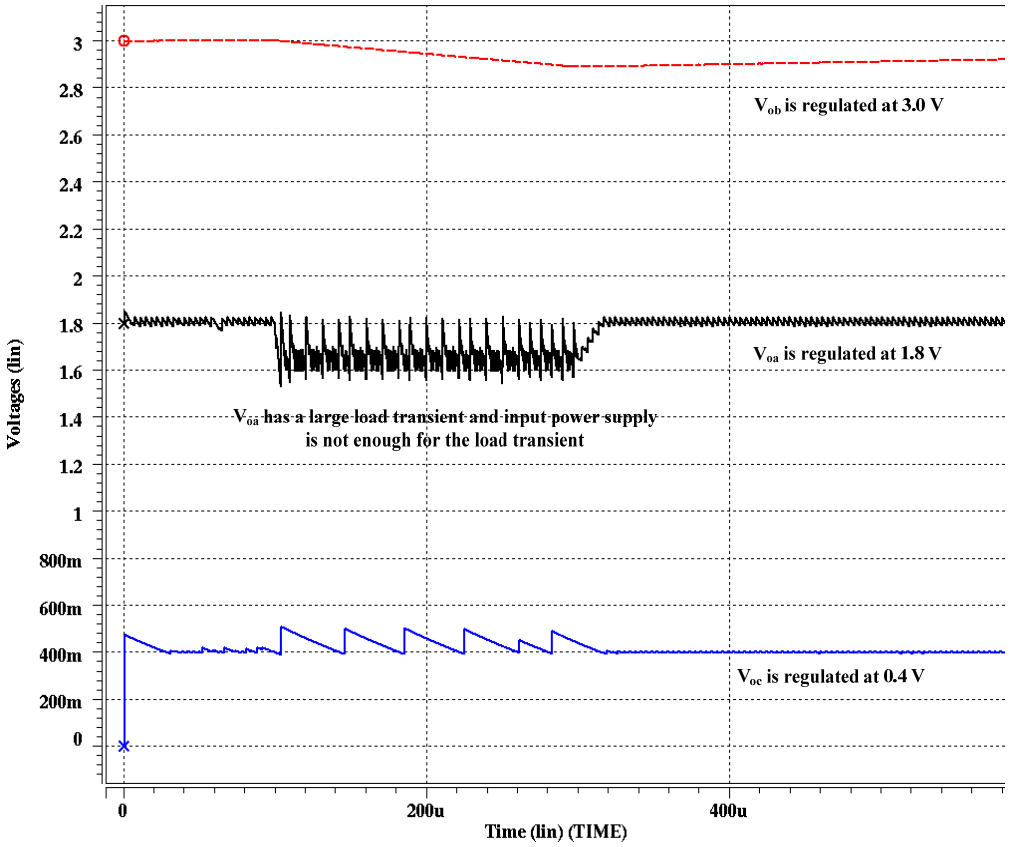


Figure 6.3.10 Simulated three output voltages when the input power is smaller than the total power demands: without bi-directional power control.

With our proposed bi-direction power path, at this condition, transistor M_{bb} will turn on, and V_{ob} will become a second power source and deliver power to the other two outputs. As shown in Figure 6.3.11, with the same test condition as Figure 6.3.10, V_{oa} and V_{oc} will stay constant at their desired regulated level: 1.8 V and 400 mV, respectively, with less than 50 mV voltage violation.

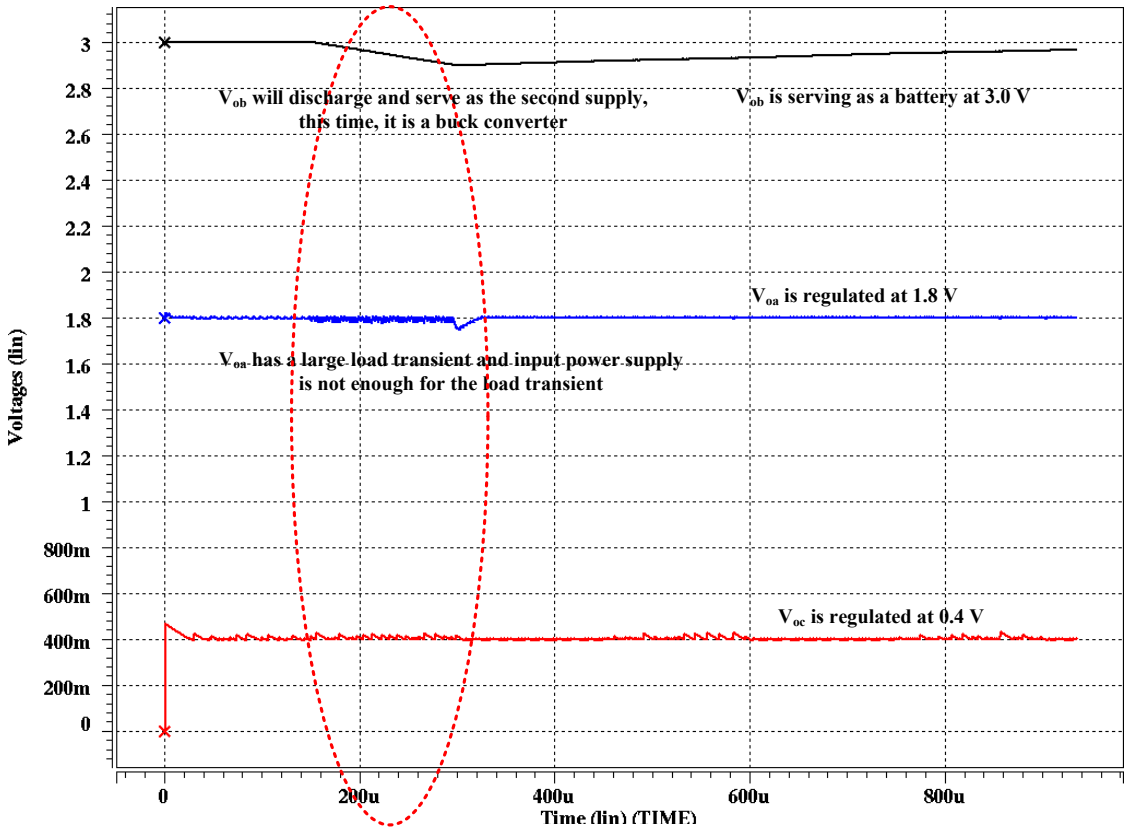


Figure 6.3.11 Simulated three output voltages when the input power is smaller than the total power demands: with bi-directional power control.

6.3.2 Thermal Sensing and Thermal Shutdown Circuit

Temperature sensors are incorporated in a number of electronic circuits for a variety of purposes. For example, dissipation by integrated circuits exceeding a safe temperature limits needs to be signaled so that the dissipation can be controlled. In addition, the operating temperature range for a particular electronic system may have to be limited [Matranga].

Conventionally, thermal sensing circuits are designed using a constant temperature-independent reference voltage. Typically, Bandgap reference circuit is used for this purpose, and a thermal sensor and a comparator. Figure 6.3.12 shows the block diagram of this type of thermal sensing circuit. As a result, the reference circuit is typically complex and includes a relatively

large number of components and occupies a relatively large area on the chip. It would be desirable to be able to provide systems and methods for thermal sensing that are less complex, and that require less area of the chip [Yoshida].

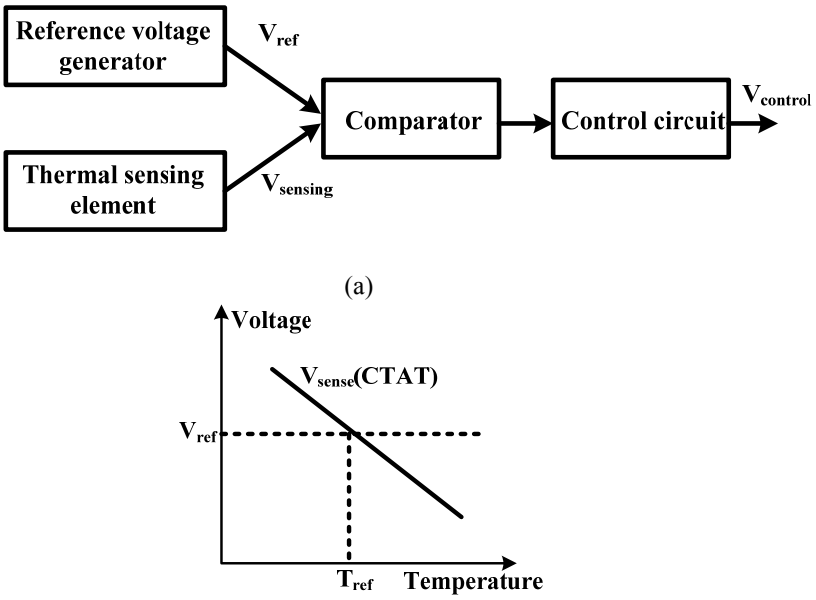


Figure 6.3.12 (a) Block diagram of one thermal sensing circuit, and (b) corresponding V_{ref} and V_{sense}.

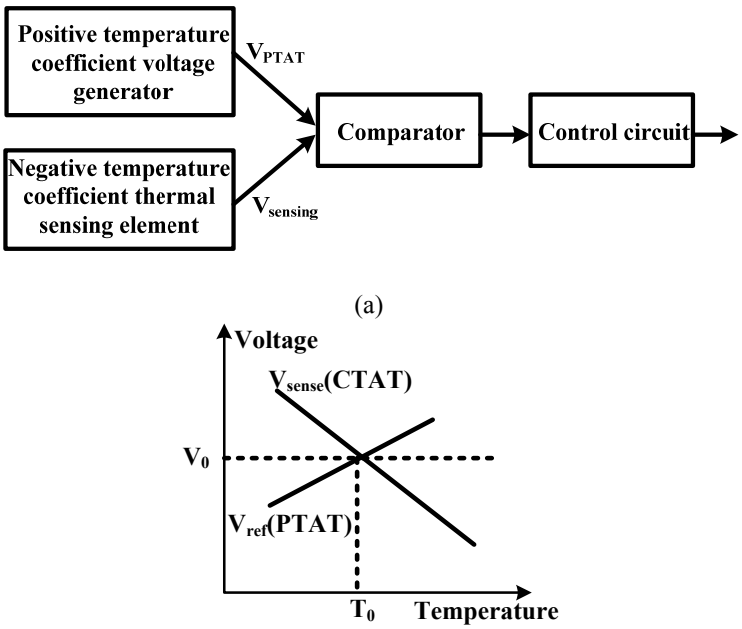


Figure 6.3.13 (a) Block diagram of our proposed thermal sensing circuit, and (b) corresponding V_{ref} and V_{sense}.

The block diagram of the proposed thermal sensing circuit is shown at Figure 6.3.13. As we can see, the generation of a reference voltage that increases with temperature is typically easier than the generation of a constant reference voltage, so the reference voltage generation circuit is less complex. Additionally, the differences between the sensing voltage and the reference voltage are greater in the proposed design, which is easier to amplify than the small voltage difference in previous design.

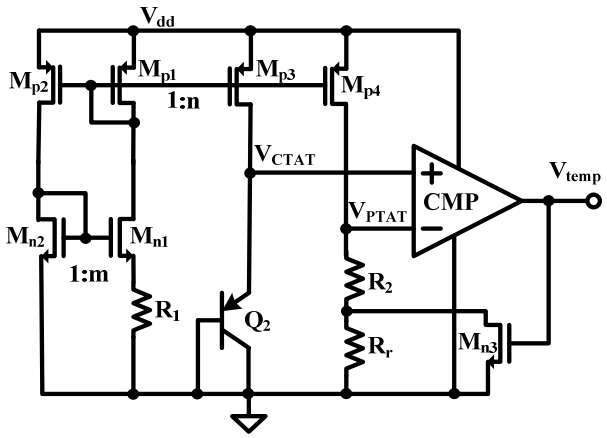


Figure 6.3.14 Schematic of the thermal sensor/thermal shutdown circuit.

Figure 6.3.14 shows the schematic of the CMOS thermal sensing and thermal shutdown circuit. In general, temperature can be measured in integrated circuits on the basis of a voltage differential ΔV_{be} which is proportional to temperature (PTAT), and a voltage value which is proportional to V_{be} and decreases linearly with temperature (CTAT). As we can see, M_{n1}, M_{n2}, M_{p1}, M_{p2}, M_{p4}, R_1, and R_2 form the PTAT voltage sensor, which generate a linearly increasing voltage with the temperature to be detected. Q_2 is a vertical bipolar transistor and is diode connected as an element which provides a voltage value decreasing linearly with the temperature (CTAT). By adjust the resistance of R_2, V_{PTAT} can be generated to be equal to the V_{CTAT}. The comparator will detect the difference of V_{PTAT} and V_{CTAT}, and determine when the temperature of the circuit which accommodates the sensor reaches a predetermined target value.

Advantageously, the PTAT sensor only operates on resistance and eliminates all the problems connected with process spread and/or the resistor thermal coefficients. And, all the transistors are to be operated in the sub-threshold region. By operating in sub-threshold region, the consumption of the PTAT sensor can be kept quite low. The voltage V_{PTAT} is calculated as:

$$V_{PTAT} = \frac{\left(W/L\right)_{M_{P4}}}{\left(W/L\right)_{M_{P1}}} \cdot \frac{R_2}{R_1} \cdot V_t \cdot \ln\left[\frac{\left(W/L\right)_{M_{P2}}\left(W/L\right)_{M_{n1}}}{\left(W/L\right)_{M_{P1}}\left(W/L\right)_{M_{n2}}}\right], \tag{6.1}$$

Where V_t=kT/q, with k being Boltzman's constant and q the electron charge.

The circuit in Figure 6.3.14 also provides a hysteresis of the switching temperature to make it more accurate, and prevent possible oscillations in the comparator output and make the sensor immune to noise. This hysteresis is generated by the M_{n3} and R_r. When the temperature is below the triggering temperature, V_{temp} is high, which turn on M_{n3}, R_r is shorted; when the temperature is high and over the triggering temperature, V_{temp} become "0", and M_{n3} will be off and R_r is connected in as the comparator switches over. Thus, the V_{PTAT} is increased by approximately 10 millivolts in our design. R_r will again be short-circuited as temperature drops and the comparator switches over again. In this way, a hysteresis about 1-2 °C can be obtained in the triggering temperature, as illustrated by the simulation result in Figure 6.3.15, which shows the V_{PTAT} and V_{CTAT} versus temperature.

Figure 6.3.16 shows the simulation result of the thermal sensor/thermal shutdown circuit. The shutdown block generates a signal that turns off the power stage if the temperature of the internal chip goes higher than a fixed internal threshold (148 °C). The sensing element of the chip is very close to the power transistor area, so ensuring accurate and fast temperature detection. A hysteresis of approximately 1.5 °C avoids that the devices turns on and off continuously.

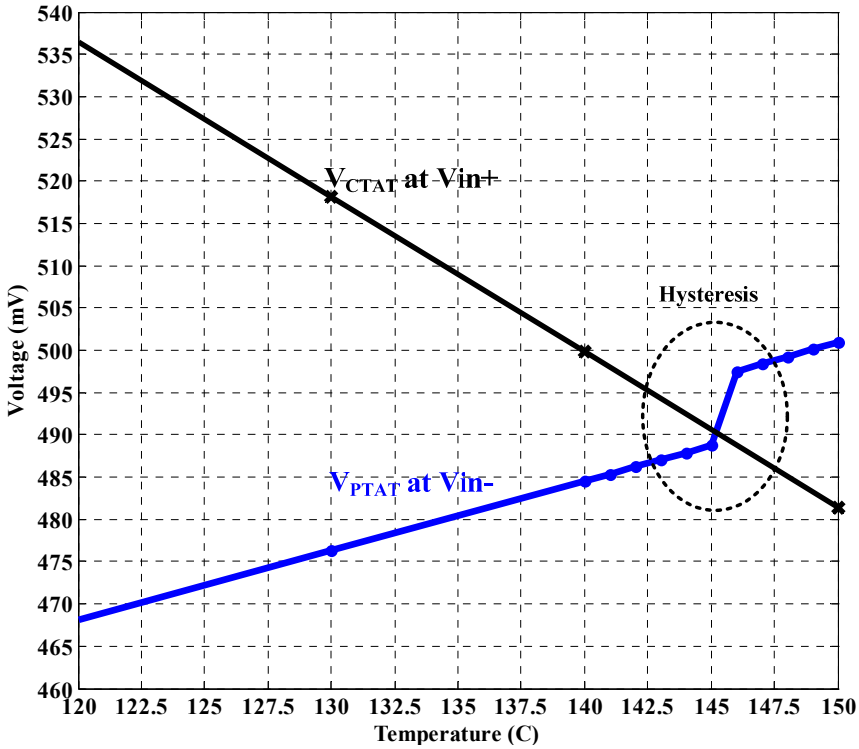


Figure 6.3.15 Simulated outputs of the PTAT and CTAT voltages with hysteresis.

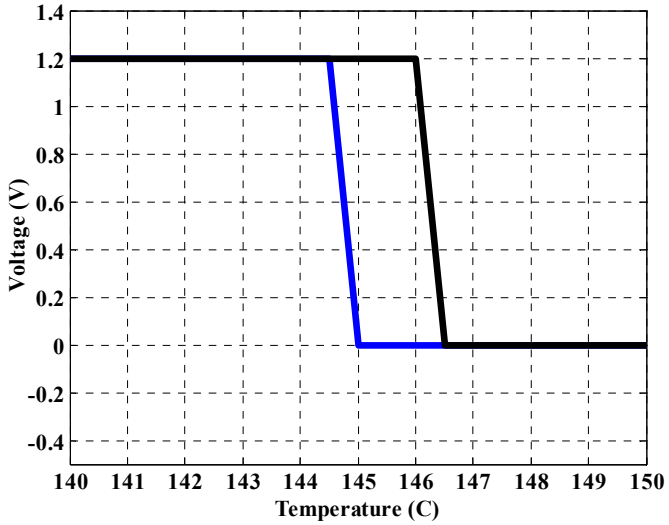


Figure 6.3.16 Simulated output of the thermal sensor/thermal shutdown circuit.

APPENDIX: PUBLICATION LIST

1. **F. Luo** and D. Ma, "A Periodically Kicked Chaos Circuit for Rank-One Attractor Generation", *IEEE International Midwest Symposium on Circuits and Systems* (***MWSCAS 2006***), Vol 1, pp: 192 – 196, Aug. 2006.

2. **F. Luo** and D. Ma, "An Integrated Switching Power Converter with a Hybrid Pulse-Train/PWM Control", *IEEE International Symposium on Circuits and Systems* (***ISCAS 2007***), pp: 305-308, May, 2007.

3. D. Ma and **F. Luo**, "Robust Multiple-Phase Switched-Capacitor DC-DC Power Converter with Digital Interleaving Regulation", *IEEE Trans. Very Large Scale Integrated Systems (**TVLSI**)*, Vol. 16, No. 6, pp: 611-619, Jun. 2008.

4. **F. Luo** and D. Ma, "Integrated Adaptive Step-Up/Down Switching DC-DC Converter with Tri-Band Tri-Mode Digital Control for Dynamic Voltage Scaling", *IEEE International Symposium on Industrial Electronics (**ISIE08**)*, pp: 142-147, Jun. 2008.

5. **F. Luo** and D. Ma, "A Low-Ripple Fast-Response CMOS Integrated Switching Buck Converter with Dual-Mode Pulse-Train/PWM Control", *IEEE Power Electronics Specialists Conference (**PESC08**)*, pp: 3432-3436, Jun. 2008.

6. **F. Luo** and D. Ma, "An Integrated Switching DC-DC Converter with Dual-Mode Pulse-Train/PWM Control"**,** *IEEE Trans. Circuits and Systems II (**TCASII**)*, Vol. 56, No. 2, pp: 152-156, Feb. 2009.

7. **F. Luo**, R. Bondade, and D. Ma, "Software-Defined SIMO Step-Up/Down Power Converter with Adaptive Global/Local Power Allocation Scheme for DVS-Enabled Multicore Systems", *International Symposium on Low Power Electronics and Design (**ISLPED09**)*, Aug. 2009, accepted for publication.

8. **F. Luo** and D. Ma, "An Adaptive Single Inductor Multiple Output Buck-Boost Converter with Digital Adaptive Power Allocation Control for Dynamic Voltage Scaling Application", ***TECHCON09***, Sept. 2009, accepted for publication.

9. **F. Luo** and D. Ma, "Design of Digital Tri-Mode Variable-Output Buck-Boost Converter for DVS-Enabled Integrated Systems", *IEEE Transaction on Industrial Electronics(**TIE**)*, submitted, 2009.

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