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# NOISE AT SUBTHRESHOLD CURRENT IN MOS DEVICES

by

Pirooz Hojabri

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A Thesis Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

In Partial Fulfillment of the Requirements
For the Degree of

MASTER OF SCIENCE
WITH A MAJOR IN ELECTRICAL ENGINEERING

In the Graduate College

THE UNIVERSITY OF ARIZONA

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John L Prince

JOHN PRINCE
Professor of Electrical and Computer Engineering

9/25/85
Date

## DEDICATION

This work is dedicated to my parents whose sacrifice, love and guidance paved my way through the past twenty-four years.

ACKNOWLEDGMENT

I wish to express my special thanks and gratitude to Professor John Prince for guiding my efforts in the right direction and providing a supporting atmosphere for the ideas to develop.

I also wish to express my great appreciation to Professor James Fordemwalt and Professor Barry Johnson for their constructive suggestions during this research.

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ABSTRACT

Theoretical considerations as well as experimental results show that it is possible to take advantage of the weak inversion behaviors in designing analog MOS circuits. Both dc circuits, such as current references, and ac circuits, such as an amplitude detector, a very low-current quartz oscillator and a bandpass amplifier, are insensitive to the threshold and the mobility variations, and are fully compatible with a low-voltage si-gate MOS technology. In order to use these circuits, we need to have some understanding of the behavior of the noises in the weak inversion region of an MOS transistor.

This research paper deals with shot noise, flicker noise, and thermal noise in the subthreshold region of an MOS field effect transistor. The experimental measurements confirm the theory for flicker noise as well as the input noise voltage behavior of an MOS device.

# SECTION 1

# INTRODUCTION

The objective of this paper is to investigate the behavior of noises (especially shot, thermal and flicker) at subthreshold current in MOS technology.

In order to achieve the above objective, the weak inversion region and the drain current at subthreshold of a MOS transistor should be determined.

## Weak Inversion

Model of a p-channel MOS device operated with different gate voltages is shown in Figure 1. The study of these regions will give us a thorough understanding of factors that influence the theshold. A p-channel enhancement model is used in these derivations, and the only modification for the n-channel enhancement mode in these derivations would be a change of sign.

According to Botchek [1], in the p-channel MOSFET, all positive voltages applied to a gate with respect to ground (n-bulk) cause electrons to accumulate under the gate oxide. This accumulation is higher than the concentration of electrons deeper in the bulk, and it is called the accumulation region. If the polarity of the gate voltage

is reversed, a small negative voltage will prevent the accumulation so that the electron concentration throughout the bulk, and immediately under the gate oxide, are identical. This model is called the flat band condition because all levels in the band diagram are flat. A further increase of negative potential on the gate causes a concentration of holes in the silicon under the gate. The electric field depletes electrons producing a depleted region which increases the effective gate to bulk dielectric thickness and reduces the capacitance. Larger negative voltages on the gate widen this depleted region until the electric field depletes all the available electrons. An even larger gate voltage produces a concentration of holes in excess of electrons (under the gate surface), so that conduction can occur between source and drain. In this case, the depleted region reaches a maximum width and the excess concentration of holes produces an inverted region. According to the majority of the authors, the point at which the depletion region reaches the maximum width is called the onset of strong inversion or threshold condition. Therefore, the threshold is commonly taken to be the gate-to-source voltage ($V_T$) for this condition. Most of the definitions state that when $|V_{GS}| < |V_T|$, the drain current will immediately go to zero but this is not the case. An alternative definition by Richman [2] is the "weak" inversion criterion, which is the

gate-to-source voltage Vi at which the surface minority carrier density at the source is just equal to the intrinsic carrier concentration (ni). For $|V_{GS}| < |Vi|$, the channel current is essentially zero, and the subthreshold region is defined as $|Vi| < |V_{GS}| < |V_T|$.

The theoretical explanation of (Vi) can be found by looking at the band diagrams for a p-channel device shown in Figures 2 and 3. The energy band diagram corresponding to accumulation (Figure 2) shows the mobile electrons in the conduction band, where it interfaces with the oxide. The Fermi level is shown as a flat line through the metal oxide and the silicon region. The accumulation of the mobile electrons has a higher electrostatic potential because the positive bias on the gate lowers the electron energy at the silicon surface where all the bands bend downward. Also, looking at the flat band condition in Figure 3 (uniform distribution of electrons throughout the bulk), all the valence, conduction, and intrinsic Fermi levels are flat because the positive charge $Q_G$ on the gate is equal to the fixed surface-state charge-density $Q_{SS}$ in the oxide. Therefore, looking at these two conditions we can conclude that the weak inversion (Vi) in the p-channel device occurs when the intrinsic band is just bent above $E_F$ at the surface (Figure 4).

Physically Vi for the p-channel enhancement device is the minimum gate voltage that produces a concentration

of holes in the silicon under the gate at least equal to $n_i$ and, therefore, produces a depletion region (Figure 1c). Hence, as a matter of definition it can be said that the subthreshold region is the region after the flat band and before the strong inversion conditions. Also, looking at the CV characteristics of a p-channel enhancement device in Figure 5 shows that the weak inversion (Vi) forms just between region a and region c, and the threshold is between region c and region d.

When the gate voltage is between Vi and $V_T$ ($|Vi| < |V_{GS}| < |V_T|$) the MOS device is in weak inversion, and the corresponding drain current is called the subthreshold current.

## Subthreshold Current

In the region $|Vi| \leq |V_{GS}| \leq |V_T|$ the drain current is due solely to the diffusion of carriers between the source and the drain because the increase of $V_{GS}$ in this region will only increase the width of the depletion region and will not produce any lateral electrical field and hence drift current.

Troutman and Chakravarti [3] have derived a model valid for any substrate bias and extendable to short channel lengths; they have also shown mathematically that the channel current in weak inversion flows by diffusion. The current at weak inversion can be derived in the same way as the collector current in a bipolar transistor with homogeneous

base doping. Considering the MOSFET as an n-p-n (source-substrate-drain) bipolar transistor, we have:

$$I_D = -qAD_N \frac{\partial_N}{\partial_Y} = qAD_N \frac{n(o) - n(L)}{L} \tag{1}$$

Where A is the cross section of the current flow, n(o) and n(L) are the electron densities in the channel at source and drain. The electron densities are given by:

$$n(o) = np_o e^{\beta\psi_S} \tag{2}$$

$$n(L) = np_o e^{\beta\psi_S - \beta V_D} \tag{3}$$

where $\psi_S$ is the surface potential at the source and $\beta$ is equal to $\frac{KT}{q}$ . The area of current flow is given by the width Z and the effective channel thickness normal to the semiconductor-insulator surface. Because of the exponential dependence of electron density on the potential $\psi_S$, the effective channel thickness corresponds to the distance in which $\psi_S$ decreases by $\frac{KT}{q}$ . Therefore, the effective channel thickness is $(\frac{KT}{q})\,\varepsilon_S$. $\varepsilon_S$ is the weak-inversion surface field given by:

$$\varepsilon_S = -\frac{Q_B}{E_S} = \sqrt{2qNA\psi_S/E_S} \tag{4}$$

where:

$E_S$ = semiconductor permittivity

$E_i$ = insulator permittivity

$Q_B$ = charges within surface depletion region

$q$ = electric charges = $1.602 \times 10^{-19}$C

$\psi_S$ = surface potential at the source

Substituting equations (2),(3), and (4) into (1) gives [4,5,6]:

$$I_D = \mu_n (Z/L) \frac{a C_i}{2\beta^2} \left(\frac{ni}{NA}\right)^2 \left[1-e^{-\beta V_D}\right] e^{\beta\psi_S} (\beta\psi_S)^{-\frac{1}{2}} \tag{5}$$

In equation (5) we have used

$$D_N = \frac{\mu_n KT}{q} \quad , \quad a = \sqrt{2}\ (E_S/L_D)/C_i \quad , \quad L_D = \left[\frac{KTE_S}{NAq^2}\right]^{\frac{1}{2}}$$

where $C_i \equiv E_i/d$ is the capacitance per unit area. Now using equation (5), Swanson and Meindl [7], Barron [8], and also Vittoz and Fellrath [9] have completed a simple model for the subthreshold current which is in terms of the gate, source and drain voltages. This is discussed below.

## Simple Model in Weak Inversion

In a simple model for weak inversion the following assumptions are made:

1. The channel is sufficiently long so that the gradual channel approximation can be used and channel-length modulation effects are negligible.
2. Generation currents in the drain, source, channel and depletion region are negligible; source and drain currents are then equal.

3. The fluctuation of surface potential is negligible.

4. Due to very slow variation of $C_d$ with $\psi_S$, $I_D$ essentually depends exponentially on $\frac{\psi_S}{U_T}$. The subthreshold current ($I_D$) under these assumptions is given by [9]:

$$I_D = S\, I_{D_o}\, e^{V_G/nU_T} \left[ e^{-(V_S/U_T)} - e^{-(V_D/U_T)} \right] \qquad (6)$$

where $I_{D_o}$ is a characteristic current and (n) is a slope factor.

$$n = 1 + \frac{C_d}{C_{ox}}$$

$C_d$ = total surface capacitance per unit area

$C_{ox}$ = oxide capacitance per unit area

$\psi_S$ = surface potentials constant along the channel in weak inversion

$V_S$ = source-to-substrate voltage

$V_G$ = gate-to-substrate voltage

$V_D$ = drain-to-substrate voltage

$I_D$ = drain current

S = geometric shape factor of transistor (W/L)

W = width of channel

L = length of channel

$U_T = \beta = \frac{KT}{q}$

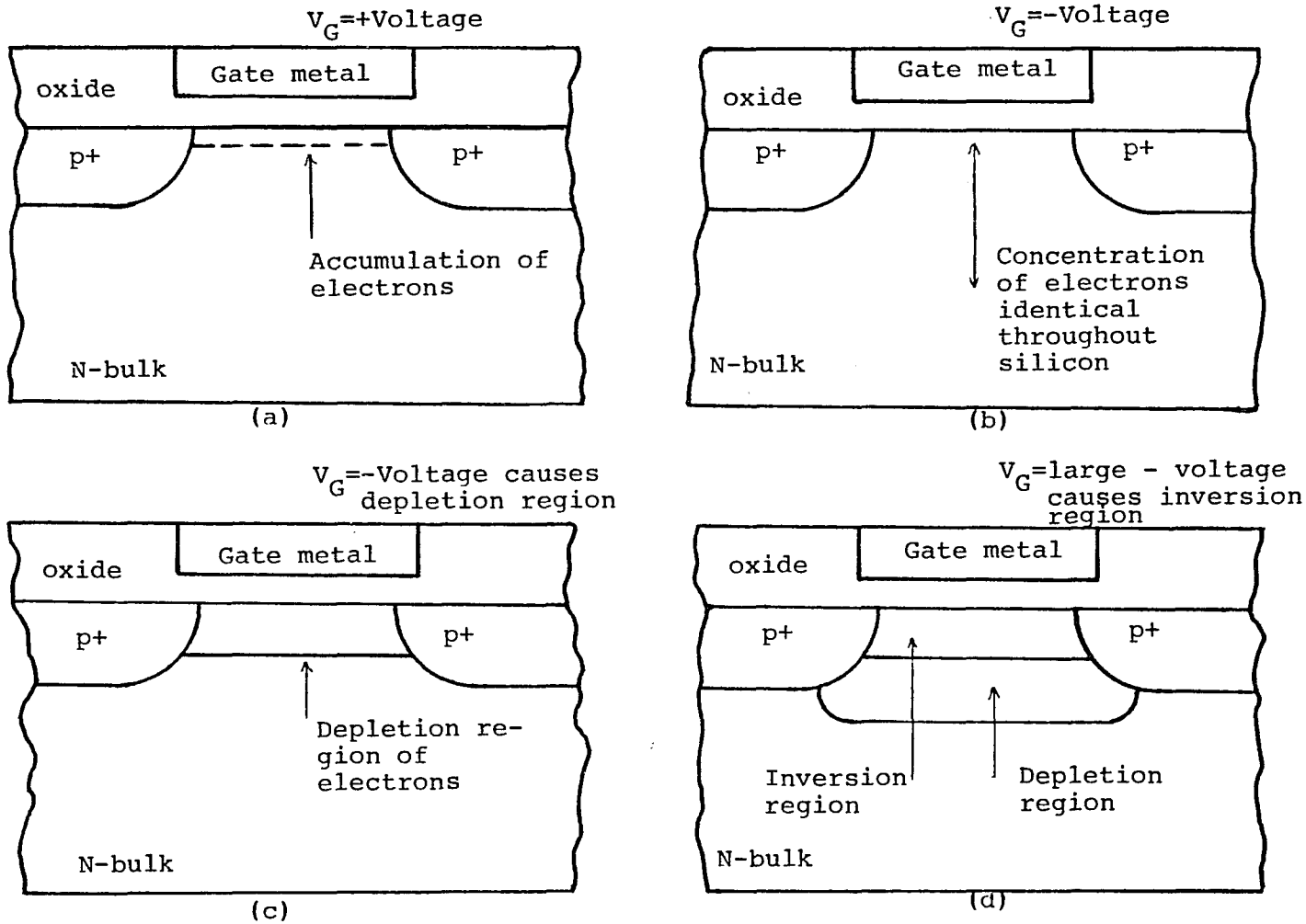
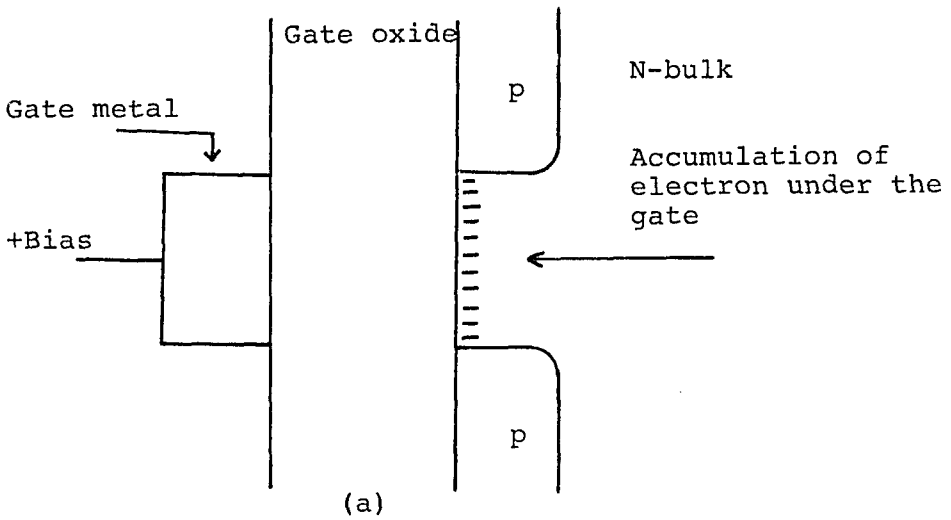



Figure 1. Model of a p-channel MOS device. (a) accumulation; (b) flat band; (c) depletion; (d) inversion



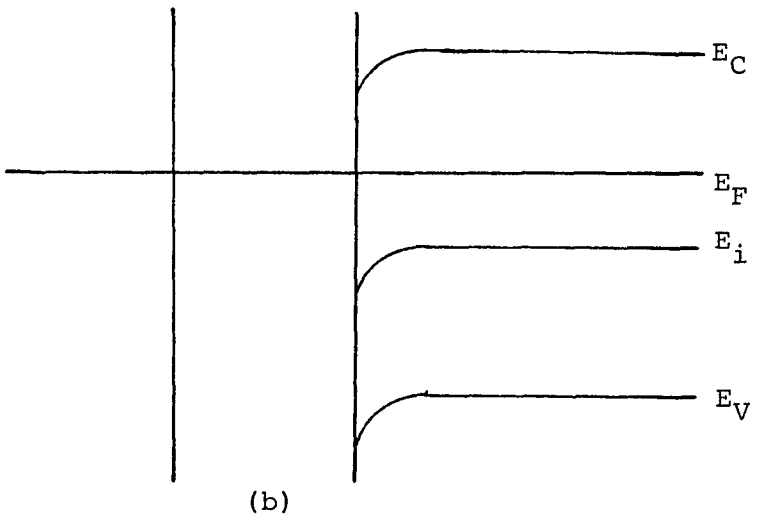
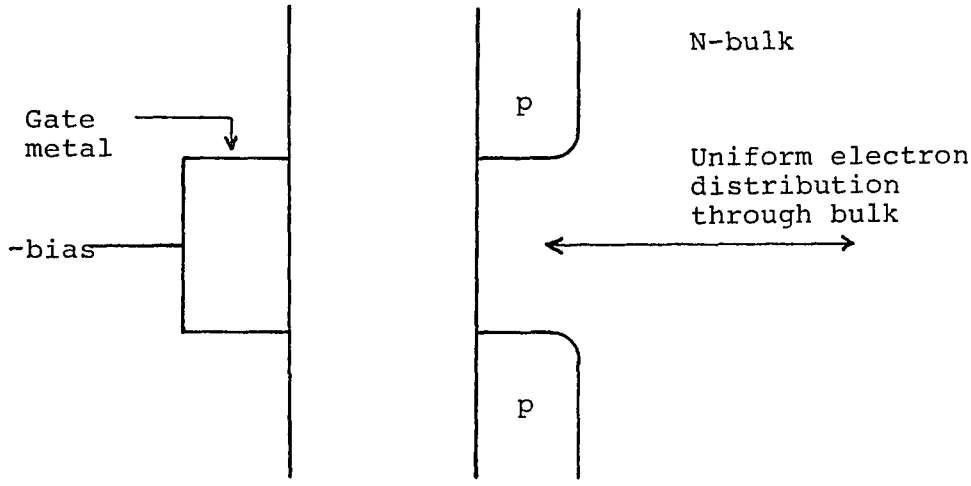
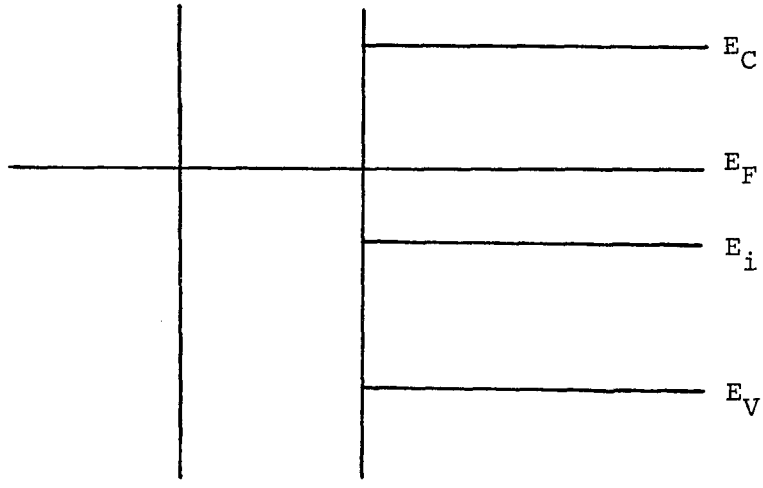




Figure 2. Accumulation model. (a) Device model; (b) Band model.




(a)




(b)

Figure 3. Flat band model. (a) Device model; (b) Band model.

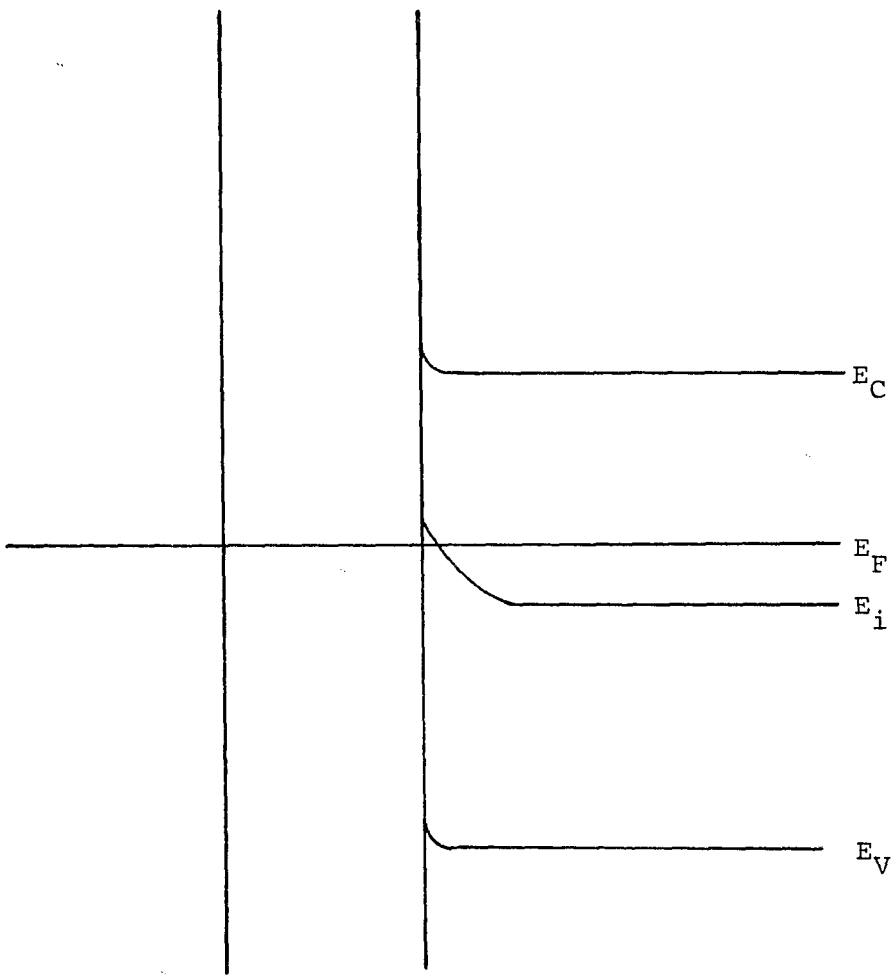



Figure 4. Band model for the onset of inversion.

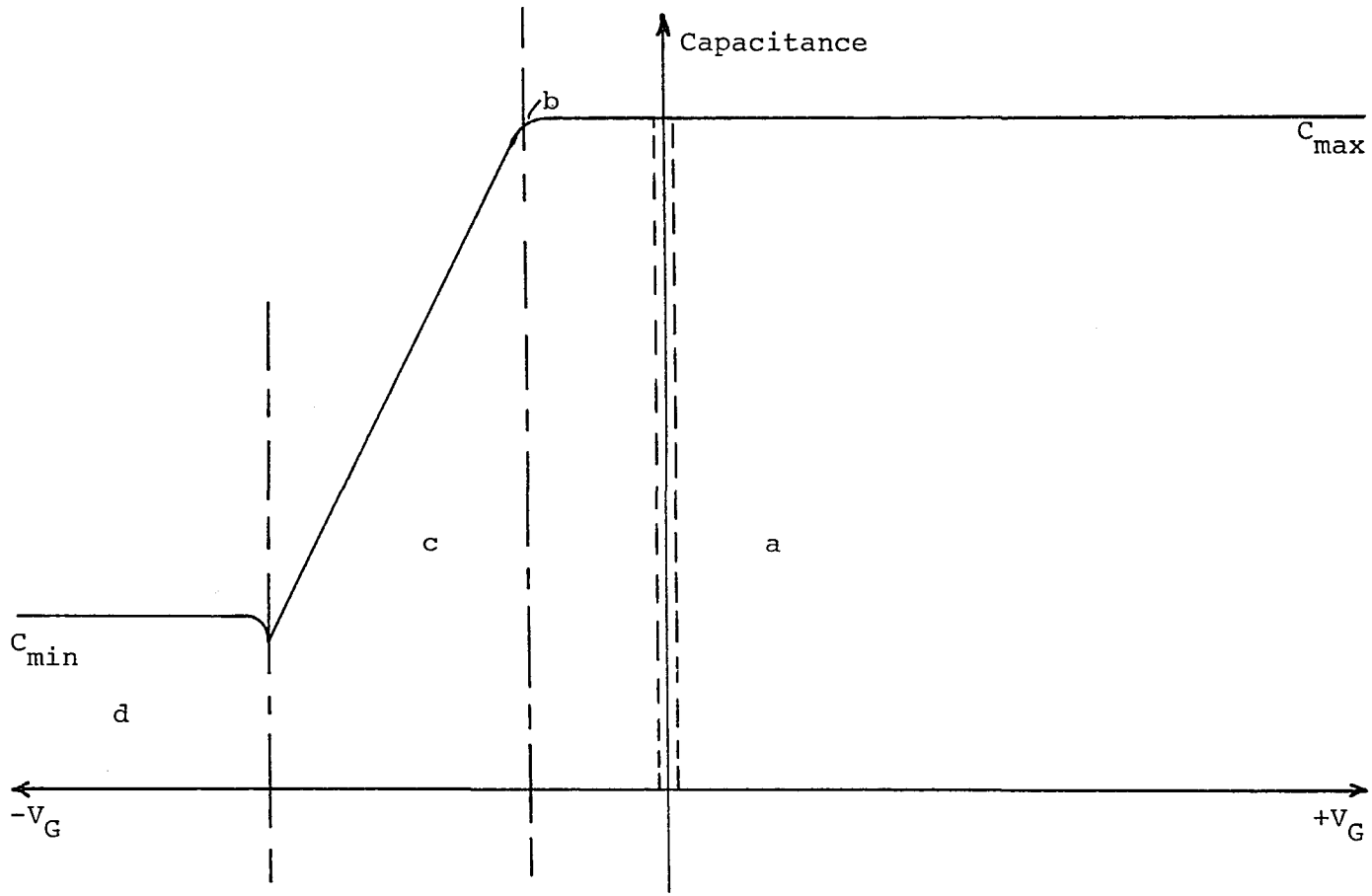



Figure 5. CV characteristics for a P channel device. (a) accumulation region; (b) flat band point; (c) depletion region; (d) inversion region.

# SECTION 2

# NOISE THEORY

## Introduction

The known weak inversion behavior of the MOS transistor was described in previous discussions, and it was shown that the drain current is due to diffusion of the carriers. In this section a model for calculation of thermal and shot noises will be offered.

In addition to thermal and shot noises, it is known that MOS transistors exhibit a flicker (1/f) noise. We will try to offer some explanations for 1/f noise and arrive at an approximation for its behavior.

### Thermal Noise

Any electrical system at a finite temperature has a thermal noise associated with the resistances existing between any two nodes of the system. This is also referred to as Johnson noise. The motions of carriers between collisions constitute currents and these will cause a fluctuating voltage to appear across the terminals of any resistance.

The magnitude of the thermal noise is given by the Nyquists theorem [23]. The thermal noise of a resistance R

kept at the temperature T can be represented by $[\overline{V_N^2}]^{\frac{1}{2}}$ in series with R ($\overline{V_N^2} = 4KTR\Delta f$) or by a noise current generator $[\overline{i_N^2}]^{\frac{1}{2}}$ in parallel with g = 1/R ($\overline{i_N^2} = 4KTg\Delta f$). To calculate the input noise voltage of MOS transistor, we assume that the source and drain are short-circuited. The equivalent noise circuit of a MOS in high frequency is given in Figure 6.

If we assume the parasitic resistances $r_s$ and $r_d$ are very small compared with the transconductance, the input noise current is given by:

$$\overline{i_d^2} = 4KTg_s\Delta f + 4KTg_{gs}\Delta f$$

where $g_s$ and $g_{gs}$ are the source and gate input conductances. The input noise voltage is given by:

$$\overline{V_N^2} = 4KTR_{NS}\Delta f + 4KTR_{NG}\Delta f = \overline{V_N^2} = 4KT(R_{NG} + R_{NS})\Delta f \tag{7}$$

where:

$R_{NS}$ = input noise resistance of the source

$R_{NG}$ = input noise resistance of the gate

The Nyquists theorem holds for any conductor at thermal equilibrium (no direct current is flowing). It also holds for most conductors through which direct current is flowing, as long as the carrier density in the sample

does not fluctuate. In contrast, shot noise only manifests itself when the conductor is carrying current.

Shot Noise

When a direct current flows through a MOSFET device carriers are generated and recombine. The carrier density shows spontaneous fluctuations; therefore, the noise resistance (i.e. $R_{NS}$, $R_{NG}$) of the MOS transistor will fluctuate. This direct current flowing through the device transforms these fluctuations into a noise which is called shot noise at the device terminals. This means that instead of a perfectly smooth flow of current through the device, the carriers tend to move in a more "jerky" fashion.

The mean square fluctuation in current (shot noise) for a noise bandwidth $\Delta f$ is given by:

$$\overline{i_N^2} = 2qI\Delta f$$

where I is direct current and q is the carrier charge. For a MOS device, the shot noise is:

$$\overline{i_N^2} = 2qI_D\Delta f \tag{8}$$

where:

$I_D$ = Drain current

Noise Modeling

We can conclude from the above discussion that shot noise and thermal noise are related through the input noise

resistances (i.e. $R_{NS}$, $R_{NG}$); therefore, in a MOS device carrying a direct current, the shot and thermal noise will be interrelated and one is dependent on the other. Also, it is known that both thermal and shot noises are essentially white. This means that the power spectrum of these two noises are uniform over the range of frequencies.

In order to find a noise model, we must divide the d.c. current into physically distinct components and then identify a separate noise model for each distinquishable group of carriers.

We have shown that diffusion dominates channel current injected by the source-to-gate junction which flows near the surface with a very long diffusion length and is collected by the drain. Neglecting the generation currents in the space charge region of the source, channel and drain, the diffusion current remains as the only component.

The shot noise current related to the diffusion of carrier is given by equation (8):

$$\overline{i_{DN}^2} = 2qI_D\Delta f \tag{8}$$

where:

$q$ = the charge of electron

$\Delta f$ = the bandwidth

$I_D$ = drain current

According to its physical origin, the drain current can be represented by a current source $\overline{i^2_{DN}}$ between the source and the drain.

When the MOS device is reduced below $V_t$ (threshold voltage) value, the transistor enters the weak inversion region. According to equation (6) the drain current in this region is given by:

$$I_D = S\, I_{D_o} \exp\left(\frac{V_G}{nU_T}\right)\left[\exp\left(-V_S/U_T\right) - \exp\left(-\frac{V_D}{U_T}\right)\right]$$

$V_G$ = gate voltage with respect to substrate

$V_S$ = source voltage with respect to substrate

$V_D$ = drain voltage with respect to substrate

S = geometrical factor of the transistor (effective width over effective length of channel) = W/L

$I_{D_o}$ = characteristic current

$U_T = \beta = .0259v = \frac{KT}{q}$

K = Boltzman constant

T = temperature

n = slope factor

Now we can define a gate and source transconductance: (assuming $V_D >> U_T$, the transistors operating in saturation)

$$g_{m_G} = \frac{\partial I_D}{\partial V_G} = \frac{1}{nU_T} \underbrace{SI_{D_o} \exp\left(\frac{V_G}{nU_T}\right)\left[\exp\left(-\frac{V_S}{U_T}\right) - \exp\left(-\frac{V_D}{U_T}\right)\right]}_{I_D}$$

$$g_{m_G} = \frac{I_D}{nU_T} \tag{9}$$

Assuming $V_D >> U_T \Rightarrow \exp(-\frac{V_D}{U_T}) = 0$, $g_{m_S} = \frac{\partial I_D}{\partial V_S}$

$$g_{m_S} = -(1/UT)SI_{D_o} \exp(\frac{V_G}{nU_T}) \underbrace{\left[\exp(-\frac{V_S}{U_T})\right]}_{I_D}$$

The minus sign changes the direction of $I_D$

$$g_{m_S} = -\frac{I_D}{U_T} \tag{10}$$

The input noise voltage (thermal noise) is given by (7):

$$\overline{v_N^2} = 4KT\Delta f \overbrace{(R_{NS} + R_{NG})}^{R_N} \tag{7}$$

where $R_N$ is an equivalent input noise resistance.

Since the shot noise equation (8) and thermal noise equation (7) are related through $R_N$ and shot noise is due to direct fluctuation of $R_N$ (for transistors operating with $V_D >> U_T$), from equation (7) we can conclude:

$$\overline{v_{NG}^2} = 4KT\Delta f R_{NG} = \frac{\overline{i_{DN}^2}}{g_{m_G}^2} \tag{11}$$

$$\overline{v_{NS}^2} = 4KT\Delta f R_{NS} = \frac{\overline{i_{DN}^2}}{g_{m_S}^2} \tag{12}$$

$R_{NG}$ = gate input shot noise resistance

$R_{NS}$ = source input shot noise resistance

Therefore, from equations (7), (8), (9), (10), (11), and (12):

$$R_{NG} = \frac{2qI_D\Delta f}{4KT\Delta f} \cdot \frac{1}{g_{m_G}^2} = \frac{n^2}{2} \cdot \frac{U_T}{I_D} \tag{13}$$

$$R_{NS} = \frac{2qI_D\Delta f}{4KT\Delta f} \cdot \frac{1}{g_{m_S}^2} = \frac{1}{2} \cdot \frac{U_T}{I_D} \tag{14}$$

and from equations (13) and (14) we have:

$$\overline{V_{NS}^2} = 4KT\Delta f \left(\frac{1}{2} \cdot \frac{U_T}{I_D}\right) \Rightarrow \frac{V_{NS}}{\sqrt{\Delta f}} = \sqrt{\frac{2KTU_T}{I_D}}$$

$$\overline{V_{NG}^2} = 4KT\Delta f \left(\frac{1}{2} \cdot \frac{n^2U_T}{I_D}\right) \Rightarrow \frac{V_{NG}}{\sqrt{\Delta f}} = \sqrt{\frac{2KTn^2U_T}{I_D}}$$

The total mean square input noise voltage is:

$$\overline{V_N^2} = 4KT\Delta f \left(R_{NG} + R_{NS}\right)$$

Therefore, the total equivalent input voltage noise is:

$$\frac{V_{N\,total}}{\sqrt{\Delta f}} = \frac{V_{NG}}{\sqrt{\Delta f}} + \frac{V_{NS}}{\sqrt{\Delta f}} \tag{15}$$

or

$$\frac{V_{N\,total}}{\sqrt{\Delta f}} = \gamma \left(\frac{1}{\sqrt{I_D}}\right) \tag{16}$$

Where $\gamma$ is a constant and is given by:

$$\gamma = \sqrt{2KTU_T(1 + n^2)}$$

Flicker Noise

1/f noise in MOS transistors has been studied by a number of investigators [10-21]. According to Newltorter [13] the flicker noise is due to trapping of carriers and there are two consequences of trapping of carriers in semiconductors:

1. It causes a direct change in current due to change in the number of free carriers.
2. It causes an indirect change in current due to a change in the number of trapped carriers. The random occupancy of surface states modulates the surface potential, which causes a fluctuation in surface recombination velocity.

According to Hsu [14], the 1/f noise in an MOS transistor is due to conduction channel charge density fluctuation caused by the modulation of surface potential due to the random occupany of surface states.

Unlike most others, this noise is not classified by associating a physical process with it. Instead, it is identified by the shape of the noise spectrum, especially since it has an inverse frequency dependance. As such, it overrides all other noise phenomena at low frequencies. This low frequency fluctuation is given the name flicker noise.

It has been argued that 1/f noise is an equilibrium phenomena and, although one has to pass an electric current through the sample to observe it, the current only reveals this noise and does not create it. It has further been argued that this noise is generated by fluctuations in the conductivity of the sample. The conductivity is just the product of electronic charges and the sum of all the carrier mobilities. Therefore, if we assume that the electronic charges do not fluctuate, the only quantities that can fluctuate are either the number of terms in the summation (number fluctuation) or the density of traps near the surface. Number fluctuation incorporates a surface effect. On the contrary, one can talk about mobility fluctuations even in the bulk and, hence, the mobility fluctuation is referred to as a bulk effect. Therefore, for quite some time there has been a controversy as to whether 1/f noise is a bulk effect or a surface effect [13,20]. Since MOSFETS are surface effect devices, we can safely conclude that number fluctuation is the main cause of flicker noise in the MOS devices.

In conclusion, we can say 1/f noise is caused by random trapping of free carriers in surface states which modulates the channel conductivity and, hence, produces fluctuations in drain current. From references [14] and

[15] (basically from experimental results) the flicker noise is proportional to:

$$\frac{V_{NF}}{\sqrt{\Delta f}} \propto 1/f \cdot \frac{1}{WL} \quad (WL = \text{gate area}) \tag{17}$$

Hints for Actual Measurement of the Input Voltage and Flicker Noise

Since the total input noise voltage ( $\frac{V_N}{\sqrt{\Delta f}}$ ) decreases with the increase of drain current where as flicker noise ( $\frac{V_{NF}}{\sqrt{\Delta f}}$ ) is constant, it is always possible by varying the drain current or measurement frequency to distinguish the two noise components. For low current and high frequency, the input noise voltage dominates, while the flicker noise dominates at high current and low frequency.

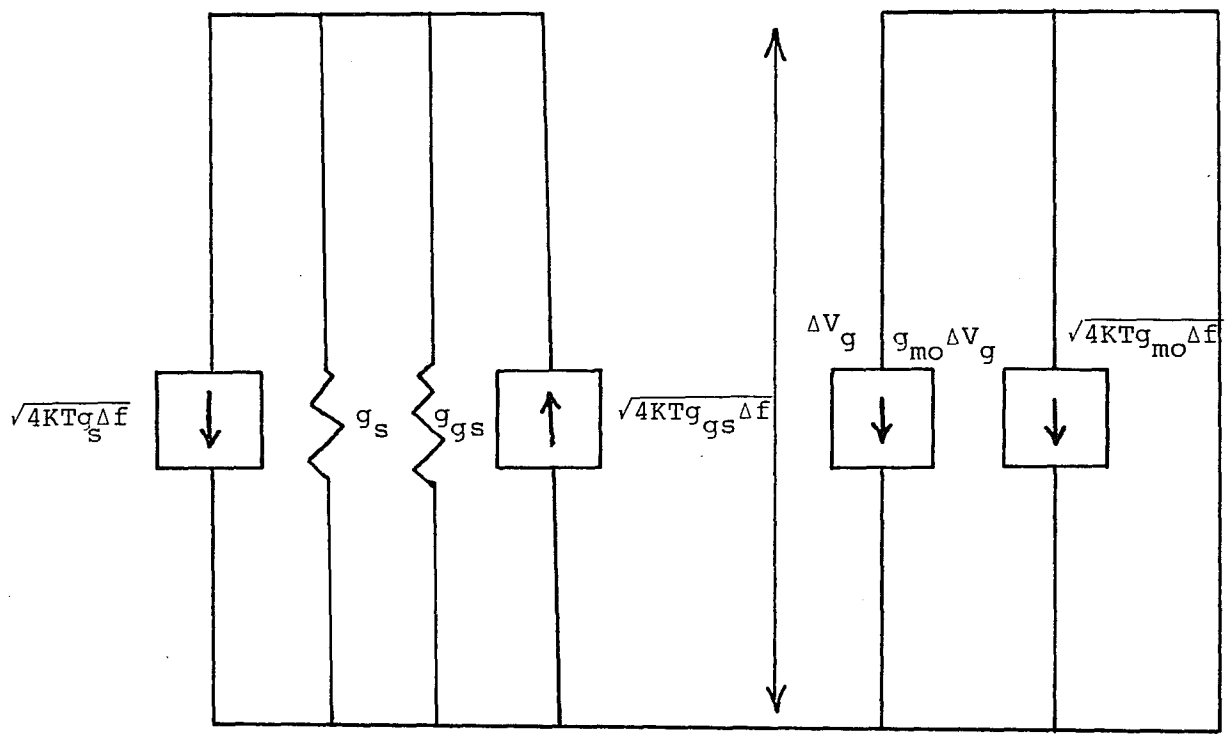



Figure 6. MOS device in high frequency.

## SECTION 3

## EXPERIMENTAL RESULTS

The intention of our work is to confirm experimentally the noise model that was offered in the previous section (i.e. equations 16 and 17). In the beginning we were experimenting with a spectrum analyzer in order to view the magnitude of the noise at different frequencies. Since to neglect the flicker noise, one has to work at a very small drain current; a low noise noninverting amplifier was used. But since we needed a very large gain, we had to use very large resistances. Metal film resistors were used to reduce the excess noise (non-Johnson noise) in the resistors. Unfortunately, the noise spectrum of the MOS test devices were falling under the noise spectrum of the op-amp and the metal film resistors, and it was impossible to measure the transistor noise with this spectrum analyzer.

An alternative noise measurement device (Appendix D, Figure D.1) was located at Burr-Brown [22]. The device was equipped with a low noise op-amp, an internal gain of 10,000, a self biasing network for MOSFETS, and had a selection switch for n and p channel MOS devices (Appendix D). After testing several n channel enhancement devices, we found that at subthreshold (i.e. very small current) the gain of the

device was not sufficiently large to detect any noise. To overcome this obstacle, we decided to use VMOS devices instead of regular MOS transistors because in the VMOS technology the drain current is larger than a regular MOS device, for identical gate voltages. A brief review of VMOS power MOSFET technology is offered as a supplement in Appendix A.

In these experiments three types of VMOS devices were used:

1. Intersil: VN98AK
2. Intersil: IVN5200TND
3. Siliconix: VN64GA

The specification of each type is given in Appendix C.

As a first step, it was necessary to find the threshold voltages for each test device. This was accomplished by measuring the drain current for different gate to source voltages (Appendix B, Table B.1) and drawing the ($\sqrt{I_D}$ versus $V_{GS}$), Figures 7, 8, and 9. The x-intercept of the line tangent to the curves in Figures 7,8 and 9 determines the threshold voltage. Then, the noise measurement at subthreshold currents were performed for each test device at different frequencies. Appendix B, Table B.2 shows the experimental result of the noise in $\left(\frac{nV}{\sqrt{Hz}}\right)$ for each device. In order to eliminate the flicker noise and evaluate the behavior of input voltage noise, from Appendix B, Table B.2

we draw the noise ($\frac{nV}{\sqrt{Hz}}$) versus subthreshold current at 10KHz for each device in Figures 10, 11, and 12 (the transistors are operated in saturation). We notice that all the transistors have the predicted low current given by equation (16) which corresponds to the input voltage noise. The same set of figures (10, 11, and 12) also shows that at high currents, the noise does not depend on the current because at these currents the device is entering the threshold region and the value of the noise decreases with the gate area (WL) and depends upon the channel conductance and technology.

Using Appendix B, Table B.2 we can also draw frequency (Hz) versus noise ($\frac{nV}{\sqrt{Hz}}$) at high current (i.e. magnitude of shot noise is minimal) for three devices (Figures 13, 14 and 15). Again, it is noted that all the transistors have the predicted behaviors of flicker noise given by equation (17). However, at high frequency, the magnitude of flicker noise is very small; therefore, we can see some shot noise contributions at these frequencies (i.e. Figures 13, 14 and 15).

We also decided to evaluate the effect of ionizing radiation on the same devices. The source of radiation was cobalt 60. (See Table 1 on the next page).

Again, the drain current ($I_D$) for different gate voltages ($V_{GS}$) was measured after irradiation and is shown in Appendix B, Table B.3. Then, from Table B.3, the $\sqrt{I_D}$

Table 1. Device Irradiation

| Device Type | Device Condition |
|---|---|
| 1. Intersil VN98AK | $2 \times 10^3$RADS(Si) cobalt 60 radiation |
| 2. Intersil IVN5200TND | $3 \times 10^3$RADS(Si) cobalt 60 radiation |
| 3. Siliconix VN64GA | $3 \times 10^3$RADS(Si) cobalt 60 radiation |

versus $V_{GS}$ was drawn and the threshold voltages for each post-irradiation device was found (Figures 16, 17 and 18).

Appendix B, Table B.4 shows the noise measurement at subthreshold current for each irradiated test device, post-irradiation. The input voltage noise is given in Figures 19, 20 and 21, and flicker noise is shown in Figures 22, 23 and 24 for the irradiated devices.

In order to evaluate the effect of radiation we look at each device separately.

## Intersil VN98AK

From Figures 7 and 16, we can look at Table 2 on the next page.

As one can see from Appendix B, Tables B.2 and B.4 and Figures 10, 13, 19, and 22, the input voltage and flicker noises of radiated device is much larger than before.

Table 2. Measurements for Intersil VN98AK

| $2 \times 10^3$RADS(Si) Cobalt 60 Radiation | | Without Radiation |
|---|---|---|
| Threshold voltage | 1.44V | 1.33V |
| Drain current at threshold | .1MA | 70 μA |

Radiation introduces some traps in the oxide and since MOS transistors are surface devices and the current flows on the surface, the traps will cause some fluctuations in the current and these fluctuations in the current will produce some radiation-induced noises in the device.

Intersil IVN5200TND

From Figures 8 and 17:

Table 3. Measurements for Intersil IVN5200TND

| $3 \times 10^3$RADS(Si) Cobalt 60 Radiation | | Without Radiation |
|---|---|---|
| Theshold voltage | .55V | .86V |
| Drain current at threshold voltage | .4MA | .4MA |

From Figures 11, 14, 20, and 23 we can see the magnitude of input voltage and flicker noises for radiated

device is much larger than before the radiation. The reason for this increase is the creation of the traps in the oxide (i.e. it was explained in previous discussions).

Siliconix VN64GA

From Figures 7 and 18:

Table 4. Measurements for Siliconix VN64GA

| $3 \times 10^3$ RADS(Si) Cobalt 60 Radiation | | Without Radiation |
|---|---|---|
| Threshold voltage | 1.25V | 1.43V |
| Drain current at threshold | .384MA | .2MA |

From Figures 12, 15, 21 and 24 we can see the magnitude of input voltage and flicker noises for radiated device is smaller than before the radiation. A possible reason for this decrease is the existence of some traps in the oxide before the radiation; and by radiating the device, we have caused the traps to be neutralized in the oxide, therefore causing an improvement in the noise of the radiated device. Without extensive post-irradiation testing, it is not possible to pin down the mechanism responsible for the observed decrease in noise magnitude.

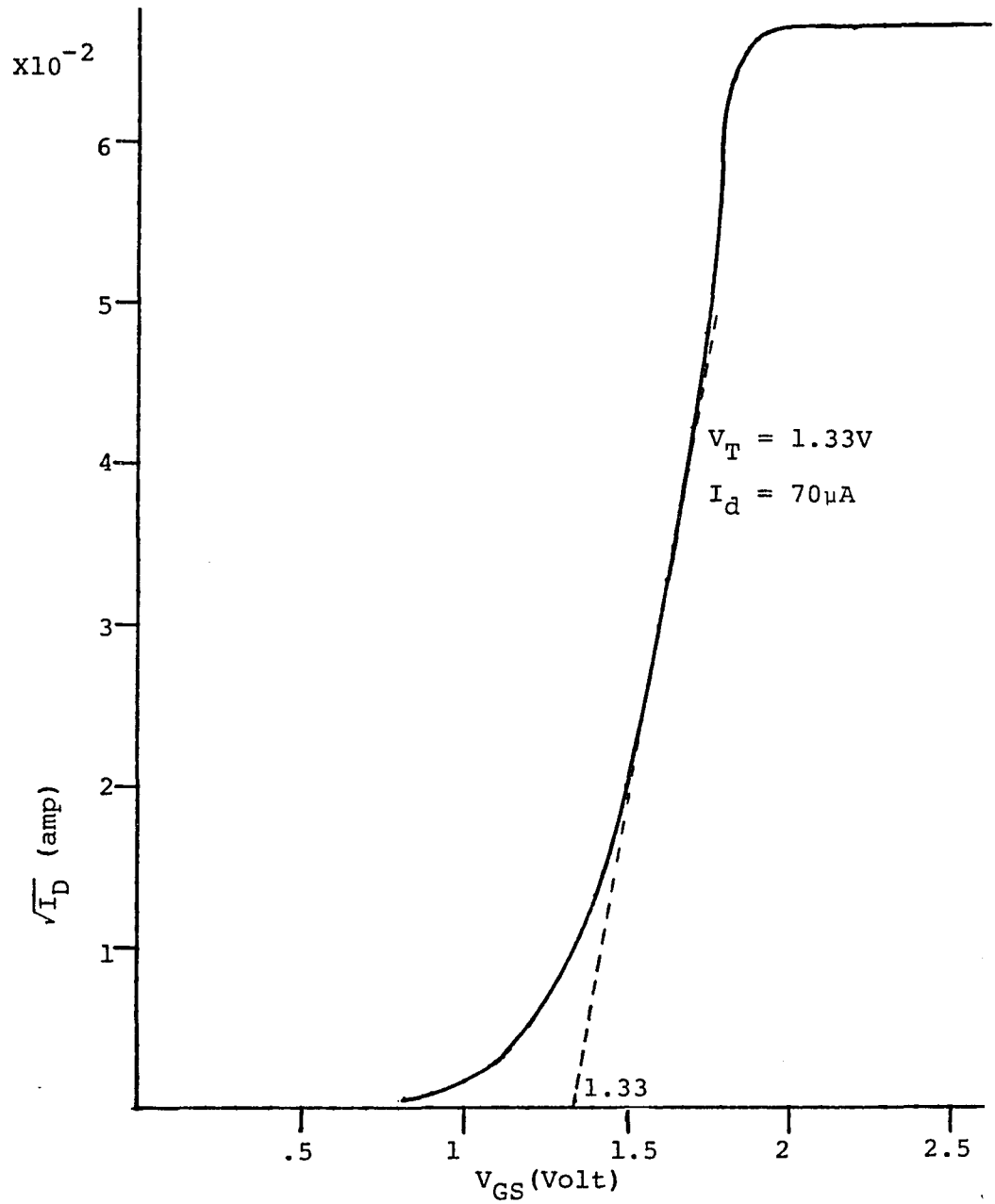



Figure 7. Threshold voltage for VN98AK (unradiated).

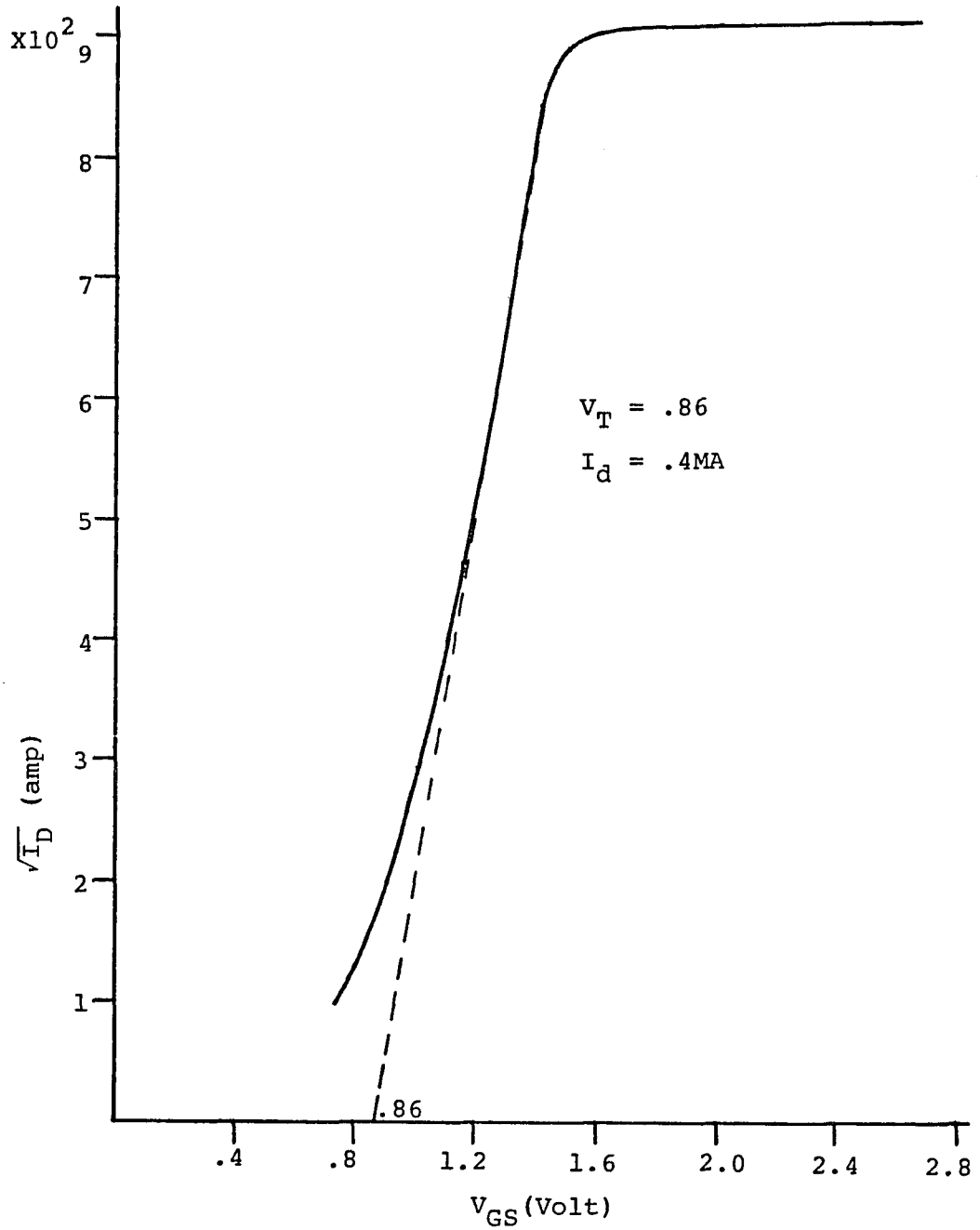



Figure 8. Threshold voltage for IVN5200TND (unradiated).

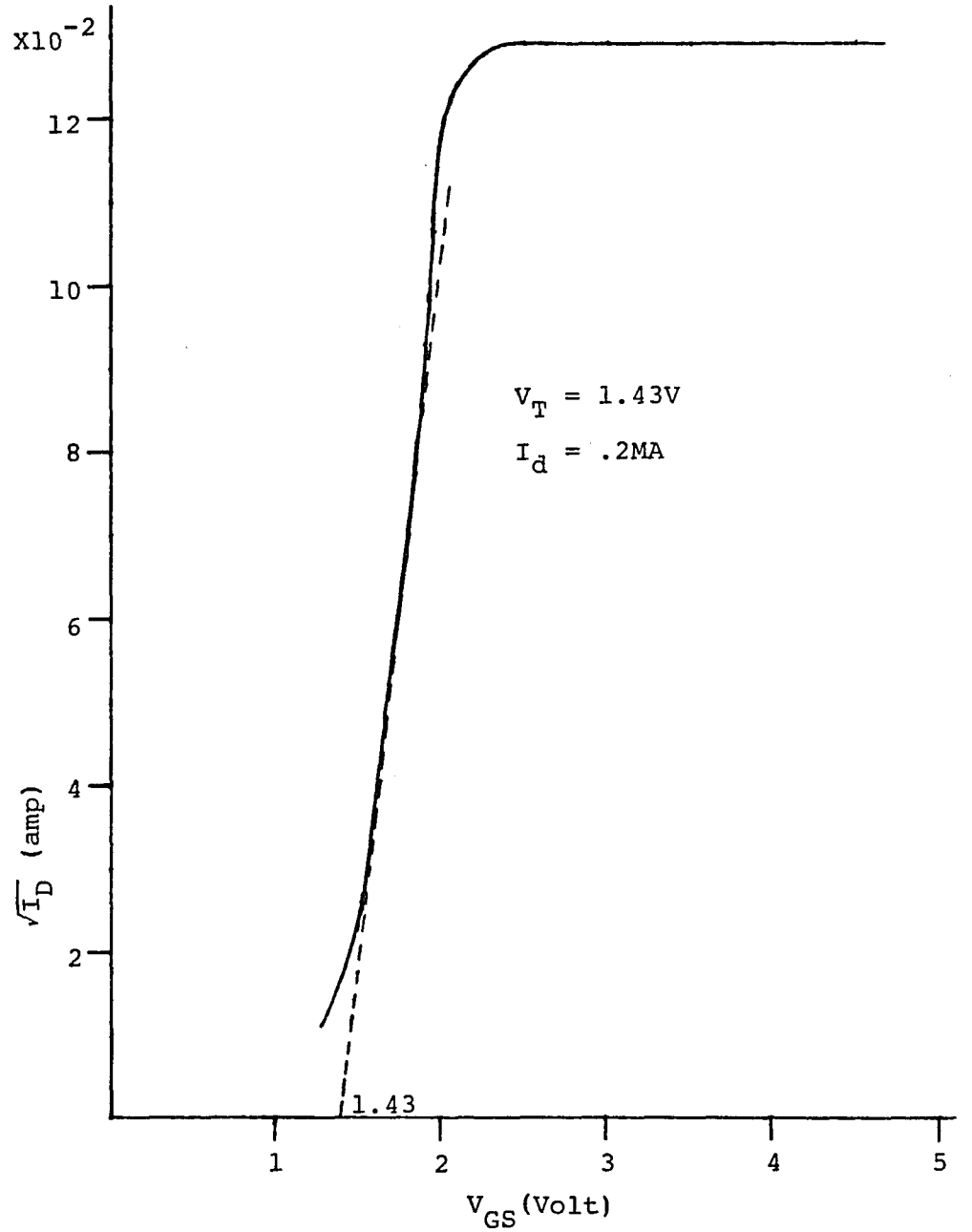



Figure 9. Threshold voltage for VN64GA (unradiated).

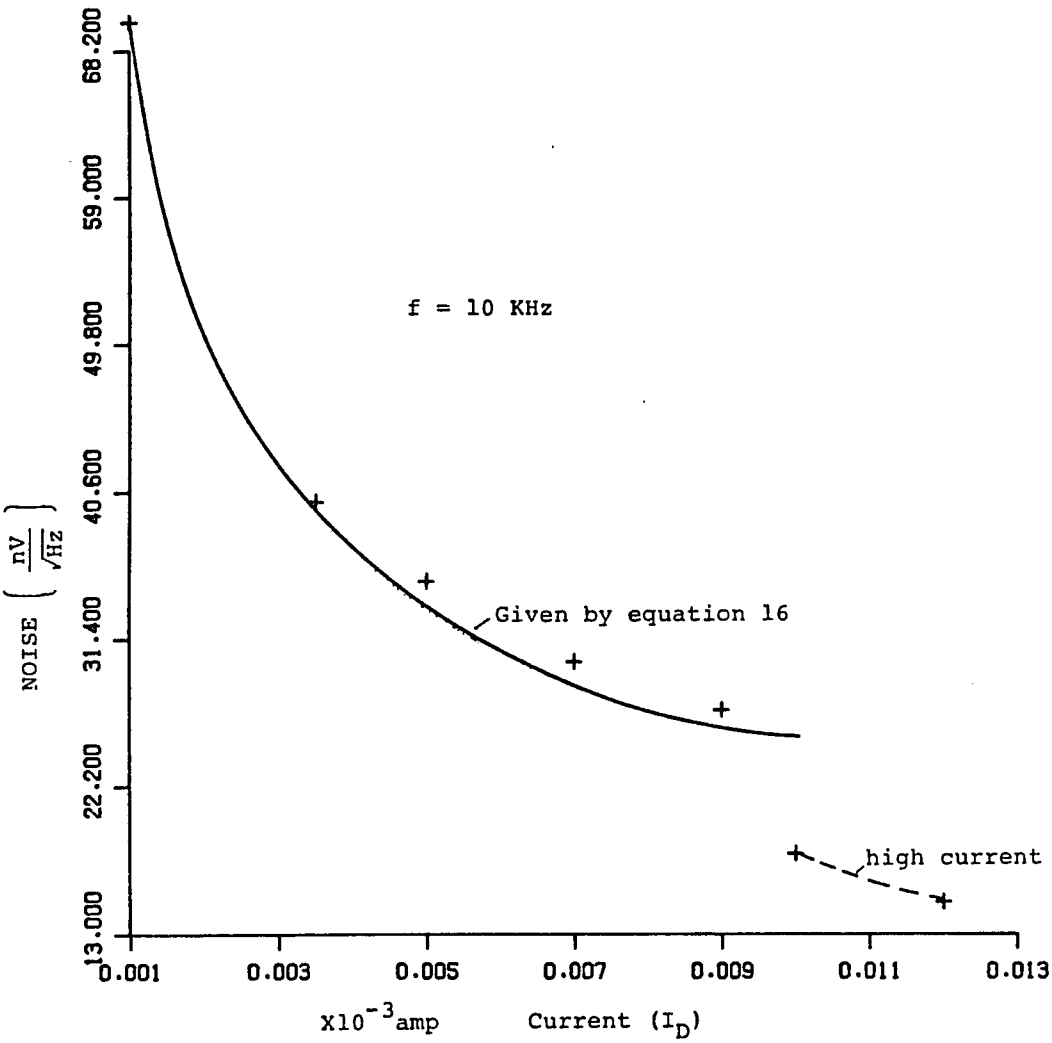



Figure 10. Input voltage noise for VN98AK (unradiated).

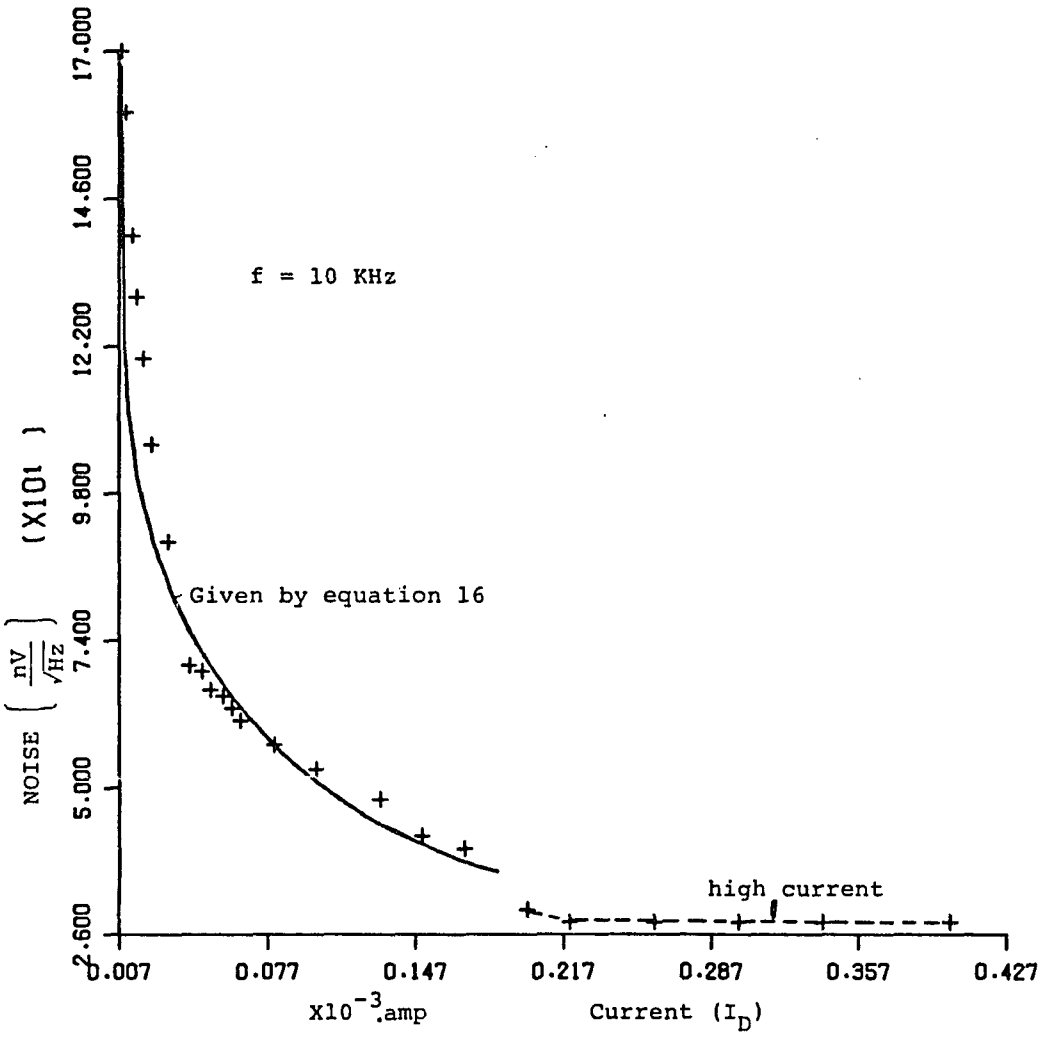



Figure 11. Input voltage noise for VN5200TND (unradiated).

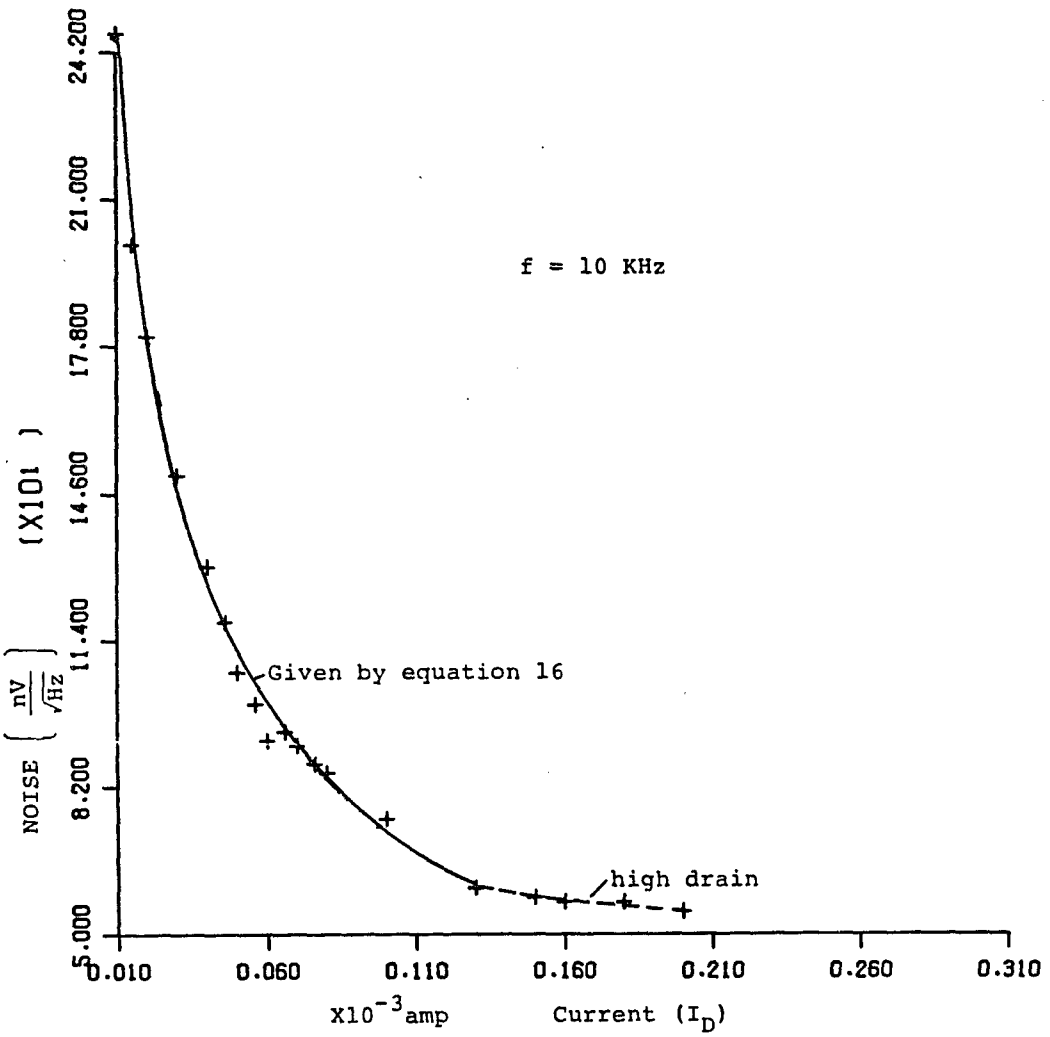



Figure 12. Input voltage noise for VN64GA (unradiated).

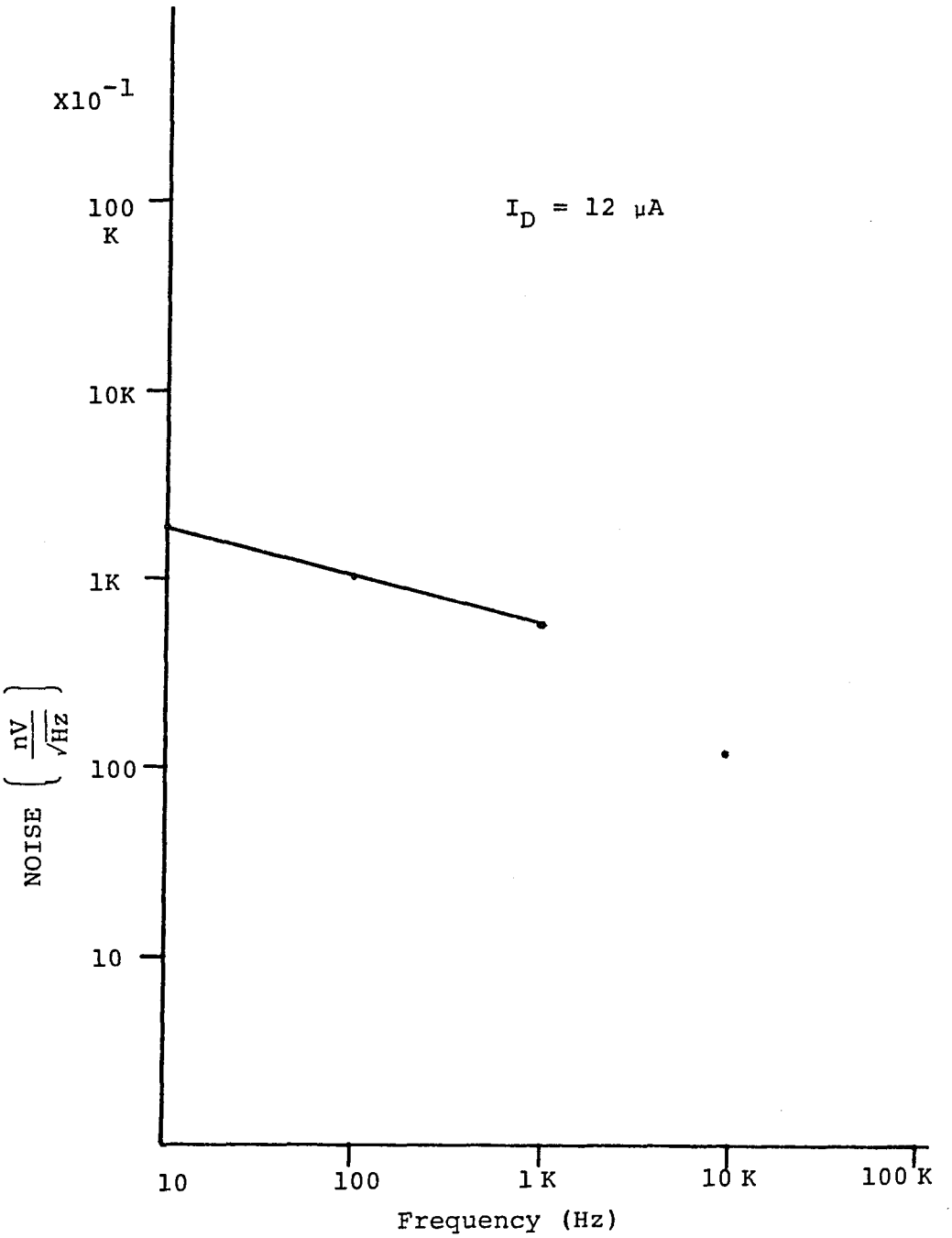



Figure 13. Flicker noise for VN98AK (unradiated).

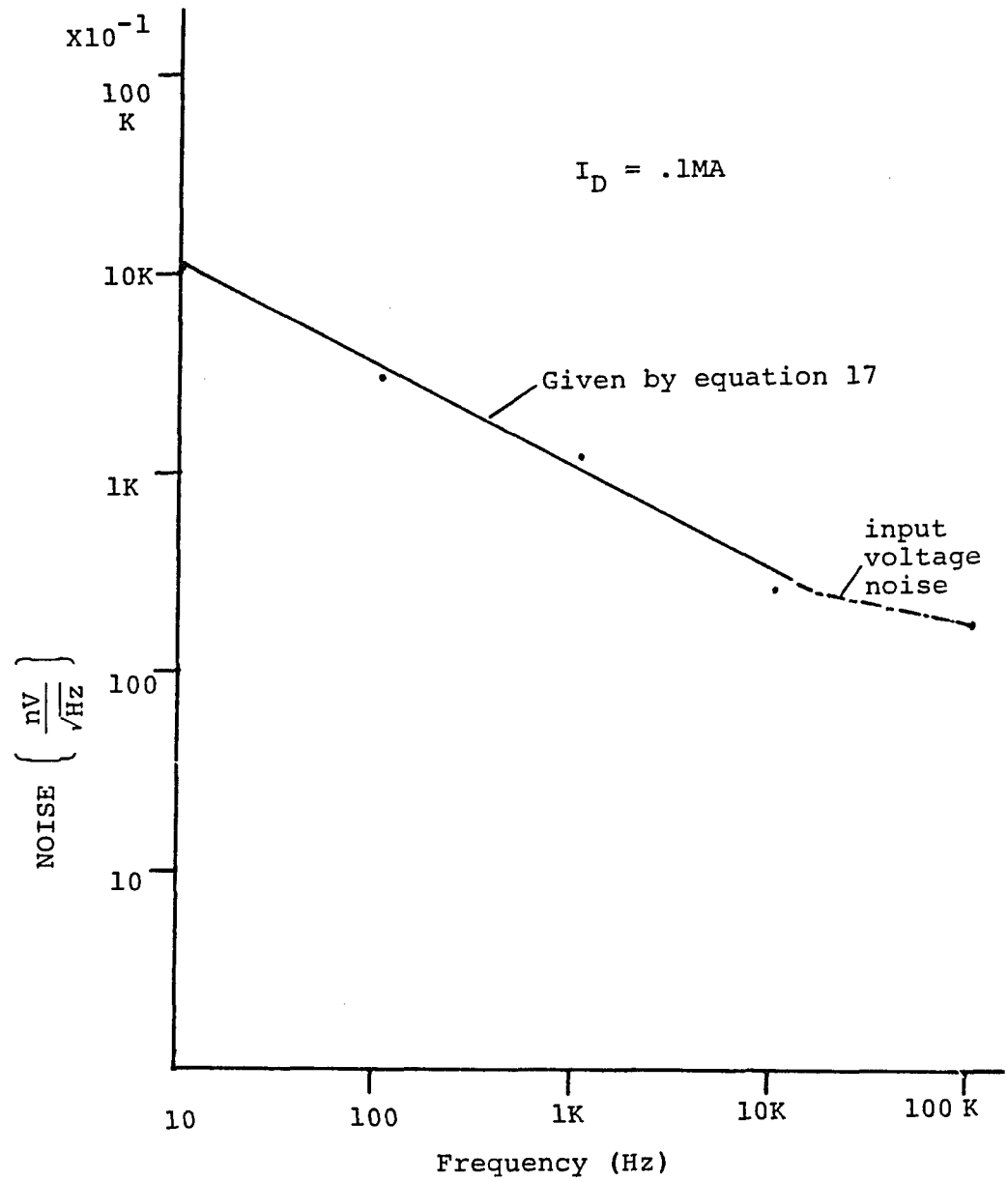



Figure 14. Flicker noise for IVN5200TND (unradiated).

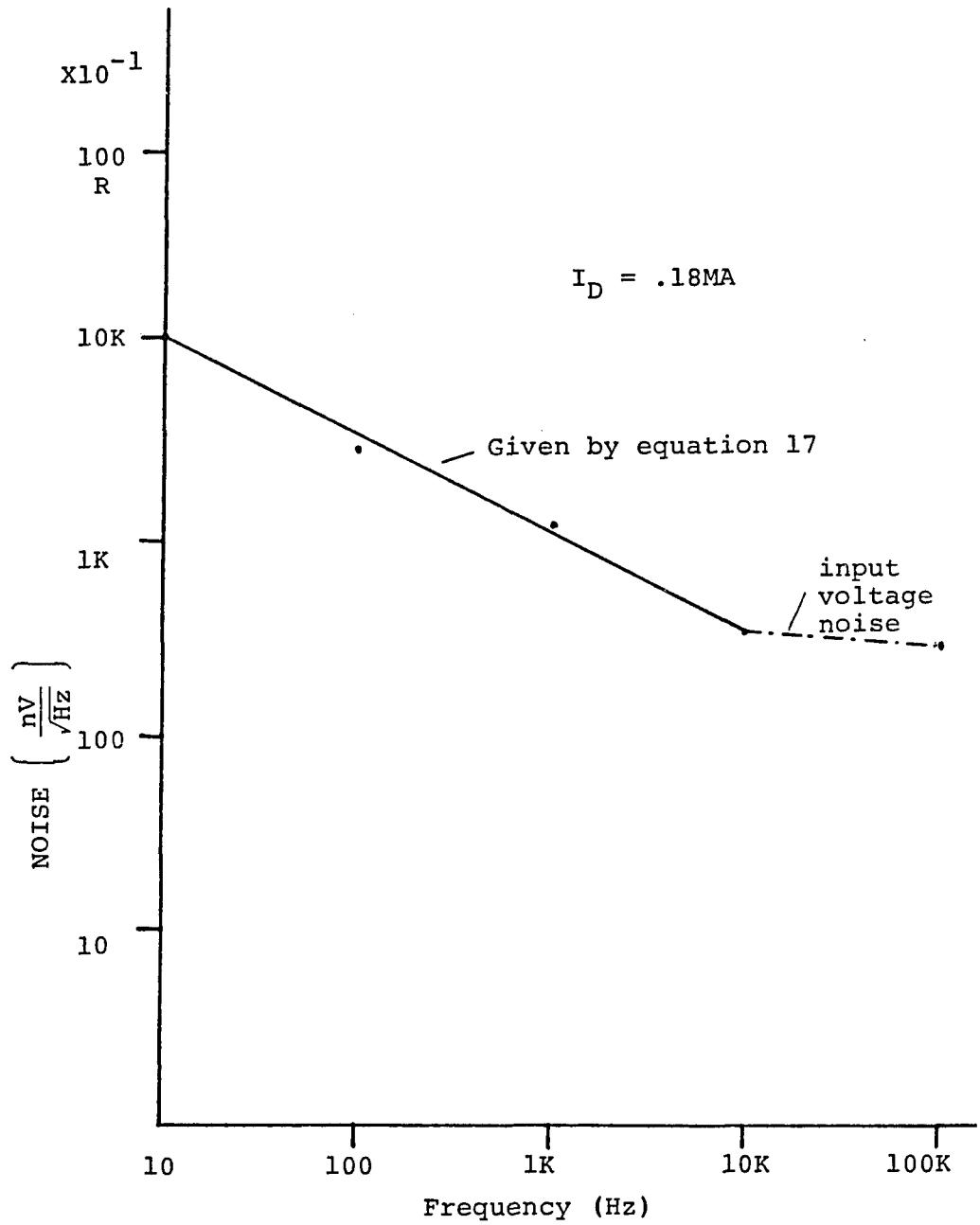



Figure 15. Flicker noise for VN64GA (unradiated).

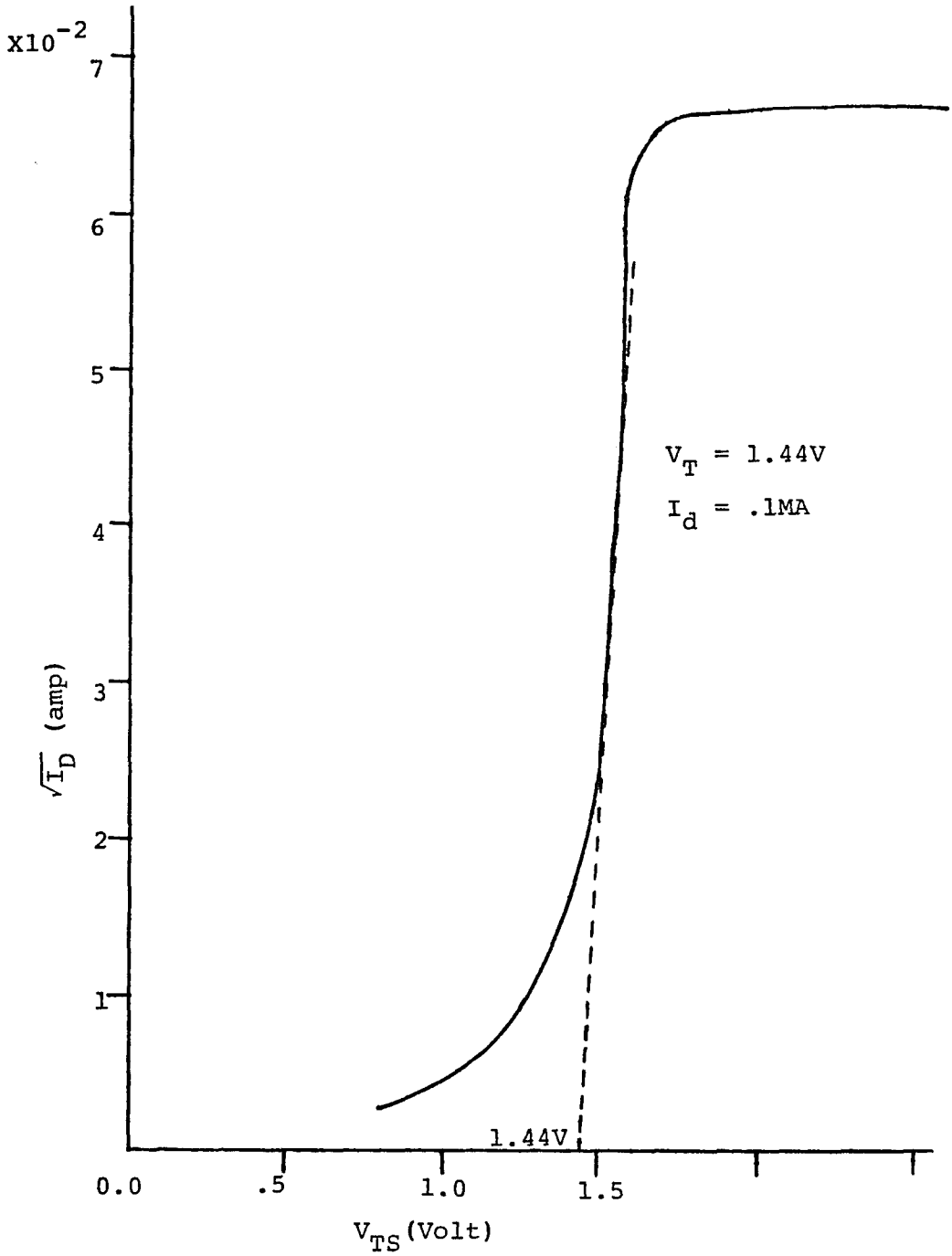



Figure 16. Threshold voltage for VN98AK ($2x10^3$RADS(Si) cobalt 60 radiation).

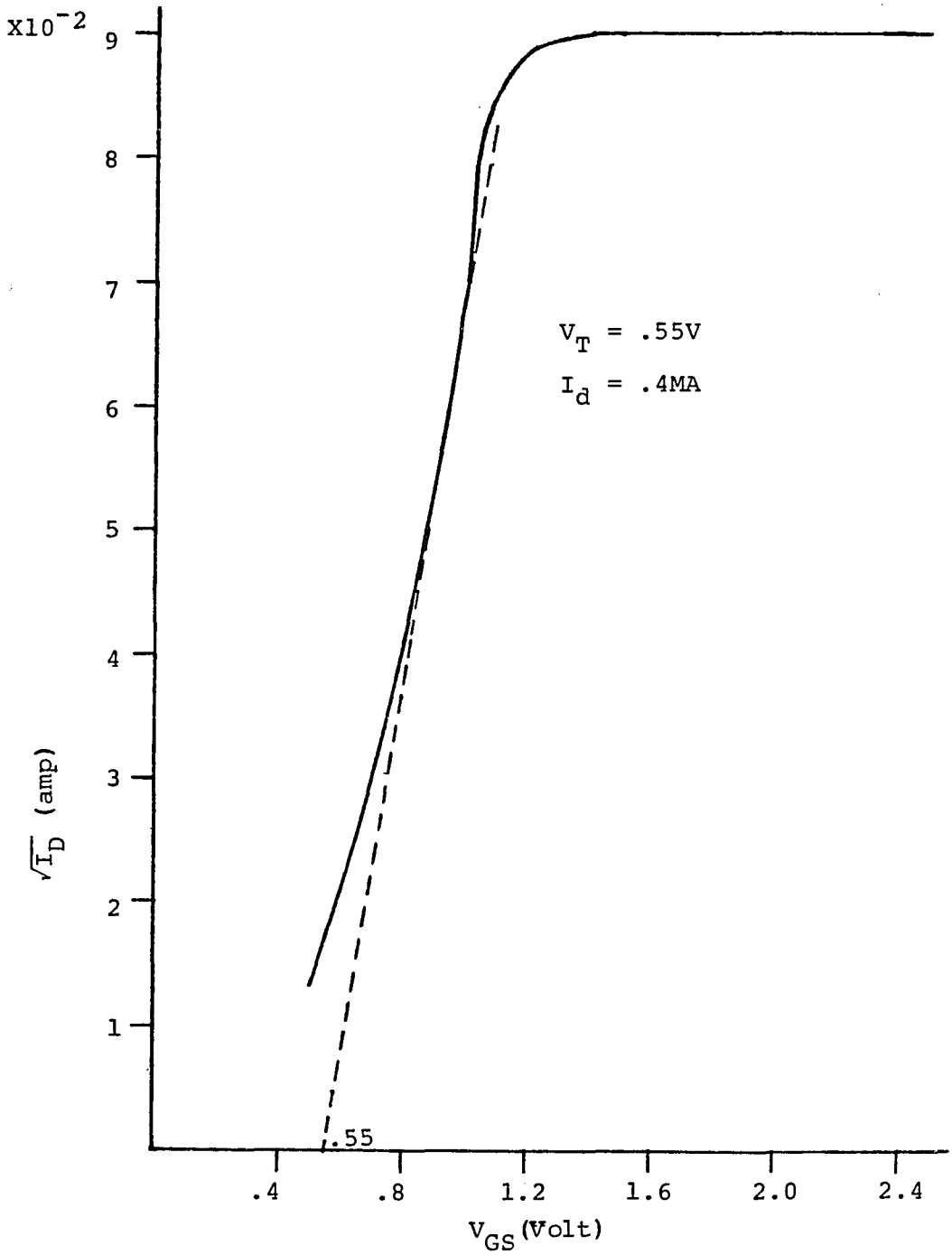



Figure 17. Threshold voltage for IVN5200TND ($3x10^3$RADS(Si) cobalt 60 radiation).

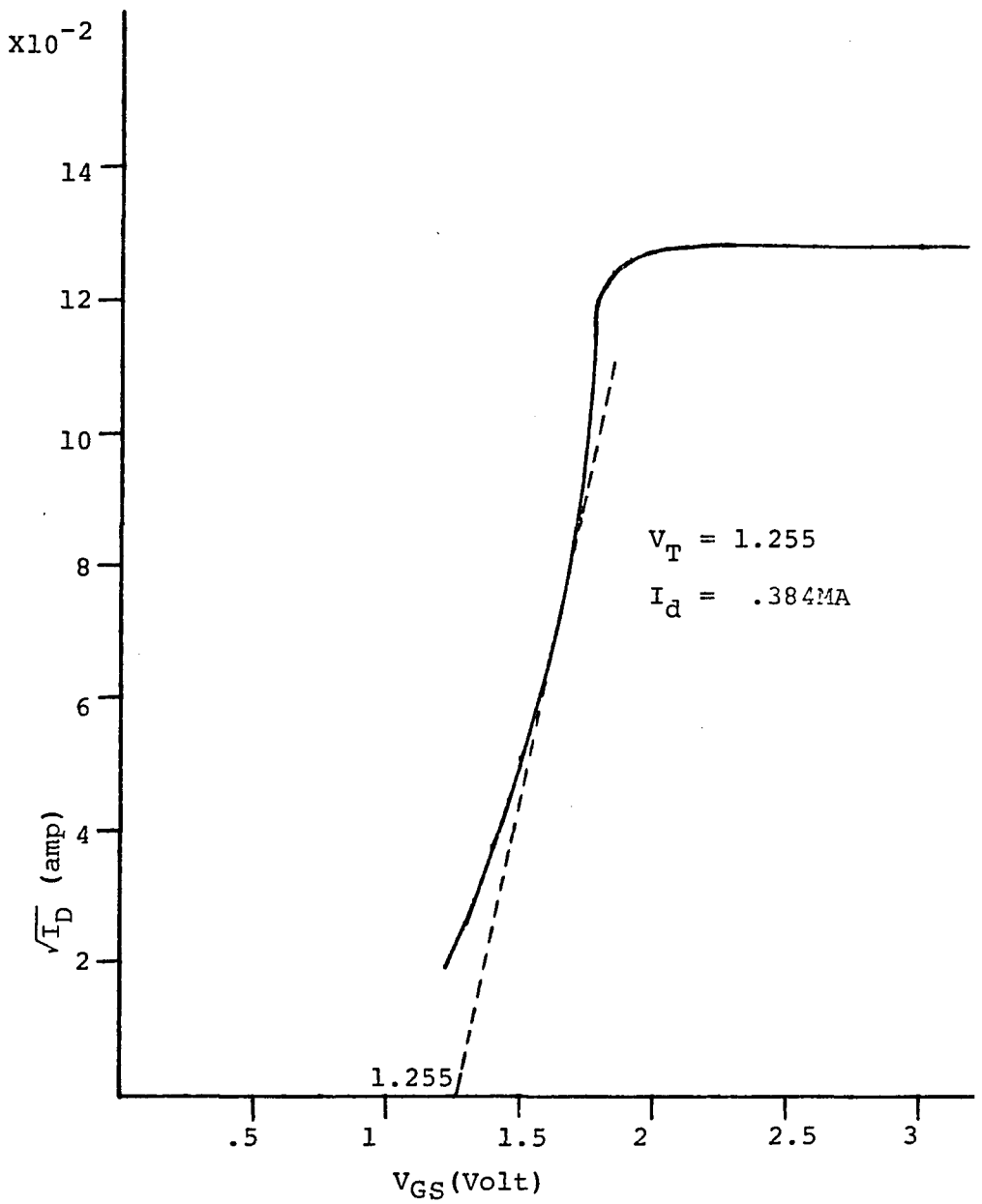



Figure 18. Threshold voltage for VN64GA ($3x10^3$RADS(Si) cobalt 60 radiation).

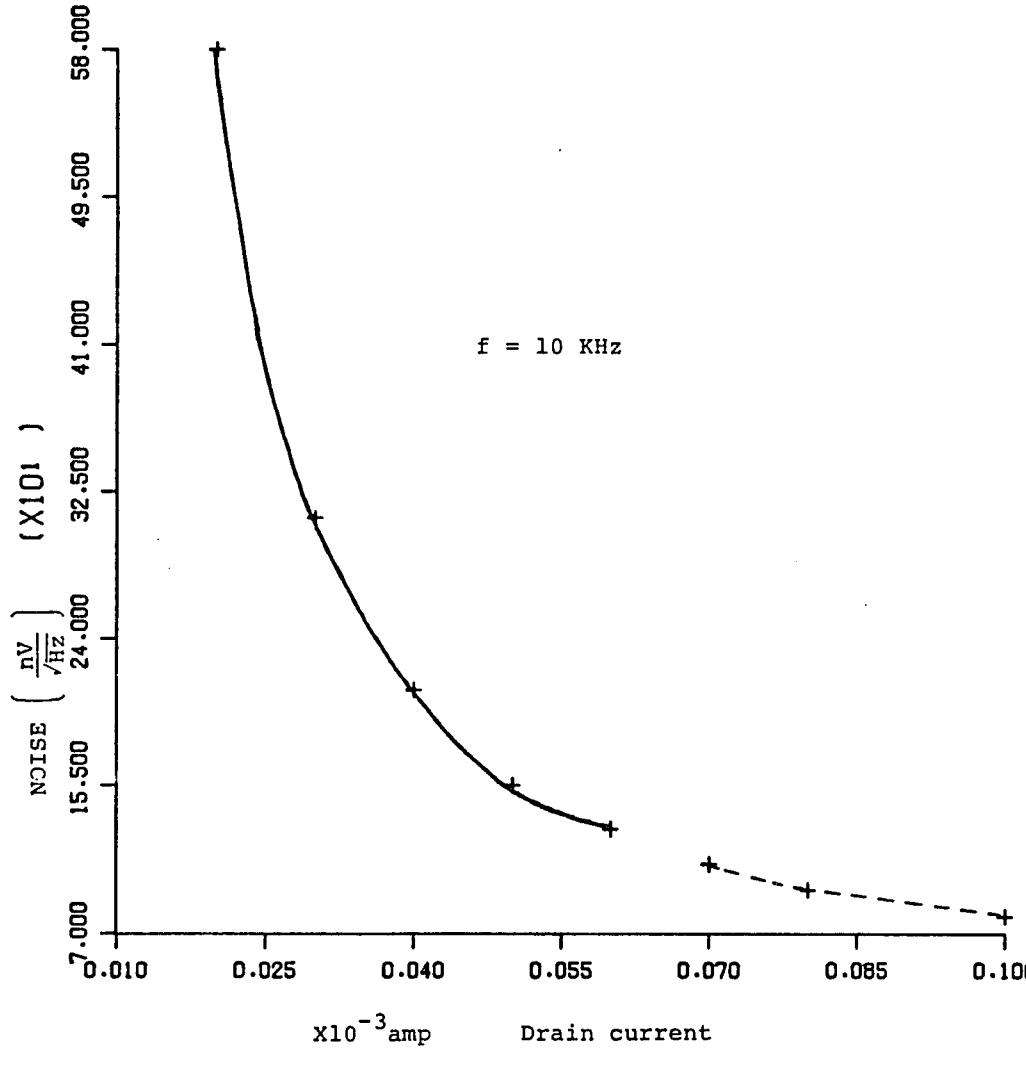



Figure 19. Input voltage noise for VN98AK ($2x10^3$RADS(Si) cobalt 60 radiation).

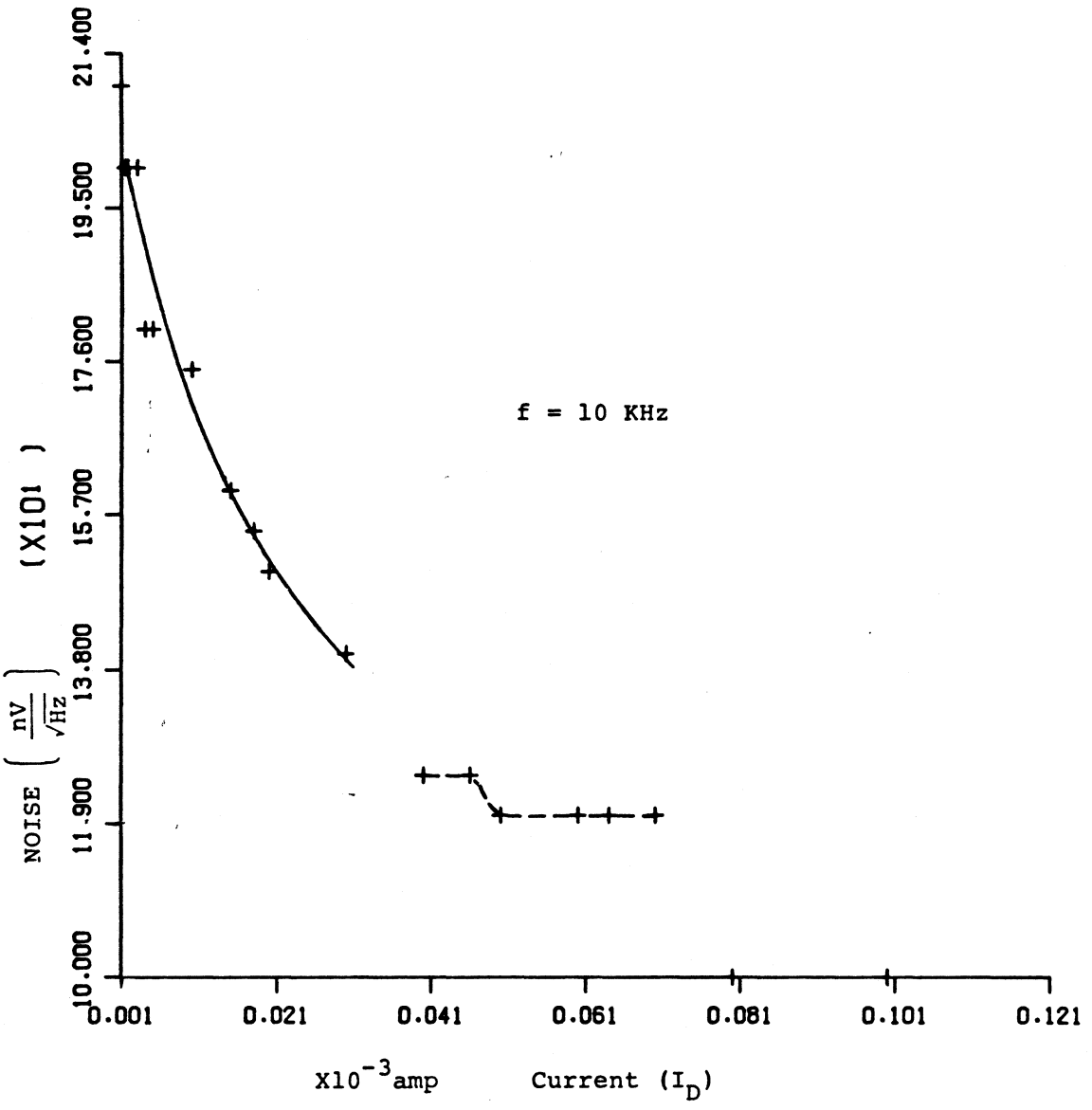



Figure 20. Input voltage noise for IVN5200TND ($3x10^3$ RADS(Si) cobalt 60 radiation).

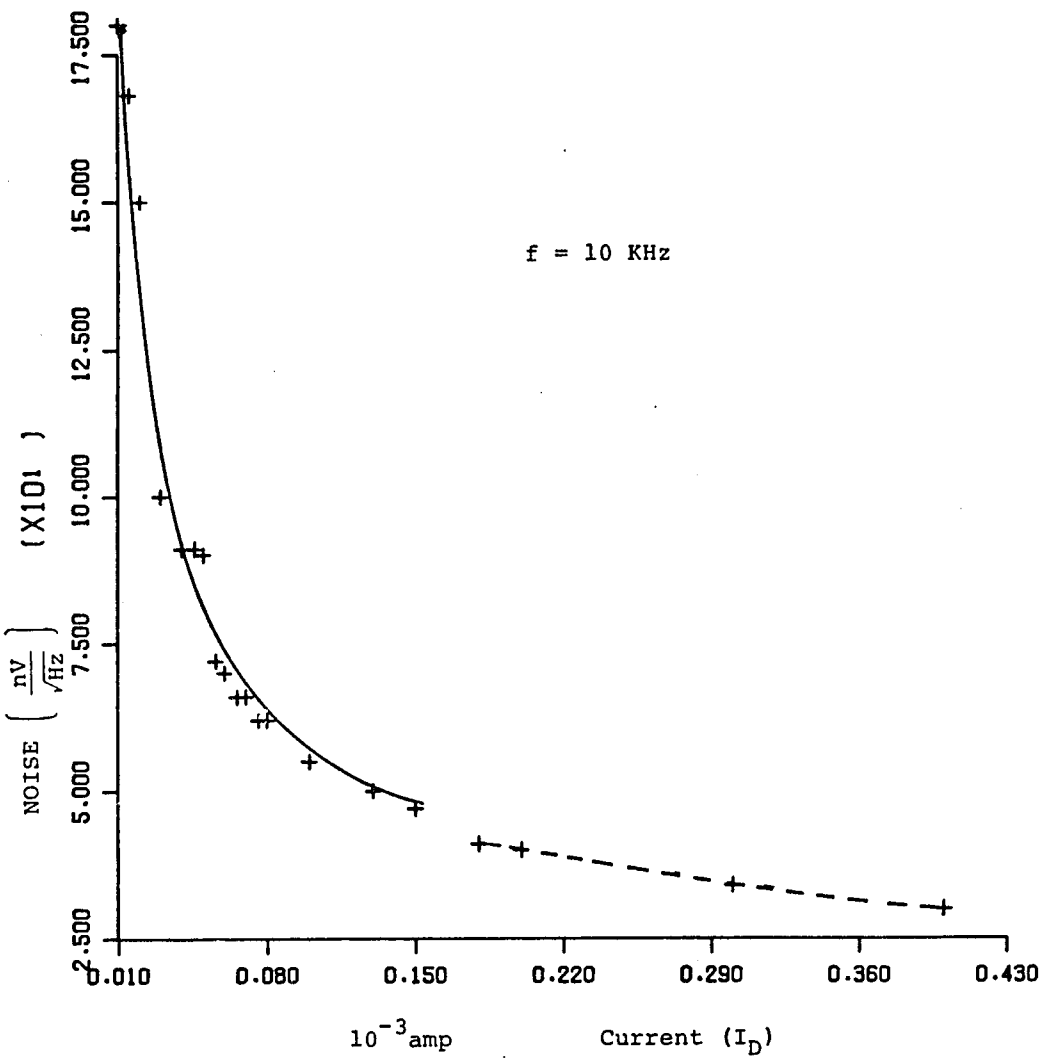



Figure 21. Input voltage noise for VN64GA ($3x10^3$RADS(Si) cobalt 60 radiation).

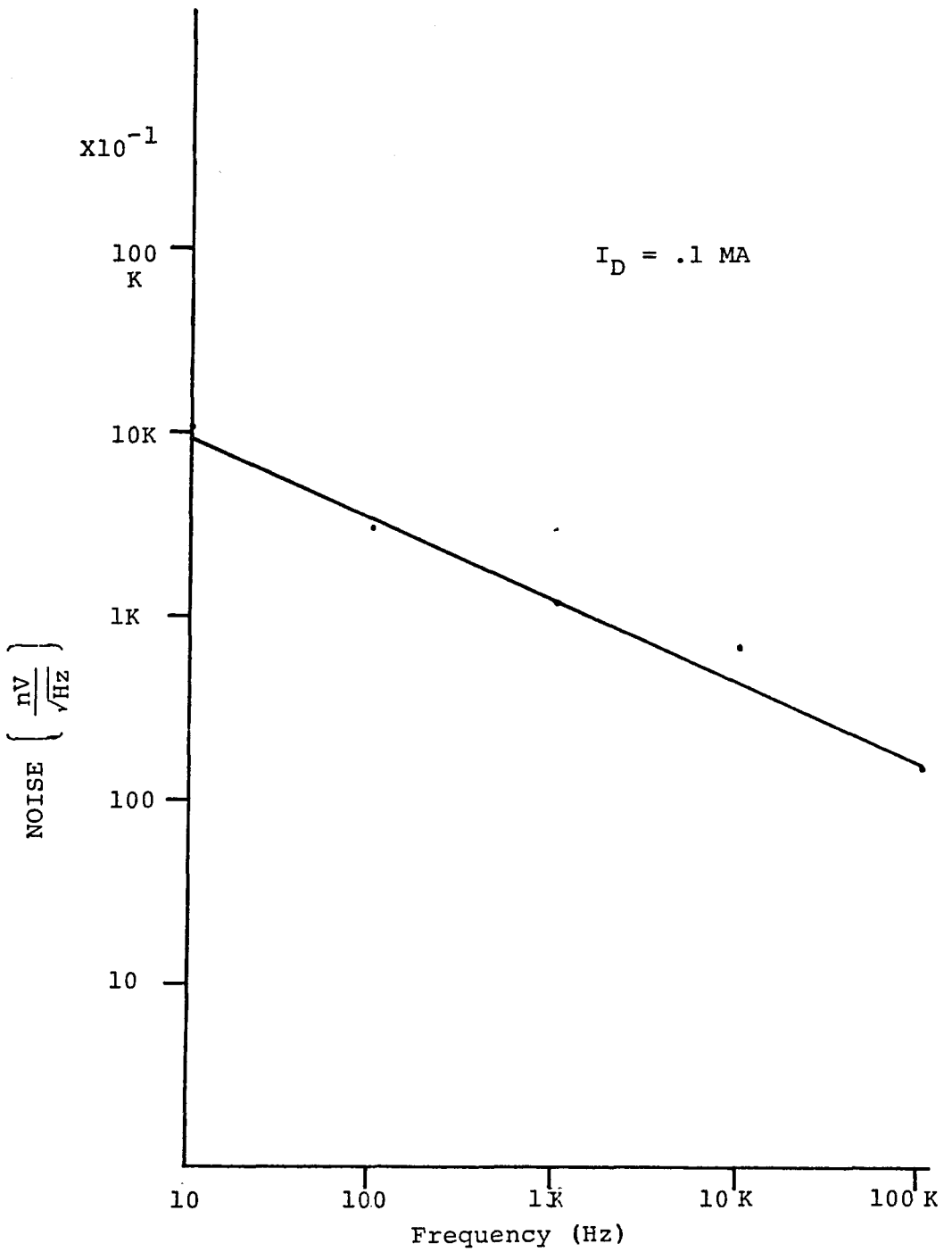



Figure 22. Flicker noise for VN98AK ($2x10^3$RADS(Si) cobalt 60 radiation).

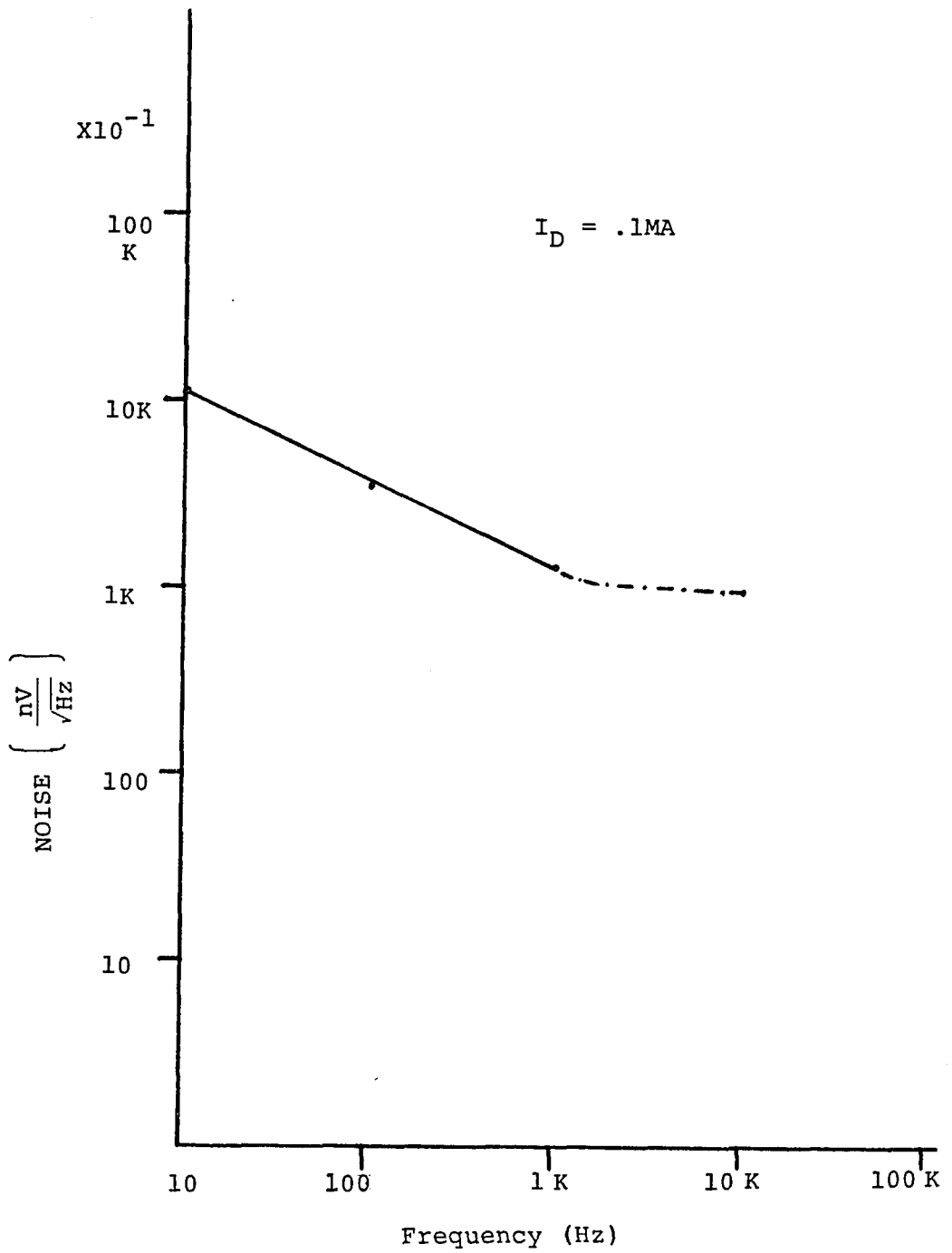



Figure 23. Flicker noise for IVN5200TND ($3x10^3$RADS(Si) cobalt 60 radiation).

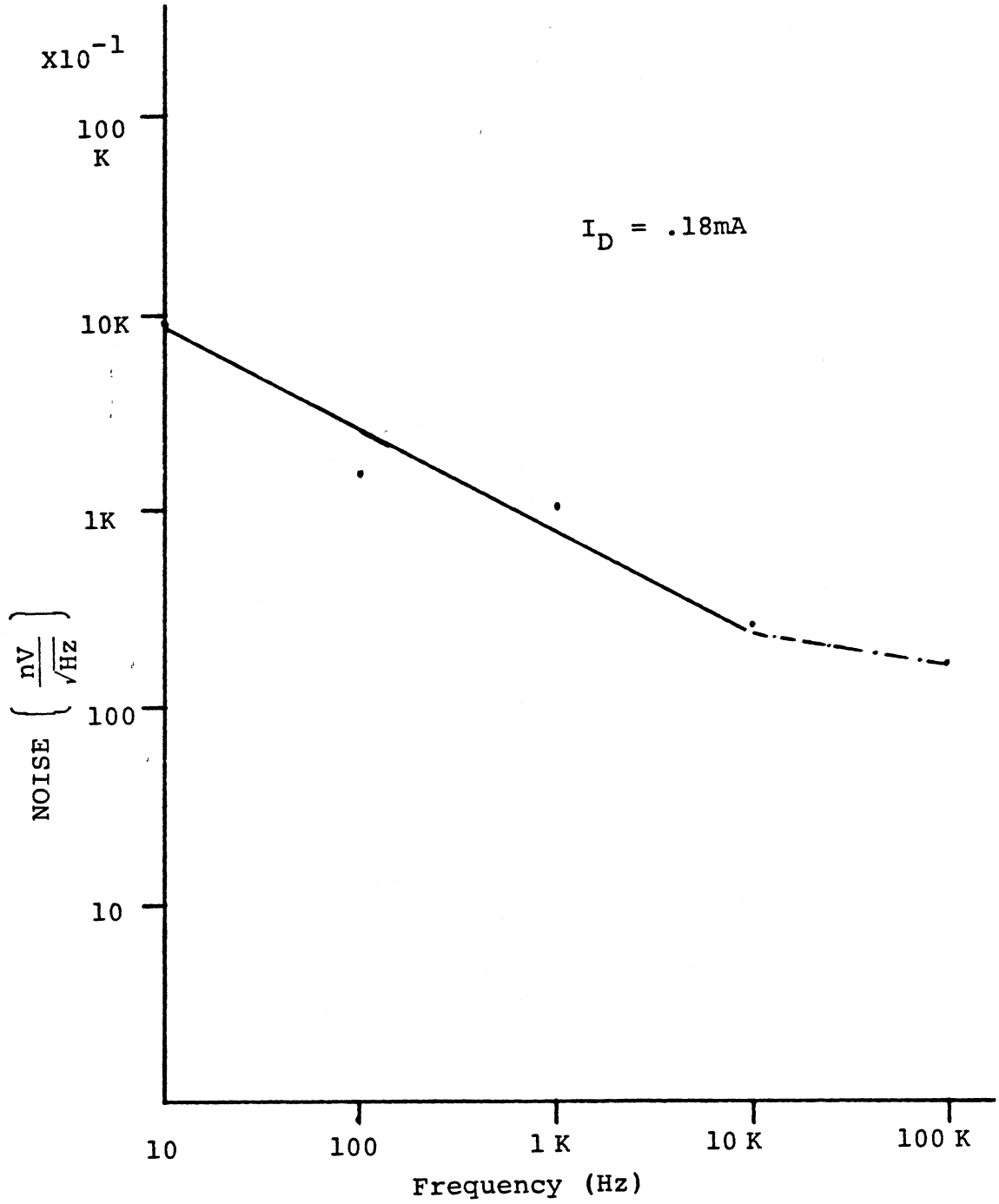



Figure 24. Flicker noise for VN64GA ($3x10^3$RADS(Si) cobalt 60 radiation).

## SECTION 4

## CONCLUSION

The purpose of this research paper was to confirm the available theoretical noise models with experimental observations.

The theoretical evidence was provided by a number of investigators [1 - 35]. Theoretically, we have shown that the input noise voltage is given by:

$$\frac{V_{N\,total}}{\sqrt{\Delta f}} = \gamma \left( \frac{1}{\sqrt{I_D}} \right) \tag{16}$$

where

$$\gamma = \sqrt{2KTV_T(1 + n^2)}$$

and the flicker noise (1/f) is proportional to:

$$\frac{V_{NF}}{\sqrt{\Delta f}} \propto \frac{1}{f} \frac{1}{WL} \quad (WL = \text{gate area}) \tag{17}$$

Since the slope factor (n) and the gate area (WL) were not known for these three devices, the exact values of the noise could not be calculated theoretically. But the slope factor and the gate area are constant for each device; therefore,

the noise could be normalized according to (n) and (WL) at subthreshold for each transistor.

The experimental work was done at Burr-Brown [22] using a noise measurement instrument. Three VMOS devices were considered for confirmation of theoretical results. These devices were tested at a subthreshold current with radiated and unradiated conditions. The experimental results of the flicker noise and the input noise voltage are given in Figures 10, 11, 12, 13, 14, 15, 19, 20, 21, 22, 23 and 24. These figures support the theoretical noise model (equation 16 and 17) of the MOS transistor. Figures 10, 11 and 12 show that the input noise voltage is proportional to $\frac{1}{\sqrt{I_D}}$ and Figures 13, 14 and 15 show that the flicker noise is proportional to 1/f.

The main source of error in the experimental data was due to instrumental reading and round off errors. Also, we have some errors due to the assumptions that were made in the simple model which was presented for the theoretical calculations of the drain current (page 6). There are discrepancies between the theoretical calculations and the experimental results due to our original assumption that the device channel was sufficiently long so that the channel-length modulation effects are negligible when, in fact, VMOS has a shorter channel than a "normal" MOSFETS.

# APPENDIX A

## VERTICAL MOS ( VMOS ) DEVICES

### Introduction

Until several years ago, field effect transistors have been useful only at low (<1W) power levels. Some practical limitations in measuring high power devices precluded FETS competing with bipolar transistors in power applications. A major limitation was that FET's were strictly horizontal devices, so their current densities were much less than the bipolar's (which utilized vertical current flow). For a given current, then, the FET chip area had to be quite large, which meant higher cost.

The VMOS (or vertical MOS technology) exploits a diffused channel and vertical current flow to achieve its high power capabilities and for the same voltages it produces more currents than a "normal" MOSFETS.

### VMOS Technology

Appendix A, Figure A.1 shows a cross section of VMOS channel. The substrate, which eventually becomes the drain and provides a low resistance current path, is $N^+$ material. An $N^-$ epi layer absorbs the depletion region from drain-body junction, which is reversed biased and that increases

the drain-source breakdown voltage. Since the gate overlaps $N^-$ rather than $N^+$, the feedback capacitances are greatly reduced. A p material body and $N^+$ source are then diffused into epi, followed by etching of a v groove through the source body and into the epi. The gate produces an electric field which induces an N-type channel on both surfaces of the body facing the gate, allowing electrons to flow from the source, through the N-type channel, and the epi, and into the substrate (drain). It should be noted that VMOS inherents a shorter channel than a "normal" MOSFETS, for comparable layout rules; but, VMOS fundamentally operates the same as an MOS device.

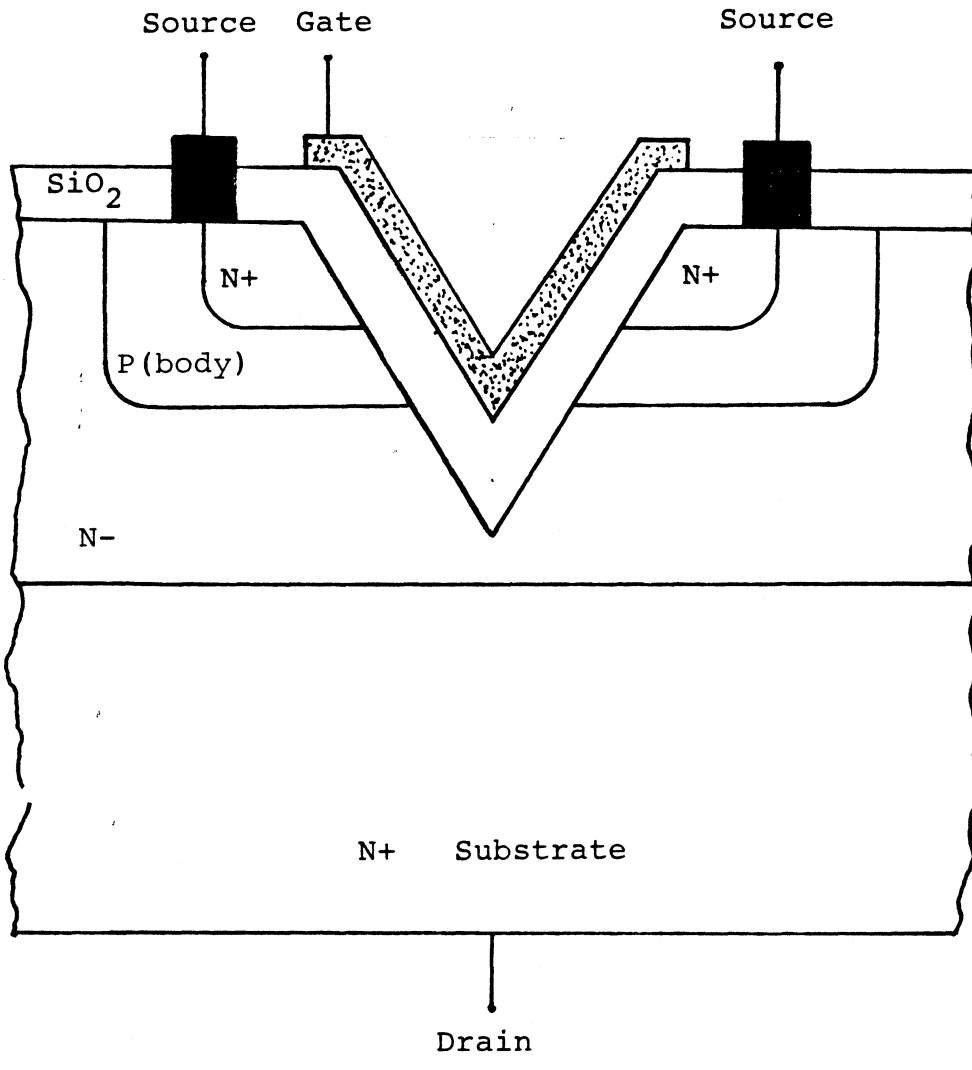



Figure A.1. The cross section of a VMOS channel.

# APPENDIX B

# EXPERIMENTAL DATA

Table B.1. Non-Radiated Devices

| VN98AK $R_D$=1.093KΩ | | IVN5200TND $R_D$=.598KΩ | | VN64GA $R_D$=.2997KΩ | |
|---|---|---|---|---|---|
| $V_{GS}$(VOLT) | $I_D$(AMP) | $V_{GS}$(VOLT) | $I_D$(AMP) | $V_{GS}$(VOLT) | $I_D$(AMP) |
| 3.504 | 4.5732MA | 2.5 | 8.404MA | 4.5 | 16.793MA |
| 3.2513 | 4.57138MA | 2.0 | 8.38MA | 4.0 | 16.766MA |
| 3.00 | 4.5686MA | 1.8 | 8.33MA | 3.5 | 16.786MA |
| 2.907 | 4.5667MA | 1.6 | 8.247MA | 3.0 | 16.756MA |
| 2.8 | 4.5658MA | 1.5 | 8.05MA | 2.5 | 16.756MA |
| 2.6 | 4.56129MA | 1.4 | 7.10MA | 2.0 | 15.348MA |
| 2.505 | 4.5576MA | 1.35 | 5.9MA | 1.96 | 11.344MA |
| 2.404 | 4.54937MA | 1.3 | 4.728MA | 1.950 | 10.744MA |
| 2.304 | 4.54432MA | 1.2 | 3.04MA | 1.938 | 9.67MA |
| 2.202 | 4.53653MA | 1.15 | 2.172MA | 1.92 | 8.808MA |
| 2.1049 | 4.525534MA | 1.1 | 1.62MA | 1.90 | 7.8MA |
| 2.00 | 4.50444MA | 1.0 | .88A | 1.80 | 6.0MA |
| 1.904 | 4.4448MA | .9 | .481MA | 1.70 | 5.17MA |
| 1.803 | 3.1378MA | .8 | .1721MA | 1.60 | .900MA |
| 1.75 | 2.359MA | | | 1.50 | .5MA |
| 1.706 | 1.8MA | | | | |
| 1.654 | 1.2725MA | | | | |
| 1.605 | .904007MA | | | | |
| 1.506 | .4153MA | | | | |
| 1.408 | .17786MA | | | | |
| 1.305 | $7.004 \times 10^{-2}$MA | | | | |
| 1.206 | $2.649 \times 10^{-2}$MA | | | | |
| 1.102 | $9.53 \times 10^{-2}$ MA | | | | |
| 1.002 | $3.525 \times 10^{-3}$MA | | | | |
| .9 | $1.2835 \times 10^{-3}$MA | | | | |
| .8 | $4.564 \times 10^{-4}$MA | | | | |

Table B.2. Noise Measurement for Unradiated Device At Different Frequencies

| $I_D$(AMP) | 10Hz | 100Hz | 1K Hz | 10 KHz | 100 KHz |
|---|---|---|---|---|---|
| | | | VN98AK | | |
| 12μA | 360 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 120 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 80 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 15 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | Instrumentation Error |
| 10μA | 360 " | 120 " | 86 " | 18 " | " |
| 9μA | 380 " | 130 " | 92 " | 27 " | " |
| 7μA | 380 " | 130 " | 100 " | 30 " | " |
| 5μA | 380 " | 130 " | 110 " | 35 " | " |
| 3.5μA | 380 " | 130 " | 120 " | 40 " | " |
| 1μA | 380 " | 160 " | 160 " | 70 " | " |
| | | | IVN5200TND | | |
| .4MA | 1140 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 440 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 85 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 28 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 22 $\left(\frac{nV}{\sqrt{Hz}}\right)$ |
| .34MA | 1140 " | 440 " | 100 " | 28 " | 24 " |
| .3MA | 1140 " | 440 " | 120 " | 28 " | 24 " |
| .26MA | 1140 " | 440 " | 135 " | 28 " | 25 " |
| .22MA | 1140 " | 460 " | 165 " | 28 " | 29 " |
| .2MA | 1140 " | 480 " | 185 " | 30 " | 30 " |
| .17MA | 1230 " | 500 " | 200 " | 40 " | 30 " |
| .15MA | 1260 " | 500 " | 210 " | 42 " | 31 " |
| .13MA | 1320 " | 500 " | 210 " | 48 " | 32 " |
| .1MA | 1380 " | 550 " | 215 " | 53 " | 34 " |
| .08MA | 1380 " | 565 " | 220 " | 57 " | 36 " |
| 64μA | 1500 " | 610 " | 250 " | 61 " | 40 " |
| 60μA | 1530 " | 610 " | 250 " | 63 " | 40 " |
| 56μA | 1500 " | 610 " | 250 " | 65 " | 40 " |
| 50μA | 1530 " | 610 " | 250 " | 66 " | 40 " |
| 46μA | 1530 " | 610 " | 255 " | 69 " | 42 " |
| 40μA | 1530 " | 620 " | 255 " | 70 " | 43 " |
| 30μA | 1590 " | 620 " | 265 " | 90 " | 46 " |

Table B.2, Continued

| $I_D$(AMP) | 10Hz | 100Hz | 1K Hz | 10 KHz | 100 KHz |
|---|---|---|---|---|---|
| | | | IVN5200TND | | |
| 22μA | 1600 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 610 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 270 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 106 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 51 $\left(\frac{nV}{\sqrt{Hz}}\right)$ |
| 18μA | 1600 " | 700 " | 420 " | 120 " | Instrumentation Error |
| 15μA | 1900 " | 700 " | 430 " | 130 " | " |
| 13μA | 1900 " | 750 " | 450 " | 140 " | " |
| 10μA | 1900 " | 750 " | 510 " | 160 " | " |
| 8μA | 1950 " | 750 " | 580 " | 170 " | " |
| | | | VN64GA | | |
| .2MA | 1320 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 420 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 155 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 55 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 51 $\left(\frac{nV}{\sqrt{Hz}}\right)$ |
| .18MA | 1440 " | 480 " | 175 " | 57 " | 56 " |
| .16MA | 1620 " | 540 " | 180 " | 57 " | Instrumentation Error |
| .15MA | 1740 " | 580 " | 200 " | 58 " | " |
| .13MA | 1800 " | 600 " | 220 " | 60 " | " |
| .1 MA | 2200 " | 700 " | 250 " | 75 " | " |
| 80μA | 2500 " | 850 " | 290 " | 85 " | " |
| 76μA | 2500 " | 850 " | 295 " | 87 " | " |
| 70μA | 2500 " | 850 " | 300 " | 88 " | " |
| 66μA | 2600 " | 850 " | 305 " | 90 " | " |
| 60μA | 2800 " | 850 " | 310 " | 92 " | " |
| 56μA | 2800 " | 900 " | 310 " | 100 " | " |
| 50μA | 2800 " | 900 " | 315 " | 107 " | " |
| 46μA | 2850 " | 950 " | 320 " | 118 " | " |
| 40μA | 2900 " | 950 " | 325 " | 130 " | " |
| 30μA | 2950 " | 950 " | 360 " | 150 " | " |
| 20μA | 3000 " | 1740 " | 800 " | 180 " | " |
| 15μA | 3000 " | 1530 " | 900 " | 200 " | " |
| 10μA | 3000 " | 1530 " | 1200 " | 250 " | " |

Table B.3. Radiated Devices

| VN98AK RAD=$2x10^3$Cobalt $R_D$=1.093KΩ | | IVN5200TND RAD=$3x10^3$ Cobalt $R_D$=.598KΩ | | VN64GA RAD=$3x10^3$ Cobalt $R_D$=.2992KΩ | |
|---|---|---|---|---|---|
| $V_{GS}$(VOLT) | $I_D$(AMP) | $V_{GS}$(VOLT) | $I_D$(AMP) | $V_{GS}$(VOLT) | $I_D$(AMP) |
| 3.5 | 4.501MA | 2.5 | 8.24MA | 4.5 | 16.477MA |
| 3.253 | 4.5114MA | 2.01 | 8.23MA | 4.00 | 16.473 |
| 3.00 | 4.3815MA | 1.8 | 8.22MA | 3.5 | 16.4705 |
| 2.908 | 4.395MA | 1.6 | 8.207MA | 3.0 | 16.463 |
| 2.605 | 4.4135MA | 1.5 | 8.17MA | 2.5 | 16.44 |
| 2.502 | 4.4135MA | 1.4 | 8.16MA | 2.0 | 16.366 |
| 2.40 | 4.409MA | 1.35 | 8.127MA | 1.9 | 16.28 |
| 2.2 | 4.428MA | 1.3 | 8.093MA | 1.8 | 15.5 |
| 1.903 | 4.40MA | 1.2 | 7.959MA | 1.7 | 7.606 |
| 1.802 | 4.3769MA | 1.15 | 7.759MA | 1.6 | 5.046 |
| 1.7 | 4.3495MA | 1.1 | 7.19MA | 1.5 | 2.64 |
| 1.6 | 3.96MA | 1.0 | 4.916MA | 1.4 | 1.437 |
| 1.544 | 2.0677MA | .9 | 3.043MA | 1.30 | .7018 |
| 1.5 | .5818MA | .8 | 1.722MA | 1.20 | .384 |
| 1.4 | .267MA | .7 | .89967MA | | |
| 1.3 | .11894MA | .61 | .4682MA | | |
| 1.2 | .0567MA | .5 | .1839MA | | |
| 1.1 | .03019MA | | | | |
| 1.0 | .0192MA | | | | |
| .901 | .0128MA | | | | |
| .803 | .0100MA | | | | |

Table B.4. Noise Measurement for Radiated Device At Different Frequencies

| $I_D$(AMP) | 10HZ | 100HZ | 1K Hz | 10 KHz | 100 KHz |
|---|---|---|---|---|---|
| | | VN98AK ($2x10^3$ Cobalt Radiation)* | | | |
| .1MA | 1440 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 540 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 200 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 80 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 31 $\left(\frac{nV}{\sqrt{Hz}}\right)$ |
| 80μA | 1560 " | 620 " | 230 " | 95 " | 41 " |
| 70μA | 2100 " | 750 " | 285 " | 110 " | 48 " |
| 60μA | 2600 " | 800 " | 300 " | 130 " | 54 " |
| 50μA | 3000 " | 1200 " | 410 " | 155 " | 70 " |
| 40μA | 4100 " | 1500 " | 540 " | 210 " | 100 " |
| 30μA | 5400 " | 2100 " | 800 " | 310 " | 130 " |
| 20μA | 11100 " | 4100 " | 1600 " | 580 " | 280 " |
| *. Noise was so large that it was out of scale to read. | | | | | |
| | | IVN5200TND ($3x10^3$ Cobalt Radiation) | | | |
| .1MA | 1600 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 600 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 220 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 100 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 42 $\left(\frac{nV}{\sqrt{Hz}}\right)$ |
| .08MA | 1600 " | 600 " | 220 " | 100 " | 42 " |
| 70μA | 1700 " | 650 " | 240 " | 120 " | 45 " |
| 64μA | 1750 " | 650 " | 241 " | 120 " | 45 " |
| 60μA | 1750 " | 650 " | 241 " | 120 " | 45 " |
| 50μA | 1750 " | 650 " | 250 " | 120 " | 48 " |
| 46μA | 1750 " | 650 " | 270 " | 125 " | 49 " |
| 40μA | 1750 " | 650 " | 290 " | 125 " | 51 " |
| 30μA | 1800 " | 650 " | 300 " | 140 " | 59 " |
| 20μA | 1900 " | 1300 " | 500 " | 150 " | Instrumentation Error |
| 18μA | 2000 " | 1350 " | 500 " | 155 " | " |
| 15μA | 2000 " | 1350 " | 510 " | 160 " | " |
| 5μA | 2100 " | 1350 " | 500 " | 180 " | " |
| 4μA | 2200 " | 1350 " | 580 " | 180 " | " |
| 3μA | 2200 " | 1350 " | 580 " | 200 " | " |
| 1.8μA | 2400 " | 1350 " | 580 " | 200 " | " |

Table B.4, Continued

| $I_D$(AMP) | 10HZ | 100HZ | 1K Hz | 10 KHz | 100 KHz |
|---|---|---|---|---|---|
| | | | IVN5200TND ($3x10^3$Cobalt Radiation) | | |
| 1.5μA | 2800 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 1350 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 580 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 200 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | Instrumentation Error |
| 1μA | 2800 " | 1350 " | 620 " | 210 | " |
| | | | VN64GA ($3x10^3$ Cobalt Radiation) | | |
| .4MA | 600 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 200 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 90 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 30 $\left(\frac{nV}{\sqrt{Hz}}\right)$ | 19 $\left(\frac{nV}{\sqrt{Hz}}\right)$ |
| .3MA | 660 " | 230 " | 110 " | 34 " | 21 " |
| .2MA | 930 " | 300 " | 125 " | 40 " | 32 " |
| .18MA | 930 " | 310 " | 150 " | 41 " | 40 " |
| .15MA | 1140 " | 350 " | 160 " | 47 " | 41 " |
| .13MA | 1200 " | 410 " | 180 " | 50 " | 50 " |
| .1MA | 1320 " | 425 " | 200 " | 55 " | 60 " |
| 80μA | 1680 " | 540 " | 215 " | 62 " | Instrumentation Error |
| 76μA | 1680 " | 540 " | 215 " | 62 " | " |
| 70μA | 1710 " | 540 " | 215 " | 66 " | " |
| 66μA | 1710 " | 541 " | 216 " | 66 " | " |
| 60μA | 1800 " | 610 " | 220 " | 70 " | " |
| 56μA | 1800 " | 610 " | 230 " | 72 " | " |
| 50μA | 2100 " | 610 " | 230 " | 90 " | " |
| 46μA | 2100 " | 650 " | 270 " | 91 " | " |
| 40μA | 2300 " | 750 " | 290 " | 91 " | " |
| 30μA | 2800 " | 800 " | 345 " | 100 " | " |
| 20μA | 2950 " | 2800 " | 615 " | 150 " | " |
| 15μA | 3000 " | 3000 " | 900 " | 168 " | " |
| 10μA | 3000 " | 3000 " | 1250 " | 180 " | " |

# APPENDIX C

## DEVICE SPECIFICATIONS

Table C.1. Specification for Siliconix VN64GA.*

**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| | | Characteristic | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| 1 | STATIC | $BV_{DSS}$ | Drain-Source Breakdown | 60 | | | V | $V_{GS}$ = 0V, $I_D$ = 500 μA |
| 2 | | $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | 2.7 | 4.0 | | $V_{DS}$ = $V_{GS}$, $I_D$ = 10 mA |
| 3 | | $I_{GSS}$ | Gate-Body Leakage | | 0.3 | 100 | nA | $V_{GS}$ = 12 V, $V_{DS}$ = 0 |
| 4 | | $I_{DSS}$ | Zero Gate Voltage Drain Current | | | 500 | μA | $V_{DS}$ = Max.Rating, $V_{GS}$ = 0 |
| 5 | | $I_{D(on)}$ | ON-State Drain Current | 12.5 | | | A | $V_{DS}$ = 25 V, $V_{GS}$ = 12 V (Note 1) |
| 6 | | $R_{DS(on)}$ | Drain-Source ON Resistance | | 0.3 | 0.4 | Ω | $V_{GS}$ = 12 V, $I_D$ = 10 A |
| 7 | DYNAMIC | $g_{fs}$ | Forward Transconductance | 1.5 | 2.2 | | ℧ | $V_{DS}$ = 20 V, $I_D$ = 5 A (Note 1) |
| 8 | | $C_{iss}$ | Input Capacitance | | 700 | | pF | $V_{GS}$ = 0, $V_{DS}$ = 25 V, f = 1.0 MHz |
| 9 | | $C_{rss}$ | Reverse Transfer Capacitance | | 25 | | | |
| 10 | | $C_{oss}$ | Output Capacitance | | 325 | | | |
| 11 | | $t_{on}$ | Turn-ON Time | | 45 | | ns | $V_{DS}$ = 10 V, $I_D$ = 10 A (Note 2) $R_L$ = 1 Ω, $R_S$ = 50 Ω |
| 12 | | $t_{off}$ | Turn-OFF Time | | 45 | | | |

NOTES: 1. Pulse Test – 300 μs, 1% duty cycle
2. See switching time test circuit

VNG

*. Siliconix Data Book.

Table C.2. Specification for Intersil VN98AK.*

**ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

| | | CHARACTERISTIC | | VN35AK | | | VN66AK, VN67AK | | | VN98AK VN99AK | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| 1 | STATIC | $BV_{DSS}$ Drain-Source Breakdown | | 35 | | | 60 | | | 90 | | | V | $V_{GS}$ = 0, $I_D$ = 10μA | |
| 2 | | $V_{GS(th)}$ Gate-Threshold Voltage | | 0.8 | | 2.0 | 0.8 | | 2.0 | 0.8 | | 2.0 | | $V_{DS}$ = $V_{GS}$, $I_D$ = 1mA | |
| 3 | | $I_{GSS}$ Gate-Body Leakage | | | 0.5 | 100 | | 0.5 | 100 | | 0.5 | 100 | nA | $V_{GS}$ = 15V, $V_{DS}$ = 0 | |
| 4 | | | | | | 500 | | | 500 | | | 500 | | $V_{GS}$ = 15V, $V_{DS}$ = 0, $T_A$ = 125°C (Note 2) | |
| 5 | | $I_{DSS}$ Zero Gate Voltage Drain Current | | | | 10 | | | 10 | | | 10 | μA | $V_{DS}$ = Max. Rating, $V_{GS}$ = 0 | |
| 6 | | | | | | 500 | | | 500 | | | 500 | | $V_{DS}$ = 0.8 Max. Rating, $V_{GS}$ = 0, $T_A$ = 125°C (Note 2) | |
| 7 | | | | | 100 | | | 100 | | | 100 | | nA | $V_{DS}$ = 25V, $V_{GS}$ = 0 | |
| 8 | | $I_{D(on)}$ ON-State Drain Current | | 1.0 | 2.0 | | 1.0 | 2.0 | | 1.0 | 2.0 | | A | $V_{DS}$ = 25V, $V_{GS}$ = 10V | |
| 9 | | $V_{DS(on)}$ Drain-Source Saturation Voltage | VN66AK | | | | | 1.0 | | | 1.1 | | V | $V_{GS}$ = 5V, $I_D$ = 0.3A | (Note 1) |
| 10 | | | VN98AK | | | | | 2.2 | 3.0 | | 2.2 | 4.0 | | $V_{GS}$ = 10V, $I_D$ = 1.0A | |
| 11 | | | VN35AK VN67AK | | 1.0 | | | 1.1 | | | 1.2 | | | $V_{GS}$ = 5V, $I_D$ = 0.3A | |
| 12 | | | VN99AK | | 2.2 | 2.5 | | 2.2 | 3.5 | | 2.2 | 4.5 | | $V_{GS}$ = 10V, $I_D$ = 1.0A | |
| 13 | | $g_{fs}$ Forward Transconductance | | 170 | 250 | | 170 | 250 | | 170 | 250 | | mU | $V_{DS}$ = 24V, $I_D$ = 0.5A | |
| 14 | DYNAMIC | $C_{iss}$ Input Capacitance | | | 40 | 50 | | 40 | 50 | | 40 | 50 | pF | $V_{GS}$ = 0, $V_{DS}$ = 24V, f = 1MHz | (Note 2) |
| 15 | | $C_{oss}$ Common Source Output Capacitance | | | 38 | 45 | | 35 | 40 | | 32 | 40 | | | |
| 16 | | $C_{rss}$ Reverse Transfer Capacitance | | | 7 | 10 | | 6 | 10 | | 5 | 10 | | | |
| 17 | | $t_{on}$ Turn ON Time | | | 3 | 8 | | 3 | 8 | | 3 | 8 | ns | | |
| 18 | | $t_{off}$ Turn OFF Time | | | 3 | 8 | | 3 | 8 | | 3 | 8 | | | |

**Note 1.** Pulse test — 80μs pulse, 1% duty cycle. **Note 2.** Sample test.

*. Intersil Data Book.

Table C.3. Specification for Intersil IVN5200TND.*

**ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted), $V_{BS}$ = 0

| | | CHARACTERISTICS | | IVN5200TND IVN5201TND | | | IVN5200TNE IVN5201TNE | | | IVN5200TNF INV5201TNF | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| 1 | STATIC | $BV_{DSS}$ Drain-Source Breakdown Voltage | | 40 | | | 50 | | | 80 | | | V | $V_{GS}$ = 0, $I_D$ = 100μA | |
| 2 | | $V_{GS(th)}$ Gate Threshold Voltage | IVN5200 Series | 0.8 | | 2.0 | 0.8 | | 2.0 | 0.8 | | 2.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 5mA | |
| 3 | | | IVN5201 Series | 0.8 | | 3.6 | 0.8 | | 3.6 | 0.8 | | 3.6 | | | |
| 4 | | $I_{GSS}$ Gate-Body Leakage | | | 0.2 | 20 | | 0.2 | 20 | | 0.2 | 20 | nA | $V_{GS}$ = 12V, $V_{DS}$ = 0 | |
| 5 | | | | | | 100 | | | 100 | | | 100 | | $V_{GS}$ = 12V, $V_{DS}$ = 0, $T_A$ = +125°C | |
| 6 | | $I_{DSS}$ Zero Gate Voltage Drain Current | | | | 100 | | | 100 | | | 100 | μA | $V_{DS}$ = Max. Rating, $V_{GS}$ = 0 | |
| 7 | | | | | | 5.0 | | | 5.0 | | | 5.0 | mA | $V_{DS}$ = 0.80 Max. Rating, $V_{GS}$ = 0, $T_A$ = +125°C | |
| 8 | | | | | 100 | | | 100 | | | 100 | | nA | $V_{DS}$ = 24V, $V_{GS}$ = 0 | |
| 9 | | $I_{D(on)}$ ON-State Drain Current | IVN5200 Series | 5.0 | 10 | | 5.0 | 10 | | 5.0 | 10 | | A | $V_{DS}$ = 24V, $V_{GS}$ = 10V | |
| 10 | | | IVN5201 Series | 5.0 | 10 | | 5.0 | 10 | | 5.0 | 10 | | | $V_{DS}$ = 24V, $V_{GS}$ = 12V | |
| 11 | | $V_{DS(on)}$ Drain-Source Saturation Voltage | IVN5200TND IVN5200TNE IVN5200TNF | | 1.5 | | | 1.5 | | | 1.5 | | V | $V_{GS}$ = 5V, $I_D$ = 2.0A | |
| 12 | | | | | 1.9 | 2.5 | | 1.9 | 2.5 | | 1.9 | 2.5 | | $V_{GS}$ = 10V, $I_D$ = 5.0A | |
| 13 | | | IVN5201TND INV5201TNE IVN5201TNF | | 1.2 | | | 1.2 | | | 1.2 | | | $V_{GS}$ = 7V, $I_D$ = 2.0A | (Note 1) |
| 14 | | | | | 1.8 | 2.5 | | 1.8 | 2.5 | | 1.8 | 2.5 | | $V_{GS}$ = 12V, $I_D$ = 5.0A | |
| 15 | | $r_{DS(on)}$ Static Drain-Source ON Resistance | IVN5200 Series | | 0.38 | 0.50 | | 0.38 | 0.50 | | 0.38 | 0.50 | Ω | $V_{GS}$ = 10V | $I_D$ = 5.0A |
| 16 | | | IVN5201 Series | | 0.36 | 0.50 | | 0.36 | 0.50 | | 0.36 | 0.50 | | $V_{GS}$ = 12V | |
| 17 | DYNAMIC | $r_{ds(on)}$ Small-Signal Drain-Source ON Resistance | IVN5200 Series | | 0.38 | 0.50 | | 0.38 | 0.50 | | 0.38 | 0.50 | | $V_{GS}$ = 10V | $I_D$ = 5.0A f = 1KHz |
| 18 | | | IVN5201 Series | | 0.36 | 0.50 | | 0.36 | 0.50 | | 0.36 | 0.50 | | $V_{GS}$ = 12V | |
| 19 | | $g_{fs}$ Forward Transconductance | | 1.0 | 1.8 | | 1.0 | 1.8 | | 1.0 | 1.8 | | mho | $V_{DS}$ = 24V, $I_D$ = 5.0A, f = 1KHz | |
| 20 | | $C_{iss}$ Input Capacitance | | | 210 | 250 | | 210 | 250 | | 210 | 250 | pF | $V_{DS}$ = 24V, $V_{GS}$ = 0, f = 1MHz | (Note 2) |
| 21 | | $C_{oss}$ Output Capacitance | | | 160 | 200 | | 160 | 200 | | 160 | 200 | | | |
| 22 | | $C_{rss}$ Reverse Transfer Capacitance | | | 45 | 60 | | 45 | 60 | | 45 | 60 | | | |
| 23 | | $t_{d(on)}$ Turn-ON Delay Time | | | | 20 | | | 20 | | | 20 | ns | See Switching Times Test Circuit $I_D$ = 4.0A | (Note 2) |
| 24 | | $t_r$ Rise Time | | | | 20 | | | 20 | | | 20 | | | |
| 25 | | $t_{d(off)}$ Turn-OFF Delay Time | | | | 20 | | | 20 | | | 20 | | | |
| 26 | | $t_f$ Fall Time | | | | 20 | | | 20 | | | 20 | | | |

**Note 1.** Pulse test — 80μsec, 1% duty cycle
**Note 2.** Sample test.

*. Intersil Data Book.

# APPENDIX D

## QUAN-TECH NOISE ANALYZER

### Description

The Quan-Tech Model 2181 Filter Unit provides the noise readout in the 2173C/2181 noise analysis system. This unit was designed to monitor the noise output of the Model 2173C at five frequencies simultaneously. Front panel metering and attenuator switches are provided to perform this function.

### Specifications

Noise Ranges

3, 10, 30, 100, 300, 1000 and 3000 nanovolts full scale (Referred to the base of the transistor under test for an equivalent one cycle noise bandwidth).

Measurement Accuracy

± 1 db.

Filter Frequencies

10 and 100 cycles; 1 Kc, 10 Kc and 100 Kc.

Power Input

117/234 volts, 60 cycles.

Dimensions

5¼" x 10" standard rack panel, 17" deep overall.

Weight

2181 without case-20 lbs., 2181 with 5¼" case-31 lbs., 2173C/2181 with 10½" case-58 lbs.


The transistors were connected to a socket inside the box located on the lower left hand corner of the transistor noise analyzer.

Figure D.1. Transistor noise analyzer system. (a) Model 2173C control unit. (b) Model 2181 Filter unit.

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