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The University of Arizona, 1987

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ALTERNATE SCREENING PROCEDURES FOR
SEMICONDUCTOR VISUAL INSPECTION

by
Fernando Guarin

A Thesis Submitted to the Faculty of the
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
In Partial Fulfillment of the Requirements
For the Degree of
MASTER OF SCIENCE
WITH A MAJOR IN ELECTRICAL ENGINEERING
In the Graduate College
THE UNIVERSITY OF ARIZONA

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ABSTRACT

A sequence of electrical tests was developed to provide a viable alternative to the performance of high magnification visual inspection for high reliability integrated circuits in a large volume production environment.

The primary approach was based on: close monitoring of the Substrate-N epi I-V characteristics, voltage overstress exposure and subsequent verification of the devices' low level leakage and thermal response.

This method was implemented and evaluated for the specific case of a 16K Bipolar Schottky PROM. Reliability tests indicated that devices processed using the proposed alternate screen sequence achieved failure rates as low as those obtained using high magnification visual inspection.

CHAPTER 1

INTRODUCTION

The purpose of this project is to assess the reliability implications of instituting alternate screening procedures in lieu of the 100% internal visual screen requirements as outlined by method 2010.8 of MIL-STD-883C.

The implementation of an alternate screening procedure that could achieve or enhance the reliability levels attained by optical inspections represents a very attractive alternative for semiconductor manufacturers.

As the integration levels increase, the inspection of higher density devices will not lend itself to the achievement of a uniform visual inspection making this operation more susceptible to variations in optical equipment, operators' subjective criteria and ability to contend with monotonous highly repetitious patterns. From the economic point of view, the alternate screening procedures have a clear advantage; visual inspections increase manufacturing costs and also decrease through-put during the assembly operation.

Per the MIL-STD-883 requirements the visual inspection can be divided into two major groups; high magnification

visuals (100x to 200x), and low magnification visuals (30x to 60x). The high magnification visuals are set to detect faults in the following areas: metallization defects, diffusion and passivation layer(s) faults, scribing and die defects, glassivation defects, dielectric isolation defects, and film resistor defects. The low magnification visual inspection's aim is to detect faults in the following areas: bonds, internal leads, and package conditions.

The main goal of this project was to evaluate the feasibility of electrical screening procedures as a viable alternative, specifically for the replacement of the high magnification criteria. As a starting point the methods outlined by method 5004.7 of MIL-STD-883C were evaluated in a practical manner by using a 2048 x 8 Bipolar Schottky PROM, currently manufactured and qualified to 883 class B requirements. Two lots from different wafer runs were assembled in compliance to 883C requirements except for the high magnification visual criteria which was completely deleted for these evaluation lots (except for one sub-lot). The reliability implications of this approach were then evaluated by performing a burn-in life test to assure the long term performance of the devices.

The secondary goal was to establish a practical implementation of this approach in an actual product flow,

generating a sequence of tests and inspections that will be capable of assuring product reliability in a standard production environment.

In order to develop an alternative to the visual inspection we must have a clear understanding of the rationale behind each of the visual criteria to be replaced by an alternate electrical test. In Chapter 2 we will present and analyze the high magnification visual inspection criteria currently required by MIL-STD-883 method 2010.

The development of the actual test sequence that will be used in lieu of the visual inspection is presented in Chapter 3. The experimental procedures and results are given in Chapter 4 and the final conclusions are drawn in Chapter 5.

The formulation of an electrical screen is highly dependent upon the specific fabrication process and actual circuit implementation. This information will be presented in Appendix A for the Bipolar Schottky PROMs used throughout this evaluation.

CHAPTER 2

VISUAL INSPECTION REQUIREMENTS

2.1. Limitations

The amount of criticism of MIL-S-883C method 2010.7 visual inspection requirements has increased in a manner that is directly proportional to the decrease of feature sizes for semiconductor devices. It is widely recognized that a new standard will be required for handling today's VHSIC program and other small geometry device requirements.

From the economic point of view the impact of 100% visual inspection has a significant effect on the price of the semiconductor devices sold for end use in government equipment. According to one author¹, in 1978 he calculated a total of 2,000,000 man hours of highly skilled operators' labor were spent performing pre-seal visual inspection. Human inspection also creates a bottle neck in the process as it is slow compared to the production rates of other assembly steps, thus increasing cycle times. This operation is also going to have a yield impact that will be considerable in many cases, as rejection is clearly preferred for marginal devices and the correlation between rejected units to actual reliability rejects is dubious in

many instances.

The visual inspection requirement has been instituted for an improved reliability level. It is almost totally dependent on human inspectors whose performance is affected by multiple factors. Their ability to perform repeatable and accurate results when inspecting the highly repetitious patterns used in VLSI semiconductor devices has been documented^{2,3,4,5} as being generally inadequate and variable. There is therefore a level of uncertainty introduced that is in direct conflict with the improved reliability level sought by performing the visual inspection.

In addition to the economic and human factors outlined above, there are technical arguments about the ability of fault detection by visual means. Limitations are introduced by the use of optical microscopes, such as the ability to detect microcracks formed as aluminum thins out over steps. There are several metallization-inspection criteria geared to the detection of electromigration inducing faults, such as scratches or voids that could result in higher current densities. For a dual metal process such as the bipolar PROMS utilized throughout this project, the thickness of the top layer of metal is greater, causing the current density on the lower layer (that can not be visually inspected in most of its area) of

metal to be larger and therefore more prone to electromigration related failures. The lower layer of metal cannot be inspected for corrosion, adherence, bridging or alignment. The inspection for diffusion, passivation and dielectric isolation cannot be performed over the entire die surface area. In addition we are confronted with the fact that the bond visual inspection is not indicative of wire-bond strength.

On the otherhand, visual inspection can be quite effective for the detection of workmanship related defects, chip interconnections, mounting to package, gross mechanical damage or misplacement of bonds, large cracks and chip-outs. It is our contention that these types of defects can be adequately detected by a low magnification visual inspection.

2.2 MIL-M-38510

MIL-M-38510 is a set of specifications defining the requirements a manufacturer must meet in order to have a particular device type included on the qualified parts list (QPL), and the steps necessary to maintain that qualification. This document also outlines the quality and reliability assurance requirements which must be met in the acquisition of microcircuits, providing users with a mechanism to procure standardized integrated circuits with replaceability and screening flow uniformity. This

standardization program utilizes the testing procedures of MIL-STD-883. The MIL-M-38510 is tailored to a specific device by a document commonly referred to as a "Slash-Sheet" which is a very detailed specification that defines the appropriate electrical test sequence as well as any other specific processing attributes that may be applicable to the device.

2.3. MIL-STD-883

MIL-STD-883 is a standard outlining uniform methods, controls and procedures for the design, test and certification of microelectronic devices intended for military and aerospace applications. It can be subdivided into two primary areas: 1) Methods 1001 through 4007 are detailed how-to specifications. 2) Requirements for screening, qualification and quality conformance are contained in methods 5001 through 5009.

2.4 MIL-STD-883C Method 2010

Due to the nature of this project a closer presentation of the requirements outlined by Mil-STD-883C Method 2010.7 Paragraph 3.2 will be given, specifically emphasizing those pertaining to "B" level or test condition B. Method 5004 defines a generalized alternate screening procedure that can be used in place of method 2010 and will

be presented in section 2.5.

2.4.1 Metallization Defects

The inspection for metallization defects is conducted in the 75X to 150X magnification range on all devices. The various criteria inspected are outlined in table 2-1. Any tearing defect in the surface of the metallization layer is referred to as a "scratch". The various criteria for this type of defect are intended to guarantee not only that there will be sufficient metal remaining to provide good electrical contact, but also that there will be enough conductor area left to handle the required current density. Operation at excessively high current densities will induce electromigration effects that compromise the reliability of the devices. This phenomenon will be presented in Chapter 3.

Any defect in the metallization where underlying metal or passivation is visible and is not caused by a scratch is referred to as a "void". The main concern, once again is to provide the electrical connection with adequate current density handling capability. The inspection for probing will check for damage induced on bond pads during electrical wafer sort test. It follows the same criteria given for Scratches. Another cause for visual rejection is metallization "Bridging", where the separation between any two metallization paths must be greater than 0.1 mil,

"S" Level	"B" Level	
<u>30x to 60x</u>	<u>30x to 60x</u>	<u>Low magnification (L M)</u>
<u>100x to 200x</u>	<u>75x to 150x</u>	<u>High Magnification(H M)</u>
3.1.1	3.2.1 *	Metallization defects (H M)
3.1.1.1	3.2.1.1	Metallization Scratches
3.1.1.2	3.2.1.2	Metallization Voids
3.1.1.3	3.2.1.3	Metallization Corrosion
3.1.1.4	3.2.1.4	Metallization Adherence
3.1.1.5	3.2.1.5	Metallization Probing
3.1.1.6	3.2.1.6	Metallization Bridging
3.1.1.7	3.2.1.7	Metallization alignment
3.1.2	3.2.2 *	Diffusion and Passivation Faults (H M)
3.1.3	3.2.3 *	Scribing and Die defects (H M)
3.1.4	3.2.4	Bond Inspection (L M)
3.1.5	3.2.5	Internal Leads (L M)
3.1.6	3.2.6	Package (L M)
3.1.7	3.2.7 *	Glassivation Defects (H M)
3.1.8	3.2.8 *	Dielectric Isolation (H M)
3.1.9	3.2.9 *	Film Resistor (H M)
3.1.10	3.2.10	Laser Trimmed Film Resistor (H M)

* Deleted for Method 5004

TABLE 2-1
883C Method 2010 Requirements

unless specifically so intended by design.

The inspections for metallization "Corrosion" and "Adherence" are intended to spot faults induced by poor processing, such as incomplete cleaning operations where residual chemicals corrode the metallization lines or prevent them from properly adhering to the surface of the die. These faults are visually manifested on metal lines by : discoloration, lifting, peeling or blistering.

One final inspection of the metallization is for proper "alignment" over contact windows to assure an adequate connection with low resistive losses to underlying layers.

At this point it is important to mention one more screen prescribed for the metallization layer by MIL-STD-883C method 2018: Scanning Electron Microscope (SEM) Inspection of Metallization. Unlike the other visual criteria it is only performed on a sample basis and only over specific areas of the device. It is primarily geared for step coverage verification over oxide steps to detect microcracks or adhesion problems.

2.4.2 Diffusion and Passivation Faults

This inspection is geared to detect: diffusion junction lines that unintentionally cross into other diffusion junction lines, isolation diffusions that are discontinuous or substantially reduced in their width, and finally, active junctions that are not covered by passivation unless

by design. Incomplete isolation or unintentional contacts between junction tubs are sought by this criteria.

2.4.3 Scribing and Die Defects

Devices are inspected for chip-outs and cracks on both the die and passivation regions. These types of mechanical defects are generally induced during the assembly process either in the saw or die attach operations. As the devices operate over sudden wide temperature variations, there are concerns that these defects will propagate and degrade the device's reliability.

2.4.4 Glassivation Defects

Reasons for rejection are: lifting or peeling of the glassivation, lack of coverage over two or more adjacent active metallization paths (except for bond pad areas), glassivation over bond pad areas and lack of coverage at the edge of bond pad areas.

The main concerns are: to assure that glassivation will adequately protect adjacent metal lines from becoming connected by foreign materials within the package, to make sure that bond pad areas are free from glass that would prevent adequate bonding of wires, and that the periphery of bond pads should be covered to protect bonding wires from making connections that were not intended.

2.5 MIL-STD-883C Method 5004

The military flow already has a provision for alternate screening. The high magnification inspections presented in table 2-1 and marked with asterisks can be deleted per this method. It should be pointed out that they are not all completely deleted as the following requirements are added to the low magnification "package" visual inspection: Scratches or other mechanical damage to the die surfaces and defects along die edges (chip-outs, cracks, tool marks).

In order to allow for the deletion of the high magnification visual inspection, the minimum total of temperature cycles is increased from 10 to 50, as well as the addition of a voltage stress at 120 percent of the normal operating voltage followed by a low level leakage test on all input and output pins which can be reverse biased.

CHAPTER 3

DEVELOPMENT AND IMPLEMENTATION OF AN ALTERNATE SCREEN TEST SEQUENCE

3.1 Failure Modes/Mechanisms and Accelerating Factors

In order to develop an effective alternate screen, we must first understand clearly the failure mechanism, its associated failure mode and accelerating factors prior to formulating an adequate test or sequence of tests. In our case we are trying to replace a visual inspection step by introducing an alternate way to screen the same types of faults by means of additional electrical tests that will maintain or improve the reliability of the integrated circuits. These tests are to be performed on all units and must therefore be of a non-destructive nature. They must also be rapid and repeatable, so they will be performed using automatic electrical testers, sampling a specially developed sequence of tests that can be instituted during the standard first electrical test step for packaged devices, without requiring additional operations.

The inspection of the metallization layer for scratches and voids is performed primarily to reduce the risk of conductors being exposed to current densities above

their capabilities that could induce electromigration related failures. A void or a scratch that is large enough to cause an "open" in a metal stripe will be very easily detected by means of both parametric and functional electrical testing. A fault created by bridging metal would also be detected by the electrical testing.

In the cases where there is a narrower continuous metal path remaining, conditions of stress that would accelerate the failure mechanism shall be included in the screen. These conditions include elevated temperature operation-- this will be accomplished by performing a burn-in operation; and higher current density--the devices will be exposed to overstress voltages that will lead to operation in higher current ranges. Electrical screening at elevated temperature will also help eliminate this type of defect.

There are also scratches that are not caused during the fabrication process but are induced by subsequent steps such as wafer probing, handling with tweezers and other packaging-related activities. These defects will be detected by the method 5004 visual inspection. This low power visual inspection will also be sufficient for adequate inspection for corrosion induced discoloration of metal, metallization adherence, metallization probing, metallization alignment and scribing defects. These faults

can also be temperature accelerated. Those that are due to mechanical stress can be accelerated by temperature cycling.

The inspection for diffusion-related failures is performed to screen out devices where non-uniform current flow is likely to occur because of diffusion-related causes, which could affect the curvature of the junctions, emitter resistivity, base width, and in severe cases create undesired connections to isolation tubs. These faults can be electrically screened out by close monitoring of the I-V characteristics of the diffused junctions and can also be accelerated by higher temperature operation and testing.

The detection of passivation faults seeks to detect faults in the passivation layer that would cause it to provide inadequate insulation or lower breakdown voltages due to the presence of contaminants which can not be detected by visual means, or due to cracks or holes in this layer. These faults can be electrically screened by measuring currents under voltage overstress conditions that would force faulty devices into breakdown operation. Reverse current leakage tests are also useful. Both high temperature exposure and cycling can be used for accelerated testing.

3.1.1 Electromigration Overview

Electromigration has been defined as ⁶"The mass transport of metal atoms by momentum exchange with conducting electrons". It occurs as a result of a high current density ($>10^5 \text{ A cm}^{-2}$ for Al) and at elevated temperatures ($>100 \text{ deg. C.}$) that lead to metal flow toward the positive potential and vacancies or voids to flow in the opposite direction, leading to ⁷growths, hillocks and bumps in one area and voids and microcracks in others, resulting in open-circuit device failures. A model has been developed ⁸that presents the following relationship;

$$1/\text{MTTF} = C J^2 e^{-E_a/KT}$$

Where:

MTTF = Median time to failure in hours

C = Constant which contains a factor involving
the cross-sectional area of the film

J = Current density in Amps/cm²

E_a = Activation Energy

K = Boltzman's constant, and

T = Film temperature in degrees kelvin

Therefore suitable acceleration factors can be both temperature and current density. Factors that are relevant are: grain size, area, temperature and current density. A more in-depth list of the variables affecting the formation

of a single void would include⁹: the spacial variation in current density within the conductor, temperature gradients, flux divergence, preferred orientation, variations in grain boundary orientation, local fields, external ambients, intentional dopants, precipitates, surface oxide layer, stress, and effective charge. All of these factors are presented as a mere reference to present the reader with the complexity and variety of factors that will influence the electromigration process. Their detailed study is beyond the intent of this project.

3.2 Accelerated Testing

We have seen that for a vast number of integrated circuits today the time to failure is in the 10^6 to 10^9 operating hour range, which would give us a time to failure from 114.2 to 114,200 years making it, therefore, quite impractical to conduct life tests under normal operating condition. It is necessary to find ways to accelerate the device's failure mechanisms to be able to conduct meaningful reliability testing of life expectancy in a reasonable amount of time. The most common stresses used are: temperature, temperature cycling, vibration and shock, humidity, voltage, current, power cycling, electrostatic discharge and radiation.

In order to make good use of accelerated testing we

must develop a good understanding of the failure mechanisms as well as their acceleration as a function of the applied stress. The failure modes observed in the accelerated environment must be the same as those observed under normal conditions of use, and it should be possible to extrapolate from the accelerated environment to the normal operating condition.

3.2.1 Temperature Acceleration (Arrhenius Equation)

A very common relationship between stress and time to failure involves the effect of temperature which accelerates physical and chemical processes that could lead the devices to failure. The best known stress-lifetime relationship is given by the Arrhenius Equation:¹⁰

$$R = R_0 e^{-(E_a/KT)}$$

Where:

R_0 = Constant

E_a = Activation Energy in Electron-Volts (ev)

K = Boltzman's Constant, 8.6×10^{-5} ev/ °K

T = Absolute Temperature in Degrees Kelvin(°K)

and the temperature-lifetime relationship is given by:

$$t = C e^{E_a/KT}$$

or

$$\ln t = C + E_a/KT$$

where C is a temperature independent constant.

The key parameter in the Arrhenius Equation is the Activation energy, E_a ; this parameter is determined experimentally and it is connected primarily with a failure mechanism. The reported values for E_a will also be different for the main population compared to those used for the weak population. Different semiconductor manufacturers will quote activation energies with their published reliability reports; some typical values for bipolar devices are presented in Table 3-1.^{12,13}

Mechanism	E_a
Oxide Defects	1.0 to 1.05 ev
Metallization	
Electromigration	0.5 to 1.2 ev
Corrosion	0.3 to 0.6 ev
Bond and Other Mechanical Interfaces	1.0 to 1.05 ev

TABLE 3-1
Typical Reported " E_a " Values for Bipolar Devices

It should be noted that special care must be exercised in selecting the appropriate E_a value as these reported values are often from laboratory tests at temperatures in

the range of 150 to 300 C. and there is no guarantee that the same mechanisms will be dominant under normal operating conditions. There can be different failure mechanisms for two different manufacturers of an integrated circuit of the same function. Also there could be stresses other than temperature such as electrical or mechanical stress that will influence the value of E_a .

Using the Arrhenius Equation we can calculate the activation energy from equivalent failure times t_1 and t_2 at two temperature T_1 and T_2 as follows:

$$\ln t_1 = C + E_a / K T_1$$

$$\ln t_2 = C + E_a / K T_2$$

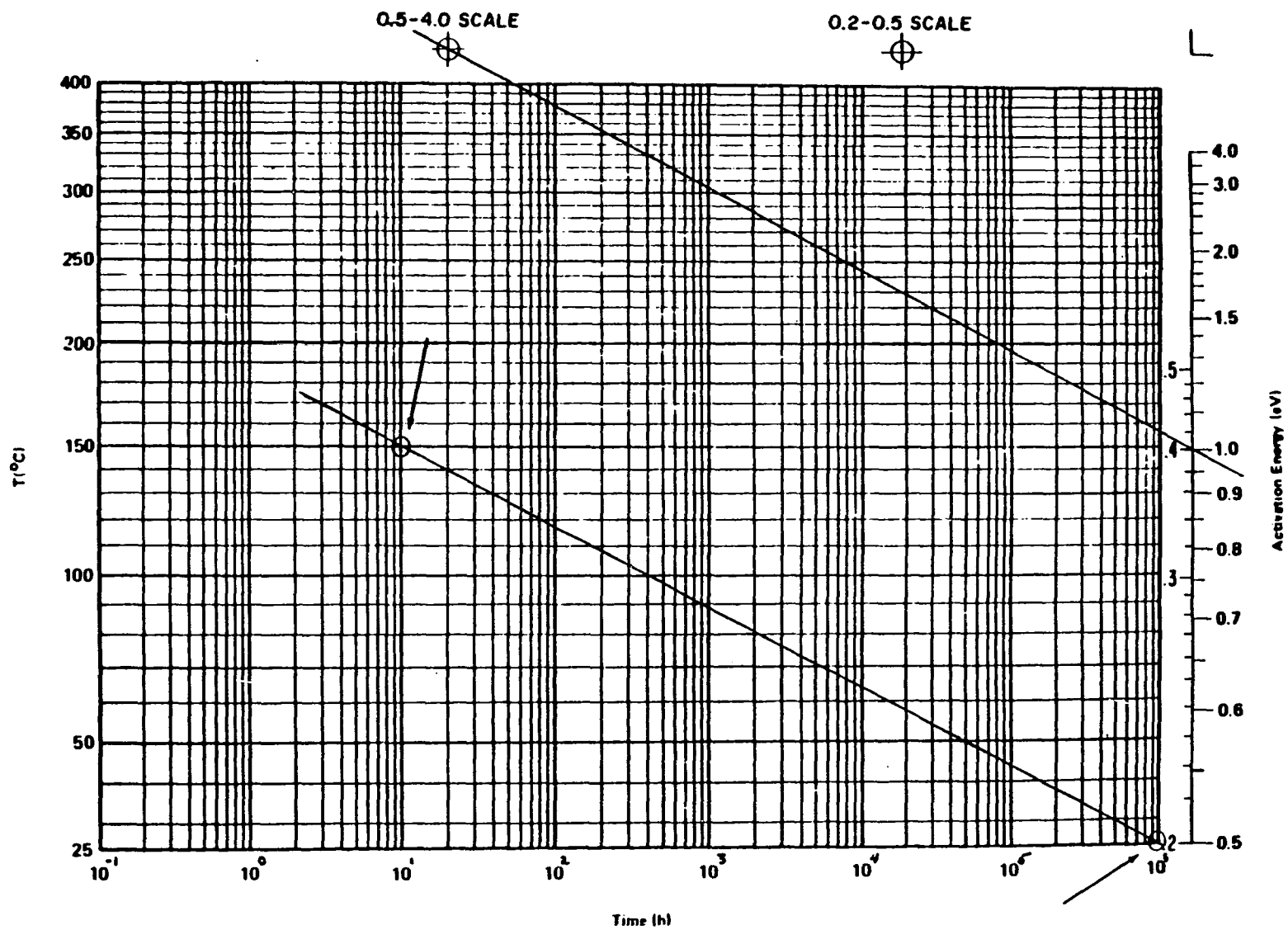
subtracting the two equations.

$$\ln t_1 - \ln t_2 = (E_a / K) (1/T_1 - 1/T_2)$$

$$\ln t_1 / t_2 = (E_a / K) (1/T_1 - 1/T_2)$$

It was beyond the scope of this project to experimentally determine the appropriate levels of E_a for the utilized Bipolar Schottky PROMs. A plot for the 1.0 eV E_a level used by MIL-M-883B method 1015 is presented in Fig 3-1. This plot provides a convenient mean for rapidly estimating time equivalencies at different temperatures with a reasonable level of accuracy (calculated 1000 hr. @ 125 C. equivalency to 184 hr. @ 150 C. is marked).

Arrhenius Graph
Figure 3-1



3.2.2 Temperature Cycling

The purpose of this test is to determine the immunity of a device to exposure to rapid temperature variations without suffering degradation of the hermeticity of the package or cracks on the chips due to temperature coefficient mismatches in utilized material. MIL-M-883C method 1010 describes this test which consists normally of 10 cycles of -65 to +150 degrees C but is increased to 50 cycles for the alternate screen flow.

3.2.3 Voltage and Current Stress

Both voltage and current are effective accelerating stresses for: dielectric breakdown, interface charge accumulation, charge injection and corrosion. The acceleration factor due to voltage stress can be computed following the model¹¹:

$$V_1/V_2 = e^{B(V_1 - V_2)}$$

Where:

V₁=Stress voltage

V₂=Maximum operating voltage

B=Constant

Device operation at higher current levels can be used to accelerate failures caused by electromigration in the metallic conductors.

3.3 Test Development

3.3.1 Substrate-Isolation Diode Characteristics

When designing electrical screens for integrated circuits we are confronted with the fact that not all nodes are readily available for testing and we must therefore select those structures where the probability of encountering the various types of defects is the greatest. It is for this reason that one of the key areas targeted for this evaluation is the substrate-isolation diode. The current-voltage or I-V characteristic for this diode can be seen in Figure 3-2. This distributed substrate-NEpi isolation diode can be accessed from the external VCC and ground pins.

Looking at the schematic for the individual memory cell array given in figure A-6 of Appendix "A", we take advantage of the fact that each of the pass transistors to the individual fuses has its collector directly tied to the VCC pin, and the underlying substrate connected to ground.

This structure forms the main memory array and occupies the largest area of the device providing, therefore, the greatest probability for fault detection when tested. To obtain the curve presented in Figure 3-2 the voltage on the VCC pin was varied from -2.50 volts to +2.50 volts and the current to the ground lead was measured. For the voltage around -0.5 volts the substrate

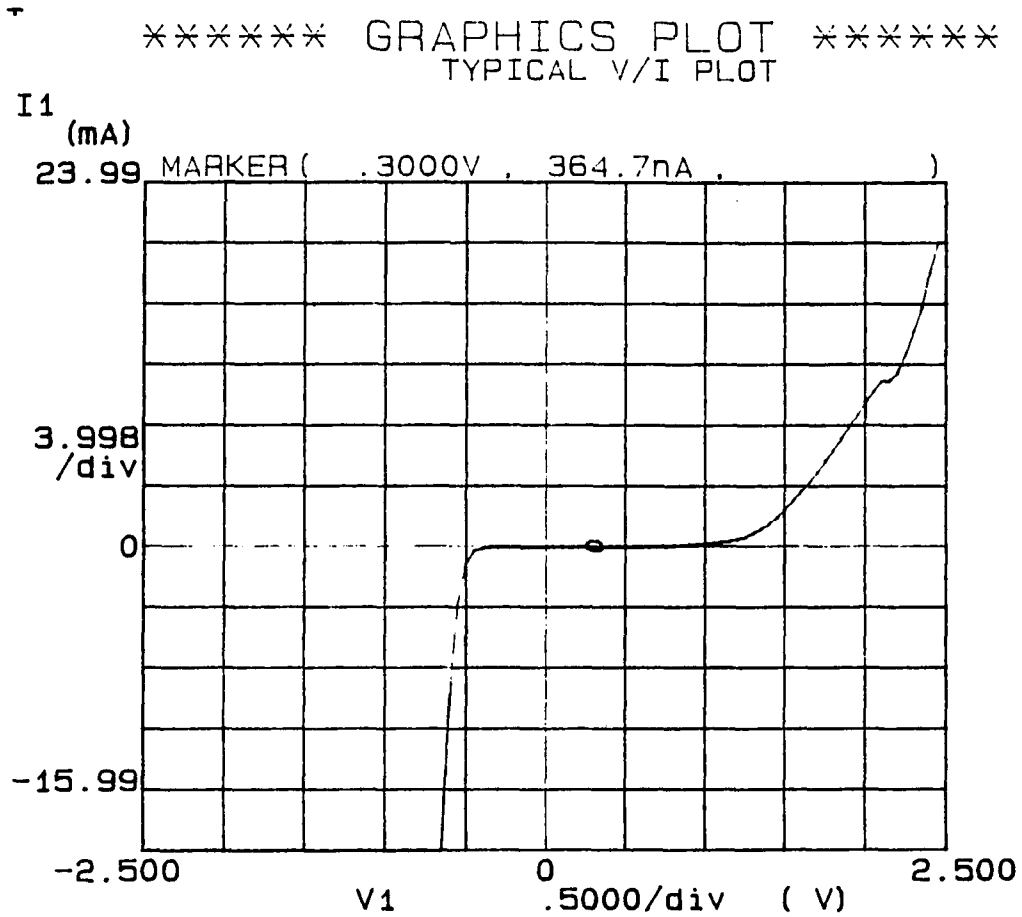


Figure 3-2
Typical V/I Plot

diode is forward biased and the negative current increases sharply for small variations in voltage. When a positive voltage is forced, the substrate-isolation diode is operating under reverse-bias conditions; only for voltages above 1.0 volt is there a noticeable increase in current. This increase in the current drained from the VCC lead for voltages above 1.0 volt is due to other areas of the internal circuitry becoming active and demanding current from the supply.

Figure 3-3 plots the I-V characteristic, greatly expanding the vertical current axis to give a more detailed view of the low current characteristic. At about 0.4 volts, the current begins to rise sharply. After characterizing several devices it was decided to select a voltage of 0.3 volts as the level to be forced on the VCC pin for the low-level reverse-leakage measurement. This point is on the flatter portion of the curve for the bulk of the distribution of the tested devices, so by operating in this region the low current measurements will be made more repeatable.

The ideal diode equation relating current to voltage is given by:

$$I = I_s (e^{V/V_t} - 1)$$

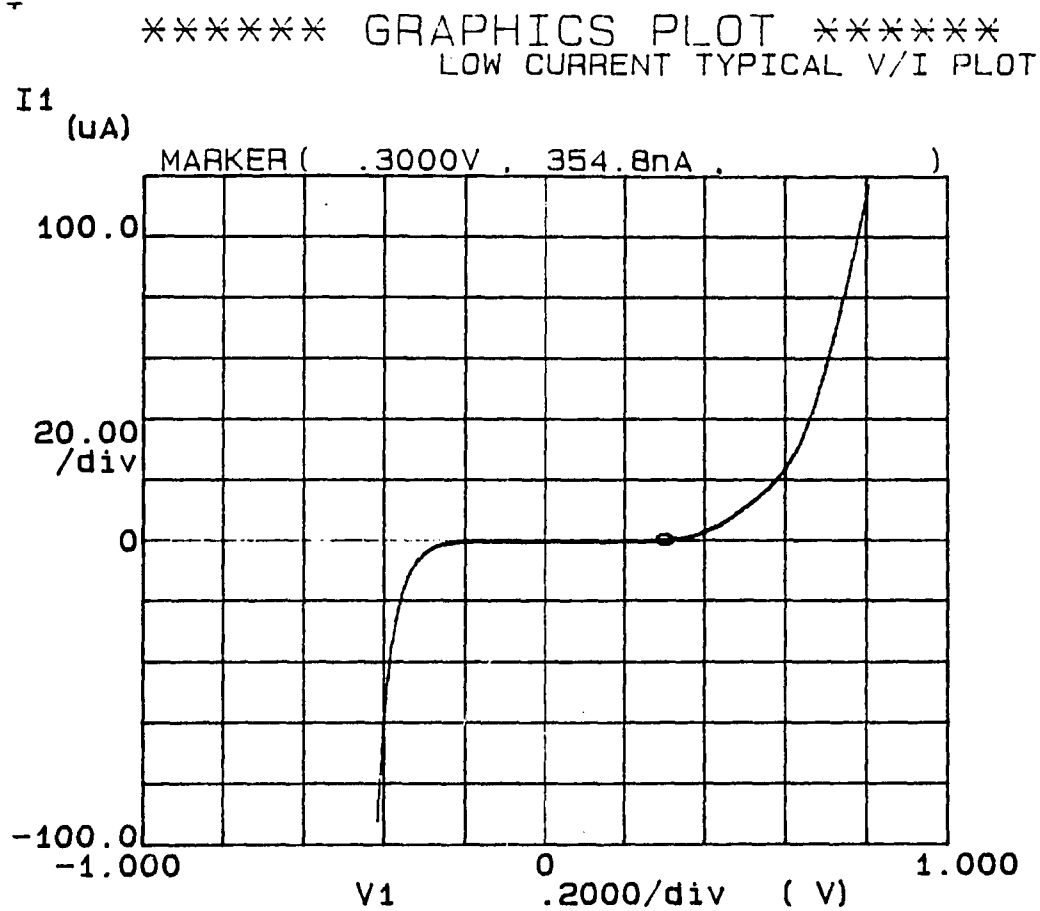


Figure 3-3

Low Current Typical V/I Plot

where " V_t " is the thermal voltage given by: $V_t = KT/q$ and the term " I_s " denotes a constant referred to as the saturation current. For values of $V < -4V_t$, the diode equation becomes; $I = -I_s$, for the voltage of -0.3 volts that we have selected the ideal diode equation would yield a $-I_s$ value. This " I_s " term has been shown ⁹ to be directly proportional to the square of the intrinsic carrier concentration n_i which in turn is proportional to $T^3 e^{-E_{go}/KT}$.

It is therefore rather sensitive to temperature variations. In practice the currents measured at this voltage level are due to thermal generation of holes and electrons in the depletion region, and to leakage across the surface rather than to " I_s ". A controlled temperature environment will be required for this measurement.

3.3.2 VCC Stress Level Characteristics

To understand how the limit and voltage level are selected, we refer to Figure 3-4. The Y axis plots ICC and VCC is plotted along the X axis. For the device shown, ICC increases linearly with VCC up to a value of 7.98 volts. After this value an alternate path of the circuit is enabled via the 8.0 volt High Voltage Clamp Zener diodes shown in Figures A-5 and A-6 of Appendix "A" and described in section A.3.4. The value of ICC decreases temporarily for values above this level.

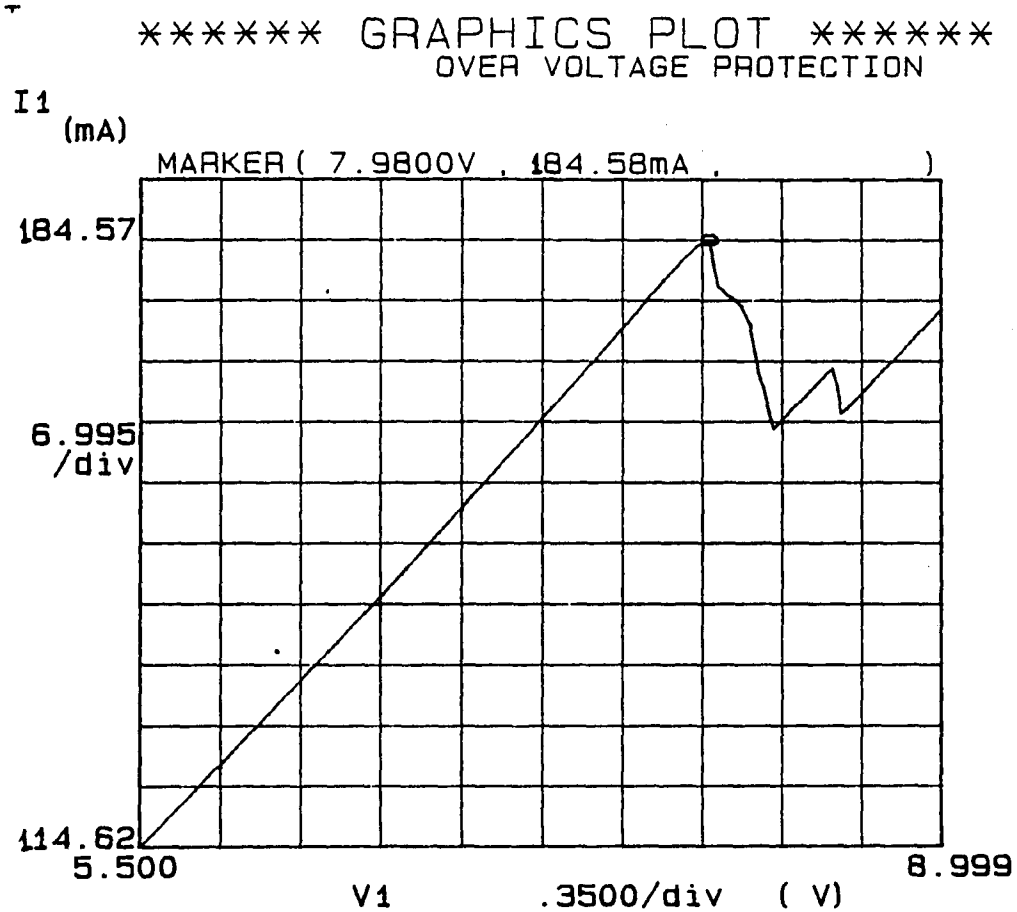


Figure 3-4
Over-Voltage Protection

By testing at 7.50 volts we are high enough to have both increased current density levels as well as voltage overstress.

This supply current or ICC test at 7.50 volts will screen voltage overstress, lower breakdown voltage and provide operation under higher current densities.

3.4 Proposed Alternate Screen Test Sequence

The actual sequence of tests instituted for the alternate screen are shown in Table 3-2. The limits were set to approximately three standard deviations of the mean value for the units characterized.

The first test performed is a low level current test at -10 uA of the input clamp diodes (VICL) on all the address and chip enable pins. The rationale and types of defects targeted are the same as those previously discussed for the substrate-isolation diode. The limit of -0.36 volts was selected from characterization data, and the VCC line is held at 0.0 volts. It was decided to establish this VICL test over the low level current leakages recommended by method 5004 as a result of the fact that the voltage test proved to be more easily distinguishable on early characterization lots. It also was easier to get better voltage than current resolution in the utilized range.

ICC1 tests the low level reverse leakage current of the substrate-isolation diode as it was described

SUB GROUP	SYMBOL	HIL- STD-883 METHOD	CASE J, K, L	CASES																								MEASURED TERMINAL	TEST LIMITS		UNIT
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		MIN	MAX	
				A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	OE3	OE2	OE1	A10	A9	A8	VCC				
				TEST NO.																											
1 Tc = +25°C	VIOL	5004	501	-10 uA										GND												0.0V	A7	-0.36		V	
	VIOL		502		-10 uA									GND												0.0V	A6	-0.36		V	
	VIOL		503			-10 uA								GND												0.0V	A5	-0.36		V	
	VIOL		504				-10 uA							GND												0.0V	A4	-0.36		V	
	VIOL		505					-10 uA						GND												0.0V	A3	-0.36		V	
	VIOL		506						-10 uA						GND											0.0V	A2	-0.36		V	
	VIOL		507							-10 uA					GND											0.0V	A1	-0.36		V	
	VIOL		508								-10 uA				GND											0.0V	A0	-0.36		V	
	VIOL		509												GND						-10 uA					0.0V	OE3	-0.36		V	
	VIOL		510												GND							-10 uA				0.0V	OE2	-0.36		V	
	VIOL		511												GND								-10 uA			0.0V	OE1	-0.36		V	
	VIOL		512												GND									-10 uA		0.0V	A10	-0.36		V	
	VIOL		513												GND										-10 uA	0.0V	A9	-0.36		V	
	VIOL		514												GND											-10 uA	0.0V	A8	-0.36		V

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage.
Inputs not designated are high ≥ 2.0 V or ≤ 0.8 V.

ALTERNATE SCREEN
TABLE 3-2

		MIL-STD-883 CASE 3																								MEASURED		TEST LIMITS		UNIT		
SUB GROUP	SYMBOL	METHOD	CASES J, K, L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	TERMINAL	MIN	MAX		
				A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE3	CE2	CE1	A10	A9	A8	VCC					
				TEST NO.																												
1 Tc = +25°C	ICC1	5004	100	GND	GND	GND	GND	GND	GND	GND	GND	GND				GND							GND	GND	GND	GND	GND	0.3V	VCC		600	nA
	IOC2	5004	101	GND	GND	GND	GND	GND	GND	GND	GND	GND				GND							GND	GND	GND	GND	GND	5.5V	VCC		185	mA
	Stress	5004	102	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	GND	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	7.5V	Outputs	1/	1/	
	IOC3	5004	103	GND	GND	GND	GND	GND	GND	GND	GND	GND				GND							GND	GND	GND	GND	GND	7.5V	VCC		240	mA
	IOC4	5004	104	GND	GND	GND	GND	GND	GND	GND	GND	GND				GND							GND	GND	GND	GND	GND	0.3V	VCC		600	nA
	Delta		105	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	2/	-5	32

NOTES:

- 1/ The stress test shall verify that no fuses are blown for unprogrammed devices. By exercising all address locations and testing all bits while using the following voltage stress levels:
a. Inputs: $V_{IH} = 6.20V$, $V_{IL} = 0.0V$
b. Outputs: $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$
c. $V_{CC} = 7.50V$
The outputs are loaded per Figure 5 of MIL-H-38510 /210 D.
- 2/ Delta measurement shall be calculated as the difference on the readings between ICC1 (test 100) and IOC4 (test 104), $IOC4 - ICC1$.

ALTERNATE SCREEN
TABLE 3-2 (continued)

earlier in this section. A voltage of 0.30 volts is forced on the VCC pin, all of the input pins are connected to the ground potential and all of the outputs are left open. Prior to the performance of this test the device has been soaked at 25 degrees centigrade for an amount of time long enough to guarantee that the device under test has reached the correct temperature. Due to the close interaction between temperature and measured current it was very important to make every attempt to provide as controlled as possible a temperature environment for the test. Also, as it will be seen later, this effort was necessary to perform meaningful thermal characterization of the units. The ICC2 test is basically a current supply test at the maximum nominal limit of 5.50 volts and will insure that the device is within the reasonable range of supply currents under normal operating conditions.

In order to provide voltage overstress levels throughout more internal nodes, a sequential scan of all address locations under overstress voltage levels on all inputs, as well as the VCC line, will be performed. For this purpose the VCC pin is set to 7.50 volts, the input high level, V_{IH} , is set to 6.20V and the low level, V_{IL} , is set to 0.0V. All address locations are sequentially scanned, and the output data is verified to be that of a blank device (all 0's) under the specified load conditions.

To provide an additional current density stress and verify absence of undesired low breakdown voltage levels, the supply current is tested at 7.50 volts, in ICC3, and compared against the maximum current limit given by the characterization data.

The low-level reverse-leakage measurement performed in ICC1 is repeated now in ICC4 and the delta between the two measurements is calculated and compared against a minimum and a maximum limit. Due to the power dissipated in the device, especially during the stress test there will be an increase in the actual die temperature. Due to the close relationship between the measured current and device temperature, a thermal profile of the tested device is obtained and devices tested with higher or lower readings than those of the main population are rejected. This delta measurement would also be instrumental in detecting variations of current due to metal lines opening or becoming shorted due to Electromigration effects.

The full sequence of tests performed in the alternate screen test program is presented in Table 3-3. It includes all of the tests required by the slash sheet presented in Appendix "A" (Table A-2 in section A.4) plus the alternate screen test sequence. Note that Input and Output leakage tests recommended in method 5004 are already included in the standard Slash Sheet test program.

Low Current Input Clamp Voltage	*	VICL
Substrate Leakage	*	ICC1
Supply Current	*	ICC2
Stress Functional	*	
Stress Supply Current	*	ICC3
Substrate Leakage	*	ICC4
Delta	*	ICC4-ICC1
Test Word-Test Bit		TW/TB
Input Clamp Voltage		VIC
Low-Level Output Voltage		VOL
High-Level Output Voltage		VOH
Low-Level Input Current		IIL
High-Level Input Current		IIH
High Impedance Output High Current		IOHZ
High Impedance Output Low Current		IOLZ
Short Circuit Output Current		IOS
Supply Current		ICC
Gross Functional		
Prop. Delay High to Low (Address to Output)		TPHL1
Prop. Delay Low to High (Address to Output)		TPLH1
Prop. Delay High to Low (CE to Output)		TPHL2
Prop. Delay Low to High (CE to Output)		TPLH2

* Indicates tests not included in standard MIL-M-38510/210 or (S/S) program

TABLE 3-3
ALTERNATE SCREEN TEST PROGRAM (A/S)

CHAPTER 4

EXPERIMENTAL PROCEDURES AND RESULTS

4.1 Purpose

For the experimental part of this evaluation two lots (A and B) were used. Lot "A" was used mainly for two purposes; first to gather characterization data to implement the testing with realistic values in a repeatable manner; secondly it was used to assess long term reliability by performing several consecutive burn-in cycles, and subsequent electrical testing.

The primary objective of lot "B" was to test the effectiveness of the electrical alternate screen for detecting those devices that would have been rejected to the high magnification visual inspection and producing devices with the same or greater reliability level as those obtained by performing the full visual inspection to method 2010 of MIL-STD-883. It was for this reason that this lot was formed by material from only one wafer run and was split into two lots: "B-1" and "B-2".

The general flow for all of these lots is presented in Table 4-1. The main difference will be the visual inspection criteria.

Wafer Fabrication
Wafer Probe Testing
Saw
1st Visual Inspection
Die Attach
Lead Bond
2nd Visual Inspection
Seal
Bake (6HR @ 175 degree C)
Temperature Cycle (50 cycles, -65 to
+150 Degrees C.)
Centrifuge
Trim
Electrical Testing

TABLE 4-1
Lot Processing Flow

4.2 Visual Inspection Requirements

The requirements for MIL-STD-883C methods 2010 and 5004 have already been presented in Chapter 2, sections 2.4 and 2.5. For the purpose of our experiment: lot "A" was inspected per the reduced method 5004 requirements at magnifications ranging between 30x and 60x, lot "B-1" was inspected to the full 2010 requirements at both high and low magnification ranges, while lot "B-2" was only given a gross visual inspection at 30x per method 5004 guidelines. For this last lot whenever there were marginal/questionable visual rejects they were left in the lot to further test the ability of the electrical tests to detect such devices.

4.3 Lot Processing Requirements

4.3.1 Wafer Fabrication

Wafer fabrication was performed on a MIL-M-38510 class "B" certified line. The individual wafer runs used to form these lots were processed in conformance with the standard flow qualified for JAN (38510 QPL) bipolar PROMS. Each individual die on every wafer was electrically tested during the WAFER PROBE operation. Those that failed the test were inked, and removed from the lot, after the separation of each individual die was accomplished by the SAW operation.

4.3.2 Wafer Probe Testing

For wafer probe testing, each die was connected to the tester by using sharp, needle-like probes that are precisely controlled to make contact to the bond pads. Only one attempt to make this contact is allowed for military grade components as there is some scratching to the bond pad region by the probe during this operation. This test step was not to the device's slash sheet limits and requirements. It was merely a gate to screen out gross wafer defects. During this test the D.C. parametric performance was verified and a gross functionality check was also executed.

4.3.3 SAW

Individual die separation was performed using a diamond saw blade. This operation is particularly important for good yield during subsequent visual inspection. One of the most common criteria for visual rejection is chip-out (see Figure 4-1) induced during the saw operation. The main reasons for inducing chipping are:¹⁰ feed rate, grit size, coolant distribution, vibration, mounting media, cut depth, blade sharpness and cutting mode (down cutting or up cutting). Lot "B" experienced significant fall-out due to problems experienced during this operation during the first visual inspection.



Figure 4-1
Chip-Out Visual Reject

4.3.4 First Visual Inspection

After the separation of individual die, the first visual inspection was performed. This inspection was per method 2010 of MIL-STD-883 for lot "B-1" only, all of the other lots were screened per the alternate set of criteria outlined by method 5004. Both lots "B-1" and "B-2" experienced low yields due to the already mentioned problems during the Sawing operation. The yield loss was comparable even with the different visual magnification levels due to the fact that most of these Saw induced defects are gross and easily detectable at low magnification. Major rejection criteria were Chips, Cracks and Glassivation faults. Lot "A" yield, on the other hand, was at a normal level. Die inked during wafer probe testing was also removed at this step.

4.3.5 Die Attach

A eutectic manual die attach process was used. The package cavity was heated on a specially designed block and a gold-silicon preform placed over the cavity. The operator then picks up the die with tweezers. (This operation is prone to induce visual rejects; see Fig. 4-2

It is then oriented in the proper direction and placed over the solder compound with a scrubbing action in both the X and Y directions. The gold-silicon preform is classified as a hard solder,¹⁶ meaning it has high flow

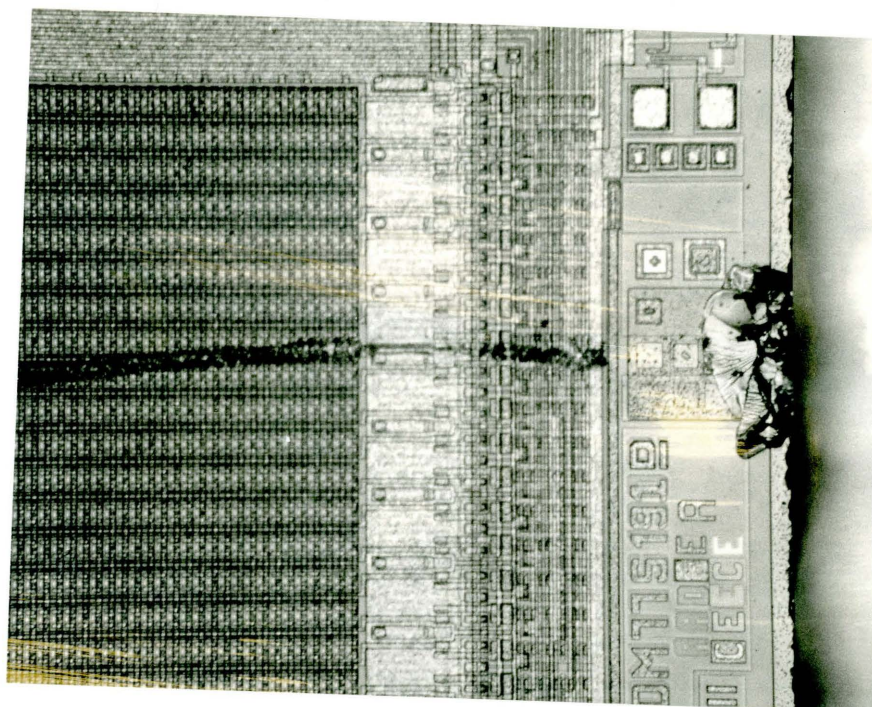


Figure 4-2
Tweezer Induced Chip-Out and Scratch

stress, therefore, it offers excellent fatigue and creep resistance. On the other hand the disadvantage of using hard solders is their lack of plastic flow, which leads to high stresses in the silicon chip due to thermal expansion mismatch. The main reliability issues raised by the die attach operation are: Disbonding and Die cracking.

Common causes for chip disbonding are¹⁶: Solder and/or die backside oxidation; non-bonding impurities on the solder surface; formation of brittle intermetallic phases, substrate metallization adhesion failure; solder fatigue or creep rupture, insufficient amount of adhesive or solder, and finally, extensive voiding under the die.

Die cracking (see Figure 4-3) is more prone to occur on larger die. It is a more serious reliability threat as the crack propagation may be delayed and go undetected by subsequent screens.

Observed cracks are vertical and horizontal. The occurrence of horizontal cracks has been attributed¹⁷ to the high shear stresses near the die edges when bonded to a substrate with a higher thermal expansion coefficient than silicon. Vertical fracture propagation from the die backside requires a tensile stress field to be present in silicon near the microcrack. The presence of voids in the die bond region also accentuates vertical cracks.¹⁸

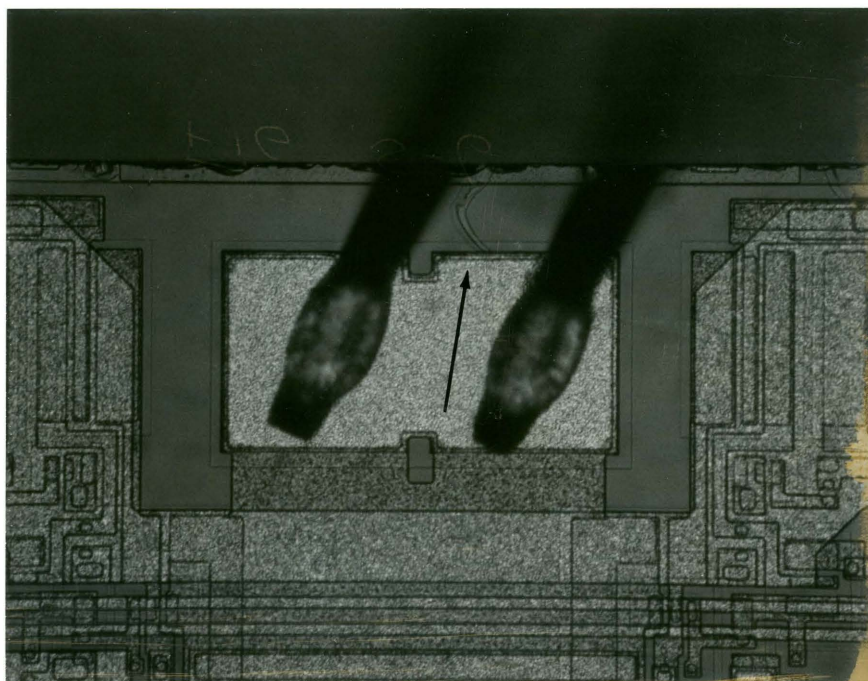


Figure 4-3
Die Cracking

4.3.6 Lead Bond

The Lead Bond or Wire Bond system used for our evaluation lot was an ultrasonic wire bond with temperature assist; 1.25 mils aluminum wire was used. The major bonding defects are: Lack of wire bond sticking, sagging wires, off-center bonds, excessively long tails, and stressed loops. Most of these are detected as opens, shorts, or higher ohmic resistance paths during electrical test after environmental stressing of the units.

In order to test the strength of the die attach a bond pull test was performed, per method 2011 of MIL-STD-883, on a sample of 10 devices, all of which passed the 3 gram-force minimum limit prescribed for 1.25 mil aluminum wire.

4.3.7 Second Visual Inspection

This inspection was also performed per method 5004 of MIL-STD-883 for all lots except "B-1". It provided a second gate for escapes to the first visual inspection. It also pointed out defects in the die attach, such as chip disbonding and die cracking or defects in the wire bonding, length of tail (see Figure 4-4) sticking of wire bonds, sagging or stressing of wires and placement of the bonds.

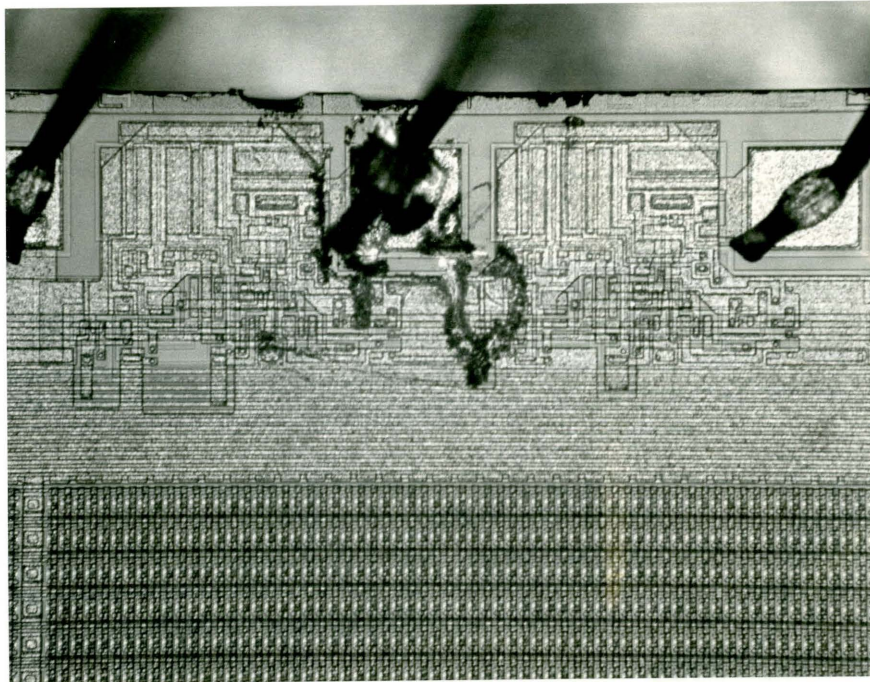


Figure 4-4
Wire Bond Reject

4.3.8 Seal

The units were assembled in a standard 24 pin "J" ceramic package, which employs a glass frit seal through which the lead frame passes. This operation provides a hermetic seal with a low internal cavity moisture content, and will protect the die itself from harsh environmental conditions.

Even though no package-sealing related difficulties were encountered on our evaluation lot, reports¹⁹ reviewing package related failure mode data were obtained from RADC (Rome Air Development Center) government/industry alerts. Life test results clearly showed that lack/loss of hermeticity was the major packaging system failure mode. Among the most common manufacturing/design problems in this area the following can be cited: cleanliness of seal surface and control of sealing temperature profiles, excess sealing glass over lead frame bonds, misaligned lids, leads and bases, cracked lead seals and exposure of lead base metal due to lead forming/flexing, and finally, blow holes in the sealing glass.

4.3.9 Bake

High temperature storage was performed with no bias voltages applied to devices in conformance with method 1008.2 of MIL-STD-883, condition C for a total of 6 hours at an ambient temperature of 175 degrees C.

4.3.10 Temperature Cycling

In order to accelerate the propagation of cracks and/or other package related detrimental effects the standard number of ten cycles was increased to fifty. Each cycle was from -65 to +150 degrees centigrade.

4.3.11 Centrifuge

In this test the devices were subjected, for a total duration of one minute, to a constant acceleration of 30,000 g. along the Y1 axis which is defined as the one in which the element tends to be removed from its mount.

4.3.12 Trim

This operation removed the shorting bars that were used as mechanical and electrical protection for the devices during all the handling involved in all operations performed up to this point. Leads were cleaned to remove oxide or other contaminants that may cause poor electrical contacts for the subsequent electrical screens.

4.4 Electrical Tests (Lot "A")

The sequence of electrical tests performed is given in Table 4-2, indicating quantities into each step and the amount of rejects, as well as the program used.

A 25 C test was the first electrical screen given to the lot. All electrical parameters were tested to the

ELECTRICAL TEST					
STEP #	OPERATION	PROGRAM	QTY IN	QTY OUT	REJ. QTY.
1	+25 C. Test	A/S	119	93	26
	Mark and Serialize				
2	+25 C. Test	A/S	119	92	27
	Burn-In 160 hours @ +127 C.				
3	+25 C. Test	S/S	92	92	0
4	+125 C. Test	S/S	92	92	0
5	-55 C. Test	S/S	92	92	0
	Burn-In 504 hours @ +153 C.				
6	+25 C. Test	S/S	92	92	0
	Burn-In 168 hours @ +153 C.				
7	Room Temp. Test	A/S	92	91	1
	Burn-In 168 hours @ +153 C.				
8	Room Temp. Test	A/S	91	91	0
	Burn-In 168 hours @ +153 C.				
9	+25 C. Test	A/S	91	91	0
	Programmability				
10	+25 C Test	S/S	91	90	1

S/S denotes MIL-M-38510/210 (Slash Sheet, see Table A-2)

A/S denotes Alternate Screen Electricals (see Table 3-3)

TABLE 4-2
(LOT "A" ELECTRICAL TESTING)

slash sheet limits and requirements (MIL-M-38510/210). Additional tests for visual inspection alternate electrical screening were also included in the alternate screen test program, A/S test tape, as presented in Table 3-3. This was the first iteration and had some differences with the tests outlined in section 3.4, specifically in Table 3-2: the level used for the stress test for VCC was at 7.0 volts instead of 7.5 volts, the ICC3 test was performed with VCC=5.0 V, instead of 7.5 V, no units were rejected based on the 500 nA maximum limit for ICC1 and ICC4, and finally, the delta measurements were disregarded as there was no adequate thermal control in place to gather meaningful results during most of the processing of this lot. The only electrical screen in conformance with Table 3-2 was the electrical test step 9 (see Table 4-2).

A total of 119 units went into this operation. 93 devices passed all testing and 26 were rejected. These 26 rejects were split from the main lot to form subplot "A-R". A detailed analysis for these failures will be given in section 4.6. The actual readings for this and all of the other lots are presented in Appendix "B". There will also be a set of Plots of the Substrate-N Epi I/V characteristics for this sub-lot "A-R" presented in Appendix "C".

The units were marked and serialized. Passing devices were serialized 1001 to 1093. Initial failures were given serial numbers 1100 through 1125. All units were retested after serialization in electrical test step 2. All 26 initial rejects failed again. All units initially passing were good except for S/N 1081, which failed propagation delay low to high TPLH.

The initial burn-in cycle had a duration of 160 hours at an ambient temperature of +127 degrees C. All input lines were toggled at a maximum frequency of 100 KHZ. All output lines were connected via 300 ohms to VCC. The VCC pin was maintained above 5.0 volts at all times.

After the completion of the burn-in cycle, the lot was tested at +25, +125 and -55 degrees C. to the slash sheet program. As can be seen in Table 4-2, all 92 devices going into each of these tests passed.

A second burn-in operation was now performed for 504 consecutive hours at an accelerated temperature of 153 C, under the same dynamic conditions as the first burn-in. (This is equivalent to 3000 hours at 125 degree C.) Subsequent testing at 25 degree C. (Step #6) showed no rejects. This step was performed to the slash sheet screen program.

The units were once again subjected to a dynamic burn-in for 168 hours at +153 degrees C. This is a normal life test cycle, being equivalent to 1000 hours @ +125 degrees C., as it was presented for temperature acceleration by The Arrhenius Equation in section 3.2.1.

Electrical testing (step 7), to the alternate screen program, showed one failure out of the 92 units, S/N 1077, failing the 10 microamp VIC test on pin 18 (CE3) with a marginal reading of -359 milivolts on a -360 mv limit. Reviewing data for electrical test step #2, it was found that it had marginally passed with a reading of -362 mv. Although this unit was considered as a valid reject, it was kept with the lot to monitor for further degradation. Two more burn-in cycles of 168 hours at +153 degrees C and subsequent electrical testing at room temperature to the alternate screen program, showed no additional rejects.

As a final step a programmability check was performed on all of the devices. In this test 50% of all the fuses were blown in a checker-board pattern. Upon electrical verification one device S/N 1052 was determined to be a failure due to propagation delay readings of 123 ns for a maximum allowable of 100 ns. Reviewing previous data for this device it was noticed that it exhibited a much higher than average reading for ICC1 and ICC4, as can be seen in Appendix B. (results for Electrical step 9).

It should be noted that previously rejected S/N 1081 also failed this test.

4.5 Lot "A" Observations and Conclusions

The conditions and limits established in Table 3-2 were a direct result of the readings obtained from this lot. The criticality of providing a carefully controlled test temperature environment was clearly manifested in the collected test data shown in Appendix B, where the readings for ICC1, ICC2, ICC3, ICC4 and deltas are tabulated for electrical test steps 2,7,8 and 9. Steps 2 and 9 were performed forcing $+25 \pm 3$ degrees C through a handler, while steps 7 and 8 were carried out at room temperature. Comparing readings for ICC1 in all four steps, we notice a wide variation in the total averages between 311 nA to 440nA, and even for the two steps (2 and 9) performed on a handler there was a difference of 29nA. This difference can be explained by the tolerance of ± 3 degrees allowed in the handler. If we examine the standard deviation for Step 2 (259.77nA) and Step 9 (256.95nA) we see a difference of only 2.82nA which is well within the tester's margin of error. Comparing this with the standard deviations for Step 7 (285.48nA) and Step 8 (308.69nA), we become aware of the benefits of forcing temperature on the devices to be tested in order to get meaningful comparison in the low nA

range.

The delta measurement will also be very temperature sensitive, especially (as it is intended) to junction heating by the devices' internal power dissipation. This fact becomes apparent studying the ICC4 and delta readings gathered in Step 2 and Step 9. Note that ICC3 in Step 2 was at a VCC level of 5.0 volts with a pause of approximately 400 milliseconds after the removal of the stress voltage level, resulting in an average delta of 3.89nA with a standard deviation of 3.40nA. ICC3 in Step 4 was to a level of 7.5 volts with a pause of less than 40 milliseconds, yielding an average delta of 16.68nA with a standard deviation of 12.42nA, thus reflecting the increase in leakage currents due to the power dissipated at higher VCC levels. For the readings of Steps 7 and 8, ICC3 was at 5.0 volts and the pause was approximately 2 seconds. The negative average deltas indicate that the ICC4 measurement took place at a slightly lower temperature.

The effect of different pauses between measurements was also observed. Low currents were read when outputting test data to a slower peripheral such as the line printer as opposed to the readings gathered when data was sent directly to a disk drive.

4.6 Electrical Tests (Lot "A-R")

As it was mentioned in the previous section, this lot is made up from the lot "A" rejects to the first screen at +25 degrees C using the A/S program. This is indicated as Step A in Table 4-3 which follows the same format of Table 4-2. The same differences to the alternate screen conditions and limits (ICC3 @ 5.0 volts instead of 7.50 volts, etc) given in Table 3-2 apply for electrical Steps A and A', and electrical Step D is in conformance with Table 3-2.

The electrical readings for ICC1, ICC2, ICC3, ICC4, deltas and reasons for rejection are given in Appendix B. Plots of I-V characteristics for some of these devices serialized from S/N 1100 to S/N 1126 are given in Appendix C and will be discussed in section 4.7.

Electrical test Steps A' and A to the alternate screen test rejected all 26 units. Eight failed the low current VIC test (VICL). Seven failed TW/TB (test word-test bit as described in section 4.4) verification alone, seven failed TW / TB and other tests. Three failed ICC leakage and the remaining ones failed due to various other reasons. All of the 26 rejects were then tested to the slash sheet program (S/S). Ten units were found to meet all of the electrical requirements as outlined per the slash sheet. A 168 hour @ 153 C. burn-in was performed on all units and then another

ELECTRICAL TEST					
STEP	OPERATION	PROGRAM	QTY IN	QTY OUT	REJ. QTY.
A'	+25 C. Test	A/S	26	0	26
A	Room Temp. Test	A/S	26	0	26
B	Room Temp. Test	S/S	26	10	16
	Burn-In 168 hours @ +153 C.				
C	Room Temp. Test	S/S	26	10	16
D	+25 C. Test	A/S	26	0	26
	Programmability				
E	+25 C. Test	S/S	26	10	16

TABLE 4-3
(LOT "A-R")

test, electrical test Step C, at room temperature to the slash sheet program was done, obtaining the same results of 10 passing and 16 rejected. All 26 units were once again rejected to the alternate screen test tape in Step D.

The units were submitted to a programmability test in which a checker-board pattern was attempted to be stored in the PROMS. Testing to slash sheet conditions, electrical test Step E indicated that 10 of the 26 units had been successfully programmed.

4.7 Lot "A-R" Observations and Conclusions

Although the same total of 10 devices passed the slash sheet program and the programmability test, upon closer examination it was established that it was not the same 10 units. Three of the devices passing electrical test Steps B and C, failed the programmability test and three of the units failing gross functional testing in steps B and C, passed the programmability test.

Comparing the failing criteria listed in Appendix B with the I-V characteristics given in Appendix C, we observe that all of the devices failing VICL: S/N 1100 through S/N 1107, also exhibited higher than average ICC1 and ICC4 readings. These readings are closely matched with the marker values in the plots which correspond to the same 0.3 volt point.

The units failing TW/TB verification did not exhibit the same definite trend; S/N's 1108, 1110, 1111, 1114 and 1115 had ICC1/ICC4 readings that were well within the average range obtained for the good units in lot "A", S/N's 1109 and 1112 did show high ICC1/ICC4 readings.

S/N's 1121, 1122 and 1123 did not exhibit a diode but a resistive characteristic indicating a substrate diode anomaly. Both S/N's 1122 and 1123 did pass all of the slash sheet electricals. S/N 1113 also presented an early resistive characteristic, as well as failing VOH, IOS and

TW/TB tests.

The predominant failure mode was test-word/test bit (TW/TB). This test exercises all of the control portions of the die to be sure the proper bits can be selected, accessed and read.

4.8 Electrical Tests (LOT "B")

The sequence of electrical testing for lot B-1 is given in Table 4-4. There were 3 devices rejected on the first electrical screen to the A/S program, two failing the delta of ICC4-ICC1. These two devices correspond to S/N's 26 and 49 on the readings presented in Appendix B. The other failure corresponds to S/N 11 which exceeded the 600 nA maximum ICC1 and ICC4 limit. There were only two more failures at the -55 C. electrical test. For this lot the burn-in cycles were only two for 168 and 184 hours at a temperature of +150 degrees C. After the second burn-in cycle, the devices were subjected to a programmability test in which 50% of the fuses were blown and then all the electrical parameters outlined in the slash sheet were tested.

The initial 3 rejects plus the 2 failing the cold electrical test were also burned-in for 184 hours @ +150 C and all 5 passed the programmability verification to the S/S program at +25 C.

The sequence of electrical testing for lot B-2 is given in Tables 4-5 and 4-6. This lot was separated into subplot B-2-P for those devices that passed the alternate screen program @ +25 C (Table 4-5) and subplot B-2-R for the ones failing to the A/S tape (Table 4-6). An initial quantity of 176 units was tested @ +25C to the A/S program.

ELECTRICAL TEST					
STEP	OPERATION	PROGRAM	QTY IN	QTY OUT	REJ. QTY.
1	+25 C. Test	A/S	52	49	3
	Mark and Serialize				
	Burn-In 168 hours @ +153 C.				
2	+25 C. Test	S/S	49	49	0
3	+125 C. Test	S/S	49	49	0
4	-55 C. Test	S/S	49	47	2
	Burn-In 184 hours @ +153 C.				
	Programmability				
5	+25 C Test	S/S	47	47	0

TABLE 4-4

(LOT "B-1" ELECTRICAL TESTING)

ELECTRICAL TEST					
STEP	OPERATION	PROGRAM	QTY IN	QTY OUT	REJ. QTY.
1	+25 C. Test	A/S	176	72	104
	Mark and Serialize				
	Burn-In 168 hours @ +153 C.				
2	+25 C. Test	S/S	72	70	2
3	+125 C. Test	S/S	70	70	0
4	-55 C. Test	S/S	70	65	5
	Burn-In 184 hours @ +153 C.				
	Programmability				
5	+25 C Test	S/S	65	65	0

TABLE 4-5

(LOT "B-2-P" ELECTRICAL TESTING)

ELECTRICAL TEST					
STEP	OPERATION	PROGRAM	QTY IN	QTY OUT	REJ. QTY.
1	+25 C. Test	A/S	176	72	104
	Mark and Serialize				
	Burn-In 168 hours @ +153 C.				
2	+25 C. Test	S/S	104	72	32
3	+125 C. Test	S/S	72	72	0
4	-55 C. Test	S/S	72	51	21
	Burn-In 184 hours @ +153 C.				
	Programmability				
5	+25 C Test	S/S	51	44	7

TABLE 4-6

(LOT "B-2-R" ELECTRICAL TESTING)

72 units passed and their readings are labeled from S/N 1 to S/N 72 on the print out for lot B-2 in Appendix B. 104 devices were rejected and are labeled S/N 200 to S/N 303.

Sublot B-2-P lost: 2 units following the first burn-in, none at +125 C test, 5 at -55 C test and none after the second burn-in operation programmability check. Sublot B-2-R lost: 32 units following the first burn-in, none at +125 C test, 21 at -55 C test and seven (S/N's 204, 217, 220, 23, 270, 280 and 295) following the second burn-in operation programmability check.

4.9 Lot "B" Observations and Conclusions

There is a great contrast in the number of initial rejects on the first screen to the A/S program for lots B-1 (3 out of 52) and B-2 (104 out of 176).

There is a strong indication that the visual inspection to the full method 2010 requirements was highly effective in removing defective devices prior to the first electrical test for the B-1 lot. There is also a good indication about the reliability of the units from this lot in the fact that they all passed the programmability testing after the second burn-in operation, which was the equivalent of 1000 hours of burn-in at +125 C. That constitutes a life test for 883 class B devices.

The fact that all 3 devices failing the alternate

screen test passed the programmability test is not indicative of inability of the A/S program to point out potentially lower reliability devices as this is not a reasonable statistical sample.

Lot B-2 had a very high initial rejection rate, some of which can be attributed to the fact that this lot had a minimum visual inspection to the lowest magnification allowable of 30x. It needs to be pointed out that during this visual, a large number of cracks and chipped devices were observed. This indicates that there were problems during the saw operation. (This problem was also observed on Lot B-1 visuals.) On the other hand this high rejection ratio gives a favorable indication of the A/S program's ability to detect defects that would have been visually rejectable.

The fact that there were no rejects after the final programmability test for subplot B-2-P and there were 7 programmability rejects on subplot B-2-R gives a good indication of the alternate screen program's effectiveness for weeding out defects in the fuse array area.

Throughout this evaluation there was no clear indication of any correlation between the devices failing the delta of ICC4-ICC1 to visual defects.

There was correlation between higher ICC1 and ICC4 readings and programmability rejects observed on subplot

B-2-R's readings in Appendix B for S/N's 204, 217, 243 and 280. S/N's 220 and 225 also failed programmability but did not fail ICC1/ICC4.

Higher readings of ICC1/ICC4 are not always indicative of rejection, as evidenced by S/N 248 which passed all the testing steps.

CHAPTER 5

CONCLUSIONS

An electrical test sequence was designed to replace the high-magnification visual inspection required by MIL-S-883C. Two separate lots were assembled and subjected to the alternate screen flow. Lot A was used to determine the parametric limits for the alternate electrical tests, and also subjected to an extended life test that gave a positive indication of the reliability of this approach. Lot B was used to demonstrate the effectiveness of the specific test sequence (including the limits obtained from Lot A) when compared to high magnification visual screening.

The fact that the units from Lot "A" (which was visually inspected to the low magnification requirements) that passed the alternate electrical screen test exhibited a very low failure rate after completing several extensive accelerated burn-in steps, is indicative of the long term reliability achieved with the proposed alternate screen method. It is very interesting to observe that the one device failing the programmability test after all the burn-in operations (S/N 1052) would have been rejected by the ICC1/ICC4 maximum limit of 600nA that was used on Lot B.

The Higher Initial Rejection Rate of Lot "B-2" when compared to that of Lot "B-1" is indicative of the ability

of the A/S test program to detect devices that would have been rejected by the High Magnification Visuals. These lots (B-1, B-2) also provided a strong indication of the ability of the A/S program to detect programmability rejects. There was no practical evidence that the Delta of ICC4-ICC1 was capable of detecting visually rejectable or lower reliability devices. The results of this test were not conclusive and would need further characterization on a larger sample.

This evaluation has provided encouraging results for the alternate screen as a viable alternative to the high magnification visual inspection. Although we can not unequivocally state that all of the devices passing the electrical alternate screen would pass the High Magnification Visual Criteria, we can state that all of the devices processed to the A/S program in our evaluation did pass the Extended Life Test.

The visual requirements of method 5004 of MIL-STD-883C proved to be an adequate alternative to the high magnification. This method can, however, be improved in its approach to the selection of appropriate electrical alternate tests. These cannot be proposed in a generalized manner. They must be specifically selected for each device type based upon its electrical circuit implementation and fabrication process.

APPENDIX A

16K BIPOLAR PROM OVERVIEW AND TEST PLAN IMPLEMENTATION

A.1 Scope

This appendix will present the implementation of the electrical testing requirements as outlined by a specific "slash sheet" specification, MIL-M-38510/210, for a 16.384 Bit Schottky, Bipolar, Programmable Read Only Memory (PROM). This discussion will not be limited to a brief description of the parameters tested but will focus on the development and intention of a specific testing plan, and its actual implementation.

It is for this reason that a more in-depth familiarization with the devices to be tested from both the fabrication process and actual circuit implementation standpoint are necessary, and will be presented in section A.2 and A.3 respectively. A description of purpose and the methodology of performed electrical tests will be given in section A.4.

A.2 Qualitative Overview of the Fabrication Process²⁰

The intent of this section is not to provide an actual detailed fabrication process for a particular bipolar PROM but to provide a generalized qualitative description of the process with typical rather than actual dimensions. It is given for the purpose of providing some insight as to how electrical parameters can be affected by small variations in the wafer fabrication process. Five inch P-type silicon wafers were used as the starting material,

allowing the use of an N type EPI which was used to form vertical NPN and lateral PNP transistors.

<111> material was used to maximize final surface charge QSS providing high thresholds against parasitic MOS action.

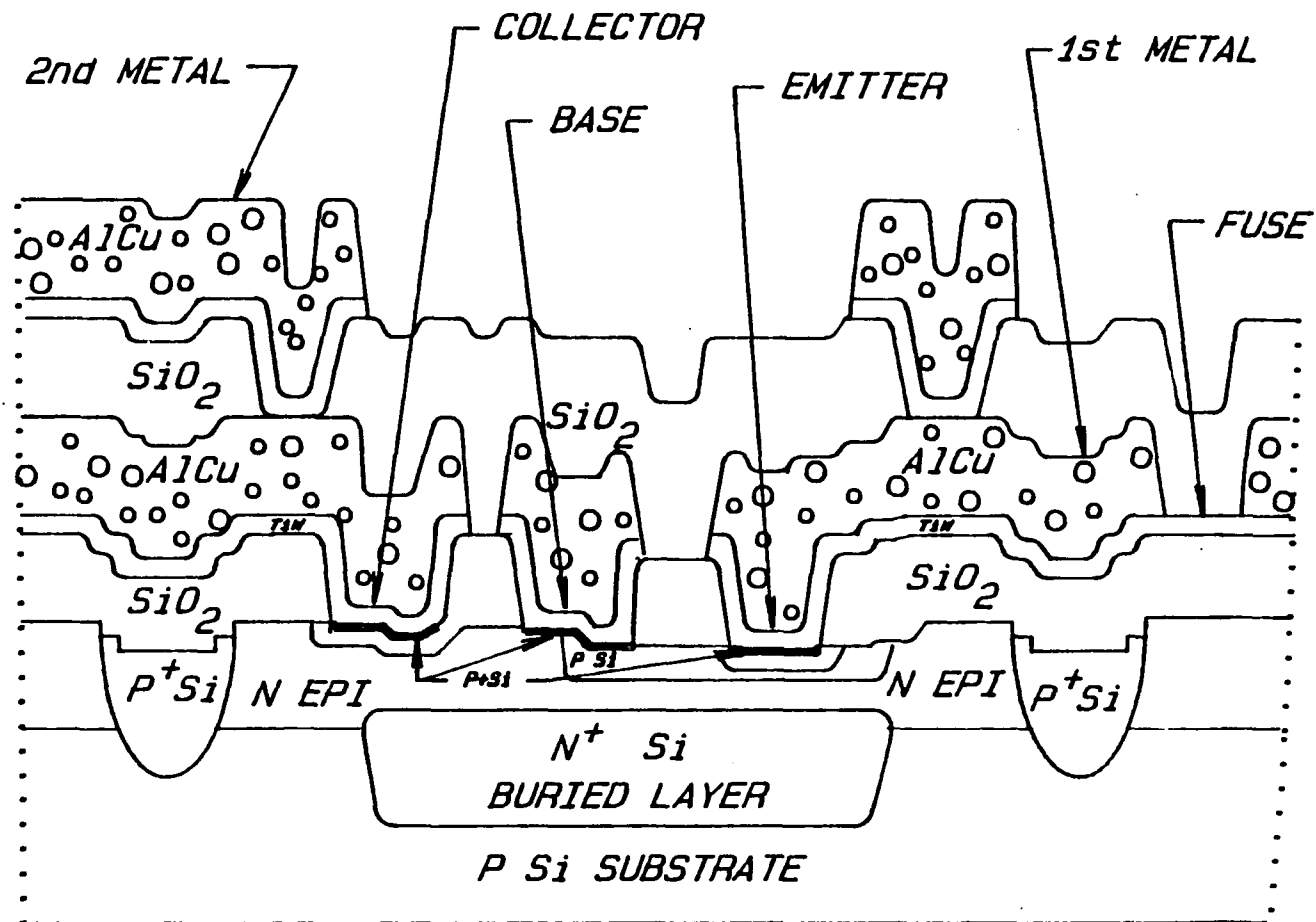
A typical fabrication sequence is given in Table A.1. Each of the individual steps is described thereafter. A cross-section of a single structure fabricated with this process is presented in Figure A-1.

Initial Oxidation
Buried Layer Mask
Buried Layer Diffusion
EPI Pre-Clean
EPI Growth
Re-Oxidation
Isolation Mask
Isolation Pre-Deposition / Diffusion
Base Mask
Base Pre-Deposition / Diffusion
Nitride Deposition and Nitox
Emitter Mask
Emitter Diffusion
Contact Mask
Platinum Silicide
TiW Sputter and AlCu Evaporation
First Layer Metal
Fuse Mask
Dielectric Vapox Deposition
Via Mask
Second Layer TiW and Al Depositions
Second Layer Metal Mask
Vapox Deposition
Pad Mask

TABLE A-1
Dual Metal Bipolar Schottky Fabrication Sequence

Single Transistor and Fuse
Silicon Implementation

Figure 4-1



A.2.1 Oxidation

A uniform 12,000 to 14,000 Angstrom Layer of oxide (SiO_2) is grown over the entire surface of the wafer with the purpose of masking the diffusion of impurities over selected areas during the next step. A thermal oxidation process is performed in which the wafers are inserted into a diffusion furnace @ 1100 C. Hydrogen (H_2) and Oxygen (O_2) are burned at one end of the furnace to form steam. The silicon removes oxygen from the steam and forms silicon dioxide (SiO_2) in a very predictable manner. It should be pointed out that approximately 44% of the thickness of the grown layer used to be silicon. Prior to this oxidation step the wafers have been through clean operations to remove organic contaminants as well as water soluble inorganics.

A.2.2 Buried Layer Mask

This mask will be used to create openings through the silicon dioxide layer at the specific locations where transistors are to be fabricated, exposing the P-Type substrate for the next step.

A.2.3 Buried Layer Diffusion

An N type dopant is diffused through the openings created by the buried layer mask and will over-compensate the original P-Type material into N-Type. The purpose of

this step is to reduce the series collector resistance.

A.2.4 EPI Pre-Clean

The wafers are cleaned in order to remove particles and oxide for the growth of an epitaxial layer.

A.2.5 EPI Growth

A new layer of N-Type silicon is grown over the complete surface of the wafer to form a continuous crystal structure by means of an epitaxial deposition. All of the devices that will be fabricated will be physically located on this layer rather than the substrate itself.

A.2.6 Re-Oxidation

A new layer of oxide will be grown over the entire surface of the wafer to be used as a mask against impurity diffusion.

A.2.7 Isolation Mask

This mask will selectively open channels that will allow the P⁺ISO to reach down to the substrate, thus isolating the various components fabricated in each of these N-Type islands with a reverse biased diode when appropriate bias is applied.

A.2.8 Isolation Pre-Deposition/Diffusion

This operation puts B₂O₃ glass down on the surface. Some boron diffuses into silicon in areas opened by the

isolation mask. Excess B_2O_3 is dipped off in HF and the pre-deposited impurities are driven down long enough to reach the substrate, at which point a distributed P-N diode is formed surrounding each tub.

A.2.9 Base Mask

This mask will be used to remove the oxide in the base regions so that boron may be diffused to convert them into P-Type silicon. In this step all the resistors are also defined. The PNP base widths are determined and the NPN transistor bases are put into place.

A.2.10 Base Pre-Deposition/Diffusion

B_2O_3 glass is put on the surface again in a very well controlled pre-Deposition to get the right amount of doping. This dose will not only control resistor values but will also be important for BV_{EBO} or ZENER Diode Voltage. For the same reasons the diffusion step must also be well controlled.

A.2.11 Nitride Deposition and Nitox

The purpose of this step is to deposit a very dense, uniform layer of silicon nitride on the wafers. The Si_3N_4 will be used as a mask to prevent diffusion of phosphorus into any region other than the emitter and N^+ collector contacts. The nitox, or SiO_2 converted from Si_3N_4 is used to improve resist adhesion for the emitter mask.

A.2.12 Emitter Mask

Emitter areas will be opened by removing the nitride from all emitter areas. It will also create openings for the collector N^+ area. The base oxide under the nitride will not be disturbed at this step, whereas the oxide under nitride for collector contacts and emitters will be completely removed.

A.2.13 Emitter Diffusion

During this step phosphorus is diffused into the exposed silicon in the emitter and N^+ collector areas. This is a critical diffusion step, as the emitter must be driven into the base just the right amount. Insufficient drive in will result in low betas. Excessive drive-in will result in low breakdown voltages.

A.2.14 Contact Mask

This mask will selectively remove the oxide from the base, emitter and N^+ collector contact areas, as well as any other regions where electrical contacts may be required. It also removes the nitride that was used to mask the contacts.

A.2.15 Platinum Silicide

This step will be used to form a very thin layer of platinum and silicon alloy, PtSi, in all the contact regions of the transistors, resistors and diodes. The

formation of this layer will improve the ohmic contact of the first layer of metal (Ti-W) that will be deposited in the next step. But the primary reason for the PtSi layer is to place a Schottky Clamp Diode on the base-collector junction by making the base contact overlap the N-type collector region, forming in this, manner the Schottky Transistors required to achieve high speed operation.

One more benefit from the platinum silicide layer is to prevent the alloying of silicon and aluminum creating spikes that could lead to potential shorts. (Even though the Ti-W layer is used for this purpose, due to its low thickness, pin-holes are quite common.)

A.2.16 Ti-W Sputter and AlCu Evaporation

During this operation uniform layers of titanium tungsten alloy (TiW) and aluminum-copper alloy (AlCu) are deposited over the wafer surface.

The TiW layer which is evaporated first will form the fuses for the programmability of the PROMS. It will also present a barrier between the Al-Cu and the silicon to prevent potential shorts. The Al-Cu layer is used to provide connections between the desired circuit elements. The TiW layer is 650 angstroms and the AlCu is 6000 angstroms thick. The second layer thickness is 18,000 angstroms, so this layer can therefore have a much higher current density.

A.2.17 First Layer Metal

The first layer of metal deposited in the previous step is selectively removed to leave only those connections that are desired.

A.2.18 Fuse Mask

This mask will selectively remove the TiW in between the aluminum copper interconnections leaving only small links between certain interconnects. These links constitute the fuses.

A.2.19 Dielectric Vapox Deposition

At this point, an insulating layer of SiO_2 is placed to serve as an insulator between the already deposited first layer of metal and the second layer of metal that will be deposited next. This layer of SiO_2 is phosphorus doped to prevent it from cracking during large changes in wafer temperature.

A.2.20 Via Mask

This mask will provide small openings called vias in the dielectric vapox layer through which metal can be deposited to form electrical contacts between the first and second layer metals.

A.2.21 Second Layer TiW and Al Depositions

New metal layers will be deposited to form the second

layer of electrical interconnects. TiW is used to improve ohmic contact between layers and to improve the coverage of metal over the steps created in the interlayer dielectric. Typical thickness is 18,000 angstroms.

A.2.22 Second Layer Metal Mask

This mask is used to selectively remove all the unwanted metal (TiW and AlCu) leaving the second level interconnect pattern defined to connect circuit elements as required.

A.2.23 Vapox Deposition

This layer of SiO_2 is once again phosphorus doped to prevent cracking. This is a low temperature layer deposited by chemical vapor deposition (CVD). The sealing of the wafer in SiO_2 will prevent any foreign contaminants from diffusing or disturbing the fabricated circuitry. It will also provide some scratch protection for the softer metal interconnects during subsequent testing and assembly operations.

A.2.24 Pad Mask

This mask is used to selectively remove the vapox layer over the bonding pads so that wires may be used to connect the fabricated die to the package leads.

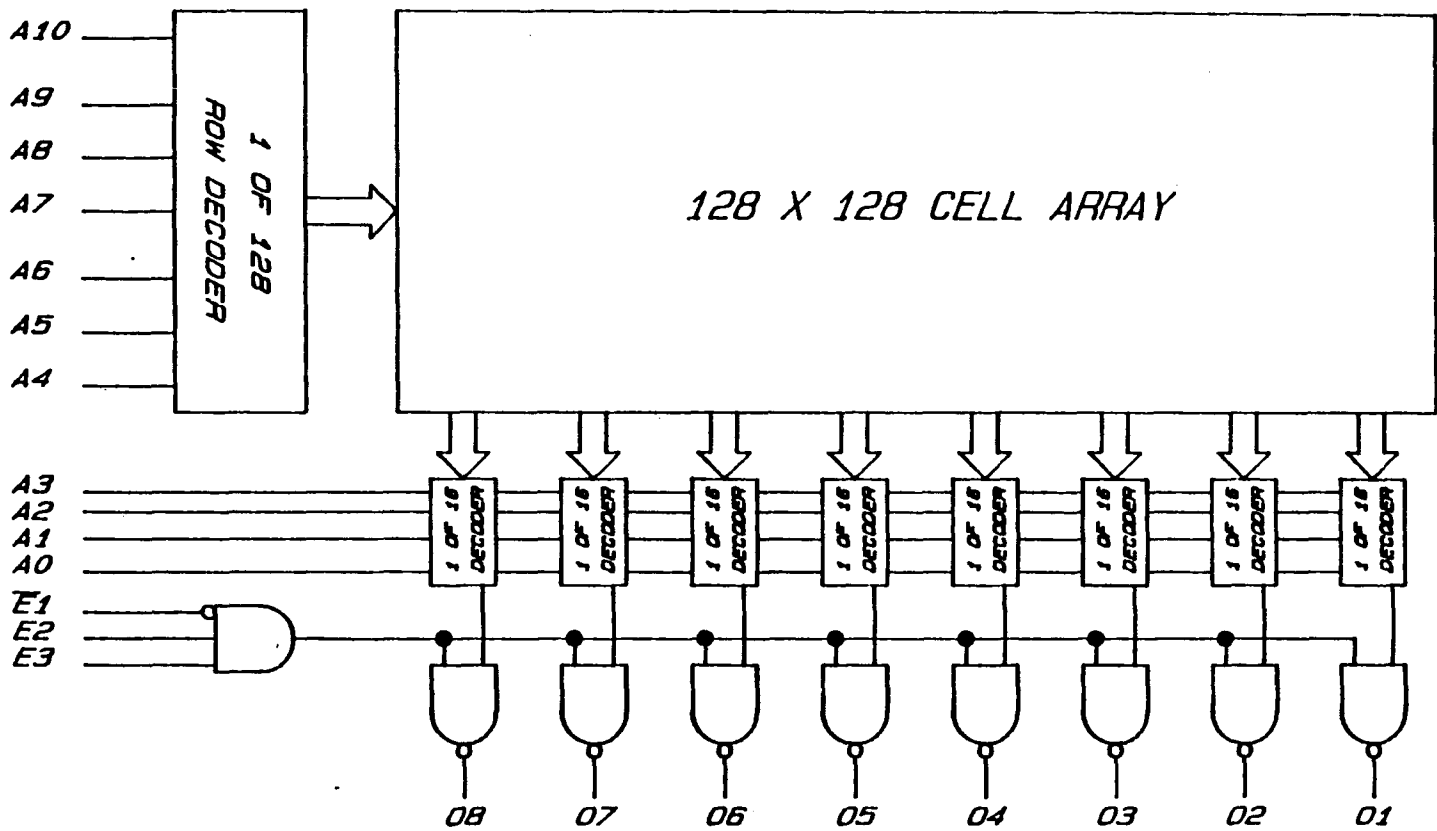


Figure 4-2

Logic Block Diagram

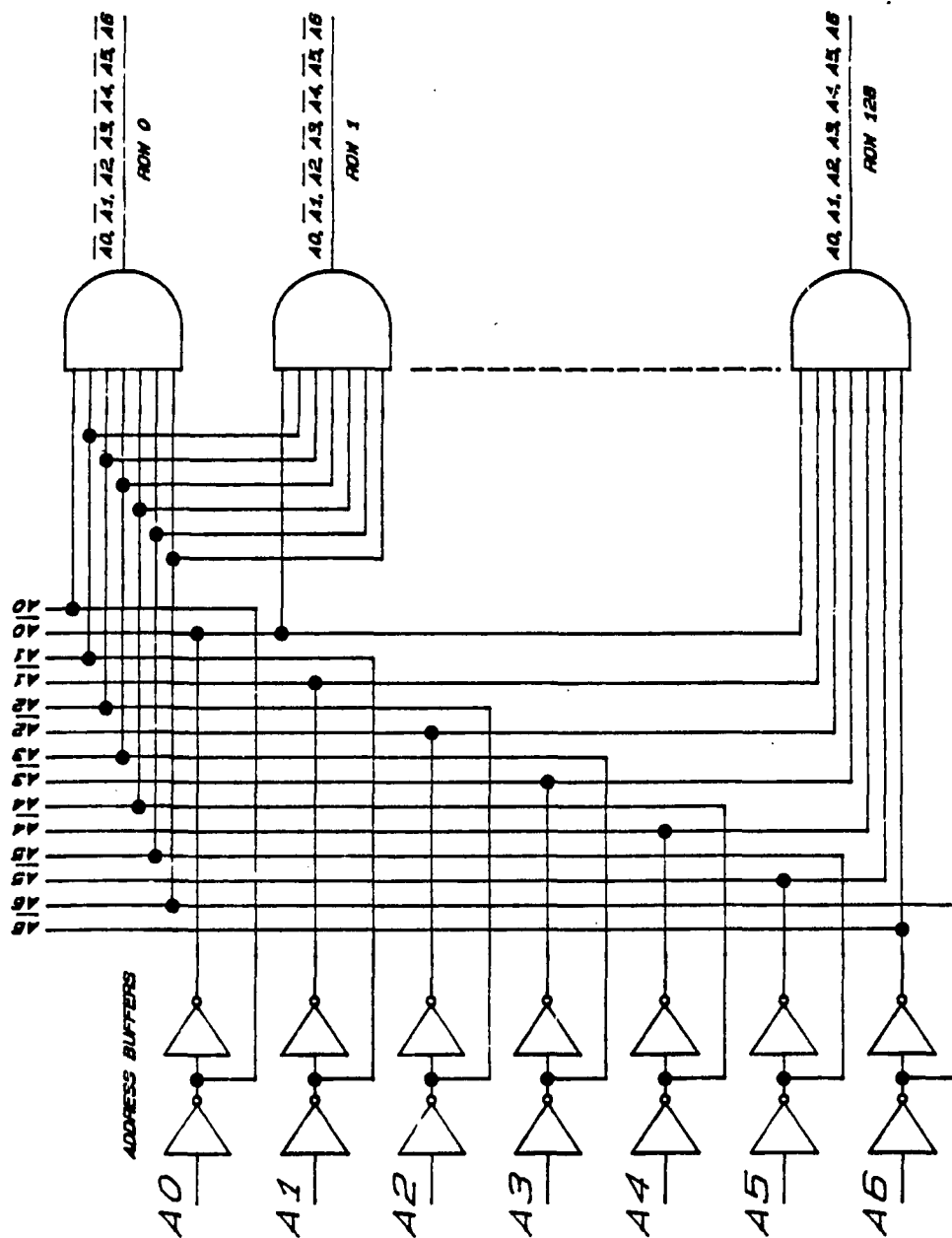
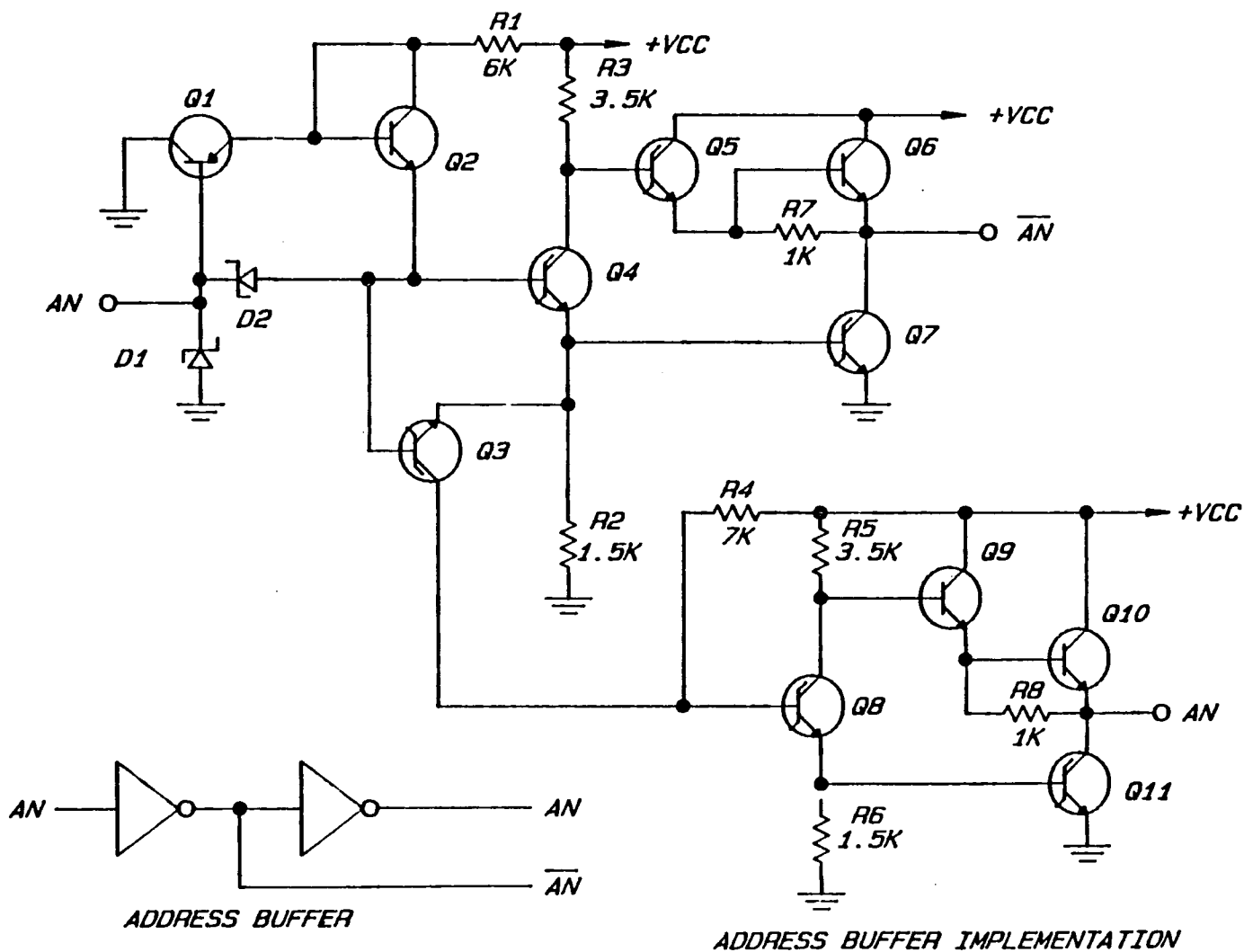


Figure 4-3
Row Decoder

Address Buffer Implementation

Figure 4-4



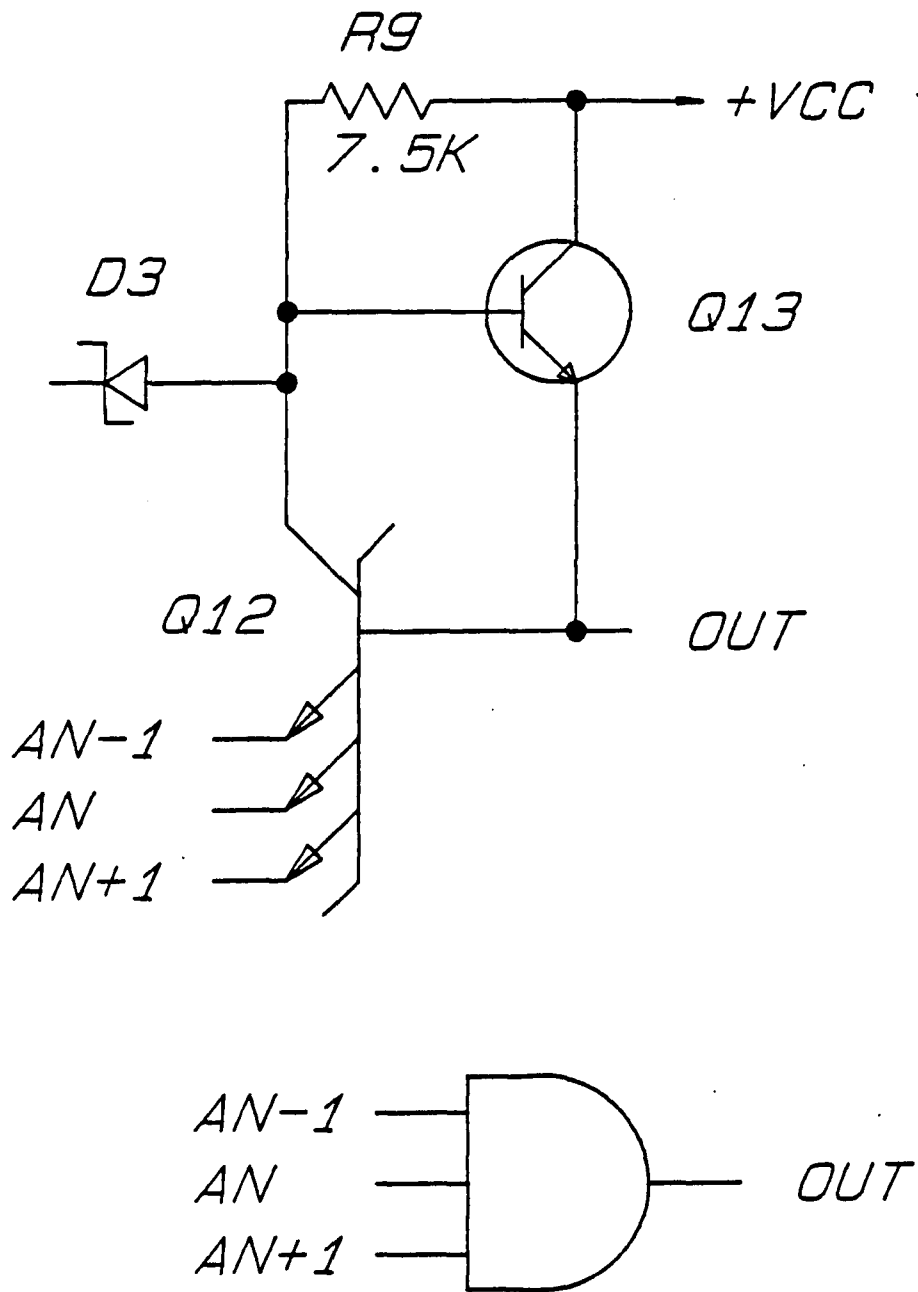
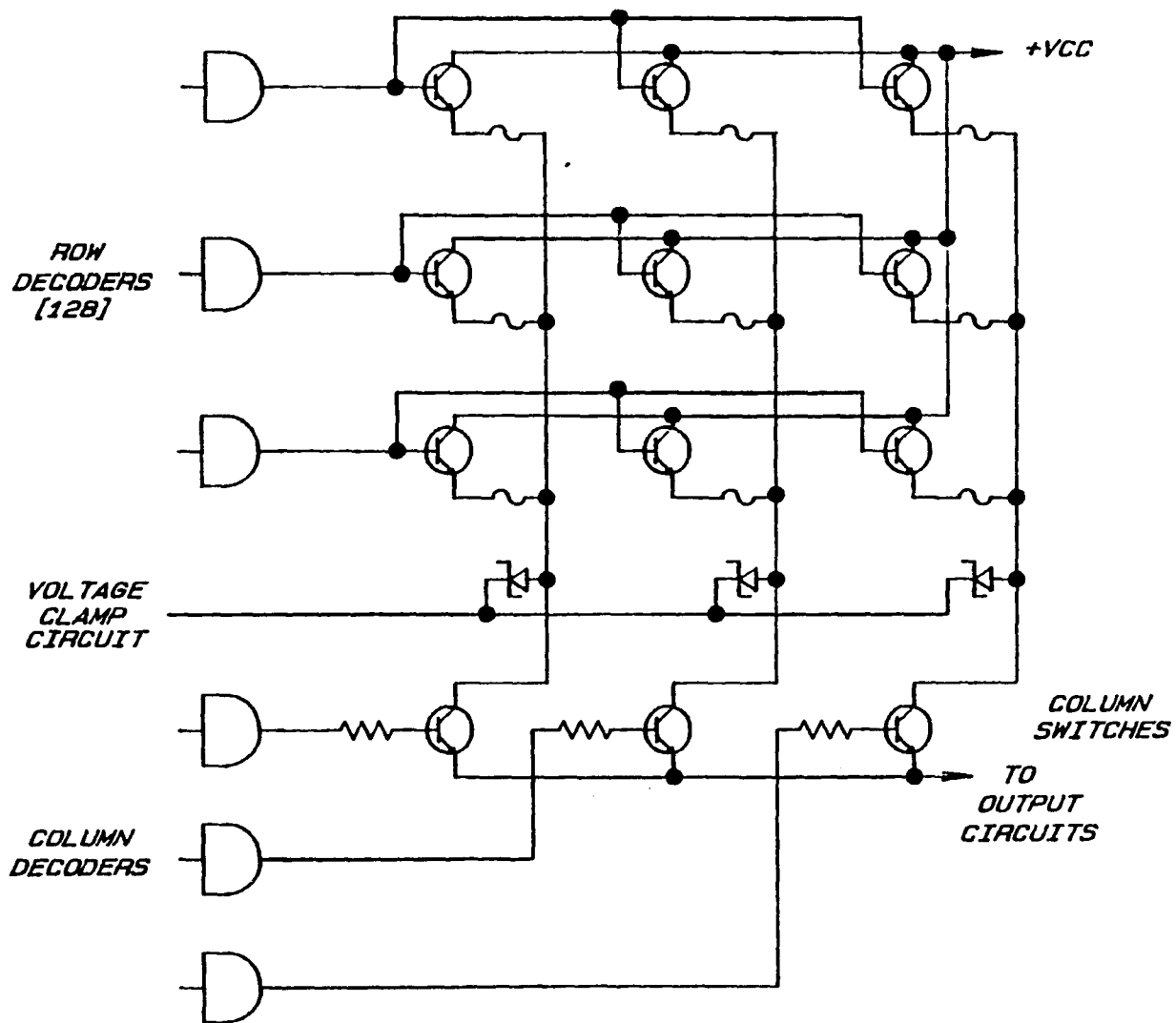


Figure 4-5
"AND" Gate Implementation

Cell Array Circuit

Figure 4-6



A.3 Actual Circuit Implementation

A typical circuit implementation will be given in this section. Although it does not provide the actual component values it conceptually reflects the particular structures used for the development of the electrical Alternate Screen, as well as the standard electrical test sequence.

A.3.1 Logic Block Diagram

Figure A-2 depicts a logic block diagram for a 16K bit Programmable Read Only Memory (PROM). The actual array is arranged in a 128 row by 128 column matrix. The 128 rows are accessed via the most significant bits of the address lines A4 through A10. This device has 8 output pins which are driven by a 1 of 16 decoder selected by the least significant four bits of the address lines A0 through A3, providing in this fashion the 128 columns that complete the programmable array.

A.3.2 Row Decoder (Figure A-3)

The row decoder circuitry will not only provide the selection to a particular row in the memory array. It also serves as an interface between signals external to the device and the internal circuitry, through the address buffers. The schematic for one of these address buffers is presented in figure A-4. A PNP input is provided to reduce the IIL loading, thus allowing an increased FAN-IN. The

actual IIL value will be given by the expression $IIL = [VCC - (VIL + VBE1)] / (R1 * B1)$, which when replaced with typical values yields, $IIL = [5 - (0.9 + 0.8)] / (6K * 50)$, therefore our typical IIL is -11 uA. Note that this value is given as a negative value to be consistent with the notation expressing currents as negative when leaving device pins.

The maximum input voltage that can be applied to the input of the address buffer and still provide a logic high at the output (AN bar) is given by the sum of the base emitter voltages of transistors Q7 and Q4 at the edge of conduction EOC (typically 0.7v) minus the voltage drop of diode D2. This voltage is defined as VIL, thus $VIL = VBE7 (EOC) + VBE4 (EOC) - VD2$, which would be $VIL = 0.7 + 0.7 - 0.5 = 0.9v$ for typical values.

VIH will be defined in turn as the minimum input level necessary at the input to provide a logic low level at the AN bar output. From figure A-4, this value would be given by $VIH = VBE7 + VBE4 - VD2$. In this case the base emitter voltage to be used is the ON value rather than the edge of conduction one (0.8v), $VIH = 0.8 + 0.8 - 0.5 = 1.1v$ typically.

The output high voltage VOH is given by $VOH = VCC - VBE5 - VBE6$. For typical values $VOH = 5 - 0.8 - 0.8 = 3.4v$; note that the voltage drop across the 3.5K resistor is neglected as its current is divided by the product of the betas of Q5 and

Q6. VOL is given by the voltage developed across the collector to the emitter of transistor Q7 when it is in the ON state. Note that this is a Schottky Clamped Transistor and its VCE is given by the base emitter minus the Schottky Diode voltage, typically $VCE = 0.8 - 0.5 = 0.3$ volts; therefore the typical $VOL = 0.3v$.

A.3.3 AND Gate Implementation (Figure A-5)

For this illustration, a three input AND gate was selected. The input levels will be the VOH and VOL levels previously obtained for the address buffer circuit. If any of the input lines to the AND gate are low, then Q12 will be ON and Q13 OFF. The output level will be given by $VOL = VIL + VBE12$. This is $VOL = 0.3 + 0.8 = 1.1v$ for the typical case. When all of the input lines of the AND gate are at a logic high voltage, then transistor Q12 will be off and Q13 will start having base drive; for this case $VOH = VCC - VCE13$, typically $VOH = 5 - 1.8 = 3.2v$.

A.3.4 Cell Array Circuit (Figure A-6)

The outputs of the AND's from the row decoders are fed to the bases of all the transistors in the selected row. These transistors have the memory cell fuses in series with their emitters, which in turn feed the collectors of the transistors driven by the column decoders. For a particular input-address combination only the fuse at the

intersection of the selected row and column will be providing the appropriate level to the output circuit depending on whether the fuse has been blown or not.

In addition to the main cell array, there are some extra rows and columns of fuses provided on every device. These locations are included to provide PROM testability, and are referred to as Test Word Test Bit (TW/TB).

Since there are no extra pins to address the additional location, these must be accessed using some of the existing row/column address pins, connecting them to the test row/column selection circuitry via a Zener diode with BV greater than 8 volts. If a voltage above this level is presented to the input, the main array is disabled and the extra test row/column portion is enabled.

A.3.5 Output Circuit Implementation (Figure A-7)

On the output circuit, Q9 combines with Q11 to form a cascaded emitter-follower, which is able to drive more source current into the load when the output goes to the high state. This active pull-up helps reduce the transition time TPLH. The turn-on voltage for transistor Q9 is raised by the base-emitter voltage of transistor Q11 to avoid the possibility of transistor Q11 getting into conduction due to the voltage developed at the collector of Q2 when the output stage is in the low state.

The 80 ohm resistor connected to the collectors of Q9

and Q11 will affect the current drain from VCC increasing it if it is too low. If, on the other hand, it has a higher value, it will decrease the speed of the device, adversely affecting TPLH.

The output stage is implemented with Schottky Clamped Transistors to improve the speed response of the device by not allowing saturation region operation minimizing, therefore, the base storage time.

The output high or low state depends on whether or not the fuse has been blown. When the fuse is still intact, the value of R_f is around 50 ohms. Once the row decoder is selected as we had seen in section A.3.3, it will provide an output voltage of 3.2 volts to the base of transistor Q3. The selected column decoder provides an output voltage of 2.4 volts that is fed to the base of Q4. This transistor will be in conduction, and its emitter current will be set to 3 mA by the current mirror and its emitter will be at 1.6 volts. This voltage level will turn Q2 and Q10 ON forcing the output voltage to be a logic low level of approximately 0.3 volts which is the collector-emitter voltage of Schottky Transistor Q10.

As a result, we have that for an intact fuse. The output is forced to VOL. If the fuse has been blown the value of R_f is around 1 M-OHM. This large value will cause the current mirror to saturate providing a voltage of 0.3

volts to the cathode of D3 which will cause Q2 and Q10 to be OFF and Q9-Q11 will be ON providing an output of VOH given by $VCC - 2V_{BE} (ON) = 3.4$ volts.

A.4. MIL-M-38510/210 (S/S) Electrical Test Requirements

A list of the testing required per the Slash Sheet is presented in Table A-2. The purpose and methodology for performing each of these tests will be given throughout this section.

A.4.1 VIC: INPUT CLAMP VOLTAGE

Refer to Figure A-4 (Typical Input Circuit)

PURPOSE:

The purpose of this test is to ensure that the input structures will be protected by the clamp diodes in the event of a negative voltage spike (or continuous voltage) on the input pins.

METHOD:

This test is performed by forcing a current of -10 mA. across diode D1 in the forward bias direction on the tested input pin and measuring the voltage. Note that all currents flowing into the device under test (D.U.T.) Will be positive and currents flowing out of the D.U.T. will be negative. The VCC pin is set to 4.5v. Output pins are open and all the other inputs are set to either a logic one or logic zero voltage.

Input clamp voltage	VIC
Low-Level Output Voltage	VOL
High-Level Output Voltage	VOH
Low-Level Input Current	IIL
High-Level Input Current	IIH
High Impedance Output High Current	IOHZ
High Impedance Output Low Current	IOLZ
Short Circuit Output Current	IOS
Supply Current	ICC
Gross Functional	
Prop. Delay High to Low (Address to Output)	TPHL1
Prop. Delay Low to High (Address to Output)	TPLH1
Prop. Delay High to Low (CE to Output)	TPHL2
Prop. Delay Low to High (CE to Output)	TPLH2

TABLE A-2

SLASH SHEET ELECTRICAL TESTS (S/S)

A.4.2 VOL: Logic Low Output Voltage.

Refer to Figure A-7 (Typical Output Circuit)

PURPOSE:

This test is conducted to ensure that when transistor Q10 is saturated, (Q10 is not heavily into the saturation region due to the Schottky Clamp Diode between base and collector) it will be at least able to sink a current equal to I_{OL} and still maintain a logic low voltage level. At larger currents, the voltage drop on the collector of the transistor could exceed the voltage level of a logic zero due to the resistance in series with the collector lead which is associated with the finite resistivity of the N-Type Collector Material.

METHOD:

A current greater than or equal to I_{OL} is forced into the tested output pin and the voltage developed at this point is read. This test is performed with the supply voltage set to 4.5V which is a worst case value for the saturation of transistor Q10. Enable inputs CE3 and CE2 are set to 2.0 volts which will guarantee that they operate correctly with a minimum V_{IH} level.

In the same fashion, CE1 is set to a voltage of 0.8 V. to guarantee its correct operation with the tighter condition of a maximum V_{IL} voltage. All address lines are set to an address such that the tested output is in a logical low

state. All other un-tested outputs are left open.

A.4.3. VOH: Logic High Output Voltage

Refer to Figure A-7 (Typical Output Circuit)

PURPOSE:

The VOH test is performed to ensure that a logic high voltage can be maintained at the output pin while sourcing an IOH current. The output voltage will be typically below VCC by two forward diode drops ($V_{BE9} + V_{BE11}$) since the current through the 1.5K resistor will be very low ($I_{OH}/(B_9 \cdot B_{11})$). The voltage drop across the 1.5K resistor can be neglected.

METHOD:

An address such that a logic one voltage is present at the output to be tested is applied to the DUT. This condition is usually selected by accessing the test word/test bit fuses for an unprogrammed device as outlined in section A.3. A current greater than or equal to IOH is forced out of the tested output pin and the voltage at that point is read. The VCC Voltage is set to the tighter 4.5V level (as $VOH = VCC - 2V_{BE} (ON)$). CE3 and CE2 are set to 2.0 V. (Min VIH), and CE1 is set to 0.8V (max VIL). Therefore VIL and VIH on the chip select inputs are tested in an implicit manner.

A.4.4 IIL: Low Level Input Current.

Refer To Figure A-4 (Typical Input Circuit)

PURPOSE:

This is the current into an input when a low level voltage is applied to that input. The low level input current test is intended to measure the value of the 6K Pull Up Resistor tied to the emitter of the PNP transistor Q1. The reading of this test will also provide an indication of Q1's Beta , and also will guarantee the maximum input load that this input presents.

METHOD:

Each input pin is measured one at a time. Since the input current is given by $IIL = [VCC - (VIL + VBE)] / (R1 * B)$, it is tighter to measure at $VCC = 5.50V$. All untested input pins are set to a logic 1 voltage level and the measured input is forced to 0.5V and its current is measured. Output terminals are left open.

A.4.5 IIH: High Level Input Current

Refer to Figure A-4 (Typical Input Circuit)

PURPOSE:

This is the current into an input when a high level voltage is applied to that input.

Each input pin is measured separately. The VCC terminal is set to 5.50V which will be the tighter condition for the reverse leakage. All un-tested input pins

are set to a logic zero voltage level and the measured input pin is forced to 5.5V and its current is measured; output pins are left open.

A.4.6 IOHZ:HIGH IMPEDANCE OUTPUT HIGH CURRENT

Refer to Figure A-7 (Typical Output Circuit)

PURPOSE:

This is the current flowing into an output with input conditions applied that will cause upper and lower output transistors to be in the OFF state.

The IOHZ test measures the current source capability of the device when both upper and lower transistor of the totem pole output structure are turned OFF, therefore measuring the ability of the chip select inputs to TRI-STATE the device.

METHOD:

VCC is set to 5.50V to ensure that the output will have the greatest drive capability. The address input lines are set to the appropriate voltage levels such that a logic zero is present at the output to be tested. The chip select inputs are set to the voltage levels that disable the device under test ($CE3=CE2=0.5V$ and $CE1=4.5V$) to simultaneously detect their ability to tri-state the output. At this point the measured output is forced to a voltage of 5.2 volts and the current drawn into the device is then measured.

A.4.7 IOLZ: High Impedance Output Low Current

Refer To Figure A-7 (Typical Output Circuit)

PURPOSE:

This is the current flowing into an output that has three state capability, with input conditions selected in a manner that will establish the high impedance state at the output, and with a low level voltage applied to it.

The IOLZ test measures the current sink capability of the device when both output transistors Q10 and Q11 are turned OFF, measuring also the ability of the chip select input to TRI-STATE the device.

METHOD:

VCC is set to 5.50V for maximum drive capability on the output. The address input lines are set to the appropriate voltage levels such that a logic one is present at the output to be tested. This condition is usually selected by accessing the Test Word-Test Bit fuses for an un-programmed device as outlined in section 4.3. The chip select inputs are set to the voltage levels that disable the device under test ($CE3=CE2=0.5V$ and $CE1=4.5V$) to simultaneously detect their ability to TRI-STATE the output. At this point the measured output is forced to a voltage of 0.5 volts and the current drawn out of the device is then measured.

A.4.8. IOS: Short-Circuit Output Current

Refer to Figure A-7 (Typical Output Circuit)

PURPOSE:

This test measures the output current drive capability for a logic high output when that output is short-circuited to ground. This test will evaluate mainly the 80 ohm resistor from VCC as well as transistors Q9 and Q11.

METHOD:

An input address such that a VOH level will be present at the output to be tested is presented to the input lines, CE3 and CE2 are held high to 4.5 volts. CE1 is set to 0.5 in order to enable the output circuitry. For an un-programmed device, the VOH level is attained by accessing the spare fuses in the Test Word/Test Bit area outside the main array. Both a minimum of -10 mA and a maximum of -100 mA (absolute values) are tested.

A.4.9 ICC: Supply Current

PURPOSE:

In this test the current flowing into the VCC supply terminal of the device is measured. The current consumption is monitored to insure that the device will not be forced to dissipate an excessive amount of power. This test can be affected by defects creating short circuit conditions or by poor control of resistor values.

METHOD:

The specified maximum VCC level of 5.5 volts is applied to the device. All of the input pins are connected to ground so that the current through the inputs is accounted for and then the current into the VCC supply is measured.

A.4.10 Gross Functional Verification**PURPOSE:**

The functional tests verify that no fuses are blown for un-programmed devices by reading all addresses in the device. This test can yield incorrect results if there are faults in the decoder circuitry. The actual functionality of a PROM cannot be established until the desired function has been programmed into it.

METHOD:

This test is performed at both minimum and maximum VCC levels of 4.5 and 5.5 volts. The input levels will be at 2.4 volts for VIH and 0.4 volts for VIL. A sequence such that all address locations are scanned is applied to the inputs. The outputs are monitored as high for voltages above 1.5 volts and low for levels below 1.5 volts. The timing set used does not verify full speed operation.

A.4.11 TPHL/TPLH Propagation Delay High-Low/Low-High

PURPOSE:

To measure the time it takes for the output circuitry to make the transitions from low to high and high to low states.

These changes of state are produced by address lines and measured in TPHL1/TPLH1 or by the chip enable lines and measured in TPHL2/TPLH2.

For the transition from low to high it is necessary to turn OFF base current to transistor Q10 (Figure A-7) which means that we must also turn OFF transistor Q2. Both Q9 and Q11 will need to be turned ON. These changes can be initiated by either: the address lines and coupled through D3 or the chip enable lines and coupled through Q8.

METHOD:

These tests are performed at both VCC=4.5 and 5.5 volts. For the un-programmed devices high logic levels on the outputs are achieved by accessing the test fuses (TW/TB) described in section A.3.4.

A transition is generated on the input lines (address or chip enable), and the time for the output to switch state measured in relation to the input transition between 1.5 volt points.

APPENDIX B

Electrical Readings

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LOT A TEST STEP 2

PRE B/I 6J2132 T= 25 C HANDLER

SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	BIN #
	VCC=0.3v	VCC=5.5v	VCC=5.0v	VCC=0.3v	ICC4-ICC1	
1001	433	145.3	127.5	438	5	1
1002	436	145.6	127.8	442	6	1
1003	229	145.5	127.7	232	3	1
1004	71	146.8	129	73	2	1
1005	394	141.4	124	404	10	1
1006	158	143.9	126.3	160	2	1
1007	132	136.1	119.4	136	4	1
1008	586	149.4	130.9	587	1	1
1009	364	137.9	121	368	4	1
1010	498	138.8	121.8	504	6	1
1011	830	142.8	125.3	839	9	1
1012	493	147	129	501	8	1
1013	111	144.6	126.8	111	0	1
1014	281	142.7	125.1	284	3	1
1015	335	141	123.7	339	4	1
1016	453	148.4	130	463	10	1
1017	115	137.5	120.5	120	5	1
1018	1273	150.3	131.8	1278	5	1
1019	341	141.3	123.9	347	6	1
1020	237	139.8	122.5	236	-1	1
1021	211	136.1	119.3	210	-1	1
1022	384	138	121.1	387	3	1
1023	361	147.8	129.6	370	9	1
1024	375	150	131.5	381	6	1
1025	260	144.7	126.9	265	5	1
1026	84	146.4	128.3	87	3	1
1027	283	143.2	125.5	288	5	1
1028	220	141.6	124.2	227	7	1
1029	458	148.2	130.1	468	10	1
1030	72	137.1	120.2	71	-1	1
1031	159	139.5	122.4	162	3	1
1032	213	136.8	120	217	4	1
1033	218	143.7	126	218	0	1
1034	119	144.5	126.8	122	3	1
1035	714	145.8	127.8	716	2	1
1036	80	141.3	124	80	0	1
1037	299	142.5	125.1	308	9	1
1038	225	138.6	121.6	231	6	1
1039	502	152.6	133.6	511	9	1
1040	605	146.7	128.7	603	-2	1
1041	255	144.7	127	262	7	1
1042	211	141	123.5	210	-1	1
1043	78	137.4	120.5	80	2	1

1044	128	138.5	121.6	129	1	1
1045	332	137	120.3	338	6	1
1046	391	140	123	397	6	1
1047	306	136.6	119.7	307	1	1
1048	504	146.2	128.3	511	7	1
1049	341	148.8	130.5	348	7	1
1050	77	138.5	121.5	77	0	1
1051	593	146	127.9	595	2	1
1052	910	143.1	125.4	909	-1	1
1053	116	138.7	121.7	120	4	1
1054	707	145.2	127.3	712	5	1
1055	141	146.8	128.7	146	5	1
1056	958	151.1	132.4	968	10	1
1057	352	139.1	121.9	357	5	1
1058	607	142.9	125.2	617	10	1
1059	89	143.5	125.9	91	2	1
1060	355	142.6	125.1	358	3	1
1061	77	137.1	120.3	79	2	1
1062	131	144.1	126.2	132	1	1
1063	119	140.2	122.9	121	2	1
1064	368	143.3	125.7	374	6	1
1065	143	146.7	128.9	143	0	1
1066	659	145.9	127.9	665	6	1
1067	80	145.9	127.9	81	1	1
1068	651	147.4	129.3	658	7	1
1069	378	145	127	386	8	1
1070	92	141.1	123.8	90	-2	1
1071	334	148.4	130.2	340	6	1
1072	989	149.7	131.3	994	5	1
1073	270	145.7	127.9	272	2	1
1074	246	143.3	125.6	246	0	1
1075	194	140.3	123.2	197	3	1
1076	81	137.8	120.9	84	3	1
1077	672	146.6	128.6	679	7	1
1078	153	142.9	125.4	154	1	1
1079	1314	144.1	126.4	1326	12	1
1080	84	142.7	125.2	86	2	1
1081	278	139.4	122.3	280	2	0
1082	328	146.5	128.3	323	-5	1
1083	87	140.8	123.4	92	5	1
1084	124	135.8	119.2	126	2	1
1085	647	140.4	123.1	660	13	1
1086	191	137.4	120.4	190	-1	1
1087	697	142.7	125	701	4	1
1088	92	138.3	121.3	93	1	1
1089	469	142.8	125.3	472	3	1
1090	168	145.4	127.6	170	2	1
1091	97	143.5	126	101	4	1
1092	85	136.8	120	87	2	1
1093	425	143.6	125.9	430	5	1
AVERAGES	340.91	141.54	124.13	344.78	3.89	
STD DEV	259.77	13.83	12.12	261.39	3.40	

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LOT A

TEST STEP 7

SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	BIN #
	VCC=0.3v	VCC=5.5v	VCC=5.0v	VCC=0.3v	ICC4-ICC1	
1001	531	144.9	127.2	527	-4	1
1002	461	145.7	127.7	455	-6	1
1003	279	145.6	127.7	279	0	1
1004	99	146.6	129	93	-6	1
1005	483	141.4	124.1	483	0	1
1006	199	144	126.3	197	-2	1
1007	171	136	119.5	172	1	1
1008	679	149.5	131.2	666	-13	1
1009	403	138	121.1	401	-2	1
1010	560	138.8	121.8	560	0	1
1011	974	142.7	125.2	960	-14	1
1012	585	146.6	128.7	583	-2	1
1013	131	144.6	127	131	0	1
1014	315	142.7	125.1	311	-4	1
1015	423	141	123.8	415	-8	1
1016	507	148.5	130.2	502	-5	1
1017	143	137.5	120.7	143	0	1
1018	1417	149.9	131.5	1400	-17	1
1019	424	141.2	123.9	414	-10	1
1020	315	139.6	122.5	309	-6	1
1021	254	136.1	119.4	255	1	1
1022	500	137.8	120.9	493	-7	1
1023	413	146.9	128.8	410	-3	1
1024	453	149.4	131.1	446	-7	1
1025	324	144.8	127	318	-6	1
1026	106	146	128.1	103	-3	1
1027	379	143.2	125.7	376	-3	1
1028	252	141.6	124.3	253	1	1
1029	542	148.3	130	545	3	1
1030	92	137.2	120.3	88	-4	1
1031	183	139.3	122.2	181	-2	1
1032	243	136.7	120	239	-4	1
1033	249	143.5	125.9	248	-1	1
1034	136	143.5	125.9	132	-4	1
1035	733	146	128.1	725	-8	1
1036	96	141.3	124	96	0	1
1037	344	142.4	125	340	-4	1
1038	257	138.5	121.6	254	-3	1
1039	587	152	133.4	583	-4	1
1040	669	146.7	128.2	668	-1	1
1041	305	144.7	127	297	-8	1
1042	261	140.6	123.4	262	1	1
1043	96	136.9	120.1	93	-3	1

1044	153	138.5	121.3	147	-6	1
1045	380	136.7	120	377	-3	1
1046	332	139.9	122.8	325	-7	1
1047	314	136.7	120	312	-2	1
1048	508	146.4	128.5	510	2	1
1049	383	149.1	130.8	375	-8	1
1050	94	138.5	121.6	92	-2	1
1051	835	145.9	127.9	829	-6	1
1052	930	143.1	125.1	926	-4	1
1053	145	138.4	121.5	140	-5	1
1054	785	144.8	127.1	775	-10	1
1055	170	146.8	128.9	168	-2	1
1056	1073	151	132.4	1059	-14	1
1057	410	139	122	408	-2	1
1058	684	142.5	125	686	2	1
1059	112	143.1	125.5	108	-4	1
1060	391	142.6	125.2	386	-5	1
1061	93	136.4	119.8	90	-3	1
1062	147	144	126.3	148	1	1
1063	131	140.3	123.1	130	-1	1
1064	423	143.2	125.7	417	-6	1
1065	162	146.5	128.9	157	-5	1
1066	686	145.2	127.4	683	-3	1
1067	150	145.7	127.8	143	-7	1
1068	742	147.7	129.6	732	-10	1
1069	439	145	127.2	432	-7	1
1070	120	141.1	123.9	116	-4	1
1071	373	148.5	130.3	365	-8	1
1072	1093	149.6	130.9	1090	-3	1
1073	305	145.8	127.9	304	-1	1
1074	300	143.3	125.8	296	-4	1
1075	218	140.3	123.1	212	-6	1
1076	95	137.9	121.1	92	-3	1
1077	852	146.8	128.7	848	-4	4
1078	176	143.2	125.6	172	-4	1
1079	1401	144.2	126.6	1388	-13	1
1080	93	142.7	125.2	90	-3	1
1081	287	138.7	121.7	287	0	0
1082	367	146.4	128.4	368	1	1
1083	98	140.8	123.5	102	4	1
1084	141	135.9	119.2	135	-6	1
1085	710	140.4	123.1	703	-7	1
1086	200	137.3	120.5	199	-1	1
1087	720	142.7	125.2	712	-8	1
1088	105	138.3	121.3	105	0	1
1089	519	142.9	125.4	516	-3	1
1090	193	145.3	127.4	193	0	1
1091	94	143.7	126.1	92	-2	1
1092	89	137.1	120.4	88	-1	1
1093	438	143.5	125.9	438	0	1
AVERAGES	388.48	141.44	124.10	384.63	-3.79	
STD DEV	285.48	13.86	12.11	283.38	3.98	

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LOT A

TEST STEP 8

POST B/I 504+168 HR+168 HRS ROOM TEMP.

HAND-TEST

SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	BIN #
ICC4-ICC1						
VCC=0.3v VCC=5.5v VCC=5.0v VCC=0.3v						

1001	527	145.1	127.3	521	-6	1
1002	474	145.4	127.5	468	-6	1
1003	314	144.9	127.2	309	-5	1
1004	104	146.1	128.6	101	-3	1
1005	561	141.2	124.3	558	-3	1
1006	237	143.7	126.1	233	-4	1
1007	182	135.8	119.3	180	-2	1
1008	731	149.2	131	725	-6	1
1009	424	137.9	121.1	425	1	1
1010	602	138.7	121.8	587	-15	1
1011	1032	142.3	124.9	1028	-4	1
1012	649	146.8	128.9	635	-14	1
1013	153	137.1	120.5	150	-3	1
1014	362	142.3	124.8	356	-6	1
1015	413	140	122.9	411	-2	1
1016	568	146.7	128.8	561	-7	1
1017	177	136.7	120.1	178	1	1
1018	1525	149.6	131.4	1523	-2	1
1019	470	139.8	122.8	459	-11	1
1020	297	139	122.1	295	-2	1
1021	254	135.9	119.4	249	-5	1
1022	478	137.8	120.8	476	-2	1
1023	456	144.7	126.9	448	-8	1
1024	496	149.4	131.2	489	-7	1
1025	368	144.3	126.7	359	-9	1
1026	130	146	128.2	129	-1	1
1027	373	143	125.5	369	-4	1
1028	292	140.8	123.6	290	-2	1
1029	596	147.9	129.9	589	-7	1
1030	118	136.8	120.2	115	-3	1
1031	224	138.2	121.3	224	0	1
1032	296	136.3	119.8	289	-7	1
1033	305	143.2	125.9	304	-1	1
1034	179	139.5	122.2	172	-7	1
1035	767	145.9	127.9	764	-3	1
1036	117	140.3	123.1	115	-2	1
1037	371	141.6	124.4	381	10	1
1038	287	138.3	121.4	289	2	1
1039	661	150.5	132.1	656	-5	1
1040	669	146.7	128.2	668	-1	1
1041	352	144.4	126.7	351	-1	1
1042	283	140.7	123.5	276	-7	1
1043	125	135.9	119.5	123	-2	1

1044	187	138.3	121.5	181	-6	1
1045	440	136.7	120	439	-1	1
1046	403	138.5	121.6	394	-9	1
1047	357	136.7	120	354	-3	1
1048	626	146.1	128.3	617	-9	1
1049	488	148.9	130.7	486	-2	1
1050	99	138.3	121.5	96	-3	1
1051	715	145.8	127.9	709	-6	1
1052	954	143	125.5	954	0	1
1053	158	139.1	122.2	161	3	1
1054	908	144.6	127	911	3	1
1055	252	146.3	128.5	247	-5	1
1056	1367	150.1	131.8	1355	-12	1
1057	555	137.6	120.9	548	-7	1
1058	877	141.5	124.2	876	-1	1
1059	184	143	125.6	183	-1	1
1060	531	141.9	124.6	530	-1	1
1061	155	136.5	119.3	152	-3	1
1062	267	143.3	125.9	263	-4	1
1063	246	139.6	122.7	242	-4	1
1064	585	142.1	124.9	575	-10	1
1065	172	146.1	128.4	173	1	1
1066	743	145.8	127.9	736	-7	1
1067	117	145.8	127.9	116	-1	1
1068	820	147.5	129.5	801	-19	1
1069	487	144.9	127.1	486	-1	1
1070	127	140.7	123.6	124	-3	1
1071	413	148.4	130.3	411	-2	1
1072	1172	149.2	131	1168	-4	1
1073	347	145.7	127.9	345	-2	1
1074	325	143	125.5	323	-2	1
1075	249	140.1	122.9	249	0	1
1076	124	137.6	120.9	123	-1	1
1077	881	146.4	128.6	857	-24	4
1078	222	142.3	125	219	-3	1
1079	1569	143.9	126.4	1553	-16	1
1080	113	142.5	125.1	112	-1	1
1081	329	138.8	121.9	329	0	0
1082	399	145.9	128.1	390	-9	1
1083	134	140.5	123.3	130	-4	1
1084	179	134.6	118.2	179	0	1
1085	811	140.1	122.9	802	-9	1
1086	263	136.8	120.1	255	-8	1
1087	834	141.9	124.6	831	-3	1
1088	186	137.8	121	183	-3	1
1089	630	142.5	125.1	619	-11	1
1090	251	144.8	127.2	252	1	1
1091	151	143.4	125.9	146	-5	1
1092	121	136.7	120	119	-2	1
1093	587	143.3	125.9	587	0	1
AVERAGES	440.61	140.91	123.71	436.45	-4.10	
STD DEV	308.69	13.78	12.09	306.84	4.86	

LOT A

TEST STEP 9

POST B/I 504 + 168 + 168 + 168

T = 25 C. HANDLER

SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	BIN #
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ICC4-ICC1

VCC=0.3v VCC=5.5v VCC=7.5v VCC=0.3v

1001	407	145	218	447	40	1
1002	402	144.3	218	421	19	1
1003	216	144.2	217	222	6	1
1004	60	145.2	217	61	1	1
1005	402	140.7	212	415	13	1
1006	140	143.3	216	152	12	1
1007	123	135	203	130	7	1
1008	551	147.9	223	604	53	1
1009	327	137.4	207	349	22	1
1010	478	137.9	207	486	8	1
1011	828	142.5	215	857	29	1
1012	487	145.6	220	505	18	1
1013	86	143.4	216	88	2	1
1014	257	142.2	214	278	21	1
1015	296	139.8	211	319	23	1
1016	399	143.1	215	432	33	1
1017	88	136.5	205	97	9	1
1018	1235	149.2	224	1273	38	1
1019	323	140	211	336	13	1
1020	207	136.9	206	214	7	1
1021	170	134.8	202	181	11	1
1022	368	136.1	204	397	29	1
1023	322	145.4	219	337	15	1
1024	345	148.7	224	359	14	1
1025	225	143.2	216	235	10	1
1026	58	145.2	219	63	5	1
1027	242	142.1	214	261	19	1
1028	195	140.6	212	215	20	1
1029	435	146.5	221	471	36	1
1030	49	135.7	204	58	9	1
1031	131	137.7	207	146	15	1
1032	185	135.7	204	197	12	1
1033	187	141.1	212	194	7	1
1034	91	143	215	98	7	1
1035	610	144.2	217	658	48	1
1036	64	138.8	209	72	8	1
1037	268	139	209	277	9	1
1038	198	137.5	207	208	10	1
1039	475	149.2	225	501	26	1
1040	575	143.5	216	594	19	1
1041	229	143.8	217	241	12	1
1042	173	138.5	208	195	22	1
1043	51	135.6	204	63	12	1

1044	96	136.8	205	104	8	1
1045	306	135.3	203	321	15	1
1046	274	138.9	209	289	15	1
1047	263	134.7	202	284	21	1
1048	436	143.7	216	454	18	1
1049	307	148.4	224	346	39	1
1050	48	136.8	206	59	11	1
1051	583	144.7	218	598	15	1
1052	871	136.6	207	878	7	1
1053	93	137.8	207	97	4	1
1054	668	143.2	216	713	45	1
1055	119	146.3	221	134	15	1
1056	951	149.6	225	997	46	1
1057	336	138.1	207	361	25	1
1058	594	140.2	211	607	13	1
1059	76	132.3	200	82	6	1
1060	342	140	211	350	8	1
1061	48	135.7	204	54	6	1
1062	106	141.4	213	118	12	1
1063	87	137.6	207	98	11	1
1064	327	141.2	213	357	30	1
1065	108	143.2	214	113	5	1
1066	614	144.7	218	628	14	1
1067	49	141	213	54	5	1
1068	629	146.7	221	669	40	1
1069	367	133.6	216	386	19	1
1070	60	138.5	208	74	14	1
1071	300	145.2	219	313	13	1
1072	961	147.6	222	1005	44	1
1073	239	144.4	218	248	9	1
1074	220	142.2	214	220	0	1
1075	158	139.7	210	164	6	1
1076	52	135.6	204	61	9	1
1077	644	143.8	216	669	25	4
1078	131	140.3	211	140	9	1
1079	1253	129.9	196	1304	51	1
1080	63	142	214	67	4	1
1081	243	134.1	199	261	18	0
1082	312	145.7	220	319	7	1
1083	72	139.8	211	74	2	1
1084	93	132.9	200	102	9	1
1085	621	140.1	211	646	25	1
1086	150	136.4	205	166	16	1
1087	639	141.9	214	682	43	1
1088	65	136.8	206	68	3	1
1089	437	142.9	216	447	10	1
1090	139	145.4	220	148	9	1
1091	53	141.5	213	59	6	1
1092	48	135.9	204	60	12	1
1093	384	142.2	214	394	10	1
AVERAGES	311.17	139.50	210.14	327.82	16.69	
STD DEV	256.95	13.74	20.72	266.00	12.42	

LOT A-R TEST STEP A

6J2132E2

PRE B/I

T= ROOM

HAND-TEST

SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	TESTS FAILED
	VCC=0.3v	VCC=5.5v	VCC=5.0v	VCC=0.3v	ICC4-ICC1	
1100	1492	148.9	130.6	1439	-53	VICL, IIL, TPHL
1101	1261	147.2	129.1	1218	-43	VICL, CE
1102	1216	149.1	130.6	1173	-43	VICL, TW-TB
1103	1405	148.2	129.9	1355	-50	VICL
1104	616	136.5	119.8	594	-22	VICL
1105	1304	148.1	129.9	1254	-50	VICL
1106	1901	149	130.5	1871	-30	VICL
1107	1063	147.4	129.2	1014	-49	VICL
1108	191	144.5	126.7	180	-11	TW-TB
1109	714	152.8	134.2	685	-29	TW-TB
1110	381	143.1	125.5	361	-20	TW-TB
1111	181	145.2	127.4	172	-9	TW-TB
1112	856	144.4	126.7	835	-21	TW-TB
1113	2047	142.2	124.8	2047	0	TW-TB
1114	243	142.3	124.8	233	-10	TW-TB
1115	119	140.9	123.8	110	-9	TW-TB
1116	1479	147.6	129.5	1400	-79	VOH, IOS
1117	661	145.4	127.5	643	-18	IIL, IOHZ-LZ
1118	416	136.1	119.3	408	-8	VOL, TW-TB
1119	413	139.4	122.3	401	-12	VOH, IOS, TW-TB
1120	747	148	129.7	733	-14	GF, TW-TB
1121	2047	154.6	135.7	2047	0	IIL, IIC1/4
1122	2047	145.4	127.2	2047	0	ICC1/4
1123	2047	139.4	122.3	2047	0	ICC1/4
1124	517	145.6	127.7	495	-22	VIC, VOL, TW-TB
1125	624	147.7	129.4	598	-26	VIC, VOL/H, IOS

AVERAGES	985.86	140.83	123.51	962.50	-22.47
STD DEV	630.15	23.43	20.54	627.39	21.35

6J2132A3

111

LOT A-R

TEST STEP A'

PRE B/I

T= 25 C HANDLER

SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	TESTS FAILED
	VCC=0.3v	VCC=5.5v	VCC=5.0v	VCC=0.3v	ICC4-ICC1	

1100	1283	149	130.5	1297	14	VICL,TPHL
1101	1105	147.2	129.1	1134	29	VICL,CE
1102	996	149.1	130.8	1015	19	VICL,TW-TB
1103	1191	148.4	130	1199	8	VICL
1104	486	136.7	119.9	489	3	VICL
1105	1054	148.2	129.8	1059	5	VICL
1106	1493	149.1	130.6	1514	21	VICL
1107	823	147.6	129.3	836	13	VICL
1108	124	144.7	126.8	127	3	TW-TB
1109	581	153	134.3	587	6	TW-TB
1110	268	143.2	125.6	275	7	TW-TB
1111	115	145.3	127.4	119	4	TW-TB
1112	705	144.6	126.8	709	4	TW-TB
1113	2047	142.3	124.9	2047	0	TW-TB
1114	168	142.5	124.9	171	3	TW-TB
1115	74	140.9	123.9	75	1	TW-TB
1116	1255	147.7	129.4	1272	17	VOH,IQS,TW-TB
1117	563	145.4	127.5	575	12	IOHZ\ LZ,CE
1118	328	136.1	119.5	332	4	VOL,TW-TB
1119	319	139.5	122.3	323	4	VOH,IQS,TW-TB
1120	574	148	129.8	582	8	GF,TW-TB
1121	2047	154.9	135.7	2047	0	ICC1/4,IIH
1122	2047	145.4	127.2	2047	0	ICC1/4
1123	2047	139.6	122.4	2047	0	ICC1/4
1124	395	145.7	127.8	410	15	VIC,VOL,TW-TB
1125	472	147.9	129.5	482	10	VIC,VOL/H,TW-T

AVERAGES	858.71	140.94	123.56	866.49	8.04
STD DEV	625.15	23.45	20.55	625.33	7.20

LOT A-R TEST STEP D

POST B/I

T= 25 C

HANDLER

SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	TESTS FAILED
	VCC=0.3v	VCC=5.5v	VCC=7.5v	VCC=0.3v	ICC4-ICC1	

1100	1171	149.2	225	1220	49	VICL,TPHL
1101	1021	147.5	223	1061	40	VICL,CE
1102	958	149.5	226	999	41	VICL,TW-TB
1103	1148	148.6	224	1230	82	VICL
1104	449	137	206	476	27	VICL
1105	1014	148.5	224	1095	81	VICL
1106	1454	149.3	226	1516	62	VICL
1107	783	147.9	224	817	34	VICL
1108	97	144.9	219	107	10	TW-TB
1109	541	153.3	230	565	24	TW-TB
1110	225	143.5	217	241	16	TW-TB
1111	87	145.8	220	96	9	TW-TB
1112	674	144.9	219	702	28	TW-TB
1113	2047	142.7	215	2047	0	ICC1/4,TWTB
1114	135	142.8	215	146	11	TWTB
1115	52	141.4	211	57	5	TWTB
1116	1157	148	224	1203	46	TW-TB,IOS,V0H
1117	526	145.8	220	544	18	CE,IOH/LZ,IIL
1118	295	136.4	205	312	17	VOL,TWTB
1119	288	140	211	306	18	TWTB,IOS,V0H
1120	504	148.6	225	544	40	GF,TPHL
1121	2047	155.2	234	2047	0	ICC1/4,IIL
1122	2047	145.2	220	2047	0	ICC1/4
1123	2047	139.9	211	2047	0	ICC1/4
1124	384	146	220	405	21	TW-TB
1125	415	148	224	454	39	VIC,VOL,IOS,TW

AVERAGES	822.07	141.24	213.09	848.70	27.42
STD DEV	629.87	23.49	35.48	630.78	22.32

LOT B-1

TEST STEP # 1

SERIAL #	PRE B/I		T= 25 C.		HANDLER	BIN #
	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)		
	ICC4-ICC1					
	VCC=0.3v	VCC=5.5v	VCC=7.5V	VCC=0.3v		
1	143	129.3	193	156	13	1
2	72	138.7	208	74	2	1
3	83	131.1	197	88	5	1
4	61	126.9	190	69	8	1
5	269	127.4	191	275	6	1
6	86	129.3	194	96	10	1
7	260	124.9	187	269	9	1
8	136	128.8	193	147	11	1
9	78	133.1	199	92	14	1
10	78	134.3	202	96	18	1
11	866	129.4	194	883	17	13
12	145	139.1	209	159	14	1
13	187	134	201	190	3	1
14	372	132.2	198	381	9	1
15	141	128.9	193	163	22	1
16	75	136	204	88	13	1
17	327	127.8	192	350	23	1
18	114	129.6	194	122	8	1
19	116	126.6	190	127	11	1
20	84	126.9	190	99	15	1
21	409	132.4	199	433	24	1
22	575	134.6	201	611	36	1
23	87	129.5	194	99	12	1
24	84	125.8	188	90	6	1
25	273	123.8	185	276	3	1
26	325	131.1	196	399	74	13
27	79	133.5	200	99	20	1
28	197	138.3	207	221	24	1
29	374	130.4	196	381	7	1
30	96	127.2	191	105	9	1
31	80	126.6	190	89	9	1
32	65	128.5	193	80	15	1
33	85	133.4	200	93	8	1
34	69	124.7	187	74	5	1
35	277	132.7	199	289	12	1
36	81	135.7	204	91	10	1
37	66	131.6	197	83	17	1
38	106	132.1	198	131	25	1
39	425	129.4	194	438	13	1

40	388	131.6	198	396	8	1
41	460	123.4	185	467	7	1
42	284	137	205	303	19	1
43	170	133.5	200	195	25	1
44	265	130	195	285	20	1
45	115	131.2	197	124	9	1
46	515	134.4	202	525	10	1
47	348	131.4	197	356	8	1
48	423	131.1	196	446	23	1
49	769	135.8	203	820	51	15
50	93	125.8	188	99	6	1
51	172	127.3	190	183	11	1
52	575	128.7	193	599	24	1
53	85	140.7	210	95	10	1
AVERAGES	227.64	128.77	192.98	242.38	14.87	
STD DEV	184.45	15.99	23.98	189.41	11.83	

LOT B-2-R

TEST STEP #1

SERIAL #	PRE B/I T= 25 C				HANDLER
	ICC1	ICC2	ICC3	ICC4	DELTA
	(nA.)	(nA.)	(nA.)	(nA.)	(nA.)
	ICC4-ICC1				
	VCC=0.3v	VCC=5.5v	VCC=7.5v	VCC=0.3v	
200	551	130.8	196	570	19
201	193	128.9	193	210	17
202	145	153.6	232	153	8
203	119	134.2	201	125	6
204	874	124.3	187	896	22
205	66	161.5	245	70	4
206	2047	136.8	205	2047	0
207	357	147.6	222	368	11
208	49	148.5	224	55	6
209	455	140.5	222	480	25
210	186	133.1	200	196	10
211	102	175.6	254	114	12
212	2047	129.9	194	2047	0
213	152	125.9	188	160	8
214	70	131	197	78	8
215	108	131	228	121	13
216	25	134	201	31	6
217	1342	142.5	217	1363	21
218	147	132.2	199	155	8
219	135	132.5	199	149	14
220	313	124.6	187	325	12
221	248	143.2	216	262	14
222	27	136.1	204	28	1
223	342	132.5	199	352	10
224	346	126.3	189	370	24
225	95	138.8	208	110	15
226	-14	0	-1	-15	-1
227	819	138.1	207	850	31
228	592	130.6	196	607	15
229	223	127.8	191	227	4
230	407	141.7	214	438	31
231	255	130.9	196	268	13
232	411	135.7	204	438	27
233	361	129.4	194	374	13
234	279	136.7	205	289	10
235	112	162.6	246	124	12
236	465	133.5	201	479	14
237	120	132.4	202	133	13
238	164	132.8	199	176	12
239	191	131.4	198	200	9

240	2047	145.1	219	2047	0
241	345	147.6	223	376	31
242	244	127.5	191	266	22
243	825	172.5	241	896	71
244	339	174	251	366	27
245	63	137.9	207	72	9
246	217	130.7	196	244	27
247	96	134.3	201	118	22
248	1145	152.7	231	1226	81
249	218	136.8	206	242	24
250	93	130.9	196	106	13
251	125	173.7	261	156	31
252	779	129.7	194	816	37
253	305	129.5	194	317	12
254	200	132.1	198	204	4
255	303	131.9	198	315	12
256	391	133.1	200	411	20
257	143	129.3	193	153	10
258	2047	199.6	1197	2047	0
259	2047	199.6	1197	2047	0
260	352	131.7	198	374	22
261	90	137.7	207	105	15
262	409	130.8	196	427	18
263	25	199.5	298	34	9
264	2047	161.5	204	2047	0
265	638	134	201	651	13
266	532	126.4	189	546	14
267	742	133.6	200	771	29
268	109	179.3	260	138	29
269	70	132.5	199	78	8
270	539	133.7	201	561	22
271	2047	130.1	195	2047	0
272	2047	140.6	215	2047	0
273	147	133.8	201	158	11
274	73	132.8	199	80	7
275	349	171.7	246	364	15
276	68	126.7	190	72	4
277	186	129.4	194	199	13
278	298	142.2	213	309	11
279	409	135.3	203	428	19
280	977	134.9	202	1060	83
281	54	156.7	222	67	13
282	2047	132.5	199	2047	0
283	388	134.8	203	408	20
284	4	33.4	76	64	60
285	70	130.2	196	78	8
286	-16	0	-1	-16	0
287	369	139.1	209	387	18
288	140	130	195	156	16
289	2047	123	185	2047	0
290	2047	144.8	218	2047	0
291	56	176.7	255	78	22
292	2047	133.6	203	2047	0
293	207	161.5	253	242	35

294	366	199.5	313	388	22
295	255	135.1	203	285	30
296	313	132.3	199	342	29
297	124	128.9	193	130	6
298	92	131.9	215	105	13
299	6	22.5	43	138	132
300	30	162.6	234	29	-1
301	296	152	230	331	35
302	368	134.7	202	402	34
303	274	135.1	203	294	20
AVERAGES	488.06	135.51	221.47	505.21	17.36
STD DEV	610.16	31.67	142.24	607.43	18.80

LOT B-2-P

TEST STEP # 1

BIN 1'S

PRE B/I

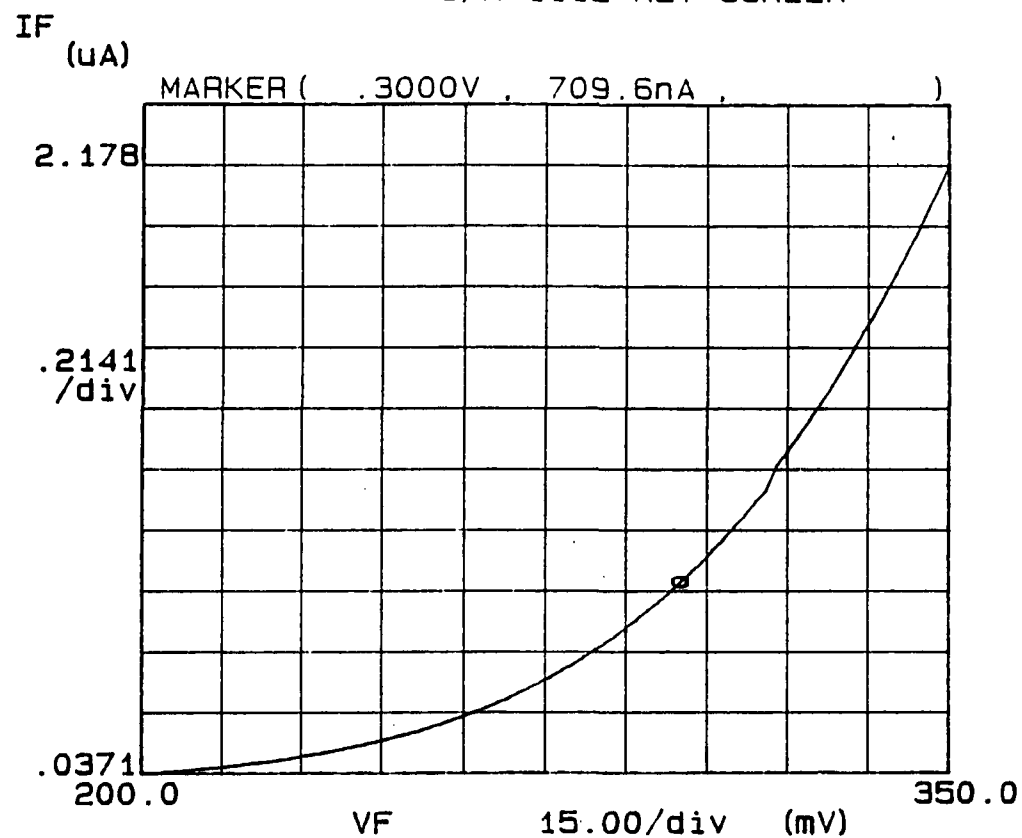
T= 25 C. HANDLER

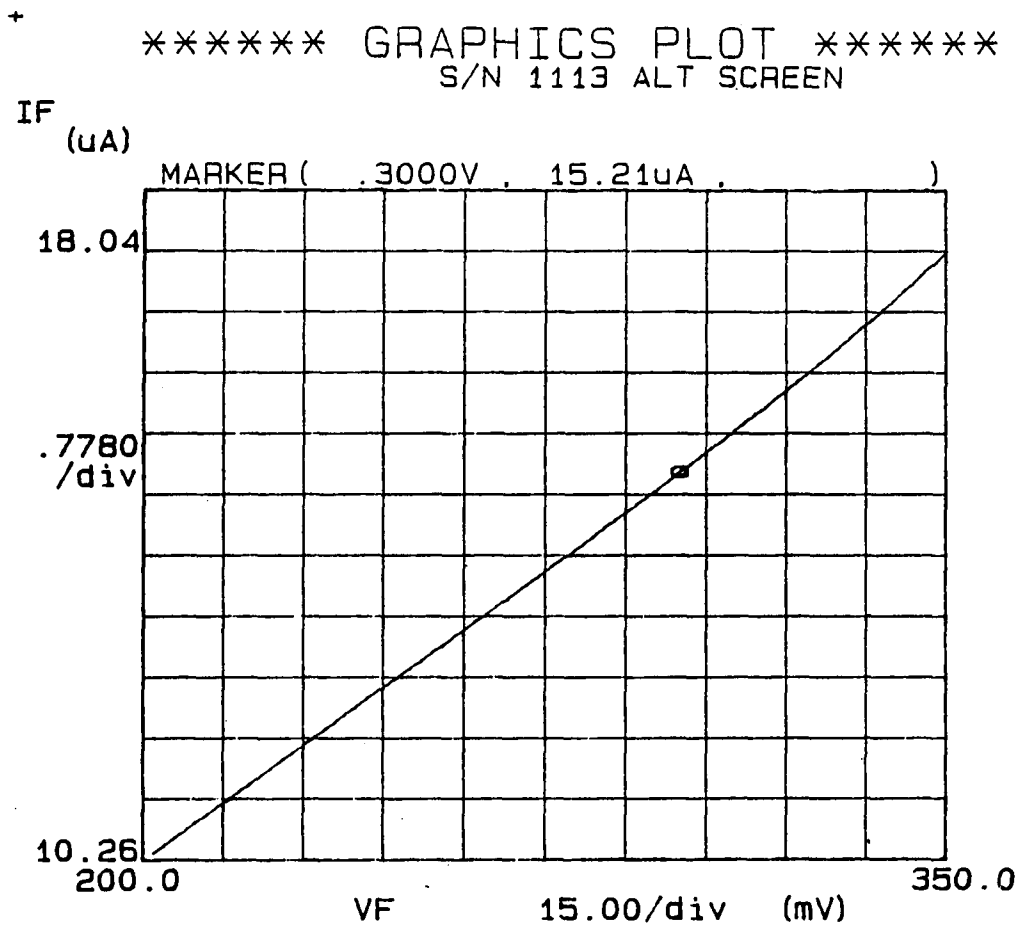
SERIAL #	ICC1 (nA.)	ICC2 (nA.)	ICC3 (nA.)	ICC4 (nA.)	DELTA (nA.)	BIN #
	VCC=0.3v	VCC=5.5v	VCC=7.5v	VCC=0.3v	ICC4-ICC1	
1	152	129.7	194	157	5	1
2	63	121.9	183	68	5	1
3	94	134.3	201	102	8	1
4	235	135.4	204	257	22	1
5	551	130	195	560	9	1
6	163	137	206	167	4	1
7	138	142.5	215	140	2	1
8	104	130.8	196	111	7	1
9	104	128.4	192	122	18	1
10	80	131.9	198	92	12	1
11	68	122.9	184	77	9	1
12	86	132.5	199	90	4	1
13	86	127.4	190	95	9	13
14	139	133.3	200	154	15	1
15	78	129.8	195	91	13	1
16	89	128.8	193	97	8	1
17	99	130.4	195	103	4	1
18	109	143.6	216	113	4	1
19	95	129.5	194	98	3	1
20	184	136.7	201	201	17	1
21	134	129.9	195	136	2	1
22	88	130.9	196	95	7	1
23	207	125.5	188	213	6	1
24	65	127.4	191	70	5	1
25	145	133.6	200	163	18	1
26	81	128.6	193	92	11	1
27	526	135.6	204	527	1	1
28	181	134.3	201	195	14	1
29	74	130.7	196	94	20	1
30	71	133.8	201	89	18	1
31	118	131.7	198	134	16	1
32	123	131.3	197	133	10	1
33	56	123	185	60	4	1
34	69	131.5	197	86	17	1
35	78	139.1	209	92	14	1
36	105	131.4	197	121	16	1
37	70	123.3	185	78	8	1
38	71	133.5	200	80	9	1
39	172	130.6	196	184	12	1

40	58	130.6	197	68	10	1
41	267	135.5	203	281	14	1
42	153	130.2	195	156	3	1
43	65	139.4	209	73	8	1
44	68	131.6	197	78	10	1
45	70	130.5	195	83	13	1
46	500	127	191	537	37	1
47	76	199	199	85	9	1
48	115	193	193	124	9	1
49	71	133.8	201	81	10	1
50	232	130.2	195	244	12	1
51	78	132.8	199	96	18	1
52	90	130.4	196	112	22	1
53	83	130.5	196	99	16	1
54	99	133.5	200	116	17	1
55	74	132	198	83	9	1
56	57	125.8	189	65	8	
57	404	131.2	197	406	2	
58	276	129.4	194	314	38	
59	100	132.5	199	108	8	
60	547	129.9	195	567	20	
61	69	140.1	210	79	10	
62	66	137.3	206	76	10	
63	63	122.9	184	66	3	
64	86	137.3	206	103	17	
65	74	138.7	208	88	14	
66	72	131.2	197	81	9	
67	70	130.1	195	79	9	
68	79	132.2	198	89	10	
69	72	137.7	206	86	14	
70	86	130.2	195	103	17	
71	137	129.5	194	141	4	
72	79	124.5	187	84	5	
AVERAGES	132.88	131.79	194.87	143.87	11.07	
STD DEV	112.94	17.63	21.48	114.69	6.90	

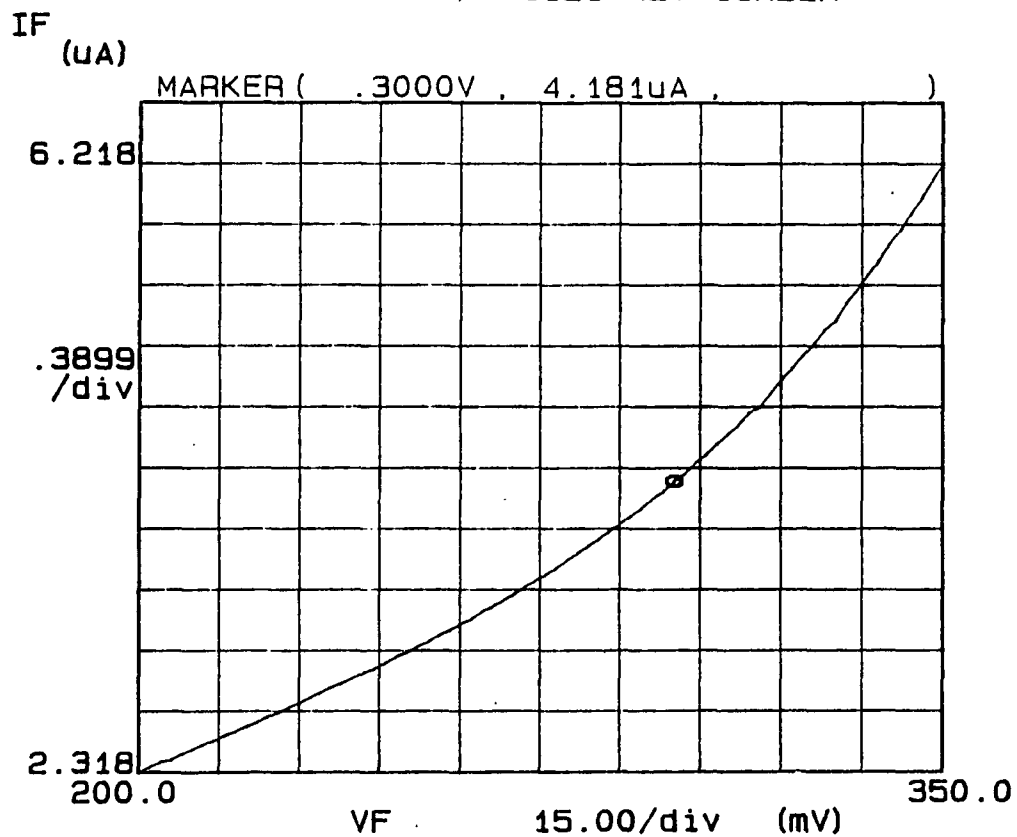
APPENDIX C
LOT "A-R" I/V Plots

***** GRAPHICS PLOT *****
S/N 1112 ALT SCREEN

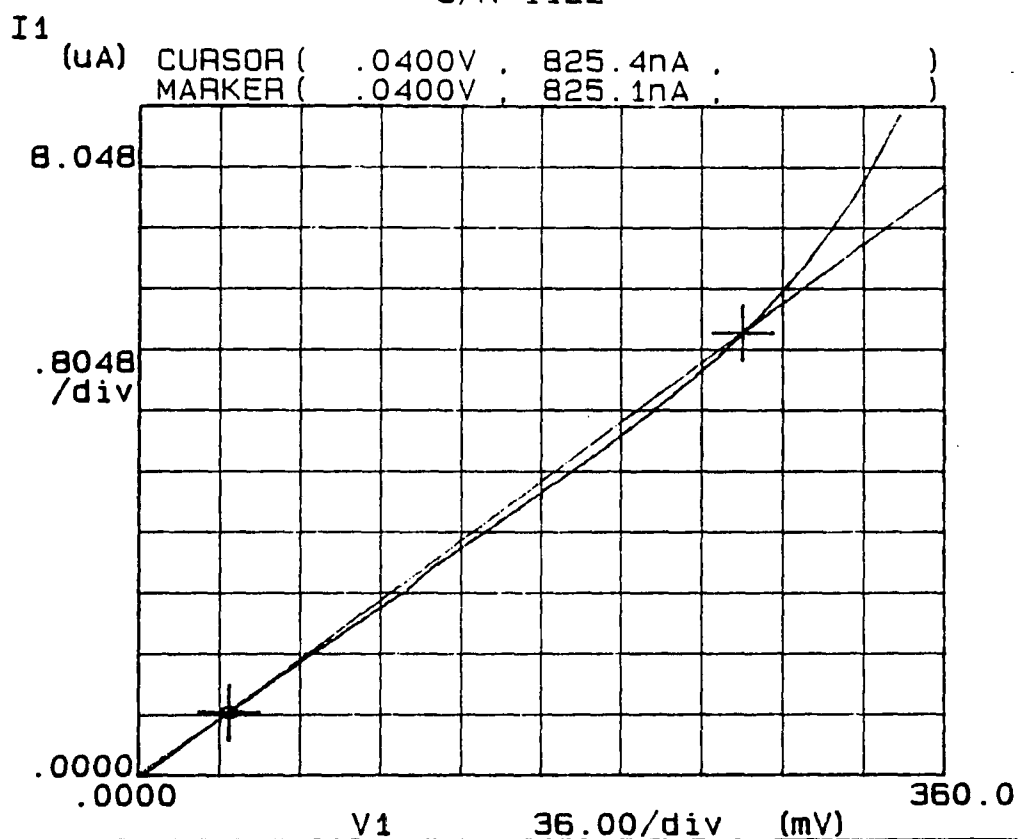




***** GRAPHICS PLOT *****
S/N 1121 ALT SCREEN

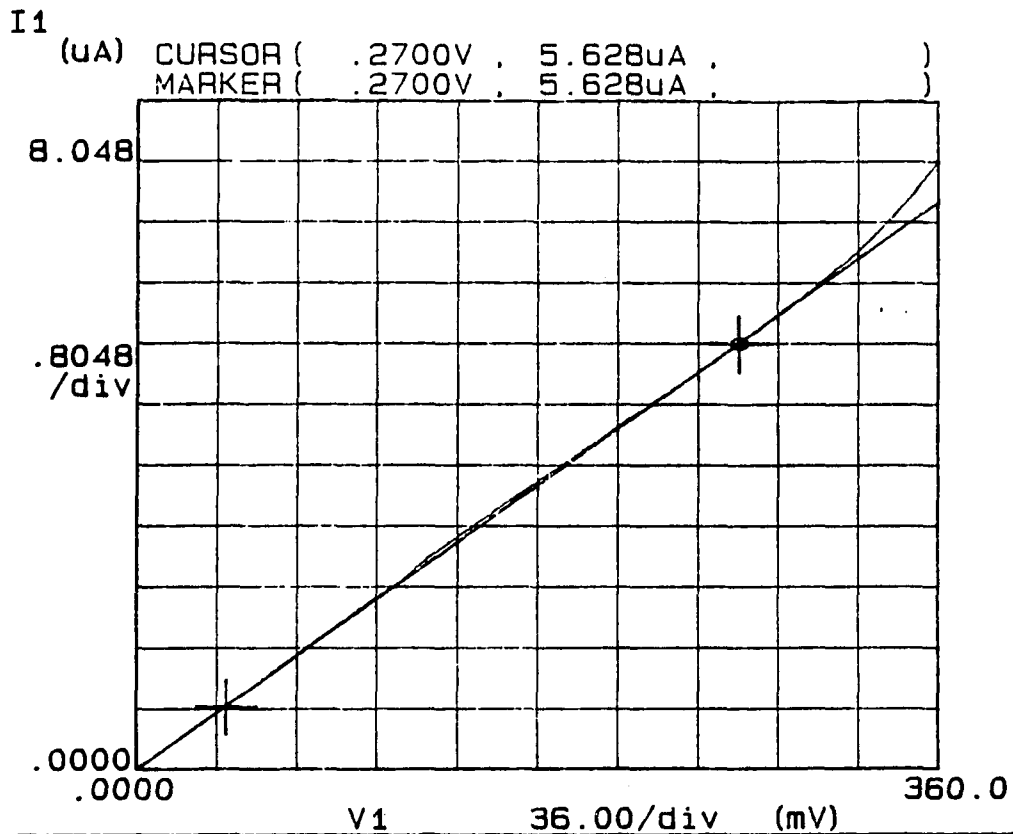


***** GRAPHICS PLOT *****
S/N 1122



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	21.8E-06	45.8E+03	2.16E-03	-47.1E-09
LINE2				

***** GRAPHICS PLOT *****
S/N 1123



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	20.9E-06	47.9E+03	265E-06	-5.53E-09
LINE2				

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