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A CUSTOM BIPOLAR MICROPROCESSOR SUPPORT INTEGRATED CIRCUIT

by

Ira Gene Miller

A Thesis Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

In partial Fulfillment of the Requirements
For the Degree of

MASTER OF SCIENCE
WITH A MAJOR IN ELECTRICAL ENGINEERING

In the Graduate College

THE UNIVERSITY OF ARIZONA

1 9 8 6

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Douglas J. Hamilton — May 29, 1986

Douglas J. Hamilton
Professor of Electrical Engineering

Date

ACKNOWLEDGMENTS

The author wishes to thank his academic advisor, Dr. Douglas J. Hamilton, for his valuable assistance during the development of this thesis and its preparation.

Also to Freida H. Long for her invaluable assistance in the preparation and typing of the manuscript.

And to my wife Carolyn, and my children, Jodi, Erica, and Mike, for their many years of understanding and patience as I devoted time and energy to scholastic activities.

A special thanks to my wife, who helped with the preparation of the manuscript.

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ABSTRACT

Over the past several years the single-chip microprocessor has emerged as an effective building block in digital designs. With adequate capacity to handle specific requirements, the approach can save on board space as well as component and manufacturing cost. Typically, most of the digital aspects of a small system can be accomplished with the microprocessor, although a small number of digital and linear functions usually exist that the microprocessor cannot do or cannot achieve efficiently.

The purpose of this thesis is to examine a custom integrated circuit that was designed to complement a single chip microprocessor, which was programmed to functionally simulate the logic interface electronics that exists between the remote keyboard and a host computer.

The system application, the function of the chip in the system, the circuit design concepts, and the results obtained from the integrated circuit are presented.

CHAPTER 1

INTRODUCTION AND STATEMENT OF THE PROBLEM

1.1 Background

Keyboards for most of the present generation computer systems are peripheral to the mainframe, connected by an interface bus similar in appearance to the coiled cord connecting a telephone handset to the electronics contained in the handset cradle, as illustrated in Fig. 1.1.

The keyboard is an alpha-numeric "typewriter" style ASCII (American Standard Code for Information Interchange) keyboard for text editing and high-level language programming. The alpha-numeric entry from the typewriter keyboard is by nature serial, or one letter at a time, so nothing is lost by presenting the information from the approximately 128 keys, to the computer in a cost effective and convenient asynchronous serial format. Electronics located at the keyboard debounces the pressed key (allowing time for the mechanical switch to settle), codes its identity, and transmits the information to the computer via the connecting cable. Usually the keyboard electronics is Transistor Transistor Logic (TTL) compatible, with a high logic level of 2.4 volts and a low logic level of 0.4 volts providing a 2 volt noise margin. But when data are interface to other remote electronics, such as in the keyboard to Central Processing Unit (CPU) cable interface application, a higher noise margin is desirable and the signals

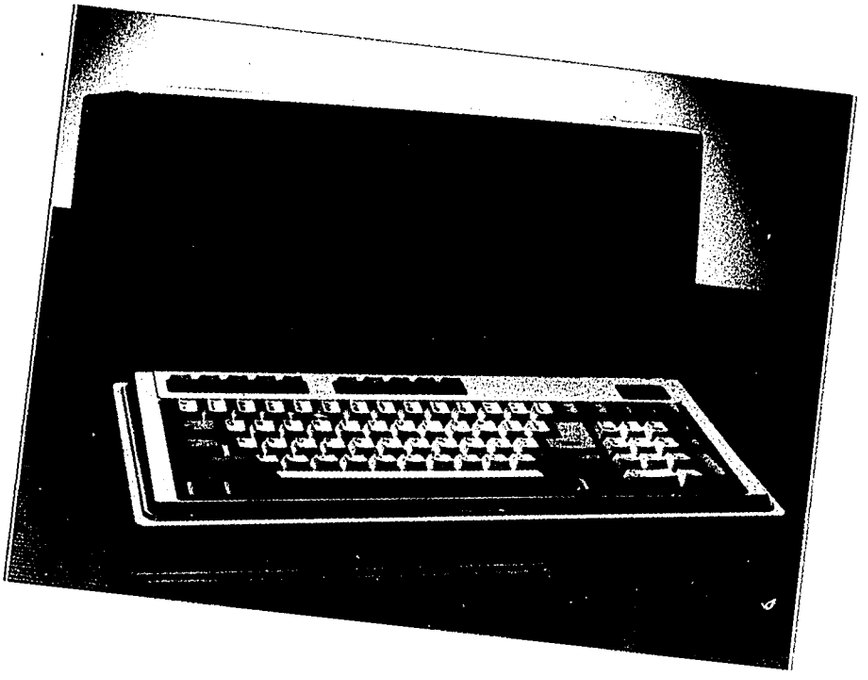


Fig. 1.1 Peripheral Computer Keyboard

are generally converted to larger swings. A few of the levels are represented in the specifications of the popular EIA General Purpose Line Standards in Table 1.1

For short distance applications and where RFI (Radio Frequency Interference) is a consideration, the RS423 standard is a good choice because the driver can be slew-rate controlled, and by sloping the rise and fall times of the squarewave data, many of the high frequency components that can contribute to RFI are avoided. The RS423 standard provides a minimum of 7.2 volts of noise margin with a single-ended driver output swing of $\pm$ 3.6 volts.

In the past, keyboard electronics have been constructed with standard logic, but now by using a single-chip microprocessor and a custom support chip, a more cost effective and improved performance system has been achieved.

1.2 Statement of the Project

Digital interface function was accomplished by using a microprocessor with a custom program contained in 4160 bytes on a chip ROM. The microprocessor (μP) is an MC68HC05, a member of a low cost 8-bit μP family. It is a fully static device which allows operation down to DC, with low power consumption in the standby mode of operation. In addition to the ROM, the chip contains an oscillator, RAM, I/O, a timer, and two Serial Peripheral Interface (SPI) ports. It can operate from a positive supply ranging from 3 to 6 volts.

Table 1.1 Popular EIA Line-Circuit Standards

Parameter	RS232C	RS423A	RS422A	RS485
Mode of operation	Single-ended	Single-ended	Diff	Diff
Number of drivers and receivers	1	1	1	32
allowed on-line	1	10	10	32
Maximum cable length (ft.)	50	4,000	4,000	4,000
Maximum data rate (Kbits PS)	20	100	10,000	10,000
Maximum common mode voltage (V)	± 25	± 6	+ 6 to -0.25	+ 12 to -7
Driver output (V)	±5 min. +5 max.	± 3.6 min. ± 6.0 max.	± 2 min.	± 1.5 min
Driver load (Ω)	3,000 to 7,000	450 min.	100	60
Drive slew-rate (V/μs)	30 max.	Externally Controlled	N/A	N/A
Driver-output short-circuit current limit (mA)	500 to V_{cc} or Gnd	150 to Gnd	150 to Gnd	150 to Gnd 250 to V_{cc} (- 7 or + 12)
Driver-output resistance (kΩ) (High Z State) Power OFF	0.3	60	60	120
Receiver input resistance (kΩ)	3 to 7	4	4	12
Receiver sensitivity (mV)	± 3,000	± 200	± 200	± 200

Keyboard electronics consisting of the microprocessor and the custom chip are assembled on a small printed circuit board. In addition to the keyboard coding function, the system contains four Light Emitting Diodes (LEDs) status indicators, one audio tone generator that synthesizes key clicks and produces various audible status indications, and enough intelligence to recognize a number of different keyboard formats and styles. Keyboards can be supplied by several vendors without any special custom keyboard specifications. Each of the different keyboard formats is converted to a standard for the CPU via software. Status data for the LED and the audio indicators are stored in the custom integrated circuits Integrated Injection Logic (IIL) data latches. Data are transmitted from the μP to the chip on a SPI interface bus.

1.3 Statement of the Custom IC

This report describes the design of the custom integrated circuit used with the microprocessor in the keyboard computer interface application. The chip is powered by a 12 volt digital supply from the computer, provides a regulated 5 volt output for the microprocessor, and converts the TTL keyboard signals to RS423 levels and the RS423 levels to TTL. This chip also contains the four 12 milliampere LED current sources, the 70 milliampere maximum, digitally level controlled 2048 Hz toggled current source, and a +DC to -DC voltage converter to generate the voltage for the RS423 negative level. The 2048 Hz is produced by an on-chip squarewave generator that is also used to drive the charge pump for the negative voltage generator.

A block diagram for the IC version of the custom chip is shown in Fig. 1.2, and the initial design specifications are listed in Table 1.2.

The initial goal was to contain all the functions in a single die under 12,000 square mils, due die cost considerations, and to allow it to fit into the cavity of a high volume 20 pin, low cost dual-in-line plastic package, that was readily available.

1.4 Circuit Design and Analysis Procedure

The initial concept for the project was first functionally constructed using another custom IC and standard components, as illustrated in Fig. 1.3. Although it was quite a bit different from the final IC, it was useful in the preliminary system evaluation.

An equivalent schematic for the custom chip is shown in Fig. 1.4, and a microphotograph is shown in Fig. 1.5 to provide an overall indication of the complexity of the chip.

The circuit was designed and verified with basic calculations, breadboard analysis, and computer simulation. An example with SPICE analysis is contained in Appendix D.

A breadboard was constructed with individual transistors from kit parts that were made with the same process used to fabricate the complete chip, although a complete cell of a D-Flip Flop was available in the kit parts. It was modified to perform the serial-to-parallel and buffer latch function as shown in Fig. 1.6. Structures available from the kit parts are shown in Fig. 1.7.

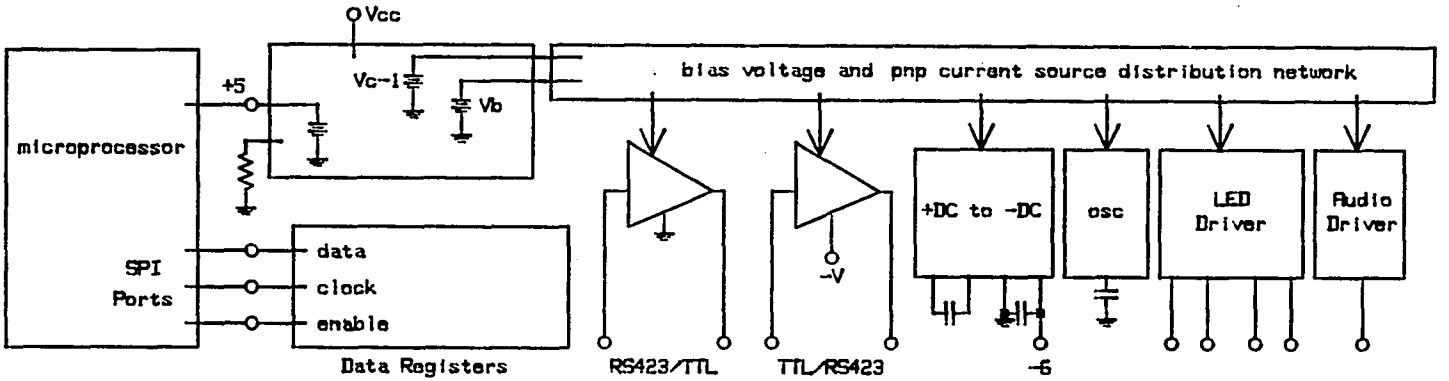


Fig. 1.2 Basic Block Diagram of the Custom Chip

Table 1.2 Initial Custom Chip Design Specifications

Temperature = 27°C

R_{set} = 4530 ohms

C_{ext} = .027 µF

$C_1 = C_2$ = 10 µF

C_{bypass} = .1 µF

V_{in} = 12 volts ± 20%

V_o	Output Voltage (I_o = 0 to 10 mA)	4.7 - 5.3 volts
I_{LED}	LED Currents (V_{LED} = 4 volts)	8.8 - 13.2 (mA)
I_{audio}	Audio Currents (V_{audio} = 4 volts)	± 12%

Digital Code: A_3, A_2, A_1, A_o
X = Don't Care

	(mA)
000X	0.0
1001	6.0
0100	9.0
1100	12.0
0101	17.9
1101	23.9
0110	32.9
0011	47.8
1111	71.7

F osc	Audio Oscillator Rate	2048 ± 12%
F data	Clock, Data, Enable Data Rate	500 kHz min
TTL in	TTL Input Level Thresholds	.8/2.0 volts min/max
TTL out	TTL Output Level Thresholds	.4/2.4 volts max/min

Table 1.2 (Continued)

RS423-in	RS423 Input Level Thresholds	0 volts $\pm$ 200 mV
RS423-out	Rise and Fall Times	20 µs < t_f < 50 µs
P_d	Chip Power Dissipation	372 mW max quiescent

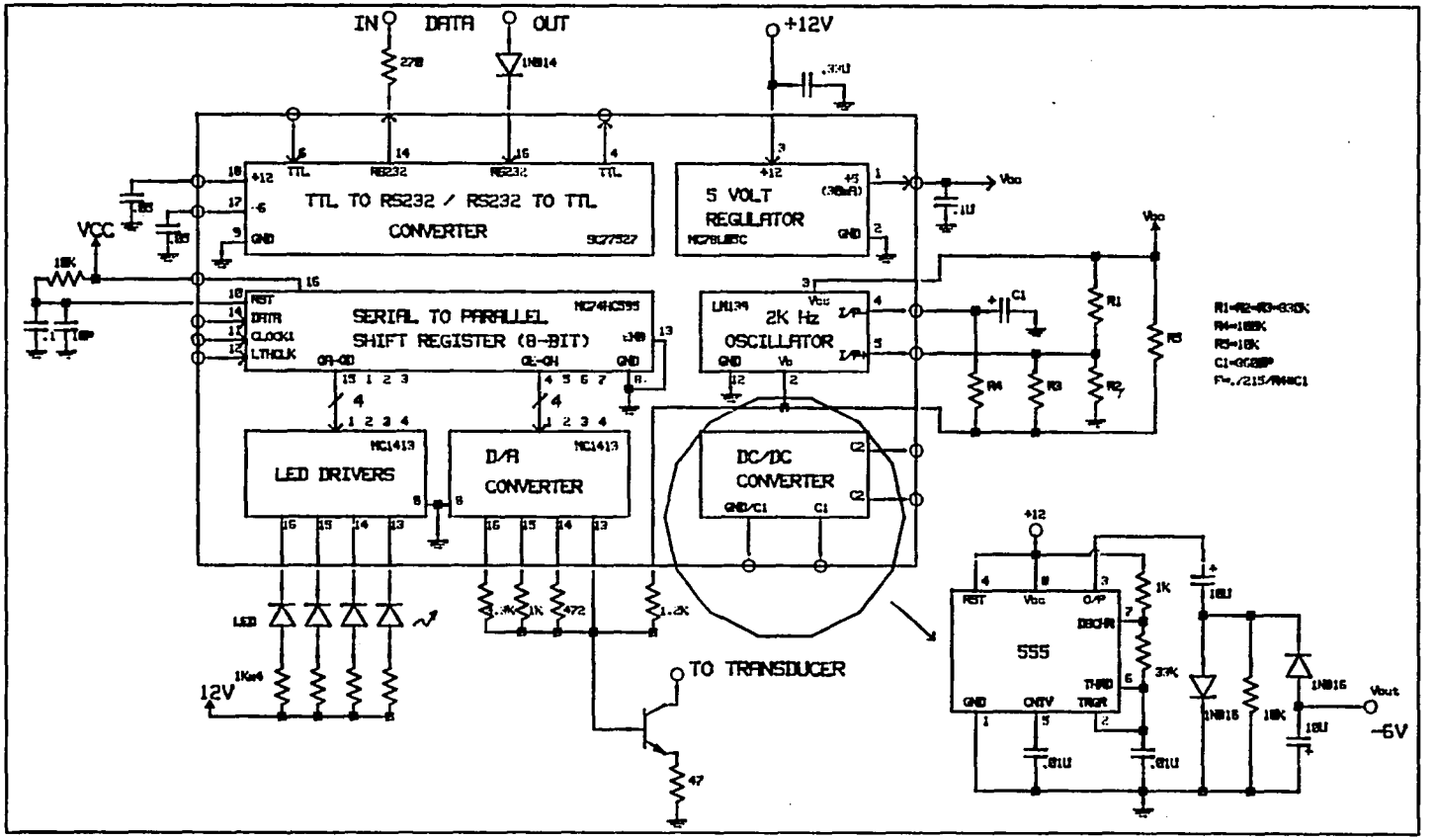


Fig. 1.3 Functional Breadboard Equivalent

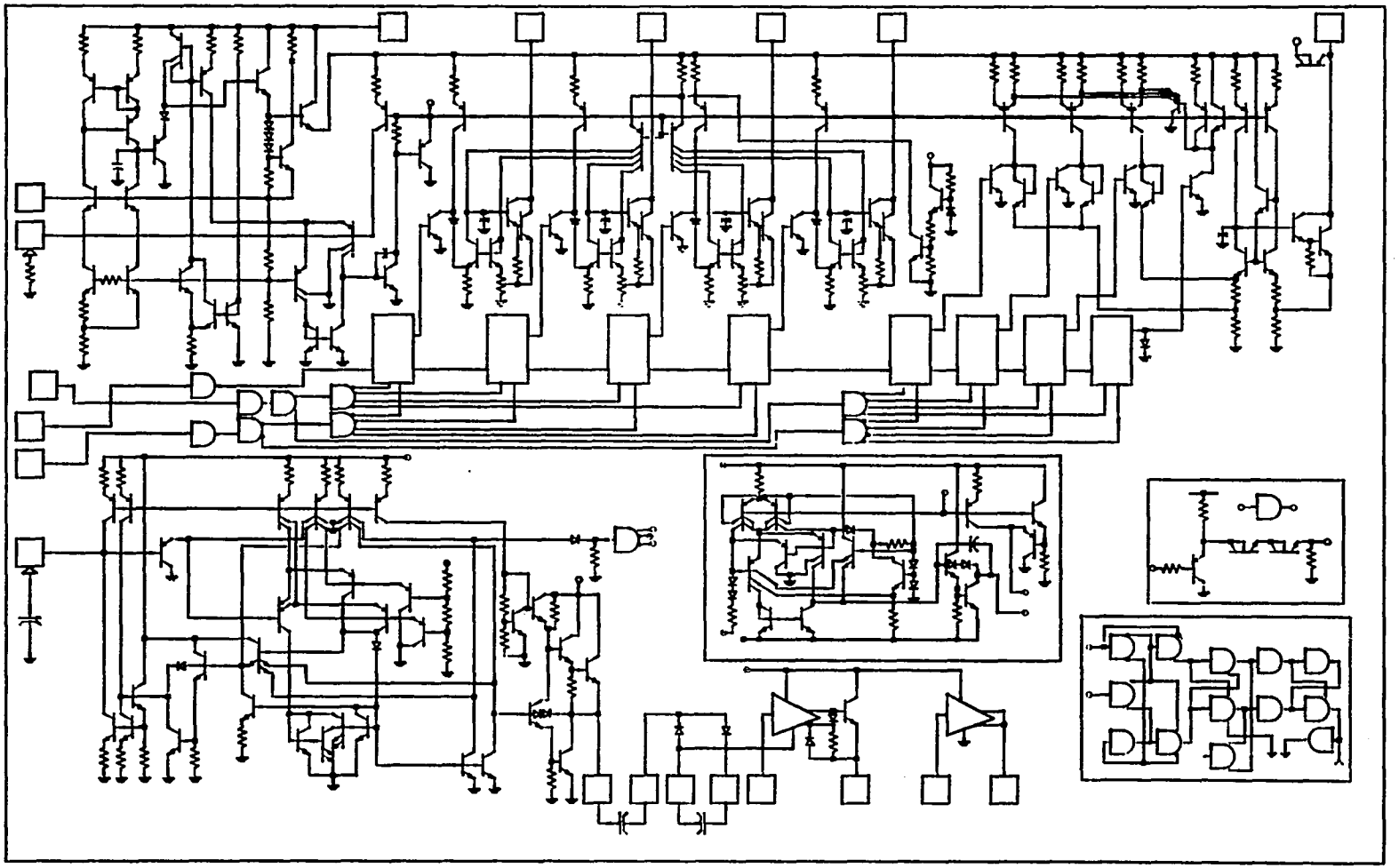


Fig. 1.4 Complete IC Equivalent Schematic

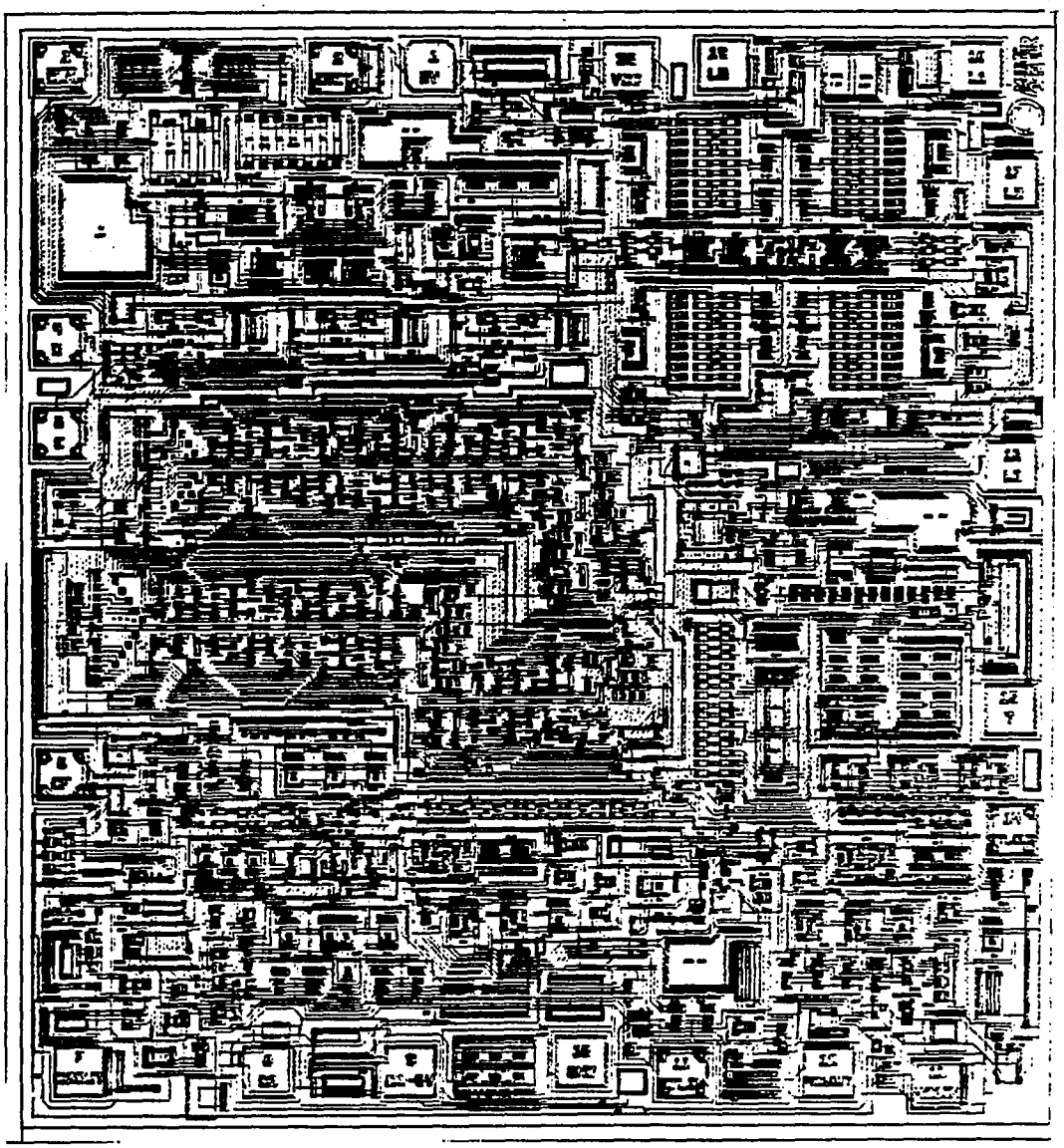


Fig. 1.5 Die Microphotograph of the Custom IC

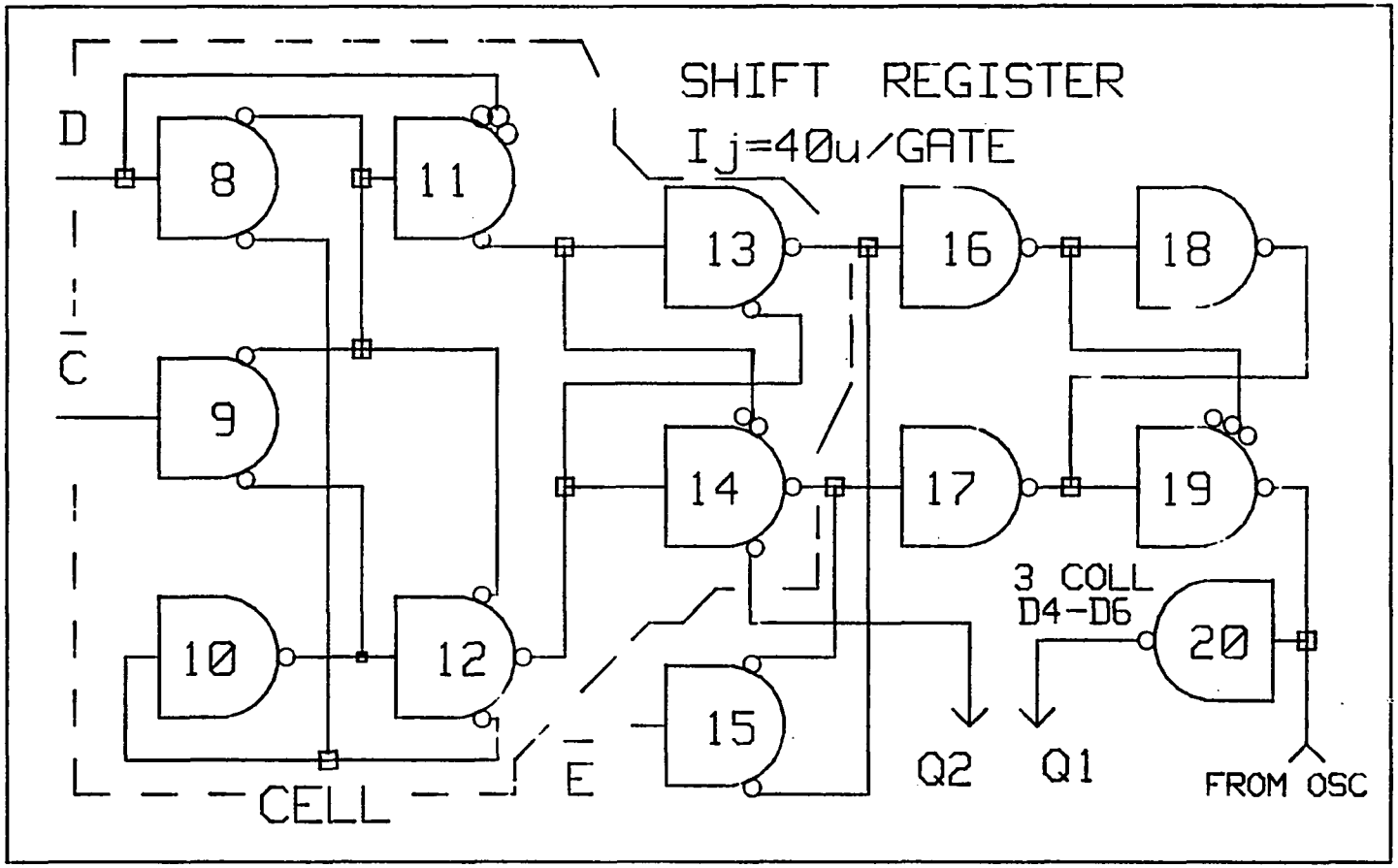


Fig. 1.6 Shift Register and Buffer Latch

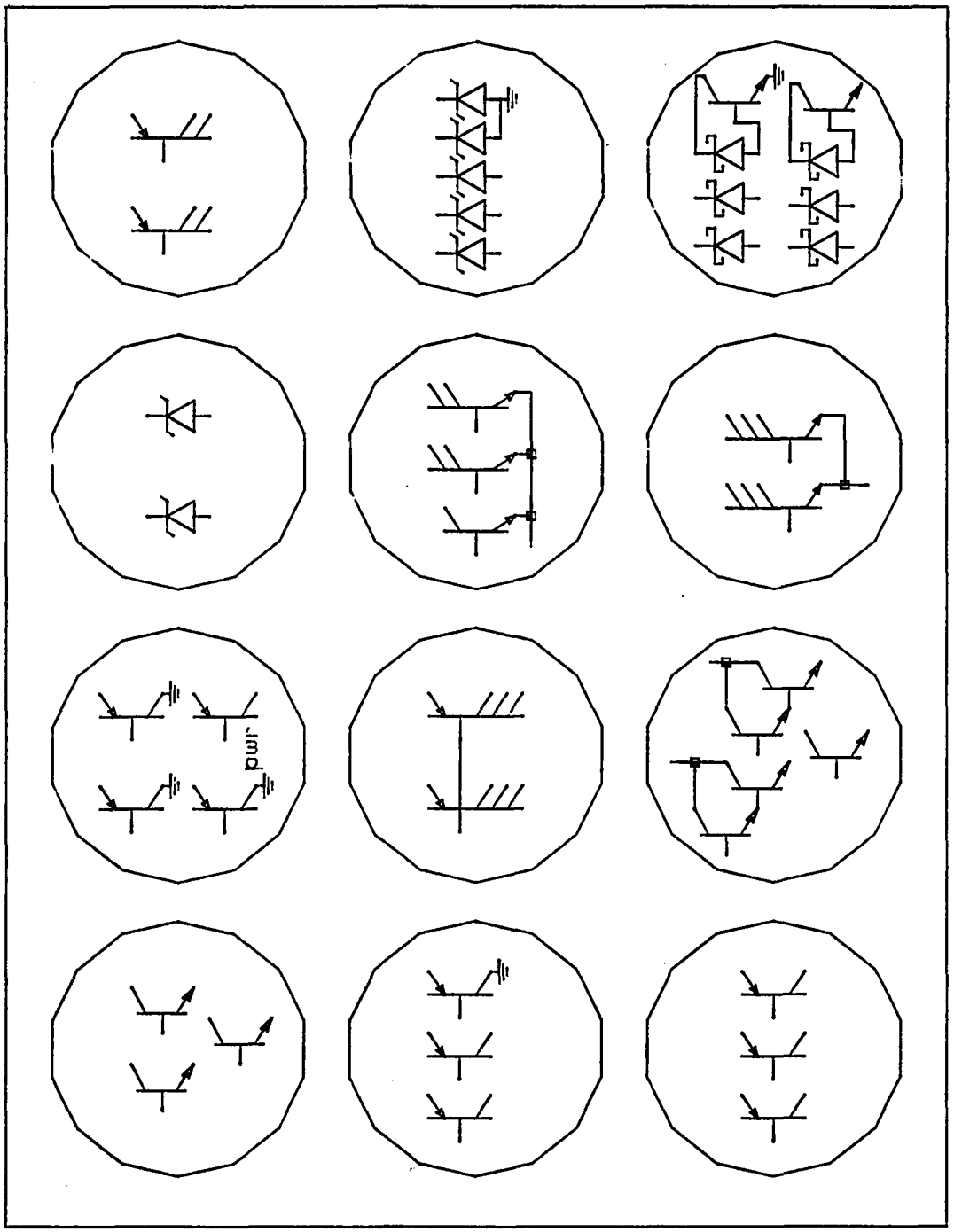


Fig. 1.7 Breadboard Devices

1.5 General Results

The custom IC has been designed, computer simulated, breadboarded, manufactured, and characterized. As is true with almost any engineering project, there are always a few things one would do differently if given the opportunity, but overall, the device accomplishes the desired tasks as initially proposed. Some small changes will be made to the layout to adjust parametrics, but no major modifications are required.

The +DC to -DC voltage converter developed the right voltage level under no-load conditions, but has slightly poorer load regulation than predicated. The problem has been traced to the improper modeling of the parasitic resistances used for the catch diodes and the TTL output stage driving the charge pump. Values have been modified and new computer simulations run. Synthesized data are now very close to what the IC is actually producing, which is acceptable. One would have thought the problem would have been noticed during the breadboard evaluation, but because the geometries for the breadboard transistors used in the charge pump were different from the geometries used for the layout, the problem was not detected. Actually, several transistors were placed in parallel to make up the larger structure for the breadboard because devices that large were not available from the kit parts, while one structure was used for the layout. At this point in time the initial design is going to production and the part will be sold to a major computer manufacturer. The modified layout will replace the first-pass layout as soon as it is available for production.

1.6 Development of the Report

Chapter 2 contains a short process description. Then, each of the functional blocks are described in Chapter 3. First, a functional basic concept is presented and described for each function: LED current source, audio driver, squarewave generator, data level transistors, data registers, and the voltage regulator and chip bias network. Following each explanation of the basic configuration are brief descriptions of the actual circuit used, and with refinements that make it either perform better or make it more "integratable".

Appendices are used to present discussions whose length or detail would detract from the main body of the manuscript. Emitter sizing and ratioing with emitter degeneration are reviewed in Appendix A; pnp collector splitting and ratioing in Appendix B; transistor beta and collector-to-emitter voltage considerations in Appendix C; and an example of SPICE modeling and simulation is given in Appendix D.

A die photo with each functional block labeled "a" through "g" is presented in Appendix E.

CHAPTER 2

PROCESS TECHNOLOGY

A 20 volt bipolar process was used to fabricate the circuit because it could provide devices with good matching characteristics and high transconductance. The LED and transducer current drive requirements could be achieved with smaller bipolar transistors than with MOS transistors, and the small amount of digital function could be accomplished with the IIL.

The process provides npn transistors with beta values that can range from a minimum of 80 to sometimes over 400. A value of 120 is typical and was used for the computer modeling. The pnp structures will typically have a beta range of 50 to 140, and usually 50 is used for calculations and simulations. Note that although a typical value is used, the circuits are simulated for the worst case minimum and maximum ranges. The inverted npn used in the IIL will typically have a beta of 2-3 with a four-collector gate.

Although resistors can be made with the epi layer and with the emitter diffusion, they were not used in this design, because they were not needed. Only the 125 ohms/square base diffusion and the 1000 ohms/square ion implanted resistor were used. The capacitors are constructed with a nitride structure yielding a capacitance of approximately .33 pF per square mil.

Key device parameters of the process are given in Table 2.1, and a drawing of a minimum npn is provided in Fig. 2.1 to illustrate feature size. For comparison, typical industry standard bipolar device structure feature sizes with parameters are listed in Hamilton and Howard [1975].

Table 2.1 Typical Device Parameters

Epi Thickness - x_j	8.5 - 11 μm
Epi Concentration	1.5 - 2.3 ohm-cm
B. L. Sheet Resistance	20 ohms/square
Isolation Sheet Resistance	4 ohms/square
Deep N^+ Sheet Resistance	3 ohms/square
Base Sheet Resistance	125 ohms/square
Implant Resistor Sheet Resistance	1K ohms/square
Emitter Sheet Resistance	6.8 ohms/square
NPN BVCEO	> 18 volts
NPN BVEBO	6.7 volts
NPN HFE	100-300
PNP BVCEO	> 20 volts
PNP HFE	40-100
IIL Gate Beta	3-4

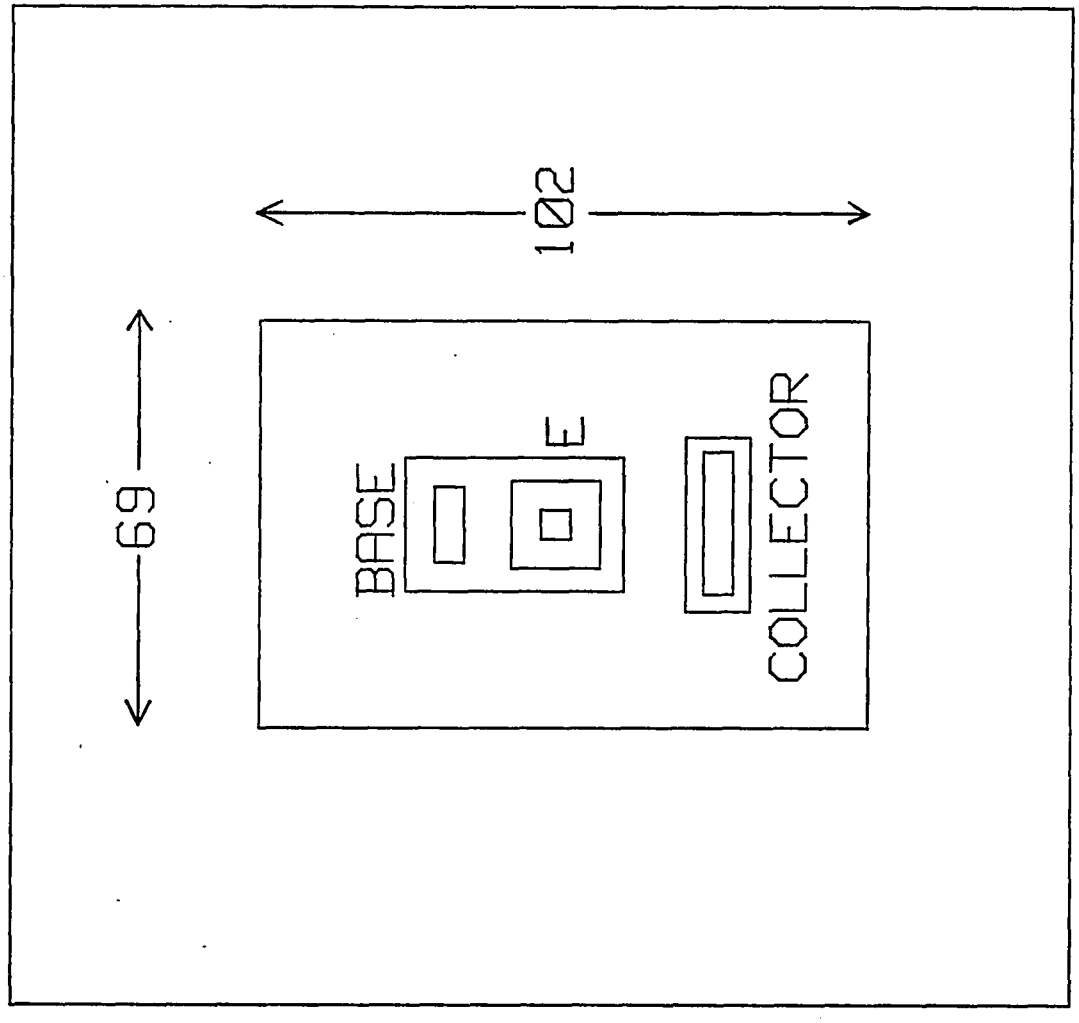


Fig. 2.1 Minimum Geometry NPN

CHAPTER 3

FUNCTIONAL BLOCK DESCRIPTION

3.1 LED Current Amplifier Concept

Current sources are used for the LED drivers so that a wide range of LEDs can be used with a variety of supply voltages, without a significant LED brightness variation. The basic concept used is shown in Fig. 3.1 and is a mirror configuration using an emitter scaling technique and a darlington output. The circuit amplifies a 272 μA reference current to a nominal output current of 12 milliamperes. The method helps keep quiescent current drain low when the output is OFF. This is important because most of the time the LED is OFF. The circuit contains equal-valued tapped emitter resistors R_{101} and R_{102}, such that the larger section R_b is 44.4 times larger than the smaller section R_a. When the reference current IR is injected into the tap on the emitter resistor between R_a and R_b, Q_{101} will be de-biased causing the bias current I_b to drive the darlington output pair $Q_{103/104}$, until the current I_o' develops the same voltage at the tap of the emitter resistor of Q_{102}. Since the IR voltage drop across the smaller section R_a will require 44.4 times the current for a balanced condition, an output current that is approximately 44.4 times the reference current results, thus producing 12 mA.

Looking at the equations to a first order approximation, we have

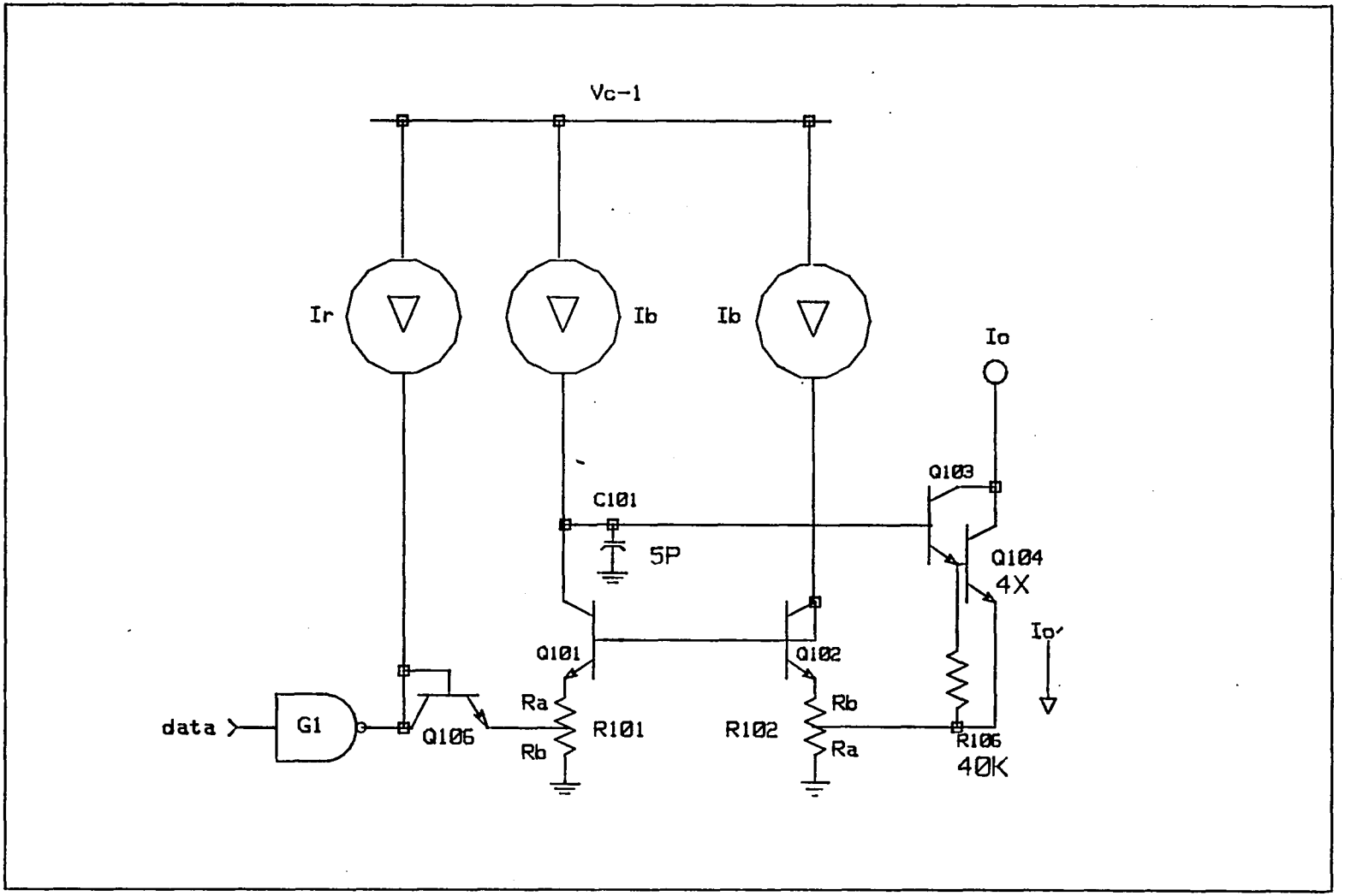


Fig. 3.1 LED Current Amplifier Concept

$$I_B R_a + (I_B + I_R)\, R_b = I_B R_b + (I_B + I_o')\, R_a$$

$$I_B R_a + I_B R_b + I_R R_b = I_B R_b + I_B R_a + I_o' R_a$$

$$I_R R_b = I_o' R_a$$

$$I_o' = I_R R_b / R_a \qquad (3.1)$$

Switching the current to an OFF condition is accomplished by steering the reference current away from the R_{101} tapped resistor with diode Q_{106} and IIL gate, G_1.

Since a feedback loop exists with this configuration, it must be compensated with capacitor C_{101}. The 5 pF capacitor establishes a unity frequency at

$$f_u = g_m / 2\pi \cdot C_{101}$$

$$= (34E\text{-}6)(38.5)/(2\pi)(5E\text{-}12)$$

$$\approx 41 \text{ MHz} \qquad (3.2)$$

3.2 IC Implementation of the LED Current Amplifier

The LED amplifiers as implemented on the die are shown in Fig. 3.2. In order to conserve die area the mirror bias currents were established with "segmented pnp collectors" which divide the approximately 272 μA of reference current into eight currents of about 34 μA

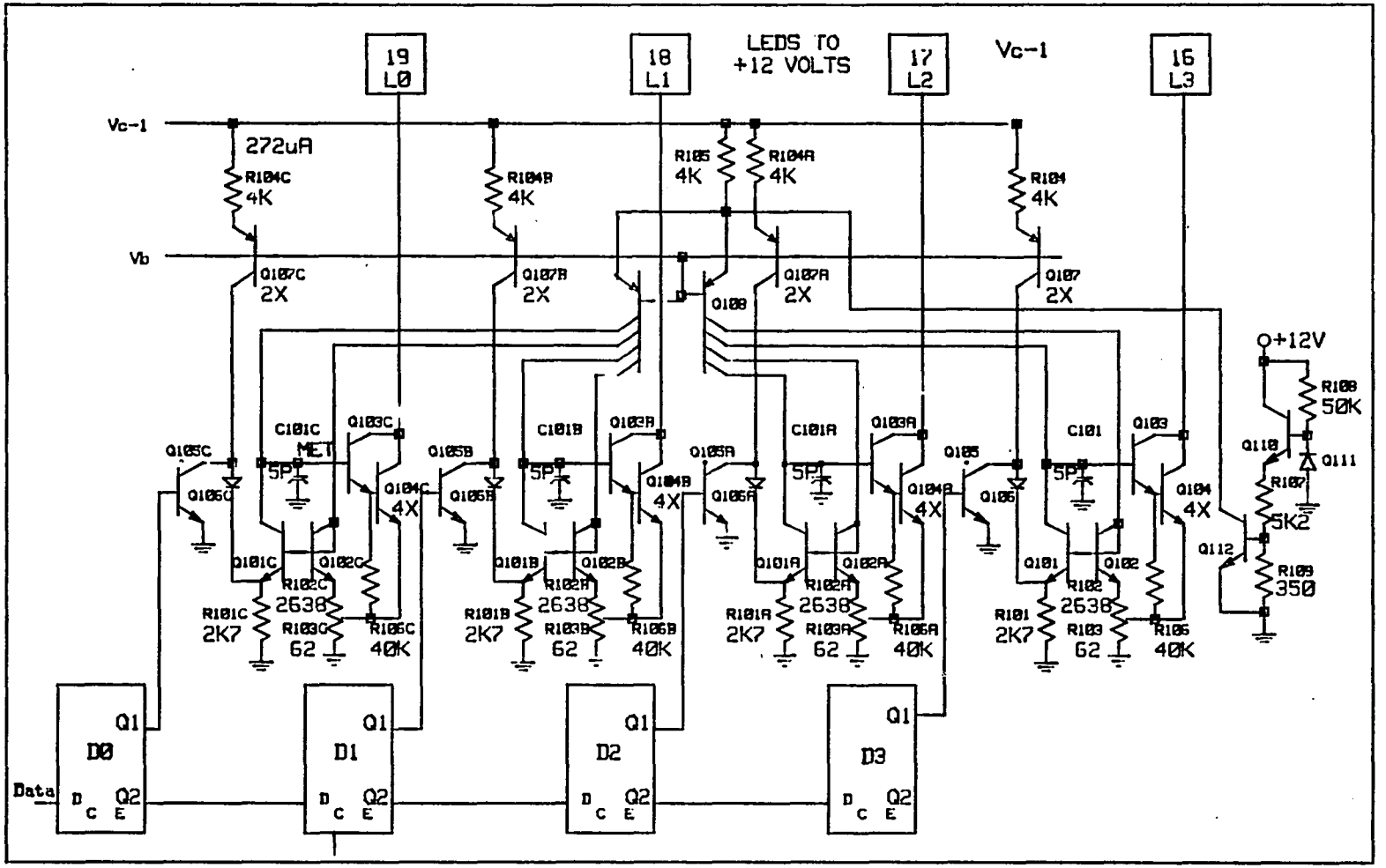


Fig. 3.2 IC Equivalent Schematic of Current Sources

each. (See Appendix B.) The current sources are cut off if the power dissipation of the die reaches a particular level. If the LED current sources are ON at a maximum condition and the audio amplifier is ON at its maximum rate, the power dissipation can heat the die to a temperature greater than 170°C, a condition that is not desirable because it can degrade the integrity of the IC over time. In order to keep the die from reaching this mode, a circuit (shown in Fig. 3.3) consisting of Q_{110}, Q_{108}, Q_{112}, R_{107}, R_{108}, and R_{109} sense die temperature and at the 170°C point, cut off the current sources feeding the current mirrors, reducing the output current, thus reducing the power dissipation and the temperature.

For a quick approximation of how the circuit works, consider that the voltage at the base of $Q_{112}(V')$ is equal to

$$V' = (V_z - V_{be})R_{109}/(R_{107} + R_{109}) \qquad (3.3)$$

At conduction

$$V' = V_{be}$$

and, by substitution

$$R_{109}/(R_{107} + R_{109}) = V_{be}/(V_z - V_{be})$$

$$V' = V_z/(V_{be} - 1) \qquad (3.4)$$

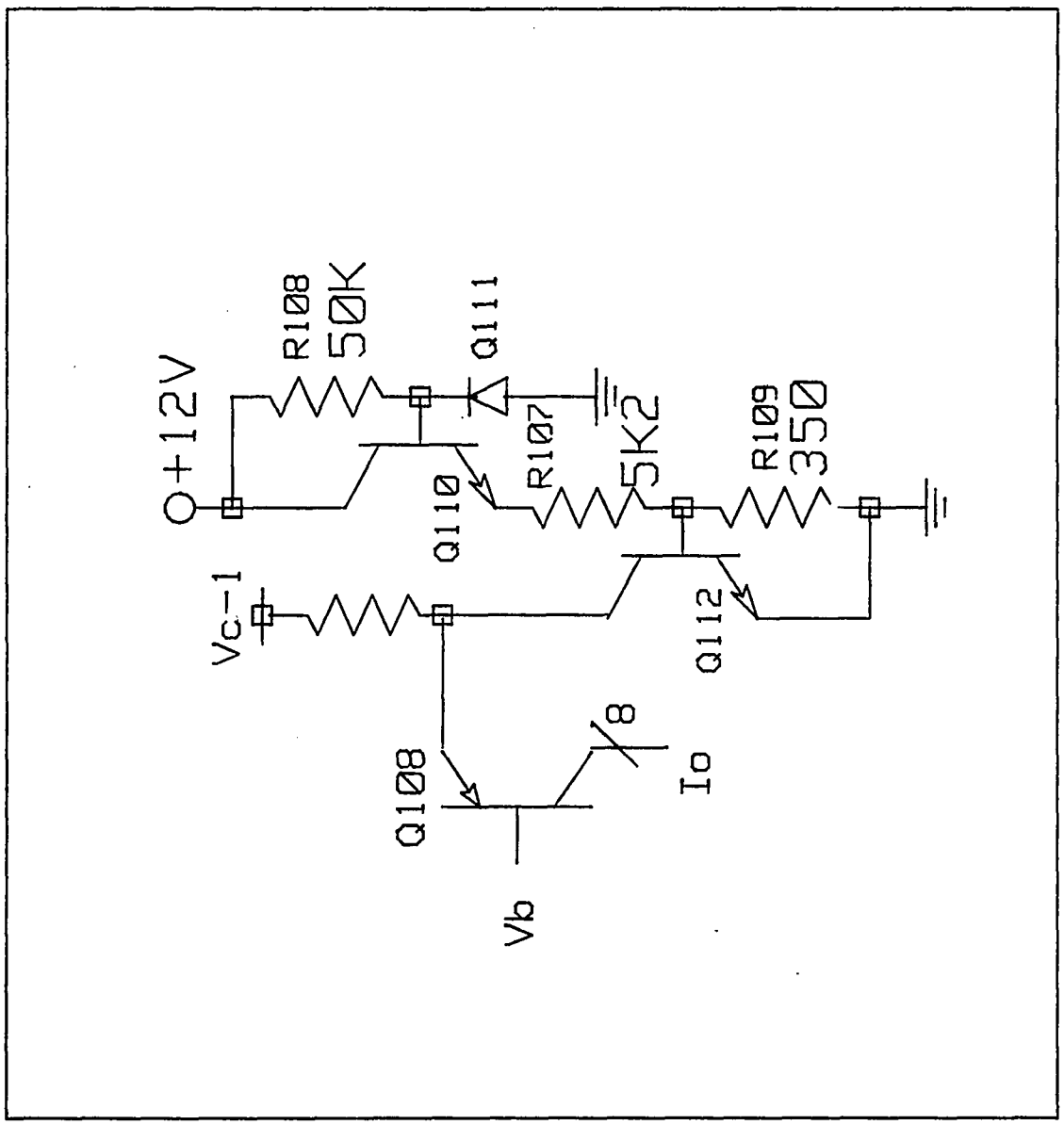


Fig. 3.3 Die Temperature Sense Circuit

Considering the temperature characteristics of the zener V_z and the V_{be} voltages, and letting V_z and V_{be} equal

$$V_z(T) = V_z[1 + \alpha_z (T - T_o)] \tag{3.6}$$

$$V_{be}(T) = V_{be}[1 + \alpha_{V_{be}} (T - T_o)] \tag{3.7}$$

where α_z is the temperature coefficient for the zener and $\alpha_{V_{be}}$ is the temperature coefficient for V_{be}, T = 170°C, and T_o = 25°C. Putting the temperature-dependent values into Eq. (3.4) and solving with a TC of 1.8 mV for the zener and -2.2 mV for the diode, the ratio for $R_{107} + R_{109}$ to R_{109} was determined to be around 17. A ratio of 15.9 was used because computer simulation which included more than first-order effects showed this to be a more appropriate value. Also note that the first order hand calculation was close, an indication that the simulations were probably correct. If the hand calculations were not performed and a poor model of data had been entered into the simulation model, bad results could have resulted.

A portion of the die photo with the four LED amplifiers is shown in Appendix E, Section a. The emitter resistors contained in the mirror can be easily identified. These are in a block of segmented small resistors that are interconnected in series and in parallel to make up the ratioed values R_a and R_b. The method produces good ratios because the secondary effects such as alignment tolerance, out-diffusion, and contact resistance all become ratios rather than

absolute values. This concept is shown in Fig. 3.4. As an example, consider that a resistor ratio of 6 was desired and it was obtained by using a resistor 6 times longer than the other as shown in Fig. 3.4, this ratio would be

$$\text{Ratio } \#1 = (6R + 2\ \Delta R)/(R + 2\ \Delta R) \tag{3.8}$$

where ΔR is the contact resistance. If the contact resistance was 15 ohms and a 6K and a 1K were ratioed, the ratio would be

$$6030/1030 = 5.85$$

For the segmented, interconnected scheme (Fig. 3.4), the ratio using 1000 ohm resistors would be

$$\text{Ratio } \#2 = (2R + 4\ \Delta R)/[(R + 2\ \Delta R)/3] \tag{3.9}$$

$$= [(2000 + 60)/(1000 + 30)/3] = 6$$

3.3 Audio Transducer Current Source

The Audio Current Source drives an electromechanical sound transducer which is used to produce synthesized key clicks and give audible status indications. The transducer is described in Fig. 3.5. Note that on the sound pressure level (SPL) versus frequency plot, the frequency peak is around 2048 Hz. To keep a consistent tone volume from unit to unit, it was important that the frequency was maintained to $\pm$ 12%. Therefore, more attention was given to the design of the

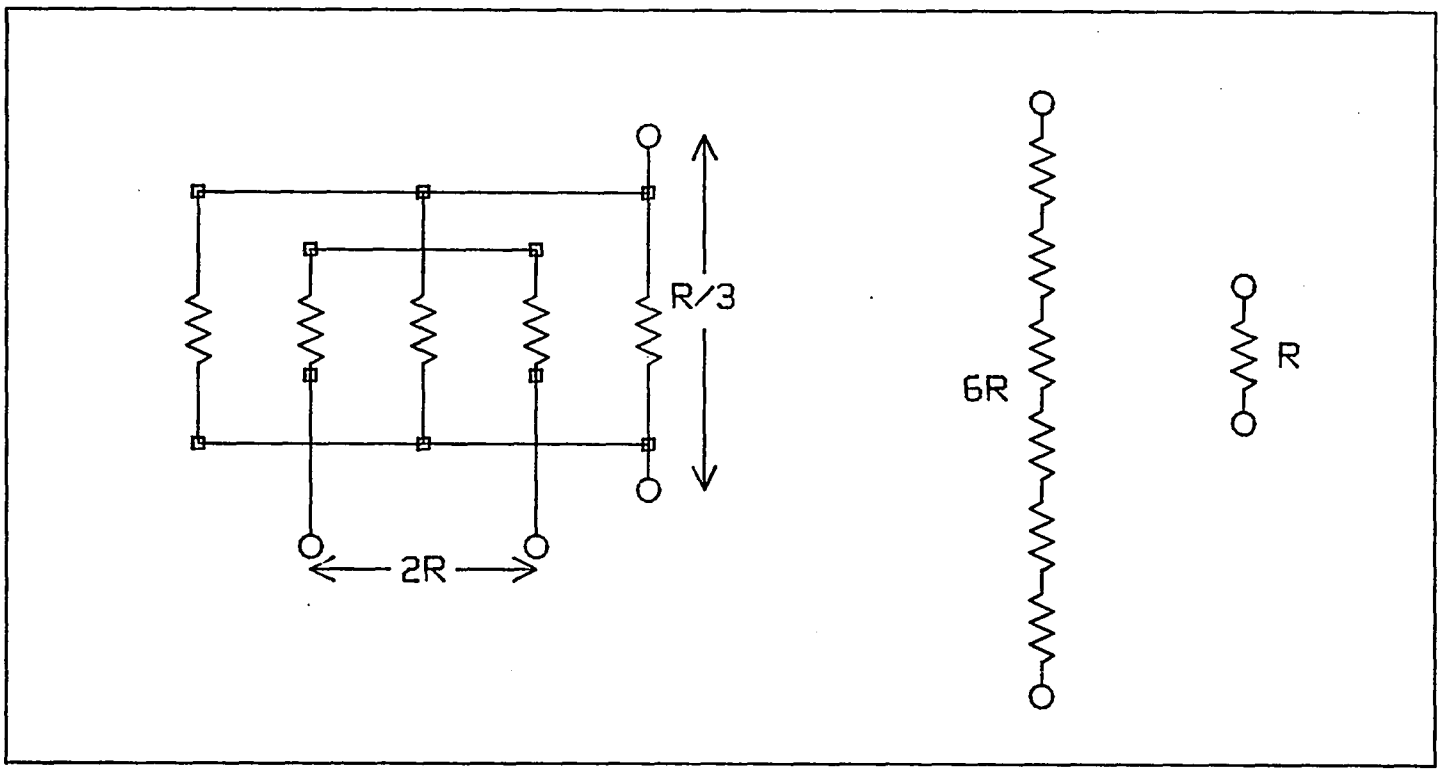


Fig. 3.4 Resistor Ratioing Technique

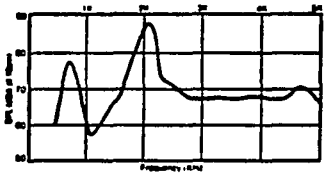
Series AT-01

Miniature Electro Magnetic Transducer

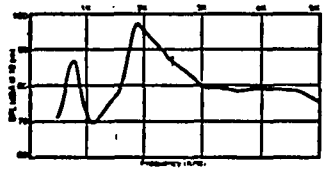
FEATURES:
- Small size and lightweight
- P.C. board mounting
- Wave solderable
- Three voltages available (1 to 3V., 4 to 9V. and 6 to 18V.) See overleaf.
- Low current drain
- Economically priced

The AT-01, AT-02 and AT-03 are electro-acoustic transducers that contain no electronics and transform AC voltages to sound pressure waves.

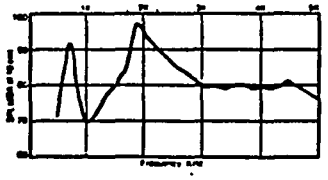
AT-01
SPL vs Frequency (1.5VP-P Symmetrical Square Wave Applied)



AT-02
SPL vs Frequency (6VP-P Symmetrical Square Wave Applied)



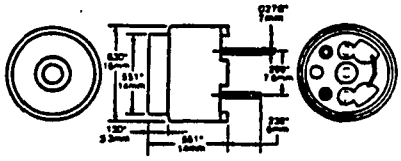
AT-03
SPL vs Frequency (12VP-P Symmetrical Square Wave Applied)



Specifications subject to change without notice.

AT-01 Actual Size

Dimensions-Series AT-01, AT-02 and AT-03



Case Black ABS.
P.C Pins Tin Plated Brass

Electrical Specifications

All data taken at 25°C unless otherwise specified

Parameter	AT-01*	AT-02*	AT-03*	Units
Rated Voltage	1.5	6	12	VP-P
Voltage Range	1-3V	4-9V	6-18V	VP-P
Resonant Freq.	2048	2048	2048	Hz
Frequency Range	1000-5000	1000-5000	1000-5000	Hz
Sound Output	Approximately 70 dBA at 6" (20 cm) at 2.1 KHz			dBA
Maximum Rated Current	20	80	80	mA
Operation Temp. Range	−20 to +70	−20 to +70	−20 to +70	°C

*Model numbers listed in bold print indicate units normally stocked in depth.

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ELECTRICAL CHARACTERISTICS

DIGITAL PART NUMBER	RATED VOLTAGE	OPERATING VOLTAGE	RATED CURRENT (MAXIMUM)	COIL IMPEDANCE
1217477-00	1.5V	1 To 3V	15 mA	165 Ohms
1217477-01	6V	3 To 12V	30 mA	260 Ohms
1217477-02	12V	6 To 18V	30 mA	430 Ohms

Fig. 3.5 Miniature Electro Magnetic Transducer

squarewave generator than was required to satisfy only the +DC to -DC charge pump function. The circuit for the transducer current source is given in Fig. 3.6, which is similar to the LED current source except for the output current, which has thirteen levels. Nine of these are used in this application to simulate approximately a logarithmic transfer function between the output current and the four-bit digital word from the microprocessor. The logarithmic characteristic is needed to compensate for behavior of the transducer and the way the ear interpolates changes in volume. The transfer function is tabulated and plotted versus the corresponding digital word in Fig. 3.7. The same scaling equation applies as was used for the LED current source

$$I_o = I_r R_b / R_a$$

The output is toggled at a 2048 Hz rate by the squarewave generator. The circuit as implemented on the integrated circuit is shown in Fig. 3.8 with the corresponding function of the die in Appendix E, Section b. The pnp Q_{310} on the output of the current source catches an inductively induced voltage from the transducer, clamping it to the V_{cc} supply. If this was not done, the output transistor may be degraded or even damaged because the spike might exceed the output transistors BV_{ceo} voltage in some situations.

3.4 Squarewave Generator

A squarewave generator on the chip provides the clock to the audio current source and also drives the +DC to -DC voltage converter.

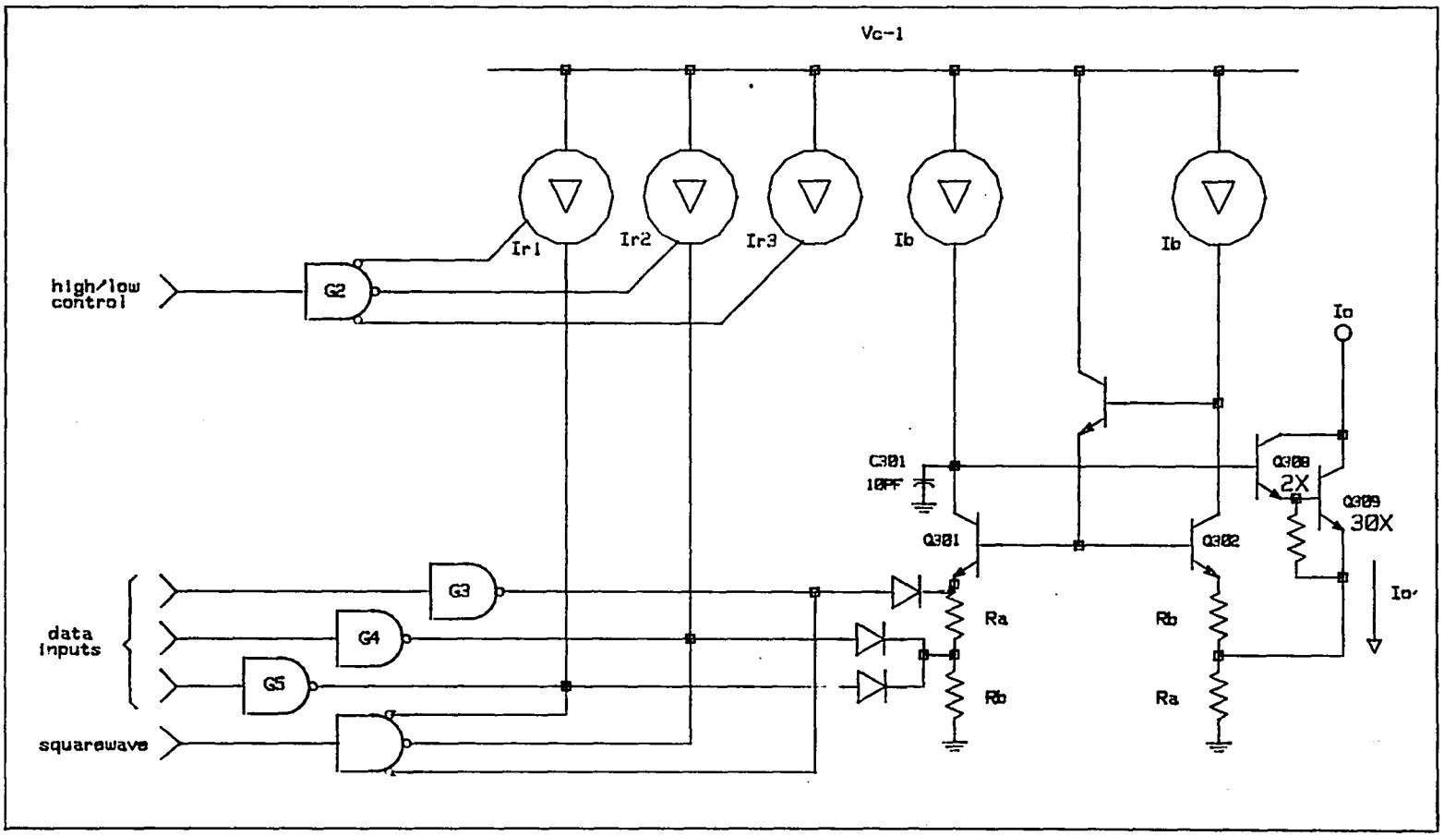

Fig. 3.6 Audio Transducer Current Amplifier Concept

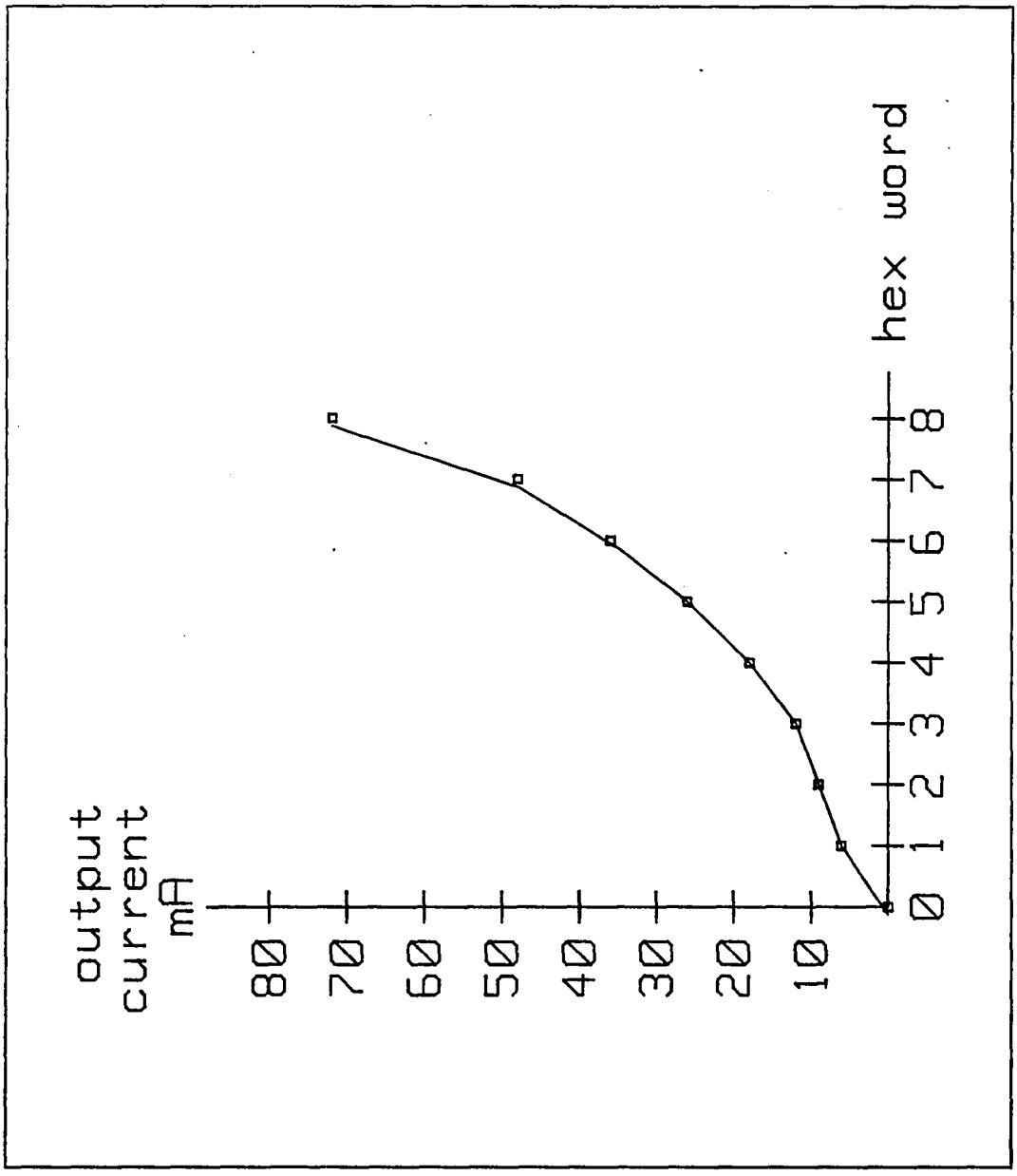

Fig. 3.7 Audio Current Output versus Digital Word

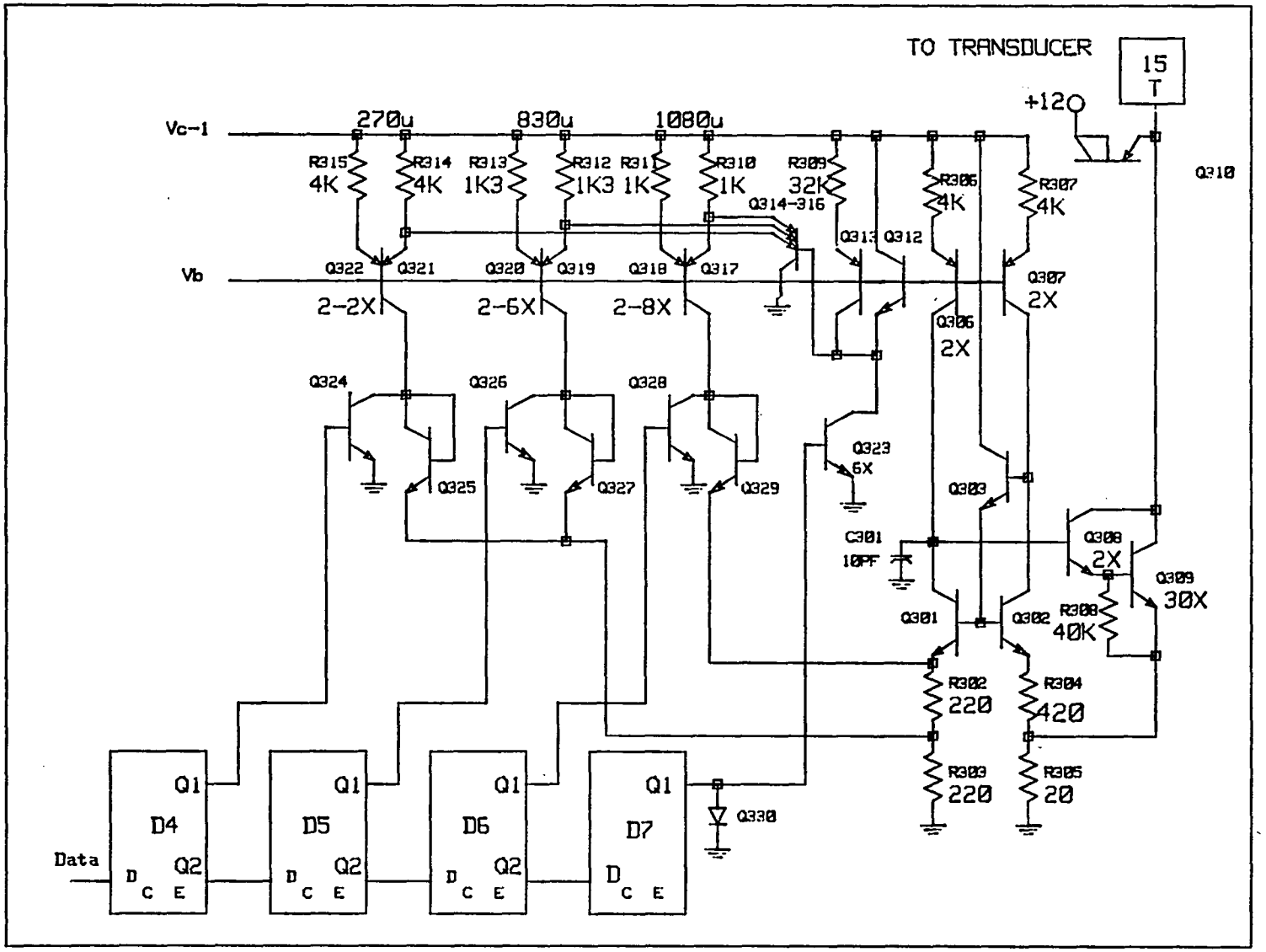

Fig. 3.8 IC Equivalent Schematic Audio Current Amplifier

The basic circuit concept is shown in Fig. 3.9. An I/2I current mirror, Q_{411}, Q_{412}, R_{408}, and R_{409}, ($R_{409} = 2R_{408}$), is fed with two equal current sources. The output of the current source is controlled with switch S_1. If S_1 is open, a current (I) will flow from the storage capacitor C_{ext}. If S_1 is closed, the mirror is turned off and current will flow into the capacitor C_{ext}. Switch S_1 is controlled by the state of the RS latch which is either set or reset by comparators comp-1 and comp-2. During operation the voltage on the capacitor will charge and discharge between two threshold voltages, V_a and V_b, that are established by a resistive divider across the 5-volt supply line V_{c-1}, as shown. The squarewave frequency is

$$\begin{aligned} f &= (I)/[2C(V_a - V_b)] \\ &= (136E\text{-}6)/[2(0.27\ \mu F)(1.23V)] \\ &= 2048\ Hz \end{aligned} \qquad (3.10)$$

Further circuit detail is shown in Fig. 3.10 on how the two comparators are constructed with a 2 emitter pnp transistor $Q_{406/7}$, Q_{408}, and Q_{409}. The latch is constructed with a cross-coupled I/2I current mirror Q_{415}, Q_{403}, Q_{404}, and Q_{416}, replacing the usual mirror found in a differential pnp gain stage [Miller, 1985]. Merging techniques like this were used to reduce silicon area.

A complete IC implementation of the squarewave generator is shown in Fig. 3.11. As is shown, a little refinement was added to the

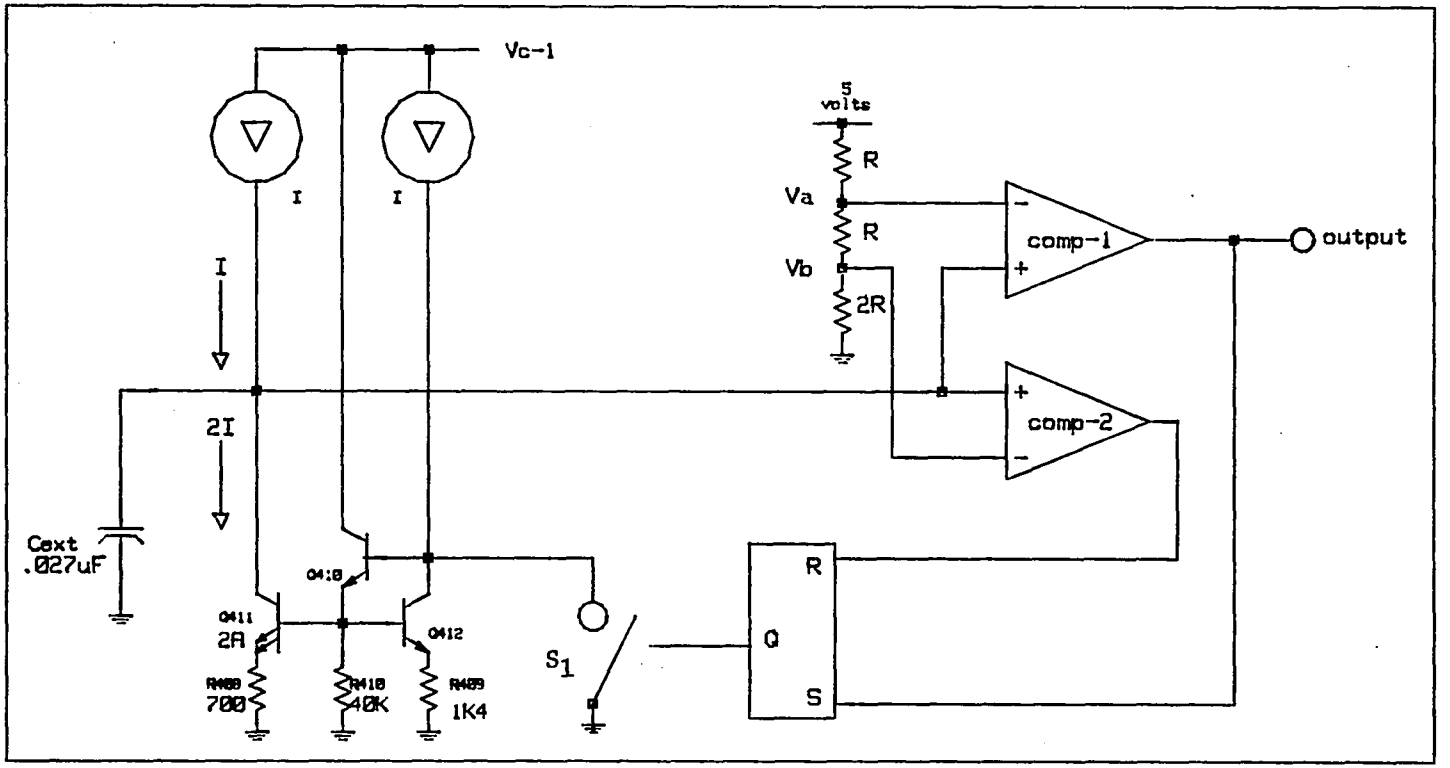

Fig. 3.9 Squarewave Generator Concept

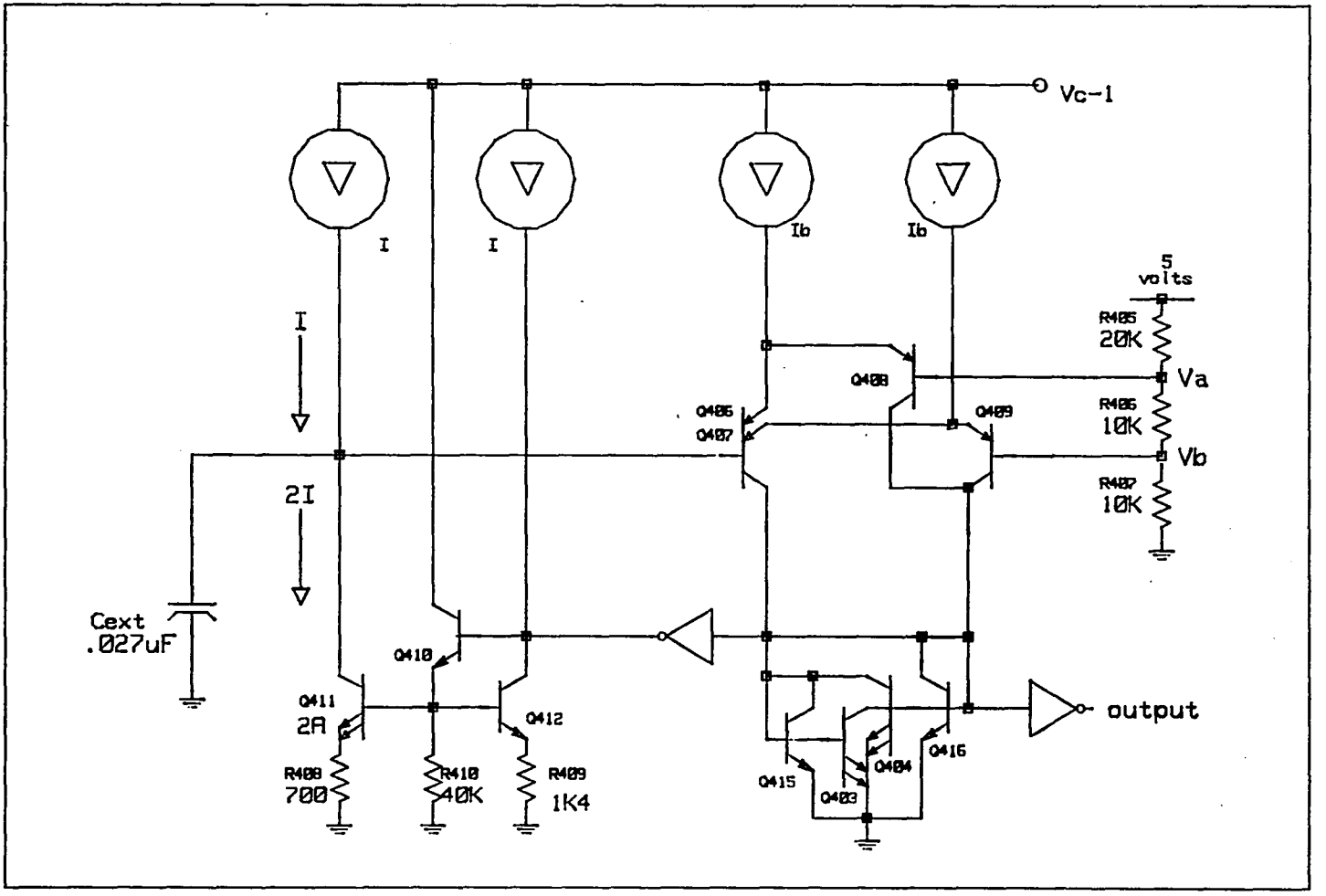

Fig. 3.10 Merged Squarewave Generator Concept

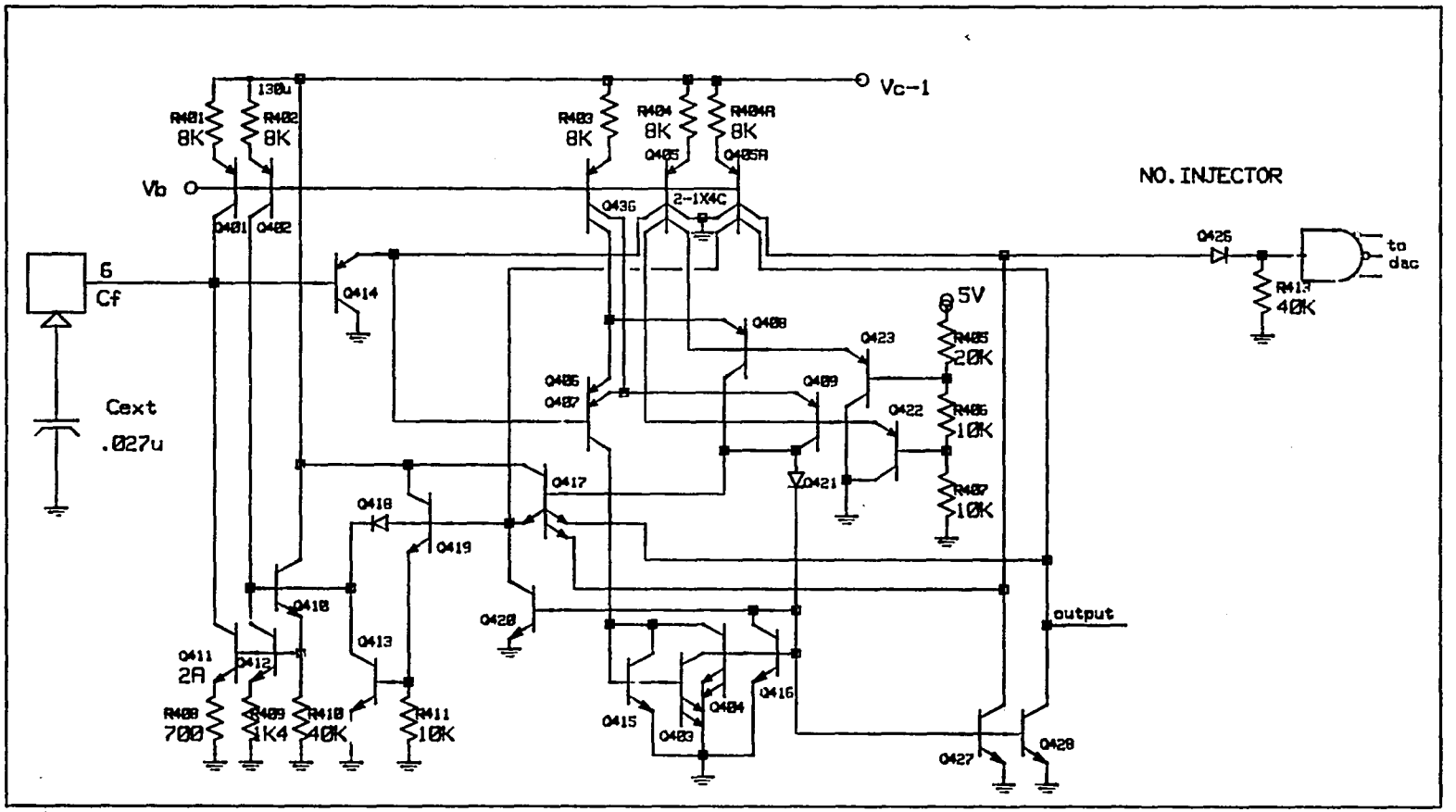

Fig. 3.11 IC Equivalent Schematic of Squarewave Generator

basic circuit to improve performance. For example, buffers were added to the comparator inputs and clamps were added to keep transistors from reaching a saturated condition, which could degrade the frequency accuracy. The clamp also prevents substrate injection that accompanies a heavily saturated transistor. Care was taken in the design to keep substrate injection to a mimimum because the substrate voltage is generated by the +DC to -DC voltage generator. Until the squarewave generator has had time to go through a few cycles during initial turn ON, there is no substrate bias. The section of the die containing the circuit is shown in Appendix E, Section c.

3.5 Negative Voltage Generator

The negative voltage for the low level of the RS423 output is generated with a simple charge pump circuit driven by the squarewave generator through a modified TTL output stage. The basic concept is shown in Fig. 3.12. The phase splitting transistor Q_{431} is driven by the 2048 Hz squarewave. Q_{431} is called a phase splitter because it turns the pull-down transistor Q_{434} ON and OFF opposite to when it turns the darlington pair pull-up transistors $Q_{432/433}$ ON and OFF. The collector of Q_{434} is held out of hard saturation by the clamp diodes Q_{429} and Q_{430} to avoid switching delays and substrate injection. Q_{431} is clamped by Q_{425}, whose base is connected to a V_{be} multiplier circuit Q_{424}, R_{419}, and R_{420}. The voltage at the base of Q_{424} is equal to

$$V_{be}(1 + R_{419}/R_{420})$$

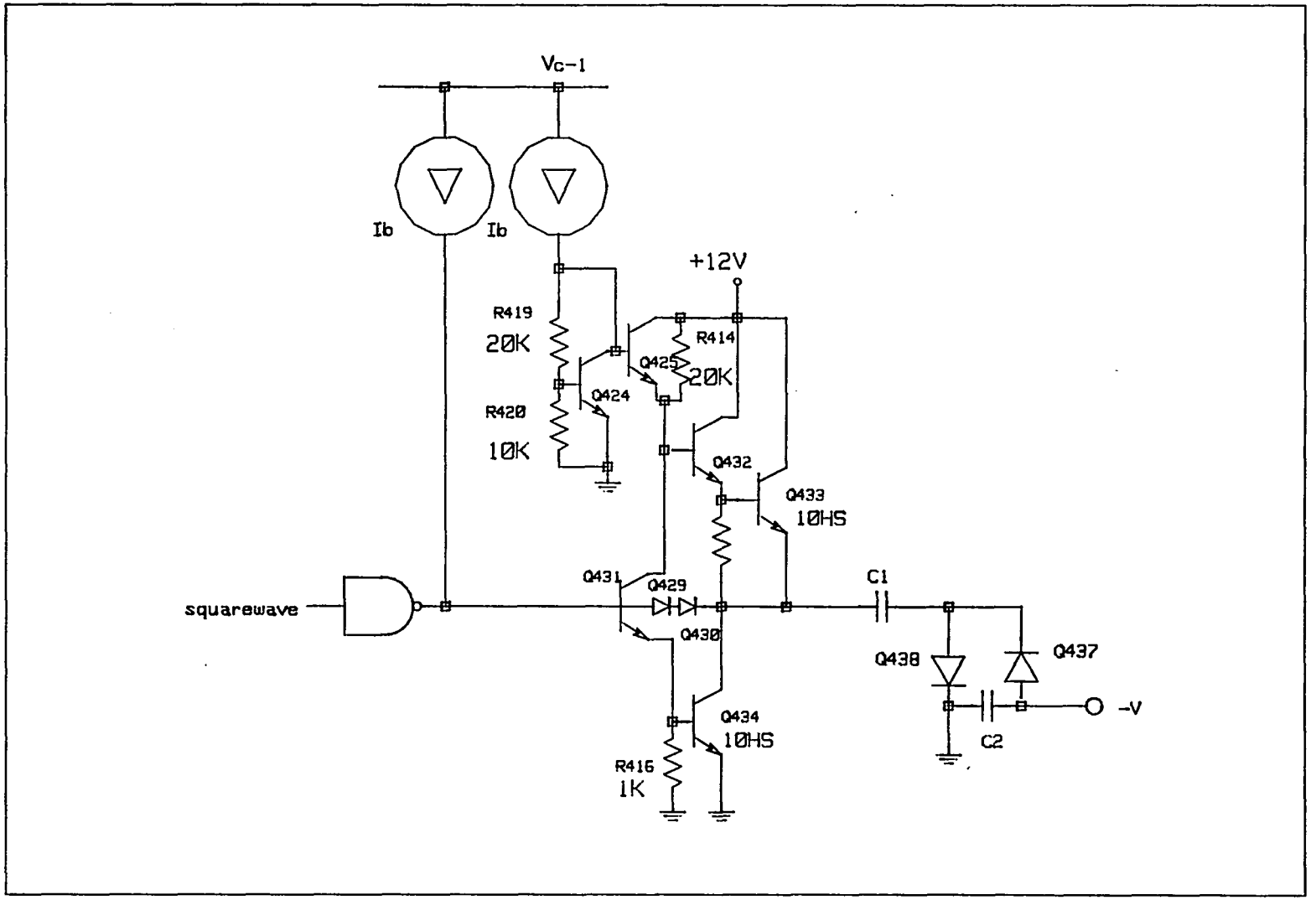

Fig. 3.12 Negative Charge Pump Concept

During the positive swing the emitter-base junction of Q_{425} will reverse bias, clamping the output voltage of the drive to a voltage $BV_{beo} + BV_{ebo}$. This was done to prevent the catch diode Q_{437} from breaking down during positive swings.

During the positive swing of the driver (Fig. 3.13), the external capacitor C_1 is charged to approximately 6.7 volts, which is the typical BV_{ebo} voltage, through the pull-up transistors $Q_{432/433}$, and the pnp diode connected transistor Q_{438}. When the driver goes low, it will pull the capacitor near ground transferring the charge to the external capacitor C_2, through the pull-down transistor Q_{434} and the diode-connected transistor Q_{437}. (See Figure 3.13a and 3.13b.) It was important to use the right diode configuration so as to avoid a forward-biased epi to substrate condition. Such a condition would cause injection into the substrate during the complete charge cycle (Fig. 3.14). If heavy injection was allowed to occur, it could cause the chip to latch rendering it inoperative.

The no-load voltage produced by the circuit is

$$-V = -BV_{ebo} + V_{be} = 6.7 - .7 = 6 \text{ volts} \qquad (3.11)$$

and the ripple is

$$\begin{aligned} V \text{ ripple} &= R_L T_{OFF}/C_2 \\ &= (6 \text{ volts} \cdot 0.25 \text{ mS})/470 \cdot 10 \text{ } \mu\text{F} \\ &= 319 \text{ mV} \end{aligned} \qquad (3.12)$$

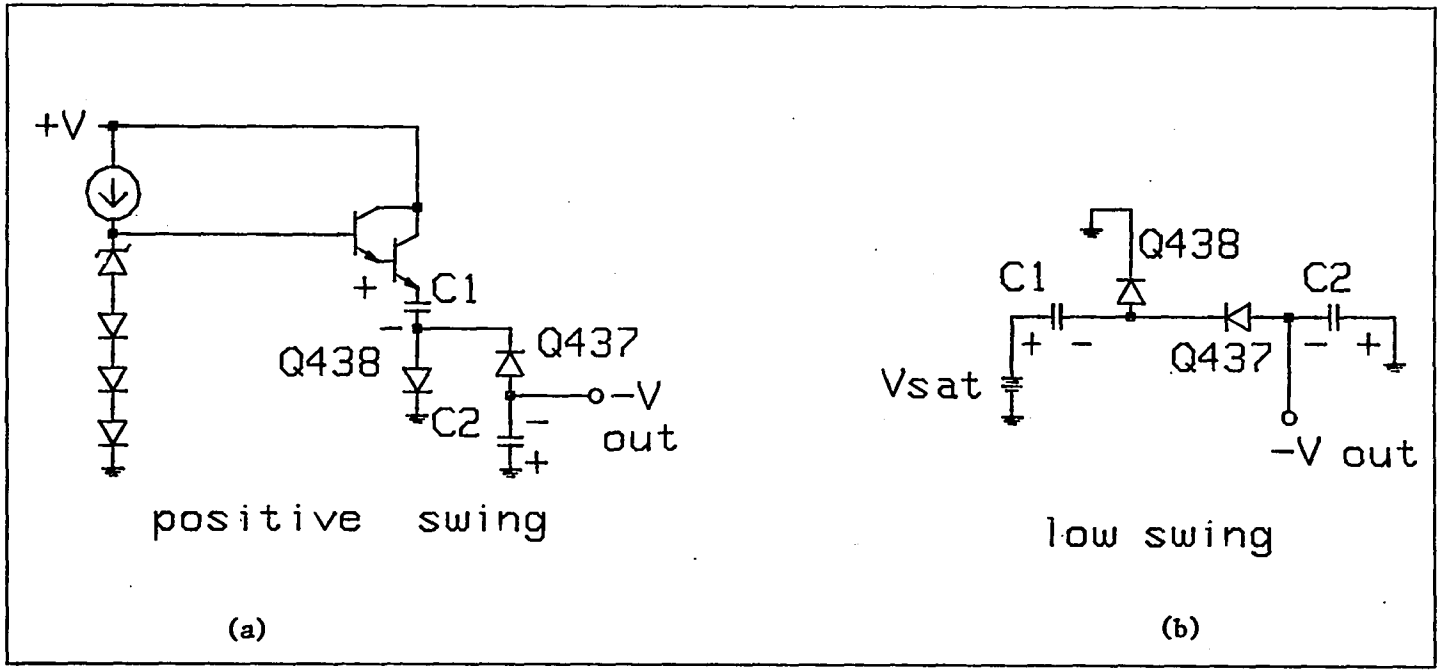

Fig. 3.13 Charge Pump Clamp Voltages

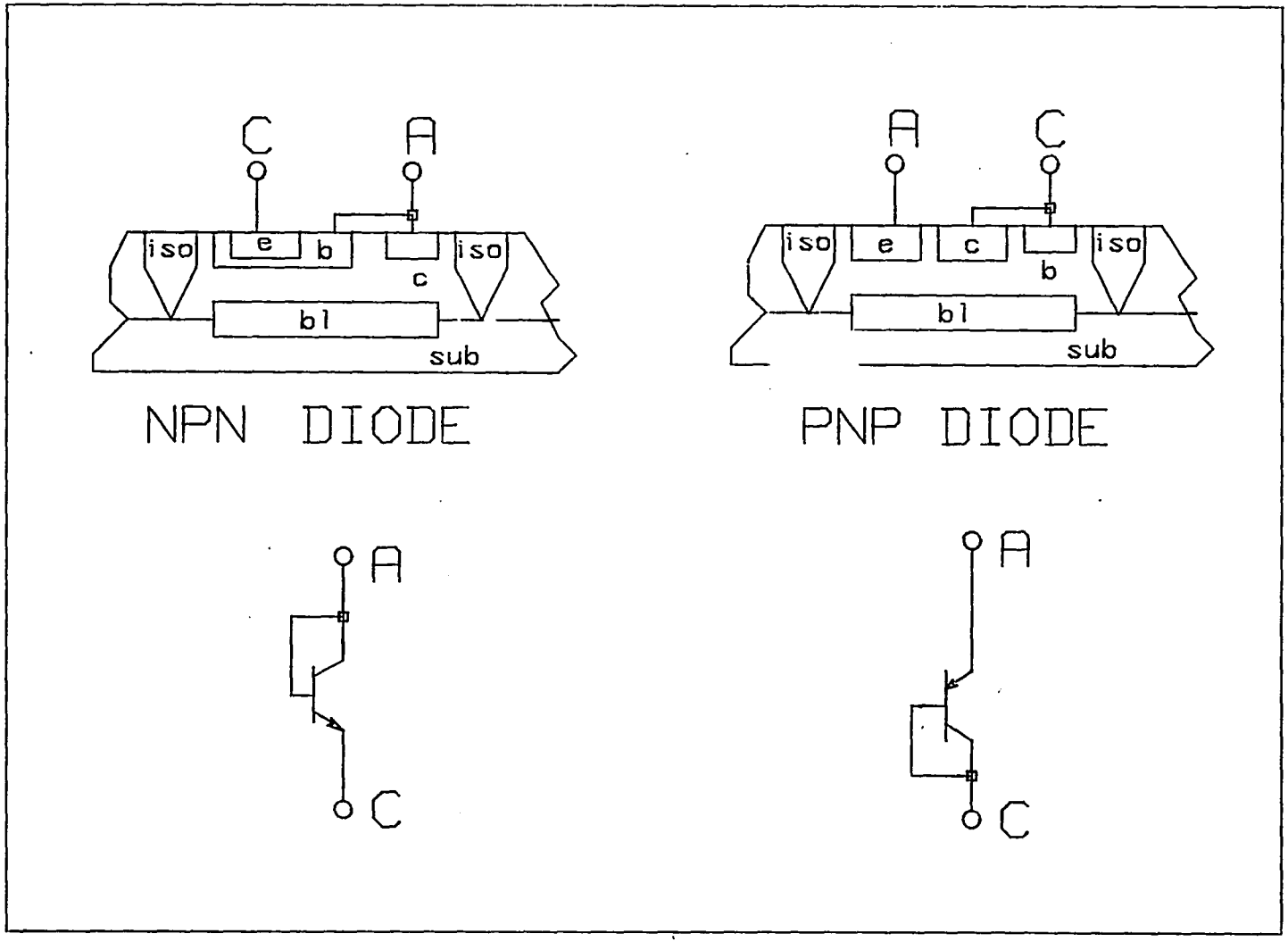

Fig. 3.14 Charge Pump Diodes

The function as implemented on the die is shown in Fig. 3.15, and also in Section d of the die photo in Appendix E.

3.6 RS423/TTL Data Translaters

The conversion between the two logic level, RS423 and TTL, is accomplished by the two circuits shown in Fig. 3.16. The two gain stages A_1 and A_2 are the same for each function. The current for the RS423 output was enhanced by current multiplying mirror configuration circuit Q_{521}, Q_{520}, and R_{508}. The threshold for the RS423 input was reduced two diodes voltages below the "a" TTL input.

The basic gain stage A_1 is shown in Fig. 3.17. It is a simple differential pnp pair driving an npn active load, with a second gain stage that has a current source load. A diode threshold reference string is on the non-inverting input. A slew-rate control capacitor is used to control the RS423 output only. The on-chip 10 pF capacitor (C_{501}) will limit the slew-rate of the output rise-time to approximately 40 μsec.

The differential input pair uses split-collector pnp transistors because this configuration reduces the size of the slew-rate capacitor (Appendix B). In this design the capacitor was reduced by a factor of four by dividing the collectors into four sections. One of the sections is used in the signal path. The other three are returned to ground. Three sections from Q_{501} are returned through Q_{517}, a diode in the non-inverting bias network, to develop hystersis at the inverting input. When the input of Q_{105} swings below the input

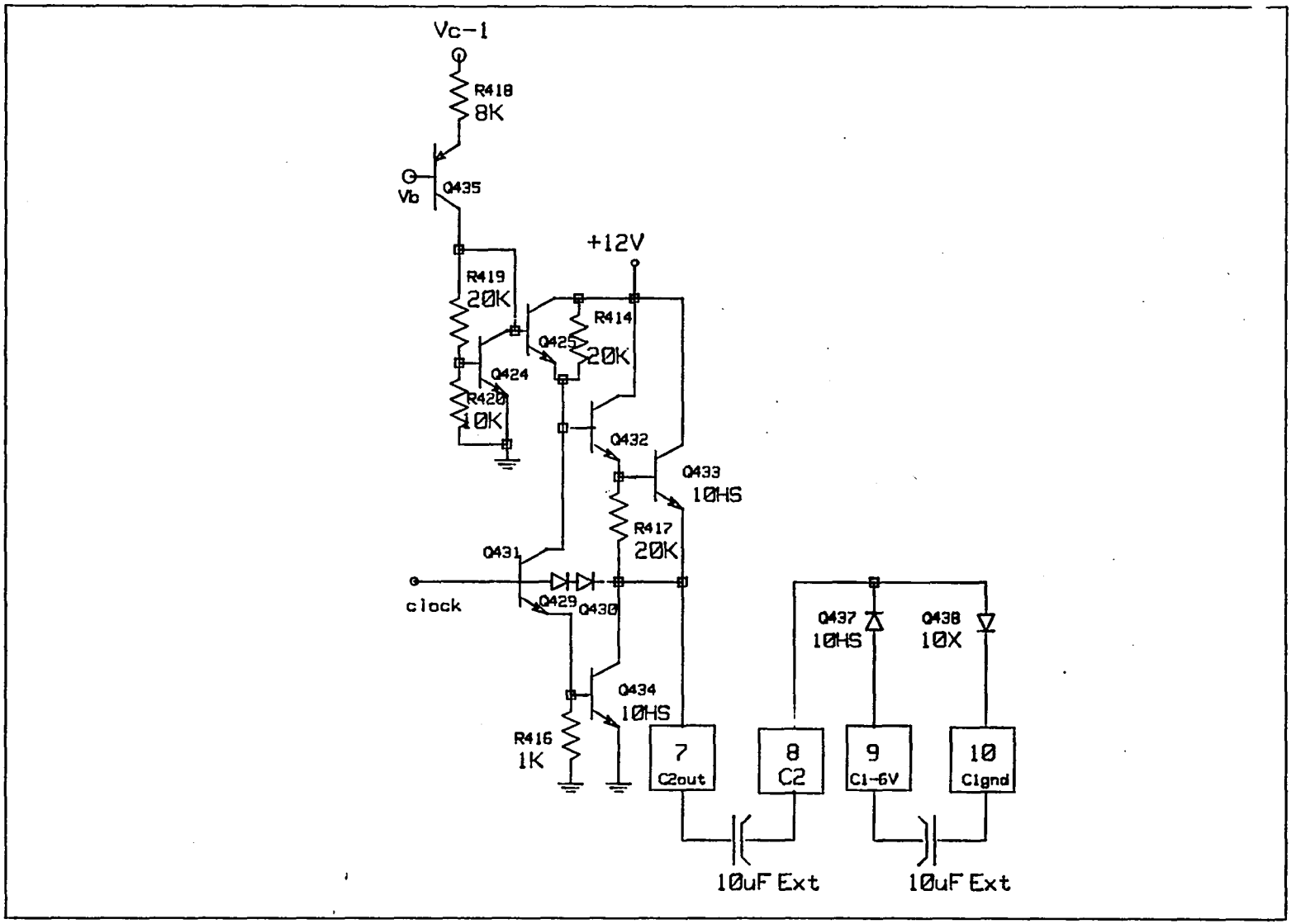

Fig. 3.15 IC Equivalent Schematic of Charge Pump

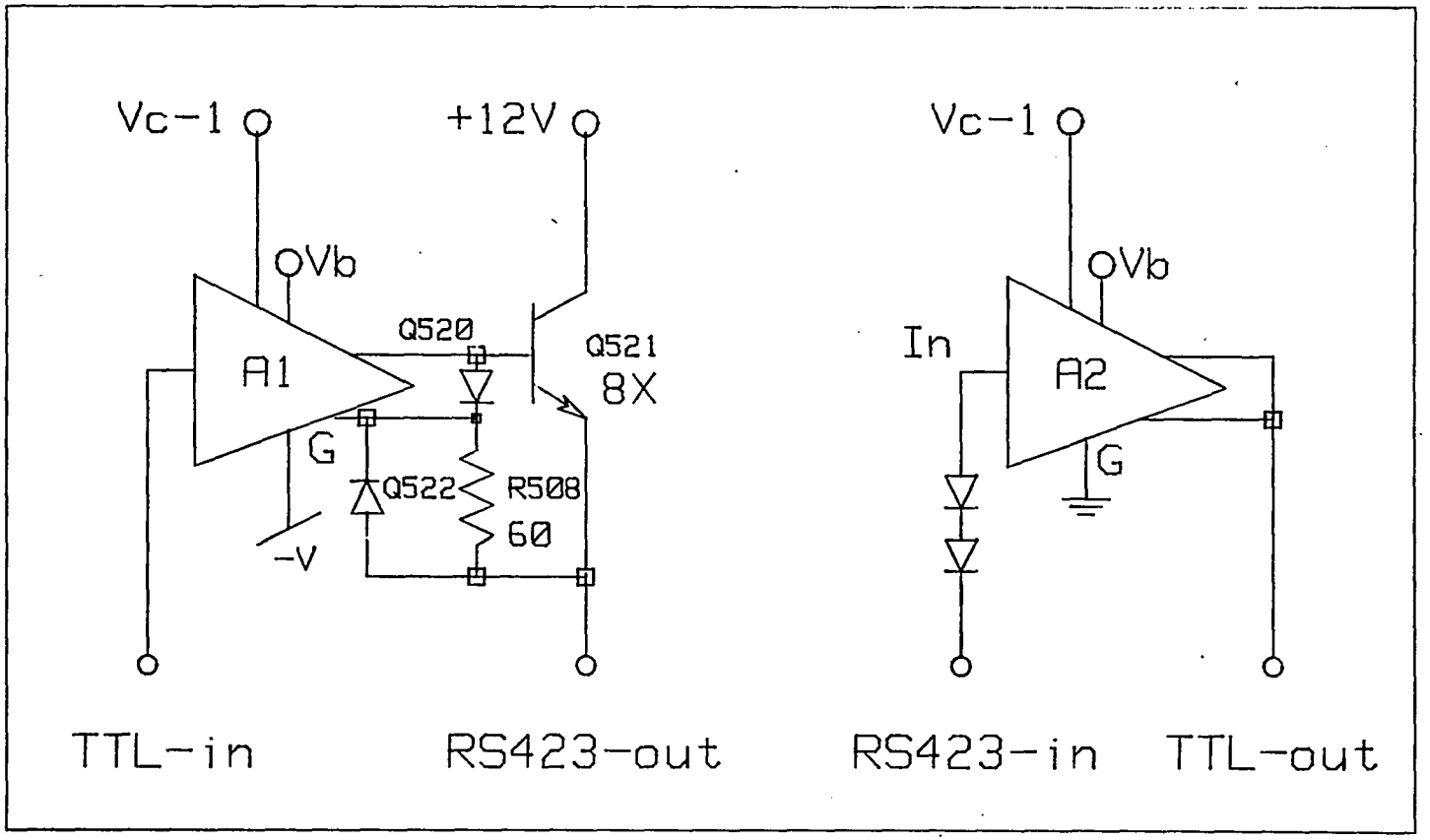

Fig. 3.16 TTL to RS423/RS423 to TTL Converters

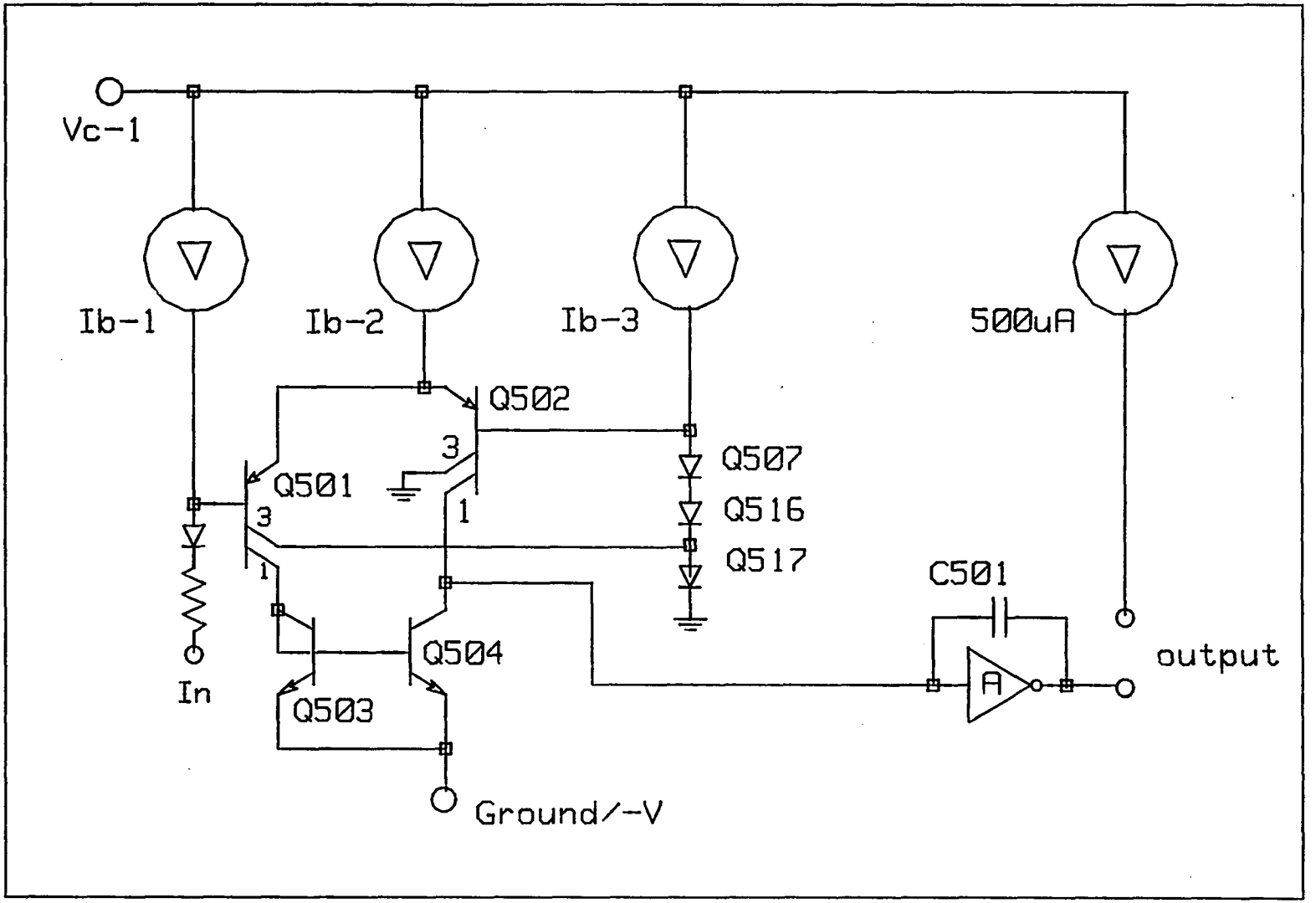

Fig. 3.17 Data Transceiver Cell Concept

threshold Q_{501} turns ON, injecting current into the diode and thus increasing the voltage drop. The hystersis is

$$\Delta V_{th} = V_t \cdot \ell n\ (1 + 0.75 \cdot I_{b2}/I_{b3})$$

For a ratio of 8:1 for I_{b2} and I_{b3} the hystersis is 45 mV.

The circuit refined for the IC implementation is shown in Fig. 3.18. The portion of the IC containing the function is designated as e of the die photo shown in Appendix E.

3.7 IIL Data Registers

Data latches and transfer buffers are constructed with IIL, also known as Merged Transistor Logic (MTL), a low-power, high density bipolar logic family, which was introduced in 1972 [Elmasry, 1983]. IIL is based on repartitioning direct coupled logic (DCTL) and merging an inverted npn transistor with a lateral pnp. The vertical npn is the switch transistor and the lateral pnp is used as an active load for the npn collector. Figure 3.19 shows a four collector IIL device which is the maximum collector fan-out with this process.

The status data are serial clocked into the latches from the SPI ports of the microprocessor at a 500 KHz rate and transferred to the LED and audio current sources on an enable low command, E.

The latches are simple "D" flip-flops as shown in Fig. 3.20. Note that the collector of gate G_{19} is larger than that of G_{18}, and that the base of G_{19} runs into the deep N^+ that surrounds each gate.

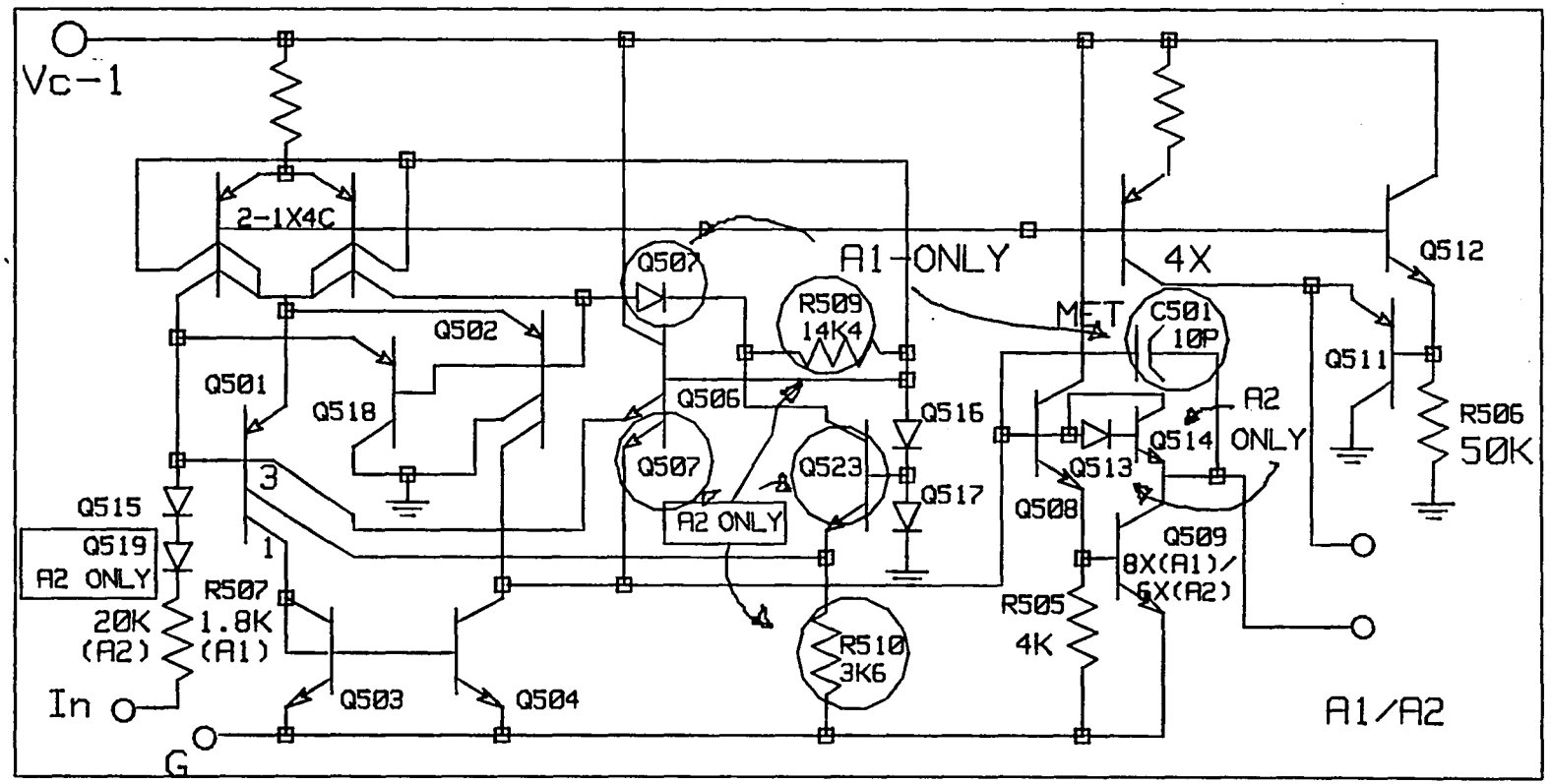

Fig. 3.18 IC Implementation of Data Transducer Cell

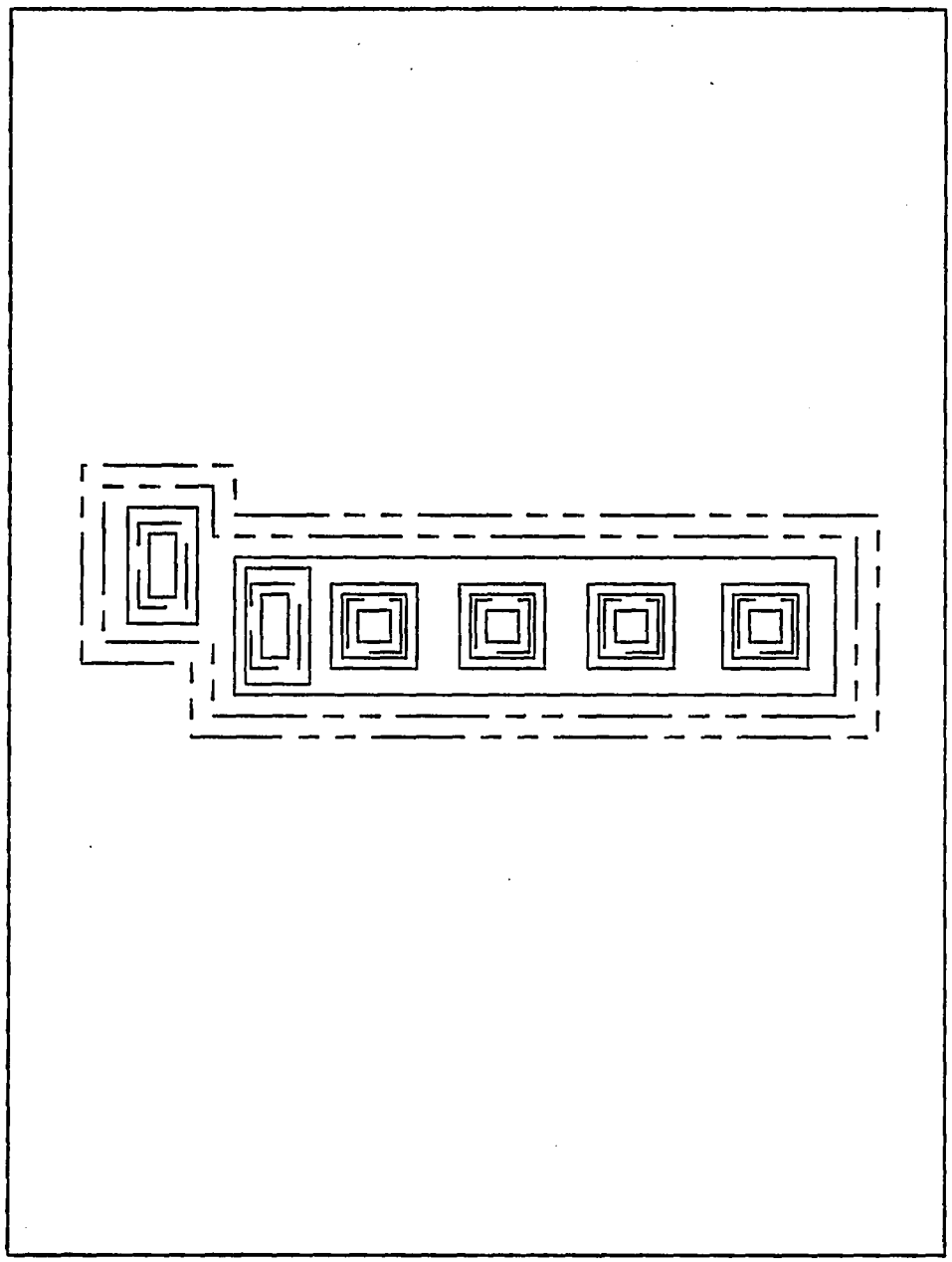

Fig. 3.19 Four Collector IIL Transistor

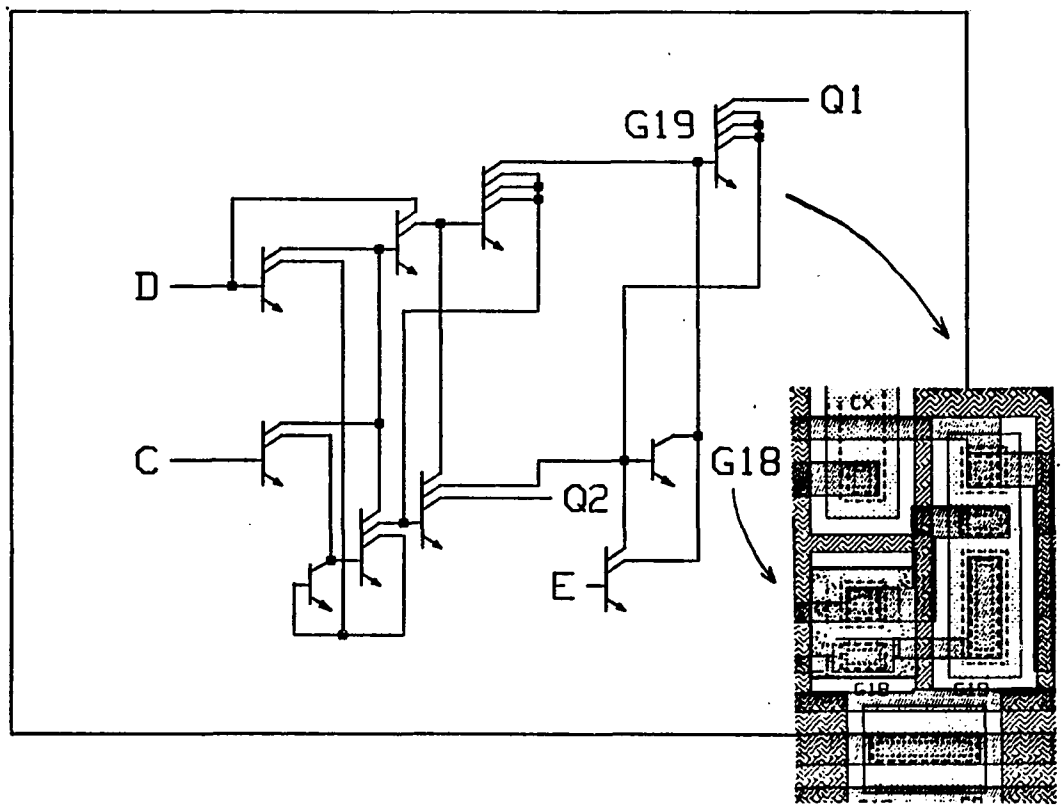

Fig. 3.20 IIL Data Register with Buffer Latch

The purpose of this was to slow gate G_{18} and to increase the gain of gate G_{19} so that during power-up conditions gate G_{19} will be the faster, forcing the output of the latch always into a favored OFF state during power-up. This is a cheap way of providng a "power-on reset" function.

The IIL logic can be found in Section f of the die photo in Appendix E.

CHAPTER 4

CHIP VOLTAGE REGULATOR AND CURRENT BIAS NETWORK

4.1 Chip Biasing Network

Each of the blocks was designed so that the accuracy of the parameters is a function of a bias current from a chip bias network. As noted by Gray and Meyer [1977], the IC technology offers poor absolute value component tolerances and temperature coefficients, but it does an excellent job of providing components with good matching characteristics, especially when care is exercised in the geometry and die location during the layout of the IC. Because absolutes are more difficult to obtain, and since the trim techniques studied were too time consuming and costly, a reference current was established from the regulated voltage with an external precision resistor. The reference is "mirrored" to each stage on the IC. (See Appendices A and B.) The accuracy constraint is therefore a function of the external resistor and the IC component matching characteristics, rather than the accuracy of absolute IC parameters.

The reference network (or the "current mirror network") is the section of circuitry shown in Fig. 1.2 and Fig. 1.4, consisting of all the pnp transistors with their emitter-resistors connected to the bias voltage V_{c-1} and their bases connected to a bias voltage V_b.

4.2 Voltage Regulator and Chip Bias Generator

The basic concept for the voltage regulator and chip bias network is shown in Fig. 4.1. The core of the network is a bandgap regulator. The bandgap voltage (V_{bg}) is buffered and increased to five volts by the gain stage A_1 and resistors R_1 and R_2. It is increased further by three diode voltages, buffered by A_2 and used for the bias voltages V_{c-1}. V_{bg} was buffered again by the gain stage A_3 and used to drive the base of the pnp transistor Q_{21} to a reference current I_{ref}, which is the current that produces a voltage drop equal to the bandgap voltage. The voltage at the base of the reference pnp transistor Q_{21} is the voltage V_B that is applied to the pnp bases in the bias network.

4.3 Basic Bandgap Regulator

A basic bandgap reference, as discussed by Brokaw [1974], is shown in Fig. 4.2. It works on the principle of forcing equal currents through unequal npn emitter areas, Q_1 and Q_2. Details on emitter scaling are given in the appendices. The larger emitter area of Q_2 will have a lower base-to-emitter voltage equal to

$$\Delta V_{be} = kT/q(\ell n\ J_1/J_2) \qquad (4.1)$$

where

k = Boltzmann constant = 8.62E-5 eV/K

T = temperature in Kelvin = 300

q = electronic charge = 1.6E-19 coulomb

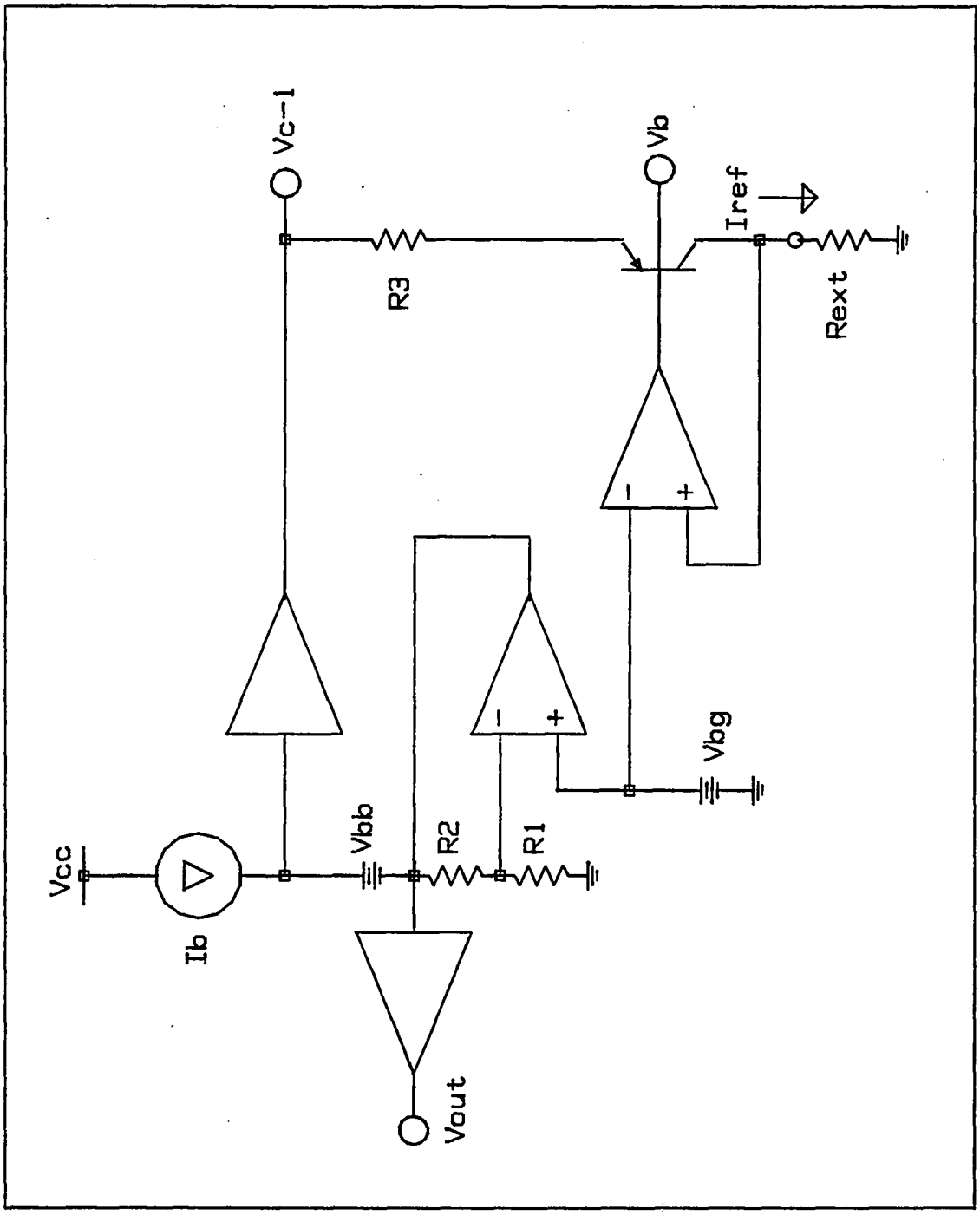

Fig. 4.1 Voltage Regulator and Chip Bias Generator

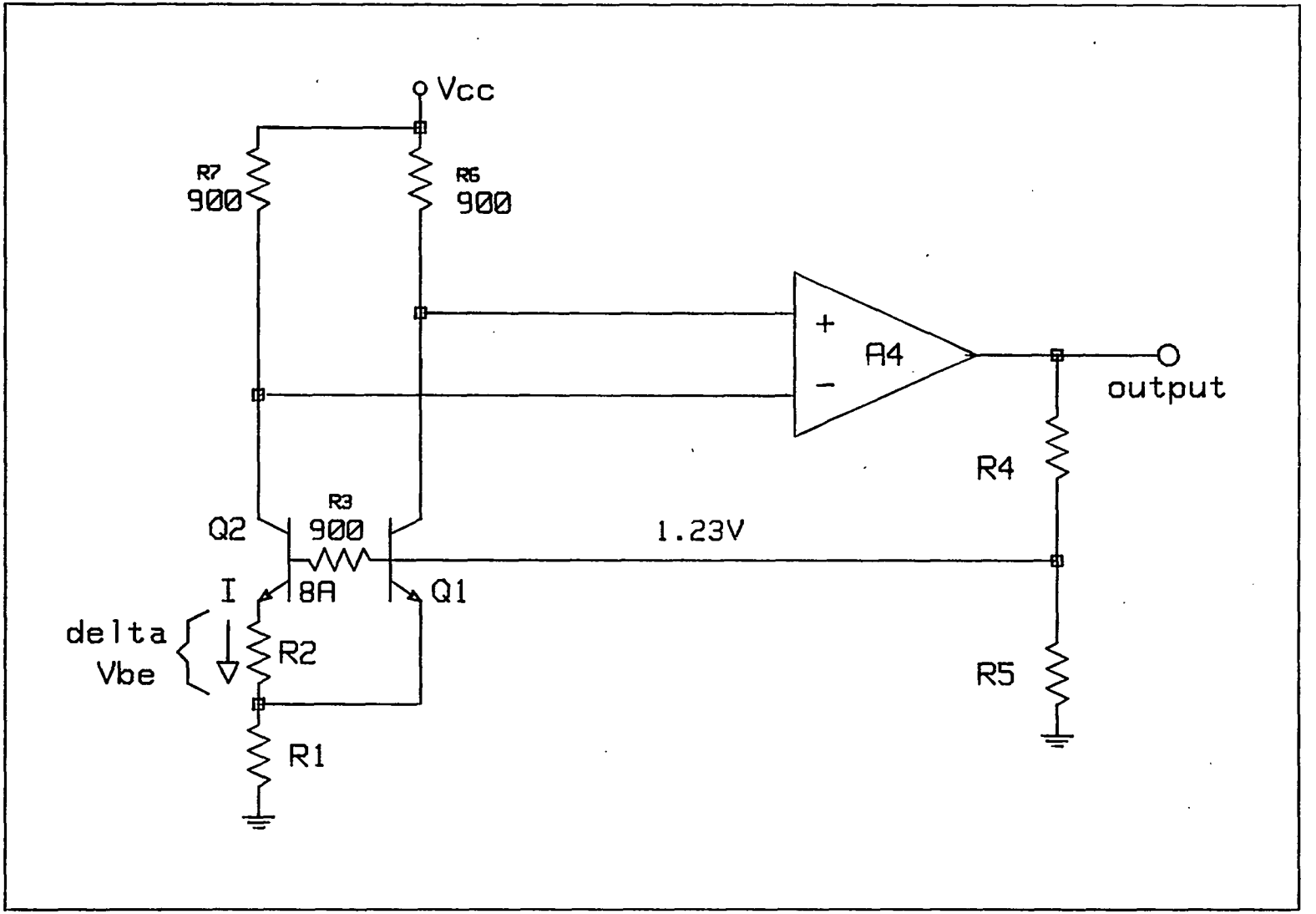

Fig. 4.2 Basic Bandgap Voltage Reference

J_1 and J_2 are the current densities of the npn transistors Q_1 and Q_2. ($A_1 = 8A_2$.) The difference between the two base-to-emitter voltages, since Q_2 is smaller by a ΔV_{be}, will appear across resistor R_2 and establish the "set-up" current for the stage.

$$I \text{ set-up} = (\Delta V_{be})/R_2 = 53.8 \text{ mV}/386 = 140 \text{ } \mu\text{A} \qquad (4.2)$$

With care in choosing the ratio of R_1 to R_2, the sum of the base-to-emitter voltage of Q_1 and the voltage drop due to the set-up current and resistor R_1, a low temperature characteristic voltage can be developed at the bases of Q_1 and Q_2. This "bandgap" voltage (V_{bg}) is increased to the final value by the resistor network R_4 and R_5

$$V_{out} = V_{bg}(R_4 + R_5)/R_5 = 5 \text{ volts} \qquad (4.3)$$

4.4 Complete Voltage and Reference Current Regulator Schematic

The schematic for the voltage and current regulator as implemented on the die is shown in Fig. 4.3, and the portion of the die for the function is shown in Appendix E, Section g.

Amplifier A_4 of Fig. 4.2 is formed by Q_5, Q_6, Q_7, Q_{14}, Q_{15}, Q_8, Q_{24}, Q_{25}, Q_{26}, and Q_9. Transistors Q_5, Q_6, and Q_7 sense the changes in voltage across the load resistors R_6 and R_7, and convert it to a change in current at the collectors of Q_3 and Q_5. The current is buffered by Q_{15} and Q_8/Q_9 and applied to the scaling resistors R_4 and R_5. The feedback loop will establish a current that will satisfy

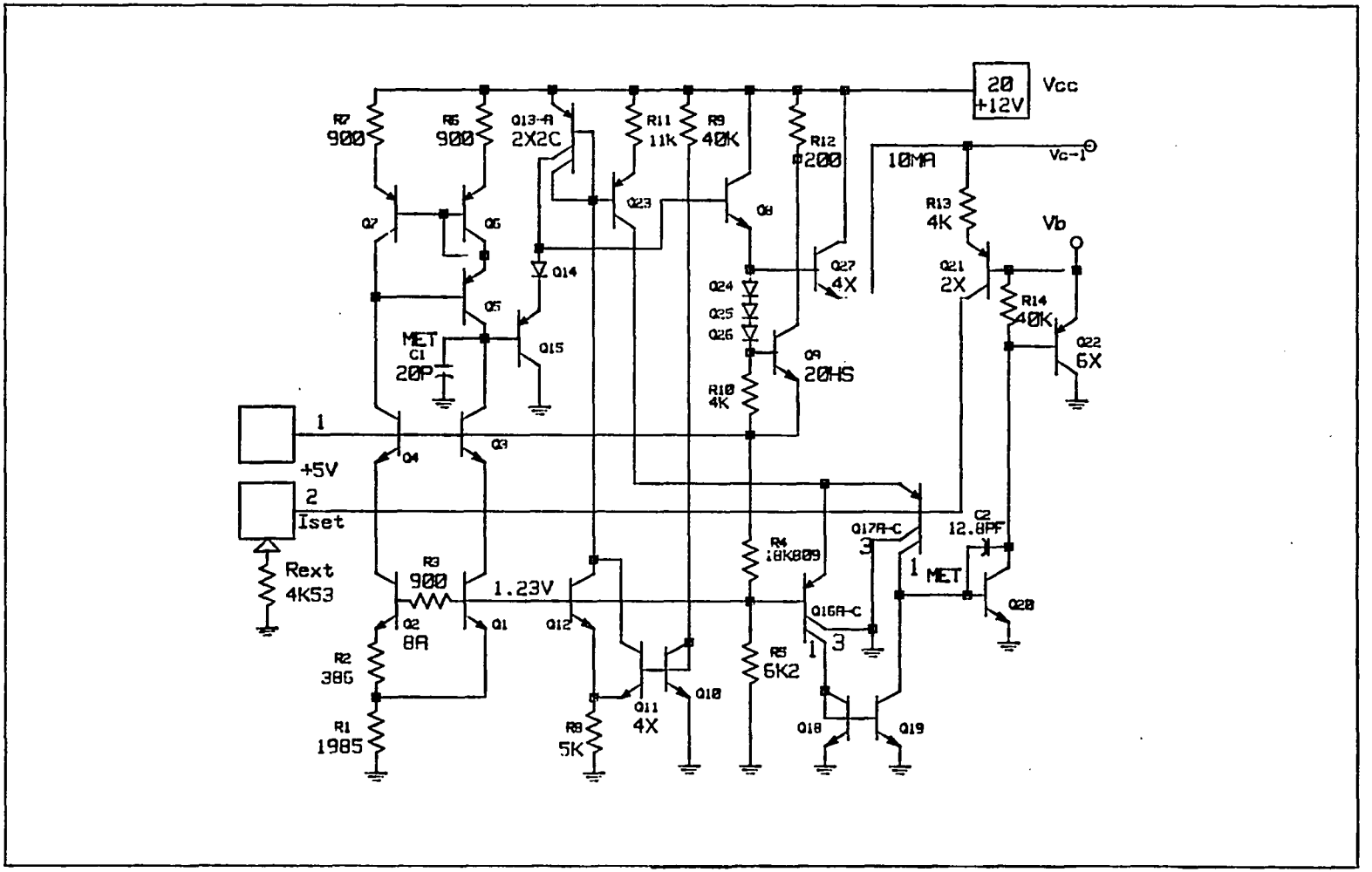

Fig. 4.3 Complete Equivalent Schematic of Bias Generator

the voltage requirement at the bases of Q_1 and Q_2, which has been designed to be the bandgap voltage, V_g = 1.23 volts. Transistors Q_3 and Q_4 are used to force equal voltages on the collectors of Q_1 and Q_2, and to buffer Q_1 and Q_2 from changes that occur in the 12 volt digital voltage supply. Equal voltages across Q_1 and Q_2 help to keep their collector currents equal. (See Appendix C.) The resistor R_3 is included to reduce the error induced by the base currents of Q_3 and Q_4 as discussed by Brokaw [1974].

$$R_3 = R_2R_4R_5/R_1(R_4 + R_5)$$

$$= (386)(18.8K)(6.2K)/[1985(18.8K + 6.2K)]$$

$$= 906.6 \text{ ohms} \qquad (4.4)$$

The regulated 5-volt output is increased by three base emitter voltages (diode connected Q_{24}, Q_{25}, and Q_{26}), buffered by Q_{27} and used to supply the voltage for the pnp current source network (V_{c-1} = 7 volts). The bias current for Q_{24}, Q_{25}, and Q_{26} is equal to the base-to-emitter voltage of Q_9 divided by resistor R_{10}, which is 175 μA. The 200 ohm resistor (R_{12}) in the collector of Q_9 is included for short circuit current limiting to about 50 milliamperes for protection should the output accidentally be shorted.

The bias current for Q_{14} and Q_{15} is supplied by Q_{13-A}, Q_{12}, and R_8. The bandgap voltage, minus a base-to-emitter voltage is across resistor R_8, which establishes the emitter current of Q_{12}. The

collector current of Q_{12} is mirrored to Q_{14} by the mirror configured, split-collector pnp transistor, Q_{13-A}. See Appendix B for split collector pnp configurations.

The voltage regulator circuit has two stable states, one of which is OFF. To make sure the active state occurs during the initial power-up phase, Q_{10}, Q_{11}, and R_9 are included as shown. Resistor R_9 and the diode connected transistor Q_{10} are across the input voltage, V_{cc}. The base-to-emitter voltage of Q_{10} is applied to the base of Q_{11}. If the circuit is not active a small voltage is developed across R_8 by the difference voltage, ΔV_{be}, of Q_{10} and Q_{11}. The current from Q_{11} will mirror base current to Q_8. This current is amplified by the beta of Q_8 and fed to the resistor network R_4 and R_5. This will produce a voltage at the bases of Q_1 and Q_2, bootstrapping in the ON condition. At turn ON

$$I_{e_{11}} = [kT/q) \cdot \ell n\ J_{10}/J_{11}]/R_8$$

$$J_{10} = 4 \cdot J_{11}$$

$$I_{e_{11}} = 7.2\ \mu A \qquad (4.5)$$

When the voltage at the base of Q_1 reaches its ON condition, the voltage V_{bg}-V_{be} at the emitter of Q_{11} will reverse the emitter-base junction of Q_{11}, turn it off, and remove the bias start-up current from the collector of Q_{11}. This is preferred because the start-up current

is sensitive to changes in the supply voltage V_{cc}, and could degrade regulation performance if allowed to remain.

The gain for the basic regulator cell is approximately the output impedance at the base of Q_{15} divided by R_1, as shown in Eq. (4.6)

$$A_v = Z_o/R_1 = \sim 120 \tag{4.6}$$

Because the circuit is in a feedback configuration, oscillation could occur if the frequency response was not controlled. Therefore, capacitor C_1 is included to establish a dominant pole in the frequency response characteristic of the circuit. The value is arrived at by considering the transconductance

$$(g_m = \Delta i\text{-}o/\Delta v\text{-}in) \tag{4.7}$$

of the stage as the ratio of an incremental change in the output current of the collectors of Q_3 and Q_5 to the change in the voltage at the base of Q_1. The transconductance can be approximated to equal $1/2R_1$. The unity frequency gain point, where the transconductance equals the capacitive reactance is

$$\begin{aligned} f_u &= g_m/(3 \cdot 2\pi \cdot C_1) \\ &= 2.5E\text{-}4/(3 \cdot 2 \cdot 3.1416 \cdot 20\ pF) \\ &= 668\ kHz \end{aligned} \tag{4.8}$$

It should be noted that the 3 in the denominator of the equation is the ratio of R_4 to R_5. This represents a 3:1 reduction in the loop gain.

The differential amplifier used in the reference current circuit is shown in greater detail in Fig. 4.3. It contains split collector pnp transistors Q_{16A-C} and Q_{17A-C}, npn transistors Q_{18}, Q_{19}, Q_{20}, and capacitor C_2. Split collectors are used again for transconductance reduction and a smaller compensation capacitor (Appendix B). The collectors are scaled for a g_m reduction of 4, which reduces the size of the capacitor by a factor of four.

One input of the amplifier is connected to the bandgap voltage and the other is connected to the collector of the reference transistor Q_{21}, along with the external resistor, R_{ext}. The differential pnp pair will reach a balanced condition when the collector current of Q_{21} produces an IR drop across the external resistor equal to the bandgap voltage, therefore

$$\begin{aligned} I_{ref} &= V_{bg}/R_{ext} \\ &= 1.23/4530 \\ &= 271.5\ \mu A \end{aligned} \tag{4.9}$$

The bias current for the differential pnp's is supplied by Q_{23} whose base is referenced to the pnp current mirror configuration Q_{13-A}. The value of the current is lower than that of Q_{13} because

of the degeneration emitter resistor R_{11}.

$$IQ_{23} = (V_t/R_{11}) \cdot \ell n(IQ_{13-A}/IQ_{23})$$

$$= (0.0259/11K) \cdot \ell n(224\ \mu A/IQ_{23})$$

$$= 8\ \mu A \qquad (4.10)$$

The capacitor C_2 sets the unity crossover frequency for the gain stage at

$$f_u = g_m/2 \cdot 3.1416 \cdot C_2$$

$$= 38.5 \cdot 4\ \mu A/(2 \cdot 3.1416 \cdot 12.8\ pF)$$

$$= 478.7\ KHZ \qquad (4.11)$$

Q_{22} buffers the base currents of the current source, and resistor R_{14} helps keep a constant load impedance at the collector of Q_{20}, so that the pole frequency of the gain stage A_3 will not change with the beta variations of Q_{22}. The latter could be as much as 4:1.

CHAPTER 5

RESULTS AND CONCLUDING REMARKS

5.1 Results

The basic initial specifications with the results are given in Table 5.1. The LED amplifiers are typically able to sink 12 mA of current, at a minimum voltage of 2.6 volts. The current varies by 0.3% per volt, and the variation over the 0 to 70°C temperature range was only 1 - 2%.

The audio transducer driver digital word to current transfer characteristic was used to drive one of the electromagnetic transducers without any problems. The output current varied with the temperature by approximately 2 - 3%.

The squarewave generator produces a typical frequency of 2059 Hz at an output voltage of 4 volts. The current values shifted about 2 - 3% over the temperature range.

The output of the TTL to RS423 data translator has an 8 mA loaded swing from +4.5 volts to -3.6 volts, with a rise and fall time of about 40 μs. The no-load swing was +4.9 to -5.3 volts. The values varied approximately 4% over the temperature range.

The room temperature TTL output was +5.36 volts at a load current of 40 μA, to a low of 0.317 volts with a load current of 1 mA. The values varied by about 7% over temperature, but remained within the specification.

Table 5.1 Initial Design Results

Temperature = 27°C	$C_1 = C_2 = 10\ \mu F$
R_{set} = 4530 ohms	$C_{bypass} = 0.1\ \mu F$
$C_{ext} = .027\ \mu F$	V_{in} = 12 volts ± 20%

		Typical Results
V_o	Output Voltage (I_o = 0 to 10 mA)	5.08 volts
I LED	LED Currents (V LED = 4 volts)	12 mA
I audio	Audio Currents (V audio = 4 volts)	
	Digital Code: A_3, A_2, A_1, A_0	
	X = don't care	

	(mA)
000X	0.0
1001	5.7
0100	8.6
1100	11.4
0101	17.7
1101	23.6
0110	32.6
0011	49.1
1111	74.0

F ocs	Audio Oscillator Rate	2116 Hz
F data	Clock, Data, Enable Data Rate	580 KHz max
TTL out	TTL Output Level Thresholds	.32/5.4 volts max/min
RS423-in	Input Level Thresholds	0 volts ± 21 mV
RS423-out	Rise and Fall Times	20 µs < t_f < 50 µs @ +4.6V/-3.6V output
P_d	Chip Power Dissipation	218 mW max quiescent

The IIL data registers could operate up to 580 KHz over the temperature range; the specification was 500 KHz volts.

The voltage regulator and chip bias network performed well. The 5-volt output has a typical value of 5.08, which was acceptable. The computer simulations had predicated that a variation of $\pm$ 130 mV could be expected. If the saturation current was varied by 10%, a 130 mV change was anticipated, and if a 10% resistor change occurred, a 25 mV variation was observed with the breadboard and computer simulation. The output voltage V_o is plotted against the output current in Fig. 5.1 to show the load regulation characteristics and where the short-circuit current appears. The short circuit starts to become evident at 30 mA, with limit occurring at 60 mA. Figure 5.2 contains a plot of the output with respect to the supply voltage V_{cc}. The "line regulation" is about .12% per V_{cc} volt with a minimum operating supply voltage of 10.5 volts. The regulator output resistance

$$R_o = \Delta V/\Delta I$$

was 0.4 ohm at a load current of 10 mA. The stability of the output was good at the rated current of 10 mA and a 1 μF capacitor. The voltage and currents that were measured from the chip bias network were within the ranges predicated by hand calculations and computer simulation.

The power dissipation without considering the LED currents and the transducer currents was typically 218 mW. The final die size was 101 x 109 mils or 11,009 square mils, just under the 12,000 mil goal.

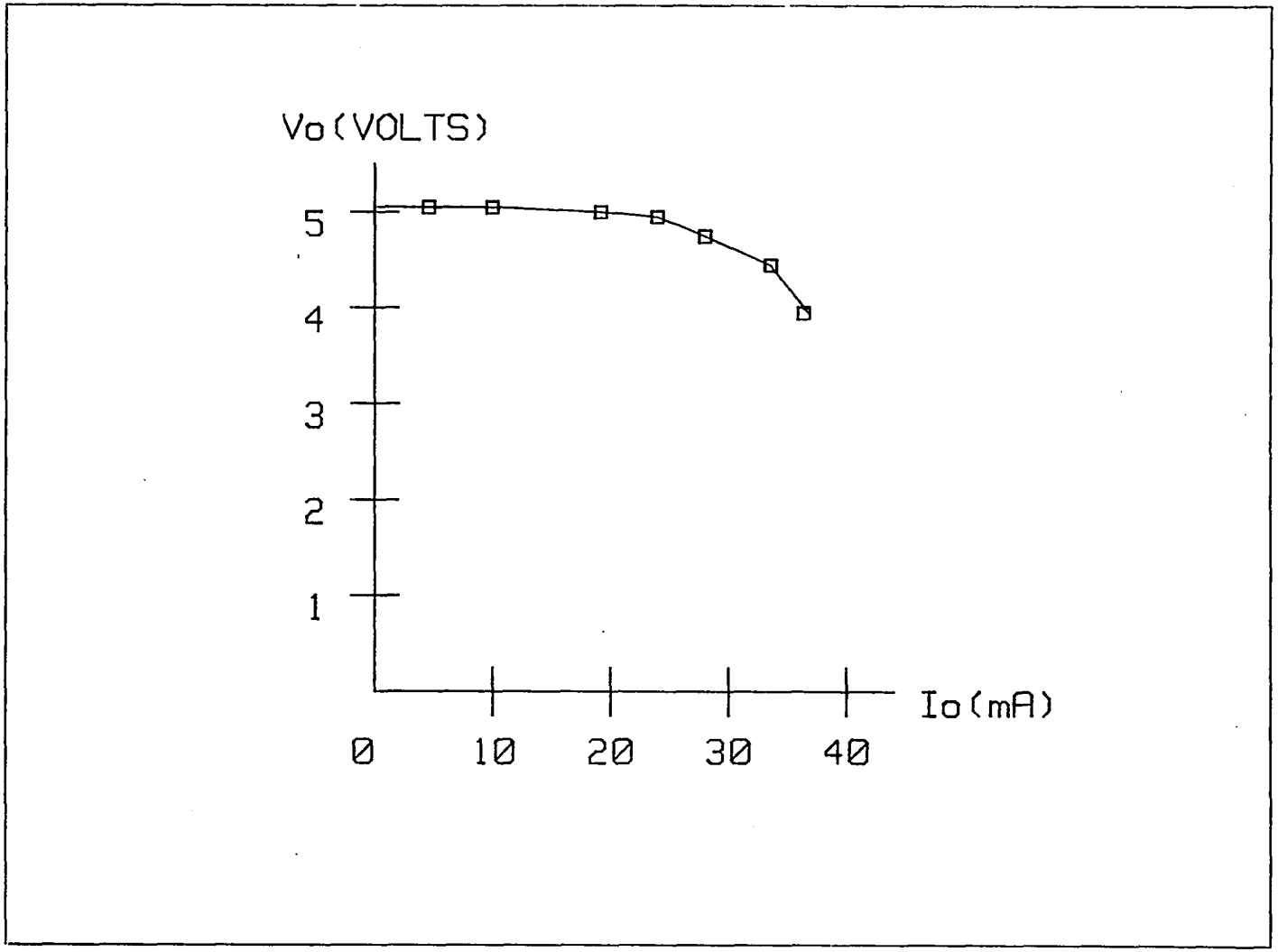

Fig. 5.1 Regulator Load Regulation

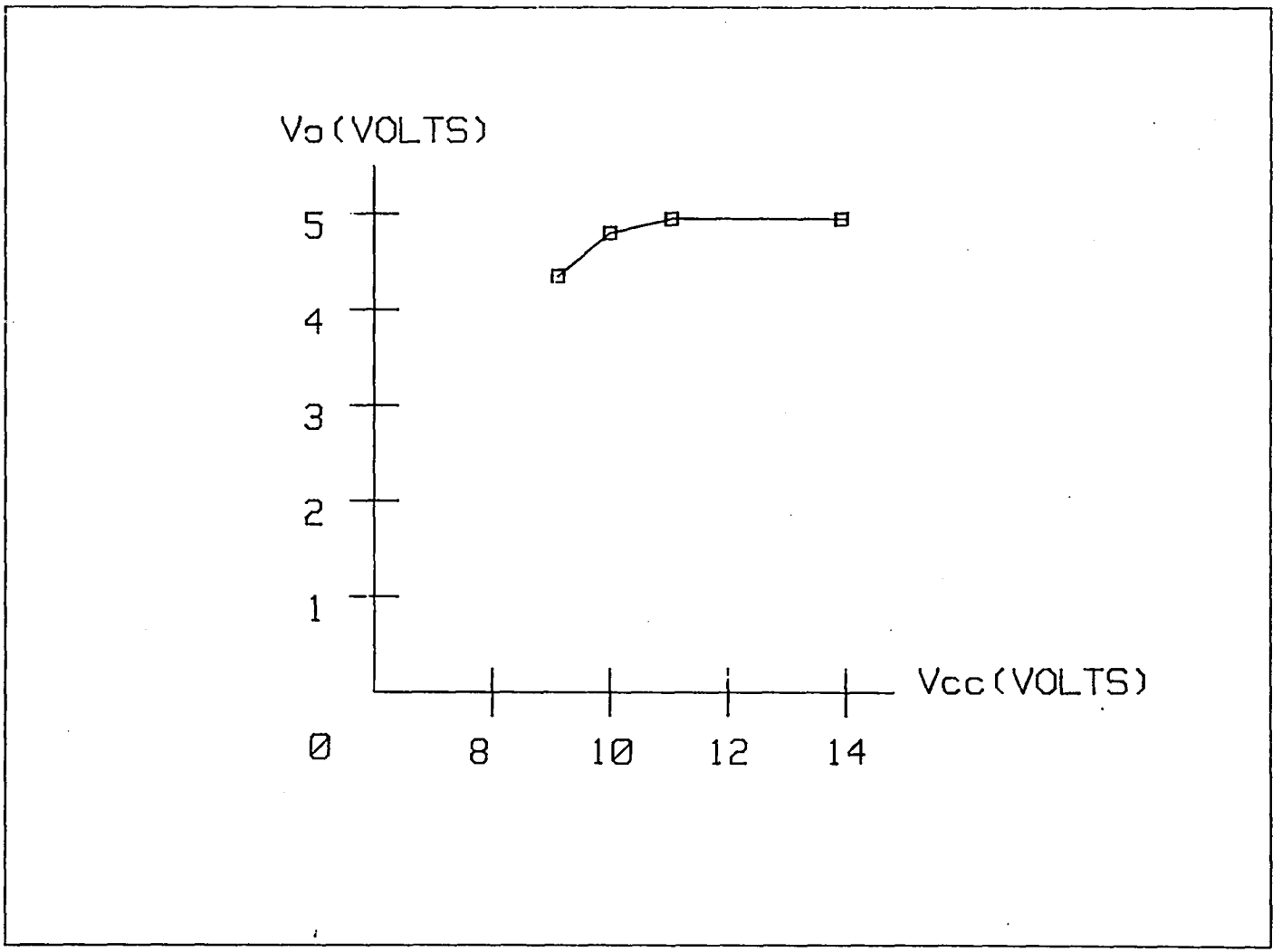

Fig. 5.2 Regulator Line Regulation

5.2 Concluding Remarks

The IC described in this report illustrates how custom circuit techniques can be used to produce a variety of functions on a single bipolar chip with optimized performance, power consumption, and die size. The optimization was realized by effectively applying merging techniques to produce the desired functions described in the discussion of the design of the squarewave generator.

Also noteworthy are the methods used to generate the large output currents from small, switched reference currents, as well as the DAC (digitally adjustable current source). In addition, the report points out that with careful design and layout consideration, a negative-high current voltage generator, complete with on-chip switching diodes is possible.

In conclusion, one should realize that a custom IC design is most effective when the application is thoroughly understood and just the right amount of circuitry is applied to the solution. Usually, a full custom design is justified only when fairly large volumes are expected. It is crucial that extra die area is not used to "over design" a function, adding to the die cost.

APPENDIX A

CURRENT SOURCES

Transistor current sources are widely used in analog integrated circuits [Gray and Meyer, 1977]. The currents can be scaled by using various resistor ratio and emitter ratio techniques. Figure A.1 illustrates how a variety of current sinks and sources can be achieved from a reference current. The different values are functions of the transistor emitter sizes and on the value of the emitter resistor, with respect to the reference. The basic equation can be arrived at by equating the two base voltages. For example, the equation for the 2I current source will be developed. Consider that the 2I current is twice as much as the reference and see if the two sides of the equation are equal

$$V_{be_1} + IR = V_{be_2} + 2IR/2$$

Since the area of the 2I transistor is twice the area of the reference, the base-to-emitter voltages will be the same:

$$IR = 2IR/2$$

$$IR = IR$$

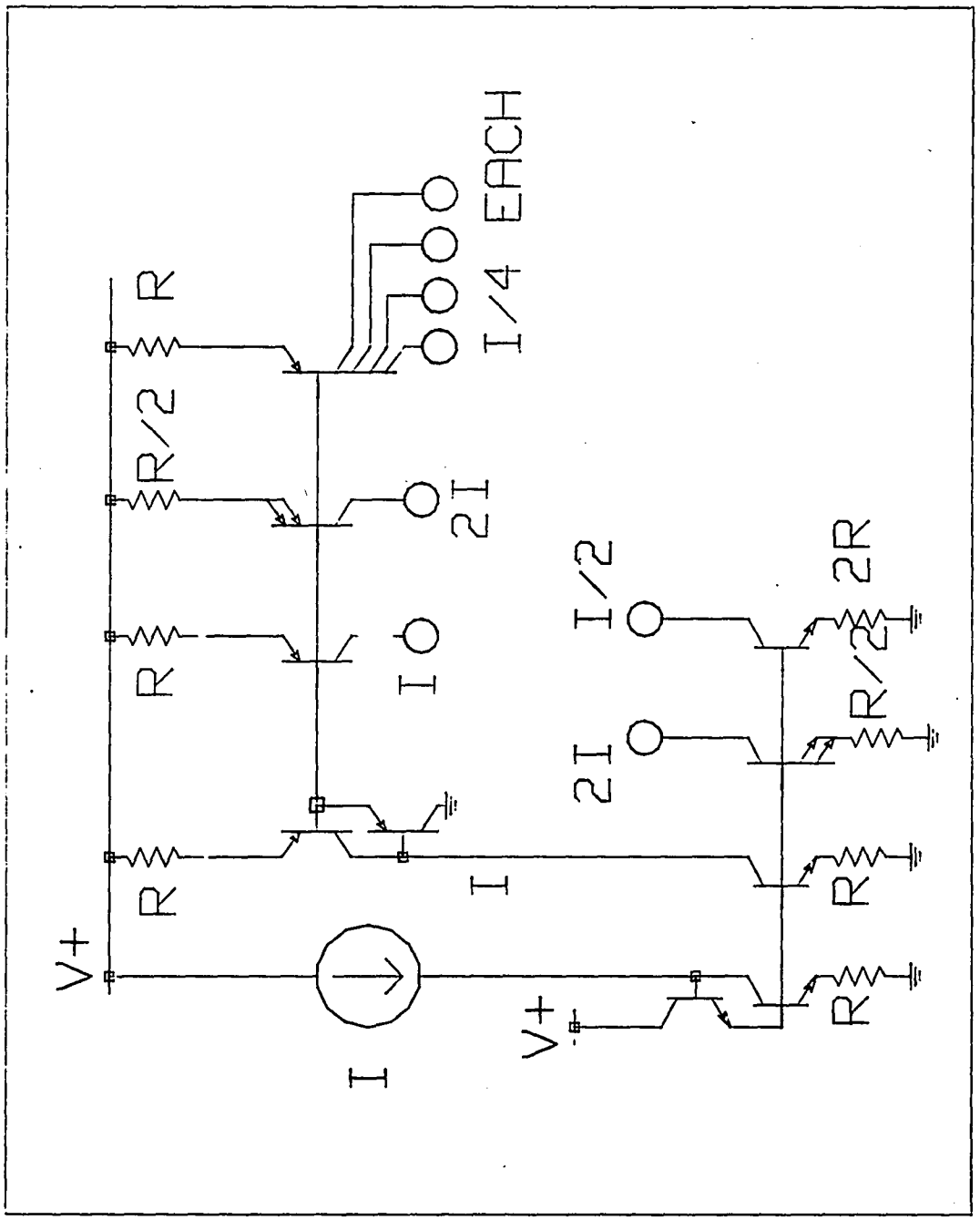

Fig. A.1 Current Sources and Sinks

which implies that the assumption that the second current was 2I is true. If the emitter sizes are different, the current densities must be considered, so a ΔV_{be} will have to be calculated.

An IC drawing of an npn with an emitter area twice the size of the other is shown in Fig. A.2 to show how it is achieved. Note that the 2X transistor has two separate emitters. This is better than just making the 2I emitter twice the area because the transistor will have some injection off the sides, and this method assures that the perimeters will also ratio by two over the variations experienced in making the masks for the IC and in making the IC itself.

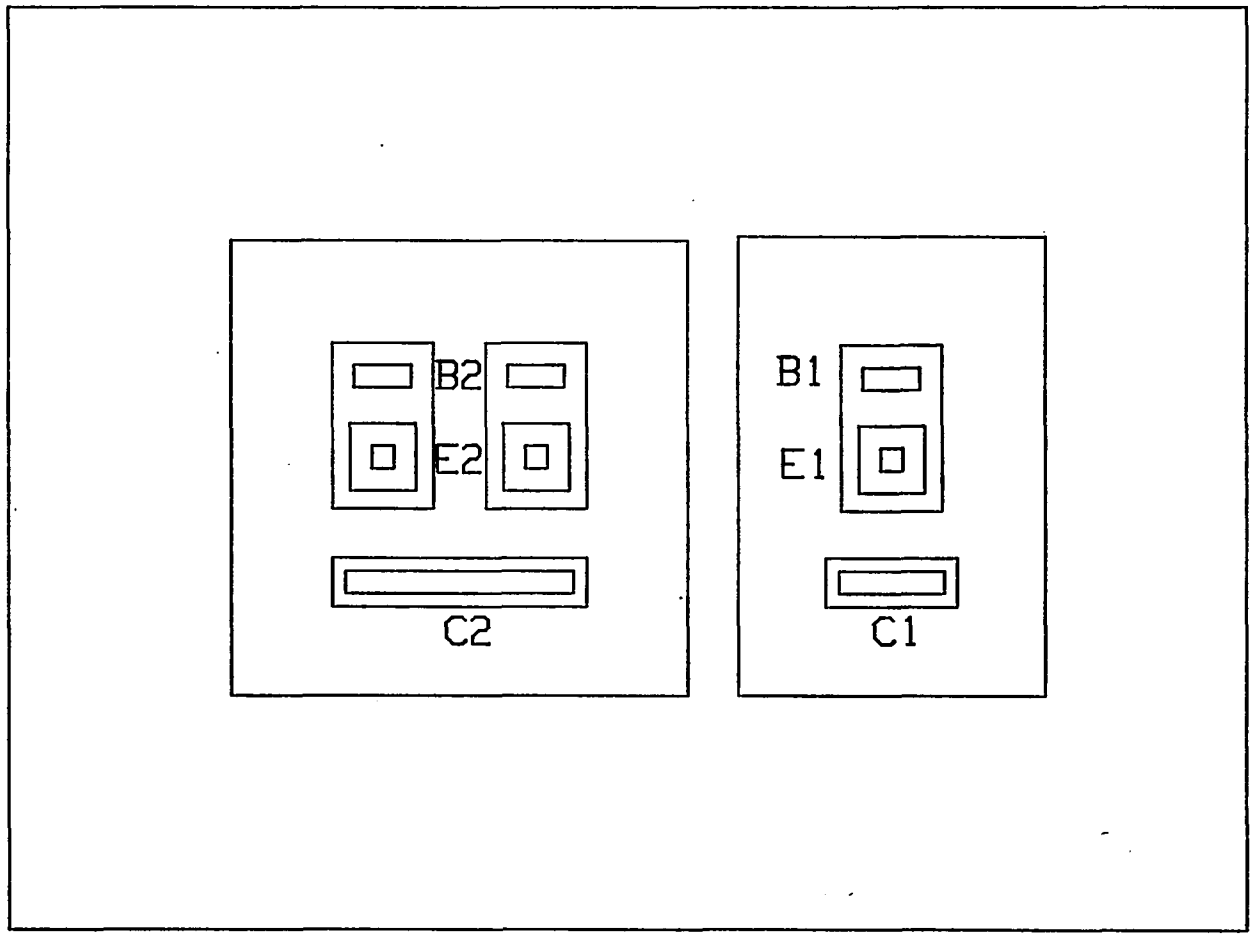

Fig. A.2 2X and a 1X NPN Transistor

APPENDIX B

SPLIT COLLECTOR PNP TRANSISTORS

The pnp transistor is sort of a fun structure to design with because the current scaling can be accomplished by "splitting" or sectioning the collector into pieces as shown in B.1. The IC layout for two pnp transistors with a 4:1 emitter ratio are shown in Fig. B.2. The layout for two scaled collector pnp transistors are shown in Fig. B.3. One has the collector chopped into four sections and the other has one complete collector. Remembering that the pnp is a vertical structure and thinking that most of the injection is off the edges of the emitter, many collector geometry configurations can be used for collecting if careful thought is put forth on what is happening and how the resulting current is used.

The split collector technique is used in operational amplifiers to keep the emitter current up while reducing the collector current in a particular collector [Frederiksen, 1984]. The current from the other collectors is usually thrown away. The advantage of doing this is to reduce the transductance, or the change in the collector current for a given change in base-to-emitter voltage. Since the unity frequency of a compensated op amp is a function of the transconductance and the compensation capacitor

$$f_u = g_m/2\pi \cdot C$$

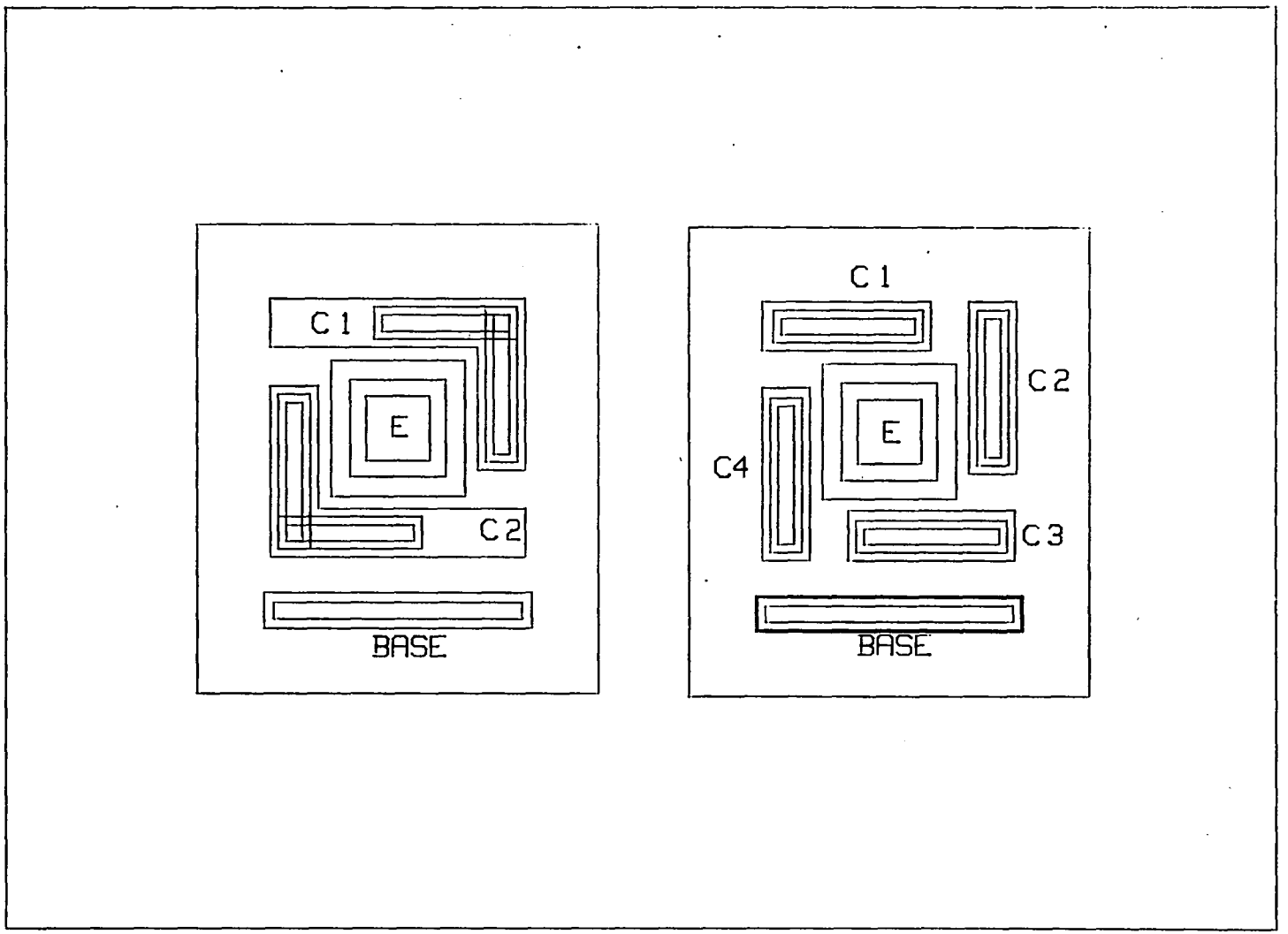

Fig. B.1 Split Collector PNP Transistor

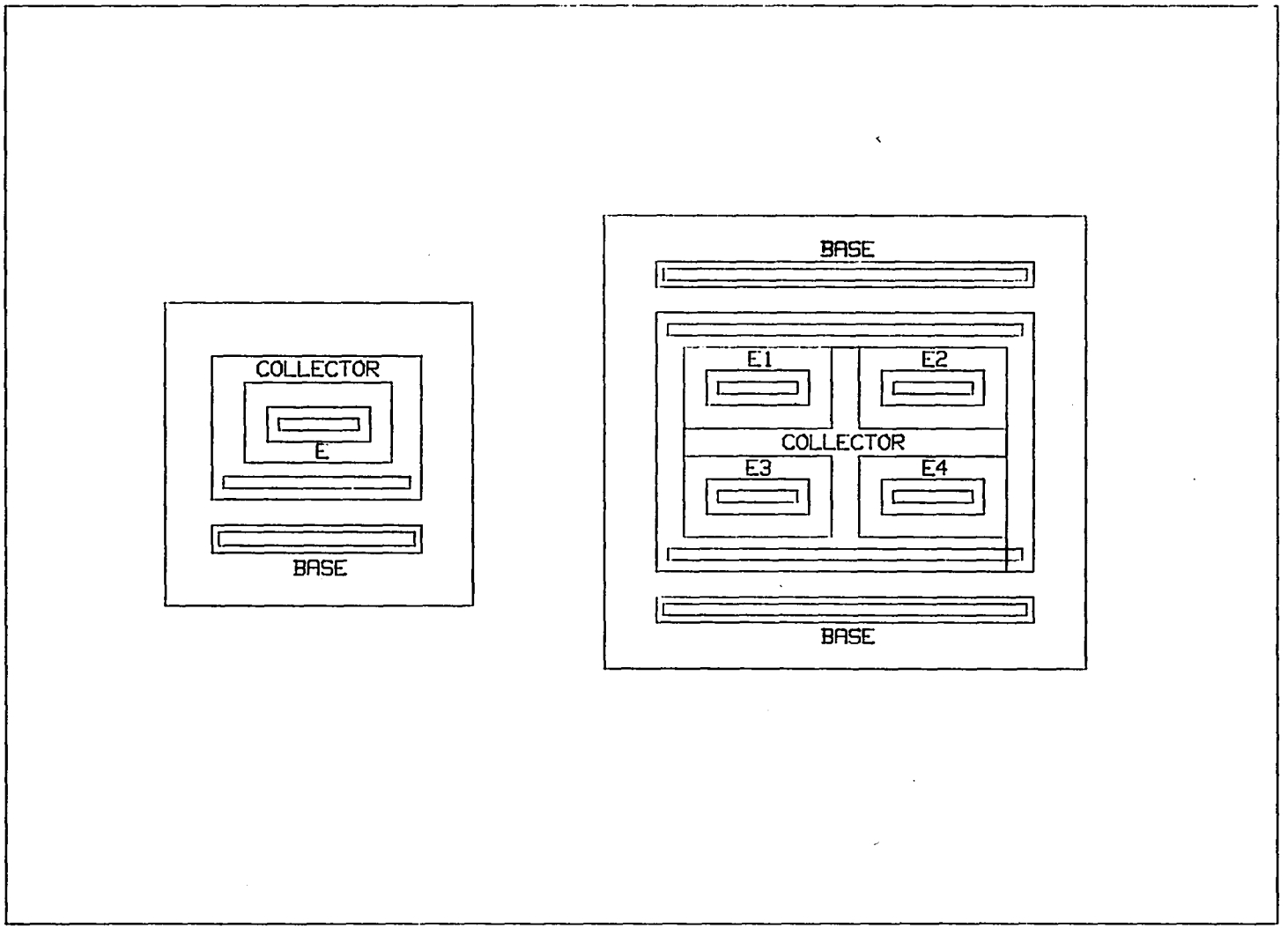

Fig. B.2 1X and a 4X PNP Transistor

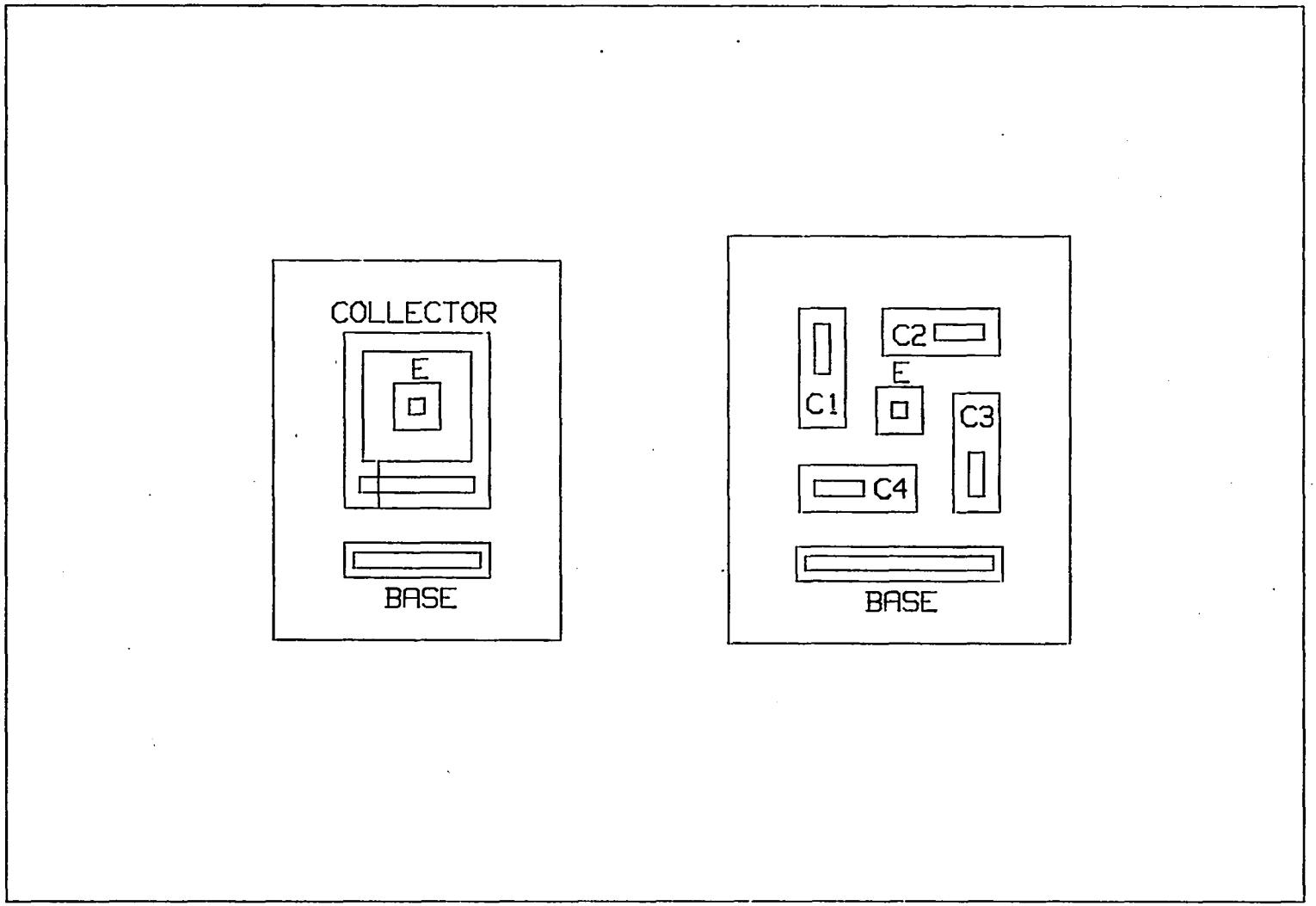

Fig. B.3 1 Collector and 4 Collector PNP

the capacitor can be smaller by the amount of the transconductance reduction which is a handy technique for conserving IC silicon area.

APPENDIX C

BETA AND EARLY VOLTAGE

When designing current sources it is important to optimize the transistor characteristics as much as possible. For example, to reduce the current error due to finite betas, it is a good idea to specifically design the structure for the level of current at which it will be operated. Figure C.1 is a plot of the beta versus the current. Note that it has a peak operating current where the beta is a maximum. Again, careful consideration during the design and the layout of the IC can produce optimum results with the least silicon.

Another consideration to consider when designing with transistors is the collector-to-emitter voltage on the devices. With different values the collector currents will be different. The effect is referred to as the "Early Voltage (V_a)" or "Basewidth Modulation". V_a is shown graphically in Fig. C.2 and is approximated mathematically as

$$I_c = I_s(1 + V_{ce}/V_a) \exp V_{be}/V_t$$

where

I_s = the transistor saturation voltage

V_t = thermal voltage = .0259

[Hamilton and Howard, 1975; Gray and Meyer, 1977].

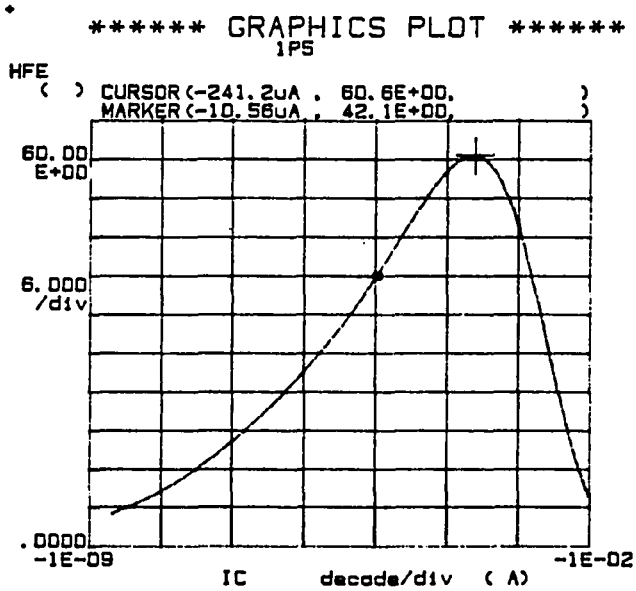

Fig. C.1 Plot of Transistor Beta versus Collector Current

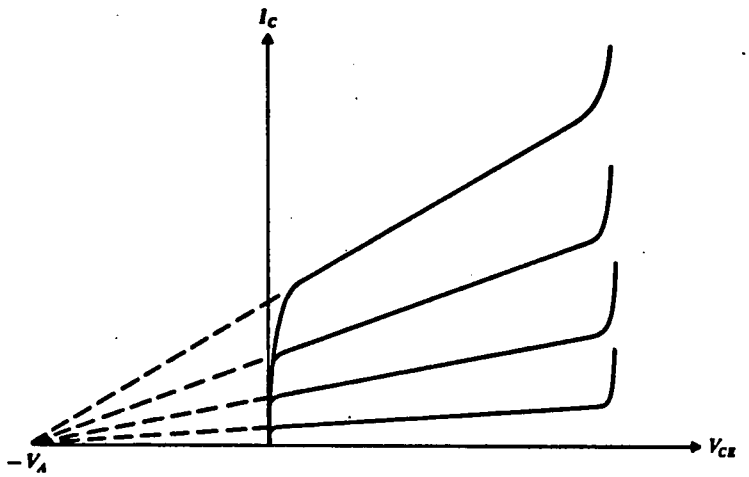

Fig. C.2 Plot Showing the Effects of Early Voltage

This equation tells one that when designs are performed with current ratioing techniques, the transistor collector-to-emitter voltages must always be considered.

APPENDIX D

SPICE SIMULATION

Computer simulations for the circuits blocks can be performed on a 16-bit personal computer and a program called PSPICE, a mini form of the popular SPICE. The program will essentially produce the same results as SPICE, except the size of the circuit will be limited and the run times will be longer on a PC.

A list of model parameters is included in Table D.1, and an example of a simple circuit with generic device parameters is included to illustrate the capabilities of the simulation program. (See Fig. D.1.) The computer run of the circuit shows that dc calculations, ac performance, transfer characteristics, operating points, sensitivities, noise investigation, and Fourier analysis are all possible with the program.

Table D.1 SPICE Model Parameters

```
        **** SPICE CIRCUIT SIMULATION EXAMPLE ****

**********************************************************
*  This program illustrates the capability of the circuit *
*  simulation program,  "PSPICE" that runs on the IBM PC. *
*  Note: some of the data in the printout was omitted,    *
*        so that the printout would fit the thesis        *
*        page format requirement                          *
**********************************************************
.OPT ACCT LIST NODE OPTS NOPAGE RELTOL=.001
.WIDTH OUT=80
.TEMP 27
.TF V(6) VIN
.DC VIN -0.01 0.01 0.001
.AC DEC 10 100 1MEG
.TRAN/OP .1US 10US
.SENS V(6)
.NOISE V(6) VIN
.FOUR 100K V(6)
VING 102 0 DC 1.23V
VIN 2 102 AC 1 SIN(0 0.1 2MEG)
VCC 1 0 DC 7
VG 3 0 1.23
IB 1 14 8U
Q1 4 2 14 QPL
Q1A 0 2 14 QPLA
Q2 5 3 14 QPL
Q2A 0 3 14 QPLA
Q3 4 5 0 QNL
Q4 5 5 0 QNL
Q5 6 4 0 QNL
Q6 0 7 8 QPL
Q7 0 7 9 QPL
Q8 0 7 10 QPL
Q9 0 7 11 QPL
Q10 0 7 12 QPL
Q11 0 6 7 QPL
R1 1 8 CRIM 400
R2 1 9 CRIM 2000
R3 1 10 CRIM 650
R4 1 11 CRIM 500
R5 1 12 CRIM 3000
R6 7 6 CRIM 42K
C 6 4 10PF
```

```
.MODEL QNL NPN (BF=100 BR=10 IS=.5E-15 VA=100 RB=250
+ RC=150 CJE=.59PF CJC=.3PF CJS=2PF XTB=.004)
.MODEL QPL PNP (BF=50 BR=30 IS=.25E-15 VA=50 RB=800
+ RC=120 CJE=.04PF CJC=.20PF)
.MODEL QPLA PNP (BF=50 BR=30 IS=.75E-15 VA=50 RB=800
+ RC=53 CJE=.08PF CJC=.60PF)
.PRINT DC V(6) V(3) V(4) V(7) V(5) V(8) V(9)
.PRINT AC VDB(6) VP(6) VDB(7) VP(7) VDB(5) VP(5) VDB(8) VP(8)
.PLOT AC VDB(6) VP(6)
.PLOT TRAN V(6)
.END
```

```
****     ELEMENT NODE TABLE
     0    VING     VCC      V6       Q1       Q1A
          Q1A      Q2       Q2A      Q2A      Q3
          Q3       Q4       Q4       Q5       Q5
          Q6       Q6       Q7       Q7       Q8
          Q8       Q9       Q9       Q10      Q10
          Q11      Q11

     1    R1       R2       R3       R4       R5
          VCC      IB
     2    VIN      Q1       Q1A
     3    V6       Q2       Q2A
     4    C        Q1       Q3       Q5
     5    Q2       Q3       Q4       Q4
     6    R6       C        Q5       Q11
     7    R6       Q6       Q7       Q8       Q9
          Q10      Q11
     8    R1       Q6
     9    R2       Q7
    10    R3       Q8
    11    R4       Q9
    12    R5       Q10
    14    IB       Q1       Q1A      Q2       Q2A
   102    VIN      VING
```

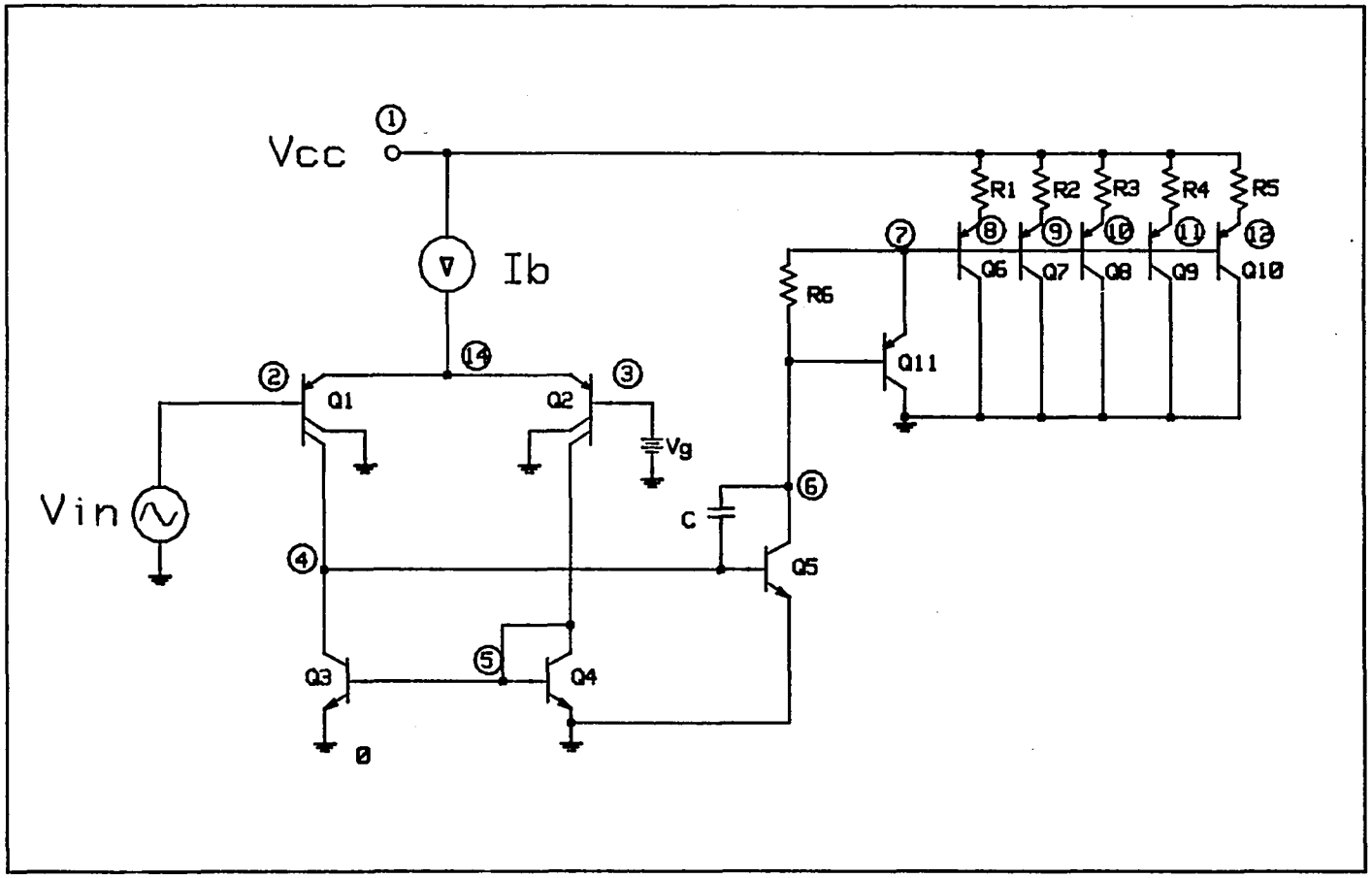

Fig. D.1 SPICE Simulation Example

COMPUTER RUN FOR SPICE SIMULATION

**** BJT MODEL PARAMETERS

	QNL	QPL	QPLA
TYPE	NPN	PNP	PNP
IS	5.00D-16	2.50D-16	7.50D-16
BF	100.000	50.000	50.000
NF	1.000	1.000	1.000
VAF	1.00D+02	5.00D+01	5.00D+01
BR	10.000	30.000	30.000
NR	1.000	1.000	1.000
RB	250.000	800.000	800.000
RC	150.000	120.000	53.000
CJE	5.90D-13	4.00D-14	8.00D-14
CJC	3.00D-13	2.00D-13	6.00D-13
CJS	2.00D-12	.00D+00	.00D+00
XTB	4.00D-03	.00D+00	.00D+00

**** RESISTOR MODEL PARAMETERS

	CRIM
R	1.00D+00
TC1	2.64D-03
TC2	2.80D-06

**** CIRCUIT ELEMENT SUMMARY

**** RESISTORS

NAME	NODES		MODEL	VALUE	TC1
R1	1	8	CRIM	4.00D+02	2.64D-03
R2	1	9	CRIM	2.00D+03	2.64D-03
R3	1	10	CRIM	6.50D+02	2.64D-03
R4	1	11	CRIM	5.00D+02	2.64D-03
R5	1	12	CRIM	3.00D+03	2.64D-03
R6	7	6	CRIM	4.20D+04	2.64D-03

*** CAPACITORS AND INDUCTORS

NAME	NODES	MODEL	IN COND	VALUE

```
    C          6   4              .00D+00  1.00D-11


*** INDEPENDENT SOURCES

 NAME  NODES   DC VALUE   AC VALUE   AC PHASE   TRANSIENT

 VIN  2  102    .00D+00   1.00D+00    .00D+00  SIN
                            OFFSET.......    .00D+00
                            AMPLITUDE....    1.00D-01
                            FREQUENCY....    2.00D+06
                            DELAY........    .00D+00
                            THETA........    .00D+00
                            PHASE........        .0
 VING 102   0   1.23D+00    .00D+00    .00D+00
 VCC    1   0   7.00D+00    .00D+00    .00D+00
 VB     3   0   1.23D+00    .00D+00    .00D+00
 IB     1  14   8.00D-06    .00D+00    .00D+00

**** BIPOLAR JUNCTION TRANSISTORS

     NAME        C   B   E   S  MODEL      AREA

     Q1          4   2  14   0  QPL        1.000
     Q1A         0   2  14   0  QPLA       1.000
     Q2          5   3  14   0  QPL        1.000
     Q2A         0   3  14   0  QPLA       1.000
     Q3          4   5   0   0  QNL        1.000
     Q4          5   5   0   0  QNL        1.000
     Q5          6   4   0   0  QNL        1.000
     Q6          0   7   8   0  QPL        1.000
     Q7          0   7   9   0  QPL        1.000
     Q8          0   7  10   0  QPL        1.000
     Q9          0   7  11   0  QPL        1.000
     Q10         0   7  12   0  QPL        1.000
     Q11         0   6   7   0  QPL        1.000
```

```
****     OPTION SUMMARY

DC ANALYSIS -

    GMIN   =  1.000D-12
    RELTOL =  1.000D-03
    ABSTOL =  1.000D-09
    VNTOL  =  5.000D-05
    ITL1   =     40
    ITL2   =     20
    PIVTOL =  1.000D-13
    PIVREL =  1.000D-03
TRANSIENT ANALYSIS -

    CHGTOL =  1.000D-14
    TRTOL  =  7.000D+00
    ITL3   =      4
    ITL4   =     10
    ITL5   =   5000

MISCELLANEOUS -

    LIMPTS =    201
    LIMTIM =      2
    CPTIME = 100000000.
    NUMDGT =      4
    TNOM   =    27.000
    DEFL   =  1.000D-04
    DEFW   =  1.000D-04
    DEFAD  =   .000D+00
    DEFAS  =   .000D+00

****     TEMPERATURE-ADJUSTED VALUES
         TEMPERATURE =   35.000 DEG C

**** RESISTORS

NAME         VALUE

R1         4.085D+02
R2         2.043D+03
R3         6.638D+02
R4         5.106D+02
R5         3.064D+03
R6         4.289D+04
```

**** BJT MODEL PARAMETERS

NAME	IS	BF	ISE	BR
QNL	5.000D-16	1.000D+02	.000D+00	1.000D+01
QPL	2.500D-16	5.000D+01	.000D+00	3.000D+01
QPLA	7.500D-16	5.000D+01	.000D+00	3.000D+01

	SC	VJE	VJC
QNL	.000D+00	7.500D-01	7.500D-01
QPL	.000D+00	7.500D-01	7.500D-01
QPLA	.000D+00	7.500D-01	7.500D-01

**** DC TRANSFER CURVES
TEMPERATURE = 27.000 DEG C

VIN	V(6)	V(3)	V(4)	V(5)
-1.000E-02	1.064E-01	1.230E+00	6.437E-01	5.473E-01
-9.000E-03	1.242E-01	1.230E+00	6.434E-01	5.478E-01
-8.000E-03	2.069E-01	1.230E+00	6.429E-01	5.484E-01
-7.000E-03	1.218E+00	1.230E+00	6.398E-01	5.490E-01
-6.000E-03	2.369E+00	1.230E+00	6.361E-01	5.496E-01
-5.000E-03	3.622E+00	1.230E+00	6.318E-01	5.501E-01
-4.000E-03	4.901E+00	1.230E+00	6.266E-01	5.507E-01
-3.000E-03	5.605E+00	1.230E+00	6.200E-01	5.512E-01
-2.000E-03	5.817E+00	1.230E+00	6.113E-01	5.517E-01
-1.000E-03	6.025E+00	1.230E+00	5.980E-01	5.522E-01
-1.301E-18	6.248E+00	1.230E+00	5.700E-01	5.527E-01
1.000E-03	6.653E+00	1.230E+00	1.355E-01	5.532E-01
2.000E-03	6.653E+00	1.230E+00	8.635E-02	5.536E-01
3.000E-03	6.653E+00	1.230E+00	7.050E-02	5.540E-01
4.000E-03	6.653E+00	1.230E+00	6.096E-02	5.544E-01
5.000E-03	6.653E+00	1.230E+00	5.407E-02	5.548E-01
6.000E-03	6.653E+00	1.230E+00	4.892E-02	5.551E-01
7.000E-03	6.653E+00	1.230E+00	4.476E-02	5.555E-01
8.000E-03	6.653E+00	1.230E+00	4.126E-02	5.559E-01
9.000E-03	6.653E+00	1.230E+00	3.827E-02	5.562E-01
1.000E-02	6.653E+00	1.230E+00	3.567E-02	5.566E-01

**** DC TRANSFER CURVES
TEMPERATURE = 27.000 DEG C

LEGEND:

*: V(6)
+: V(2)

VIN	V(6)				
(*)———	.000D+00	2.000D+00	4.000D+00	6.000D	
(+)———	1.220D+00	1.230D+00	1.240D+00	1.250D	
-1.000D-02	1.064D-01	+*	.	.	.
-9.000D-03	1.242D-01	.X	.	.	.
-8.000D-03	2.069D-01	.* +	.	.	.
-7.000D-03	1.218D+00	. + *	.	.	.
-6.000D-03	2.369D+00	. +	. *	.	.
-5.000D-03	3.622D+00	. +	.	* .	.
-4.000D-03	4.901D+00	. +	.	.	* .
-3.000D-03	5.605D+00	. +	.	.	* .
-2.000D-03	5.817D+00	. +	.	.	*.
-1.000D-03	6.025D+00	. +.		.	*
-1.301D-18	6.248D+00	. +		.	. *
1.000D-03	6.653D+00	. .+		.	. *
2.000D-03	6.653D+00	. . +		.	. *
3.000D-03	6.653D+00	. . +		.	. *
4.000D-03	6.653D+00	. . +		.	. *
5.000D-03	6.653D+00	. . +		.	. *
6.000D-03	6.653D+00	. . +		.	. *
7.000D-03	6.653D+00	. . +		.	. *
8.000D-03	6.653D+00	. . +		.	. *
9.000D-03	6.653D+00	. . +.		.	. *
1.000D-02	6.653D+00	. . +		.	. *

**** SMALL SIGNAL BIAS SOLUTION
TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	7.0000	(2)	1.2300	(3)	1.230
(4)	.5700	(5)	.5527	(6)	6.2478
(7)	6.3303	(8)	6.9877	(9)	6.9694
(10)	6.9832	(11)	6.9857	(12)	6.9635
(14)	1.8008	(102)	1.2300		

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VIN	7.679D-08
VING	7.679D-08
VCC	-1.207D-04
VG	7.679D-08

TOTAL POWER DISSIPATION 8.03D-04 WATTS

**** OPERATING POINT INFORMATION
TEMPERATURE = 27.000 DEG C

**** BIPOLAR JUNCTION TRANSISTORS

	Q1	Q1A	Q2	Q2A	Q3
MODEL	QPL	QPLA	QPL	QPLA	QNL
IB	-1.92E-08	-5.76E-08	-1.92E-08	-5.76E-08	9.55E-09
IC	-9.73E-07	-2.95E-06	-9.74E-07	-2.95E-06	9.55E-07
VBE	-.571	-.571	-.571	-.571	.553
VBC	.660	1.23	.677	1.23	-.172E-01
VCE	-1.23	-1.80	-1.25	-1.80	.570
BETADC	50.7	51.2	50.7	51.2	100.
GM	3.76E-05	1.14E-04	3.77E-05	1.14E-04	3.69E-05
RPI	1.35E+06	4.49E+05	1.35E+06	4.49E+05	2.71E+06
RX	8.00E+02	8.00E+02	8.00E+02	8.00E+02	2.50E+02
RO	5.20E+07	1.74E+07	5.20E+07	1.74E+07	1.05E+08
CPI	5.89E-14	1.18E-13	5.89E-14	1.18E-13	8.58E-13
CMU	1.62E-13	4.36E-13	1.62E-13	4.36E-13	2.98E-13
CBX	.00E+00	.00E+00	.00E+00	.00E+00	.00E+00
CCS	.00E+00	.00E+00	.00E+00	.00E+00	2.00E-12
BETAAC	50.6	51.2	50.7	51.2	100.
FT	2.70E+07	3.28E+07	2.72E+07	3.28E+07	5.08E+06

	Q6	Q7	Q8	Q9
MODEL	QPL	QPL	QPL	QPL
IB	-5.37E-07	-2.67E-07	-4.52E-07	-4.98E-07
IC	-3.02E-05	-1.50E-05	-2.54E-05	-2.80E-05
VBE	-.657	-.639	-.653	-.655
VBC	6.33	6.33	6.33	6.33
VCE	-6.99	-6.97	-6.98	-6.99
BETADC	56.3	56.3	56.3	56.3
GM	1.17E-03	5.81E-04	9.83E-04	1.08E-03
RX	8.00E+02	8.00E+02	8.00E+02	8.00E+02
RO	1.86E+06	3.75E+06	2.21E+06	2.01E+06
CPI	6.28E-14	6.20E-14	6.26E-14	6.27E-14
CMU	9.54E-14	9.53E-14	9.54E-14	9.54E-14
CBX	.00E+00	.00E+00	.00E+00	.00E+00
CCS	.00E+00	.00E+00	.00E+00	.00E+00
BETAAC	56.3	56.3	56.3	56.3
FT	1.18E+09	5.88E+08	9.91E+08	1.09E+09

**** SMALL-SIGNAL CHARACTERISTICS

V(6)/VIN = 2.430D+02
INPUT RESISTANCE AT VIN = 6.698D+05
OUTPUT RESISTANCE AT V(6) = 6.425D+04

**** DC SENSITIVITY ANALYSIS

TEMPERATURE = 27.000 DEG C

DC SENSITIVITIES OF OUTPUT V(6)

ELEMENT NAME	ELEMENT VALUE	ELEMENT SENSITIVITY (VOLTS/UNIT)	NORMALIZED SENSITIVITY (VOLTS/PERCENT)
R1	4.000D+02	-9.536D-06	-3.814D-05
R2	2.000D+03	-1.606D-06	-3.212D-05
R3	6.500D+02	-6.056D-06	-3.937D-05
R4	5.000D+02	-7.818D-06	-3.909D-05
R5	3.000D+03	-9.219D-07	-2.766D-05
R6	4.200D+04	-1.963D-06	-8.245D-04
VIN	.000D+00	2.430D+02	.000D+00
VING	1.230D+00	2.430D+02	2.988D+00
VCC	7.000D+00	9.985D-01	6.989D-02
V6	1.230D+00	-2.430D+02	-2.988D+00
IB	8.000D-06	-1.579D+04	-1.263D-03

Q1

RB	8.000D+02	4.703D-06	3.763D-05
RC	1.200D+02	1.218D-07	1.462D-07
RE	0.	0.	0.
BF	5.000D+01	-8.132D-05	-4.066D-05
ISE	0.	0.	0.
BR	3.000D+01	1.868D-12	5.603D-13
ISC	0.	0.	0.
IS	2.500D-16	-2.534D+16	-6.334D-02
NE	1.500D+00	.000D+00	.000D+00
NC	2.000D+00	.000D+00	.000D+00
IKF	0.	0.	0.
IKR	0.	0.	0.
VAF	5.000D+01	1.651D-03	8.257D-04
VAR	0.	0.	0.
RB	8.000D+02	-1.055D-07	-8.440D-07
RC	5.300D+01	-2.683D-09	-1.422D-09
RE	0.	0.	0.
BF	5.000D+01	-1.649D-05	-8.246D-06
ISE	0.	0.	0.
BR	3.000D+01	-1.222D-15	-3.665D-16
ISC	0.	0.	0.
IS	7.500D-16	6.319D+13	4.739D-04
NE	1.500D+00	.000D+00	.000D+00
NC	2.000D+00	.000D+00	.000D+00
IKF	0.	0.	0.
IKR	0.	0.	0.
VAF	5.000D+01	-2.236D-05	-1.118D-05
VAR	0.	0.	0.

**** AC ANALYSIS
TEMPERATURE = 27.000 DEG C

FREQ	VDB(6)	VP(6)
1.000E+02	4.770E+01	-3.081E+00
1.259E+02	4.769E+01	-3.876E+00
1.585E+02	4.768E+01	-4.875E+00
1.995E+02	4.766E+01	-6.129E+00
2.512E+02	4.763E+01	-7.699E+00
3.162E+02	4.759E+01	-9.659E+00
3.981E+02	4.752E+01	-1.209E+01
5.012E+02	4.741E+01	-1.510E+01

6.310E+02	4.724E+01	-1.876E+01
7.943E+02	4.699E+01	-2.316E+01
1.000E+03	4.661E+01	-2.831E+01
1.259E+03	4.608E+01	-3.416E+01
1.585E+03	4.535E+01	-4.053E+01
1.995E+03	4.439E+01	-4.714E+01
2.512E+03	4.321E+01	-5.366E+01
3.162E+03	4.182E+01	-5.979E+01
3.981E+03	4.026E+01	-6.529E+01
5.012E+03	3.856E+01	-7.008E+01
6.310E+03	3.676E+01	-7.414E+01
7.943E+03	3.489E+01	-7.755E+01
1.000E+04	3.297E+01	-8.039E+01
1.259E+04	3.102E+01	-8.278E+01
1.585E+04	2.906E+01	-8.480E+01
1.995E+04	2.708E+01	-8.656E+01
2.512E+04	2.510E+01	-8.815E+01
3.162E+04	2.310E+01	-8.963E+01
3.981E+04	2.111E+01	-9.110E+01
5.012E+04	1.911E+01	-9.263E+01
6.310E+04	1.712E+01	-9.430E+01
7.943E+04	1.512E+01	-9.620E+01
1.000E+05	1.312E+01	-9.842E+01
1.259E+05	1.113E+01	-1.011E+02
1.585E+05	9.134E+00	-1.043E+02
1.995E+05	7.143E+00	-1.083E+02
2.512E+05	5.157E+00	-1.132E+02
3.162E+05	3.178E+00	-1.191E+02
3.981E+05	1.209E+00	-1.264E+02
5.012E+05	-7.454E-01	-1.352E+02
6.310E+05	-2.683E+00	-1.456E+02
7.943E+05	-4.603E+00	-1.575E+02
1.000E+06	-6.508E+00	-1.707E+02

INITIAL TRANSIENT SOLUTION
TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	7.0000	(2)	1.2300	(3)	1.2300
(4)	.5700	(5)	.5527	(6)	6.2478
(7)	6.3303	(8)	6.9877	(9)	6.9694
(10)	6.9832	(11)	6.9857	(12)	6.9635

(14) 1.8008 (102) 1.2300

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VIN	7.679D-08
VING	7.679D-08
VCC	-1.207D-04
VG	7.679D-08

TOTAL POWER DISSIPATION 8.03D-04 WATTS

**** OPERATING POINT INFORMATION
TEMPERATURE = 27.000 DEG C

**** BIPOLAR JUNCTION TRANSISTORS

	Q1	Q1A	Q2	Q2A	Q3
MODEL	QPL	QPLA	QPL	QPLA	QNL
IB	-1.92E-08	-5.76E-08	-1.92E-08	-5.76E-08	9.55E-09
IC	-9.73E-07	-2.95E-06	-9.74E-07	-2.95E-06	9.55E-07
VBE	-.571	-.571	-.571	-.571	.553
VBC	.660	1.23	.677	1.23	-.172E-01
VCE	-1.23	-1.80	-1.25	-1.80	.570
BETADC	50.7	51.2	50.7	51.2	100.
GM	3.76E-05	1.14E-04	3.77E-05	1.14E-04	3.69E-05
RPI	1.35E+06	4.49E+05	1.35E+06	4.49E+05	2.71E+06
RX	8.00E+02	8.00E+02	8.00E+02	8.00E+02	2.50E+02
RO	5.20E+07	1.74E+07	5.20E+07	1.74E+07	1.05E+08
CPI	5.89E-14	1.18E-13	5.89E-14	1.18E-13	8.58E-13
CMU	1.62E-13	4.36E-13	1.62E-13	4.36E-13	2.98E-13
CBX	.00E+00	.00E+00	.00E+00	.00E+00	.00E+00
CCS	.00E+00	.00E+00	.00E+00	.00E+00	2.00E-12
BETAAC	50.6	51.2	50.7	51.2	100.
FT	2.70E+07	3.28E+07	2.72E+07	3.28E+07	5.08E+06

*** FOURIER ANALYSIS TEMPERATURE = 27.000 DEG C

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(6)

DC COMPONENT = 6.258D+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000D+05	9.335D-04	1.000000	-72.546	.000
2	2.000D+05	8.463D-04	.906606	-81.171	-8.624
3	3.000D+05	8.584D-04	.919609	-88.159	-15.613
4	4.000D+05	8.135D-04	.871434	-97.764	-25.218
5	5.000D+05	7.901D-04	.846354	-100.829	-28.283
6	6.000D+05	7.707D-04	.825629	-106.365	-33.819
7	7.000D+05	7.372D-04	.789685	-110.344	-37.798
8	8.000D+05	7.093D-04	.759811	-113.394	-40.848
9	9.000D+05	6.799D-04	.728306	-116.308	-43.762

TOTAL HARMONIC DISTORTION = 235.718821 PERCENT

JOB CONCLUDED

**** JOB STATISTICS SUMMARY

NUNODS	NCNODS	NUMNOD	NUMEL	DIODES	BJTS	JFETS	MFETS	GASFETS
15	15	41	25	0	13	0	0	0

NUMTEM	ICVFLG	JTRFLG	JACFLG	INDISE	NDGD
1	21	101	41	1	0

NSTOP	NTTAR	NTTBR	NTTOV	IFILL	IOPS	PERSPA
45.	167.	177.	77.	10.	337.	91.259

NUMTTP	NUMRTP	NUMNIT	MEMUSE/MAXMEM	COPYCNT

167. 0. 773. 8544/ 64000 15984/221280
44612.

	SECONDS	ITERATIONS
READIN	12.30	
SETUP	1.37	
DCSWEEP	44.49	99.
BIASPNT	40.03	50.
MATSOL	112.25	4.
ACAN	46.69	41.
TRANAN	435.67	773.
OUTPUT	30.66	
LOAD	235.75	
OVERHEAD	22.85	
TOTAL JOB TIME	634.06	

APPENDIX E

INTEGRATED CIRCUITS MICROPHOTOGRAPH WITH FUNCTIONS LABELED

To illustrate the completed chip and the sections of the chip referred to in this paper, a microphotograph is shown in Fig. E.1. Each section is labeled with the letters "a" through "g". The function of each section is given in the following table, Table E.1.

Table E.1 Designated Sections of the Completed Chip

Section	Function
a	LED Current Sources
b	Audio Current Source
c	Squarewave Generator
d	Negative Voltage Generator
e	Data Transistors
f	Data Registers
g	Voltage Regulator and Chip Bias

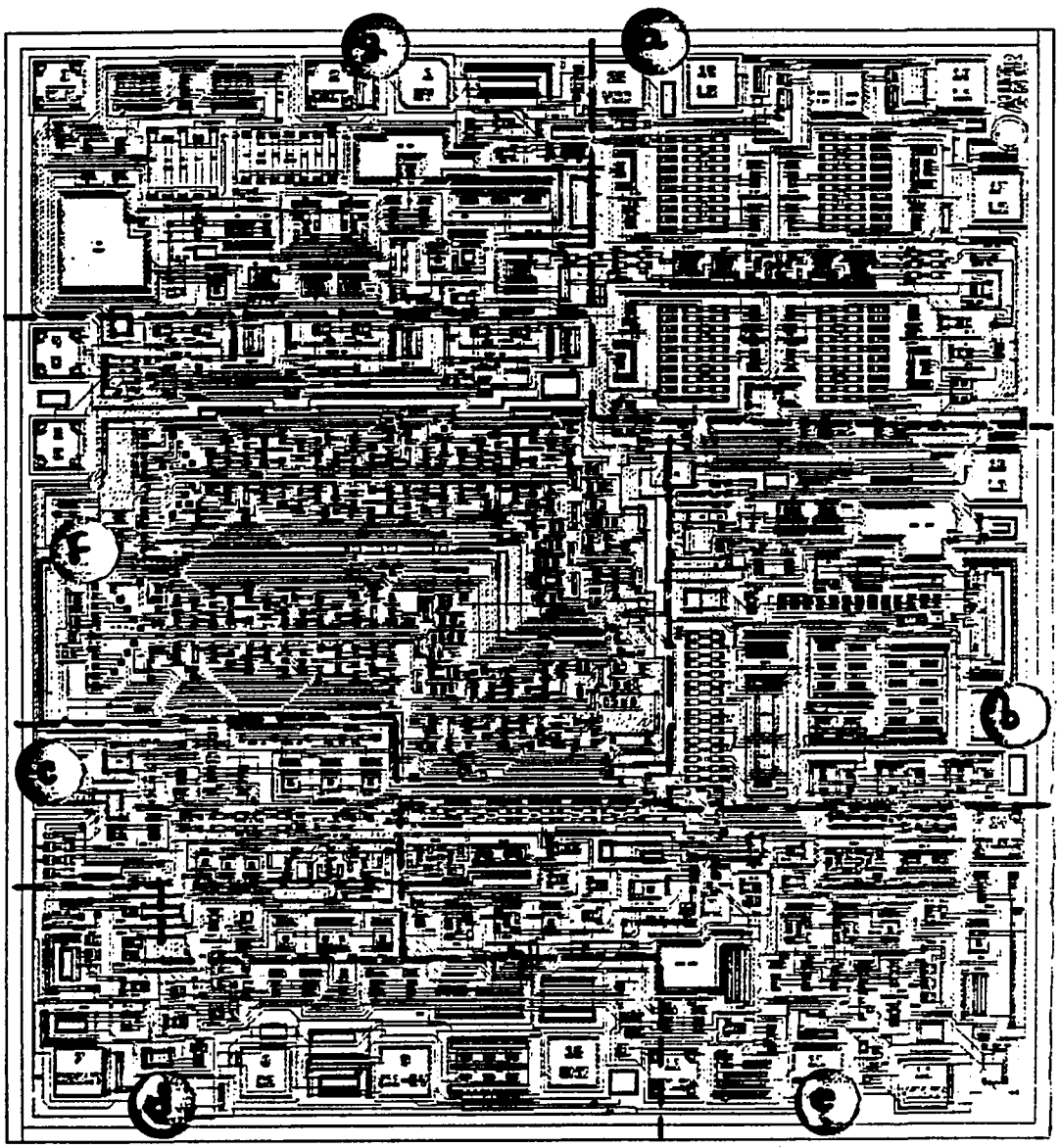

Fig. E.1 IC Microphotograph with Functions Labeled

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