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The University of Arizona, 1988

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THERMAL CHARACTERIZATION OF VLSI PACKAGING

by

DAVID ALLEN SHOPE

A Thesis Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

In Partial Fulfillment of the Requirements
For the Degree of

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In the Graduate College

THE UNIVERSITY OF ARIZONA

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21 JAN 88
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ABSTRACT

With electronic packaging becoming more complex, simple hand methods to model the thermal performance of the package are insufficient. As computer aided modeling methods came into use, a test system was developed to verify the predictions produced by such modeling methods. The test system is evaluated for operation and performance. Further, the premise of this type of test (the accurate calibration of packaged temperature-sensitive-parameter devices can be done) is investigated using a series of comparative tests. From this information, causes of possible/probable errors in calibration are identified and related to the different methodologies and devices used. Finally, conclusions are presented regarding the further improvement of the test system and methodologies used in this type of testing.

Chapter 1.

Introduction

With the continual increase in size and power of VLSI circuitry, the packaging of such circuits becomes critical to the performance of the circuits. With rising costs of production the need to predict the thermal response of the package before production starts is necessary. To meet this need computational methods have been developed but these methods need to be verified through experimental means.

In the past simple one-dimensional thermal calculations were sufficient but with the increase of die size and power dissipation, non-uniform and transient power dissipation phenomena had to be addressed. Methods to model these phenomena using three-dimensional finite difference programs have been developed [1]. To verify the predictions produced by such modeling methods, a test system was designed [2,3]. When this system was first designed the thoughts on precision, accuracy and resolution were only guesses as to what the eventual end product would be. It was thought that a $\frac{1}{2}$ ° Celsius resolution with an accuracy of ± 1° Celsius would be sufficient. It was also felt that high speed data acquisition could only be handled through sample and hold type circuitry. As the system was

developed, it was found that higher resolution and accuracy was needed and high speed data acquisition could be handled without sample and hold circuitry. As time passed it became apparent that not only was the development of test equipment sufficient but that the methodologies, types of test equipment and measurement standards had to be analyzed for errors in results.

The thesis work started with an initial conceptual design and unpopulated boards of the Computer Controlled Thermal Characterization System (CCTCS). Through engineering analysis and redesign, the CCTCS was developed into a functioning piece of test equipment. Upon the completion of the CCTCS, the premise of this type of measurement was examined. The premise is the accurate calibration of a packaged temperature-sensitive-parameter (TSP) device. From this work, ideas for further development of the CCTCS and test chips, and areas of further research are discussed.

The thesis is organized as follows. Chapter 2 explains the circuits used in the CCTCS, first as block diagrams and then as individual circuits. Chapter 3 discusses the development, operation and performance of the CCTCS. Chapter 4 examines the premise of this type of measurement and Chapter 5 presents ideas to further this type of work.

Chapter 2.

Hardware Description

The CCTCS can be split into two parts: 1) the interface control board; 2) the heater sensor board. The interface control board interfaces between the computer and the heater sensor board. The interface control board (I-C board) also conditions analog signals from the heater sensor board and digitizes these signals. The heater sensor board (H-S board) interfaces between the device under test and the CCTCS. The H-S board provides constant current sources for TSP devices and switched current sources for turning on power dissipating devices. The misnomer, heater, comes from that turning on power dissipating devices heats the test structure. The H-S board also provides the logic for detecting which sensor is being sensed and whether a power dissipating device is on or off.

2.1 Interface Control Board Block Diagram

The I-C board can be broken down into seven blocks as depicted in Figure 1. The I-C board interfaces between the computer and the CCTCS through eight data lines and four control lines. These are explained in more detail in section 2.3.1. The tri-state buffers are used to prevent

bus contention on the data lines. The logic block deciphers the control lines to determine the mode of operation the CCTCS is currently performing. The offset and gain block prepares the analog signal from the H-S board for digital conversion. This block sets the range (window) of temperatures and the resolution (bits per degree) of the CCTCS, as explained in section 3.4. The delay block allows time for the analog signal to settle after conditioning before the A/D block converts the analog signal to digital information. The NOR block lets the computer know that the CCTCS is in either; delay before A/D conversion, or presently doing conversion.

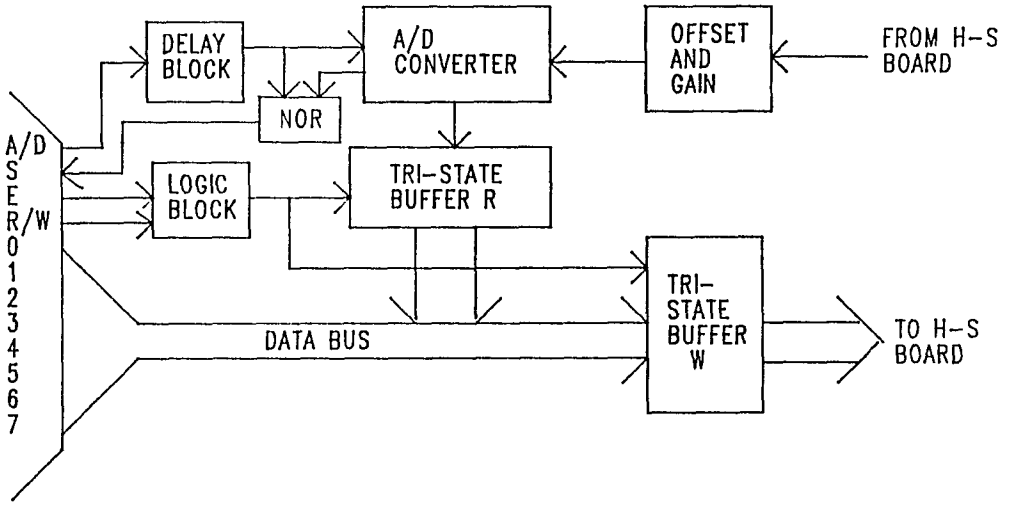


Figure 1. Interface Control block diagram.

2.2 Heater Sensor Board Block Diagram

The H-S board can be broken down into seven blocks as shown in Figure 2. The CCTCS was originally designed to handle four equivalent boards in parallel. This capability has not yet been fully implemented. Thus the system handles only one board of sixteen sensors and sixteen switched power sources (heaters). The logic block determines whether it is in the sense mode or the heater mode and which one of sixteen of either is being addressed. The heater demultiplexer is used to determine the switched current source that is being addressed while the sensor multiplexer determines which sensor is being addressed. Sensor current sources are constant current sources used for biasing TSP devices. The switchable current sources are used to turn on or off power dissipating devices. The control bus is used to communicate with the multiplexers/demultiplexers and also allows for a reset to turn off the switchable current sources for initialization. The gain block amplifies the analog signal from the TSP.

2.3 Description of Circuits I-C Board

In this section the I-C board individual circuits are explained.

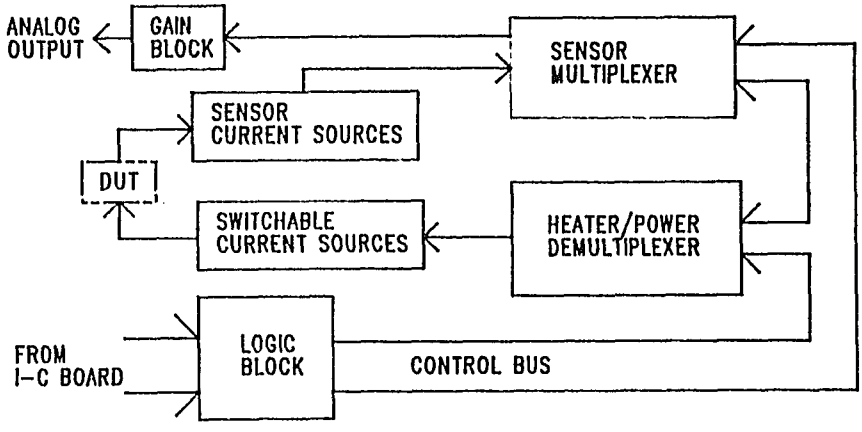


Figure 2. Heater Sensor block diagram.

2.3.1 Eight data and four control lines.

These lines come from the computer parallel port and are used to pass data to the computer and instructions to the CCTCS. The four control lines are the A/D,S,E,R/W. The A/D line is used to control the delay block and goes high to start a delay cycle. The S line is used to tell the computer that analog to digital conversion is being performed. The S line goes low during the delay cycle and during the actual conversion. The E line enables the logic block to control the tri-state buffers and is high for enable. The R/W line determines whether the CCTCS is reading data from the computer to the H-S board or writing to the computer from the A/D converter. The line is high during read and low during write. The eight data lines are

used to write instructions to the H-S board and are discussed in that section. Also the data lines are used to send the information from the A/D converter to the computer for further processing.

2.3.2 Tri-state buffers

The tri-state buffers are standard octal D flip-flops controlled by two inputs with a possible hi-impedance (hi-Z) output state (74S373). The first control input, the Z input, determines whether the output of the buffer is in the hi-Z state or, alternatively, the output states of the flip-flops. A logic one on the Z input puts the buffer output into the hi-Z state. The second control input, the E input, determines whether the input to the D flip-flops is passed to their output. A logic one allows the input data to be transferred to the output of the D flip-flops.

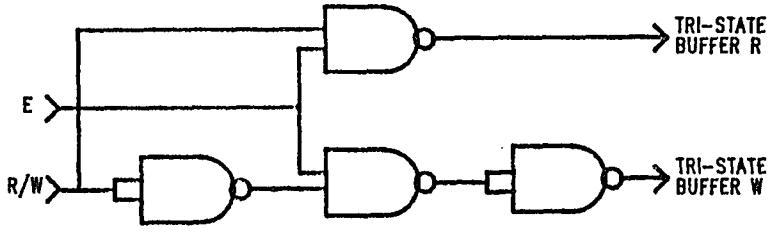
The write tri-state buffer has the Z input at logic zero so that the last instruction is always held at the output. Thus, the H-S board would not have its inputs floating. The E input is controlled by the logic block and determines if data from the computer is being passed to the H-S board.

The read tri-state buffer has the E input kept at logic one to allow all data output from the A/D shifted to the output of the D flip-flops. The Z input is controlled

by the logic block and allows the buffer to be in the data transfer state only when the computer is reading from the CCTCS.

2.3.3 Logic block

The logic block is a two input to two output decoder used to control the tri-state buffers. The decoding is accomplished using a single two input quad NAND (7400) circuit. The circuit diagram and logic table can be seen in Figure 3. It is noted that the output to the read buffer has a one gate delay while the output to the write buffer has a three gate delay. This allows enough time delay in switching from read to write as to not allow erroneous data from the A/D to be passed to the H-S board.



E	R/W	R	W
0	*	1	0
1	0	1	1
1	1	0	0

Figure 3. Logic block circuit diagram and truth table.

2.3.4 Offset and gain

The offset and gain are accomplished using a single

op-amp (MC34001) in the inverting gain configuration as seen in Figure 4. The offset is accomplished through the additive input from the analog signal from the H-S board and the offset voltage from the voltage divider consisting of R6, R7 and VR2. The offset voltage is varied by potentiometer VR2. The amount of gain from this stage is determined the variable resistor VR1. The transfer equation from input to output can also be seen in Figure 4.

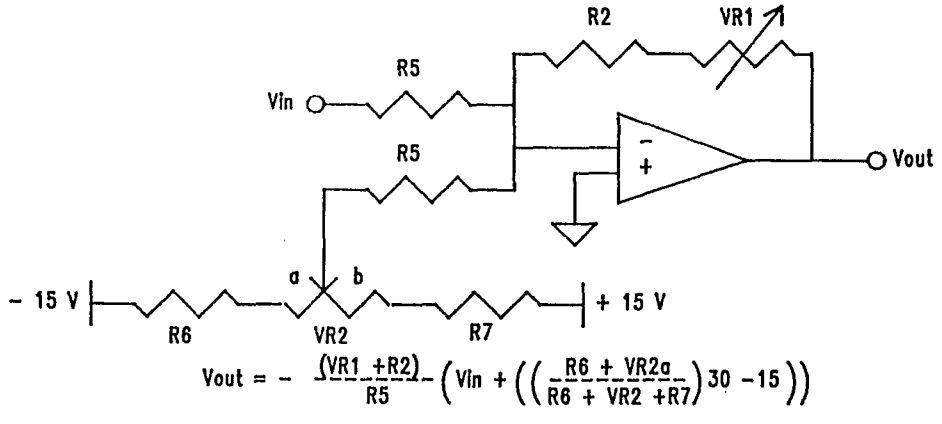


Figure 4. Offset and gain circuit diagram and transfer equation.

2.3.5 Delay circuit

The delay is accomplished using a 74121 variable delay one-shot multivibrator. The delay time is set by the external components VR3 and C1 in accordance with the

specifications of the 74121. The output of the 74121 is low until a low to high transition is seen at the B input. The output then goes high for a period determined by VR3 and C1. The period was left variable since settling times of the analog signal will vary due to the device being sensed and the amount of gain determined by the offset and gain circuitry. The delay circuit is shown in Figure 5.

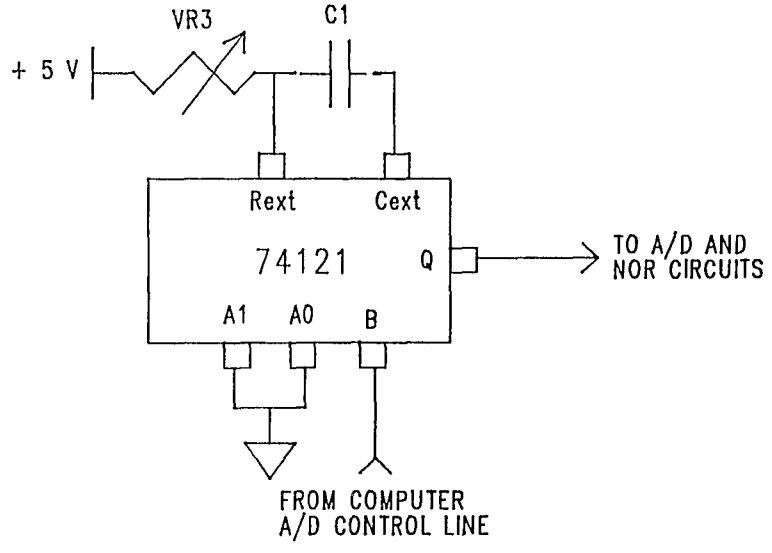


Figure 5. Delay circuit.

2.3.6 Analog to digital converter

The analog to digital converter is an eight bit successive approximation type converter, the Burr Brown ADC 82. The converter is set up for internal clock, 2.8 microsecond conversion time, 0 to 5 volt analog input range

and parallel digital data output. The conversion process is started by a high to low transition on the convert input from the delay circuit. During the conversion process the status line goes high.

2.3.7 NOR circuit

The NOR circuit was not a part of the original design and was implemented during development of the CCTCS. The reason for this circuit is explained in section 3.3.2. Since the circuit was developed at a later time the use of an I.C. was not possible, so a simple DTL gate was implemented using discrete components. The NOR gate output is high except when either the delay circuit output is high or the status output from the A/D is high. The circuit diagram can be seen in Figure 6. Note that the collector voltage and load resistor are part of the computer.

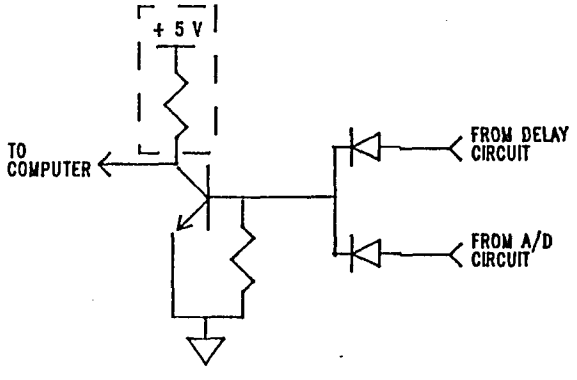


Figure 6. NOR circuit diagram.

2.4 Description of Circuits H-S Board

In this section the circuits used on the H-S board are explained.

2.4.1 Eight bit bus

The incoming eight bit bus can be broken down into five sections. First, zero through two are used as a one out of eight bit decode to choose which heater or sensor in two groups of eight are being addressed. Second, line three is used to determine if the first or second group of eight is being addressed. Third, lines four and five are used to determine which one of four blocks (boards) of sixteen is being addressed. This is useful only if the CCTCS was capable to handle more than one H-S board. Fourth, line six is used to reset all heaters simultaneously. When this line goes high the heaters are reset to the off state. Finally, line seven is used to determine whether the CCTCS is in the heat or sense mode.

2.4.2 Logic block

The logic block of the H-S board serves multiple uses. It determines which of four boards is being addressed, which of four multiplex/demultiplexers per board is being addressed, and provides an ability to reset all switchable current sources on a board to the off state. The circuit diagram is shown in Figure 7. It is noted that the paths

have different gate delays and this will be further discussed in section 3.2.

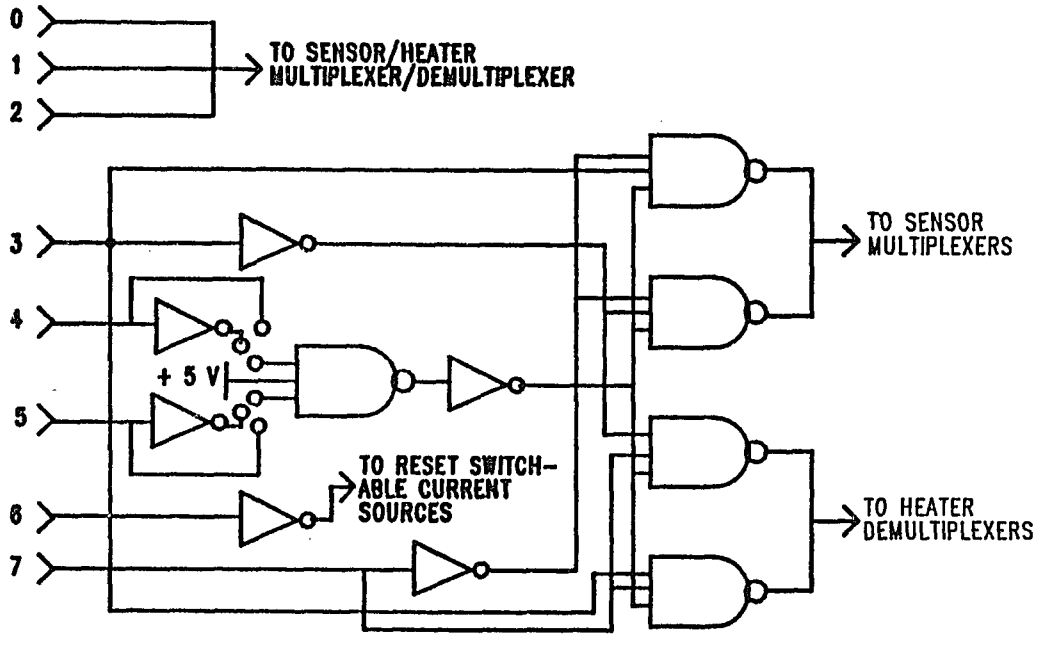


Figure 7. Logic block circuit diagram.

2.4.3 Heater demultiplexer

The heater demultiplexer consists of two three line to eight line decoders (74LS138). The three lines are passed directly from the I-C board and one of two multiplexers is chosen by the logic block. The outputs stay low until an

output is addressed. The output remains high as long as it is addressed.

2.4.4 Sensor multiplex

The sensor multiplex consists of two octal analog switches (MC14051B). The switch is turned on by three lines from the I-C board and one of two octal switches is chosen by the logic block. The analog switches can pass analog signals from 0 to +5 volts. Since voltages seen by the switches are negative, the normal supply voltage sources were modified to handle this problem (see section 3.2).

2.4.5 Sensor current sources

The sensor current sources are large resistors connected from the -15 volt rail to the device under test (DUT). This assumes the DUT is a either a transistor with the base grounded and emitter connected to the resistor or a diode with anode grounded and the cathode connected to the resistor. The resistor used is a 150 KΩ which sets the current value at about .1 mA. Sufficiency of this type of current source is discussed later.

2.4.6 Switched current sources

The switched current sources consist of a J-K flip flop operated in the clocked D mode (74107) and a saturated

switch as seen in Figure 8. The flip-flop is reset from the logic block putting the Q output in the low state. Two diode drops across the diode and base-emitter of Qeven assure that non-zero output of the flip-flop in the low state will not turn on the current source. A low to high transition on the clock input from the heater demultiplexer changes the Q output state from low to high. This high Q output forward biases Qeven which in turn heavily forward biases the base emitter junction of Qodd. This forces Qodd to saturate and the current delivered is approximately D-/R2. This current source also assumes that it is connected to an emitter of a transistor with the base grounded. R4 serves to limit the amount of current from the flip-flop during the high state and to help make sure the switch is off during the low state. R3 serves to limit the current drawn from the base emitter junction of Qodd. Another low to high transition on the clock input changes the Q output from high to low turning off the saturated current switch.

2.4.7 Gain block

The gain block is a non-inverting fixed gain op-amp circuit. The capability for correcting offsets of the op-amp is accomplished by VR1. The op-amp used is a JFET input type (MC34001).

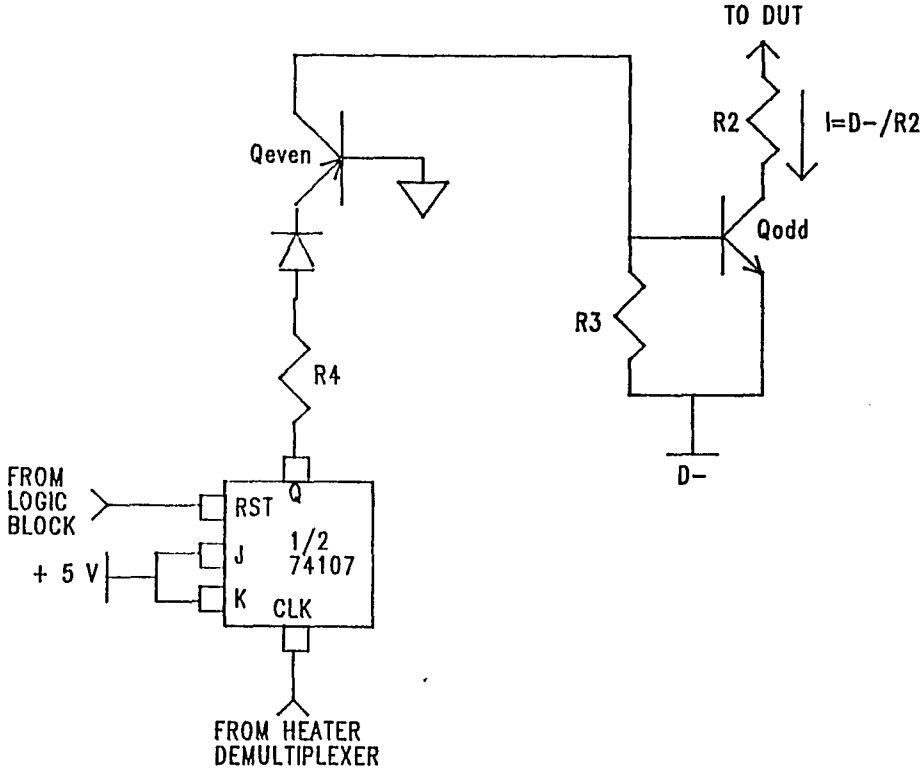


Figure 8. Switched current source.

Chapter 3.

Hardware Development of the CCTCS

Development of the CCTCS started with a schematic without exact specification of discrete components, approximate layout and two unpopulated boards (ie., no components installed but copper runs were done). The development was done in three parts; installation of components and troubleshooting of I-C board, installation of components and troubleshooting of H-S board and packaging of the CCTCS which includes connection of the two boards, power supply connections, connection to the computer and the DUT.

3.1 Development of the I-C Board

The initial development of the I-C board was limited to installation of components and checking of foil runs. Also initial sizes of components for the offset and gain block were specified. Final operational checks had to wait until the computer was connected.

Two problems with the foil runs were found. The first problem was that +5 volts was not connected to the write tri-state buffer and the second being that an output from the A/D was not connected to the write tri-state buffer. It

was also decided at this time to connect the analog ground to the digital ground at the A/D and to double bypass the power supplies per Burr Brown specifications.

The gain of the total circuit was based on a one hundred degree range with a -2mV/°C variation. This gave a total gain of 25 in two stages. Since speed was an objective the gain was evenly split between the stages with the variable gain approximately from 3 to 8. The size of the resistors around the op-amp were kept fairly large (10 KΩ and up) without offset problems due to the type of op-amp.

The offset circuit uses a voltage divider. The current in the voltage divider should be much greater than currents around the op-amp so that the voltage would not be affected by the op-amp circuitry. A current of 1 mA was used with the variable voltage being in the 0 to -5 volt range. This gave a total resistive value of 30 KΩ.

Exact values around of the resistors in this circuit were not important at this time since as further development continued these values would be changed for more stringent specifications.

3.2 Development of the H-S Board

The development of the H-S board could be accomplished in more detail owing to the ability to statically switch

the digital switches used. During this phase of the development, components were installed and checked for correct operation. Also, components for the gain block, sensor current sources and switched current sources were specified.

During this part of the development seven problems with the layout were encountered. Two Q outputs of the flip-flops were shorted together. Four vias were either missing or not drilled through the board. The connections from the outputs from the logic block to the sensor multiplexers was missing. The base of Qeven of the switching current sources was connected to analog ground. Since these are part of the TTL switching function they should be connected to the digital ground. Finally, the sensor current source resistors were laid out as discrete components rather than two 16 pin DIPs. The last problem could only be overcome by "spidering" DIP sockets on the board.

Secondly, certain parts of the circuit had to be redesigned to work. The flip-flops were originally made to work in the J-K mode which simply did not work. They were rewired to work in the D mode which also meant rewiring the logic block. This change also left an extra line free which was used to connect the resets of the flip-flops. This was advantageous in that a single command could set all

switched current sources to the off state.

Another problem that had to be dealt with involved the analog switches. The switches were built to handle analog signals from 0 to +5 volts but careful examination showed the voltages were around -0.7 volts. A quick fix solution was performed by connecting the substrate of the analog switch to -1.5 volts. The -1.5 volts was obtained by creating a voltage divider consisting of R7, R8 and R9 between the -15 volt rail and ground.

Next, components for the switching current sources had to be specified. Diodes used were the only switching diodes available free of charge. The Qodd transistors needed the following characteristics: 1) large β ; 2) large breakdown voltage ; 3) small saturation voltage 4) large current capabilities. The MPSA56 transistor best met these requirements. The MPSA06 transistor was used for Qeven as they were the complement of the MPSA56. R1 was chosen at 1 KΩ such that sufficient current would saturate Qodd. R3 was chosen large, 10 KΩ, so that most of the current would go through the base-emitter junction of Qodd. Finally, it was decided that the current delivered should be approximately equal in mA to the voltage applied at the D- node. This meant for a 1 KΩ resistor with 30 mA maximum current, a 1 watt rating was necessary.

The sensor resistors needed to deliver 0.1 mA between

the -15 volt rail and approximate ground. The resistors also needed to be of high quality with low thermal drift such that aging and thermal affects would not change the resistive value. Therefore, 150 KΩ, 200 PPM, 1% resistors packaged in 16 pin DIPs were used.

Finally, the components for the non-inverting op-amp circuit was needed. The components were chosen for an approximate gain of 5 with the resistors in the 10 to 100 KΩ range.

3.3 Packaging of the CCTCS

Packaging of the CCTCS took on three parts. The first part being the physical packaging including power supplies. The second, connection of the CCTCS to the DUT and finally connection of the CCTCS to the computer. Though the three are not truly separable, the problems involved can be separated.

3.3.1 Physical packaging

First, three power supplies internal to the CCTCS were needed. The power requirements for the power supplies was decided from worst case current drain from the components using the particular supply. For the +5 volt supply it was found that worst case was 403 mA and a simple kit supply with 1 A capabilities was used. The ± 15 volt supply needed

to deliver at least 59.9 mA without voltage degradation. A 200 mA supply from a kit was used. The power supplies were grounded together at the supplies themselves.

The two boards had edge connectors for passing the information from board to board except the analog signal. The edge connectors were 24 single-, and 48 double-sided edge connectors. This is not standard but 22 single-, and 44 double-sided edge connectors are. Therefore, the boards were trimmed to the standard size. Since the boards were not the same width or standard widths a custom card rack had to be built. The rack was enclosed with ventilation holes above and below the power supplies to allow convective heat flow.

Two ten turn potentiometers were installed on the front panel for the gain and offset controls. Also banana jacks were put on the front panel for the two external supplies needed (D- and collector).

Finally, all DC wiring external to the boards was run using shielded twisted pair with the shield connected to ground on one end. This was done to eliminate electromagnetic interference between wires, and outside sources and wires. The analog signal between boards was run using coaxial cable with the ground connected on both ends to eliminate ground differences.

3.3.2 Connection to the computer

Connection to the computer from the CCTCS was done from the I-C board to the parallel port of the computer. Since the wires had to be soldered to the CCTCS the cable had to be custom built. It was also found that the computer that was being used did not have a truly IBM compatible port and thus the computer had to be modified.

The other problems that occurred at this stage were due to either timing problems, which do not show up in the static cases or design flaws. The first problem was that the delay was triggered by the read line on the output of the write tri-state buffer. If the CCTCS were to sense two sensors in sequence then the delay and subsequently the A/D would be triggered only on the first sense command since the read line would not change state. To solve this another line from the computer was introduced to directly trigger the delay. The second problem stemmed from the fact that the output pulse from the A/D status during conversion is short enough that the computer could misinterpret or miss it all together. To solve this problem the NOR circuit was implemented such that the pulse length was increased. The final problem stemmed from the fact that the 3 to 8 code on the H-S board has no gate delays while the multiplexer chosen goes through the logic block having up to four gate delays causing erroneous selection of heaters to be

switched. This was solved by defining an address method that would prevent this from occurring. The address procedure is shown in section 3.4.

3.3.3 Connection to DUT

Connecting the DUT to the CCTCS composes mainly of building a test fixture and associated wiring which allow compatibility with other pieces of test equipment.

The wiring used had to meet two requirements. The first being the ability to handle currents up to 30 mA. The second being the ability to work in temperatures ranging from -20 to 100 °C. Ribbon cable that met these requirements was used. The ribbon cable was connected together using female card connectors with male to male connectors being made to connect the female connectors together.

The test fixture used is a small piece of circuit board with a socket and wiring soldered into the board. The middle of the circuit board is cut out to allow mounting of the test fixture onto a temperature controlled heat sink.

After the test fixture was built a serious problem occurred. This problem was that a transistor type DUT to oscillate. The best explanation is that the transistor forms a Colpitts oscillator as can be seen in [4]. The solution to the problem presented in [4] is not

satisfactory for these types of measurements. The oscillation is dependent on wire length and the collector voltage and appears as a small Early voltage of the device. Though this problem is not totally solved it was found that placement of .1 microfarad capacitors across the collector base connections at the test fixture and wire connectors help eliminate this problem.

3.4 Operation

The hardware operation of the CCTCS can be broken into four parts: 1) the digital addressing procedure; 2) setting the window and range; 3) setting the delay; 4) setting D- and collector voltage supplies.

3.4.1 Addressing Procedure

Due to gate delays the CCTCS hardware must be addressed in certain order or erroneous commands will be passed from the I-C board to the H-S board. A list of the sequences to address the CCTCS is given below.

3.4.1.1 Heater cycle

The heaters are in a toggle mode. The first time they are addressed they turn on the current source and the second time they turn off the current source. Hence, there is no difference between the two sequences but it is

assumed that the computer keeps track of the status of each heater.

1. disable + write + heater number + sense
2. enable + write + heater number + sense
3. enable + write + heater number + heat
4. enable + write + heater number + sense
5. disable + ...

The heater number is the 6 to 64 code on lines 0 through five. Line six is low except during the reset cycle. Sense is line seven high and heat is line seven low. This cycle must be gone through for each individual heater that is turned on.

3.4.1.2 Reset cycle

This cycle resets all heaters at one time.

1. disable + write + sense + ...
2. enable + write + sense + ...
3. enable + write + sense + reset +....
4. enable + write + sense + ...
5. disable

3.4.1.3 Sense cycle

The sense cycles determines which sensor is being sensed and gets the A/D reading. The write tri-state buffer is set up so that the last command to it is kept on the

output allowing the machine to do other processes while the sensor is being measured.

1. disable + write + sensor number + sense
2. enable + write + sensor number + sense
3. strobe A/D
4. check for status going high
5. disable + write + sensor number + sense
6. disable + read +.....
7. enable + read + ...
8. disable + ...

3.4.2 Setting Range(window) and Resolution.

The range and the resolution are functions of the temperatures to be measured and the device under test. The range is defined as the minimum to maximum temperatures and the resolution is defined as bits per degree Celsius. These are controlled by the offset and gain adjustments on the front panel. The range and resolution are not independent of each other but affect one another. There is a total of 256 bits available and it is advisable to use as many as possible in the test procedure to limit quantization error, that is, the error that is always present due to A/D accuracy. The A/D has a minimum accuracy of plus or minus one bit. If the resolution is one bit per degree Celsius then the output will have an accuracy of plus or minus one

degree Celsius but if the resolution is five bits per degree Celsius then the output will have an accuracy of .2 degrees Celsius. The simplest method to accomplish this is to measure the device at the maximum temperature expected and set the offset such that the output is reading 255 (or close proximity), then go to the minimum temperature expected and set the gain control such that the output is reading close to zero. It is noted that just because the output is reading zero or 255 does not mean that this is the actual output. It could well be above 255 or below 0 by an unknown amount. It is best to set it to 254 or less and 1 or more to make sure this error is not present.

3.4.3 Setting the Delay

The delay setting is a function of the difference in the sensor outputs. The larger the difference, the longer the delay must be. The delay is adjusted by VR2 on the I-C board. A measurement of settling time can be seen in section 3.5.

3.4.4 Determining Collector and Heater Voltages

The collector and heater voltages are determined by the amount of power to be dissipated. The heater voltage determines the amount of current that is sunk by the formula given in the power distribution section in the

circuit description section. If the sensors and heaters share the common collector voltage, as with the TTC03 [2,3], then this voltage should be minimized such that the sensors dissipate minimal power. In fact the sensors should minimize power dissipation as will be shown in Chapter 4.

3.5 Performance of the CCTCS

The performance of the CCTCS was measured in four areas. First, the ability to reproduce the same measurement that was performed by another piece of test equipment (accuracy). Second, the ability to reproduce the same measurement (precision). Third, the speed with which analog signals settle at the input of the A/D for setting the delay time. Fourth, the speed ta which consecutive devices may be sensed.

3.5.1 Accuracy

Accuracy of the CCTCS was compared with a Hewlett-Packard (HP) data acquisition system. A test device was calibrated in a dielectric bath system using both systems. Then the device temperature was measured while a power dissipating device was operated at three different levels of power dissipation. The results of these measurements are shown in Table 1. The CCTCS was operated at a resolution of 6.5 bits/°C while the HP system has a resolution of better

than 100 bits/°C.

Power Dissipation	Temperature	
	CCTCS	HP
.531	50.8	52.9
.749	60.2	62.2
.928	66.6	67.7

Table 1. Comparison of CCTCS to HP.

3.5.2 Precision

In this case the precision of the CCTCS is defined as the ability to reproduce an experiment. The experiment involved operating the CCTCS at high-resolution and high-data acquisition rate. A sensing device was measured starting at the same temperature and a power dissipating device was turned on for three different pulse lengths. The results can be seen in Figure 9.

3.5.3 Settling Time of Analog Systems

To measure the settling time of analog signals a worst case scenario was performed. The time measured was from the switching of an analog switch to the input voltage of the A/D being with in one bit of the final voltage. The result is shown in Figure 10.

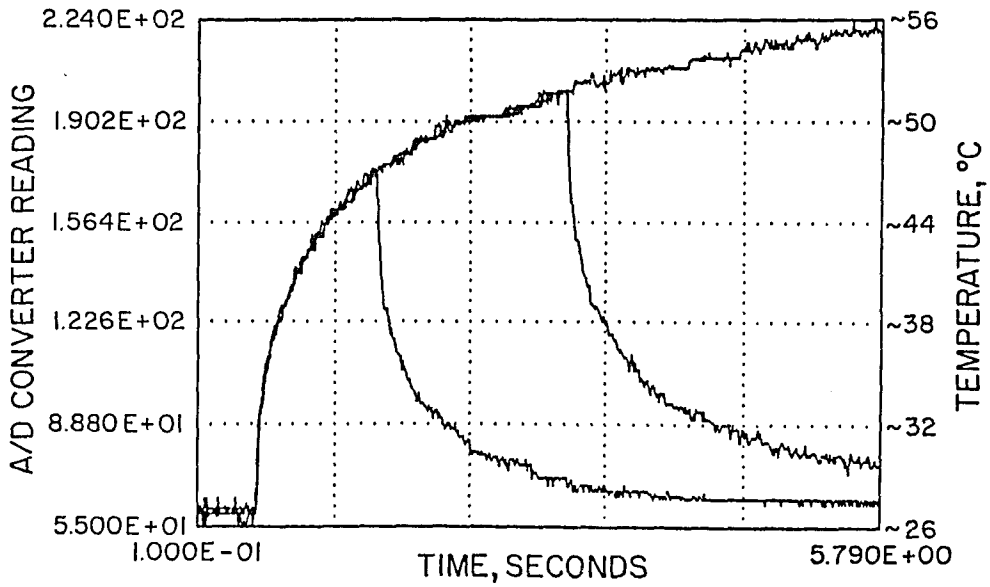
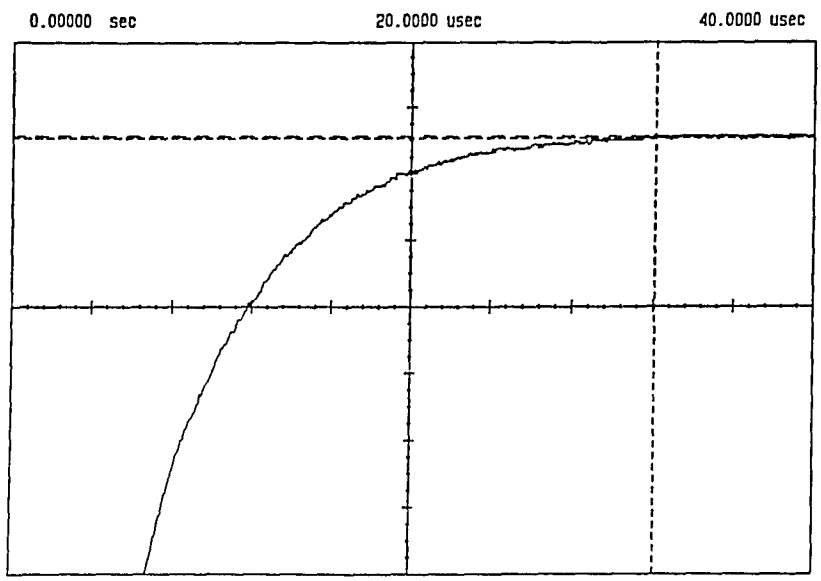


Figure 9. Results of repeatability.



Ch. 1	=	500.0 mvolts/div	Offset	=	2.400 volts
Timebase	=	4.00 usec/div	Delay	=	0.00000 sec
Delta T	=	32.0800 usec			
Start	=	0.00000 sec	Stop	=	32.0800 usec
Delta V	=	-20.00 mvolts			
Vmarker1	=	3.680 volts	Vmarker2	=	3.660 volts

Figure 10. Settling time.

3.5.4 Sensing Rate

The sensing rate was measured from the low to high transition of the A/D control line during two consecutive sense cycles. The result, Figure 11, showed a 196 microsecond time period per sense cycle. This included 40 microseconds of delay measured at the output of the NOR circuit.

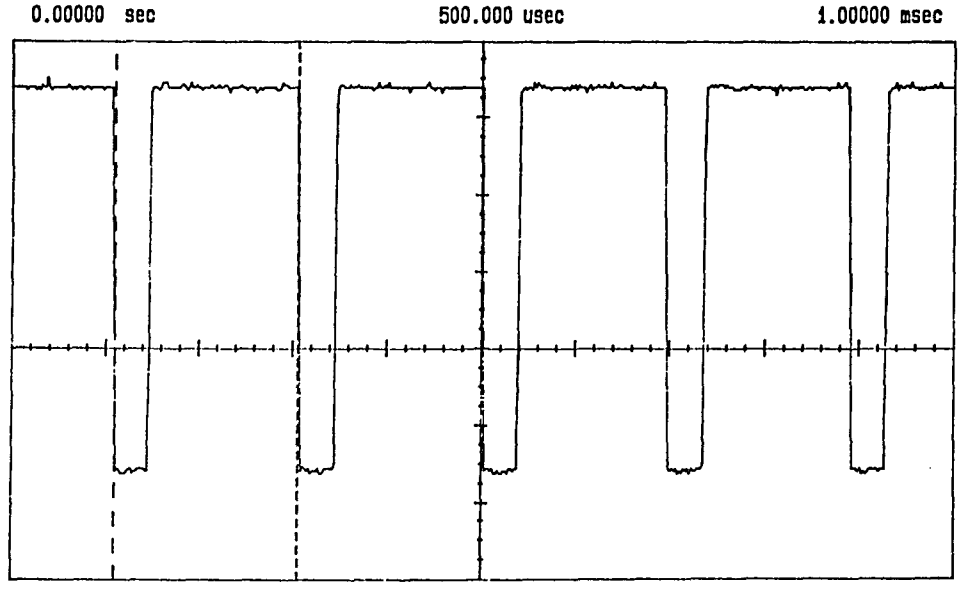


Figure 11. Sampling rate.

Chapter 4.

Examination of the Premise of Thermal Characterization

With continual increase of size and power of VLSI circuitry, the package becomes a limiting factor on the performance of the circuit. To insure optimum performance of the circuits, highly accurate measurements are needed to characterize the thermal performance of packages. To do this, normally, a temperature sensitive device inside the package is measured, but first the device behavior must be calibrated with varying temperature. The calibration is done by putting the device into a controlled thermal environment and measuring the temperature sensitive parameter of the device with respect to the environment temperature. This method assumes the device temperature is at the environment temperature when calibrated. If it is not, error will appear in the subsequent characterization of the package. This Chapter examines the different methodologies used to calibrate packaged devices and offers explanation of any discrepancies found.

4.1 Methodology

In this section the methods, type of instrumentation and test devices are discussed. The errors in measurements

usually can be attributed to not fully analyzing the methods, instrumentation and devices used. The method used as a basis is to apply a constant forward current to a pn junction and to measure the change in voltage across the junction due to a change in temperature. This pn junction voltage is hereafter referred to as the temperature sensitive parameter (TSP). The range of temperatures was limited to a 100 degree Celsius range since most measurements of this type are done in this range. Equipment used includes current sources, thermocouples, thermal measurement instrumentation, thermal environment controllers and test devices.

4.1.1 Current Sources and Temperature Sensitive Parameters

The current sources used in the following measurements are examined. Making a near-perfect current source is relatively difficult and can lead to oscillations due to the small load the current source sees [4]. Voltage sources on the other hand do not exhibit this problem. Therefore, a voltage source with a large resistor as seen in Figure 12 can closely represent a current source. Approximately a tenth of a milliamp was chosen as the current value since two manufacturers of thermal test devices specified this value and the third did not specify a value. SPICE2G [5] calculations, as shown in Figure 12, showed an error due to

using the resistor rather than a perfect current source to be ± .2 millivolts over a 100 degree range. This translates to a ± .1 °C error assuming a -2mV/°C change in the TSP. If the rate of change of the TSP is smaller than -2mV/°C (e.g., -1.9mV/°C) the resistor will produce even less error. All measurements done on test devices showed rates of change smaller than -2mV/°C but some were close enough

TEMP-ERATURE	VOLTAGE CURRENT SOURCE	RESISTOR
0	.6476	.6474
25	.5985	.5984
50	.5489	.5489
75	.4988	.4989
100	.4482	.4484

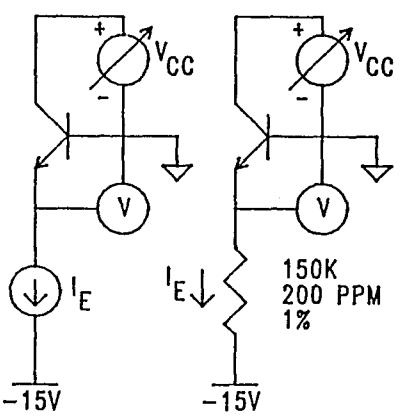


Figure 12. Ideal current source VS. resistive current source.

that this error must be accepted. It will be seen later that this is well within the uncertainty of associated equipment. The resistors used have low temperature coefficients (200 PPM) which, kept near ambient (5 °C swing), will not affect the results.

In these measurements the collector voltage on transistors will be varied. Therefore, the effect of this on the TSP is examined. The following equations can be

written [6]:

(1) $I_E = I_S/\alpha_F(\exp(V_{BE}/V_T)-1) - I_S(\exp(V_{BC}/V_T)-1)$

where I_S denotes the saturation current of the junction, α_F the forward current transfer between collector and emitter and V_T equal to kT/q, where k is the Boltzman constant, T the temperature in Kelvin and q the charge of an electron. For the devices measured, β_F was 100 or greater and therefore α_F is approximately one. Also, $\exp(V_{BE}/V_T)$ is much greater than one, reducing the first part of the equation to $I_S(\exp(V_{BE}/V_T))$. If V_{BC} equals zero, the second part of the equation reduces to zero and:

(2) $V_{BE} = V_T\ln(I_E/I_S)$

If V_{BC} is negative by more than 100 millivolts (normal forward active region of a transistor) then $\exp(V_{BC}/V_T)$ very nearly equals zero and:

(3) $V_{BE} = V_T\ln((I_E-I_S)/I_S)$

Since I_S is much less than I_E (around 10^{-10}), this can be reduced to equation (2). Finally, it is noted that the SPICE2G model does include temperature effects due to the saturation current I_S.

In this analysis it was assumed that I_S was a constant with respect to V_{BC} but I_S does vary with respect to V_{BC} due to the phenomena known as base width modulation. The effect of varying V_{BC} on I_S can be described using the measurable parameter V_A (Early voltage) such that:

(4) $$I_S^* = I_S(1-V_{BC}/V_A)$$

and (2) can be rewritten as:

(5) $$V_{BE} = V_T \ln(I_E/I_S^*)$$

This effect must be taken into account when comparing measurements taken at different levels of V_{BC}.

4.1.2 Thermometry

The references used in these measurements, the thermocouple, must not only be checked for their accuracy and precision but also for the linearity of the reference device (i.e., the ability to be precise and accurate over a range of temperatures). Through recent years the experimentalist has been inundated with thermocouple systems that have not only impressive characteristics but give us the temperature value digitized to a tenth of a degree. During initial measurements, it was seen that different thermocouple systems differed at certain temperatures but agreed at other temperatures. This led to a search for a temperature measurement system that was consistent. Simply, it was decided that a purely physical system was more reliable than digitized information. To choose a thermocouple system a set of equally qualified thermocouple systems was examined versus a precision thermometer. The results are shown in Table 2. These measurements must be held, as nearly as possible, to an

accuracy equivalent to the thermometer which was ±.25 °C. On the basis of these data, the second thermocouple was used for all experiments.

Thermocouples			Thermometer
1	2	3	
-0.4	0.7	0.7	0.5
15.7	17.4	17.1	17.0
40.2	40.6	40.5	40.5
60.2	61.3	61.5	61.0
80.3	81.6	82.3	81.0
100.2	101.2	102.3	100.5

Table 2. Comparison of thermocouples to thermometer.

4.1.3 Thermal Measurement Systems

Two different systems were used in conducting these measurements. The CCTCS designed for relative measurements, could not satisfy the need for absolute temperature measurements in this work. It did serve, however, to provide the requisite precisely controlled current sources. Hence, the CCTCS was coupled with a standard HP data acquisition ensemble consisting of a 3455A voltmeter and a 3495A scanner with a series 200 computer to constitute one

measurement system.

The second system employed, also computer controlled, was a Barnes Computherm Version 2.2 infrared imaging system. Measurement conditions with this equipment are restricted in that the test device must be unencapsulated in order to be visible. The principal distinction here is that temperature is measured by means other than interpretation of junction electrical parameters. It is important to note that some considerable subtlety attends exact calibration of the system. This concern is discussed in a later section of the paper.

4.1.4 Thermal Environment Control

Three types of thermal chambers and a temperature controlled heat sink were employed. The chambers were: a dielectric fluid bath system; a forced air oven; a convection oven. Each of these has advantages and limitations as a means for precise control of test device temperature.

The dielectric fluid bath system enjoys considerable popularity within industry for the type of measurements undertaken here. It permits complete immersion of the device within the fluid with very stable control of the device surface temperature over a wide range. In this work a range of 0 to 100 °C was used.

The forced air oven provides a flow of air, at a controlled constant temperature, over the surface of the test device. Temperature stability is comparable to that of the dielectric fluid bath. The range employed was 20 to 100 °C.

Thirdly, the convection oven, as ordinarily used, lacks adequate stability, tending to cycle around the desired set temperature. For this work, a stability augmentation scheme was devised as follows. The thermal capacity of the oven system was enhanced by placement of steel ingots within the chamber. The result was an enhanced thermal time constant for the system and a more moderate rate of cool-down from any given set temperature. With reduced cool-down rate, the oven could be stabilized at a temperature above the desired observation range and then de-energized, with measurements being made as the slowly varying temperature passed desired points. Slowdown notwithstanding, the procedure dictated that believable measured values taken at lower temperatures (a linear set) be used to extrapolate the relation to find inferred values at the upper temperature range. An example of the observed data, and the extrapolation thereof, is shown in Figure 13. The method restricted the observable temperature range to a maximum of 90 °C.

The temperature controlled heat sink referred to above

is used to control the temperature of the test device, through conduction from the package, in connection with direct infrared temperature measurements. The operation is represented in Figure 14. In this work, the temperature range available was restricted from 15 to 65 °C. Some caution is required, however, in interpreting the sink temperature as equivalent to, or even constantly displaced from, the internal device temperature. This arises from the fact that the natural convective heat transfer remains present and is itself a function of the package temperature.

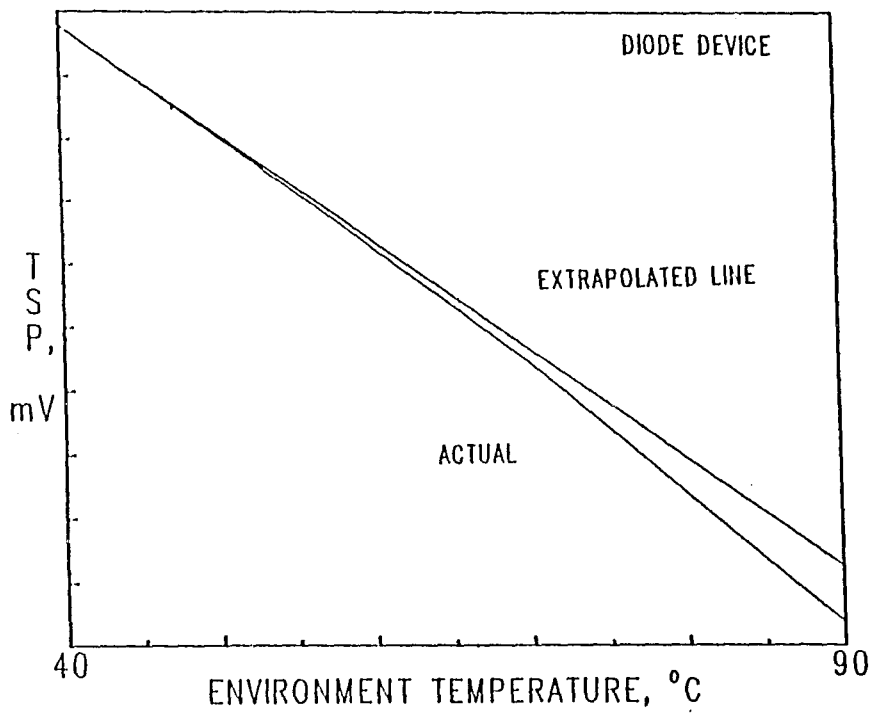


Figure 13. Convection oven extrapolated data.

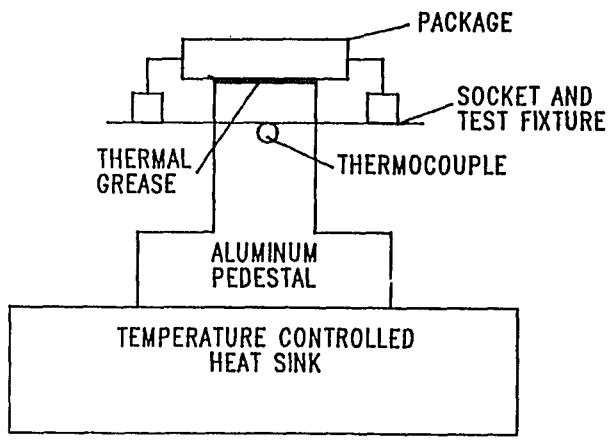


Figure 14. Temperature controlled heat sink

4.1.5 Test Devices

Three different thermal test chip devices were subjected to these measurements. Similarity was limited to the fact that all were packaged in forty-pin ceramic DIPs. The first consists of a Nichrome resistor for power dissipation with a diode available to provide a TSP and is referred to hereafter as the diode device. The second uses a transistor as the temperature sensitive device with base diffused resistors for power dissipation and is referred to hereafter as the transistor device. These two devices were made available to this laboratory by their manufacturers. The third device, identified as the TTC03, consists of a 4x4 matrix of double emitter transistors and was designed

and fabricated at this laboratory [2,3]. Of the three, only the TTC03 was available unencapsulated. To reiterate, all three devices were packaged, as mentioned above. The TTC03 was different in that the package cover was absent.

4.2 Experimental Results

4.2.1 TSP Behavior

For all test devices, the TSP was a pn junction voltage as described in equation (2). Over the temperature range explored, this measurable voltage exhibited a linear dependence upon temperature, with deviations from linear results no larger than experimental uncertainty. This is not a surprising result, given the commonly anticipated-2mV/°C rate of change predicted through differentiation of (2) at 300 K. Careful examination of the data, however, reveals that the actual rate is measurably different from the classical assumed value, by as much as +0.25mV/°C, or 12.5%, for some devices. This is explainable inasmuch as the classical expectation is predicated on the assumption of one-dimensional device geometry. It is highly relevant, however, to the application of commercially available test chips. One manufacturer, for example, explicitly recommends the use of a "one point, assumed slope" method of application. Clearly, use of an invalid slope/rate value

could produce error in the order of as much as 12.5%. These relationships are depicted in Figure 15.

4.2.2 Thermal Environment Control

Central to this subject is the notion that the actual temperature of a device, inside the package, at the junction itself, can be inferred reliably from the unequivocal knowledge of the TSP variable. The characterization of thermal test chip devices must therefore establish, between actual junction temperature and measured environmental temperature, either identity, or known predictable disagreement. With this view in mind, the

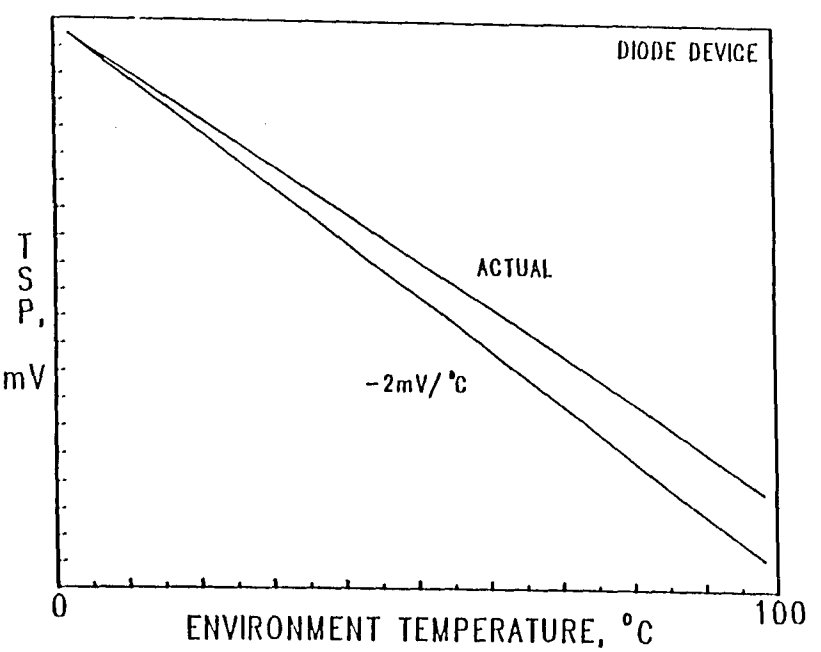


Figure 15. "One point, assumed slope" and actual.

measured data from identical devices in different thermal environment control systems was compared. If the form and magnitude of disagreements support some consistent explanation, the possible definition of usable correction factors exists.

The possibility of disagreement proceeds from the fact that the process of measurement dissipates power, i.e., albeit small, not zero. In turn, the presence of dissipation should activate heat transfer mechanisms, with attendant temperature differences between junction and environment. Among the several mechanisms, conduction- that which is best simulated by the dielectric fluid bath system - is expected to produce minimum disagreement. Hence, the dielectric fluid bath system was selected as the reference, the standard of comparison, in what follows.

For a particular device, the diode device, measured TSP versus environment temperature data is compared. Thus, as shown in Figure 16, data from the forced air oven is superimposed on the data from the dielectric fluid bath system. In this case, the straight lines are, in fact, truly superimposed at high temperatures and exhibit a small linearly increasing disagreement with diminished temperature. It is noted that this can be interpreted as a higher-than-environment junction temperature for low environment temperatures and reserve further comment for

later.

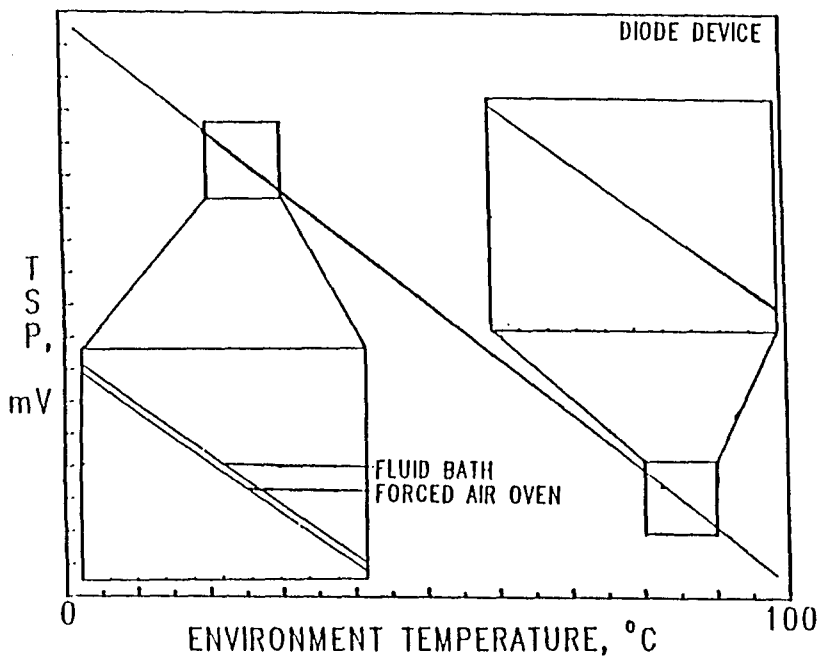


Figure 16. Forced air oven VS. dielectric fluid bath.

Figure 17 presents a corresponding comparison of data from the convection oven measurements. It is noted that, again, the convection oven data may be interpreted as a higher-than-environment junction temperature. Moreover, the disagreement is, in this instance, present throughout the temperature range and essentially independent of temperature.

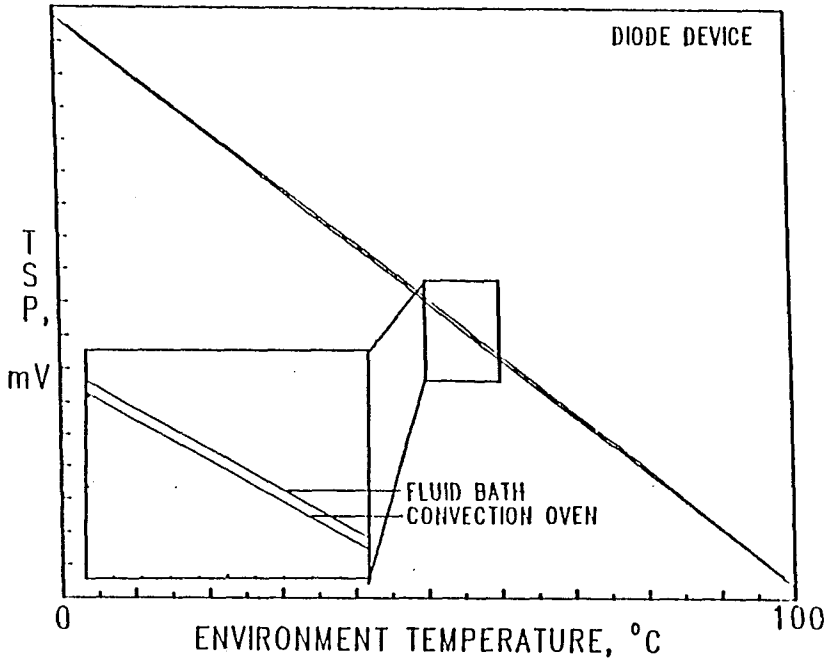


Figure 17. Convection oven VS. dielectric fluid bath.

Finally, the dielectric fluid bath system was compared to a temperature controlled heat sink. The disagreement between these two methodologies can be seen in Figure 18. To explain these results a simple thermal model is shown in Figure 19. Note that the thermal resistance due to natural convection is a function of the difference in ambient temperature and case temperature where the ambient temperature is a constant. Therefore when the case is at ambient temperature the convection resistance goes to infinity and the result is the same as the dielectric fluid

bath system. When the case temperature is lower than ambient the convection resistance becomes finite and the result is interpreted as a higher-than-environment junction temperature. Similarly, at temperatures above ambient, the convection resistance becomes finite and the interpretation is a lower-than-environment temperature. The convection resistance is not constant and therefore a straight line is not seen. If enough measurements were taken than a smooth curve would occur.

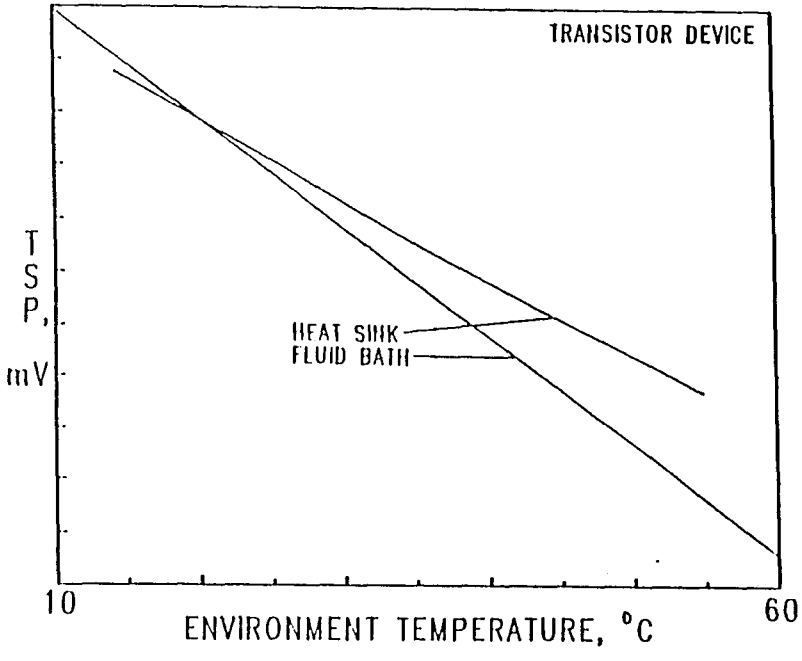


Figure 18. Temperature controlled heat sink VS. dielectric fluid bath.

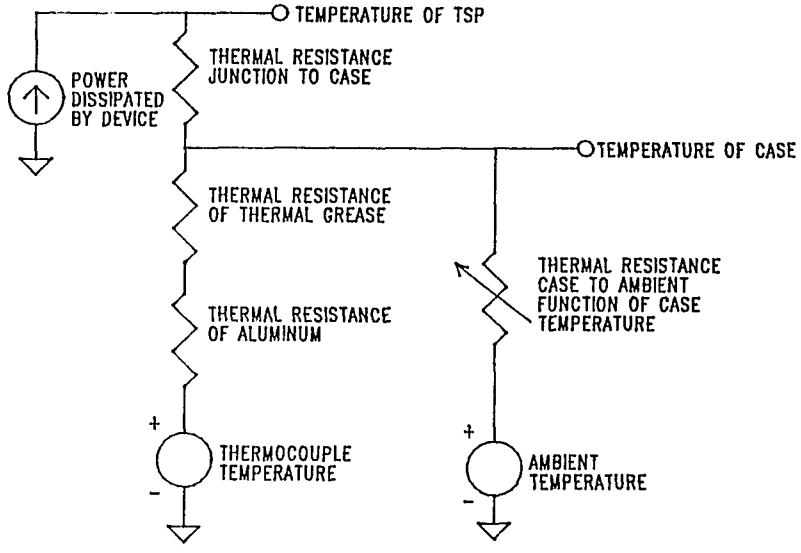


Figure 19. Thermal model of Temperature controlled heat sink.

4.2.3 Power Dissipation

As noted above, disagreement may exist between the temperature indicated by the TSP (actual device temperature) and the environment temperature. A second set of comparisons was done to examine the effects, upon these disagreements, of the level of power dissipated in the test device. These measurements were conducted in each of the three temperature environments, with similar results. They were done for the two devices whose dissipation could be controlled by variation of the transistor collector voltage

(V_{CC}). As noted in section 4.1.1, such a variation will not alter the TSP. Of these two devices, the TTC03 device was not encapsulated, while the transistor device was encapsulated. This difference is not insignificant.

Distinct from these comparisons, but providing insight as regards expected effects, direct (independent of TSP) device temperature measurements were made on the surface of the encapsulated TTC03, using the infrared system. For two power levels, 0.07 and 3.07 milliwatts, a difference display was used and the resultant averaged as shown in Figure 20. The result showed a 1.16 °C increase in the average chip surface temperature. Although a relative temperature measurement, this observation documents the expected elevation of device temperature with increased dissipation.

Figure 21 presents observed TSP values, for the unencapsulated TTC03 in the dielectric fluid bath, with the value of V_{CC} as a parameter, for V_{CC} set at 0, 15 and 30 volts, corresponding to 0.07, 1.57 and 3.07 milliwatts respectively. The nonlinear effect of dissipation is clear in that only for dissipation greater than 1.57 milliwatts is the disagreement between TSP and environment temperature discernible. Moreover, the magnitude of the disagreement is seen to be proportional to temperature.

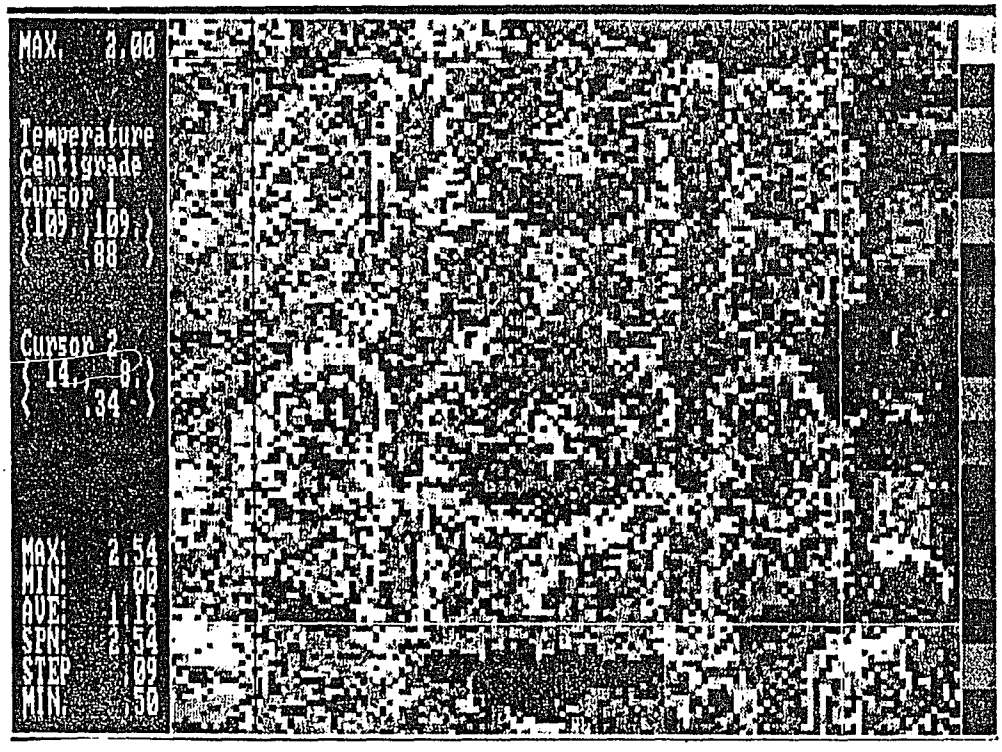


Figure 20. Infrared difference display.

The same experiment conditions were established for the TTC03 in the forced air environment, with the results presented in Figure 22. Here, the disagreement is seen to be more sensitive to dissipation and, differently, essentially independent of temperature.

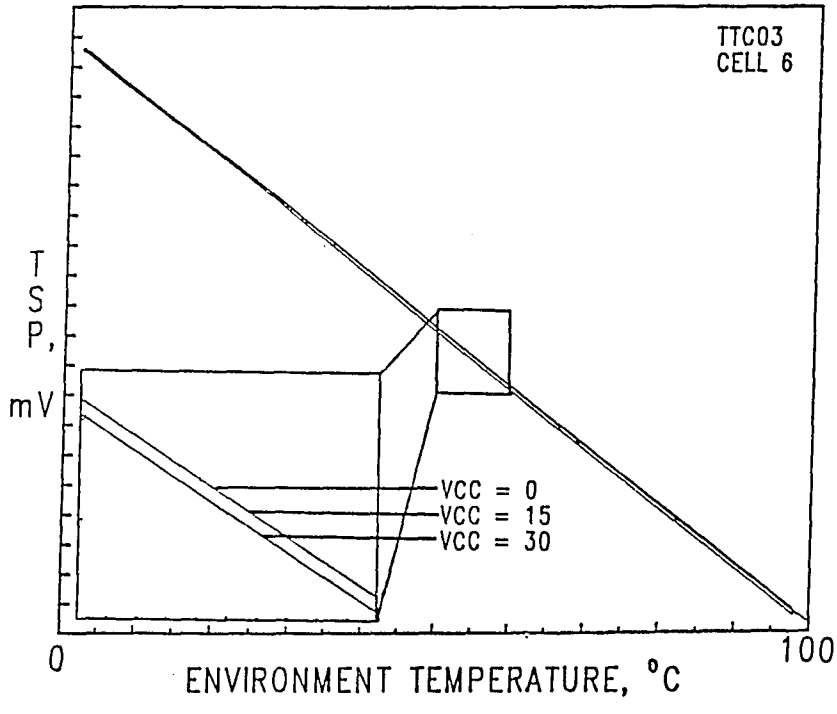


Figure 21. Dielectric fluid bath with V_{CC} as a parameter.

From these observations of the TTC03, it can be concluded that close agreement between device temperature, as measured by means of the TSP, and the environment temperature can be anticipated only for vanishingly small levels of dissipation in the test device. Further, the nature of a proposed correction factor will be a function of the type of thermal environment.

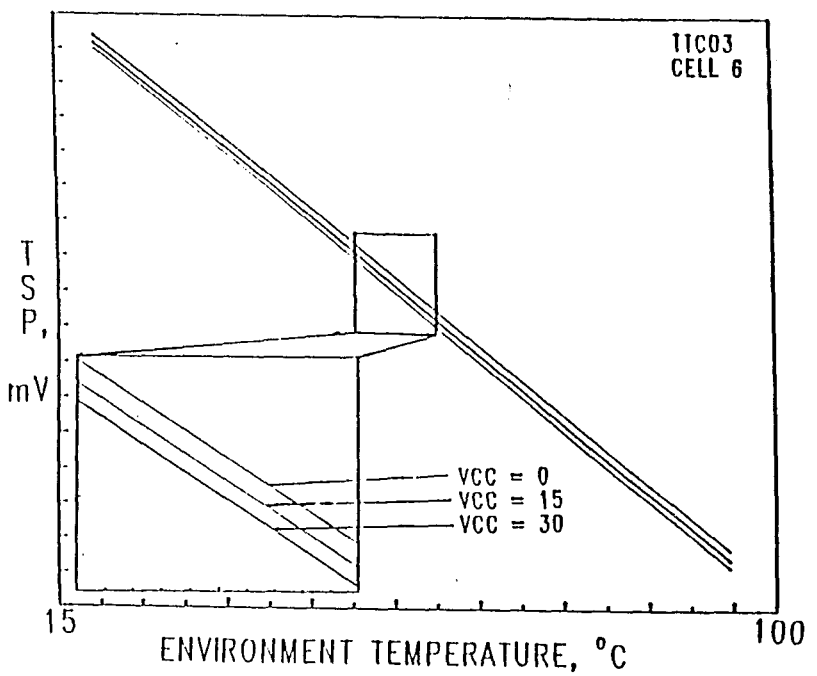


Figure 22. Forced air oven with V_{CC} as a parameter.

The transistor device, further different from the TTC03 in that it was encapsulated, was subjected to comparable experimental conditions in each of these two environments. The dissipation levels used were 0.07 and 1.07 milliwatts, corresponding to V_{CC} set at 0 and 10 volts respectively. The results for the fluid bath are shown in Figure 23 and those for the forced air environment in Figure 24. When these are compared with Figures 21 and 22, it is clear that the tendency of disagreement is comparable

in nature but much more sensitive to the level of dissipation.

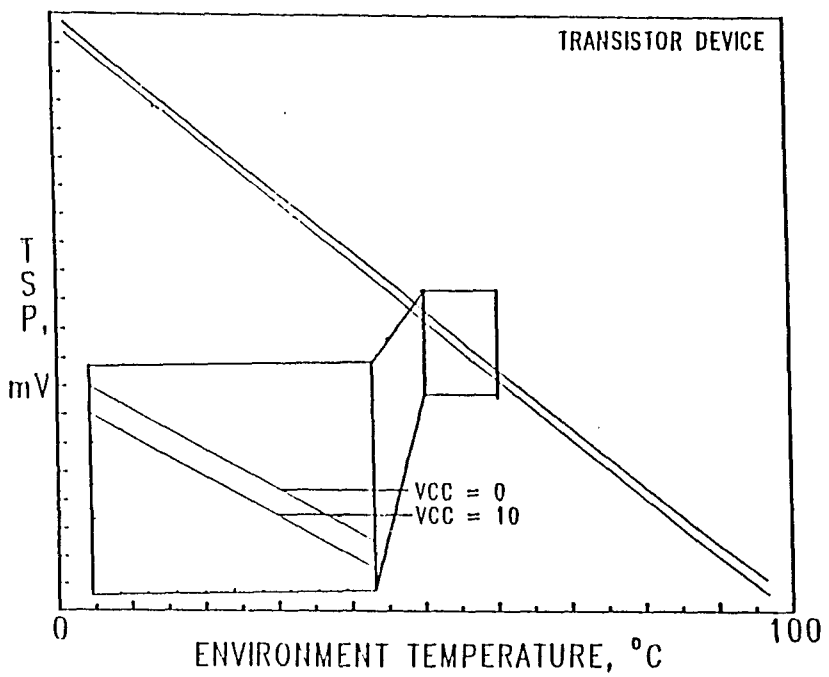


Figure 23. Dielectric fluid bath with V_{CC} as a parameter.

So far this examination of effects due to power dissipation has not included the effect on the TSP due to varying V_{BC} as described in equation (5). After measuring the Early voltage of the TSP devices and reexamining the results, it is found that the Early voltage accounted for part of the disagreement but not all of it. In fact, the

general tendency of the disagreement still holds after accounting for the Early voltage effect. In each instance, this effect produces less than half of the disagreement.

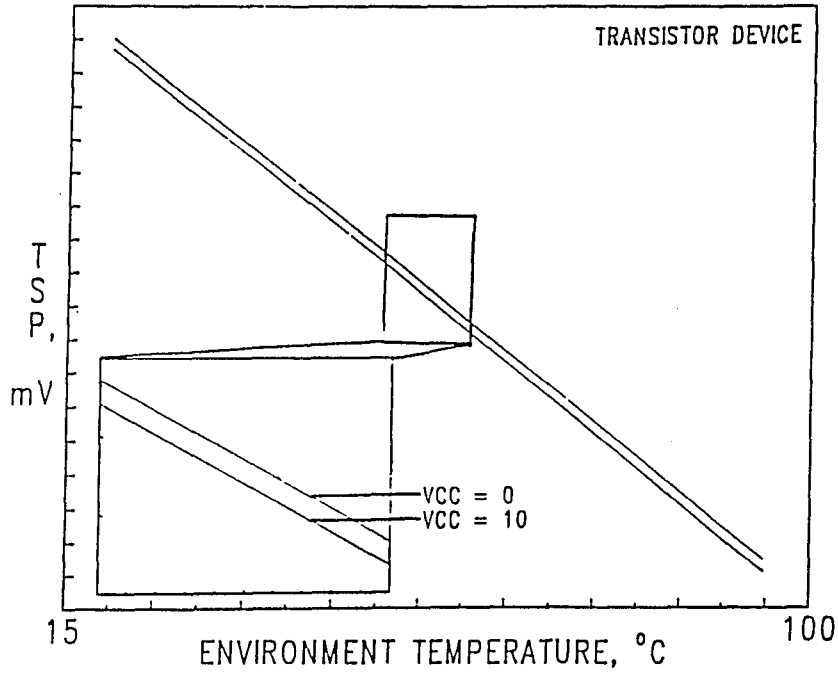


Figure 24. Forced air oven with V_{CC} as a parameter.

The effects described above may be interpreted as consequences of finite thermal resistance between the test device junction, in each case, and its environment. As shown, and in fact expected, the thermal resistance effect is largest for the encapsulated device.

The situation most sensitive to this effect of thermal resistance is that of the transistor device in forced air. For this case, the data represented by Figure 22 can be analyzed to estimate, for any fixed environment temperature, the dependence of the disagreement upon the dissipation. In turn, extrapolation reveals the residual minimum disagreement to be in the order of 0.1 °C, for this particular thermal resistance. This minimum corresponds, of course, to the requisite minimum dissipation of 0.07 milliwatts which makes the TSP available. It is noted that 0.1 °C is smaller than the experimental uncertainty in temperature. It is tempting to declare that the disagreement, provided dissipation is always held to a minimum value, may be always neglected. It must be borne in mind, however, that for some experimental package, the thermal resistance could be much larger with a correspondingly larger, and hence non-negligible, disagreement.

Chapter 5.

Conclusions

In this Chapter, ideas generated during the process of this thesis, to further research in this area, are discussed. These ideas include; a new test chip, new CCTCS circuitry and areas needing further research.

5.1 Test Chip

A new test chip would need to meet four requisites. First, the pin count should be minimized while the number of sensors and power dissipating devices is maximized. Second, the chip should be versatile to allow either uniform power dissipation or non-uniform power dissipation. Third, it should be easily fabricated. Fourth, the chip should allow access to a transistor such that the maximum power dissipation of the sensing device can be found as was done in Chapter 4.

A test chip that meets these requirements would be an NxN array of NPN transistors. This definitely meets the ease of fabrication requirement and would allow access to a transistor for measuring maximum sensor power dissipation. To minimize pin count the transistors used for sensing should be connected as diodes in a matrix format. Finally,

the chip would be versatile in that only the metallization need be changed for different configurations of non-uniform power dissipation, while a thin film resistor could be applied to the top of the chip for uniform power dissipation.

5.2 CCTCS Circuitry

To further redesign the CCTCS, certain design considerations need to be addressed. The first is the system configuration. That is whether to continue to use the parallel port for connection to the CCTCS or to directly access the computer's data and address busses. Secondly, the finished product should be analyzed for ease of connection between the computer and the DUT and the CCTCS. Also the internal connections of the CCTCS should be considered. This refers to the use of standard connectors and wiring between parts of the CCTCS and to the computer and DUT. Direct soldering of wires should be eliminated. Finally, the CCTCS needs to be versatile such that different types of devices such as resistors (diffused and thin film) and FETs can be used for power dissipation and sensing.

5.2.1 I-C Board Redesign

If the CCTCS were to stay in the present format (using

the computer parallel port), a design is shown in Figure 25 that increases the ability of the CCTCS. This design allows for higher resolution, the use of up to 64 sensors, and eliminates the use of CMOS type analog switches. The use of quality miniature relays eliminates the voltage limitations of the CMOS type switch. Finally the gain and offset are put on the H-S board such that different devices can be used on different boards.

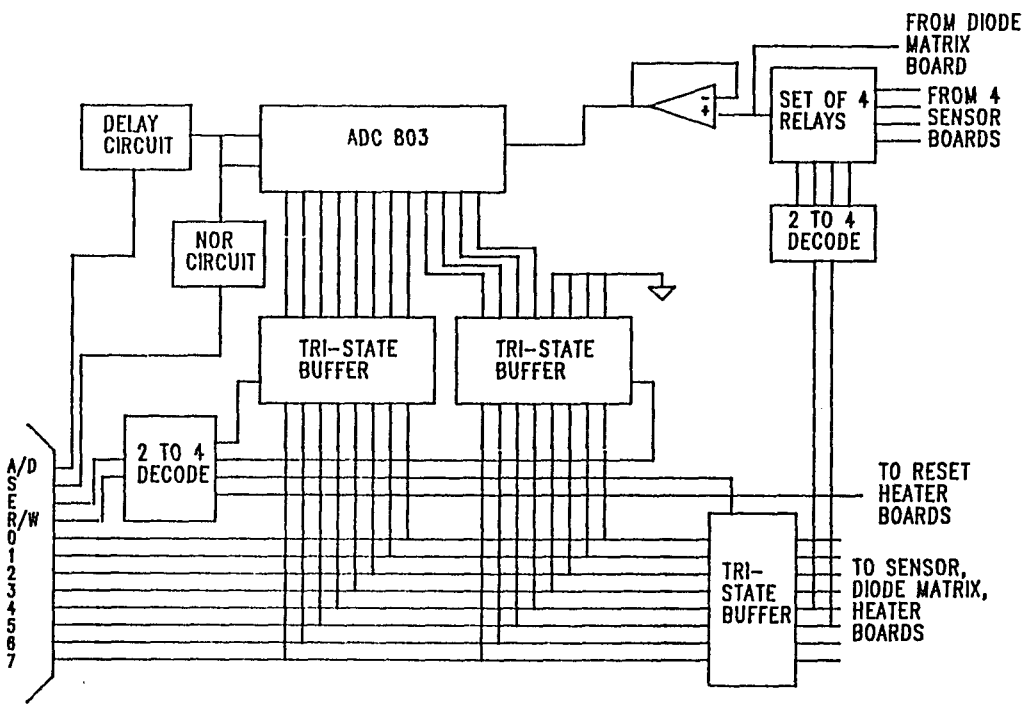


Figure 25. I-C board design.

5.2.2 H-S Board Redesign

As mentioned before, if the CCTCS format remains the same a design for the H-S board is shown in Figure 26. It should be noted that the sensors and heaters most likely should be constructed on two separate boards rather than on one single board. This design reduces the instruction set, uses relays rather than CMOS analog switches, and current sinks rather than pull down resistors. The use of current sinks, rather than pull down resistors, allows the CCTCS to be used with more types of devices. The sinks could be easily converted to sources for use with PNP or PMOS technology. The current sinks and sources, used to bias TSP devices, need to be designed to have variable values since in Chapter 4 it was noted that in different packages need different current levels to limit power dissipation of the sensing device. Figure 27 shows a design for a switchable current source. This design is TTL compatible, variable value, eliminates large currents from being switched on the power supply lines and uses standard analog voltages eliminating the need for the D- power supply. In Figure 28 a design to handle diode matrices is shown.

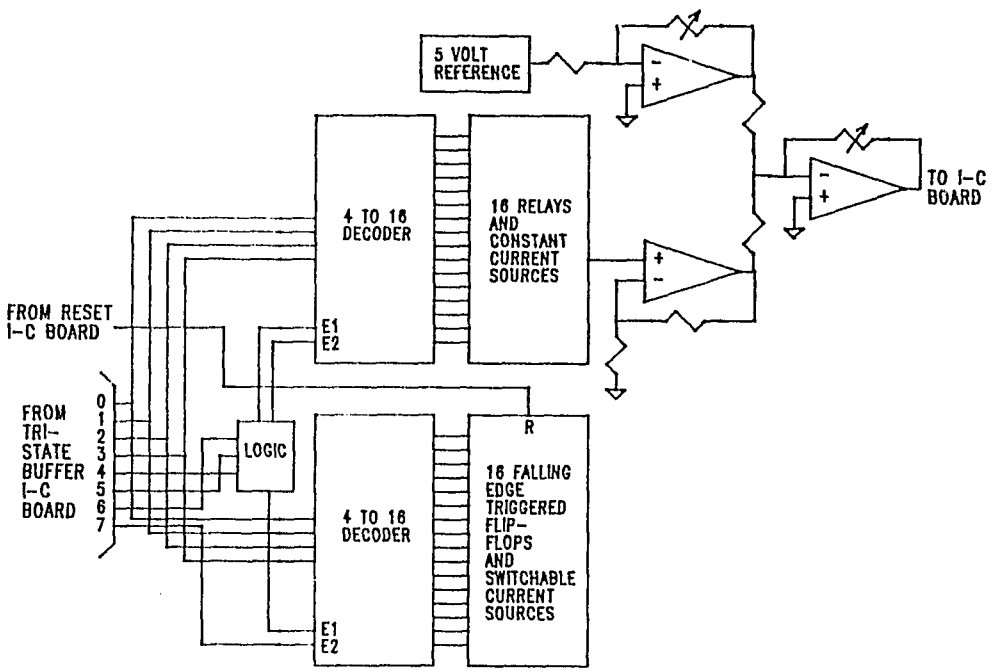


Figure 26. H-S board design.

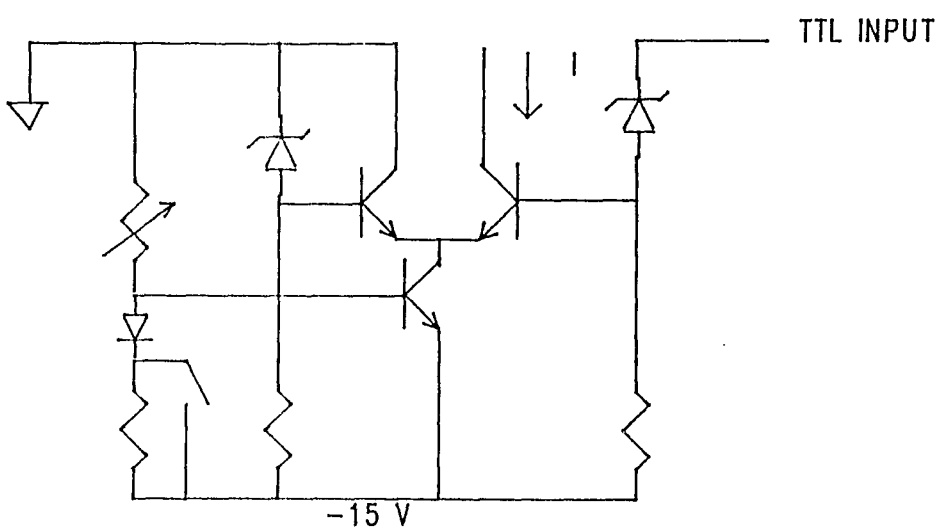


Figure 27. Switchable current source.

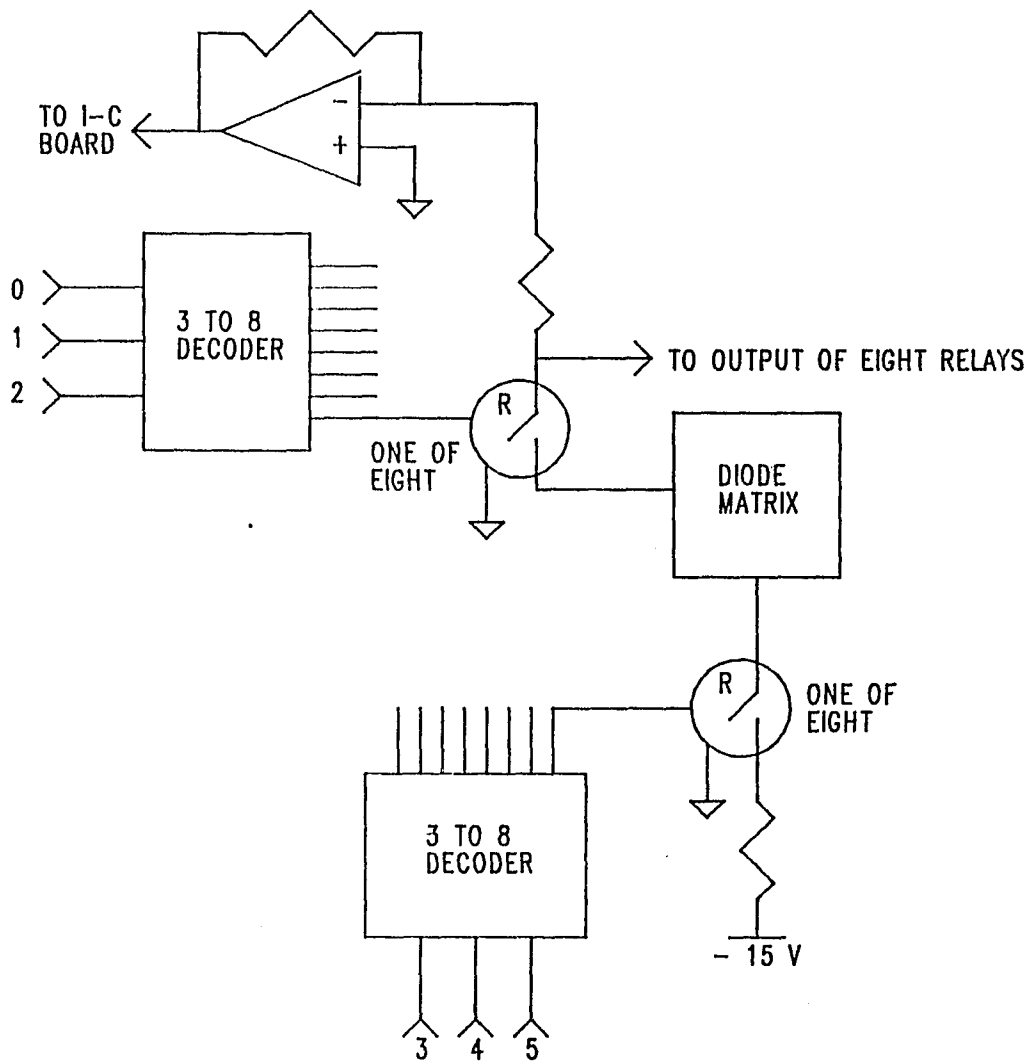


Figure 28. Diode matrix sensor circuitry.

5.3 Areas for Continuing Research

From this work, two areas needing further investigation are presented. The first is the investigation of the

current source oscillations. Many types of current sources have been designed but an investigation into which type will eliminate oscillation problems while being used with the CCTCS has not been done. Secondly, in Chapter 4 the determination of maximum sensor power dissipation was shown, but in the non-uniform case the spacing of the sensor to power dissipation device is not discussed. The establishment of close proximity spacing such that the sensor is at the temperature of the power dissipation device has not been done. This investigation is needed if further work in non-uniform power dissipation is continued.

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