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UMI

COUPLED NOISE STUDY OF THICK FILM CIRCUITS

by

JAMES EDWIN QUILICI

A Thesis Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

In Partial Fulfillment of the Requirements
For the Degree of

MASTER OF SCIENCE
WITH A MAJOR IN ELECTRICAL ENGINEERING

In the Graduate College

THE UNIVERSITY OF ARIZONA

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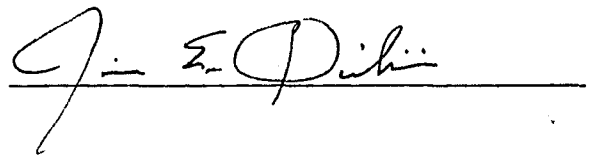
SIGNED: 

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ABSTRACT

Methods of noise coupling in high speed thick film circuits has been investigated. Parasitic coupling parameters have been experimentally determined for a variety of single and multilayer thick film layouts. In addition, the severity of the problem has been studied by measuring coupled noise induced on carefully constructed test cards. Curves are presented as an aid for predicting noise levels as a function of conductor spacing and signal edge speed. The measurements are discussed quantitatively and guidelines for the design of high speed thick film circuits are summarized.

CHAPTER 1

INTRODUCTION

Single and multilayer thick film networks are used predominantly in hybrid microcircuit design due to their relative ease of manufacturing and the high circuit densities that can be achieved. Higher interconnect densities and shorter interconnect lengths generally allow a circuit to operate at higher signal speeds. However, with increasing signal speed and circuit density, the possibility of a coupled noise problem increases. Moreover, the widespread usage of CAD autorouting for hybrid layout increases the likelihood of a noise problem because current CAD software does not consider signal coupling when determining the routing of signal interconnects. Often sensitive signal lines are excessively long or are placed too close to one another. It is left to the designer to determine the problem areas and modify the circuit layout for minimal noise.

Coupled noise, commonly referred to as crosstalk, is caused by the electromagnetic interactions between signal lines in close proximity. This coupling causes extraneous noise in analog circuits and may even cause false logic errors in digital circuits. Unfortunately, these problems typically do not surface until after the new

design has been manufactured and tested. At this point, a costly redesign is often required.

Although one may find an abundance of literature concerning high speed signal transmission and coupled noise in copper - fiberglass printed circuit boards, such studies for thick film hybrids are rare. This is particularly surprising in that the signal transmission properties of thick film structures are expected to be significantly different than those encountered with printed circuit boards. One of the major reasons is that the thick film process produces much shorter line lengths, narrower widths, tighter spacings and thinner dielectric layers than the printed circuit board approach. For instance, 15 mil line widths and spacings are generally the lower limit of the copper board process, while 5 mil widths and spacings are achievable with thick films. More importantly, multilayer printed circuit boards may have 5 to 10 mils of epoxy prepreg material between circuit layers, while the dielectric layers in a thick film multilayer circuit will range between 0.5 and 2 mils. In addition, thick film conductors and insulators are nonhomogeneous materials and respectively exhibit higher sheet resistance and dielectric constants than are available with the fiberglass printed circuit board materials.

The best way to avoid a coupled noise problem is through careful routing of the signal interconnect lines.

Yet, most hybrid designers are still unaware of the extent of the crosstalk problem. Hence, the intent of this study is to determine the severity of coupled noise in both single and multilayer thick film circuits through measurements of material properties and induced noise levels in various thick film structures. In chapter 2, methods of noise coupling are analyzed, followed by a discussion of the digital device characteristics that are most significant to the coupled noise problem. Next, in chapter 3, material properties and layout geometries are discussed with regard to noise coupling. The experimental procedures and noise measurements are presented in chapter 4. Finally, chapter 5 concludes with a discussion of the results and a brief set of design guidelines. Hopefully, this work will provide a means of predicting and thereby avoiding crosstalk problems during the early stages of design.

CHAPTER 2

THE COUPLED NOISE PROBLEM

2.1 Capacitive and Inductive Coupling

Coupled signal noise is an undesirable consequence of many different variables. It is both a function of the interconnect medium and the electrical circuit. For example, noise coupled through the parasitic capacitance between two signal lines is dependent on the line separation and the dielectric properties of the substrate material on which the circuit is built. In addition, the magnitude of the coupled noise is directly dependent on the switching speed and signal levels of the circuit components.

Coupled noise is the result of interacting electromagnetic fields between two signal lines. Generally, it is parasitic capacitance and inductance in the hybrid substrate which provide the coupling path, whereby fluctuations in the electromagnetic field of one line induces noise currents and voltages on a nearby line. The electromagnetic field interaction between two signal lines over a ground plane is depicted in figure 2.1.[1] The conductors are shown in a static state, yet biased to either a positive or negative polarity. When both conductors are the same polarity, the condition is referred to as the even

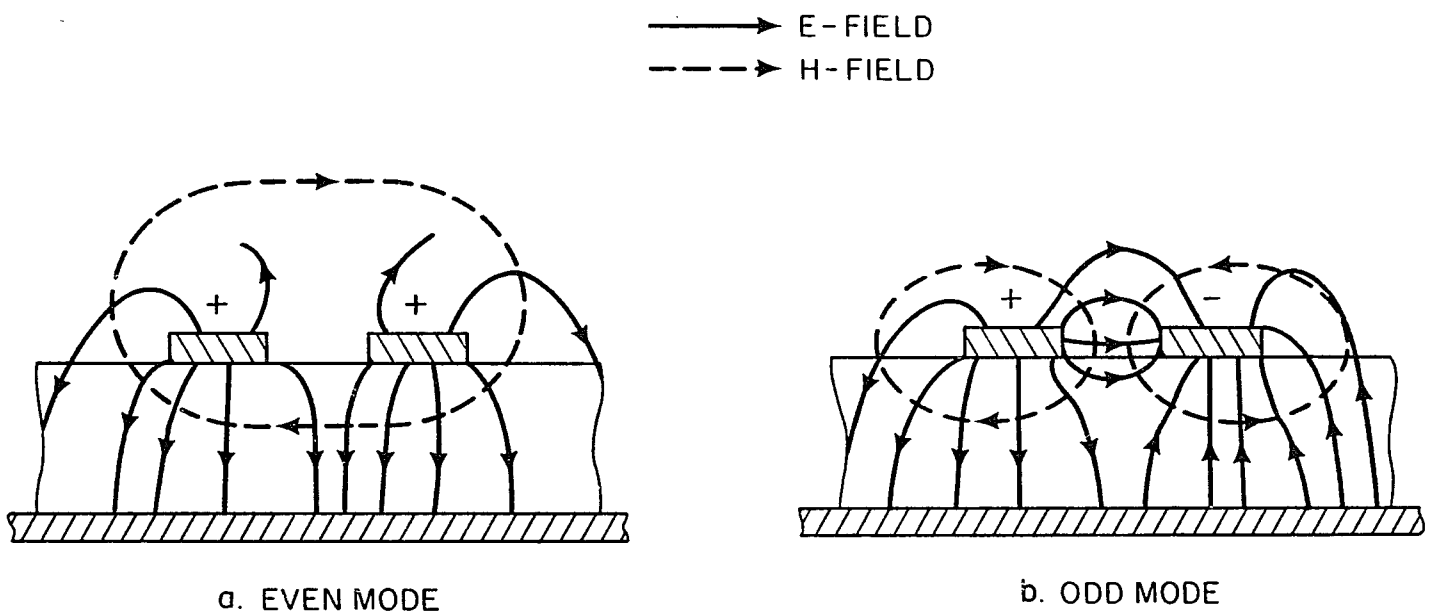


Figure 2.1 Electromagnetic Field Interactions in Parallel Coupled Microstrip Lines

mode. Currents are flowing in the same direction and the magnetic fields of both lines interact while the electric fields repel. Conversely, when the polarity of the two lines is opposite, the condition is referred to as the odd mode. The electric fields are interacting while the currents are flowing in the opposite direction and the magnetic fields cancel. Of course, crosstalk is a switching phenomena, so the field interaction will change modes as the signal levels change. Because crosstalk is a result of field interactions, the signal coupling decreases as: 1) the distance between the signal lines increases; or 2) the conductors are placed closer to a shielding ground plane (due to the decreased fringing of the electric field).

The degree of signal coupling also depends on the relative voltage and current levels present on the interacting lines. To model crosstalk in a circuit, a simple two-line system is used as shown in figure 2.2.[2] The mutual inductance, L_m, expressed in Henries, is defined as:

$$L_m = V_2 \Big/ \frac{dI_s}{dt} \Bigg|_{\frac{dI_2}{dt} = 0} \tag{2.1}$$

where V_2 is the voltage developed in the quiescent line and dI_s/dt is the time varying current in the active line.

In contrast, the coupled capacitance, C_c, expressed in Farads, is defined as:

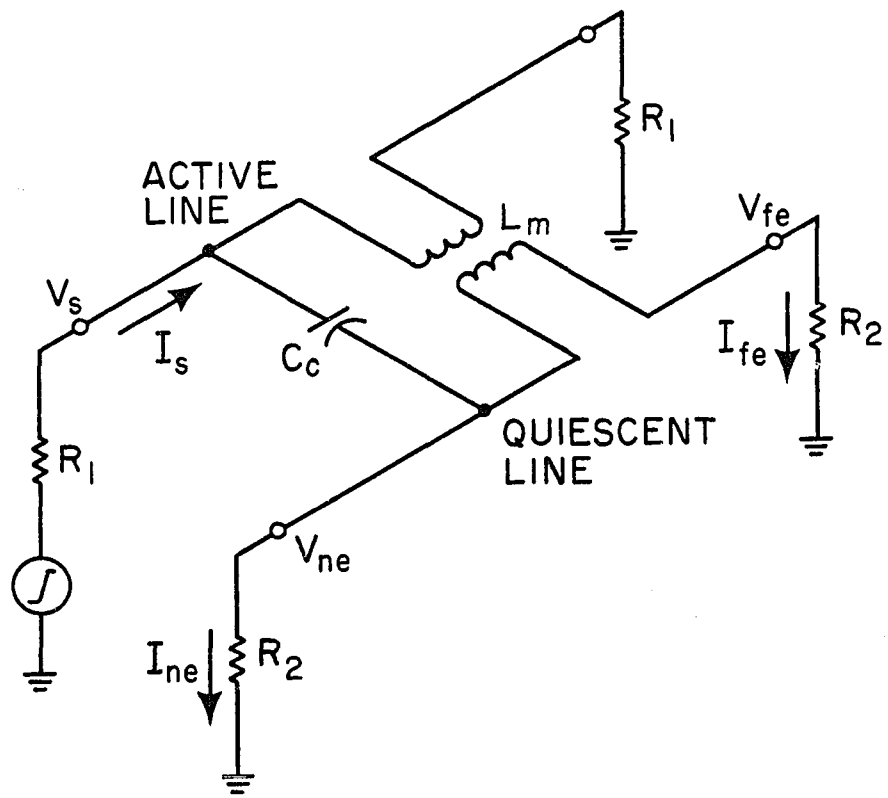


Figure 2.2 Coupled Circuit Model

$$C_c = I_2 \Big/ \frac{dV_s}{dt} \Bigg|_{\frac{dV_2}{dt} = 0} \tag{2.2}$$

where I_2 is the current developed in the quiescent line and dV_s/dt is the time varying voltage in the active line. The time dependence for both coupling parameters accounts for the increased crosstalk with faster switching times.

In figure 2.2, resistors R_1 and R_2 represent terminations for the active and quiet lines. Coupled voltages are typically discussed in terms of near end and far end crosstalk. Near end crosstalk, V_{ne}, is the induced voltage at the sending end of the quiet line, while far end crosstalk, V_{fe}, is the voltage developed at the receiving end. With properly terminated transmission lines, near end crosstalk is usually worse than far end. However, when lines are terminated by high impedances, the near and far end crosstalk differ slightly. To solve for the near and far end noise voltages, L_m and C_c are considered separately.[2] First ignoring C_c, the current developed on the quiet line is given by

$$V_{ne} - V_{fe} = L_m \left(\frac{dI_s}{dt}\right) \tag{2.3}$$

Since $V_s = I_s R_1$,

$$V_{ne} - V_{fe} = \left(\frac{L_m}{R_1}\right)\left(\frac{dV_s}{dt}\right) \tag{2.4}$$

Now ignoring L_m,

$$I_{ne} + I_{fe} = C_c \left(\frac{dV_s}{dt}\right) \tag{2.5}$$

This current is changed to voltage to yield

$$V_{ne} + V_{fe} = R_2 I_{ne} + R_2 I_{fe} = R_2 C_c \left(\frac{dV_s}{dt}\right) \tag{2.6}$$

To find V_{ne}, equations 2.4 and 2.6 are added, while to find V_{fe}, they are subtracted.

$$V_{ne} = \left(\frac{C_c R_2}{2}\right)\left(\frac{dV_s}{dt}\right) + \left(\frac{L_m}{2 R_1}\right)\left(\frac{dV_s}{dt}\right) \tag{2.7}$$

$$V_{fe} = \left(\frac{C_c R_2}{2}\right)\left(\frac{dV_s}{dt}\right) - \left(\frac{L_m}{2 R_1}\right)\left(\frac{dV_s}{dt}\right) \tag{2.8}$$

In both equations, the effect of the line terminations is evident. For low impedance circuits, the capacitive and inductive effects will tend to cancel each other at the far end, and the near and far end voltages will be significantly different. In high impedance circuits, the inductive effects become negligible and the near and far end voltages are almost identical. Generally, 377 ohms of line and termination impedance is considered the boundary between a high and low impedance line.[3]

2.2 Conductive Coupling

Another form of noise coupling is through conduction. Whenever two or more circuits share a common node, there is always a possibility of noise coupling through a common impedance. For instance, figure 2.3 shows the

condition where two circuits share a common ground. In this situation, the ground reference of circuit 1 is actually modulated by ground current flowing from circuit 2 through the common ground impedance. To put this problem into perspective, consider an example of a TTL gate switching from a logic 1 state to a logic 0 state. In a 4 ns period, it may sink 20 mA through its output stage to ground. In a hybrid circuit, it is not unreasonable to estimate 20 nH of inductance in the ground line when the wire bonds, bond pads, interconnects and header pins are taken into account. The noise generated on the ground line has a peak amplitude of

$$V = \frac{L\ dI}{dt} = \frac{(20\ nH)\ (20\ mA)}{4\ ns} = .100\ V \qquad (2.9)$$

Although below the guaranteed TTL noise margin, a false logic error could occur if many gates were to switch simultaneously.

2.3 Conductive and Capacitive Coupling

Finally, another means in which noise may be transmitted through a hybrid is by a combination of conductive and capacitive coupling. For example, figure 2.4 shows a cross section of a multilayer substrate where two adjacent signal lines are printed over another conductor pad, separated by a dielectric layer. At high frequencies, parasitic capacitors, C_{c_1} and C_{c_2}, provide a low impedance

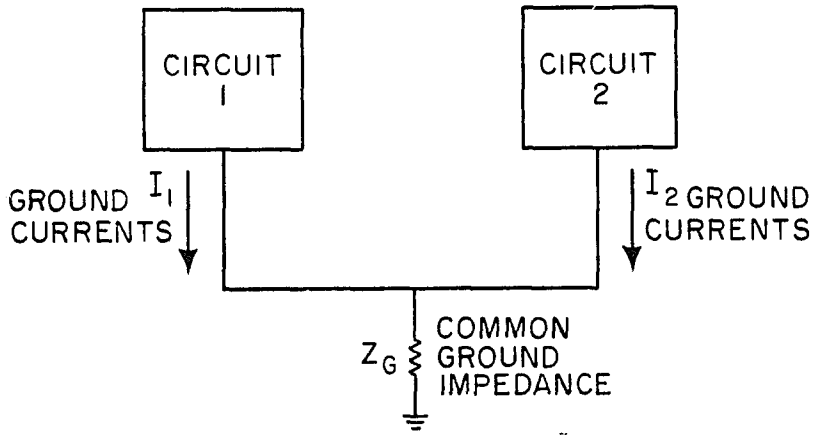


Figure 2.3 Example of Conductive Noise Coupling

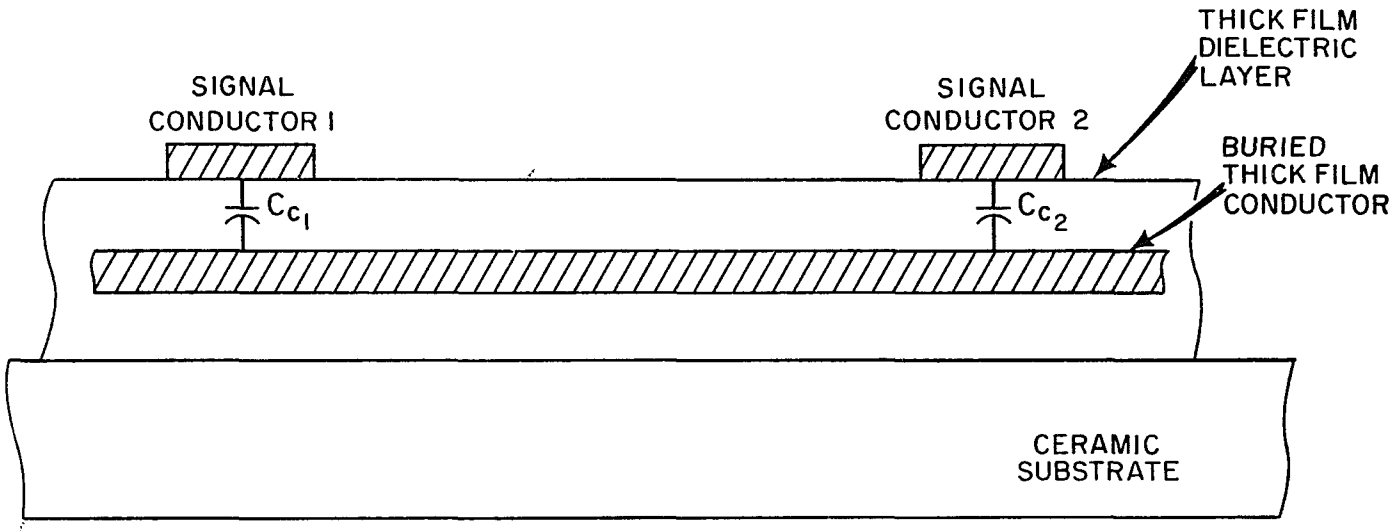


Figure 2.4 Example of Conductive and Capacitive Noise Coupling in a Multilayer Hybrid Circuit

path between the top lines and the buried conductor layer. Although the two top layer signal lines may be physically far apart, noise voltages from line 1 may be capacitively coupled to the lower layer, conductively transmitted to the region below line 2, and then coupled back up to the top layer. Coupling of this form is difficult to analyze since the source of the noise voltages is not easily determined.

2.4 Component Characteristics

When working on a hybrid layout, the designer must first be aware of some basic component characteristics before deciding what precautions need to be taken in routing signal lines. The device characteristics most significant to the coupled noise problems are signal rise and fall times, signal voltage swing, signal drive currents, input and output impedances, and device noise margins. Although coupled noise may be a problem in both analog and digital circuits, this study is primarily focused on the latter because of the fast switching speeds of current digital logic. The electrical characteristics of popular digital logic families are listed in table 2.1.[4,5,6,7]

The relationship between switching speed and coupled noise is apparent in equations 2.7 and 2.8. As the signal rise and fall times decrease, coupled noise increases. However, the fastest device does not always generate the most noise. The signal slew rate, the ratio

TABLE 2.1 Characteristics of Digital Logic Families

DEVICE	V_{oH} volts	V_{oL} volts	V_{iH} volts	V_{iL} volts	I_{oH} milli-amps	I_{oL} milli-amps	I_{iH} milli-amps	I_{iL} milli-amps
	Min	Max	Min	Max	Typ	Typ	Max	Max
TTL STANDARD	2.40	0.40	2.00	0.80	20.0	16.0	0.04	1.60
TTL FAST SCHOTTKY	2.50	0.50	2.00	0.80	50.0	40.0	0.05	0.60
CMOS FAST (Vdd=4.5V)	4.40	0.10	3.20	0.90	35.0	35.0	0.00	0.00
ECL 10K	-0.96	-1.65	-1.10	-1.47	50.0	50.0	0.14	0.00
ECL 100K	-0.96	-1.62	-1.10	-1.47	40.0	40.0	0.26	0.00

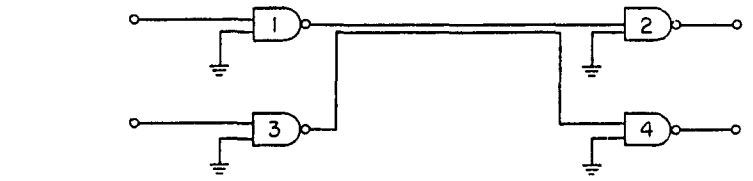
	SLEW RATE V/μs Typ	t_r ns Typ	t_f ns Typ	Z_{oH} ohms Typ	Z_{oL} ohms Typ	Z_{iH} ohms Min	Z_{iL} ohms Min	NOISE MARGIN volts Min
TTL STANDARD	310	6.4	3.4	65	15	50K	150	0.400
TTL FAST SCHOTTKY	1000	2.0	2.0	15	5	100K	300	0.500
CMOS FAST (Vdd=4.5V)	715	6.0	6.0	4	4	1M	1M	0.800
ECL 10K	444	1.8	1.8	7	*	40K	40K	0.125
ECL 100K	1000	0.8	0.8	5	*	40K	40K	0.115

*Output Impedance Dependant on Termination Resistors

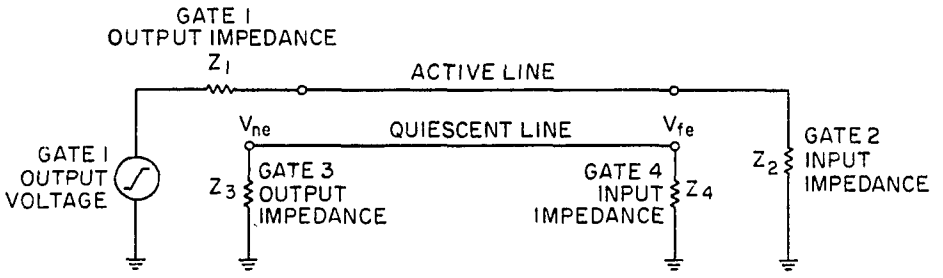
increases. However, the fastest device does not always generate the most noise. The signal slew rate, the ratio between the voltage swing and the rise or fall time, may be a more important factor. For example, properly terminated ECL 10K devices feature 1.8 ns edge speeds with signal swings slightly greater than 800 mV. The slew rate of the switching ECL signal is about 444 V/us. In comparison, the Fast Schottky TTL devices have a 2.0 V swing between logic states with edge speeds as low as 2 ns. The slew rate of the Fast Schottky device is 1000 V/us and greater than its ECL counterpart. Thus, the Fast Schottky device would generate more noise.

For fast switching speeds, the digital device must be capable of quickly charging or discharging any load capacitance created by other devices on the signal line. The output stage must provide a low impedance path to source or sink a substantial amount of current. At the device input, the impedance is purposely kept much larger than the characteristic impedance of the interconnect lines to prevent signal attenuation.

Modelling coupled noise in digital circuits is difficult due to the different impedances at either end of the signal lines. Figure 2.5 shows a schematic representation of two adjacent lines terminated by logic gates. The active line is terminated on one end by the output impedance of gate 1 and the input impedance of gate 2 at the



a. DIGITAL CIRCUIT



b. SIGNAL LINE MODEL

$$V_{ne} - V_{fe} = \frac{L_m}{Z_1}\left(\frac{dV_s}{dt}\right)$$

$$V_{ne} + V_{fe} = \frac{C_c Z_3 Z_4}{(Z_3 + Z_4)}\left(\frac{dV_s}{dt}\right)$$

$$V_{ne} = \left(\frac{C_c Z_3 Z_4}{2(Z_3 + Z_4)} + \frac{L_m}{2 Z_1}\right)\left(\frac{dV_s}{dt}\right)$$

$$V_{fe} = \left(\frac{C_c Z_3 Z_4}{2(Z_3 + Z_4)} - \frac{L_m}{2 Z_1}\right)\left(\frac{dV_s}{dt}\right)$$

Figure 2.5 Coupled Noise Between Digital Signal Lines
a) Digital Circuit; b) Signal Line Model

impedance of gate 4 at the opposite end. Capacitive coupling on the quiescent line is proportional to the parallel combination of input and output impedances. Thus, a low output impedance is also beneficial in minimizing capacitive coupling. Conversely, the current sourcing capabilities of a logic device are a function of their output impedance. Inductive coupling is predominant in devices with low output impedance and large current drive capabilities.

Probably the best measure of a logic device's vulnerability to crosstalk noise is the DC noise margin, although it is a static parameter applied to a dynamic or switching application. TTL logic guarantees a 400 mV difference between a logic output level of a driving device and the input voltage requirements of a receiving device. Thus, noise pulses on a quiescent line would need to exceed this level to cause a false switching error. Referring back to table 2.1, one sees that the ECL 100K devices have the lowest noise margin with only .115 mV of extraneous noise allowed on the signal line. With their fast switching speeds and low noise margins, the ECL devices provide the greatest challenge to the designer. However, since each of the logic families feature rise and fall times below 10 ns, crosstalk noise should always be a major concern during the circuit layout.

CHAPTER 3

ELECTRICAL PROPERTIES OF THICK FILM CIRCUITS

3.1 Thick Film Materials

Manufacturers have developed a wide variety of thick film conductor and dielectric pastes for use in a broad range of electrical applications and industrial processes. Of course, each paste is slightly different and the designer should consult manufacturer data sheets for specific details. Nevertheless, there are some general characteristics worthy of discussion in this study.

In paste form, both conductors and dielectrics have three main constituents: a binder, a vehicle, and a functional element. The functional element gives the material either conductive or dielectric properties. Metal particles are used as the functional element in conductor pastes, while ceramic particles are used to provide electrical isolation in dielectric pastes. The relative proportions of the other constituents give the paste its mechanical properties with some secondary electrical attributes. Generally, these pastes are screened onto a ceramic substrate and then oven fired at high temperatures. Once fired, the functional elements are held in place by the binder material.

The metal particles contribute 50% to 70% of the weight of a conductor paste. Particle size, shape, and distribution influence the final electrical and mechanical performance of the thick film conductor. The paste with the smallest and smoothest particles gives the best print resolution and most uniform conductivity. As expected, thick film conductors exhibit higher resistivities than the copper layer on printed circuit boards. The sheet resistivity of a thick film may range from 1.5 mΩ/□ to 150 mΩ/□. In comparison, a copper layer on a printed circuit board typically has a sheet resistivity of about 6μΩ/□.

For isolation and passivation layers, the relative dielectric constant of the film is controlled by the ceramic particles used in its composition. Ceramics with low dielectric constants are used to minimize line capacitance and capacitive coupling. Dielectric constants for the thick film pastes range from 6 to 10. These values are nearly the same as the relative dielectric constant of the substrates upon which the circuits are screened. For an alumina substrate, the relative dielectric constant is between 9.3 and 9.9, while for beryllia substrates it is 6.9. This is significantly higher than the dielectric constant of polymer-based printed circuit boards, which range from 2 to 5.

The binder material used in thick film pastes consists of low melting point glasses which suspend the

functional particles and bonds the film to the substrate. The binder comprises 10% to 20% of the weight of the paste. During firing, the viscosity of the glass binder decreases with increasing temperature. It is important for both conductive and dielectric pastes that the glass thoroughly wet the functional particles during firing. Without sufficient wetting, voids result and the conductivity or insulation properties of the thick film are nonuniform. At the same time, the binder must hold the particles together to maintain the circuit dimensions. Moreover, the binder must not deform during subsequent firings. Manufacturers confront these problems using a crystalline glass formulation with a carefully balanced viscosity. After initial firing, the viscosity of the glass material actually increases. A 10:1 change in viscosity is possible on subsequent firings.

The vehicle is a solvent used to plasticize the thick film paste and give the compound its printing characteristic. These solvents contribute 12% to 25% of the weight of the paste prior to firing. After printing, the solvents are removed from the paste by either air drying or a low temperature bake at about 100 C.

3.2 Circuit Geometries

Probably the greatest motivation for designing with thick films is that they allow tremendous circuit density with simple and proven fabrication methods. With proper

process control, 5 mil line widths and spacings are obtainable with as many as eight conductor layers. Even though smaller line geometries are possible, line widths and spacings are usually designed to a minimum of 10 mils to allow for voids and spreading. The amount of spreading is primarily a function of vehicle content in the paste. It is not uncommon for the paste to spread as much as 2 mils on each side of the screened line. Although the circuit artwork and screen may have 10 mil line widths and spacings, the final screened circuit may actually have adjacent lines 14 mils wide and 6 mils apart. If a sensitive design requires 10 mil line separations, then adjustments should be made in the artwork to compensate for lateral spreading of the conductor paste.

Figure 3.1a shows a magnified view of a thick film circuit. At high magnification, it is evident that the edges and corners of the screened conductors are not perfectly straight or square. Also, the figure gives a good view of the nonhomogeneous structure of the thick film conductor. Grey packets of glass binder can be seen among the gold particles. Surprisingly, the dielectric material, upon which the gold was screened, appears smooth and free of voids. Figure 3.1b shows a cross section of thick film conductors buried in a multilayer substrate. Conductor thickness may vary from 0.2 to 1.0 mils. The screened dielectric thickness may range from 0.5 to 2.0 mils,

a. Screened Thick Film Conductors (100X)

b. Cross Section of a Multilayer Circuit (200X)

Figure 3.1 Thick Film Conductors

depending on the material and how many layers are applied. Typical practice is to apply at least two dielectric layers between conductor layers to prevent electrical failures due to pin holes. Noteworthy of figure 3.1b is that the conductor widths are over four times greater than the thickness of the isolation layers. This photo also shows two parallel signal lines on different layers. Generally, the designer tries to place parallel lines, on separate layers, 10 mils apart. However, as shown, this precaution is not always feasible. Signal lines may overlap and be separated by only a few mils of dielectric material. Thus, the multilayer hybrid designs can be particularly vulnerable to the crosstalk problem.

3.3 Transmission Line Model

The high speeds of current digital circuits often require that the circuit interconnections be analyzed as transmission lines. The signal lines no longer behave as simple conductors, yet instead, they introduce delays and attentuation to the transmitted signals. Basic transmission line concepts are reviewed in this section and subsequently used to estimate stray capacitance on the test cards and to interpret crosstalk noise measurements.

In principle, a lumped parameter approximation of a transmission line model can be displayed schematically as shown in figure 3.2,[3] where:

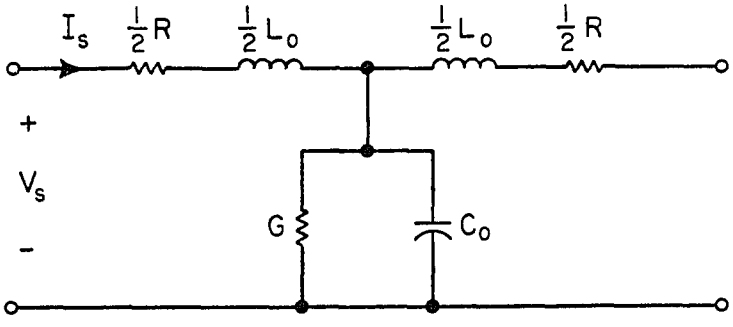


Figure 3.2 Lumped Parameter Transmission Line Model

L_o - Series Inductance Per Unit Length

C_o - Shunt Capacitance Per Unit Length

R - Series Resistance Per Unit Length

G - Shunt Conductance Per Unit Length

The characteristic impedance, Zo, of the line is defined by

$$Zo = \sqrt{\frac{R + L_o}{G + C_o}} \text{ ohms} \tag{3.1}$$

For short interconnect lengths, lossless transmission line theory may be utilized to simplify circuit analysis. With the lossless model, it is assumed that the conductor and insulator materials are homogeneous. At high frequencies, the series resistance and shunt conductance are considered to be very small in comparison to the series inductance and shunt capacitance. With negligible losses, the characteristic impedance is expressed as[4]

$$Zo = \sqrt{\frac{L_o}{C_o}} \text{ ohms} \tag{3.2}$$

For the lossless case, the impedance is real and behaves like a resistive load. Considering the nonhomogeneous composition of the thick film materials, the validity of the lossless assumption must be tested.

Three common thick film circuit configurations are shown in figure 3.3 along with equations for their transmission line parameters.[3] Microstrip lines are the most common circuit configuration found in thick film hybrids. Clearly, the microstrip has an abrupt change in dielectric

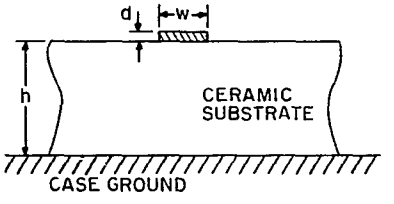
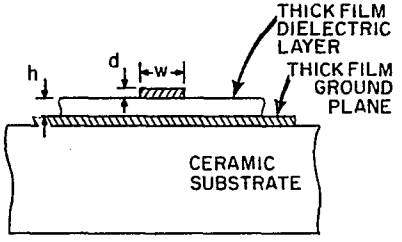
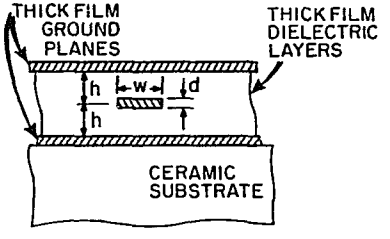
		Z_o (OHMS)	C_o $\left(\frac{\text{FARAD}}{\text{METER}}\right)$	L_o $\left(\frac{\text{HENRY}}{\text{METER}}\right)$
 SINGLE LAYER MICROSTRIP	$w<h$	$\frac{\sqrt{\frac{\mu_o}{\epsilon_{re}\epsilon_o}}}{2\pi} \ln\left[\frac{2\pi h}{w+d}\right]$	$\frac{2\pi\epsilon_{re}\epsilon_o}{\ln\left[\frac{2\pi h}{w+d}\right]}$	$\frac{\mu_o}{2\pi} \ln\left[\frac{2\pi h}{w+d}\right]$
 MULTILAYER MICROSTRIP	$h<w$ $d<h$	$\sqrt{\frac{\mu_o}{\epsilon_{re}\epsilon_o}} \frac{h}{w}$	$\frac{\epsilon_{re}\epsilon_o w}{h}$	$\frac{\mu_o h}{w}$
 STRIPLINE	$h<w$ $d<h$	$\sqrt{\frac{\mu_o}{\epsilon_r\epsilon_o}} \frac{h}{2w}$	$\frac{2\epsilon_r\epsilon_o w}{h}$	$\frac{\mu_o h}{2w}$

Figure 3.3 Transmission Parameters of Common Circuit Configurations

between the air and the substrate below it. Since electromagnetic waves travel faster in air than in dielectric materials, signals travel faster on the microstrip than if the lines were buried in the thick film dielectric material. Therefore, there is an effective dielectric constant that is a composite of the air and insulator. This effective value, ϵ_{re}, is dependent on ϵ_r and the width to height ratio, w/h, of the conductor over the ground plane. For extremely narrow lines with very low w/h values, the electric field is shared equally between the air and the substrate.[1] At this extreme,

$$\epsilon_{re} \cong \frac{1}{2} (1 + \epsilon_r) \tag{3.7}$$

In contrast, for very wide conductors with high w/h ratios, nearly all of the electric field is confined to the substrate.

$$\epsilon_{re} \cong \epsilon_r \tag{3.8}$$

The ranges of ϵ_{re} will lie between these two extremes. Figure 3.4 shows the effective dielectric constant of a microstrip conductor plotted versus the width to height ratio. This curve was derived from Super-Compact, a microwave CAD program, and is based on the Bryant-Weiss analysis technique.[8]

For multilayer hybrids, line capacitance is expected to be much higher than typically found in printed circuit boards due to the relatively higher w/h ratios and

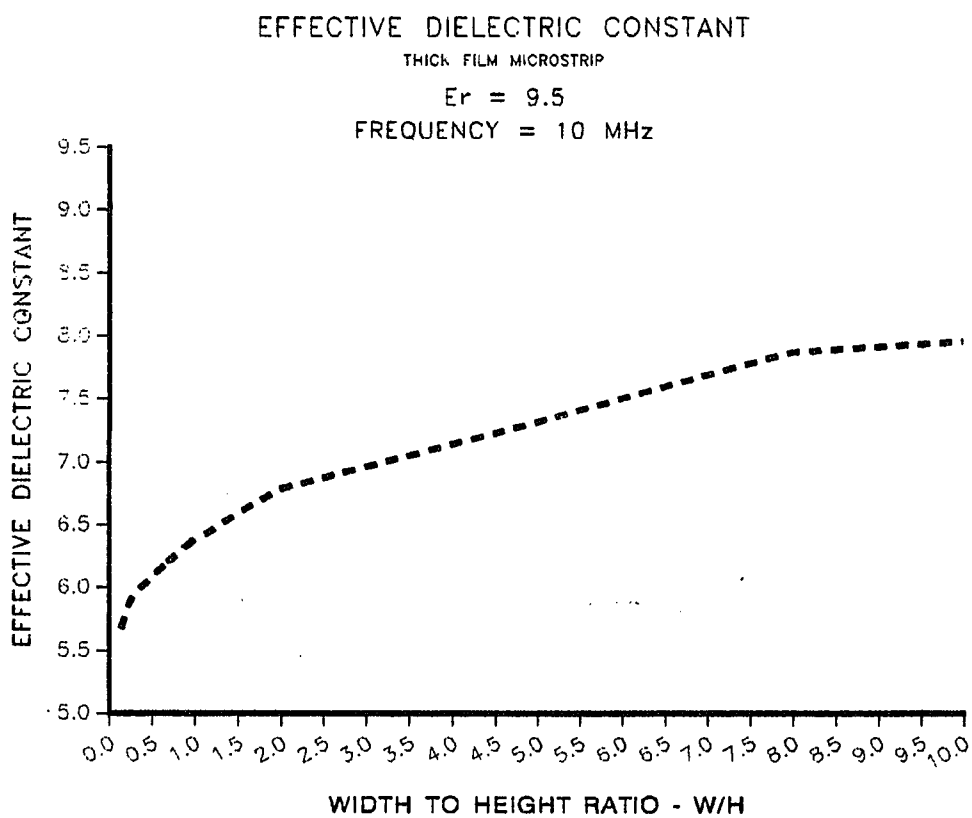


Figure 3.4 Effective Dielectric Constant For Thick Film Microstrips

the higher dielectric constants. Conversely, characteristic impedances should be lower for the same reasons.

Stripline configurations are widely used in hybrid layouts to achieve very low line impedance and good noise immunity. As shown in figure 3.3, the signal interconnect is sandwiched in between two ground planes. Generally, the stripline produces half the line impedance of a multilayer microstrip with twice as much line capacitance.

3.4 Preparation of Test Cards

This study can be divided into two tasks. First, a considerable effort was applied to measuring stray capacitance on various thick film circuit geometries. Second, actual noise tests were performed. High frequency pulses were applied to different circuit layouts and the coupled noise was measured on the adjacent lines.

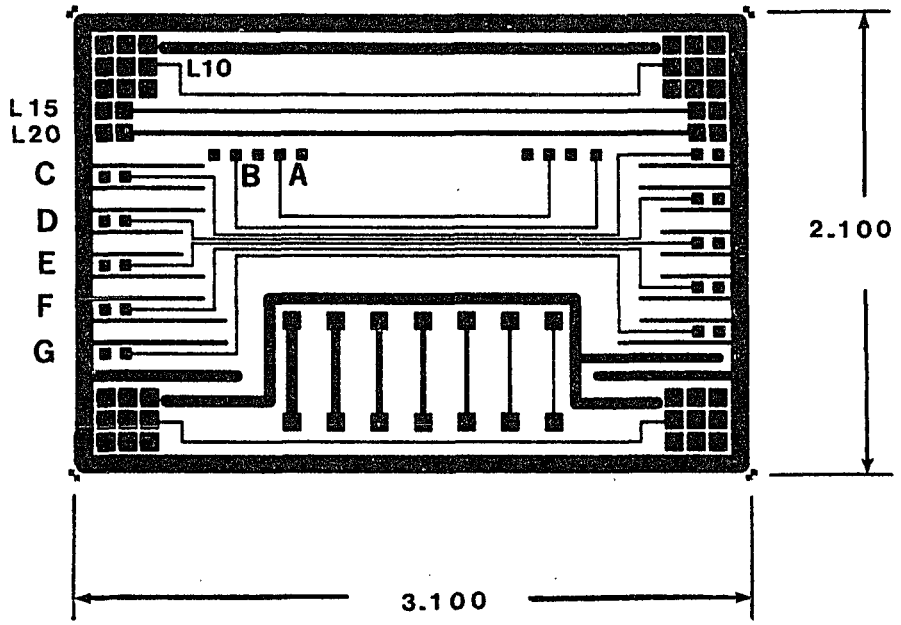
The test cards used in this project were made by screening test circuit patterns onto 3.15 x 2.15 inch alumina substrate blanks. Dupont 5715 gold conductor paste was used for circuitry, while Dupont 5704 dielectric paste was used for the insulation layers. Both materials feature good print resolution and are widely used for hybrid multilayer designs. With proper application, the 5715 conductor has a typical post fire thickness ranging from 0.3 to 0.4 mils and a sheet resistivity of 3.5 m $\Omega/\square$. Similarly, Dupont specifies a typical post fire thickness of 1.6 to

1.8 mils of 5704 dielectric, when two layers are applied. In actuality, the post fire thickness on the test cards was only .75 mils for the two layers, yet electrical isolation was still achieved.

Two test patterns were used for the measurements. The first test cards constructed were with the circuit pattern shown in figure 3.5. Lines L10, L15, and L20 were used to measure stray capacitance and basic transmission line parameters of 10, 15, and 20 mil lines. The 10 mil lines labeled A thru G were used to measure coupled capacitance and crosstalk. The spacing between each of these lines varies from 8 mils to 30 mils.

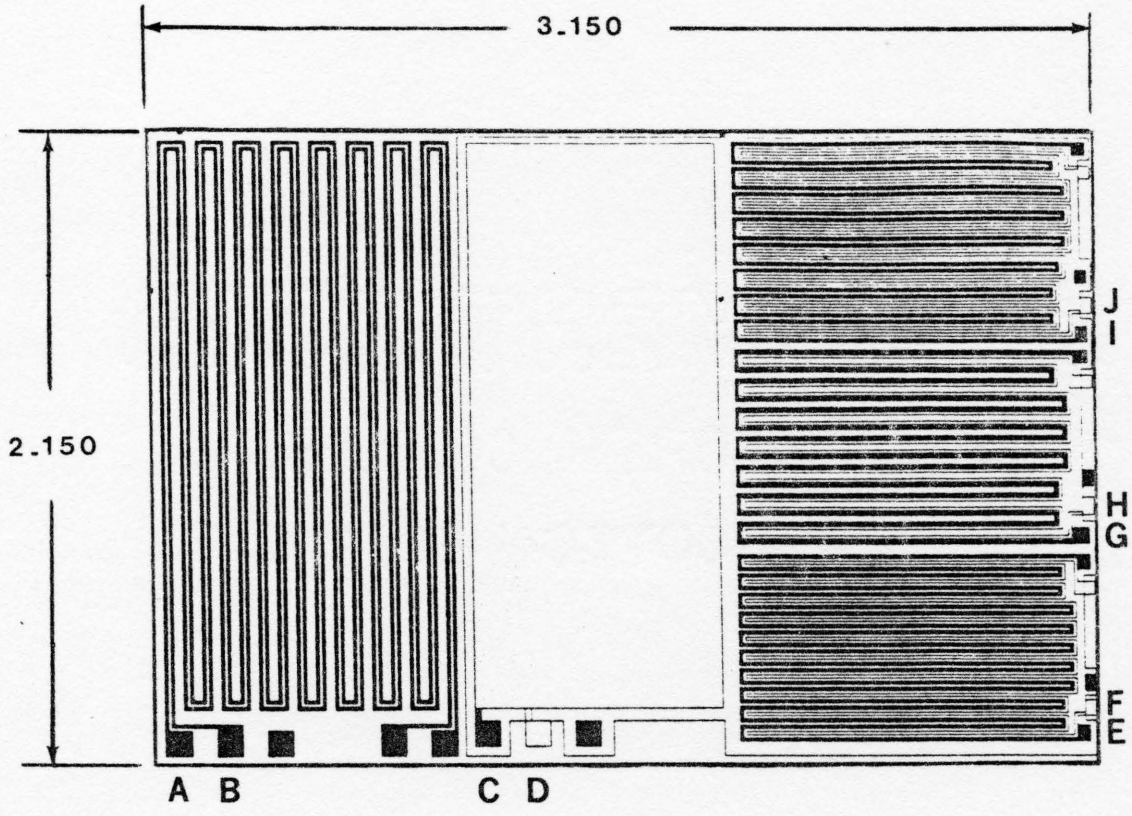
With this first pattern, five test cards were printed. Variations were made by printing the conductors at different heights from the ground plane, in microstrip and stripline configurations. Another test pattern was designed to test the loss properties of the dielectric and the stray capacitive effects of parallel lines on multilayer circuits. The capacitor test pattern is shown in figure 3.6. Lines A and B were used to accurately measure the edge to edge coupling capacitance of 10 mil parallel lines on a single layer. A serpentine pattern was used to create long line lengths and fairly large capacitor and inductor values. In total, lines A and B share a common edge 29.03 inches long. Although 10 mil conductor spacing

CONFIGURATION	TEST CARD REFERENCE DESIGNATOR	DIELECTRIC THICKNESS
SINGLE LAYER MICROSTRIP	MS0D	30.0 MILS
MULTILAYER MICROSTRIP	MS2D	0.75 MILS
MULTILAYER MICROSTRIP	MS4D	1.52 MILS
MULTILAYER STRIPLINE	SL2D	0.75 MILS
MULTILAYER STRIPLINE	SL4D	1.52 MILS



LINE WIDTHS	L10	12 MILS
	L15	17 MILS
	L20	22 MILS
LINE SPACINGS	A-B	29 MILS
	B-C	23 MILS
	C-D	6 MILS
	D-E	8 MILS
	E-F	12 MILS
	F-G	17 MILS

Figure 3.5 Crosstalk Test Pattern



TEST CARD REFERENCE DESIGNATOR	NUMBER OF DIELECTRIC LAYERS	DIELECTRIC THICKNESS
C2D	2	1.50 MILS
C4D	4	4.50 MILS
C6D	6	6.00 MILS
C8D	8	9.00 MILS
C10D	10	11.0 MILS
C12D	12	12.5 MILS

Figure 3.6 Capacitance Test Pattern

was used in the artwork design, the actual separation was measured at 6 mils.

The next segment of the test cards was dedicated to large area capacitor measurements. Total area of the capacitor plates is 1.388 inches square. This large area allowed accurate measurements of capacitance and the loss properties of the thick film dielectric material. Finally, three multilayer serpentine patterns were screened so that the capacitance between parallel multilayer lines could be measured. Six cards were printed and tested with this pattern. Each card had a different number of dielectric layers, varying from 2 to 12.

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Electrical Characterization of the Test Cards

Prior to conducting crosstalk measurements, a number of experiments were dedicated to measuring the noise coupling parameters of the thick film test patterns using a multi-frequency LCR meter. The instrument, a Hewlett Packard 4275A, basically injects a sine wave of known frequency, voltage and current into the test sample. At the output, voltage, current and phase are measured and an impedance vector is automatically calculated. With the impedance and phase information, conductance, inductance, capacitance and dissipation factors are automatically calculated by an internal processor. Measurements are possible over a range from 10 KHz to 10MHz with accuracies of 0.1% or less. The instrument also features an automatic zero routine to cancel stray inductance and capacitance in the test probes.

The resistivity of thick film conductors was measured on capacitance test card, C2, shown in figure 3.6. A total resistance of 7.02 ohms was measured on line A. Considering that the serpentine line is 29.03 inches long and 14 mils wide, the sheet resistance is found to be

$$\rho_s = \frac{(7.02\,\Omega)\ (.014\ \text{in}/\square\ )}{29.03\ \text{in}} = 3.38\ \text{m}\Omega/\square$$

This value is in agreement with the manufacturer's specification of 3.5 $\text{m}\Omega/\square$ for the 5715 gold conductor.

Attempts to measure line inductance and mutual inductance in the test cards were unsuccessful. Line and stray inductance are estimated to be lower than 100 nH, which is below the reliable measurement range of the meter.

Capacitance, however, could be measured. The large area capacitors, at pads C and D on the capacitance test cards, were used to study the capacitive properties of the thick film dielectric. The tests showed the capacitance to be very stable over a frequency range of 10KHz to 10MHz, with dissipation factors below 0.2%. Figure 4.1 shows the capacitance per square inch plotted versus the dielectric thickness. From these measurements, the relative permittivity of the thick film dielectric can be calculated. For example, 1390 pf/in^2 was measured on test card C2. The thickness of the two layers of dielectric screened onto this card was measured at 1.5 mils, yielding

$$\epsilon_r = \frac{(1390\ \text{pf/in}^2)\ (1.5 \times 10^{-3}\ \text{in})}{(8.85 \times 10^{-12}\ \text{F/m})\ (.0254\ \text{m/in})} = 9.3$$

Thus, there is good agreement with the manufacturer's specification of 9 - 10, for the 5704 dielectric paste.

Area capacitance was also measured for single layer conductor pads printed on an alumina substrate. The values

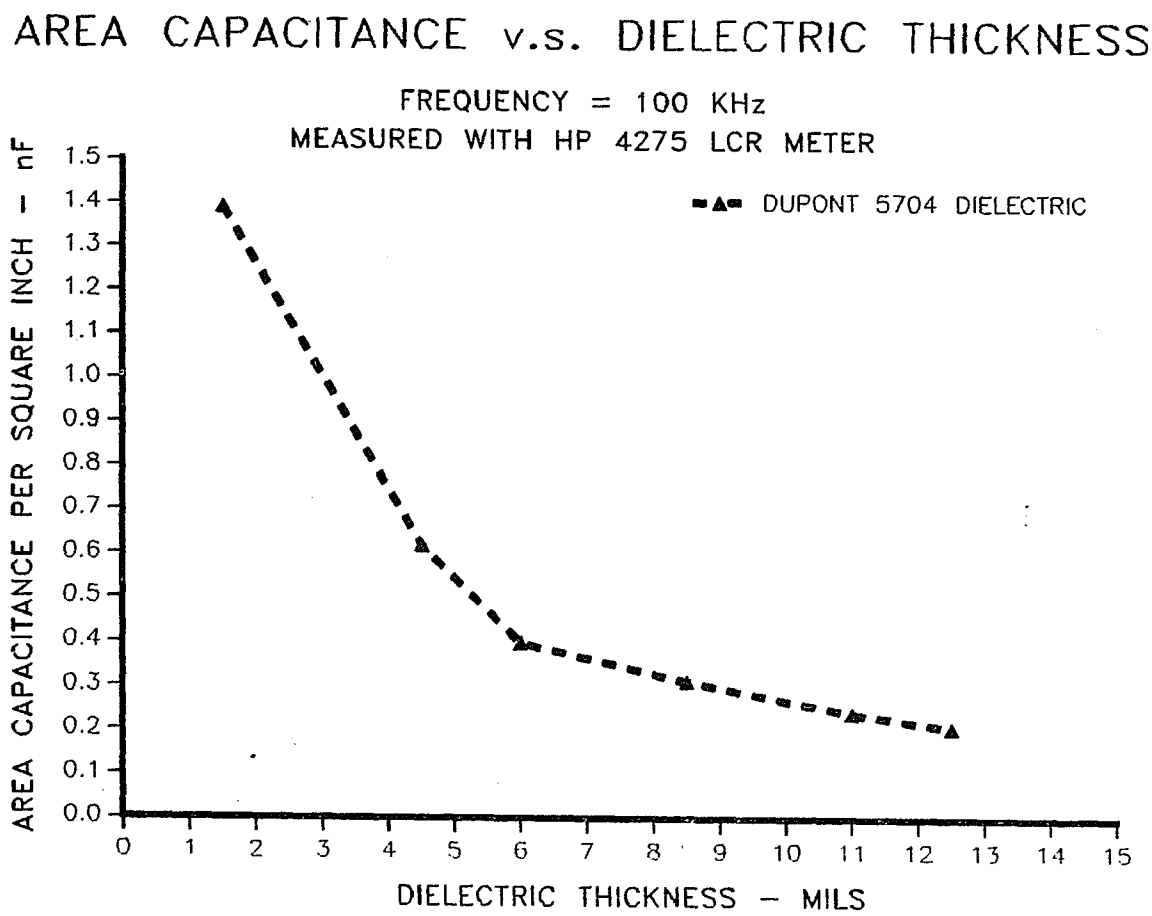


Figure 4.1 Area Capacitance vs. Dielectric Thickness

represent the stray capacitance that occurs between the single layer conductors and the metal hybrid case and were significantly lower than the capacitance found in the multilayer cards. Again, the capacitance showed only slight variation over frequency and the dissipation factors were below 0.2%. For the capacitance test card, C2, the area capacitance measured through 38.5 mils of the alumina substrate is 56.3 pf/in^2. The relative permittivity of the alumina is then

$$\epsilon_r = \frac{(56.3 \text{ pf/in}^2)\ (.0385 \text{ in})}{(8.85 \times 10^{-12} \text{ F/m})\ (.0254 \text{ m/in})} = 9.6$$

which agrees with the manufacturer's specification of 9.5 and is similar to the permittivity of the dielectric paste. However, due to the thinness of the dielectric layers, the multilayer designs inherently have more stray capacitance within the circuit.

Line capacitance, C_o, was measured on the crosstalk test cards. As expected, the single layer microstrip card, MS0D, exhibited the lowest values with only 2.2 pf/in for a 12 mil wide line. In comparison, the stripline had the largest capacitance with 54.2 pf/in measured on a 12 mil line. Generally, the measured values were in agreement with the line capacitance calculated from the equations of figure 3.3. Figures 4.2 and 4.3 show both measured and calculated values of shunt capacitance, for microstrips and striplines, plotted as a function of line width. A

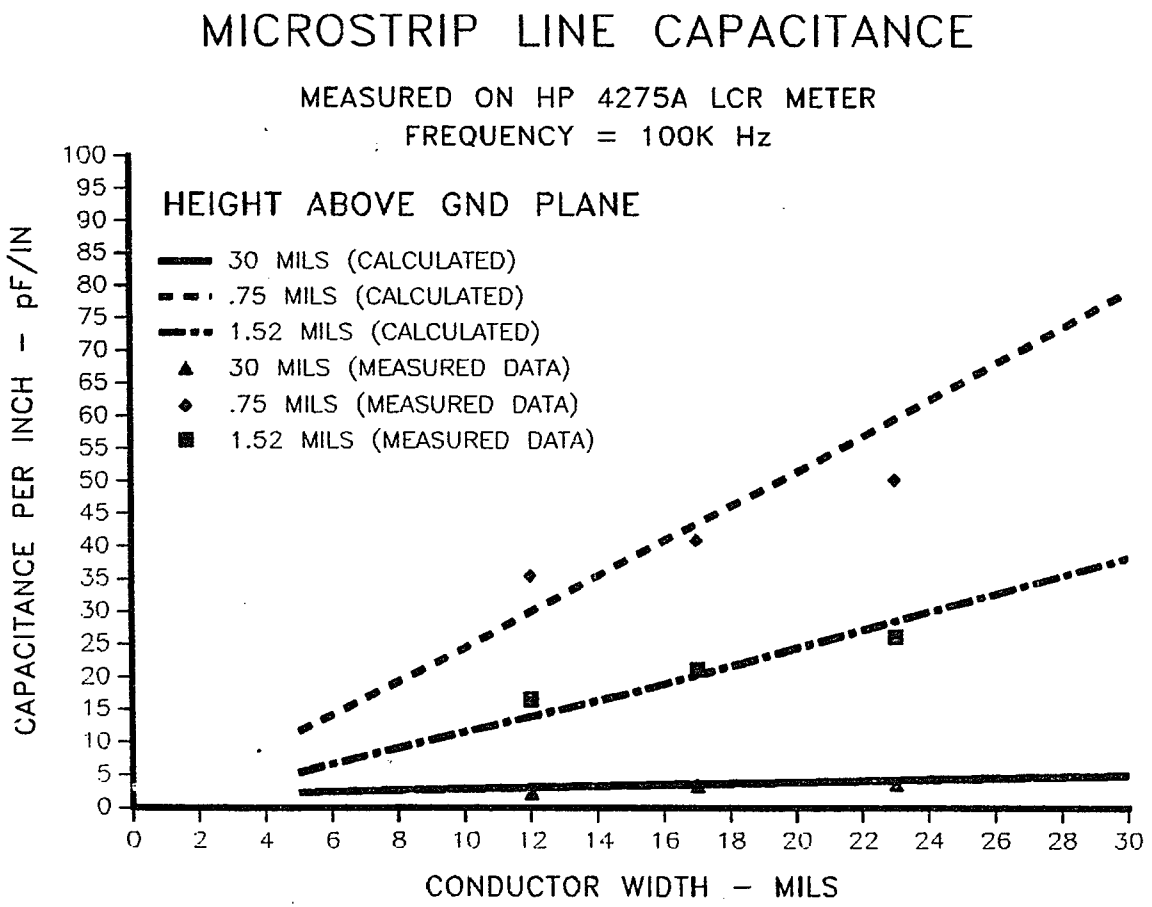


Figure 4.2 Microstrip Line Capacitance

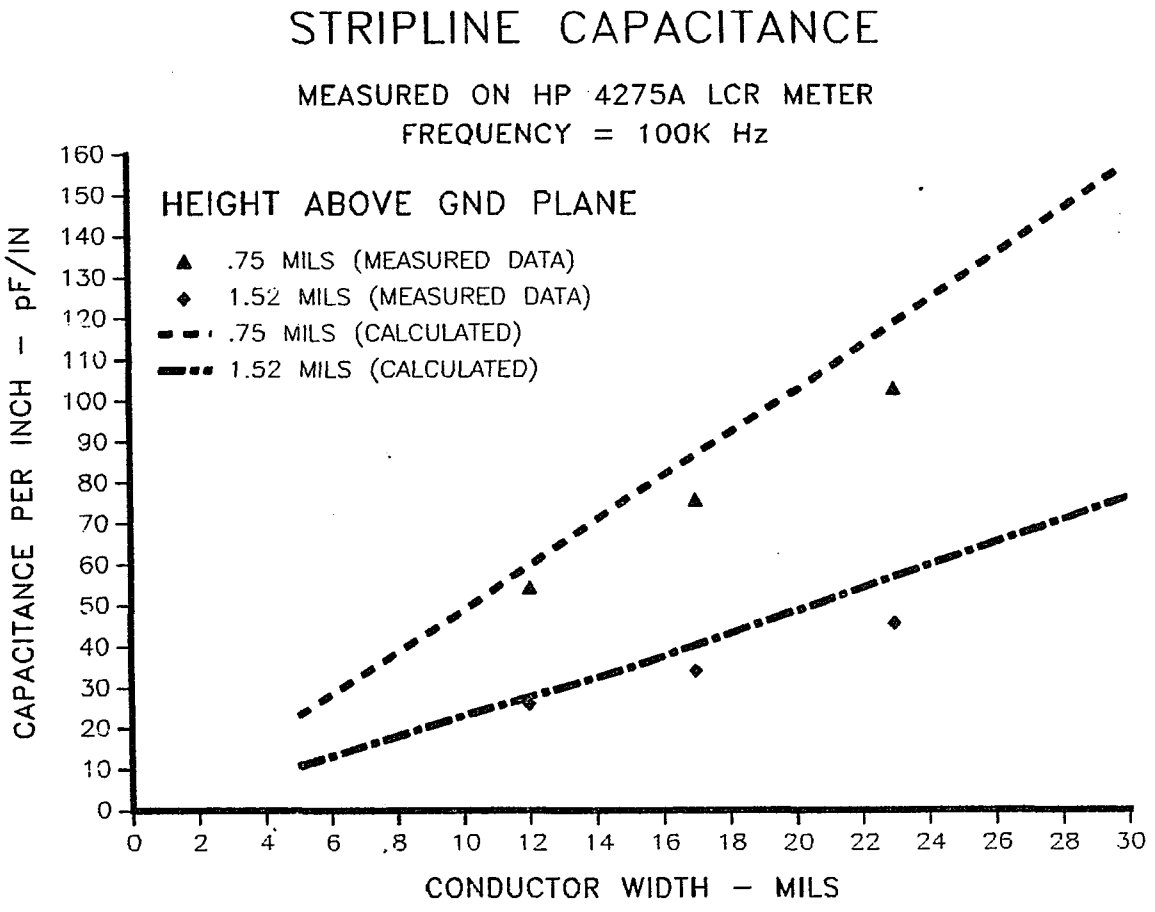


Figure 4.3 Stripline Line Capacitance

dielectric constant of 9.3 was used to calculate the capacitance of the striplines. For the microstrips, the curve of ϵ_{re} versus w/h, in figure 3.4, was used to determine the effective dielectric constant. From the curves, one sees that the line capacitance on the multilayer substrates are an order of magnitude greater than the values found on the single layer microstrip. Large line capacitance causes signal switching delays excessive signal attenuation. Figure 4.4 shows the shunt impedance measured on the microstrip cards plotted against frequency. The shunt impedance of the multilayers quickly drops below 100Ω as the frequency exceeds 10MHz. Apparently, the high frequency capabilities of the thick film multilayers are limited.

Next, the measurements were focused on the coupled capacitance between adjacent signal lines. Figure 4.5 shows the capacitance measured between two coplanar lines on the single layer crosstalk card, MS0D. For a substrate layout with 10 mil line separation, the coupled capacitance is merely 1.6 pf/in.

With the multilayer crosstalk cards, the measurements were not as successful. The problem appeared to be related to the inability to obtain an absolute ground reference on the test card's ground plane. In an attempt to assure a good ground, a braided wire strap was soldered to each card's ground plane and connected to the meter ground. Nevertheless, as much as 20 pf/in was measured between the

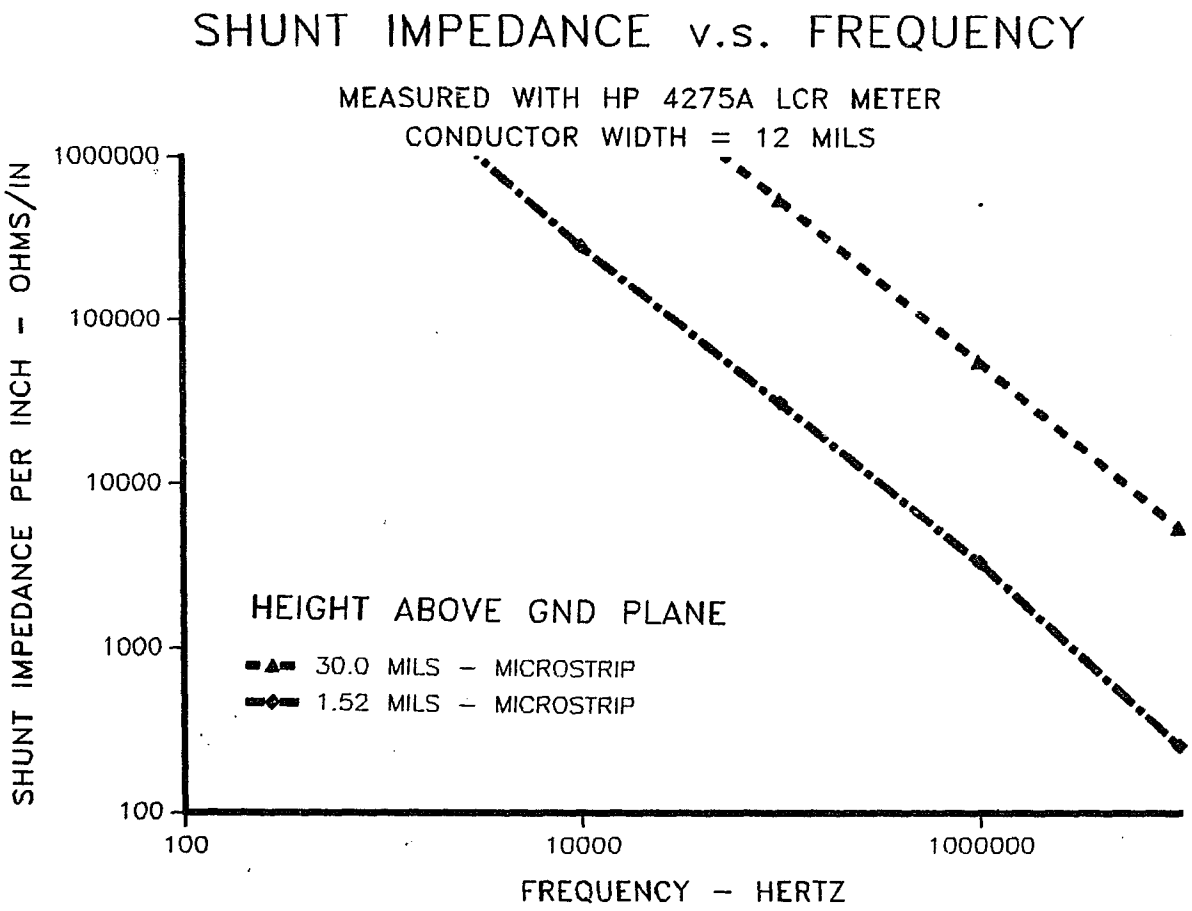


Figure 4.4 Shunt Impedance vs. Frequency

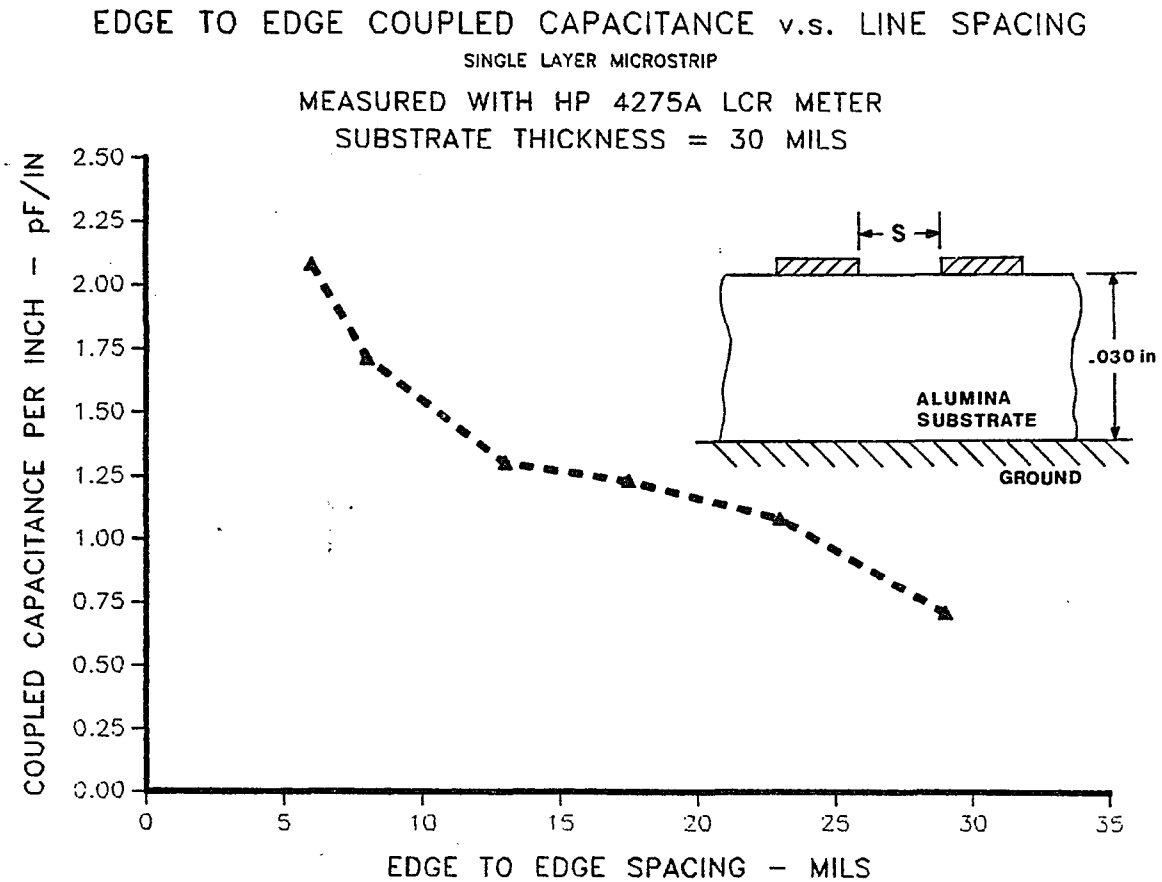


Figure 4.5 Edge to Edge Coupled Capacitance vs. Line Spacing

multilayer conductors with very little variation due to line separation. This is contrary to microstrip and stripline theory. The close proximity of the ground plane should reduce the field interaction between adjacent lines. Thus, the coupled capacitance should be much less than what was measured on the single layer microstrip. Evidently, the measurements were actually the series connection of each conductor's line capacitance. The short braided strap provided an insufficient ground and the capacitance of each line was coupled conductively to the adjacent line by the ground plane. Efforts to overcome this problem were unsuccessful.

Fortunately, a ground plane was not included in the layout of the capacitance test cards. This allowed the measurement of coupled capacitance between parallel lines on different layers. In a multilayer design, it is inevitable that conductors on different layers will run parallel, if not overlap one another. Measurements were taken between the serpentine pattern at pads C-D, E-F, and G-H. The coupled capacitance between layers is plotted versus the dielectric thickness in Figure 4.6. Note that there is almost 4 pf/in of capacitance between two conductors offset 10 mils apart on different layers, while only 1.6 pf/in was measured previously between coplanar lines of the same separation. This may partly be explained by misregistration and overlap. Thus, the multilayer lines may actually be

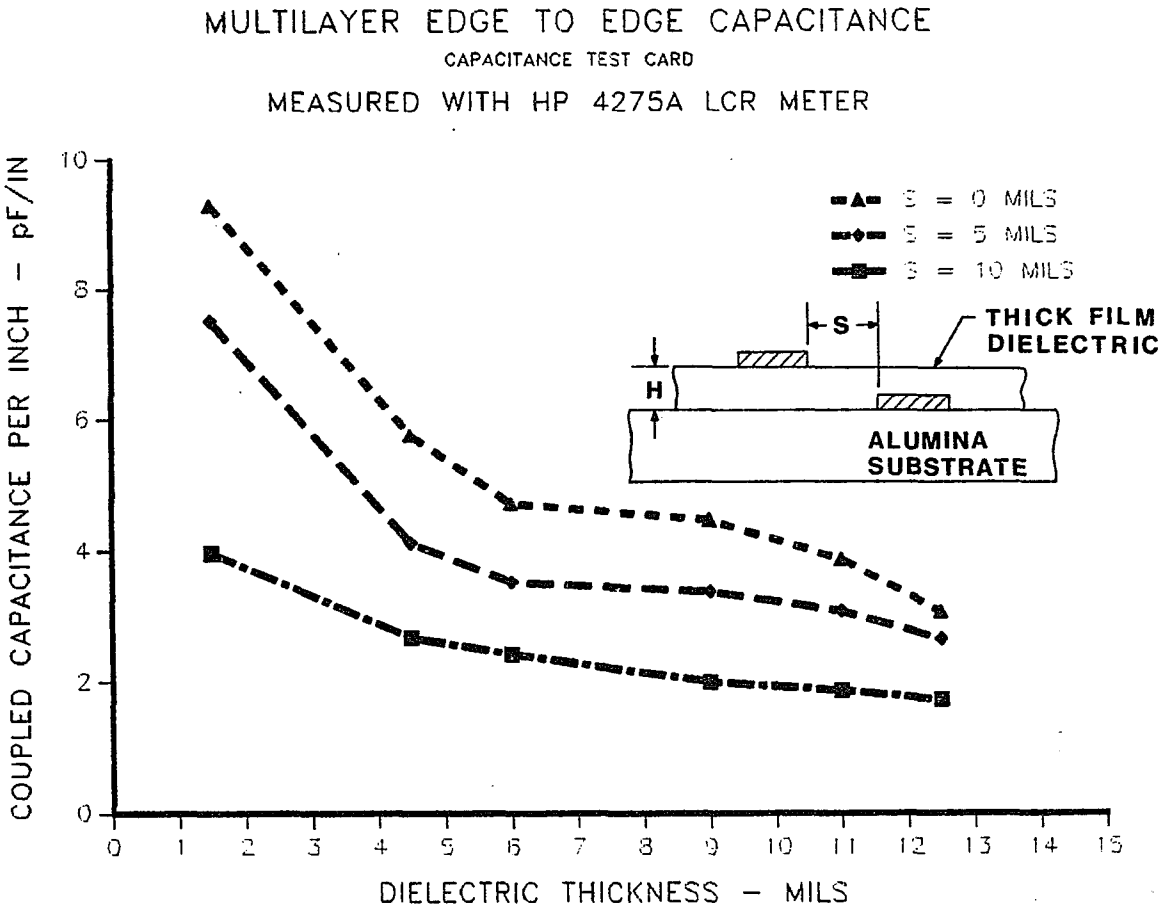


Figure 4.6 Multilayer Edge to Edge Capacitance vs. Dielectric Thickness

closer than 10 mils. More importantly is the fact that the buried conductor is surrounded by dielectric material. The effective dielectric constant between the two lines is higher than that for the coplanar lines. This allows a denser electric field to reside around the buried conductor and a greater field interaction between the two parallel lines.

4.2 Crosstalk Measurements

The procedure for the crosstalk measurements is to send a pulse down a conductor line and measure the induced pulse on the adjacent quiescent line. Probes were constructed with either 50Ω or 499Ω loads so that measurements could be taken when the lines were terminated with either high or low impedance.

Measurement of pulse signals below the 100 nanosecond range proved to be a difficult task. Stray capacitance and inductance in the test circuit had to be minimized to reduce signal delay and excessive impedances in the ground connections. Numerous trial and error experiments were required to produce a test setup that would yield accurate and repeatable measurements. Figure 4.7 depicts this test setup used. Each test card was placed on a 1 oz. copper plated epoxy board which provided a ground reference. Segments of coaxial cable from the oscilloscope and function generator were kept under one foot long to

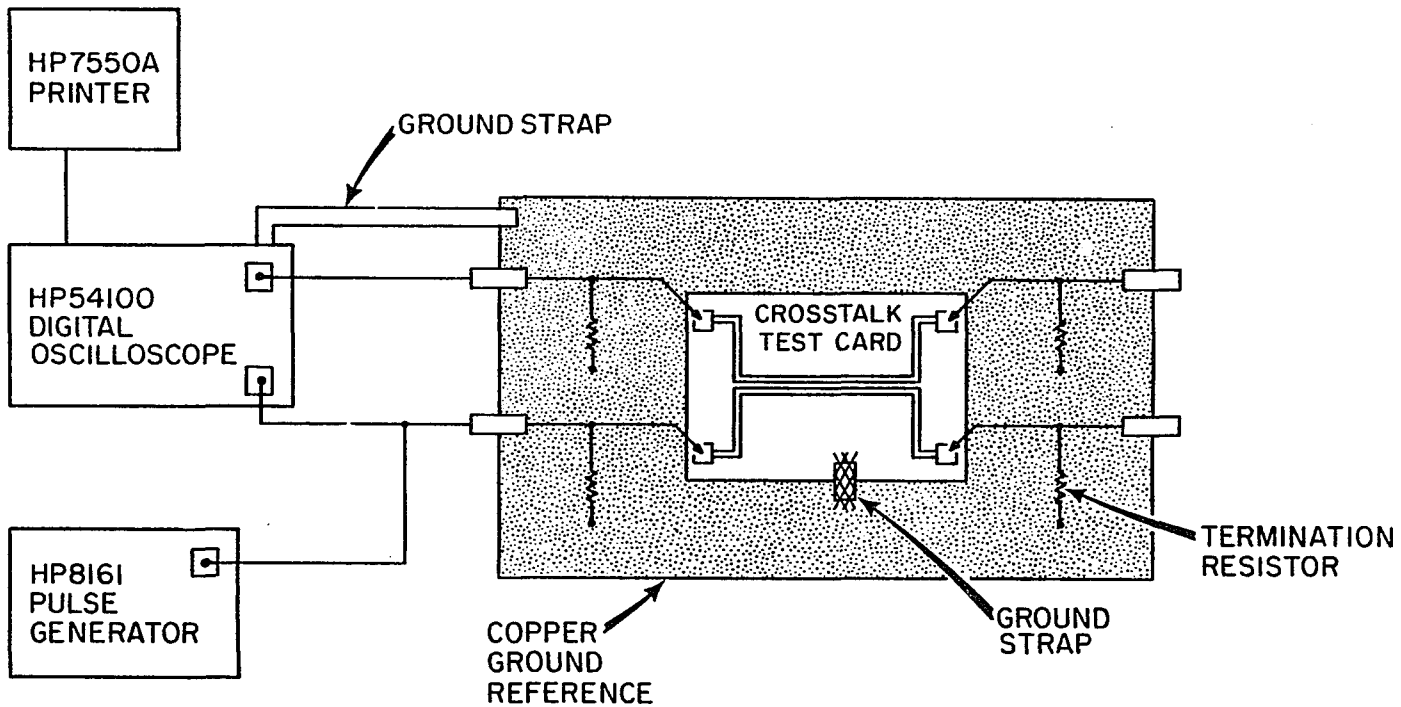


Figure 4.7 Crosstalk Test Setup

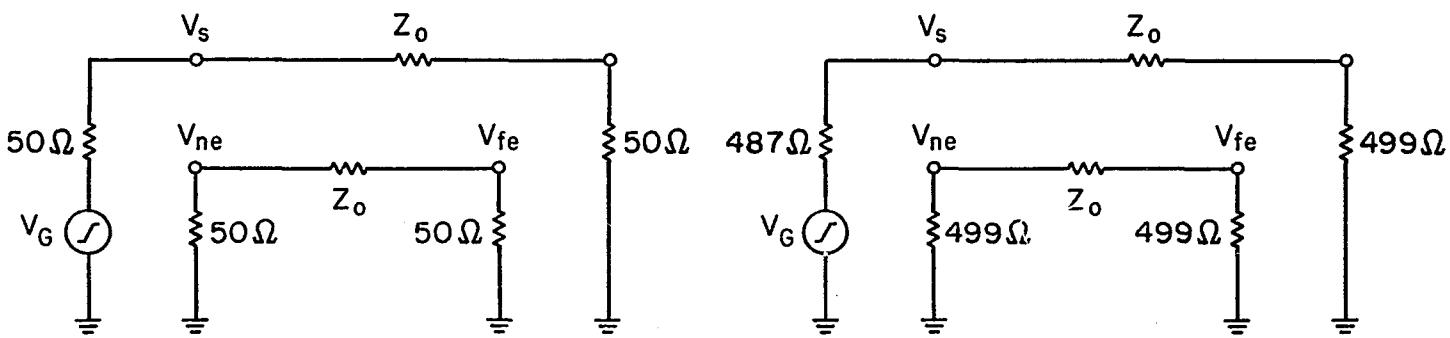
minimize stray inductance in the ground returns. These cables were plugged into coaxial connectors in the copper plate. From this point, short shielded wires were connected to the probe tips.

After some initial testing, it was evident that a probe contact was not a sufficient connection to the ground planes of the multilayer test cards. For a low impedance ground connection, a braided wire was soldered along the ground trace of the test cards and then onto the copper plate.

Pulse signals were created with a Hewlett Packard 8161 pulse generator. To measure these signals, an HP 54100 digitizing oscilloscope was used. This instrument allows accurate waveform analysis and conveniently connects to a plotter for reproduction of the display. When applicable, 50Ω input pods were used with the oscilloscope while active probes were used to monitor lines with high impedance terminations.

The single layer microstrip, MS0D, was the first card tested. Schematic diagrams of the low and high impedance test circuits are shown in figure 4.8. The characteristic impedance of the single layer microstrip is large enough to be included in the circuit model.

$$Z_o = \frac{1}{2\pi}\sqrt{\frac{(4\pi \times 10^{-7}\ \text{H/m})}{(5.95)(8.85 \times 10^{-12}\ \text{F/m})}}\ \ln\left(\frac{2\pi\ (.030\ \text{in})}{(.0125\ \text{in})}\right) = 67\Omega$$



a. LOW IMPEDANCE TEST CIRCUIT

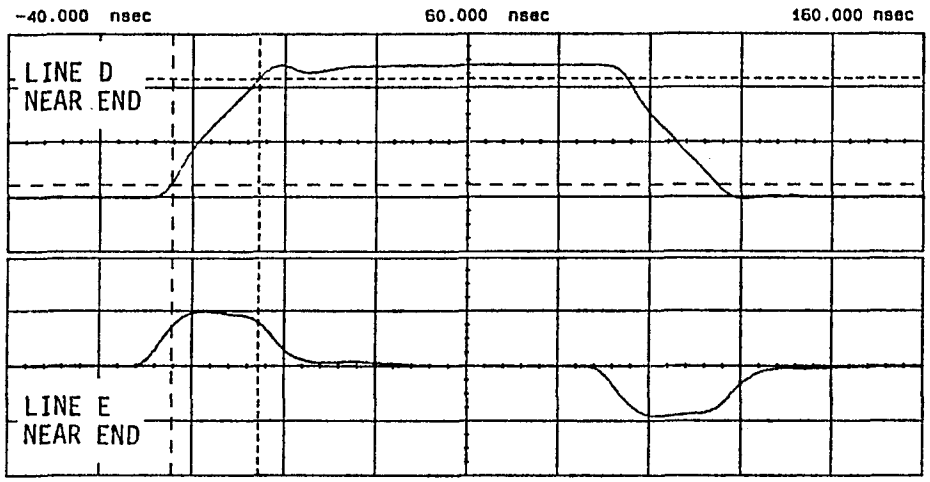
b. HIGH IMPEDANCE TEST CIRCUIT

Figure 4.8 Crosstalk Test Circuits

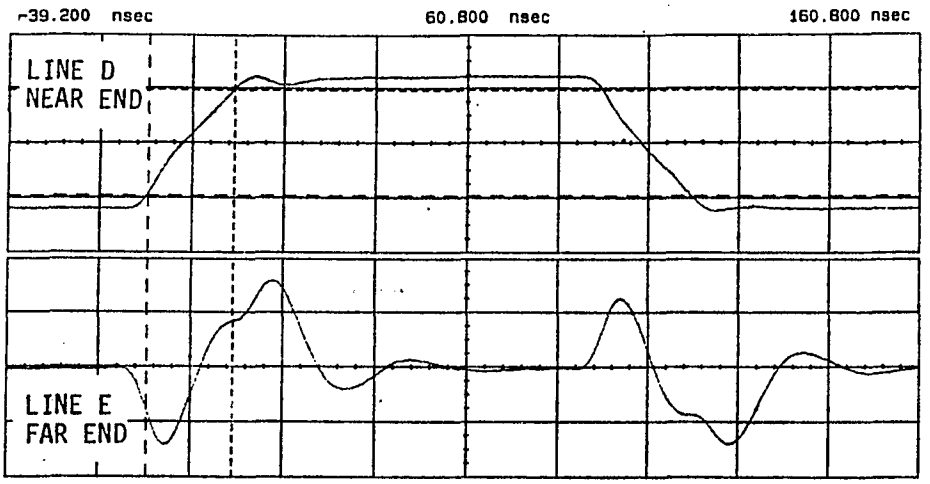
Figure 4.9 shows oscilloscope plots of the near end and far end crosstalk on the low impedance circuit. The two conductor lines are 8 mils apart and have a parallel length of 2.1 inches. The top plot of each figure displays the stimulating pulse on the active line. The oscilloscope voltage and time markers were set at the 10% and 90% amplitude levels to measure a voltage swing of 3.85 volts in a rise time of 18.87 nanoseconds. Faster edge speeds were possible with the signal generator, although the rise and fall times were kept high to minimize over-shoot and ringing effects in the stimulating pulse. The duration of the pulse was 100 nanoseconds so that any signal ringing would have sufficient time to dampen out.

The induced noise on the quiescent line is shown in the bottom waveform of each plot. At the near end, the noise pulse has a positive amplitude for the rising edge and a negative amplitude for the falling edge. The pulses rise and dampen in about 40 ns.

At the far end of the line, oscillations are evident. Initially, the induced pulse swings negative, which according to equation 2.8 indicates a high degree of inductive coupling. After about 12 nanoseconds, the far end pulse begins moving in the positive direction. Apparently, the oscillation is a step response to the L, C, and R network created by the conductor and the termination resistor.



Ch. 1	=	2.000 volts/div	Offset	=	2.000 volts
Ch. 2	=	100.0 mvolts/div	Offset	=	0.000 volts
Timebase	=	20.0 nsec/div	Delay	=	60.000 nsec
Delta T	=	18.870 nsec			
Start	=	-4.560 nsec	TEST CARD MSOD		
Delta V	=	3.850 volts	NEAR END NOISE		



Ch. 1	=	2.000 volts/div	Offset	=	2.380 volts
Ch. 2	=	40.00 mvolts/div	Offset	=	1.200 mvolts
Timebase	=	20.0 nsec/div	Delay	=	60.800 nsec
Delta T	=	18.910 nsec			
Start	=	-8.950 nsec	TEST CARD MSOD		
Delta V	=	3.856 volts	FAR END NOISE		

Figure 4.9 Crosstalk on a Single Layer Card
(Low Impedance Test Circuit)

Figure 4.10 shows near and far end crosstalk for the high impedance line. The rising edge of the stimulating pulse was reduced to 15.4 nanoseconds with a voltage swing of 3.08 volts between the 10% and 90% markers. With large termination resistors, less current flows along the active line and inductive coupling is minimized. This is evident by the fact that the polarity of the far end noise mirrors that of the near end. Yet, due to the large termination resistors, the amplitudes of the induced noise pulses on the quiescent line are still larger than they were for the low impedance circuit.

With both the high and low impedance oscilloscope plots, coupled capacitance and mutual inductance may be calculated with equation 2.7. For the low impedance line, the peak to peak value of the noise on the quiescent line was 191.0 mV. The near end voltage is then given by the equation.

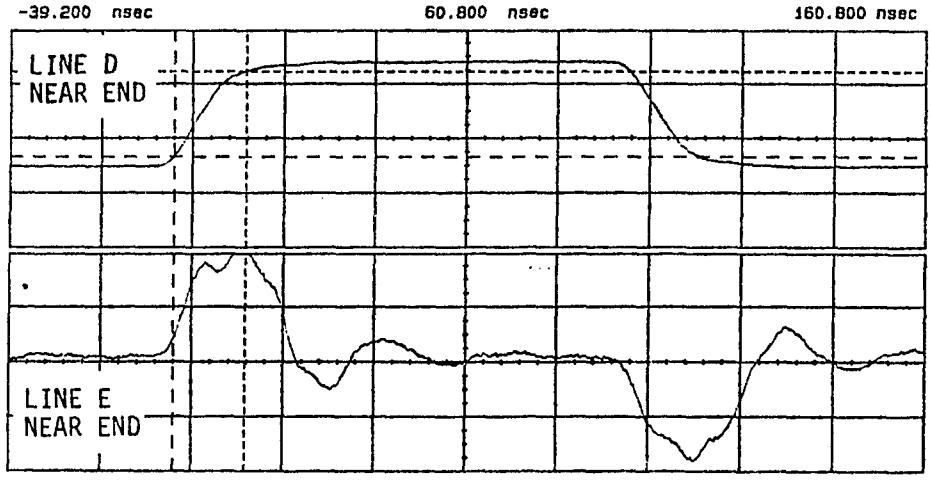
$$V_{ne} = \frac{.191\ V}{2} = \frac{C_c\ (50\Omega\ )(3.85\ V)}{2\ (18.81\ ns)} + \frac{L_m\ (3.85\ V)}{2\ (67\Omega\ +\ 50\Omega\ )(18.81\ ns)} \tag{4.1}$$

which yields,

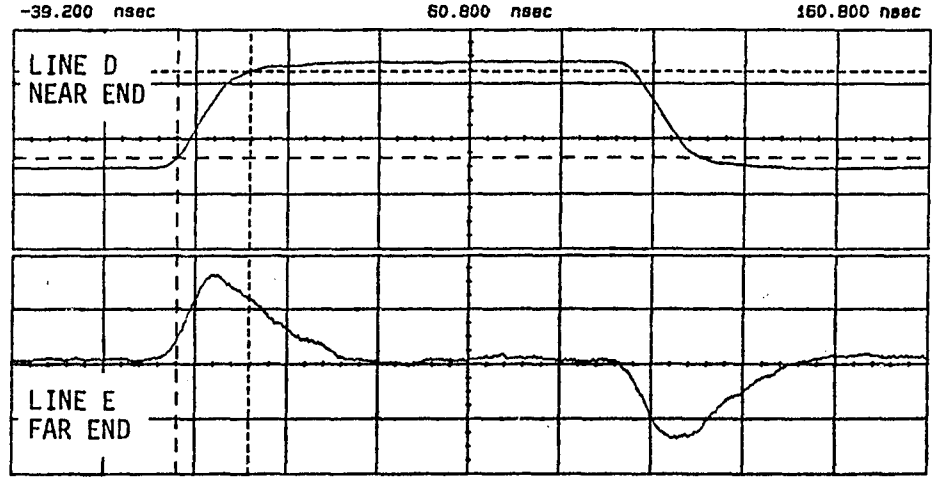
$$L_m = -\ 5.850 \times 10^{3}\ C_c + 1.090 \times 10^{-7}\ \ H \tag{4.2}$$

For the high impedance circuit, the peak to peak crosstalk noise at the near end was measured to be 381.1 mV.

$$V_{ne} = \frac{.381\ V}{2} = \frac{C_c\ (499\Omega\ )(3.088\ V)}{2\ (15.43\ ns)} + \frac{L_m\ (3.088\ V)}{2(67\Omega\ +\ 499\Omega\ )(15.43\ ns)} \tag{4.3}$$



Ch. 1	=	2.000 volts/div	Offset	=	1.000 volts
Ch. 2	=	100.1 mvolts/div	Offset	=	12.00 mvolts
Timebase	=	20.0 nsec/div	Delay	=	60.800 nsec
Delta T	=	15.430 nsec			
Start	=	-3.200 nsec	TEST CARD MSOD		
Delta V	=	3.088 volts	NEAR END NOISE		



Ch. 1	=	2.000 volts/div	Offset	=	1.000 volts
Ch. 2	=	100.4 mvolts/div	Offset	=	12.00 mvolts
Timebase	=	20.0 nsec/div	Delay	=	60.800 nsec
Delta T	=	15.510 nsec			
Start	=	-3.270 nsec	TEST CARD MSOD		
Delta V	=	3.088 volts	FAR END NOISE		

Figure 4.10 Crosstalk on a Single Layer Card
(High Impedance Test Circuit)

From equations 4.2 and 4.3, the coupled capacitance between the two lines is found to be

$$C_c = 3.58 \text{ pf}$$

Considering that the lines run parallel for 2.10 inches, the coupled capacitance per unit length is therefore,

$$C_c = 1.75 \text{ pf/in}$$

This value agrees with the 1.71 pf/in value obtained from the LCR measurements for lines separated by 8 mils. Hence, the validity of the crosstalk equations, 2.7 and 2.8, is demonstrated. Next, inserting the coupled capacitance into equation 4.2, the mutual inductance of the line is found.

$$L_m = 88.23 \text{ nH}$$

Again considering the line length,

$$L_m = 43.03 \text{ nH/in}$$

This is a large value, yet it explains the polarity of the waveforms observed for the near and far end crosstalk on the low impedance line.

In a similar fashion, crosstalk noise was measured and analyzed for the other line pairs on card MS0D to produce the plots of C_c and L_m versus line spacing that are shown in figures 4.11 and 4.12. In both cases, the coupling parameters decrease as the line separation increases. This is expected since the field interaction is reduced as the distance between the lines becomes greater. As expected, the amount of signal coupling decreases as the edge to edge conductor spacing increases. The degree of noise

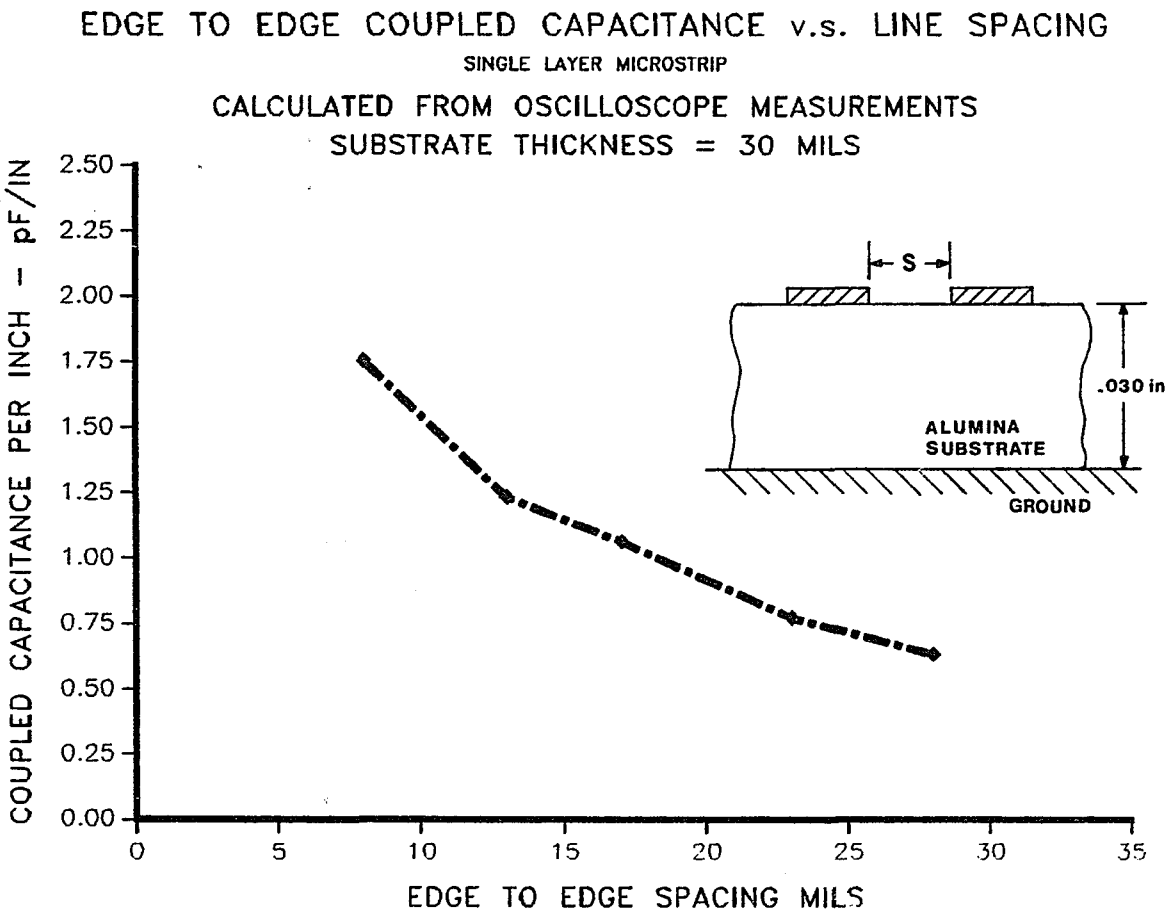


Figure 4.11 Edge to Edge Coupled Capacitance vs. Line Spacing

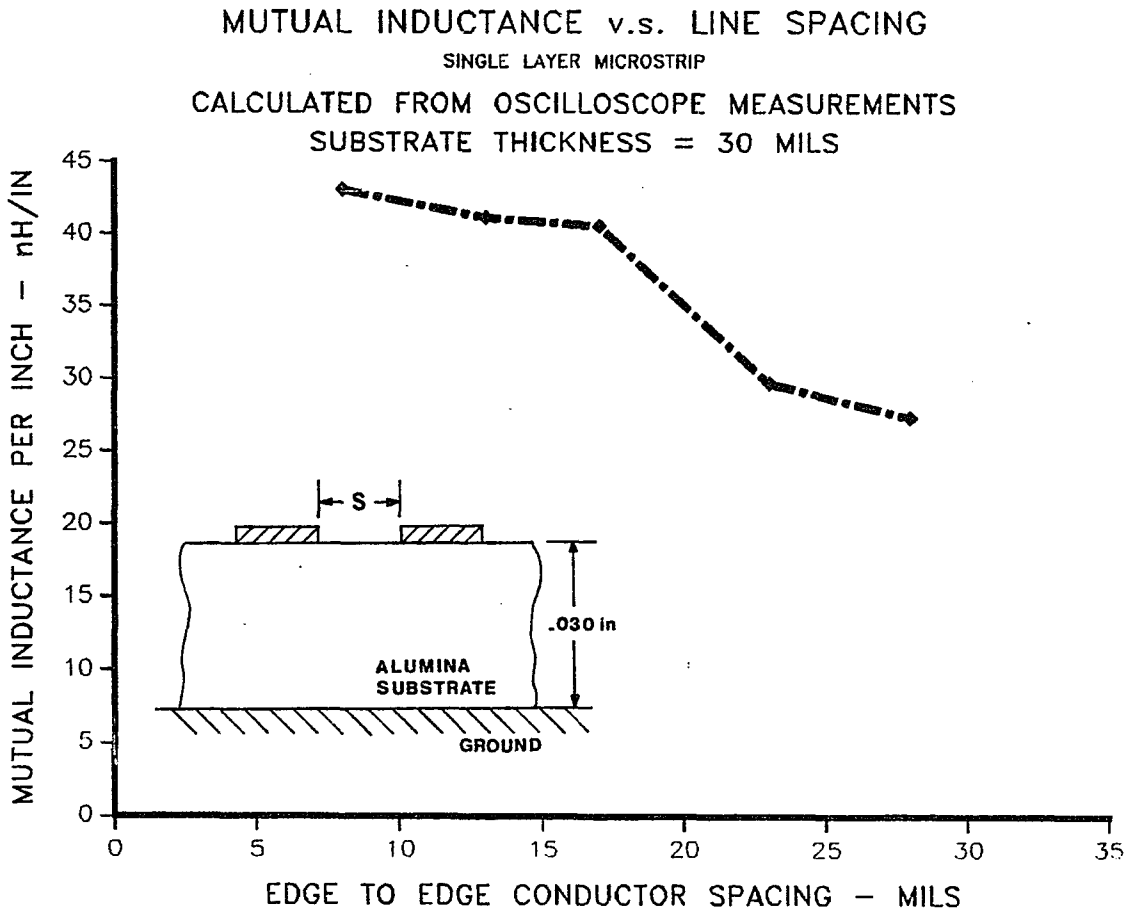


Figure 4.12 Edge to Edge Mutual Inductance vs. Line Spacing

coupling may be expressed as a ratio of the noise voltage and the stimulating pulse amplitude. Figure 4.13 shows the near and far end noise ratios plotted as a function of line spacing.

The electromagnetic field interaction also decreases as the conductor lines move closer to the ground plane. A single layer circuit on a thinner substrate or a multilayer over a ground plane is then expected to have far less capacitive and inductive coupling. This is also true for the stripline, where the ground plane on either side of the conductor is intended to reduce stray field interactions.

The first multilayer tested was the microstrip card, MS2D. Again, the same circuits in figure 4.8 were used to test the multilayer cards. An 8-volt pulse, with 15 ns rise and fall times, was transmitted from the generator to provide a stimulating pulse with amplitude and edge speeds similar to those used for the single layer measurements. The near and far end crosstalk is shown in figure 4.14. In both plots, channel 1 displays the stimulating pulse on the active line while channel 2 shows the noise induced onto the quiescent line. As before, forward and backward current flow is indicated by the opposite voltage swings at the near and far end of the quiescent line. The amplitude of the crosstalk on the multilayer is higher than observed for the single layer. In figure 4.9, the near end

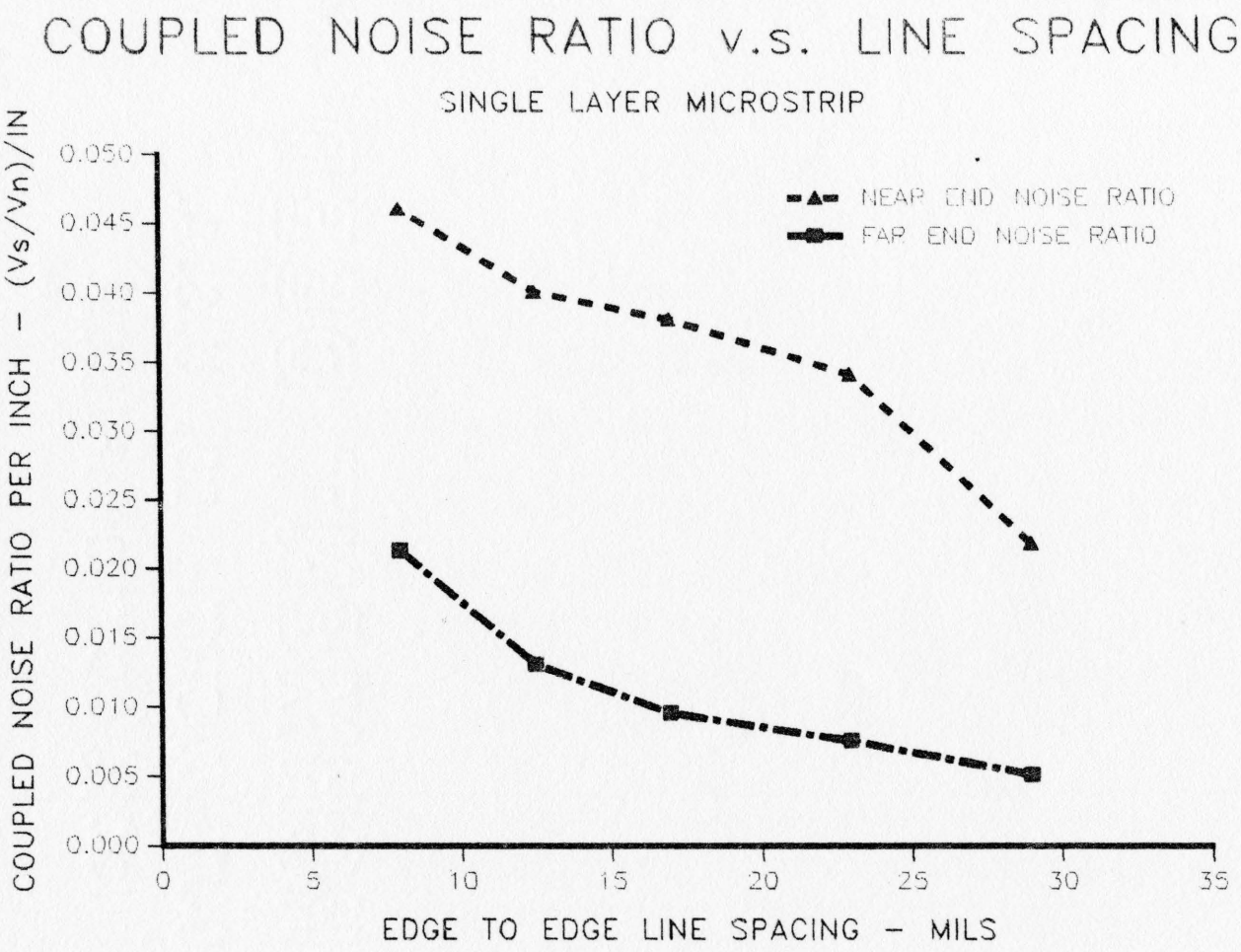
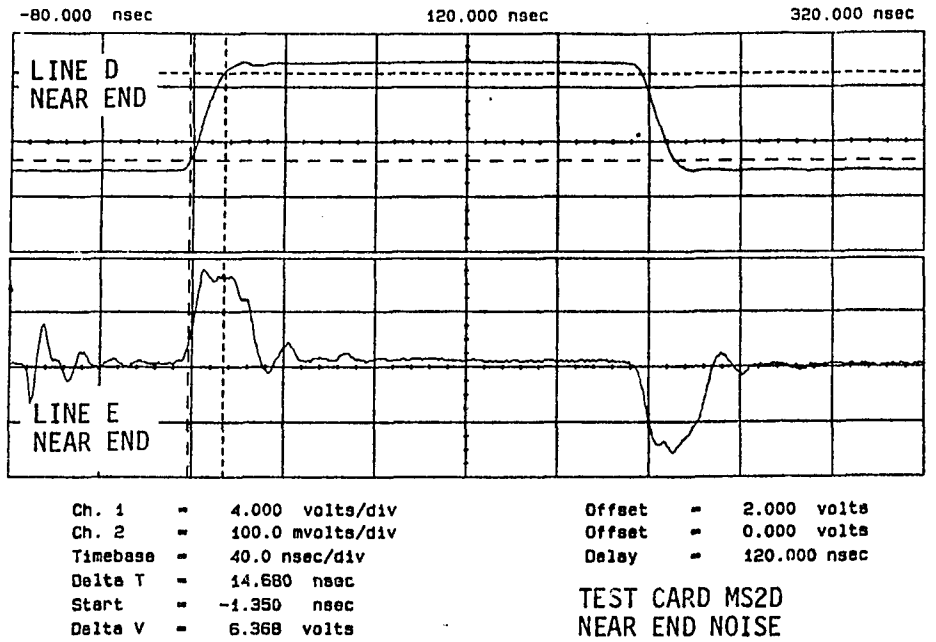


Figure 4.13 Coupled Noise Ratio vs. Line Spacing



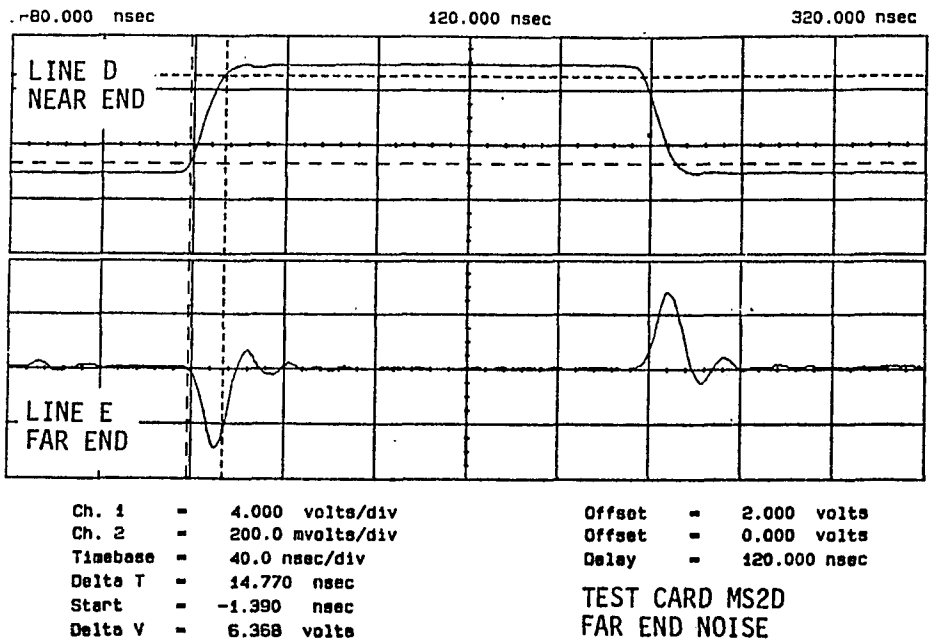


Figure 4.14 Crosstalk on a Multilayer Card
(Low Impedance Test Circuit)

crosstalk had a peak amplitude of 100 mV when the voltage of the stimulating pulse had a rate of 4.02×10^8 V/s. In contrast, the multilayer displays a 175 mV crosstalk pulse at the near end when the voltage rate on the stimulating pulse is 4.33×10^8 V/s. Although a slightly faster voltage rate was used to excite the multilayer circuit, the large signal coupling is unexpected due to the close proximity of the ground plane. With further testing it became apparent that much of the crosstalk noise on the quiescent line was coupled up from the ground plane. Figure 4.15 shows over 100 mV of noise pulse present on the ground plane at a location close to the near end of the stimulating line. Probing in various places showed that the amplitude of the noise on the thick film ground plane changed with location. Thus, the thick film seems to exhibit some current spreading limitations. It is also apparent that the braided wire strap soldered to the multilayer ground plane is not sufficient to produce an absolute ground reference. Further attempts to improve the connection between the test card and the copper ground reference proved unrewarding. Measurements were then attempted by referencing the scope probe to the thick film ground plane on the test card. The magnitude of the observed noise pulses dropped significantly, yet their amplitude varied with the placement of the ground connection on the thick film. It was not possible to produce repeatable measurements. Like the

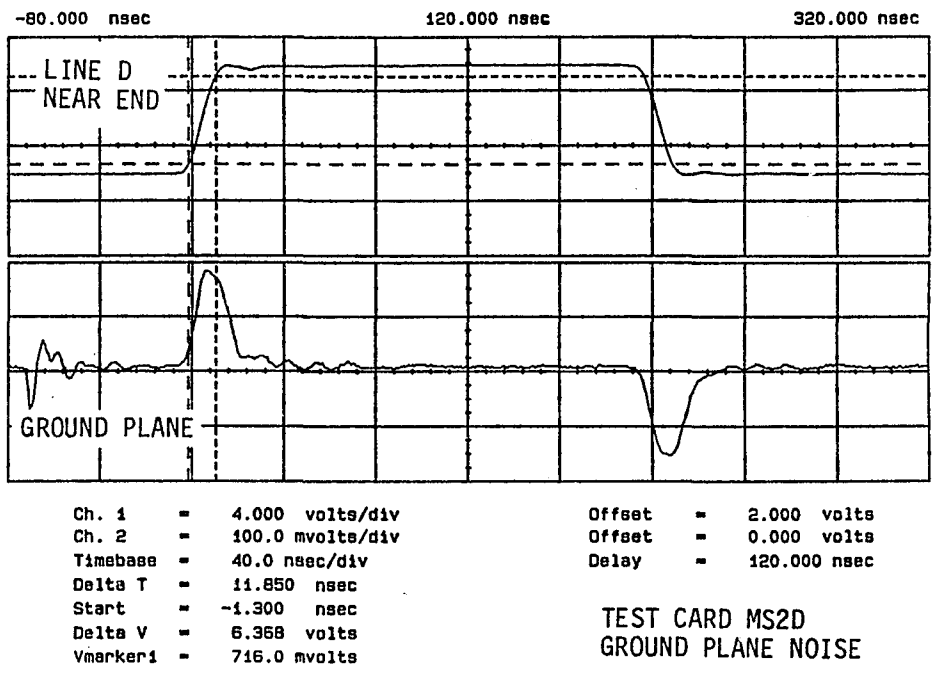


Figure 4.15 Ground Plane Noise on a Multilayer Card (Low Impedance Test Circuit)

LCR measurements described before, the multilayer test cards were plagued by both capacitive and conductive coupling.

In figure 4.2, it was shown that the multilayer microstrip cards had as much as 40 pf/in of shunt capacitance to ground. For a three-inch conductor, such as D on card MS2D, that equals 120 pf. With the 4.33×10^8 V/s signal change of the stimulating pulse, 52 mA of current is transferred from the conductor to ground. Parasitic inductance and resistance in the ground plane and braided wire strap allow the thick film ground voltage to rise above the voltage reference of the test circuit. Noise pulses are then transmitted throughout the test card on the ground plane and coupled back up to the conductor lines through their shunt capacitance. This problem is not merely peculiar to this test circuit, but is a real problem in multilayer hybrid circuits. When one considers that the ground connections in a hybrid are made by wire bonds and vias to the ground plane, it is easy to see how a coupled noise problem could arise.

With the high impedance circuit, conductive coupling continued to be a problem. The stimulating pulse and crosstalk for the high impedance multilayer circuit are shown in figure 4.16. With the large terminating resistance and shunt capacitance of the multilayer lines, the edge speeds of the stimulating pulse were slowed greatly.

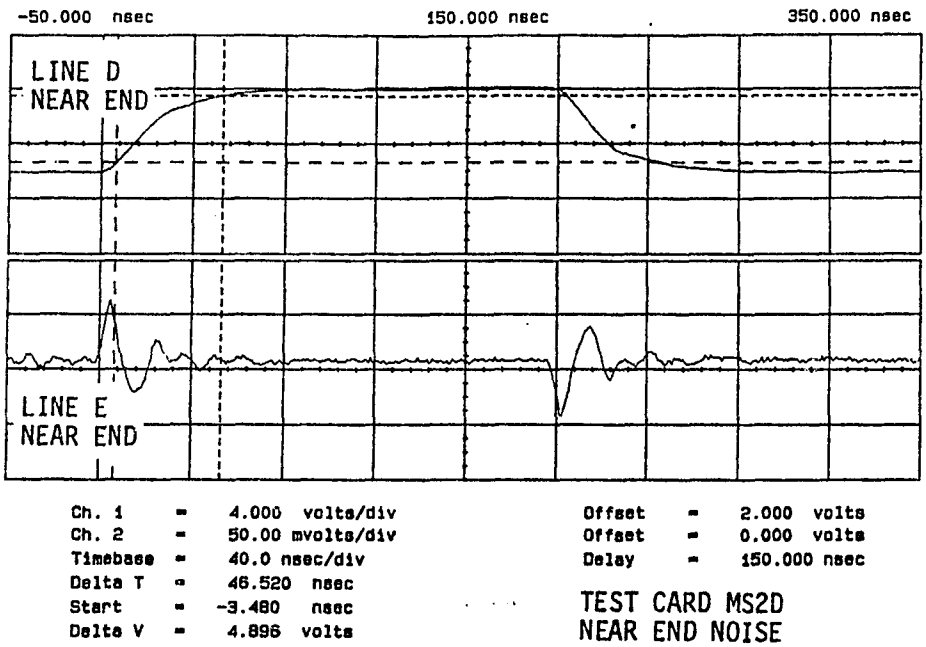


Figure 4.16 Near End Crosstalk on a Multilayer Card (High Impedance Test Circuit)

The 8161 generator was set to transmit an 8-volt pulse with 6 ns rise and fall times; yet notice the line slowed the rise time to 46.5 ns. Still, this was enough to produce a 60 mV pulse on line E. Again, conductive coupling was predominant. Figure 4.17 shows 75 mV of noise recorded on the thick film ground plane when referenced to the copper clad board.

The presence of conductive coupling complicates the crosstalk model tremendously. After analyzing a number of oscilloscope plots, it became apparent that the amount of cross channel coupling was dependent on the length of each of the parallel conductors rather than the distance that separated them. It would be futile to try to back out coupled capacitance and mutual inductance values from the multilayer plots. At best, a crosstalk noise ratio per unit length can be obtained as a function of the signal rise time. Figures 4.18 thru 4.20 show coupled noise ratios for the single layer microstrip, the multilayer microstrip, and the stripline. For each of these curves, a 6.3 V pulse was placed on the active line and the noise was measured on the parallel line 8 mils away. The signal rise time was varied and the noise amplitude was measured for each setting. The amplitude of the noise pulse was then divided by the amplitude of the stimulating pulse to determine the noise ratio. Each plot consists of two curves. One is the worst case, where a low impedance line stimulates a high impedance

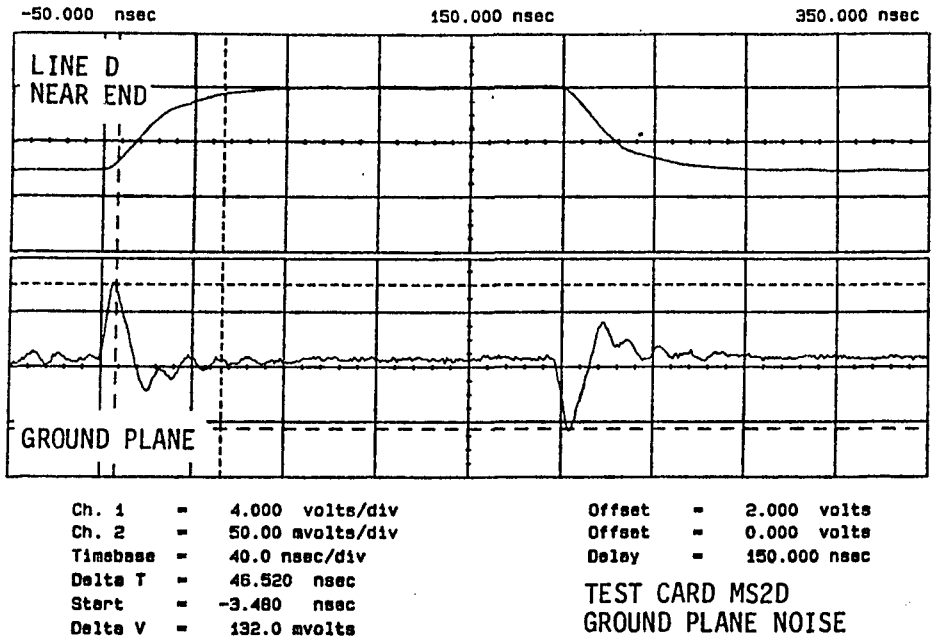
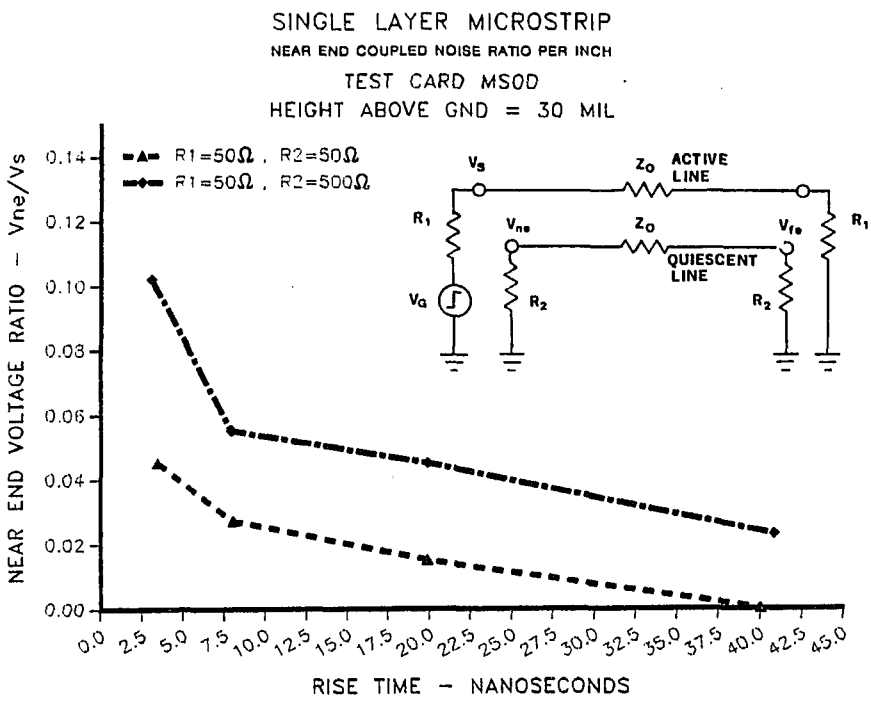


Figure 4.17 Ground Plane Noise on a Multilayer Card (High Impedance Test Circuit)



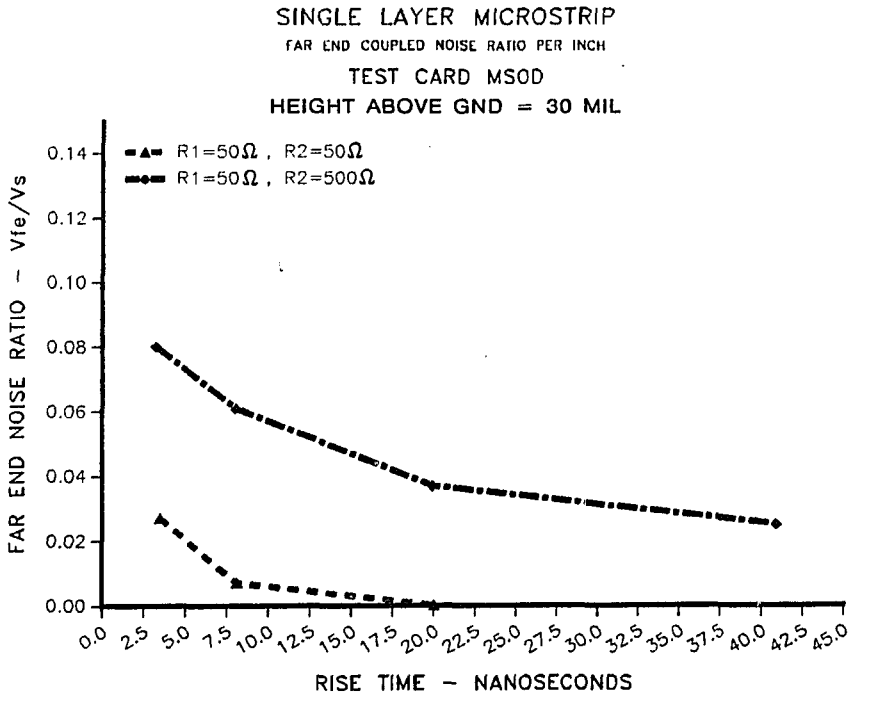
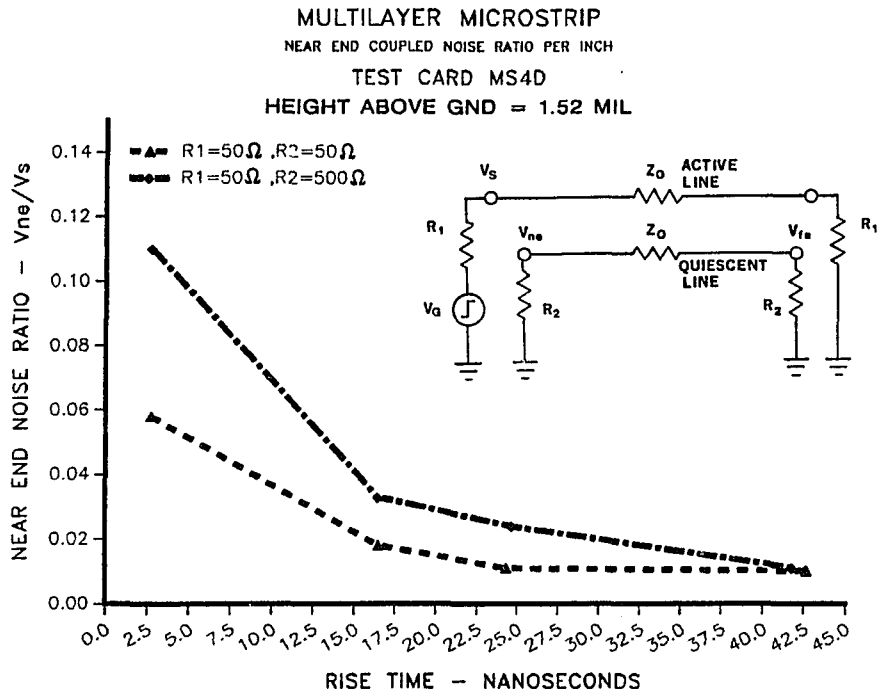


Figure 4.18 Single Layer Microstrip Coupled Noise Ratio vs. Signal Rise Time



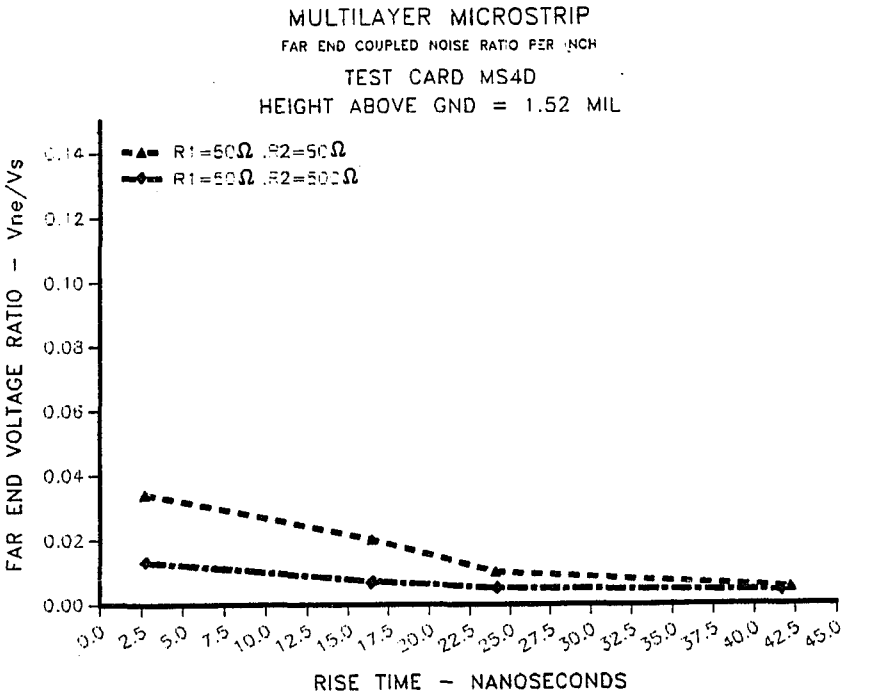


Figure 4.19 Multilayer Microstrip Coupled Noise Ratio vs. Signal Rise Time

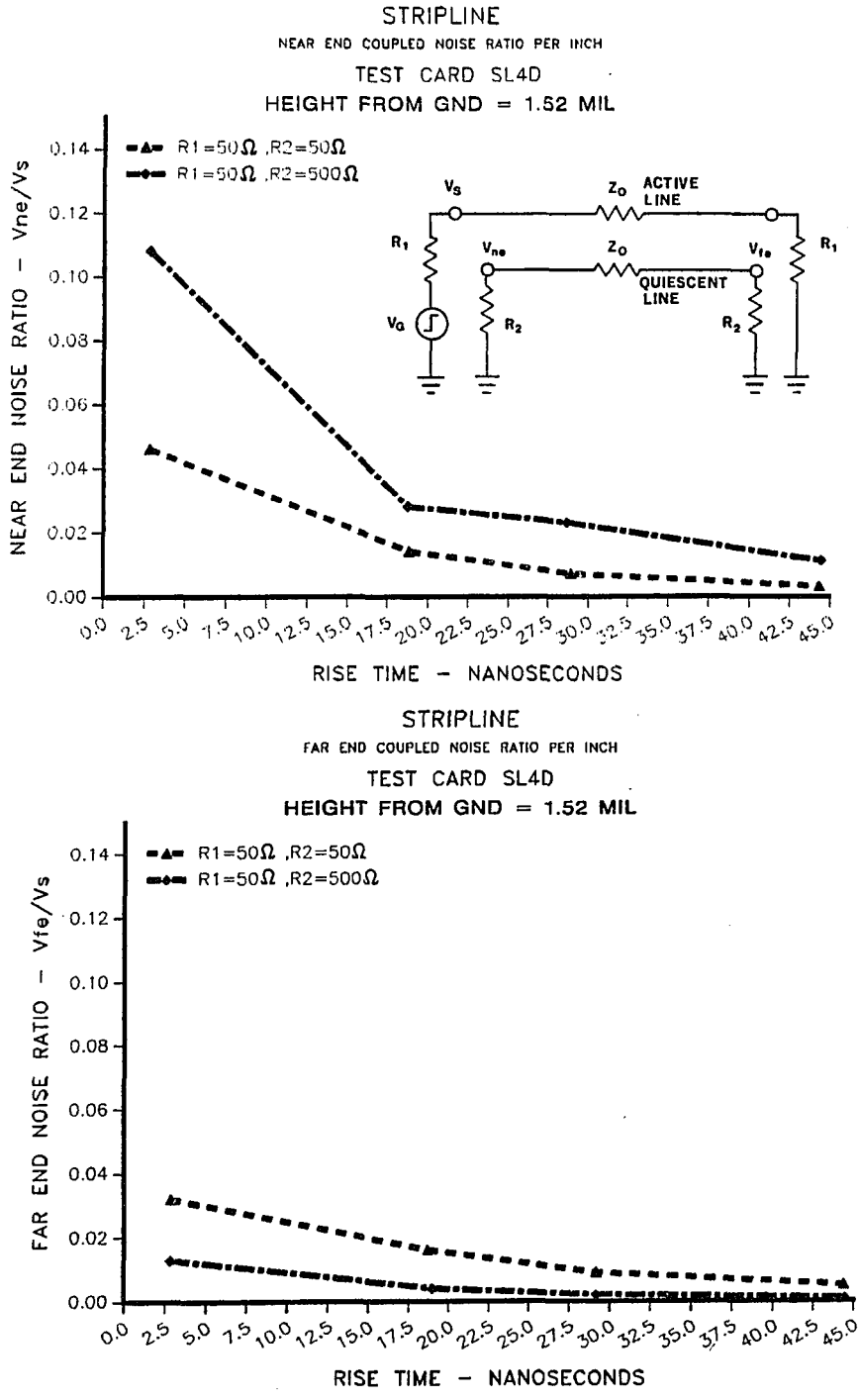


Figure 4.20 Stripline Coupled Noise Ratio vs. Signal Rise Time

quiescent line. The other represents the interaction between two low impedance lines. Considering the line terminations and characteristic impedances, approximately 50 mA of current was switching on the active line of the single layer microstrip while about 90 mA was present on the active lines of the multilayer test cards. The larger currents on the active line of the multilayer cards explains why the near end noise on the multilayers is generally larger than that of the single layer while the far end noise is generally lower. As indicated by equations 2.7 and 2.8, there is evidence of the capacitive noise component adding to the inductive component at the near end and cancelling with the inductive component at the far end. Based on layout geometries, rise times and signal levels, the noise ratios can be used to predict noise levels in a hybrid circuit. Estimated noise levels for the popular logic families are presented in the next section along with a list of guidelines for low noise design.

CHAPTER 5

CONCLUSIONS

5.1 Summary of Results

This thesis research has demonstrated the difficulties imposed by noise coupling in the design of high speed thick film circuits. The higher dielectric constant of the insulating layers and the higher circuit densities introduce large parasitic capacitances to the design. Moreover, parasitic resistance and inductance make it difficult to achieve good ground returns. These factors, coupled with the ever-faster speeds of modern digital circuits, present numerous obstacles for the hybrid designer. Understanding the noise coupling mechanism is necessary for producing a successful design.

One significant outcome of the study was the applicability of lossless transmission line theory to characterize electrical properties of the thick film networks. Transmission parameter equations successfully predicted the line capacitance measurements summarized in figures 4.2 and 4.3. From these measurements, it is evident that stray capacitance is greater on multilayer substrates than on single layers. Also, the correlation between the data and the predicted values demonstrated the usefulness of the

transmission parameter equations in characterizing a substrate's electrical properties. It is reasonable to assume that the equations for line inductance and characteristic impedance provide comparable accuracy. In addition, a coupled noise model was presented. Equations 4.7 and 4.8 were used to analyze actual near and far end crosstalk measurements. These equations were also used to extract values for coupled capacitance and mutual inductance from crosstalk measurements on the single layer test cards. The capacitance values agreed with measurements taken with a precision capacitance meter. The inductance values were large, but could not be measured directly. However, inductive coupling was shown to be predominant in the low impedance measurements.

Conductive coupling within the test card proved to be an unavoidable hindrance in the multilayer measurements. This problem is also believed to be a major source of noise in multilayer hybrid circuits. The parasitic capacitance of the thin dielectric layers provides a low impedance path to ground and allows coupling of excessive signal currents from the interconnects onto the ground plane. These currents then modulate the ground reference and distribute signal noise throughout the substrate.

Coupled noise ratios were presented as a function of signal rise times. Multilayer circuits showed slightly more signal coupling at the near end when the rise times

were below 10 ns. This is attributed to a combination of conductive and inductive coupling, whereas conductive coupling was essentially nonexistent on the single layer cards due to the low shunt capacitance to the ground plane. There is still some difficulty in applying these measurements to an actual design problem since each circuit will have unique line terminations, signal levels, and current driving abilities. However, an approximate noise voltage can be determined for two parallel lines, one inch long and 10 mils apart, terminated with digital devices and with the output of the quiescent line at the near end output of the active line. Estimated noise voltages are listed in table 5.1. These values are based on signal levels, signal rise times and device impedances. They should be useful in predicting noise levels in a new design. Of course, these values should be scaled accordingly for longer or shorter line lengths. The same is true for wider line spacings. Of the devices listed, the Fast CMOS logic will produce the highest noise voltages, due to the relatively large signal swings. Yet, CMOS logic also features the highest noise margins and is the least affected by coupled noise. In comparison, the ECL 100K devices are the most sensitive, due to their fast rise times and low noise margins. Future work should be directed towards measuring the near and far end voltages generated by the various digital circuits.

Table 5.1 Estimated Crosstalk Noise Voltages for Popular Digital Logic Families

Device Type	Single Layer Substrate Crosstalk Noise		Multilayer Substrate Crosstalk Noise	
	Near End	Far End	Near End	Far End
TTL	80 mV/in	45 mV/in	100 mV/in	60 mV/in
Schottky TTL	100	70	125	75
Fast CMOS	120	55	160	105
ECL 10K	40	30	45	25
ECL 100K	45	40	50	30

5.2 Design Guidelines

The key to minimizing coupled noise is a well-designed substrate layout. Based on the measurements described in chapter 4, the following guidelines are presented for the design of high speed digital circuits:

1. Avoid multilayer substrate designs unless they are absolutely necessary. Often a multilayer design is chosen because it simplifies the manual or CAD autorouting task. If necessary, thick film and wire bond crossovers may be used to interconnect some of the power, ground and signal lines of lesser sensitivity. In figure 4.2, it was shown that stray capacitance on a single layer microstrip

is an order of magnitude lower than values measured on the multilayer designs. Edge to edge capacitance between two conductors on a single layer is almost half as much as that found between buried conductors. Furthermore, the single layer circuit is not subject to the conductive coupling problem encountered on the multilayer test cards.

2. Minimize line lengths and maximize line spacing. This precaution will obviously reduce coupled noise in both single and multilayer designs. Often, thick film circuits are designed with 10 mil line widths and 10 mil line spacings. This limit is imposed by the thick film screening process. In a circuit with clock signals above 10 MHz, greater line spacing should be used, regardless of what the thick film process allows. Moreover, line spacing should be maximized for buried conductors on different layers. Contrary to guideline 1, line spacing can sometimes be increased by using a multilayer substrate, although the advantages must be judged by the designer. Coupling within the buried layers is increased by the dielectric material. It is best for lines on alternate layers to cross perpendicularly. Spacing between lines on buried layers should be maximized. To minimize line lengths, device placement is critical. Devices connected to

the hybrid I/O pins should be placed at the edge of the package. The length of clock and sensitive signal lines should be kept the shortest. When CAD autorouting is used for the design, the designer should carefully review the computer's circuit placement and make modifications as necessary. The computer's task is to rout all of the connections in a given wire list. Current CAD software has no considerations for line lengths, line spacing, and which signal lines are placed next to one another. The designer can often minimize the stray effects by judicious routing of a few key interconnects.

3. Minimize resistance and inductance in the ground lines. As in the case of the multilayer test cards, it is difficult to obtain an absolute ground reference on a thick film ground plane because the large line capacitance provides a low impedance path to ground for switching currents from the signal lines. These currents subsequently modulate stray impedances in the ground lines. In a digital circuit, this problem is compounded by current spikes (emitted from the device power and ground pins) residing on the power and ground lines. To minimize conductive coupling, parasitics in the power and ground lines must be reduced by several techniques. For example, it is advantageous to

have many ground pins come off the substrate at regular intervals so that all of the parasitic impedances will be in parallel. Double wires may also be used between the header and substrate. For multilayers, it is best to minimize the number of layers so that less vias are required. Paired vias may be used on power and ground lines.

In principle, crosstalk noise is generally reduced by adding ground planes to the substrate layout in order to minimize field interactions between parallel conductors. However, for multilayer thick film structures, ground planes are useless and even a source of more noise if the parasitics are great enough to cause the ground reference to rise and be modulated. It is questionable whether a reliable ground can be achieved in a high speed thick film circuit. An alternative would be to use 30 mil wide lines for power and ground connections. This approach would greatly reduce the coupled capacitance between the signal and ground lines and decrease the amount of switching currents flowing on the ground lines. Concurrently, power and ground lines can be routed on alternate layers and atop one another. The large coupling capacitance between layers can actually provide noise decoupling on the power supply lines.

Another approach is to use gridded power and ground planes; for example, 15 mil lines spaced on 50 mil centers or 10 mil lines spaced on 30 mil centers. Either configuration will decrease the shunt capacitance between the signal lines and the ground plane by 50%.[9] Current coupling between the signal lines and ground plane is reduced. At the same time, the gridded structure provides low resistance and inductance in the ground returns. Again, where power and ground lines overlap on alternative layers, continuous sheets should be used to provide added decoupling.

4. Try to keep line capacitance below 10 pf. For single layers, this should not be a problem; however, it may be difficult to achieve in a multilayer design. When laying out a multilayer circuit, the designer should first decide on a component placement and then determine the longest signal lines. The longest lines would then be placed on the upper layers, farthest from the ground plane. In addition to creating a low impedance path to ground, line capacitance also stresses the current sourcing ability of the driving circuit and adds excessive delays. For these reasons, the low impedance stripline structures are not recommended for high

speed logic designs. If required, however, gridded ground planes are advisable.

5. The top layer should be reserved for high speed clock and sensitive signal lines. Coupling into microstrip lines is less than buried lines since the effective dielectric constant is lower. Hence, the microstrips inherently have less stray capacitance than buried lines. Conversely, the lower layers should be reserved for the power and ground lines.
6. High impedance lines should not be placed next to high current, low impedance lines. Output lines should not be placed next to input lines. This will minimize inductive coupling onto the sensitive input lines. In digital circuits, every interconnect is typically terminated with both an input and an output device. As was shown in chapter 4, the far end crosstalk is much less than the near end noise. When two conductors are parallel, the low impedance outputs should be kept at the near end while the high impedance inputs belong at the far end.
7. If the material is acceptable, use a thick film paste with a low dielectric constant. Dupont 4575, for example, is a dielectric composition that

features a relative dielectric constant ranging from 6 to 7.

8. Allow for spreading of thick film conductors. Spreading is a function of the material viscosity and the screened thickness. Typically, the paste will spread 1 mil per side. If a 10 mil spacing is desired on the substrate, then 12 mil spacing should be used on the artwork.

9. Maximize the thickness of the multilayer dielectric. Dielectric thickness is controlled by the screen height and squeegee pressure. If applied too thick, spreading will occur and reduce the window size of the vias. If too thin, line capacitance can become unacceptably large. Figure 4.1 shows that a small change in dielectric thickness can change the line capacitance significantly. During production, the thickness should be carefully monitored and controlled.

APPENDIX A

LIST OF SYMBOLS

C_c	Coupled Capacitance
C_o	Line Capacitance
ϵ_o	Dielectric Constant of Free Space
ϵ_r	Relative Dielectric Constant
ϵ_{re}	Effective Dielectric Constant
F	Farads
G	Conductance
H	Henries
h	Height
I_s	Source Current
I_{he}	Near End Current
I_{fe}	Far End Current
L_m	Mutual Inductance
L_o	Series Inductance
m	Milli (10^{-3})
KHz	Kilohertz
MHz	Megahertz
ρ_s	Sheet Resistance
R	Resistance
s	Separation
t_f	Fall Time
t_r	Rise Time
μ_o	Permissivity of Free Space
μ	Micro (10^{-6})
V_G	Generator Voltage
V_S	Source Voltage
V_{ne}	Near End Voltage
V_{fe}	Far End Voltage
w	Width
w/h	Width to Height Ratio
Z_{iH}	Input Impedance, Logic State 1
Z_{iL}	Input Impedance, Logic State 0
Z_o	Characteristic Impedance
Z_{oH}	Output Impedance, Logic State 1
Z_{oL}	Output Impedance, Logic State 0
□	Square
Ω	Ohms

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