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Analysis domain truncation of interconnections in multilayer packaging structures

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ANALYSIS DOMAIN TRUNCATION OF INTERCONNECTIONS IN MULTILAYER PACKAGING STRUCTURES

by

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STATEMENT BY AUTHOR

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ABSTRACT

Interconnect lines, which connect components on a chip, can exhibit transmission line properties. Several factors like decrease in size of components, and decrease in spacing between interconnect lines, have contributed to the increase in importance of interconnect lines. A circuit-analysis approach that does not include the effect of these lines may be useless for highly dense chips. The presence of an active line does not require the analysis of all the other lines in a transmission-line system. In this thesis, a numerical experimental approach based on several industry-typical geometries is used to discuss analysis domain truncation of parallel conductors lying on a horizontal plane. It is found that " The maximum analysis domain between parallel conductors lying on a horizontal plane can be deduced from the analysis of the case of several similar, and parallel conductors of smallest possible width lying on a horizontal plane." UAC (University of Arizona Capacitance Calculator) is used as the TEM parameter extractor, while UACSL (University of Arizona Coupled Line Simulator With Linear Terminations) is used to calculate the voltages on the transmission lines.

CHAPTER 1

INTRODUCTION

In the last decade and a half, the size of components has fallen so dramatically that the size of interconnect lines, which was earlier inconsequential, has become relatively large [1]. The switching times of gates have reduced so drastically that the propagation delay of signals through interconnect lines has become significant. Reduction in size has led to higher integration, which has brought its own particular problems. Interconnect lines can severely affect the voltage levels on each other due to their proximity — at times they are seperated by no more than a micron or two. Relatively simple electrical analysis has given way to CAD tools which are able to take coupling affects into account when analyzing complex, highly integrated circuits. Any electrical analysis which does not consider the coupling between these lines may be useless.

A lumped circuit model represents the parisitic characteristics of a transmission system as lumped circuit elements like resistors, capacitors, and inductors. This model is valid if the length of line for which coupling is of interest is a few centimeters, and the highest frequency corresponds to a wavelength bigger than the physical dimension of the system [1]. The lumped-circuit model does not have to be complex all the time. In a low-speed digital system, since interconnect capacitance has high reactance and interconnect inductance is almost like a short-circuit, a simple analysis using few key resistors, capacitors, and inductors may suffice. A complex model may be required though for a high-speed system. Usually, a parameter calculator is used to first calculate circuit parameters like inductance, resistance, and capacitance. In most applications, if the length is

much greater than the cross-section, the problem can be approximated by a two-dimensional computation. Subsequently, a transmission line simulator is fed these circuit parameters to output voltages at desired points on transmission lines.

It is very common to have several interconnect lines lying next to each other on today's highly dense chips. Signal propagation through any wire may induce crosstalk, which is the unwanted coupling of a signal from a signal-carrying wire to another line. Chapter 2 deals with the theory behind UAC, the TEM Parameter Calculator. Chapter 3 outlines the theory behind UACSL, the Transmission Line Simulator utilized. Despite having an array of tools of the types described in Chapters 2 and 3, a designer may not want to calculate the crosstalk for all the lines lying in the vicinity of an active line. At present, there are very few papers dealing with Analysis Domain Truncation. This is probably because of the extremely large number of cases possible, and a perception that if a set of rules were developed, they would be severely limited to a small number of cases. Nonetheless, an attempt has been made to discover a set of rules which will allow Analysis Domain Truncation. Some results of the simulation results are presented in Chapter 4 and a theory formulated on their basis.

Several of the assumptions are imposed by the tools. UAC assumes that the dielectric media is infinite in extent, and lines have uniform cross-section. Also, UAC assumes that the lines have infinite length, and therefore, end effects are not considered. UACSL assumes TEM propogation through lossless lines, and only linear termination networks. In addition, several assumptions are made by the author. Lines are assumed to be rectangular in shape; only one active conductor is assumed to exist; regardless of duration, highest voltage level is considered; and minimum allowed width of a conductor is assumed to be one micron.

CHAPTER 2

TEM PARAMETER CALCULATORS

2.1 Introduction

Interconnect noise is defined as extraneous voltage on a line due to crosstalk and reflections [3]. Crosstalk is the unwanted coupling of a signal from a signal-carrying wire to another line. This coupling is caused primarily because of mutual inductance and capacitance between interconnect lines lying close to each other. There are several techniques for calculating self and mutual parameters. Analytical techniques like conformal mapping can be used for simple configurations, but a multilayered dielectric medium requires numerical solutions [4]. As the conductors are assumed to be uniform along their length, the problem is one of solving Laplace's equation in two dimensions. Some of the numerical techniques utilized are Semianalytic Green's Function Method (GFM), Method of Moments (MOM), Finite Difference Method (FDM), Variational Method (VM), and Spectral Domain Method (SDM). Two of the more popular parameter calculators at the University of Arizona are based on the first two methods.

There are several advantages and disadvantages to both UAC (GFM based parameter calculator), and MOM (MOM based parameter calculator). Semianalytic Green's function approach to configurations containing more than two dielectric layers is extremely complicated and computationally expensive. Though Method of Moments is faster and can handle arbitrary number of dielectric layers, both the transverse width of layers and the length of the upper ground plane have to be considered as finite. Transverse lengths can be considered as infinite in the

GFM approach. Section 2.2 uses some of the published results from [4,5,6] to explain some relationships between electrical and physical parameters. Section 2.3 briefly describes the theory behind Semianalytic Green's function Method. Section 2.4 briefly describes the capabilities and limitations of UAC, the TEM parameter calculator utilized.

2.2 Some Relationships Between Electrical and Physical Parameters

Most of the relationships presented in this section are conclusions based on results presented in [4,5,6]. Consider Figure 2-1 in which two identical conductors of thickness t, and width W are seperated by a distance s. They are placed a distance h above the ground plane. A dielectric interface, which separates air from a material with a dielectric constant of ϵ_{r2}, is at a height H above the infinite ground plane. C_s, L_s, C_m, and L_m are the four electrical parameters considered here. While C_s and L_s are defined as line-to-ground capacitance and line-to-ground inductance, C_m and L_m are described as line-to-line capacitance and line-to-line inductance.

Critical depth of bury h_c is defined as the height above which the conductors start coupling with the polarization charge on the dielectric surface and below which they act as if they are in an infinite dielectric. A conductor acts very much like a parallel plate capacitor when W/h is large. In fact, C_s is directly proportional to W/h. If no field lines penetrate the surface, C_s/ϵ_{r2} does not depend on ϵ_{r2}. Such a case happens when the line is deeply buried i.e $h < h_c$ and W is quite small. Note that if W is made too large, much of the electric field is trapped above the conductor, resulting in field lines penetrating the surface. Of course, C_s/ϵ_{r2} is greater for the larger value of w. But as h is increased, the conductor gets closer and closer to the surface, resulting in a significant drop in C_s/ϵ_{r2}. Also, C_s/ϵ_{r2} starts increasing as s is decreased.

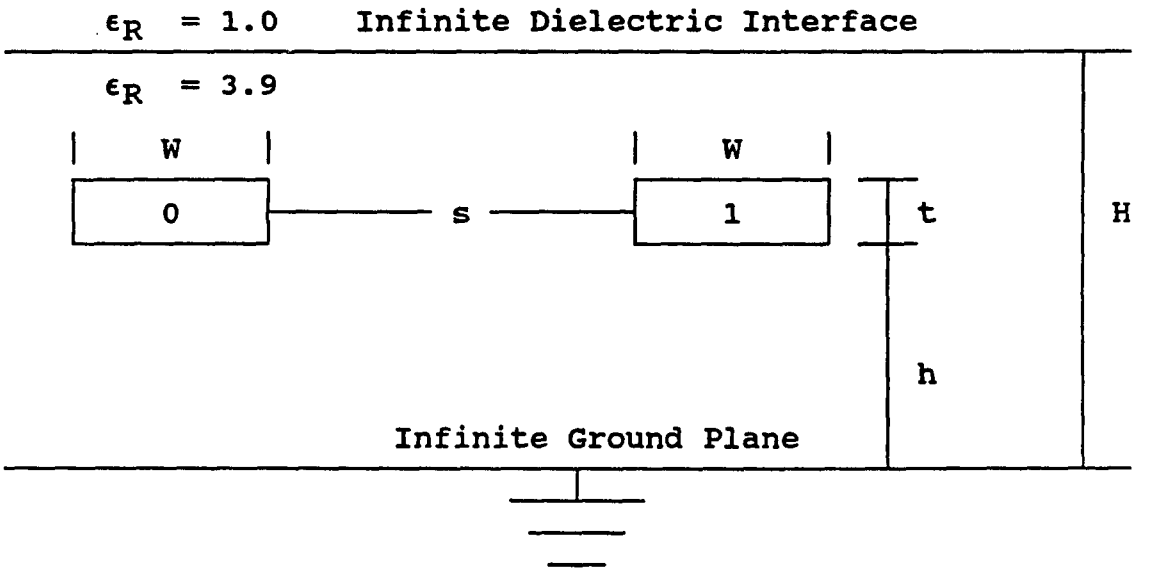


Figure 2-1. Buried Microstrip Line Geometry.

Crosstalk is a complex function of the parameters under discussion, but it can be safely said that it is directly proportional to C_{12}. Unless the conductor is far from surface and its width is comparatively small, C_{12}/ϵ_{r2} is dependent on ϵ_{r2}. In fact, C_{12}/ϵ_{r2} seems to increase with smaller ϵ_{r2}. C_{12}/ϵ_{r2} increases as s is decreased because more and more interline field lines terminate on one another. Also C_{12}/ϵ_{r2} increases until $h = h_c$, and thereafter decreases. This phenomena is explained by the fact that until $h = h_c$, the conductor behaves as if it is in an infinite dielectric and most of the interline field lines terminate on each other, but as the dielectric surface is approached, more and more interline field lines reach the surface. Such a change in C_{12}/ϵ_{r2} is more dramatic for smaller widths. Note that crosstalk can be decreased by bringing a grounded conductor near the conductors but that increases the self capacitance and thus increases the propogation delay of signals. Both the self capacitance and mutual capacitance increase with thickness of the conductors t, resulting in greater crosstalk. It should be noted that reducing thickness does lower mutual capacitance, but the resistance per unit length increases too. It should also be noted that reduction in line width does not necessarily result in a great reduction in C_m as narrow lines can not really be treated as parallel-plate capacitors.

The inductance matrix $[L]$ is related to the capacitance matrix $[C_0]$, which would be obtained if all the dielectric is replaced by free space, by the following equation

$$[L] = \frac{[C_0]^{-1}}{\epsilon_0 \mu_0}.$$

Self-inductance L_s is almost independent of s — at very low values of s it decreases slightly. L_s increases nonlinearly with h when h is very small, but the relationship becomes quite linear thereafter. Both self-inductance and mutual-inductance are greater for smaller widths. Also mutual inductance L_m decreases rapidly with increase in s.

2.3 Semianalytic Green's Function Method (GFM)

Weeks is responsible for advancing the theory for this method [2]. The calculation of interconnect parameters involves solution of Laplace's equation in unbounded regions containing multilayer dielectrics, ground planes, and multiconductor striplines. As pointed out by Weeks in his paper, there are several methods of solving Laplace's equation in two dimensions. The method suggested by him is a refinement of the the subareas method, in which he assumes piecewise linear charge density over the surfaces of the conductors.

Only one of three possible configurations allowed by UAC is used. Please see Figure 2-2. The cross section of the conductors, lying in two layers of dielectrics, should be such that it can be approximated by a polygon. Ground is assumed to be at height H = 0. Let Q_i be the charge per unit length on the ith conductor, and V_j be the potential difference between line j and ground. If M number of conductors are considered, the relationship between the charge per unit length on the ith conductor as a result of applying a voltage to the jth conductor is given by

$$Q_i = \sum_{j=1}^{M} C_{ij} V_j$$

where $(i = 1..M)$. The constants C_{ij}, which denote the capacitance per unit length, form a symmetric matrix such that

$$C_{ij} = C_{ji}.$$

The C_{ij} constants are calculated by reducing the problem to the two-terminal capacitor case. One of the plates consists of the "active" conductors — 1V being applied to them, and the other consists of grounded "inactive" conductors. The two-terminal capacitance is calculated by

$$C_{2T}^{A} = \sum_{i \epsilon A} Q_i$$

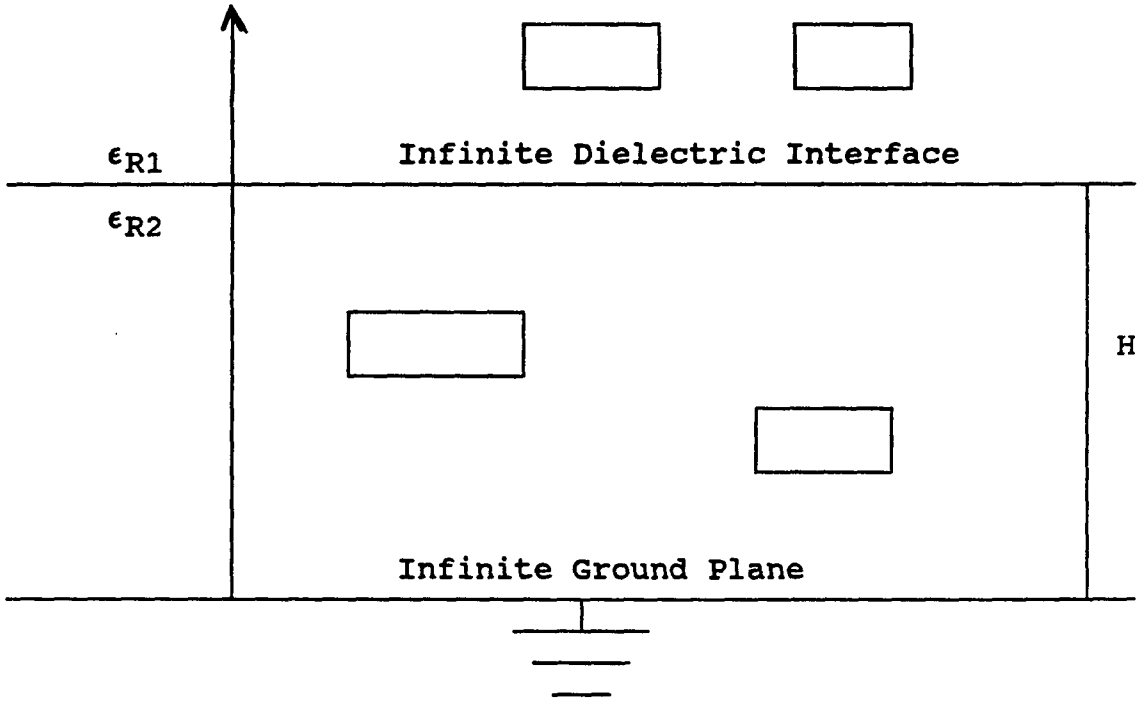


Figure 2-2. Case II of UAC.

where A is the set of active conductors. According to Weeks,

$$C_{ii} = C_{2T}{}^{(i)}$$

$$C_{ij,i\neq j} = \frac{1}{2}(C_{2T}^{(i,j)} - C_{2T}^{(i)} - C_{2T}^{(j)})$$

$C_{2T}^{(i)}$ equals the charge on the ith conductor when i is the only active conductor; similarly, $C_{2T}^{(j)}$ equals the charge on the jth conductor when j is the only active conductor; and, $C_{2T}^{(i,j)}$ is the sum of the charges on the ith and the jth conductor when they are the only active conductors.

As mentioned above, computation of the two-terminal capacitance requires a knowledge of the charge (or the charge-density) per unit length on the conductors. The charge density per unit length on the conductor surfaces can be calculated by numerically solving an integral equation which connects the surface charge density on the surface to the known potentials on the conductor surfaces. Consider Figure 2-3 in which a line carrying unit charge per unit length passes through a point (x_c, y_c). Let the symbol used to denote the potential at (x, y) due to the line charge at (x_c, y_c) be

$$G(x, y|x_c, y_c)$$

Considering Figure 2-2 again, let $\omega(x_c, y_c)$ be the surface charge density on the surface of the active conductor. If l is the arc length of the conductor,

$$x_c = x_i(l)$$

$$y_c = y_i(l)$$

where i is the active conductor. According to Weeks, the potential $\phi(x, y)$ at any point (x, y) is given by

$$\phi(x, y) = \phi_0 + \sum_{i=0}^{M} \oint_i G(x, y|x_i(l), y_i(l))\omega(x_i(l), y_i(l))dl$$

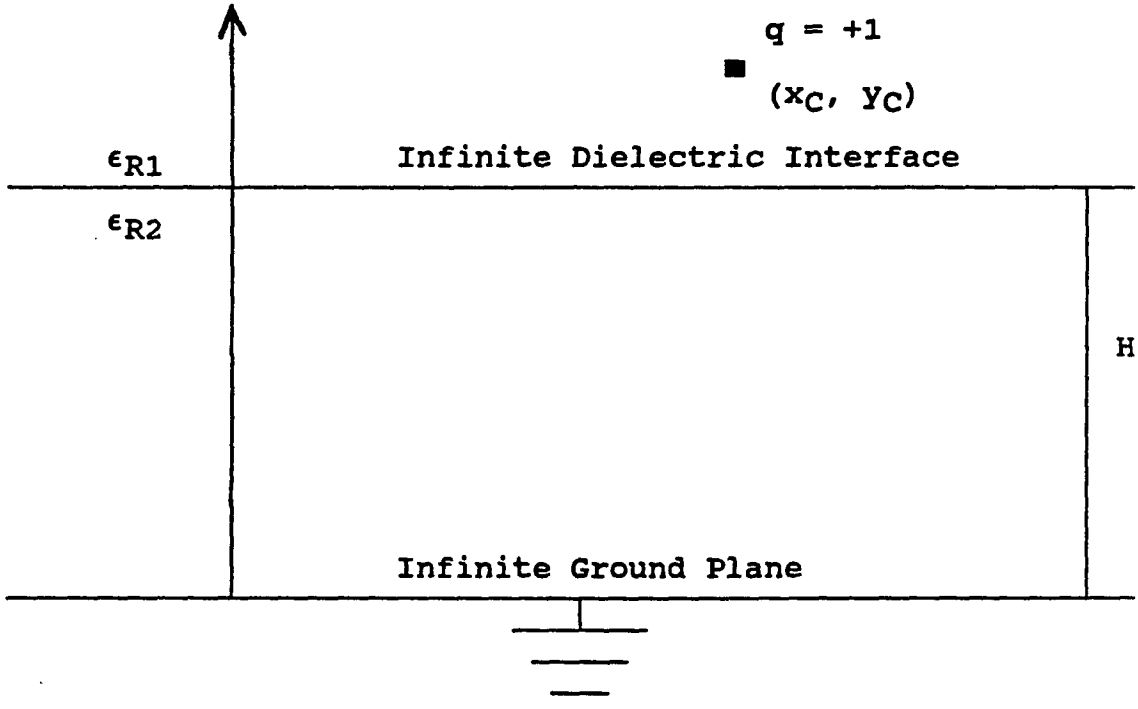


Figure 2-3. Line carrying unit charge.

where ϕ_0 is a constant, and $\phi(x, y)$ are known potentials on the surfaces of the conductors.

$G(x, y|x_i(l), y_i(l))$ has been calculated by Weeks based on the boundary conditions. Weeks outlines a numerical technique to solve the above equation for $\omega(x_i(l), y_i(l))$, the surface charge densities. Once the surface charge densities on the active conductors are known, the two-terminal capacitance can be calculated and the capacitance matrix created.

2.4 UAC

University of Arizona Capacitance Calculator (UAC) is based on the Semi-analytic Green's Function Method. It is a two-dimensional program. It is based on several assumptions. First, lines are assumed to be of infinite length. Second, the end effects are not calculated. Third, the dielectric media is taken as infinite in extent. It allows only two dielectrics and three generic geometries. The geometry shown in Figure 2-2b is used by the author for all the tests. A requirement is also placed that each conductor must lie wholly within one dielectric medium. Each side is divided into subintervals - the number of subintervals being specified by the user. The subintervals are further divided into subdivisions, which are not under user's control. The accuracy of the matrix values produced by UAC is proportional to the number of subintervals. The diagonal terms converge faster than the off-diagonal terms. According to the manual [7], several values for the subintervals should be taken so as to let the off-diagonal terms converge. Of course, CPU time increases drastically with the number of subintervals. Several software-based limits which can be changed quite easily are nevertheless mentioned. First, the maximum number of conductors is ten, second the maximum number of sides per conductor is sixteen, and third the total number of subintervals can not exceed two hundred.

CHAPTER 3

TRANSMISSION LINE SIMULATOR

3.1 Introduction

As the speed of digital circuits has increased, the rise and the fall times have decreased drastically. Consequently, the delay of signals propagating through interconnects has assumed such a significance that these interconnects have to be now considered as transmission lines. An attempt at the reduction of the propagation delay has resulted in greater density and therefore designers have to consider crosstalk between these on-chip lines. Also, improper termination of lines, right angle bends in signal conductors, and via connections among layers can introduce reflections. This problem of stray pickup becomes acute especially in ECL circuits, which have a much lower noise margin and run at greater speeds than either TTL or CMOS. In this chapter the author discusses first the properties of transmission lines and the various methods of analyzing their behavior; and second, the capabilities and limitations of UACSL, the transmission line simulator utilized.

3.2 Properties of Transmission Lines

A transmission line can be described as a device for guiding energy from one point to another. There are special properties associated with transmission lines and not all interconnects have to be considered as transmission lines. Consider Figure 3-1 in which a line of length, l, is shown. Let a signal with rise time, t_r,

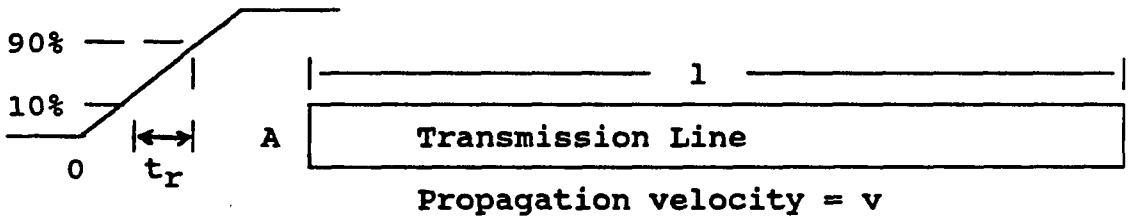


Figure 3-1. Signal with rise time, t_r, and propagation velocity, v, is applied to point A on the line. The above line will exhibit transmission-line properties if t_r is less than 21/v.

and propagation velocity, v, be applied to point A on the line. This line can be considered as a transmission line if

$$t_r \leq \frac{2l}{v}. \qquad (3-1)$$

Transmission lines can be divided into two groups — those with transverse electromagnetic (TEM) waves, and those with higher order modes. In a TEM propagation, the electric and the magnetic field are entirely transverse to the direction of propagation. In higher order modes, either electric, or magnetic, or both, may have components in the direction of transmission.

If the dielectric in which the interconnect is buried is homogeneous and the conductors are lossless, the dominant mode of propagation is TEM. But, since real lines have losses and are not buried in homogeneous mediums, waves that propagate along a line are not TEM. Also, bends, crossovers, and discontinuities can produce non-TEM modes. As TEM case is quite easy to analyze, TEM mode of propagation is often assumed. Such an assumption is quite valid if the maximum cross-sectional distances are very small compared to the wavelength of the highest frequency. Let the direction of propagation be in the z direction, electric field E_y in the y direction, and the magnetic field H_x in the x direction. It can be shown from Maxwell's equations [8] that the equation which describes TEM propagation through a lossless line is

$$\frac{\partial^2 E_y}{\partial t^2} = \frac{1}{\mu\epsilon}\frac{\partial^2 E_y}{\partial x^2} \qquad (3-2)$$

where μ is permeability of the medium, ϵ is permittivity of the medium. The propagation velociy is given by

$$velocity = \frac{1}{\sqrt{\mu\epsilon}} \qquad (3-3)$$

The velocity of propagation in a non-magnetic material is given by

$$velocity = \frac{c}{\sqrt{\epsilon_r}} \qquad (3-4)$$

where ϵ_r is relative permittivity of the medium, and c is the velocity of light in air (c = 300 Mm/s = 12 inches/ns) [5]. The characteristic impedance of a transmission line is determined by its geometry and properties of material. If the losses are negligible, the characteristic impedance is given by

$$Z_0 = \frac{V}{I} = \sqrt{\frac{L}{C}} \qquad (3-5)$$

where L is the inductance per unit length, and C is the capacitance per unit length. Characteristic impedance does not change with line length.

3.3 Methods for Analysis of Transmission Lines

Assuming TEM propagation, a multiconductor transmission system can be described by a group of partial differential equations in the time domain or a group of ordinary differential equations in the frequency domain. As discussed in the paper by Djordjevic [9], there are several methods of solving them.

Consider Figure 3-2, in which N parallel transmission lines of length D are shown. Let x be the distance between the generator and any point on the transmission line, and let t be the time at any instant. Let

$$[v(x,t)]_N = [v_1(x,t), ..., v_N(x,t)]^T,$$

$$[i(x,t)]_N = [i_1(x,t), ..., i_N(x,t)]^T$$

where T means transpose of the matrix. Let $[R]$, $[L]$, and $[G]$ be matrices of the form

$$A = \begin{pmatrix} A_{11} & A_{12} & \dots & A_{1N} \\ A_{21} & A_{22} & \dots & A_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ A_{N1} & A_{N2} & \dots & A_{NN} \end{pmatrix}. \qquad (3-6)$$

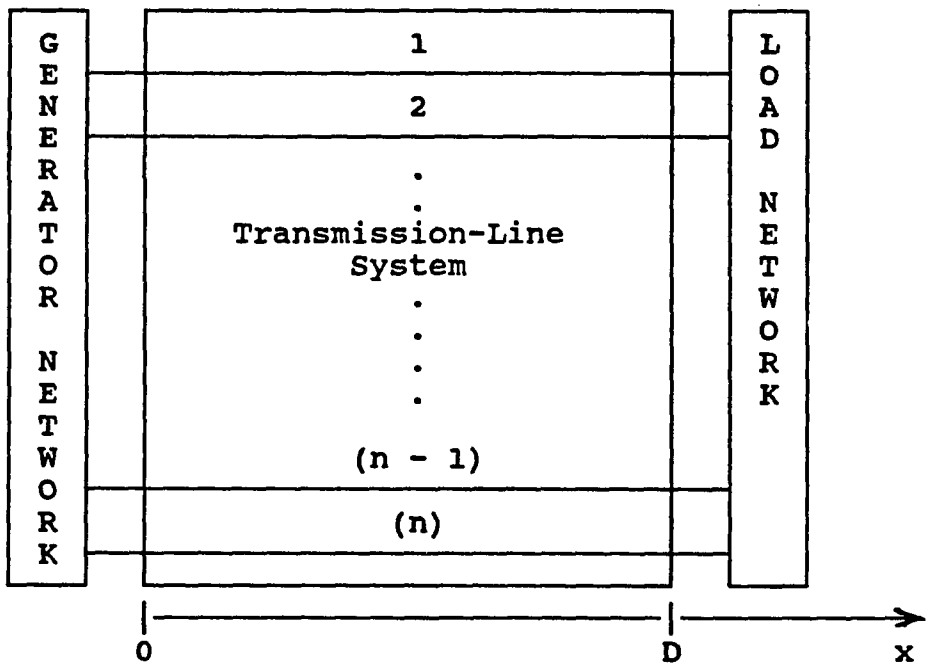


Figure 3-2. n conductor transmission-line system.

The $[R]$ matrix is defined to include effect of conductor losses, $[L]$ is defined to include the effect of electromagnetic induction, and $[G]$ is defined to include losses in dielectric. R_{ii} is self-resistance; R_{ij} is mutual-resistance, where $i \neq j$; L_{ii} is self-inductance; L_{ij} is mutual-inductance, where $i \neq j$; G_{ii} is self-conductance; and G_{ij} is mutual-conductance, where again $i \neq j$. The [C] matrix is defined to include the effect of electrostatic induction. Let it be of the form

$$[C] = \begin{pmatrix} S_1 & -C_{12} & \dots & -C_{1n} \\ -C_{21} & S_2 & \dots & -C_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{n1} & -C_{n2} & \dots & S_n \end{pmatrix}$$

where,

$$S_k = \sum_{i=1}^{n} C_{ki}.$$

C_{ii} is self-capacitance coefficient between line i and ground. C_{ij} is the mutual-capacitance coefficient between lines i and j, where $i \neq j$. The above-defined matrices [R], [G], [L], and [C] are derived from a parameter calculator of the type described in the previous chapter.

The matrices defined above are used in telegrapher equations to define the transmission system [9]. The telegrapher equations are

$$\frac{\partial[v(x,t)]}{\partial x} = -[R][i(x,t)] - [L]\frac{\partial[i(x,t)]}{\partial t} \qquad (3-7)$$

$$\frac{\partial[i(x,t)]}{\partial x} = -[G][v(x,t)] - [C]\frac{\partial[v(x,t)]}{\partial t}. \qquad (3-8)$$

In the frequency domain, the above two equations become

$$\frac{d[V(x)]}{dx} = -[R][I(x)] - jw[L][I(x)] \qquad (3-9)$$

$$\frac{d[I(x)]}{dx} = -[G][V(x)] - jw[C][V(x)]. \qquad (3-10)$$

It can be shown that for lossless lines the above equations reduce to

$$\frac{\partial^2[v(x,t)]}{\partial x^2} = [L][C]\frac{\partial^2[v(x,t)]}{\partial t^2} \qquad (3-11)$$

$$\frac{\partial^2[i(x,t)]}{\partial x^2} = [C][L]\frac{\partial^2[i(x,t)]}{\partial t^2}. \qquad (3-12)$$

There are several methods of solving the differential equations. The method used depends on the degree of accuracy desired as well as the termination networks. The Time-Stepping Method can be used for frequency-independent systems with arbitrary load terminations. Modal Analysis, which analyzes the N TEM modes for N lossless lines and linear terminations, can be done in both time and frequency domain. If nonlinear loads are used as terminations, analysis is more complicated and may be possible only in time domain. If the lines are also lossy the analysis has to be done in both time and frequency domain.

3.4 Time-domain Modal Analysis of Transmission Lines

As UACSL, the transmission line simulator used by the author, is based on modal analysis in time domain, this technique is disscussed in this section. The differential equations for a lossless line given in the previous section can be solved to give a matched termination network for the transmission line. As discussed by Amemiya [10], this matched termination network can be substituted for the transmission line and the line voltages calculated. In this section the theory behind the equations used for the matched termination network is briefly disscussed.

n lossless transmission lines can be substituted by a matched-terminal network containing $n(n+1)/2$ resistors or less in the configuration shown in Figure 3-3. In this section Equation (3-11) is solved to give the values for the resistors. A new matrix [G] (different from that in Section 2.3) is defined to be of the type in Equation (3-6), where

$$G_{kk} = \sum_{i=1}^{n} \frac{1}{R_{ki}}$$

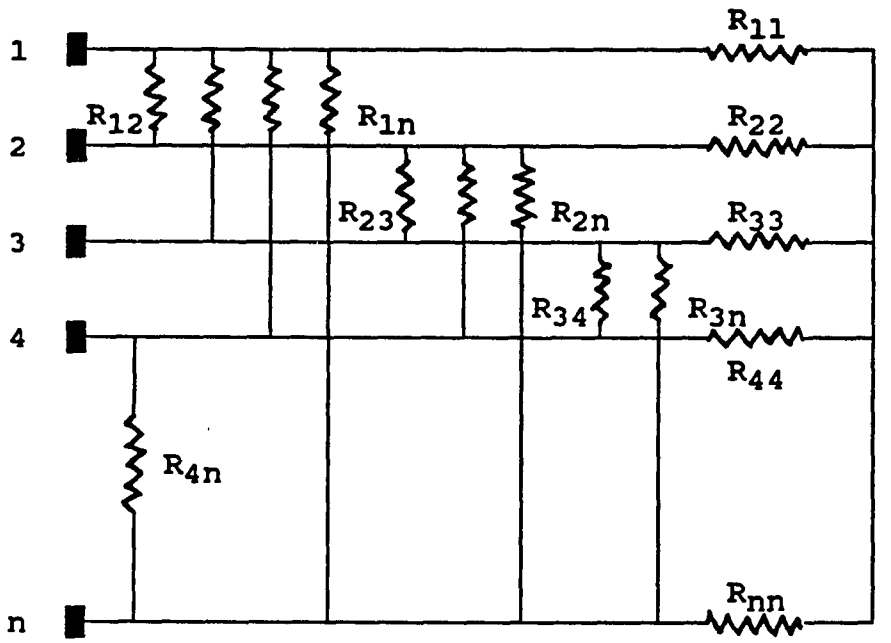


Figure 3-3. Matched termination network for lossless parallel lines. Only some of the resistors have been marked.

$$G_{jk} = -\frac{1}{R_{jk}}.$$

Equation (3-11) reduces in the frequency domain to

$$\frac{d^2V(x)}{dx^2} = -\omega^2[L][C][V(x)]. \qquad (3-13)$$

If $i = 1, .., n$ and $V_i = V_{0i}e^{j\beta x}$ (where β is known as phase constant) is taken as a solution, Equation (3-13) becomes

$$(\lambda[U] - [L][C])[V(x)] = 0 \qquad (3-14)$$

where $\lambda = \beta^2/\omega^2 = 1/v^2$, [U] is the unit matrix, and v is the propagation velocity. λ has n values (known as eigenvalues) because [L][C] is a $n * n$ matrix. It follows that there are n propagation velocities, each being associated with a propagation mode. If the medium is homogeneous, all the velocities coincide and the eigenvalues are identical. Therefore,

$$[V(x)] = exp(-j\frac{\omega}{v_0}x)[V_0] \qquad (3-15)$$

where v_0 is the common velocity. Substituting Equation (3-15) into Equation (3-9), we get

$$I[x] = -\frac{1}{j\omega}[L]^{-1}\frac{dV[x]}{dx} = \frac{1}{v_0}[L]^{-1}[V(x)]. \qquad (3-16)$$

Therefore from Equation (3-14),

$$[I(x)] = v_0[C][V(x)] = [G][V(x)]. \qquad (3-17)$$

Comparing the two matrices, [G] and [C], we get

$$R_{jk} = \frac{1}{(v_0 C_{jk})} \qquad (3-18)$$

where $j,k = 1,2,...,n$. [G] is symmetric. Let $[Z_C] = [G]^{-1}$. Then $[Z_C]$ for a homogeneous medium is given by

$$[Z_C] = \frac{1}{v_0}[C]^{-1}. \qquad (3-19)$$

$[Z_C]$ for a nonhomogeneous medium is given by [10]

$$[Z_C] = [C]^{-1}[V(x)]_m[v][V(x)]_m^{-1} = [V(x)]_m[v]^{-1}[V(x)]_m^{-1}[L] \qquad (3-20)$$

where $[V(x)]_m$ and $[v]$ are $n*n$ matrices of the form in Equation (3-6). In $[V(x)]_m$ each column represents one of the n modes and each element in each column represents the voltage on a certain line for a particular mode. The off-diagonal terms of $[v]$ are zero while each diagonal term in a particular column represents propagation velocity for a particular mode. For the purpose of calculating the voltages using $[Z_C]$, several definations are made. As shown in Figure 3-4, the generator network for a transmission line is defined as including a source resistor, R_G, and a voltage source, $V_G(t)$. Similarly, the load network includes R_L and the voltage source, $V_L(t)$. In the simple case shown in Figure 3-4, the non-diagonal terms of $[R_G]$ and $[R_L]$ are zero and the diagonal terms are source resistances. In more complicated terminal networks the off-diagonal terms will not be zero. As shown in Figure 3-4, $v_{inc}(x,t)$ is the voltage at a point x at time t due to the wave arriving from the left, while $v_{ref}(x,t)$ is the voltage due to the wave arriving from the right. For an n-line transmission-line system, $[v_{inc}(x,t)]$ and $[v_{ref}(x,t)]$ are defined as $n*1$ matrices. $[\tau_G]$, $[\rho_G]$, $[\tau_L]$, and $[\rho_L]$ are defined as $n*n$ matrices, where

$$[\tau_G] = [Z_C]([R_G] + [Z_C])^{-1} \qquad (3-21)$$

$$[\rho_G] = ([R_G] - [Z_C])([R_G] + [Z_C])^{-1} \qquad (3-22)$$

$$[\tau_L] = [Z_C]([R_L] + [Z_C])^{-1} \qquad (3-23)$$

$$[\rho_L] = ([R_L] - [Z_C])([R_L] + [Z_C])^{-1}. \qquad (3-24)$$

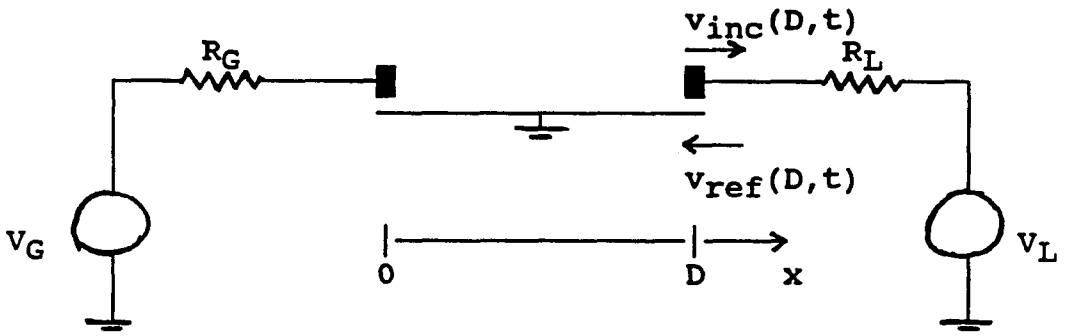


Figure 3-4. Single conductor transmission-line system.

$[\tau_G]$ is called the generator transmission coefficient, $[\rho_G]$ is the generator reflection coefficient, $[\tau_L]$ is the load transmission coefficient, and $[\rho_L]$ is the load reflection coefficient. Now, the voltage at any point x and time instant t can be defined as

$$[v(x,t)] = [v_{inc}(x,t)] + [v_{ref}(x,t)]. \qquad (3-25)$$

At point $x = 0$,

$$[v_{inc}(0,t)] = [\tau_G][V_G(t)] + [\rho_G][V_{ref}(0,t)] \qquad (3-26)$$

and at point $x = D$

$$[v_{ref}(0,t)] = [\tau_L][V_L(t)] + [\rho_L][V_{inc}(D,t)]. \qquad (3-27)$$

Note that the effect of crosstalk is included through the off-diagonal terms of the reflection coefficient and the transmission coefficient matrices.

3.5 Characteristics of UACSL

The transmission line simulator used by the author is UACSL (University of Arizona Coupled Line Simulator with Linear Terminations) [11]. UACSL is based on a paper by Djordevic [9], which outlines modal analysis in time domain for linear termination networks. Linear networks can contain resistors, capacitors, inductors, piecewise linear independent voltage sources, and lossless uniform transmission line systems.

There are several limitations in UACSL. Some of the main limitations are that the maximum number of transmission lines allowed is ten, the maximum number of nodes allowed is two hundred, and the maximum number of piecewise linear sections of each independent voltage source is ten. Thus it is not possible to study the effect of application of periodic waveform generators — maximum number of periods allowed is two-and-half. Since it is assumed that the lines are lossless, the propagation velocity is independent of the frequency, and therefore the analysis is frequency-independent.

CHAPTER 4

RESULTS OF NUMERICAL SIMULATION

4.1 Introduction

It is very common to have several interconnect lines lying next to each other on today's highly dense chips. One or more may carry a signal and may affect the voltage level on its neighbors. Despite having an array of tools of the type described in Chapters 2 and 3, a designer may not want to calculate the crosstalk for all the lines lying in the vicinity of an active line. At present, there are very few papers dealing with Analysis Domain Truncation. This is probably because of the extremely large number of cases possible, and a perception that if a set of rules were developed, they would be severely limited to a small number of cases. Nonetheless, an attempt has been made in this chapter to discover a set of rules which will allow Analysis Domain Truncation. Some results of the simulation results are presented in this chapter and a theory formulated on their basis.

The hypothesis of the author is "The maximum analysis domain between conductors lying on a horizontal plane can be deduced from the analysis of the case of several similar conductors of smallest possible width lying next to each other on a horizontal plane". The simulation results of three industry-typical geometries are presented in Sections 4.2, 4.3, and 4.4. The conductors are assumed to be buried in silicon-dioxide for all the three cases. The affect of shielding on Analysis Domain Truncation has been analyzed in Section 4.2.1.

Due to the absence of a transmission-line simulator which would analyze nonlinear termination networks, resistors and capacitors were utilized to simulate

CMOS logic. It was arbitrarily decided that the voltage level on an inactive line is acceptable if it is less than ten percent of the signal applied to the active line. Also, for the sake of simplicity, the highest voltage level produced on the inactive line was considered, regardless of the duration of this level. Of course, finite time is required for the gates to switch and practically a voltage level can only be considered as threatening if it is present for a certain duration. Only one subinterval per side was utilized for UAC to save computation time. Such an assumption does introduce slight error in the results.

In Figure 4-1a the solid-state model for an NMOS transistor is shown. The metal layer, which forms the gate, is electrically isolated from the body of the semiconductor by a silicon dioxide layer. The p-type body of the transistor has two n-wells and when the transistor is conducting, a n-type layer can form at the oxide surface between the two wells. The capacitance from gate to ground is about 0.1 – 0.2 pF. As shown in Figure 4-1b, the gate to ground capacitance is made up of the oxide capacitance and the channel capacitance lying in series. Figure 4-2 shows the relationship between the gate-to-ground capacitance (C), the oxide capacitance (C_{ox}), and the channel capacitance (C_s) [12, 13]. Let the thickness (t_{ox}) of the oxide layer lying between the metal and the silicon be 0.1μ. The permittivity of the oxide, ϵ_{ox}, is given in terms of the free-space permittivity, ϵ_0 ($\epsilon_0 = 8.85 * 10^{-14}$ F/cm), by

$$\epsilon_{ox} = 3.9\epsilon_0.$$

$$\frac{C_{ox}}{A} = \frac{\epsilon_{ox}}{t_{ox}} = 34.515\ nF/cm^2.$$

If the area A of the gate is assumed to be $(2\mu * 10\mu)$, C_{ox} comes out to be $6.903 * 10^{-15}$ F. Since more than one transistor is driven and the capacitance of the line is also included, the line-to-ground capacitance is modeled as 0.1 pF.

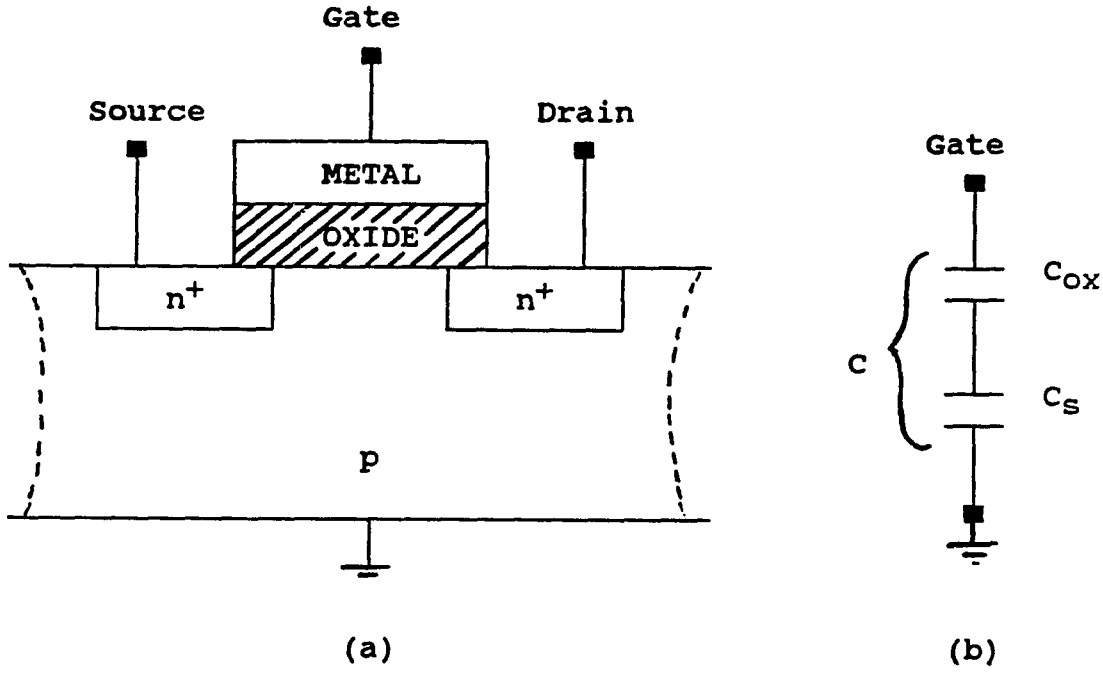


Figure 4-1. (a) Solid-state model for NMOS transistor. The p-type body of the transistor has two n-wells and when the transistor is conducting, a n-type layer between the two wells can form at the oxide surface. Three-terminals and body is grounded.
(b) Gate-to-ground capacitance, C, is made up of oxide capacitance, C_{ox}, and channel capacitance, C_s.

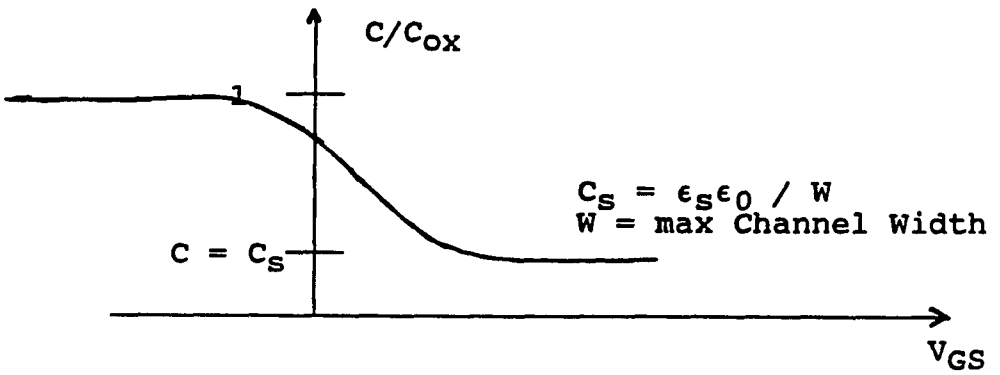


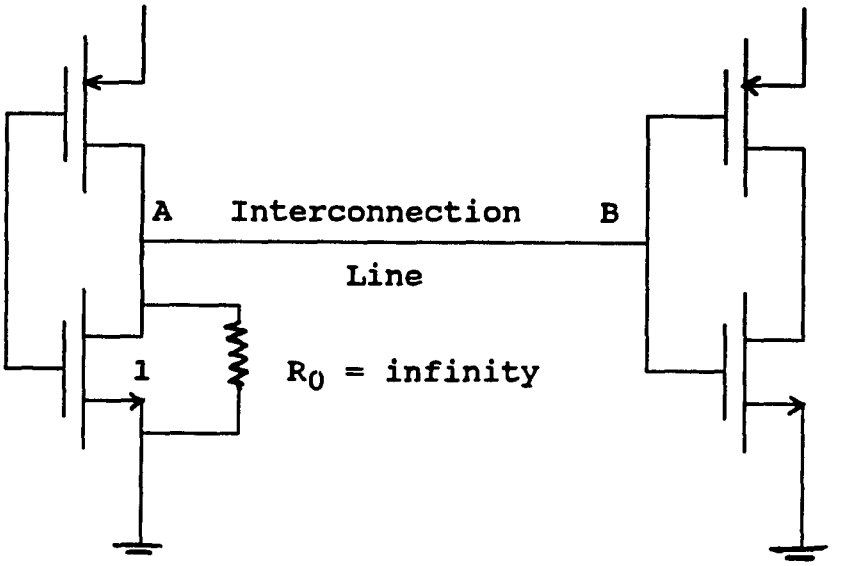
Figure 4-2. The ratio (C/C_{ox}) is plotted versus V_{GS}. C_s is the Channel capacitance, and ϵ_s is the substrate permittivity.

The interconnect line is shown as running between the driver and a load in figure 4-3a. For an inactive line, the region of operation for transistor 1 is shown in figure 4-3b — V_{DS} is small because the inactive line is not driven. The slope in the region of operation is about 1/25 mhos — hence the near-end termination for the inactive lines is taken as 25 ohms in most cases. As the resistance from gate of a transistor to the ground is almost infinite, the far-end resistance is approximated by 10K ohms in most cases.

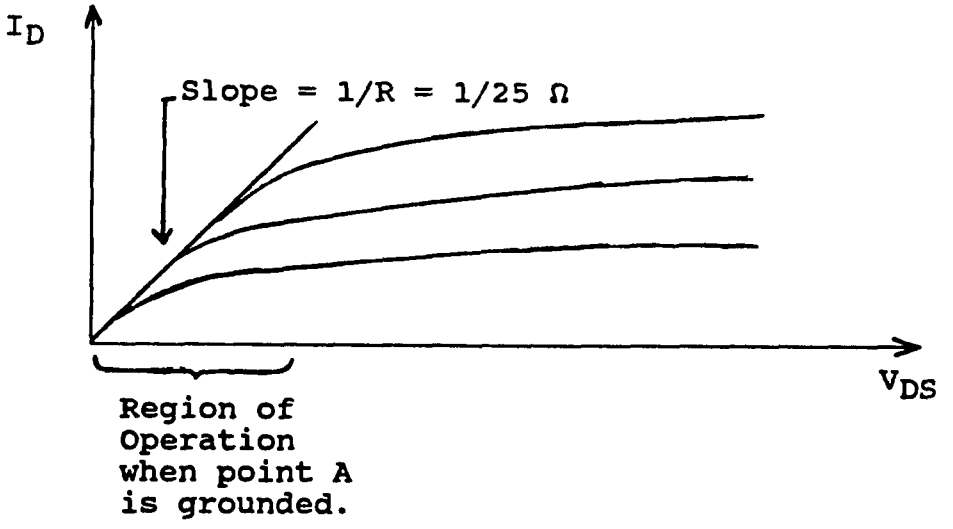
Due to the absence of a tool that would predict the behavior of the transmission line system for periodic inputs, the author resorted to using a ramp input. If the rise time of the input signal is given by t_r, the highest frequency is roughly estimated by [6]

$$Highest frequency = \frac{0.35}{t_r}$$

where rise time is defined as the time taken by the signal to go from ten percent of the final value to ninety percent of the final value.



(a)



(b)

Figure 4-3. (a) An interconnection line connecting two CMOS gates.
(b) Region of operation at point A when transistor 1 is conducting.

4.2 Analysis of Geometry One

Consider the geometry for the (n + 1) conductors shown in figure 4-4a in which (n + 1) conductors are shown buried in a dielectric (SiO_2) of relative permittivity 3.9 . The conductors are arbitrarily placed four microns below the air–silicon dioxide interface and five microns above the ground. Each conductor is of thickness one micron, and length one inch. Width of the nth conductor is denoted as W_n, and the spacing between the nth and the $(n+1)th$ conductor is denoted as sn. As shown in Figure 4-4b, both the source resistance and the near-end terminations for the inactive lines are 25 ohms, while the far-end terminations are chosen as 10K ohms. Both ends of all the lines are also tied to ground through 0.1 pF capacitors. The rise-time of the 1V voltage source is 0.1 ns, and the total length of simulations is 1 ns. It is noticed that whether the voltage is higher at the near-end or the far-end depends on which has a greater resistor tied to it.

Length does make a difference on the voltage seen at the far-end on line 2. Voltages for lengths of one centimeter, one inch, and five centimeters are compared in Figure 4-5. The effect of the dielectric interface as the height of conductors is varied is shown in Figure 4-6, where (C_{11}/ϵ_{R2}) is plotted versus ϵ_{R2} for height of conductors equal to one, two, four, six, eight, and ten microns. If there is no effect of the dielecric interface, the curves in Figure 4-6 should be flat [4]. But, as the height of the conductors is increased, there is more and more coupling with the surface and the curves are no longer constant. At a height of five microns, there is some coupling.

Consider a two conductor case. If conductor 0 is the active conductor and conductor 1 is an inactive conductor, *First – Line Separation* (*FLS*) is defined as the spacing, $s0$, between conductors 0 and 1, required to get 0.1 V on conductor 1.

If conductor 0 is the active conductor and conductors 1 and 2 are the inactive conductors, *Second – Line Separation* (*SLS*) is defined as the spacing, $s1$,

between conductors 1 and 2, required to get 0.1 V on conductor 2. The spacing between conductors 0 and 1, $s0$, is assumed to be fixed at the minimum possible spacing, i.e 1 micron. Third-Line Separation (TLS), FOurth-Line Separation (FOLS), FIfth-Line Separation (FILS), e.t.c are similarly defined.

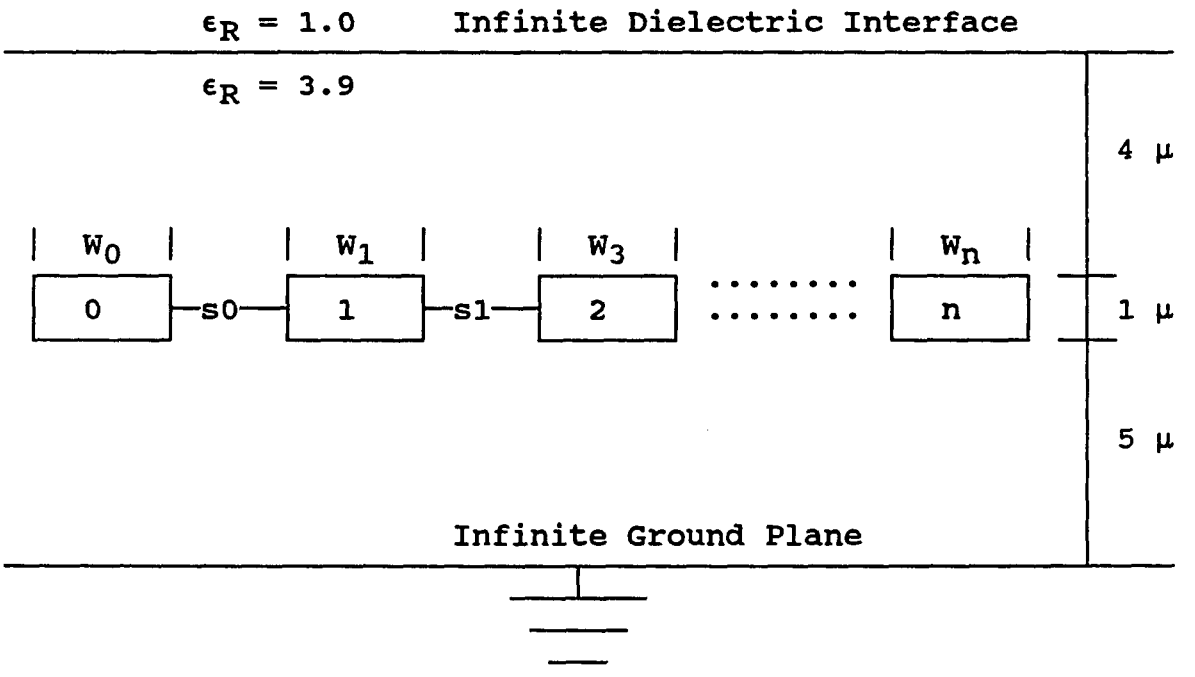


Figure 4-4a Cross-section of Geometry 1 for (n + 1) conductor case. Conductor 0 is the only active conductor. Conductors, buried in Silicon - dioxide, are at a distance of four microns from the dielectric surface and five microns from the ground plane. The thickness of each conductor is one micron.

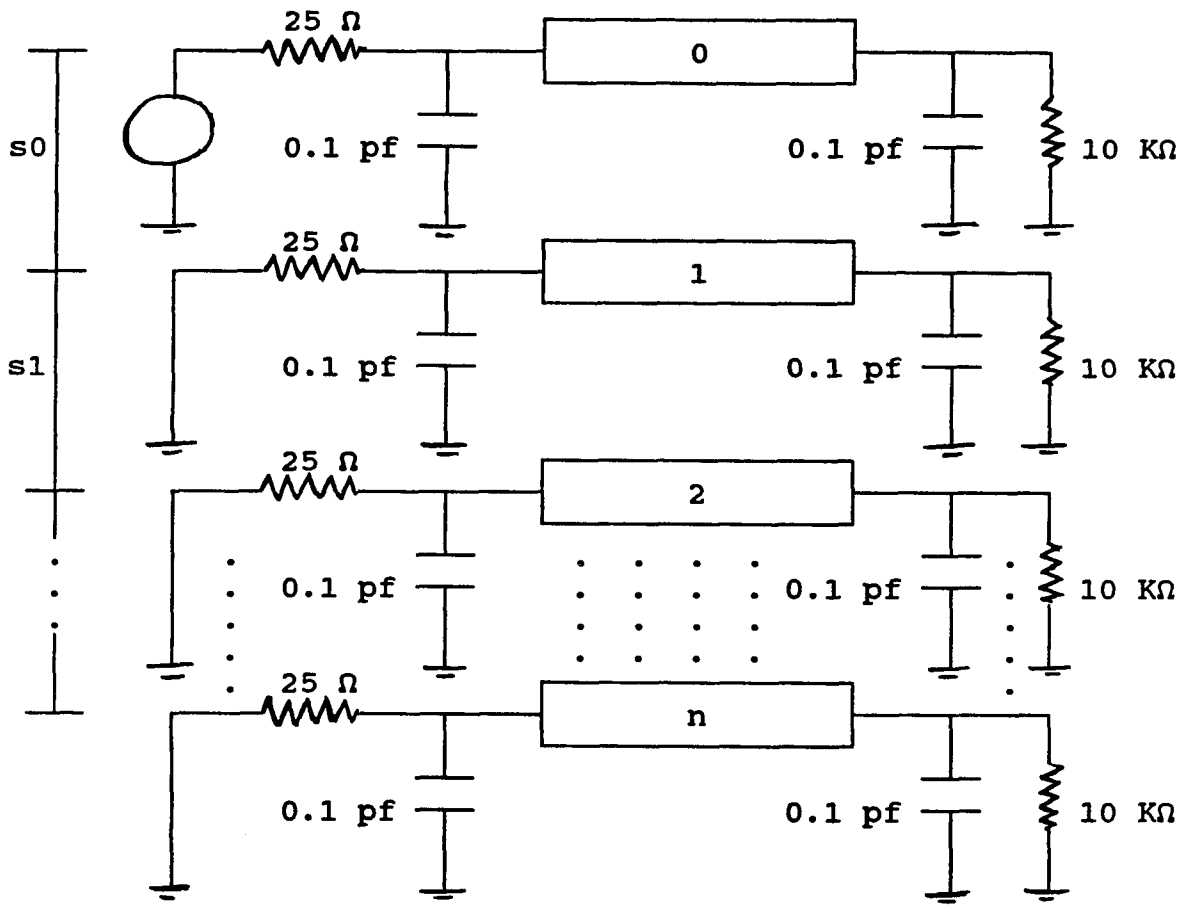


Figure 4-4b (n + 1) transmission-line system. Value of source resistor, and near-end termination resistors = 25 ohms. Value of far-end termination resistors = 10 Kohms. 0.1 pf capacitors are connected to all the near and far-ends. Conductor 0 is active.

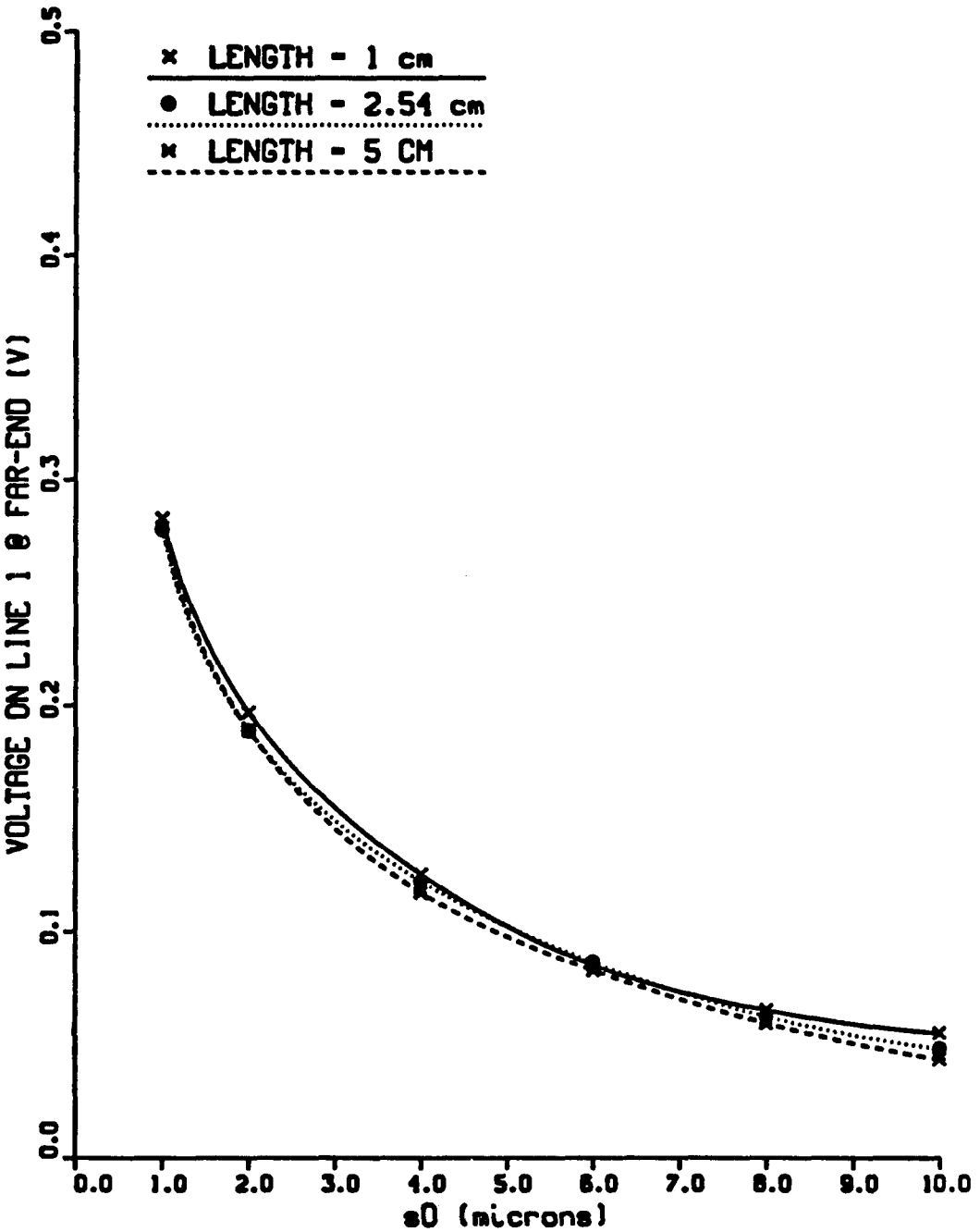


Figure 4-5 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for $W_0 = W_1 = W = 1$ micron. Two-conductor case of Geometry One. Length of conductors = 1 cm, 2.54 cm, and 5 cm.

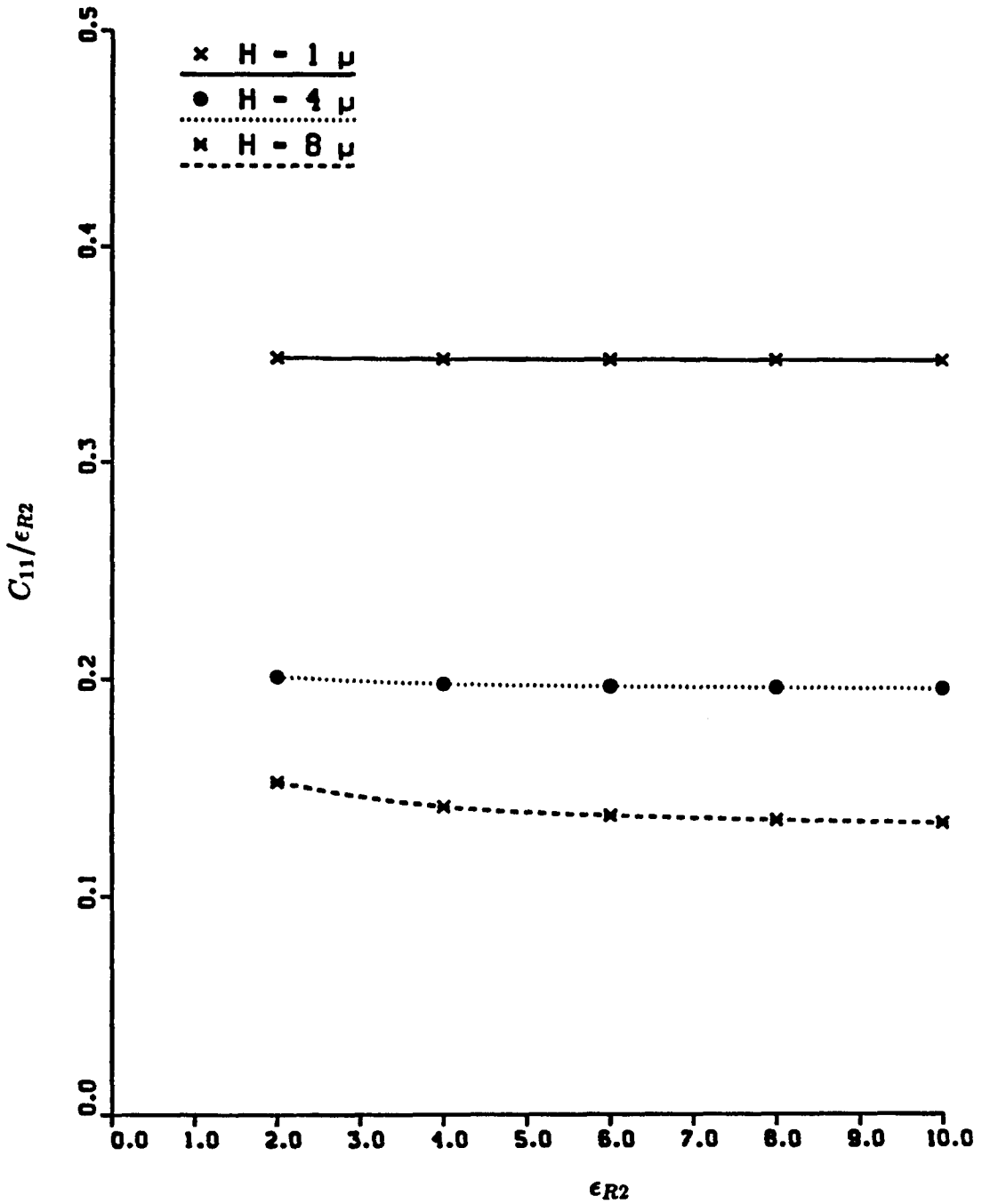


Figure 4-6 C_{11} / ϵ_{R2} versus ϵ_{R2} for W_0 = W1 = 1 micron. Height, h, of conductors above ground plane = 1, 4, and 8 microns. s0, spacing between conductors 0 and 1, is 10 microns.

4.2.1 *Analysis of Shielding Affects*

Shielding affects the crosstalk experienced by the neighbors of an active line. To illustrate this affect on a line lying next to the active line, four cases are considered. The network configurations of these four cases are presented in Figure 4-7 and the results in Figure 4-8. Also the affects of external shielding on an inactive line, which is separated from the active line by another inactive line, are considered in Figures 4-9 and 4-10.

Let x be the spacing between the active line and the inactive line being considered. The simplest two-line case is shown in Figure 4-7a as Case IA. There is no shielding in this case. Case IIA shown in Figure 4-7b depicts the case of having external shielding on conductor 1. In Case IIIA shown in Figure 4-7c, conductor 0 acts as external shielding on conductor 1, the active conductor. The separation between conductors 1 and 2 is varied and the affect on the far-end voltage on conductor 2 studied. In Case IVA shown in Figure 4-7d, both the active conductor, i.e conductor 1, and the inactive conductor being considered, i.e conductor 2, have external shielding. Cases IA, IIA, and IIIA are compared in Figure 4-8a, and Cases IA, and IVA are compared in Figure 4-8b. From Figures 4-8a, and 4-8b, it is noticed that Case IA has the maximum voltage for a given value of x. Thus, to get the maximum First-Line Separation (FLS), one should consider no shielding.

A simple three-conductors case is presented in Figure 4-9a as Case IB. The spacing between conductors 0 and 1 is fixed at 1 micron and the spacing between conductors 1 and 2 is denoted as a variable, x. The far-end voltage on conductor 2 is considered in this case. Case IIB, shown in Figure 4-9b, is similar to Case IB, except that an additional conductor, i.e conductor 3, is placed one micron from conductor 2. As in Case IB, voltage on conductor 2 is plotted versus x in Figure 4-10. In Case IIIB, Figure 4-9c, conductor 0 acts as external shielding on the active conductor, conductor 1. Let x be the spacing between conductors 1 and

2. Voltage is measured on inactive conductor 2, which is separated from the active conductor by another inactive conductor. For a given x, voltage is maximum for Case IB. The three cases are compared in Figure 4-10. Thus, no shielding should be considered to get maximum Second-Line Separation (SLS).

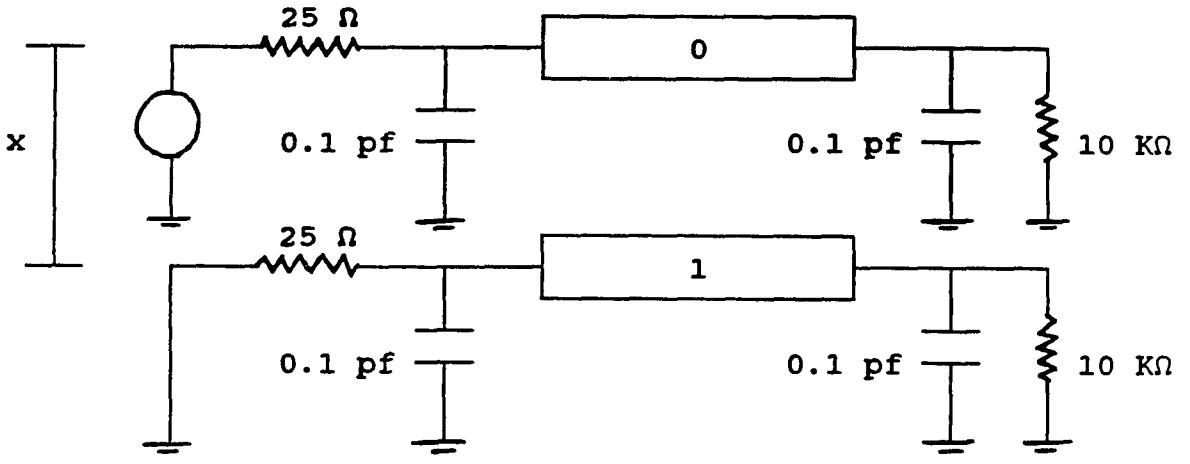


Figure 4-7a CASE IA. Voltage source on conductor 0 and voltage measured at far-end on conductor 1. s0 = x.

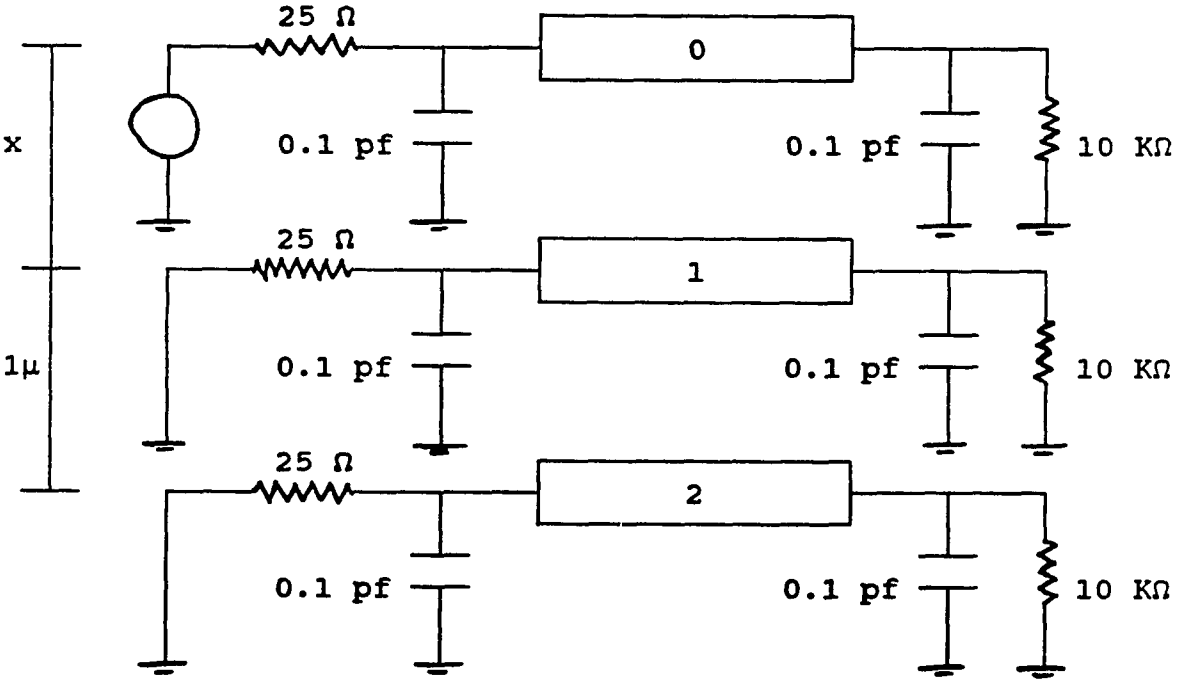


Figure 4-7b CASE IIA. Voltage source on conductor 0, and voltage measured on conductor 1. Conductor 1 is externally shielded by conductor 2. s0 = x, s1 = 1 micron.

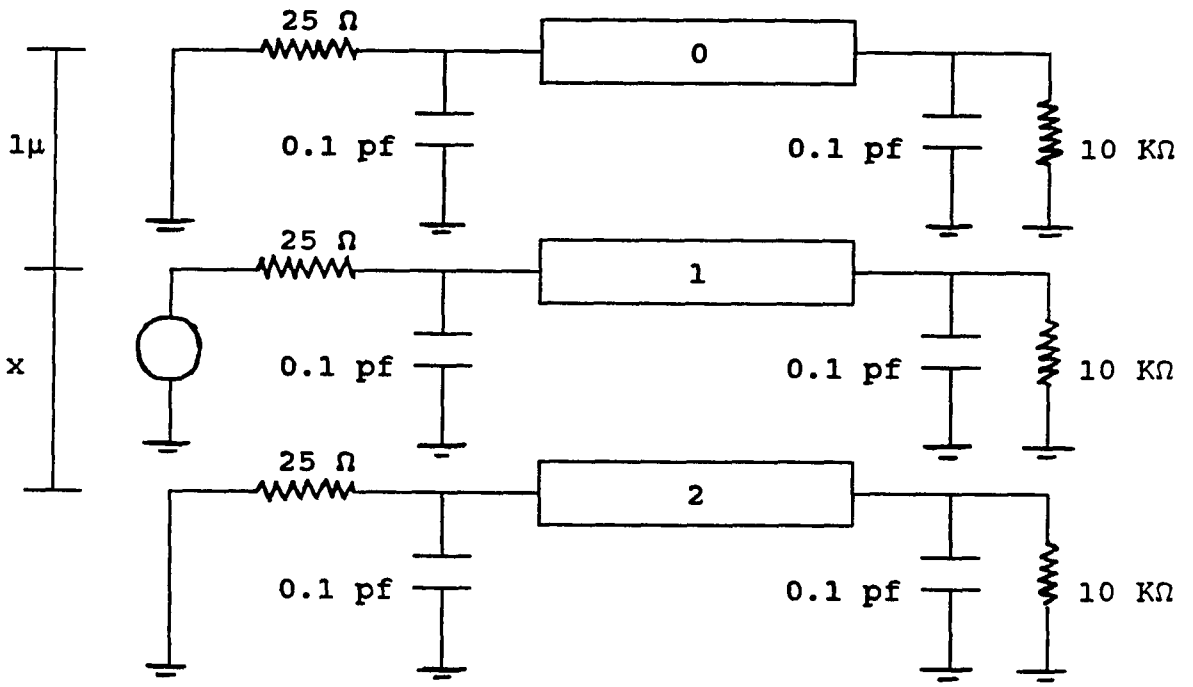


Figure 4-7c CASE IIIA. Voltage source on conductor 1, and voltage measured at far-end on conductor 2. Conductor 0 acts as external shielding for conductor 1. s0 = 1 micron, s1 = x.

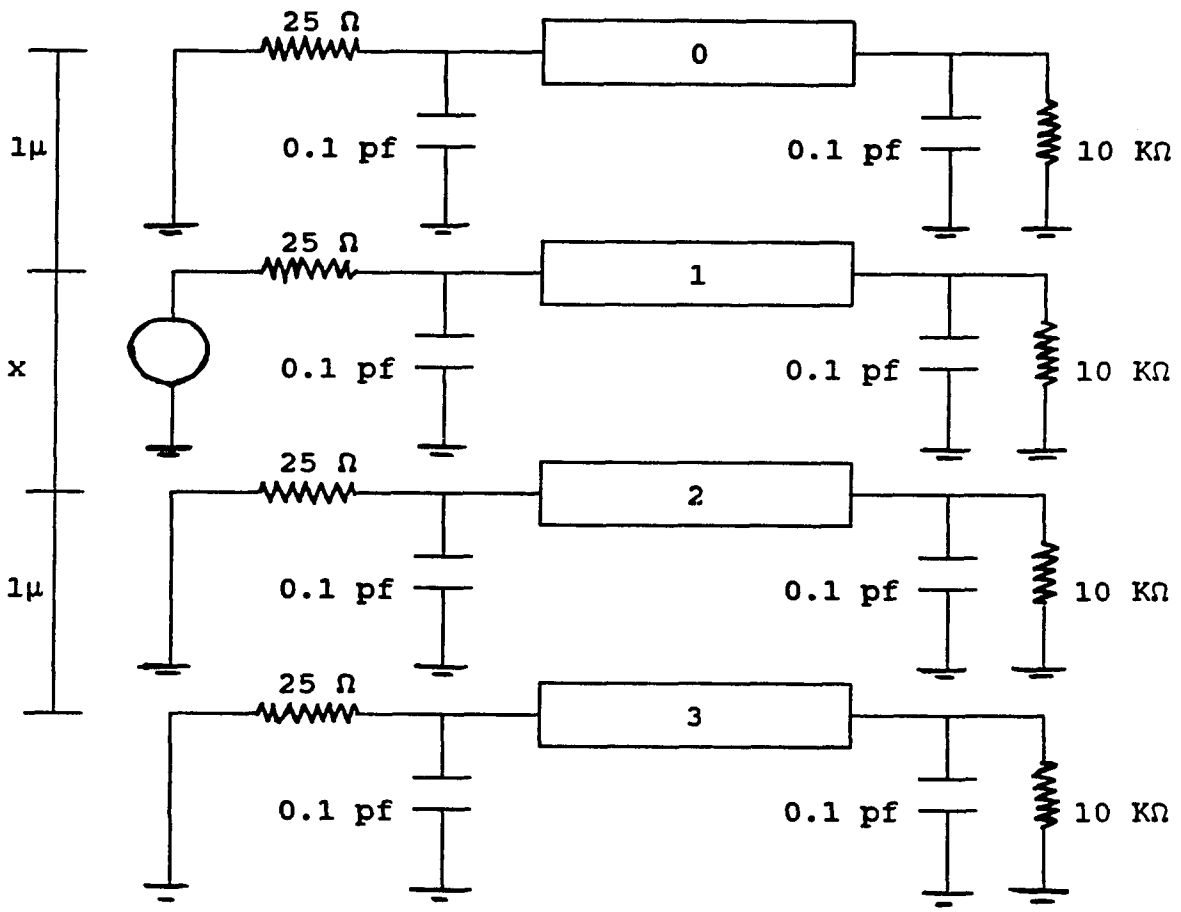


Figure 4-7d CASE IVA. Voltage source on conductor 1 and voltage measured at far-end on conductor 2. Conductor 1 is externally shielded by conductor 0, and conductor 2 is externally shielded by conductor 3. s0 = 1 micron, s1 = x, s2 = 1 micron.

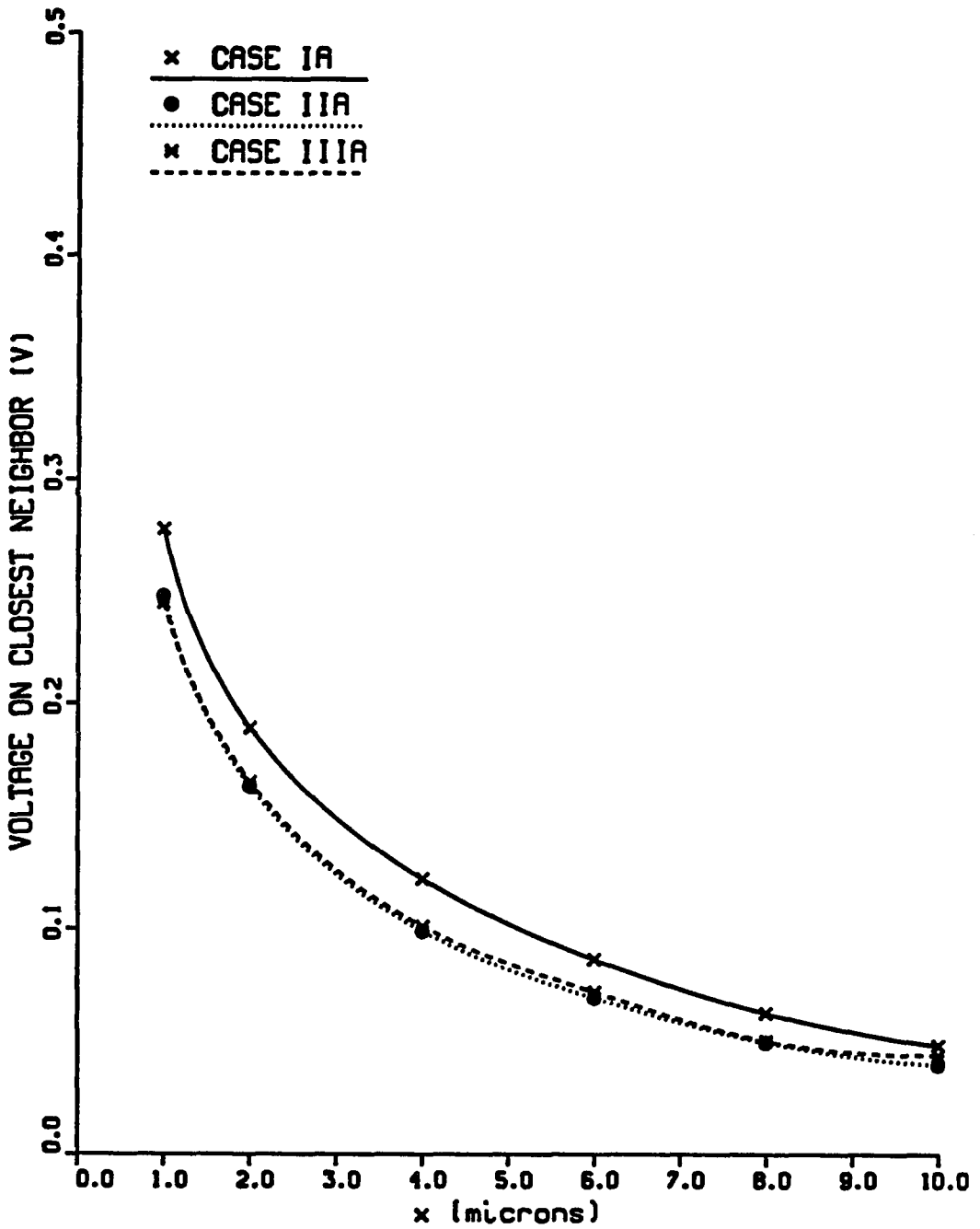


Figure 4-8a Voltage on the inactive line, lying next to the active line, versus x, spacing between the active and the inactive line. Cases IA, IIA, and IIIA, which are presented in Figure 4-7 are compared. Geometry One.

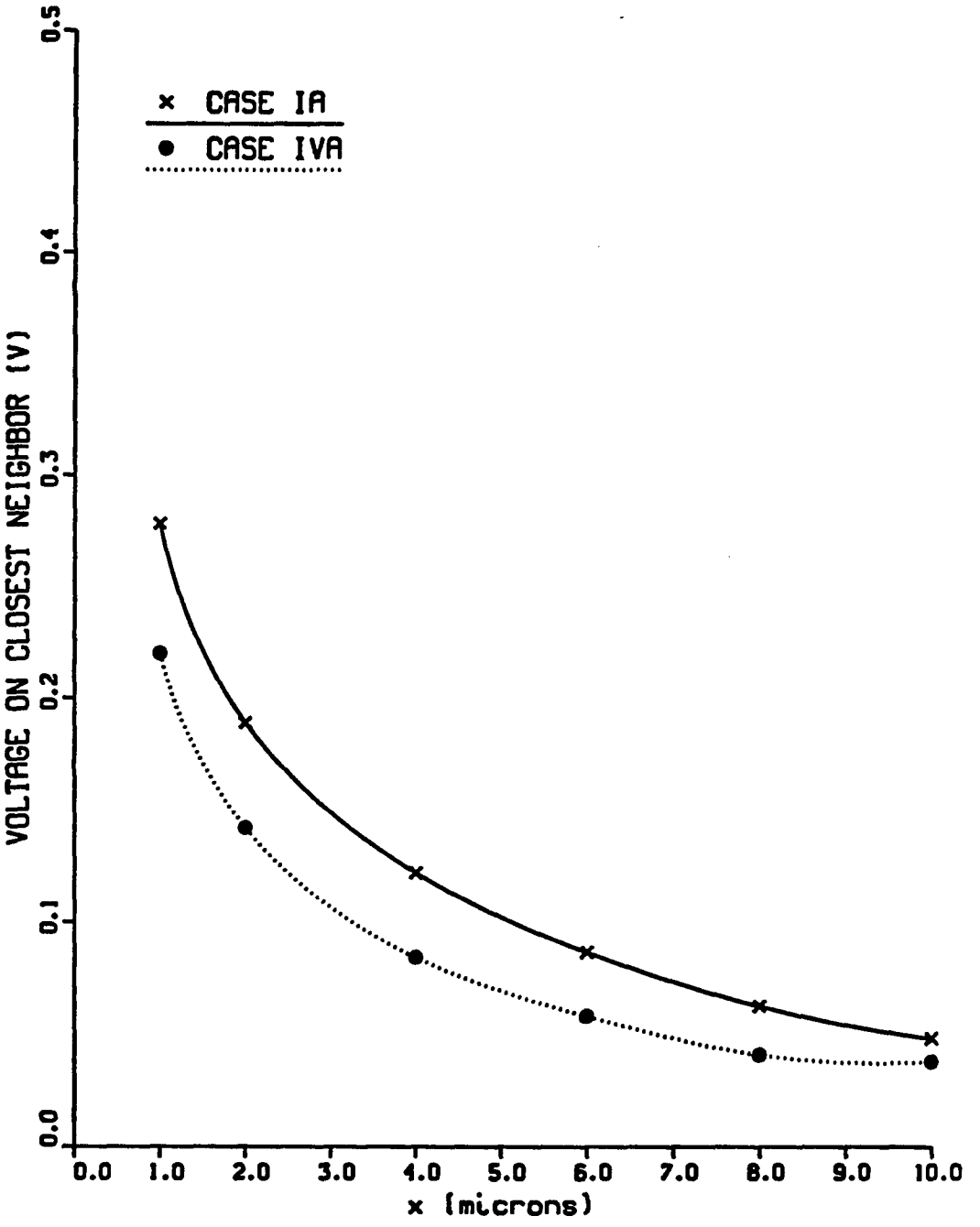


Figure 4-8b Voltage on the inactive line, lying next to the active line, versus x, spacing between the active and the inactive line. Cases IA, and IVA, which are presented in Figure 4-7 are compared. Geometry One.

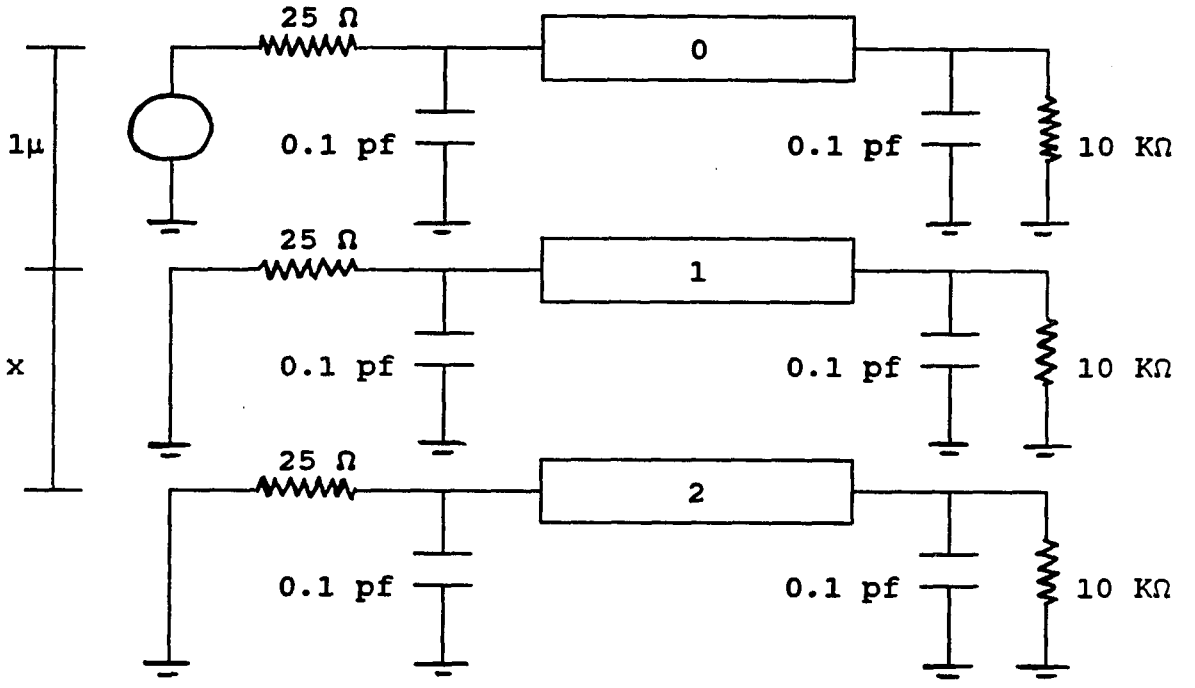


Figure 4-9a CASE IB. Voltage source on conductor 0, and voltage measured at far-end on conductor 2. s0 = 1 micron, s1 = x.

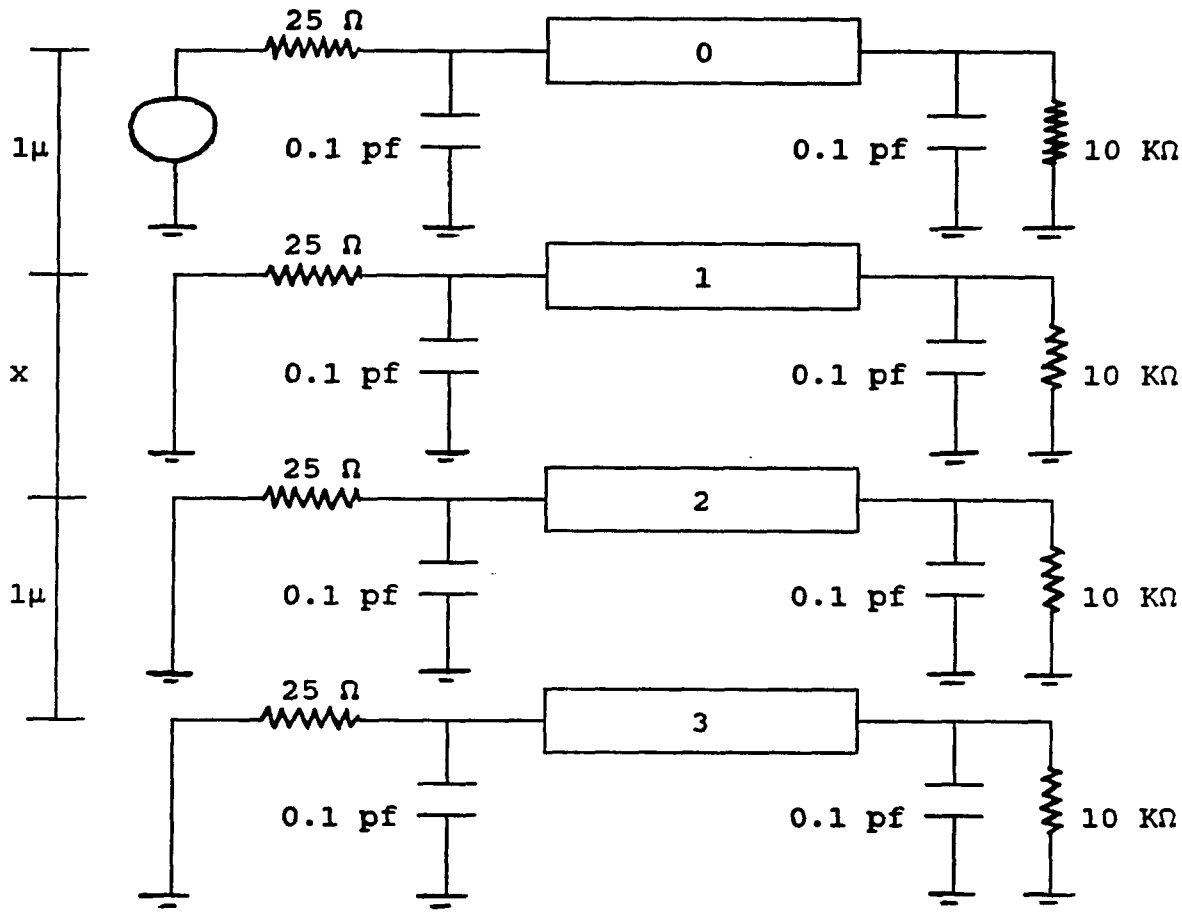


Figure 4-9b CASE IIB. Voltage source on conductor 0 and voltage measured at far-end on conductor 2. Conductor 2 is externally shielded by conductor 3. s0 = 1 micron, s1 = x, s2 = 1 micron.

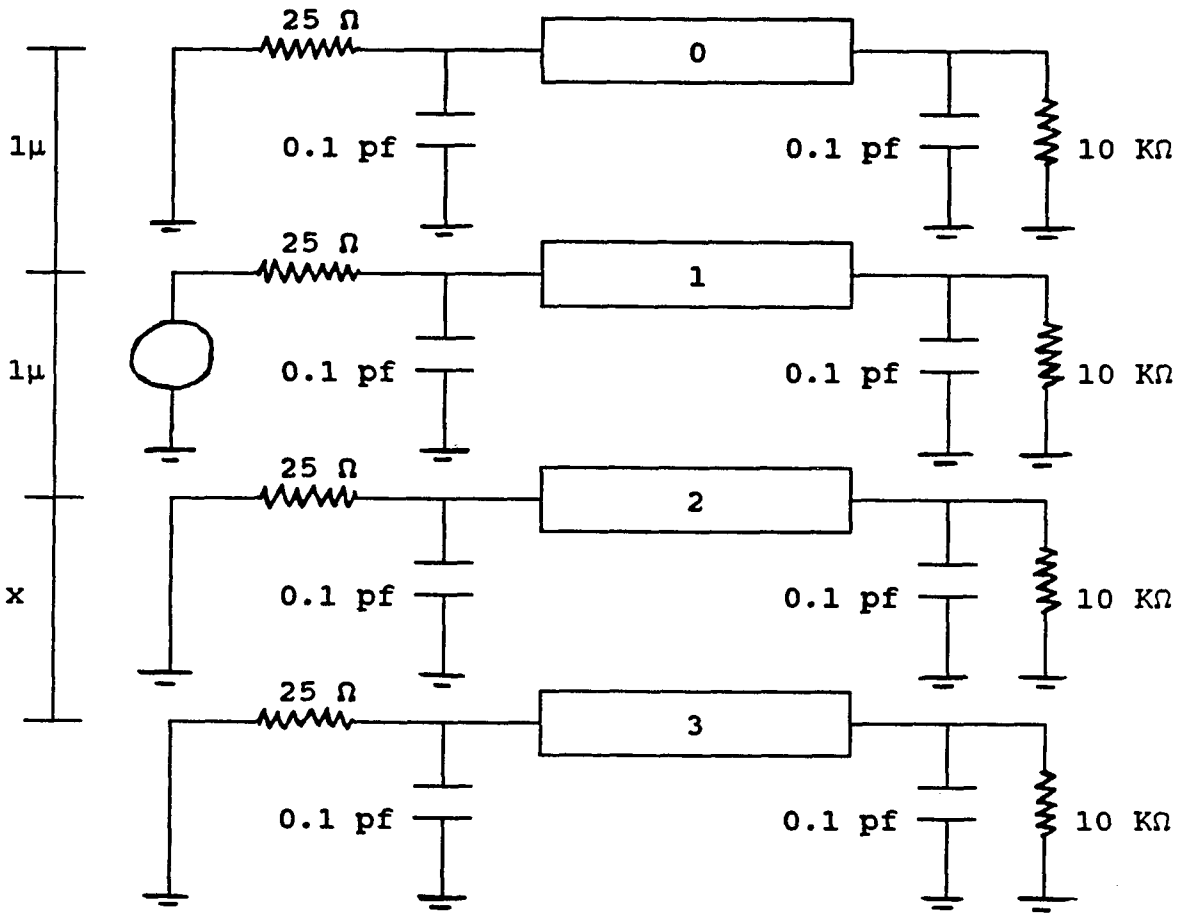


Figure 4-9c CASE IIIB. Voltage source on conductor 1 and voltage measured at far-end on conductor 3. Conductor 1 is externally shielded by conductor 0. s0 = 1 micron, s1 = 1 micron, s2 = x.

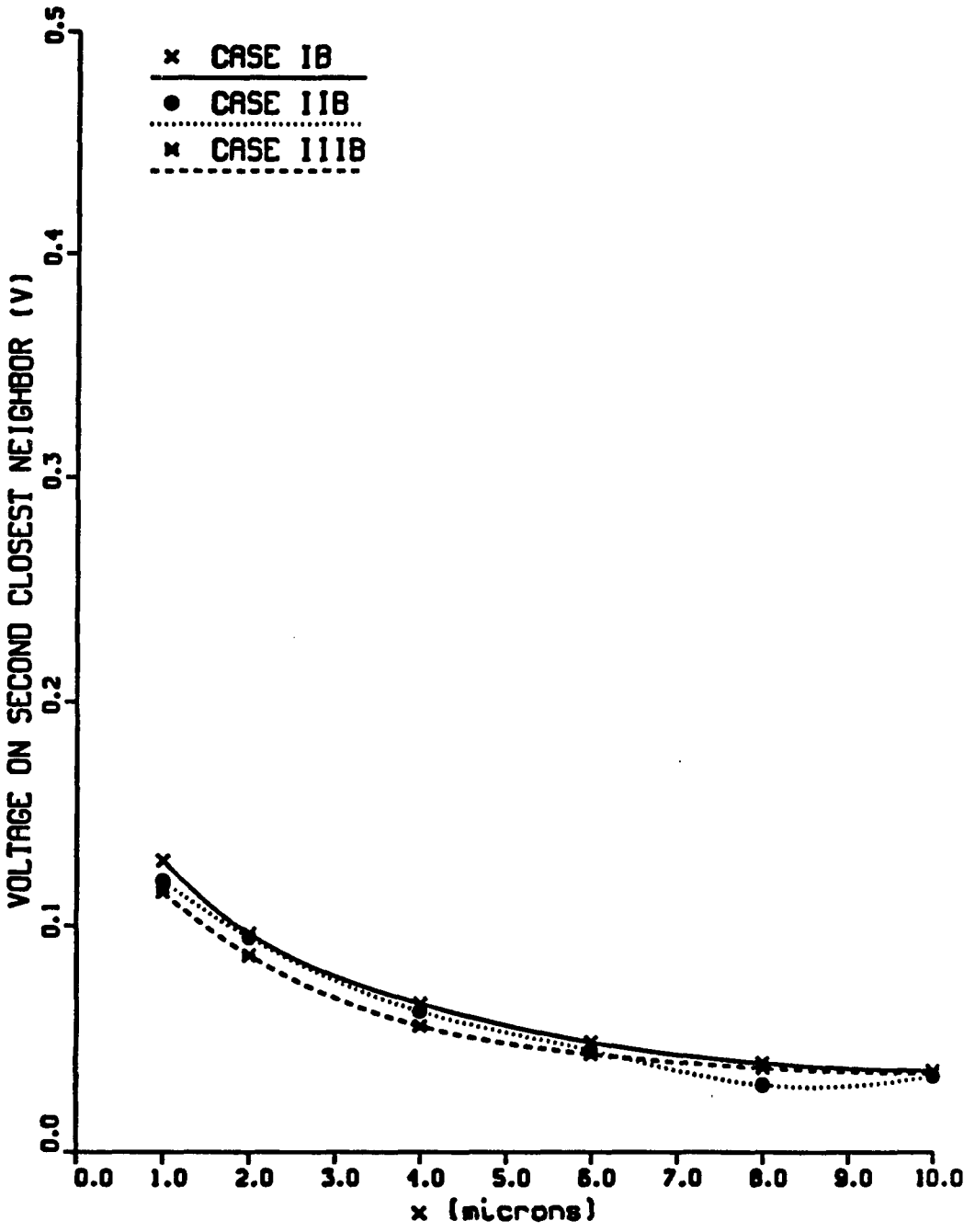


Figure 4-10 Voltage on the inactive line, separated from the active line by another inactive line, versus x, spacing between the active and the inactive line. Cases IB, IIB, and IIIB, which are presented in Figure 4-9 are compared. Geometry One.

4.2.2 *Variation of Width in Geometry One*

As shielding reduces the Line Separation values, maximum values of FLS, SLS, e.t.c are henceforth calculated using minimum number of conductors. Thus, only two conductors are utilized to get FLS, three conductors to get SLS, and so on. Consider Figure 4-4a, which presents the cross-section of Geometry One for (n + 1) conductors case. Conductor 0 is the only active conductor. Width of the nth conductor is denoted as W_n, and the spacing between the nth and the $(n+1)th$ conductor is denoted as sn. For the cases shown in Figure 4-11, $W_0 = W_1 = W$. In Figure 4-11, the variation of far-end voltage on conductor 1 with s0 is plotted for $W = 1$, 2, and 10 microns. It is noticed that the $W = 1$ micron and the $W = 2$ micron curves are almost identical and dominate until the voltage decreases below 0.08 V. Since FLS (First-Line Separation) is the spacing required to get 0.1 V on conductor 1, $W = 1$ curve can be utilized to give the maximum value of FLS. Thus, it is noticed that the smallest possible widths gives the maximum FLS.

To get the results shown in Figure 4-12, the widths of all the conductors are set to W. The far-end voltage on conductor 2 is plotted versus $s1$ for $W =$ 1, 2, and 10 microns. SLS (Second Line Separation) is equal to the value of $s1$ corresponding to a voltage level of 0.1 V on line 2 for $s0 = 1$ micron. Again, the graphs for $W = 1$, 2, and 10 microns are compared and it is noticed that $W = 1$ micron curve gives the maximum value of SLS.

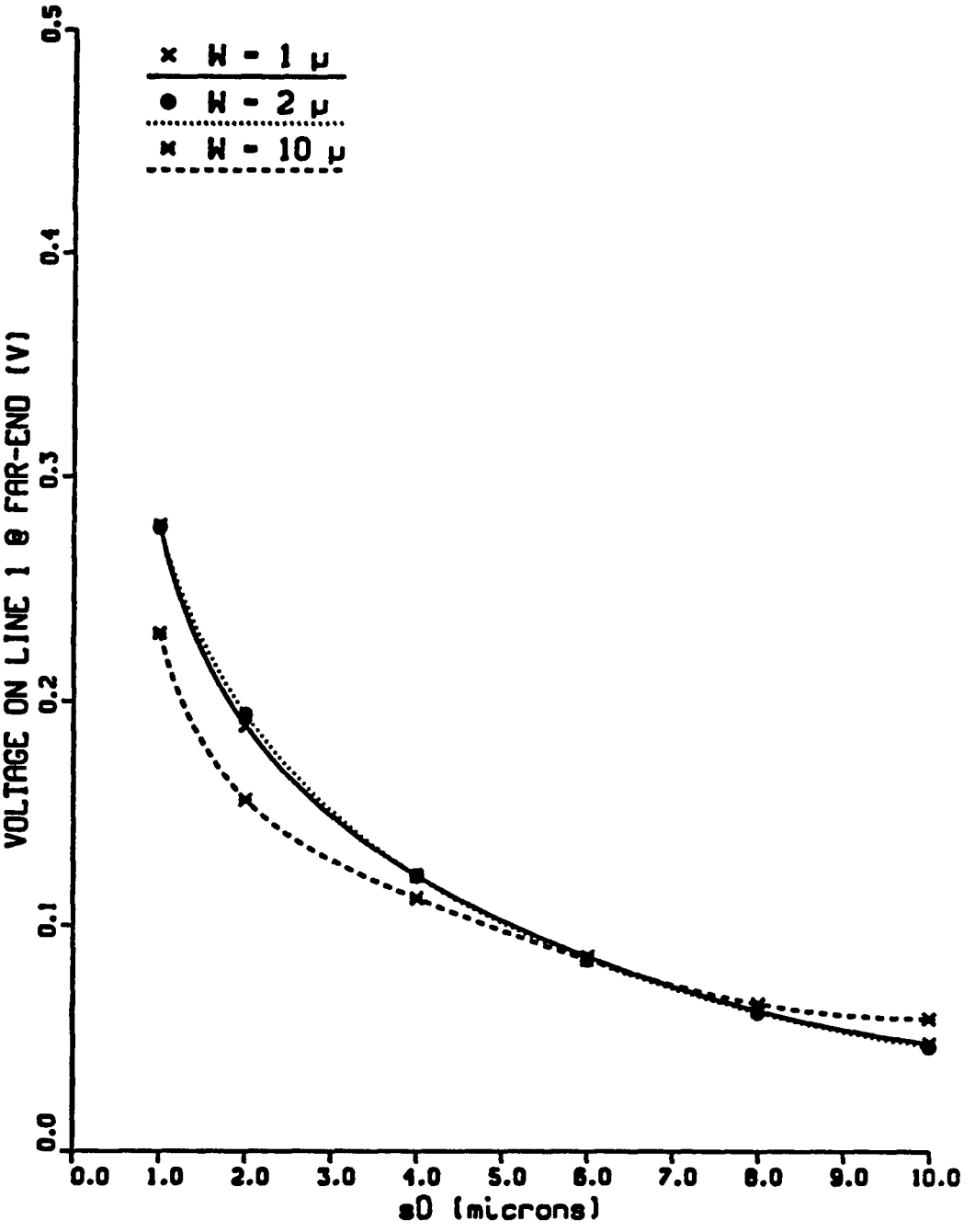


Figure 4-11 Voltage on line 1 versus s0, spacing between lines 0 and 1, for W = 1, 2, and 10 microns. Two-line case of Geometry One. $W_0 = W_1 = W$.

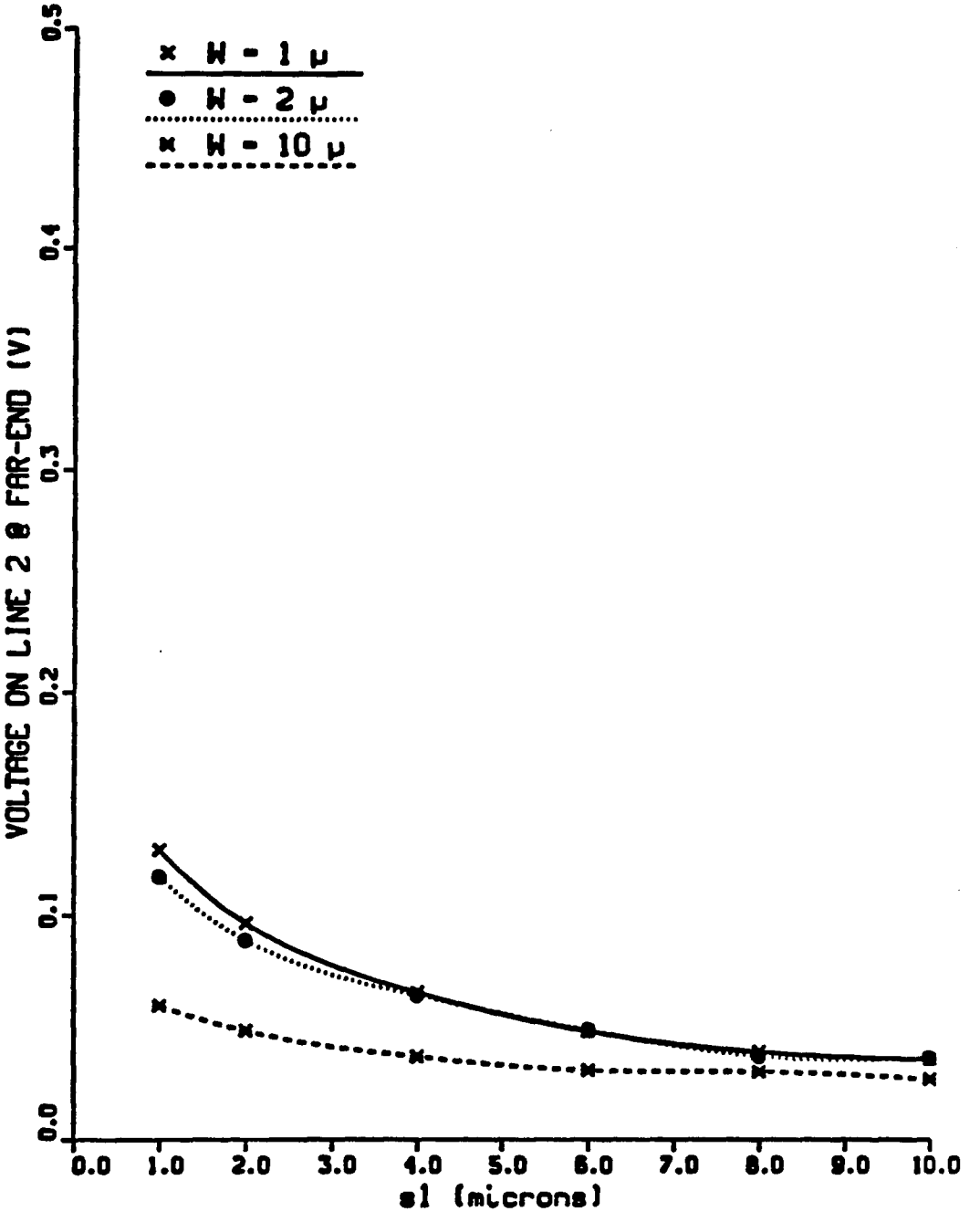


Figure 4-12 Voltage on line 2 versus s1, spacing between lines 1 and 2, for W = 1, 2, and 10 microns. Three-line case of Geometry One. s0 = 1 micron. $W_0 = W_1 = W_2 = W$.

4.2.3 *Unequal Widths in Geometry One*

Four figures, Figure 4-13, Figure 4-14, Figure 4-15, and Figure 4-16, are presented in this subsection. The first three are based on the two-conductor case while the fourth depends on the three-conductor case. Width of all the conductors is equal to one micron for solid-line case in all the four graphs. Conductor 0 is assumed to be the only active conductor.

In Figure 4-13, Figure 4-14, and Figure 4-15, the far-end voltage on conductor 1 is plotted versus s0. In Figure 4-13 W_0 is fixed at one micron and three values of W_1 are considered. The three graphs for W_1 = 1, 2, and 3 microns are noticed to be almost identical. Thus, using W_1 = 1 micron to get the maximum value of FLS (First-Line Separation) should give no error. In Figure 4-14, W_0 is fixed at 2 microns for the dotted-line and the dashed-line curves. For the solid-line case, $W_0 = W_1 = W$ = 1 micron. For the dotted-line curve, W_0 = 2 microns and W_1 = 1 micron. For the dashed-line curve, $W_0 = W_1$ = 2 microns. Again, it is noticed that the curves are almost identical and thus using $W_0 = W_1$ = 1 micron case to get FLS should not be a problem. In Figure 4-15, the above procedure is repeated for W_0 = 3 microns. The solid-line curve is the same as in Figure 4-14, but for the dotted-line curve W_0 = 3 microns and W_1 = 1 micron. $W_0 = W_1$ = 3 microns for the dashed-line curve. The conclusion is similar to that drawn for the previous two figures.

Experimental results for a three-conductors case are presented in Figure 4-16. W_0, W_1, and $s0$ are fixed at one micron. Three cases of W_2 = 1, 2, and 3 microns are considered. Since the three curves are almost identical, calculation of Second-Line Separation (SLS) using $W_0 = W_1 = W_2$ = 1 micron should be satisfactory.

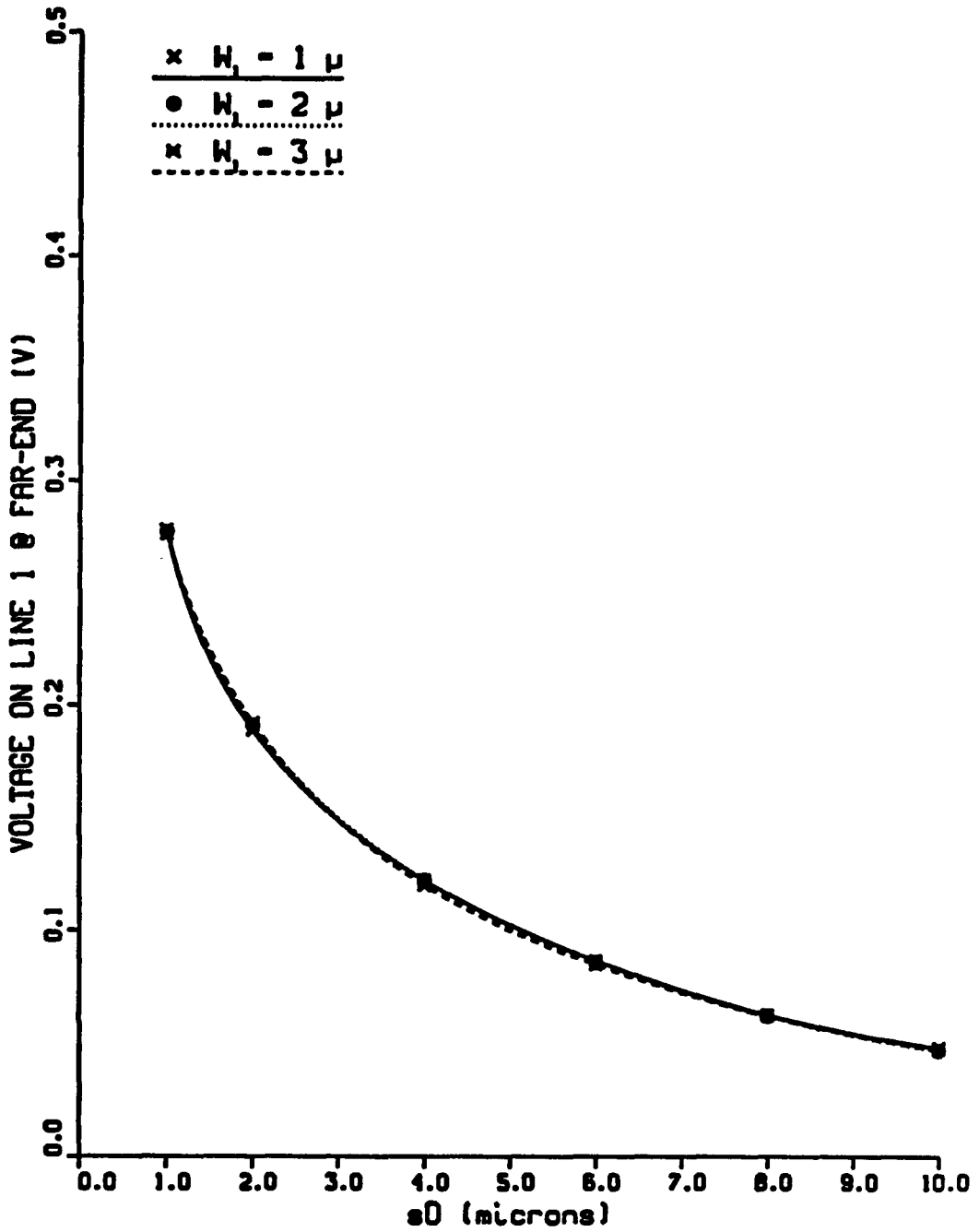


Figure 4-13 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for W_1 = 1, 2, and 3 microns. Two-conductor case of Geometry One. W_0 = 1 micron.

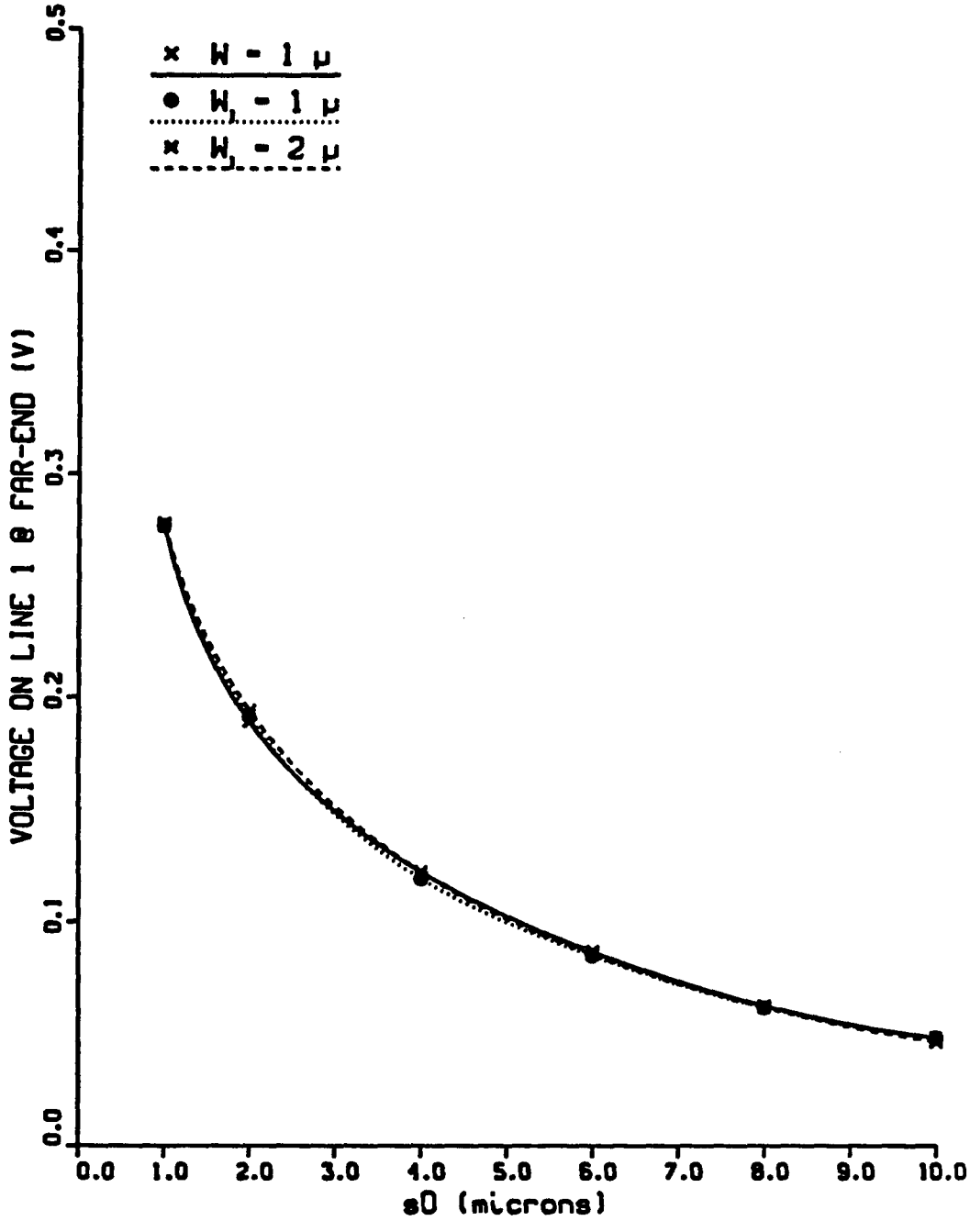


Figure 4-14 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for two-conductor case of Geometry One. In solid-line case, W_0 = W_1 = 1 micron. W_0 = 2 microns for the other two cases and W_1 equals 1 and 2 microns for the dotted-line and the dashed-line respectively.

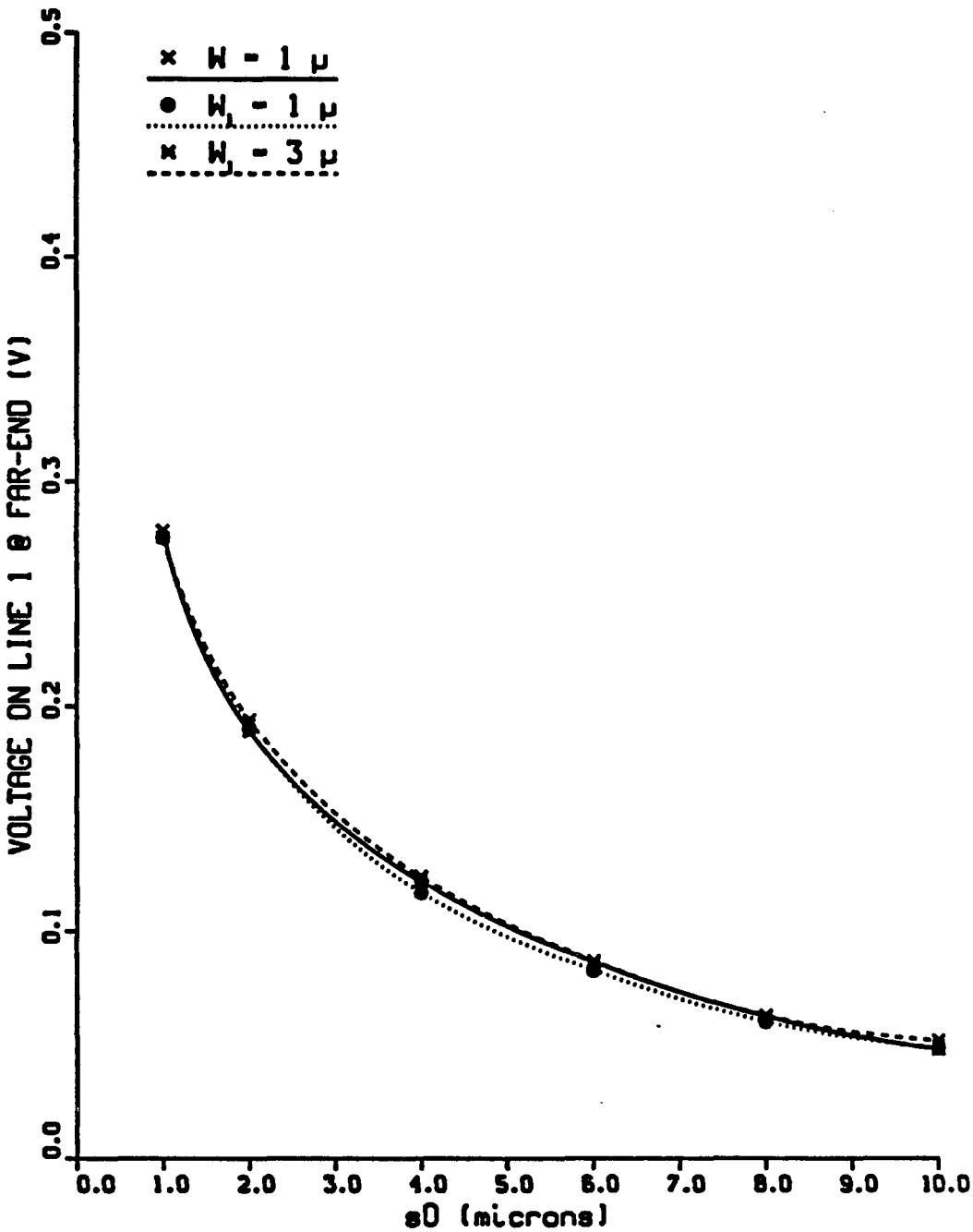


Figure 4-15 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for two-conductor case of Geometry One. In solid-line case, W_0 = W_1 = W = 1 micron. W_0 = 3 microns for the other two cases and W_1 equals 1 and 3 microns for the dotted-line and the dashed-line respectively.

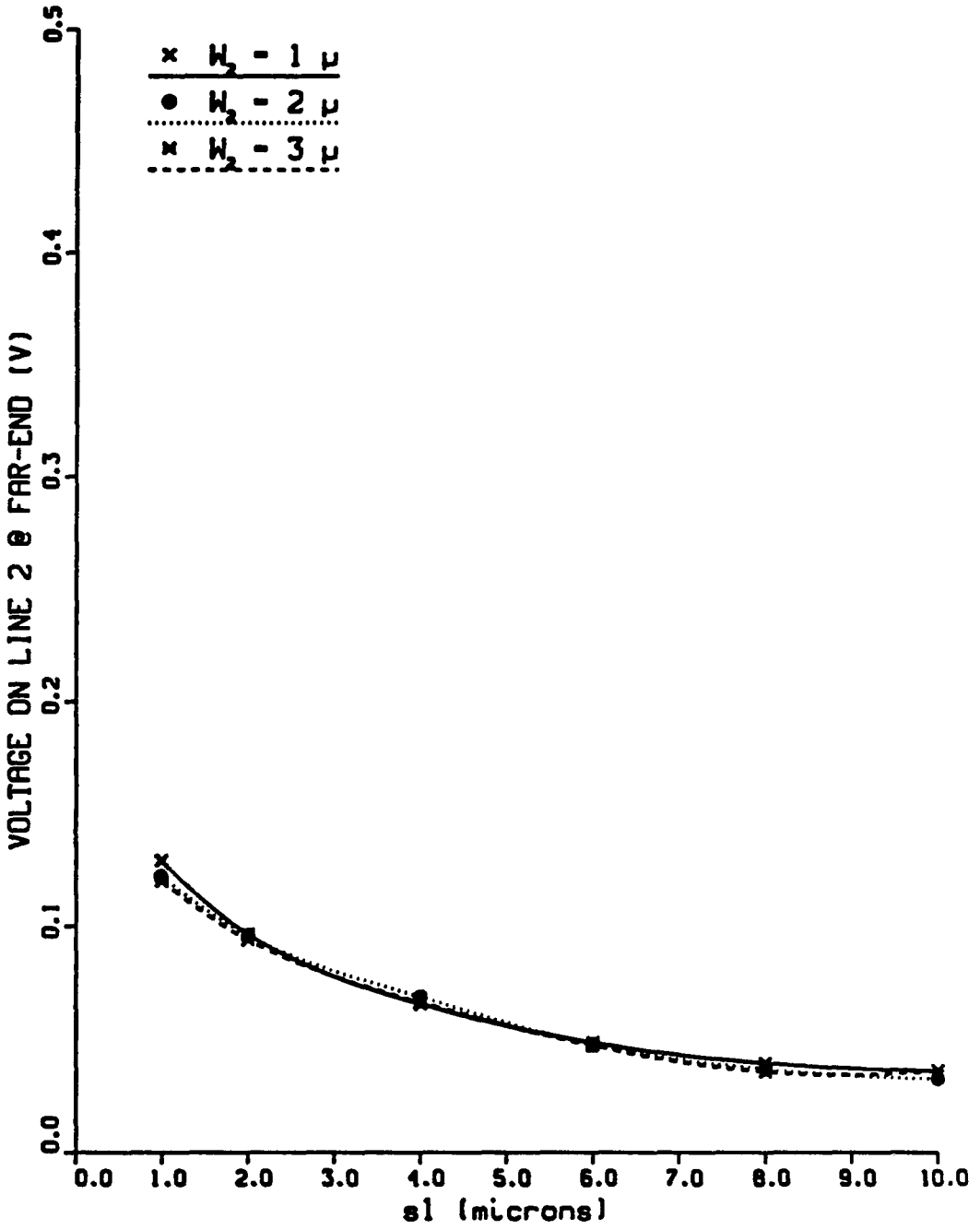


Figure 4-16 Voltage on conductor 2 versus s1, spacing between conductors 1 and 2, for three-conductor case of Geometry One. $W_0 = W_1 = 1$ micron. W2 = 1, 2, and 3 microns. s0 = 1 micron.

4.3 Analysis of Geometry Two

The (n + 1) conductors case for Geometry Two is presented in Figure 4-17. The conductors are at a distance of one micron from both the dielectric interface and the ground plane. Conductors are numbered 0 to n — conductor 0 is the only active conductor. The seperation between the nth and the $(n+1)th$ conductor is referred to as sn. The width of the nth conductor is referred to as W_n. T, thickness of conductors, is 1 micron in all cases except one.

T = 0.5 microns, and T = 1 micron are compared in Figure 4-18 for a two-conductor case. The far-end voltage on conductor 1 is plotted versus $s0$. It is noticed that decrease in thickness results in decrease in crosstalk.

4.3.1 *Variation of Width in Geometry Two*

The two-conductors case in which $W_0 = W_1 = W$ is considered is presented in Figure 4-19. The far-end voltage on line 2 is plotted versus $s0$ for W = 1, 2, and 3 microns. It is noticed that W = 1 micron curve gives the maximum voltage for a given $s0$. This is because coupling with the dielectric interface and the ground plane increases with width, resulting in increase in line-to-ground capacitance, and thus a decrease in crosstalk. FLS (First-Line Separation) can be calculated from W = 1 micron curve.

The three-conductors case is considered in Figure 4-20. $W_0 = W_1 = W_2 = W$. $s0$ = 1 micron. Two cases, W = 1, and 2 microns, are considered. It is again noticed that the far-end voltage on conductor 2 decreases with increase in the width of the conductors. It is noticed that the voltage on conductor 3 is below 0.1 V even when $s1$ = 1 micron. Thus, SLS is considered not to exist for this geometry.

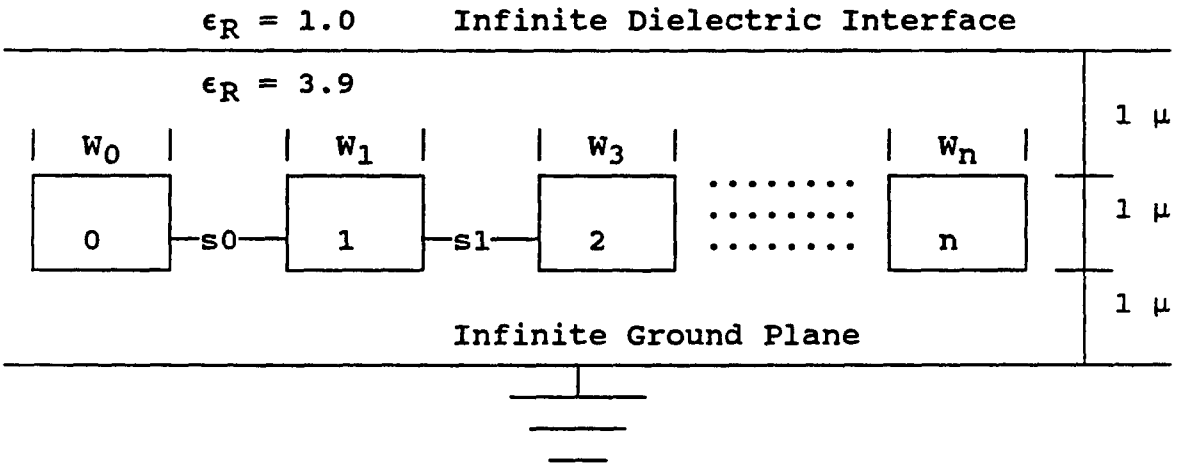


Figure 4-17 Cross-section of Geometry 2 for (n + 1) conductor case. Conductor 0 is the only active conductor. Conductors are buried in Silicon - dioxide and are at a distance of one micron from the dielectric surface and the ground plane. The thickness of each conductor is one micron.

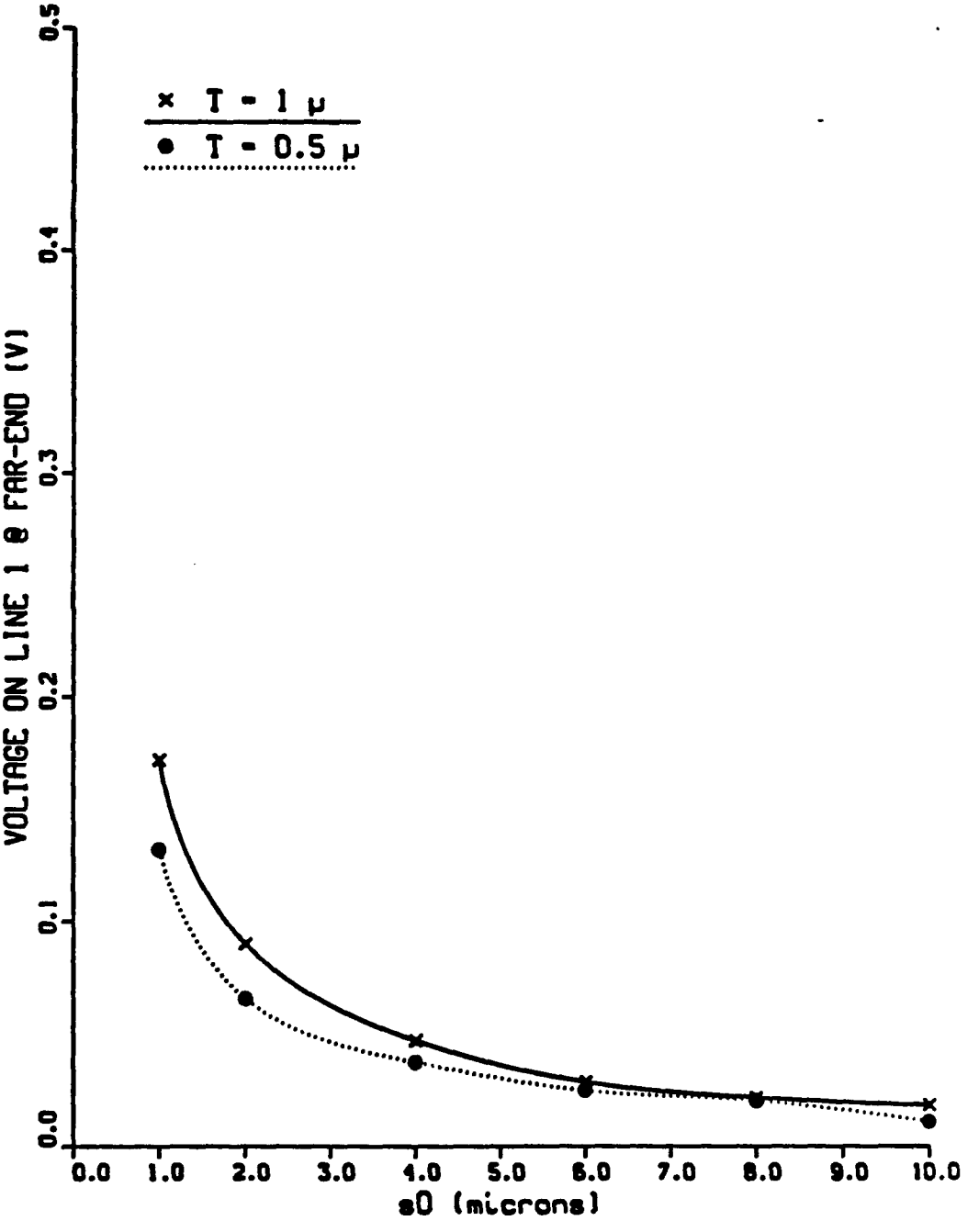


Figure 4-18 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for T = 1, and 0.5 microns. Two-conductor case of Geometry Two. $W_0 = W_1 = W = 1$ micron. T is the thickness of a conductor.

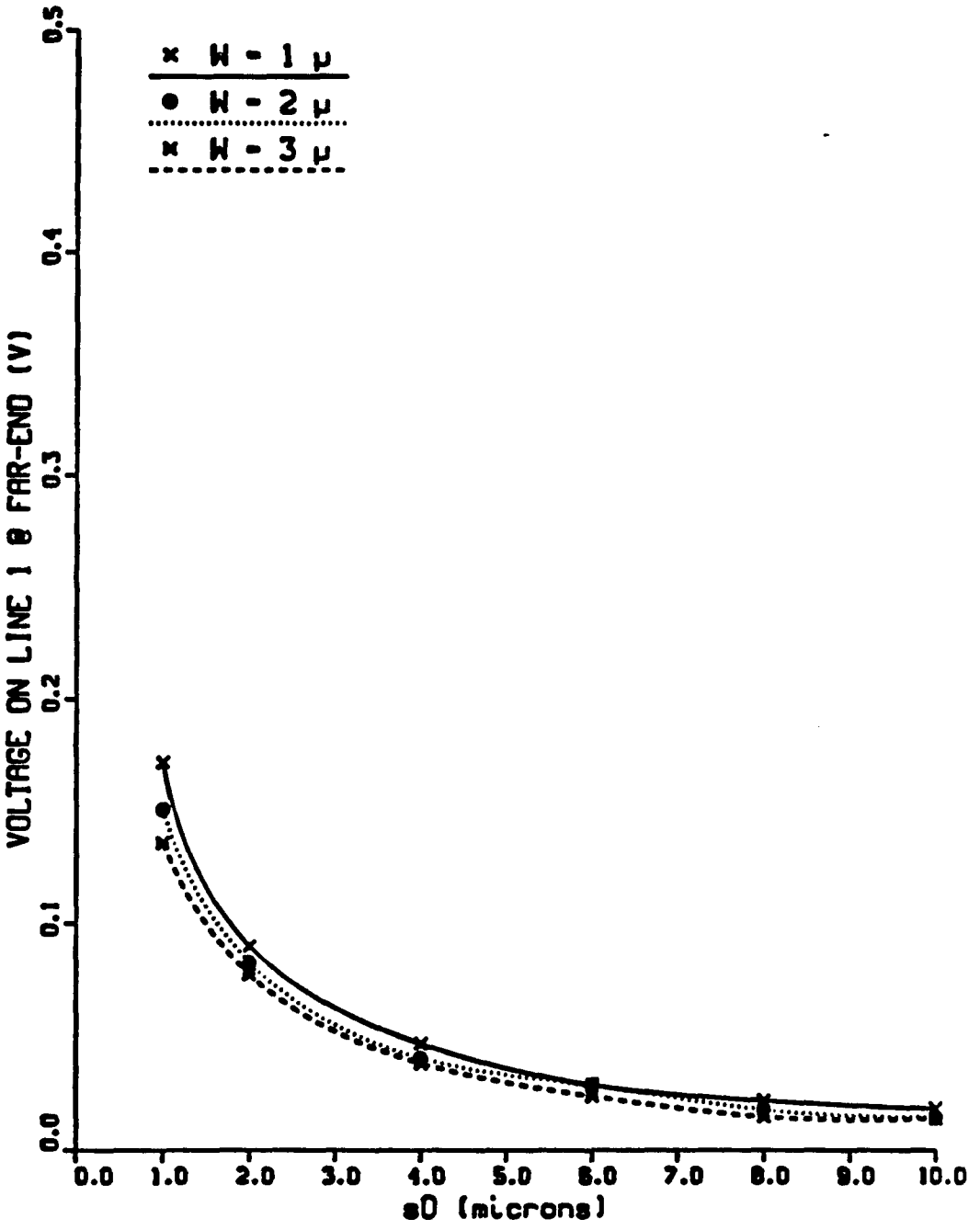


Figure 4-19 Voltage on line 1 versus s0, spacing between lines 0 and 1, for W = 1, 2, and 3 microns. Two-line case of Geometry Two. $W_0 = W_1 = W$.

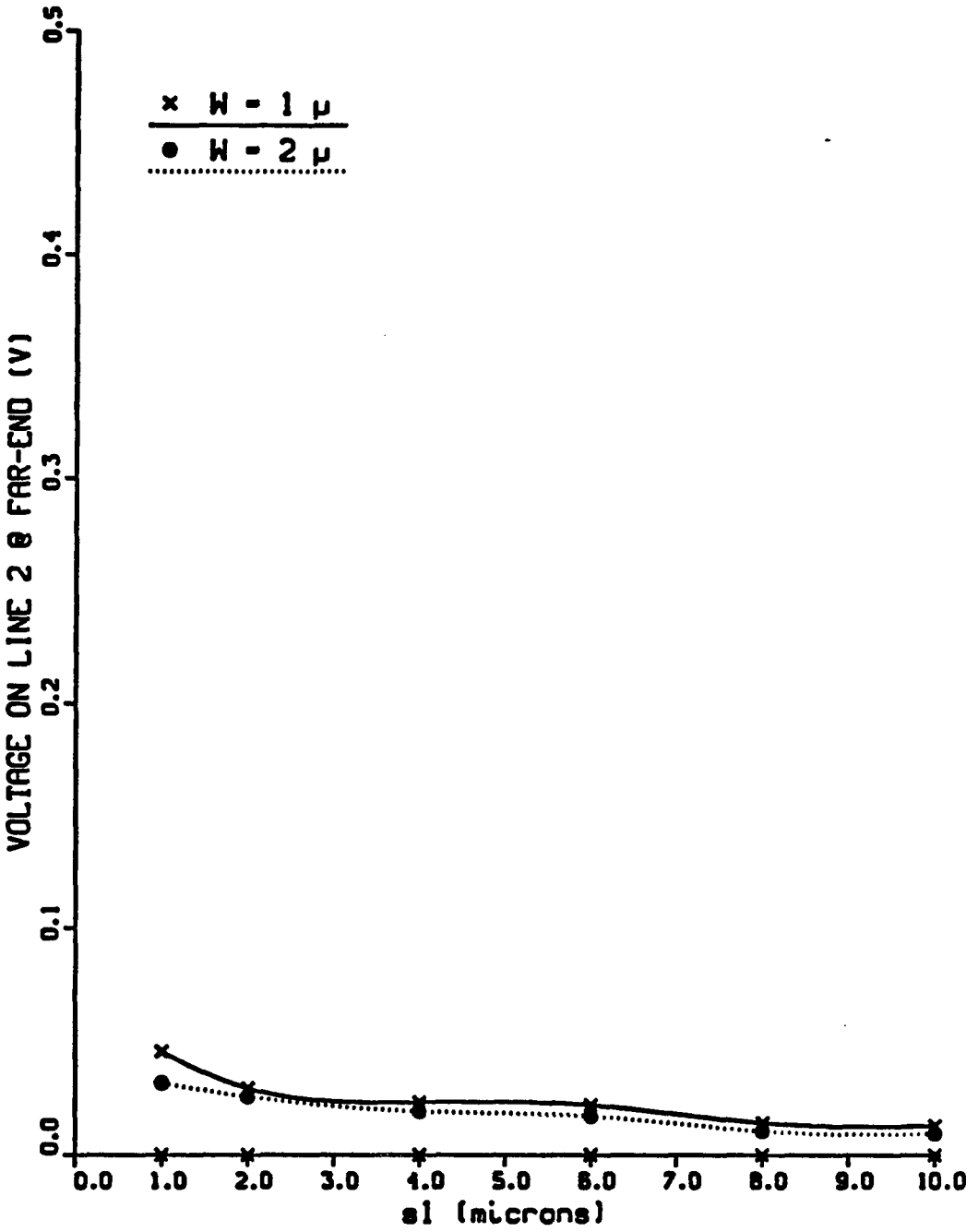


Figure 4-20 Voltage on line 2 versus s1, spacing between lines 1 and 2, for W = 1, and 2 microns. Three-line case of Geometry Two. s0 = 1 micron. $W_0 = W_1 = W_2 = W$.

4.3.2 *Unequal Widths in Geometry Two*

Due to the reasons mentioned in the previous subsection, no more than two conductors are considered for Geometry Two. Let Conductor 0 be the only active conductor. Far-end voltage on conductor 1 for $W_0 = 1$ micron is plotted versus $s0$ in Figure 4-21. Three cases — $W_1 = 1$, 3, and 10 microns are considered. $W_0 = W_1 = W = 1$ micron curve has the maximum voltage for a given $s0$. Therefore, maximum FLS can be calculated from the $W = 1$ micron curve.

In Figure 4-22, $W_0 = 2$ microns for the dotted and the dashed curves; while, in Figure 4-23, $W_0 = 3$ microns for the dotted and the dashed curves. In both the figures, $W_0 = W_1 = W_2 = 1$ micron for the solid-line curve. It is noticed from both the figures that the far-end voltage on conductor 1 is maximum for a given value of $s0$ when $W_0 = W_1 = W = 1$ micron. Thus, the maximum value of FLS can be obtained from the $W = 1$ micron curve.

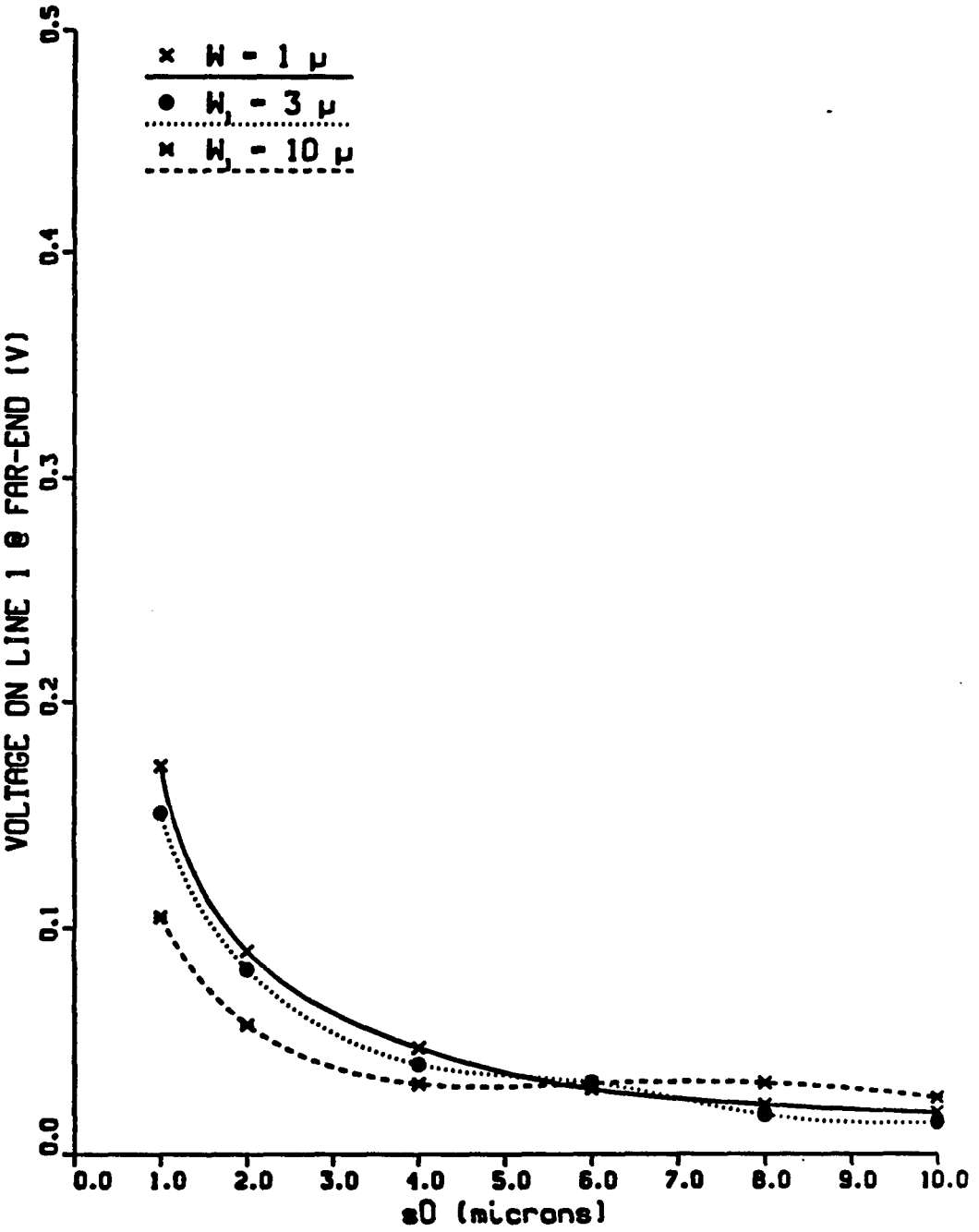


Figure 4-21 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for W_1 = 1, 3, and 10 microns. Two-conductor case of Geometry Two. W_0 = 1 micron.

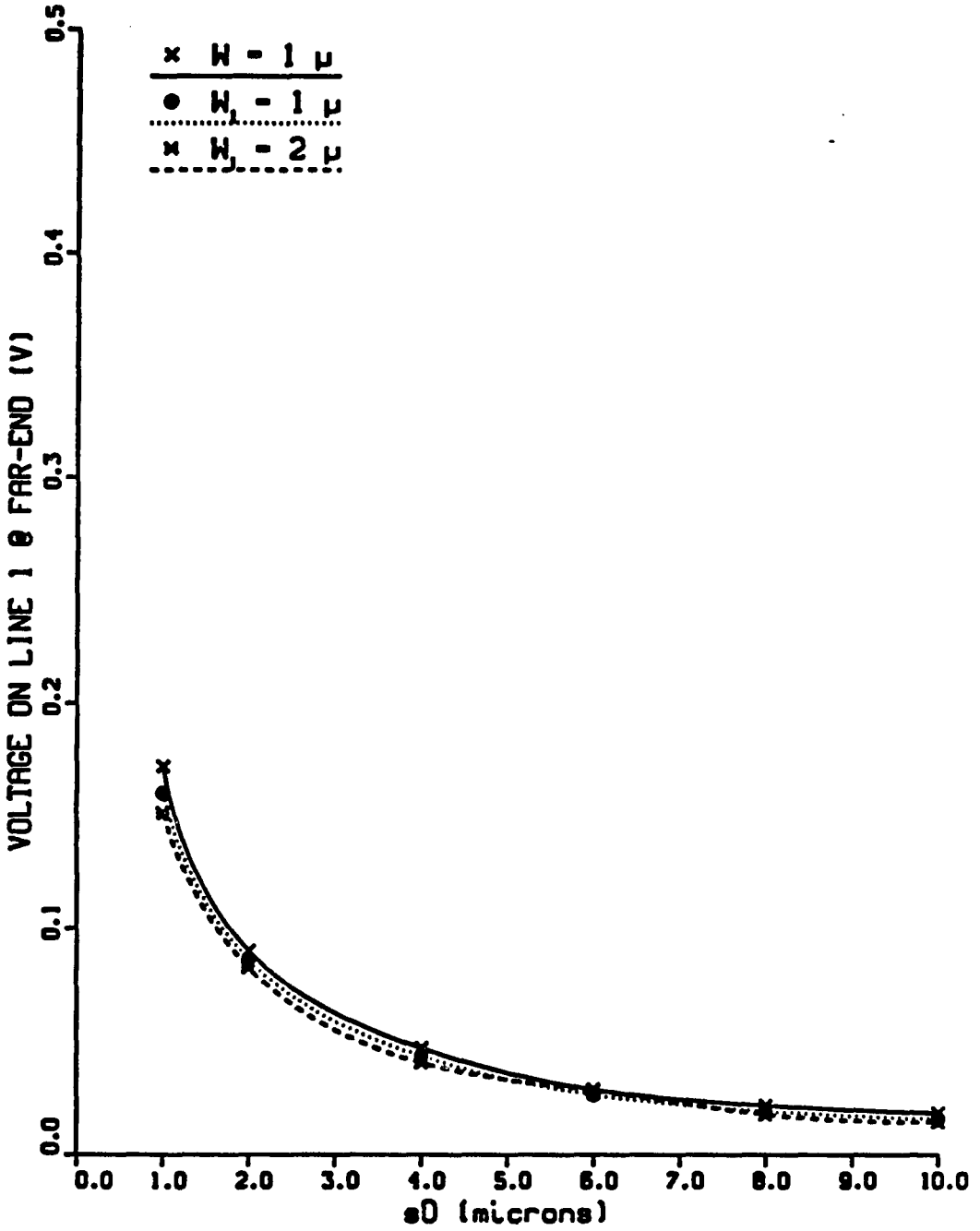


Figure 4-22 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for two-conductor case of Geometry Two. In solid-line case, W_0 = W_1 = 1 micron. W_0 = 2 microns for the other two cases and W_1 equals 1 and 2 microns for the dotted-line and the dashed-line respectively.

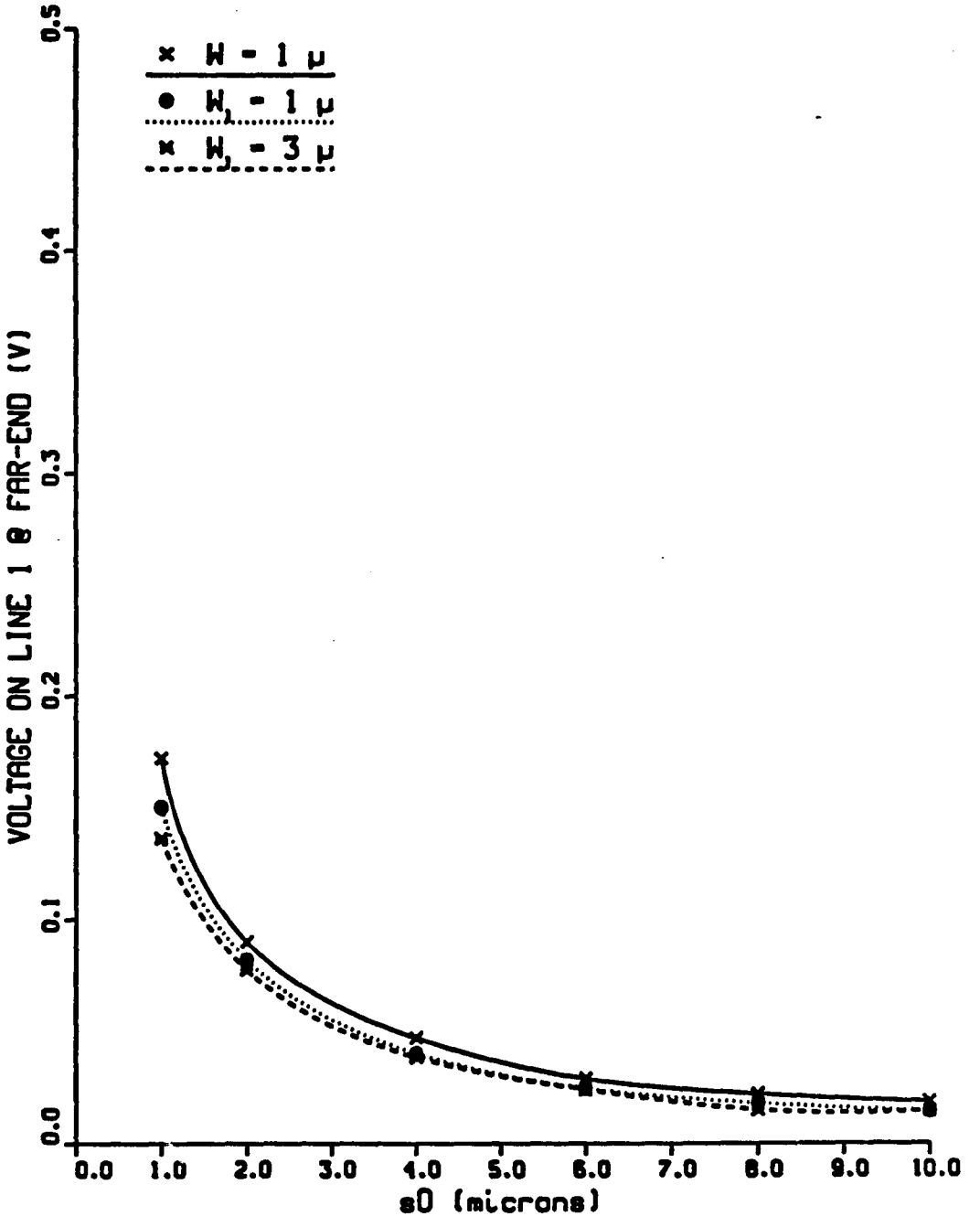


Figure 4-23 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for two-conductor case of Geometry Two. In solid-line case, W_0 = W_1 = W = 1 micron. W_0 = 3 microns for the other two cases and W_1 equals 1 and 3 microns for the dotted-line and the dashed-line respectively.

4.4 Analysis of Geometry Three

The $(n+1)$ conductors case for Geometry Three is presented in Figure 4-24. It is similar to the previous geometries except that the conductors are at a distance of 10 microns from the ground plane and 9 microns from the dielectric interface. In such a geometry the effect of the dielectric surface and the ground plane is muted enough to allow more than 0.1 V on conductor 4 (in a five-conductor case — conductor 0 being the active conductor) under certain conditions.

4.4.1 *Variation of Width in Geometry Three*

Only cases involving conductors of equal widths are considered in this subsection. Conductor 0 is the only active conductor. The experimental results for the two-conductor case are presented in Figure 4-25. The voltage on conductor 1 is plotted versus $s0$ for three cases — $W_0 = W_1 = W = 1$, 2, and 4 microns. It is noticed that the three curves are quite close and therefore, the use of $W = 1$ micron curve to get the maximum value of FLS should not give too much error.

Figure 4-26 presents the three-conductors case for $W_0 = W_1 = W_2 = W = 1$, 2, and 4 microns. $s0$ is fixed at 1 micron. It is noticed that the voltage on conductor 2 is maximum for a given $s1$ when $W = 1$ micron. Thus, maximum SLS can be obtained from $W = 1$ micron curve. The curves for four-conductors case are presented in Figure 4-37. $s0 = s1 = 1$ micron. Again, three cases, $W_0 = W_1 = W_2 = W_3 = W = 1$, 2, and 4 microns, are considered. The far-end voltage on conductor 3 is found to be maximum for a given $s2$ when $W = 1$ micron. Thus, maximum TLS (Third-Line Separation) can be obtained from the $W = 1$ micron curve. The curves for a five-conductor case are presented in Figure 4-28. $s0 = s1 = s2 = 1$ micron. $W_0 = W_1 = W_2 = W_3 = W_4 = W$. Three cases — $W = 1$, 2, and 4 microns, are considered. It is noticed that the far-end voltage on conductor 4 is maximum for a given value of $s3$ when $W = 1$ micron. Thus, the maximum

value of FOLS (FOurth-Line Separation) can also be obtained from the $W = 1$ curve.

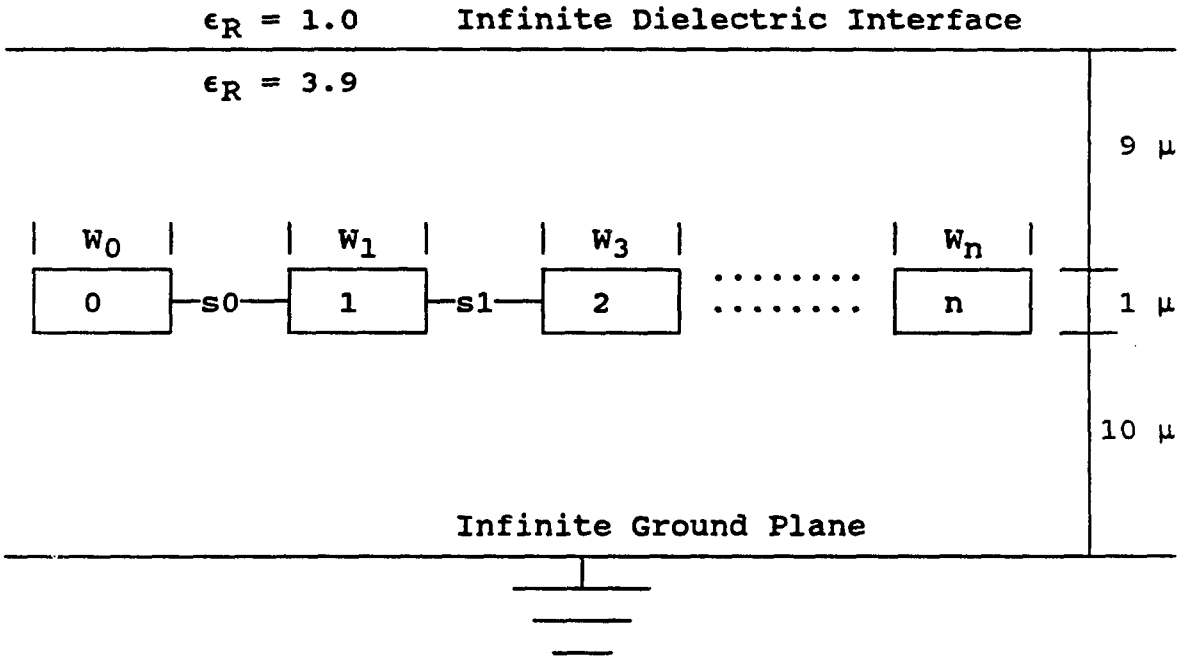


Figure 4-24 Cross-section of Geometry 3 for (n + 1) conductor case. Conductor 0 is the only active conductor. Conductors, buried in Silicon - dioxide, are at a distance of nine microns from the dielectric surface and ten microns from the ground plane. The thickness of each conductor is one micron.

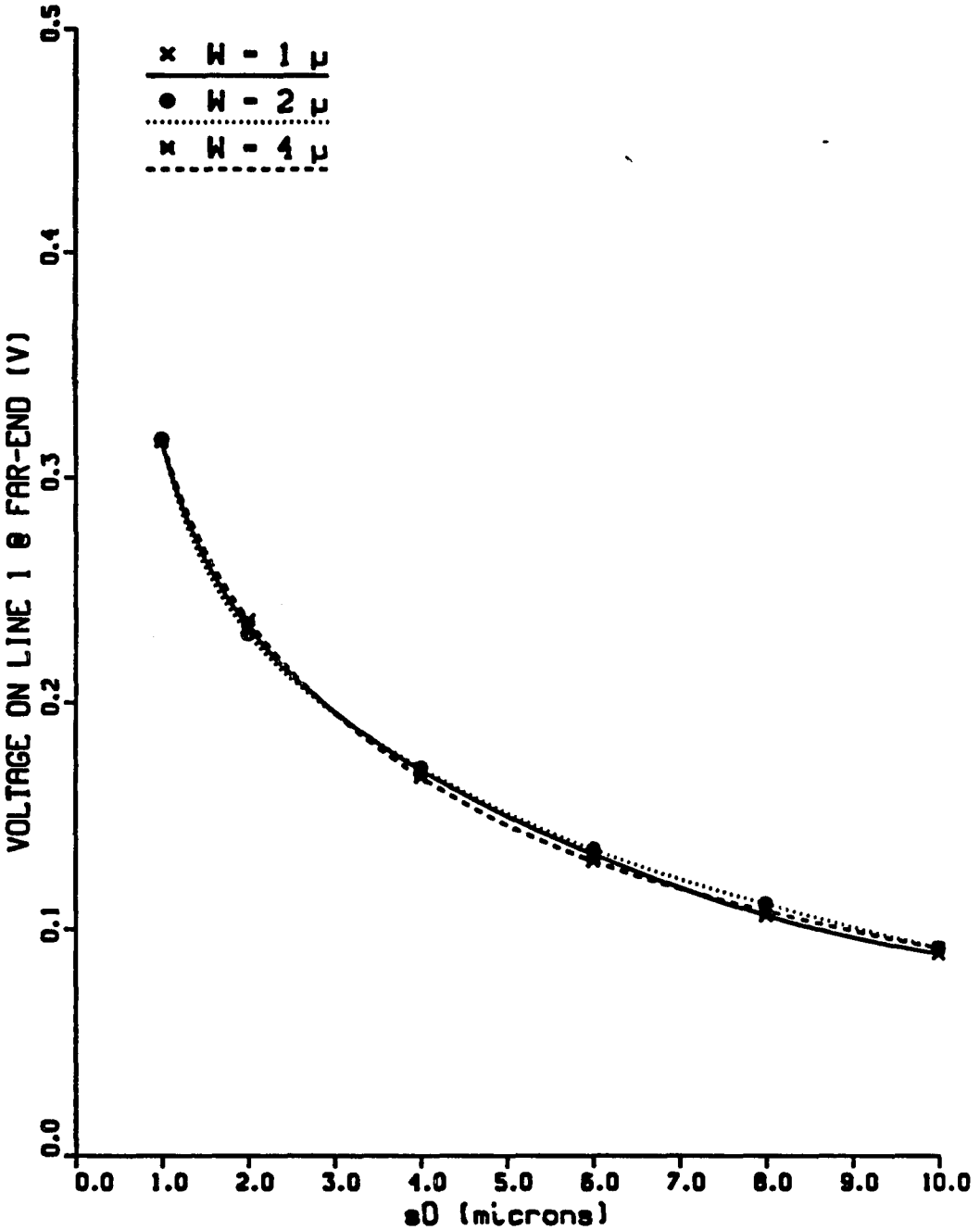


Figure 4-25 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for W = 1, 2, and 4 microns. Two-conductor case of Geometry Three. $W_0 = W_1 = W$.

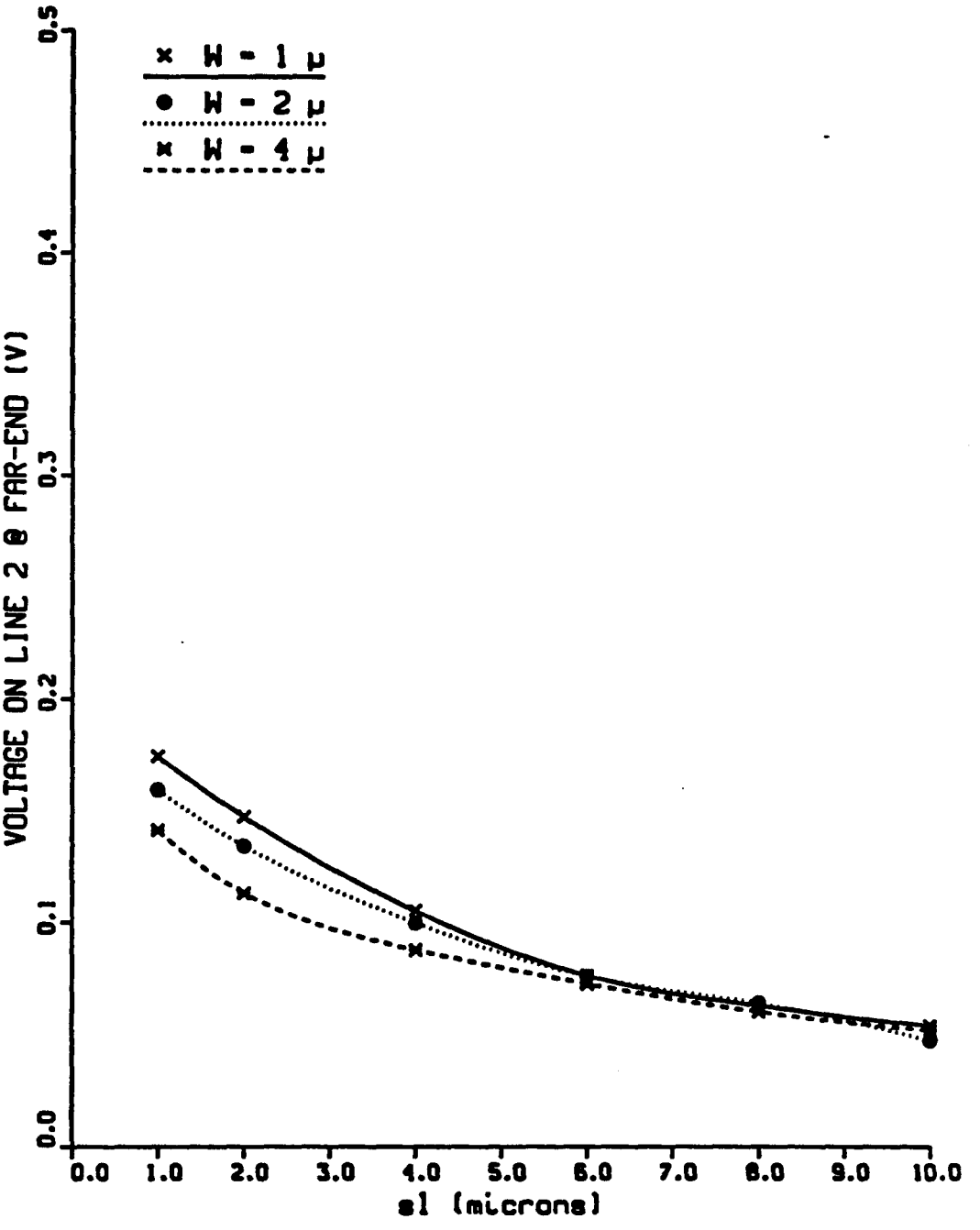


Figure 4-26 Voltage on conductor 2 versus s1, spacing between conductors 1 and 2, for W = 1, 2, and 4 microns. Three-conductor case of Geometry Three. $W_0 = W_1 = W_2 = W$. s0 = 1 micron.

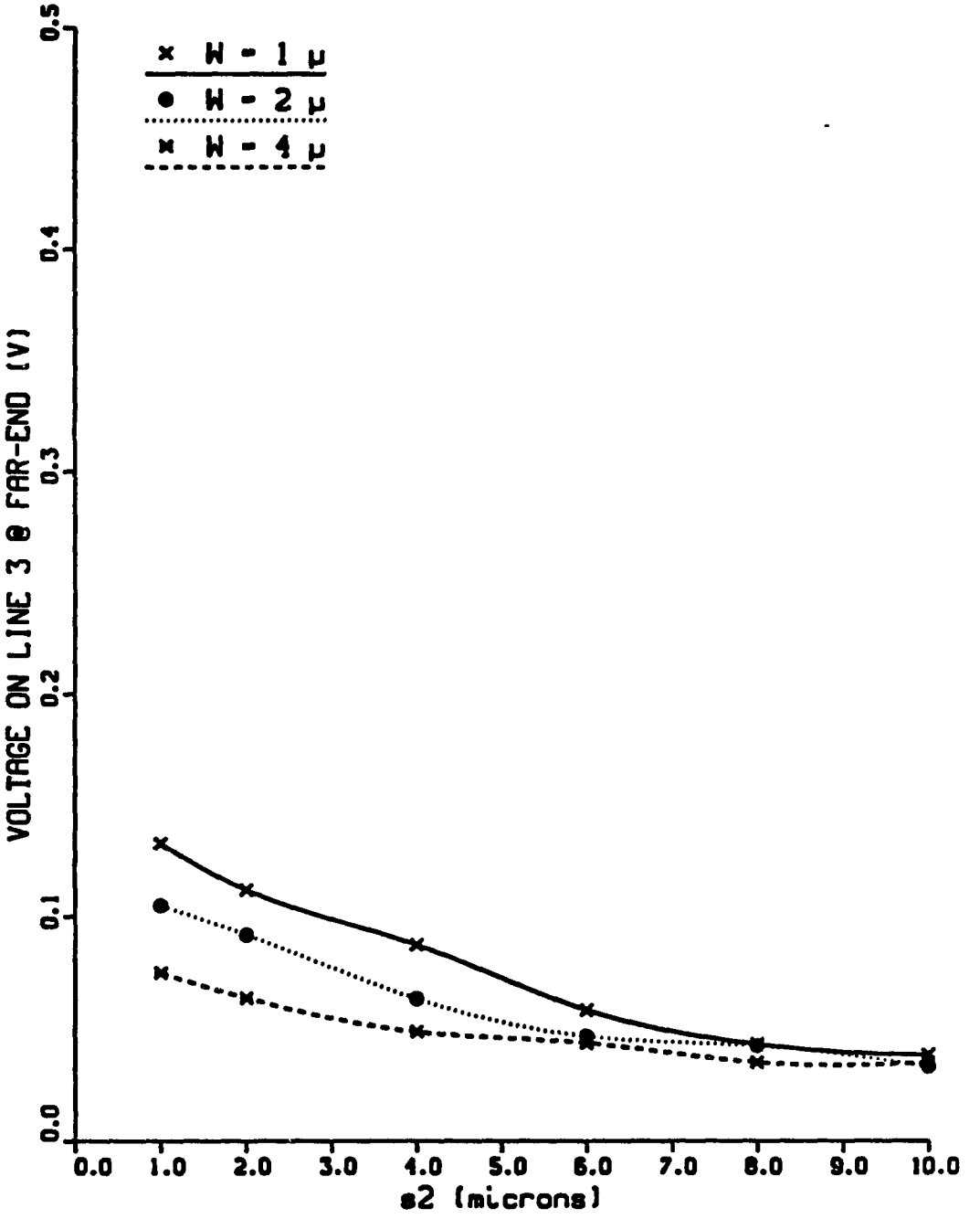


Figure 4-27 Voltage on conductor 3 versus s2, spacing between conductors 2 and 3, for W = 1, 2, and 4 microns. Four-conductor case of Geometry Three. $W_0 = W_1 = W_2 = W_3 = W$. s0 = s1 = 1 micron.

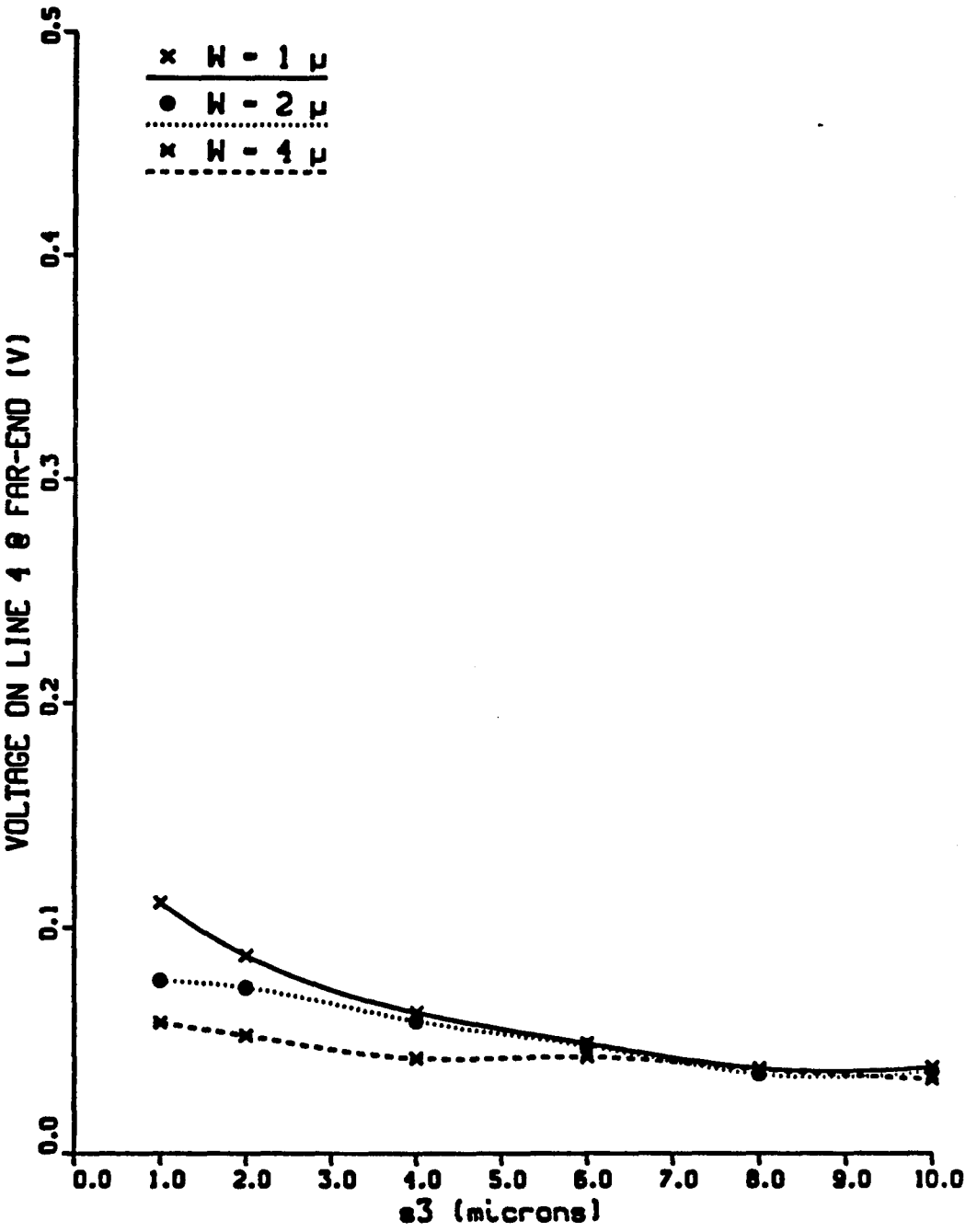


Figure 4-28 Voltage on conductor 4 versus s3, spacing between conductors 3 and 4, for W = 1, 2, and 4 microns. Five-conductor case of Geometry Three. $W_0 = W_1 = W_2 = W_3 = W4 = W$. $s0 = s1 = s2 = 1$ micron.

4.4.2 *Unequal Widths in Geometry Three*

Five figures are presented in this subsection. Let Conductor 0 be the only active conductor. The first three figures present results for two-conductors case while the other two present results for three-conductors case.

Results for the two-conductors case are presented in Figure 4-29, Figure 4-30, and Figure 4-31. The solid-line curve in all the three figures corresponds to $W_0 = W_1 = 1$ micron. The dotted-line and the dashed-line curves correspond to $W_0 = 1$, 2, and 3 microns for Figure 4-29, Figure 4-30, and Figure 4-31, respectively.

In Figure 4-29, $W_0 = 1$ micron. Three cases of $W_1 = 1$, 2, and 4 microns are considered. The curves are found to be very close. Thus, $W = 1$ micron curve can be utilized to get the maximum value of FLS.

In Figure 4-30, $W_0 = 2$ microns for the dotted-line and the dashed-line curves. $W_0 = W_1 = W = 1$ micron for the solid-line curve. $W_1 = 1$, and 2 microns for the dotted-line and the dashed-line, respectively. It is again noticed that $W = 1$ micron curve can be used to give the maximum value of FLS.

In Figure 4-31, $W_0 = 3$ microns for the dotted-line and the dashed-line curves. A similar arrangement exists for this graph as for Figure 4-30, except $W_1 = 4$ microns instead of 2 microns for the dashed-line curve.

Far-end voltage on conductor 2 is plotted versus $s1$ for a three- conductors case in Figure 4-32. Results for the three-conductors case are presented in Figure 4-32. $s0 = 1$ micron. $W_0 = 1$ micron and $W_2 = 1$, 2, and 4 microns. Until the voltage on conductor 2 drops below 0.1 V, it is noticed that the $W_0 = W_1 = W = 1$ micron curve gives the maximum voltage for a given value of $s0$. Therefore, maximum SLS can be found from $W = 1$ micron curve.

In Figure 4-33, the solid line curve corresponds to $W_0 = W_1 = W = 1$ micron. $W_0 = 2$ microns for the other two cases. Again it is noticed that $W = 1$ micron curve corresponds to the maximum far-end voltage on conductor 2 for

a given value of $s1$. Thus, maximum SLS can be obtained from $W = 1$ micron curve.

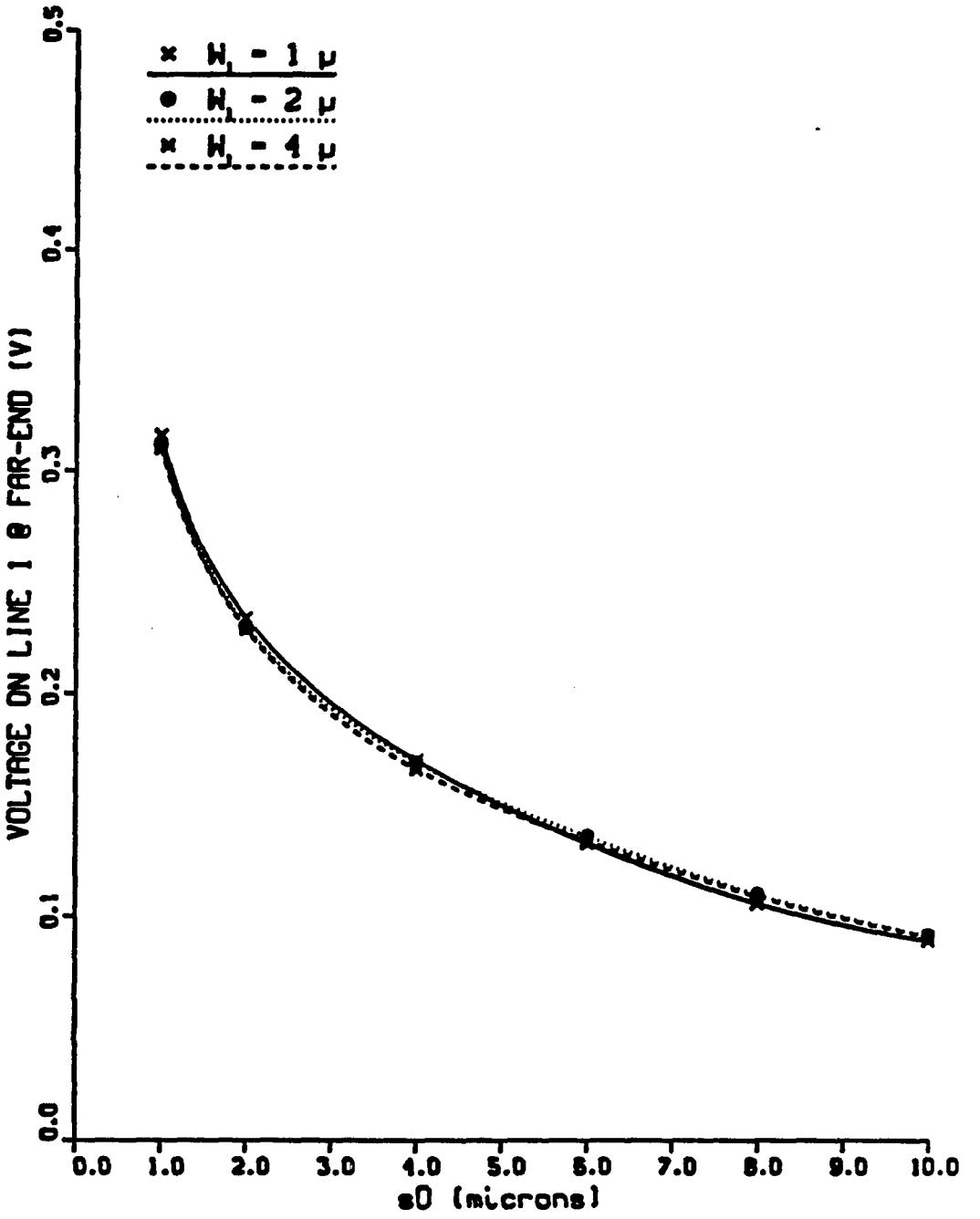


Figure 4-29 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for W_1 = 1, 2, and 4 microns. Two-conductor case of Geometry Three. W_0 = 1 micron.

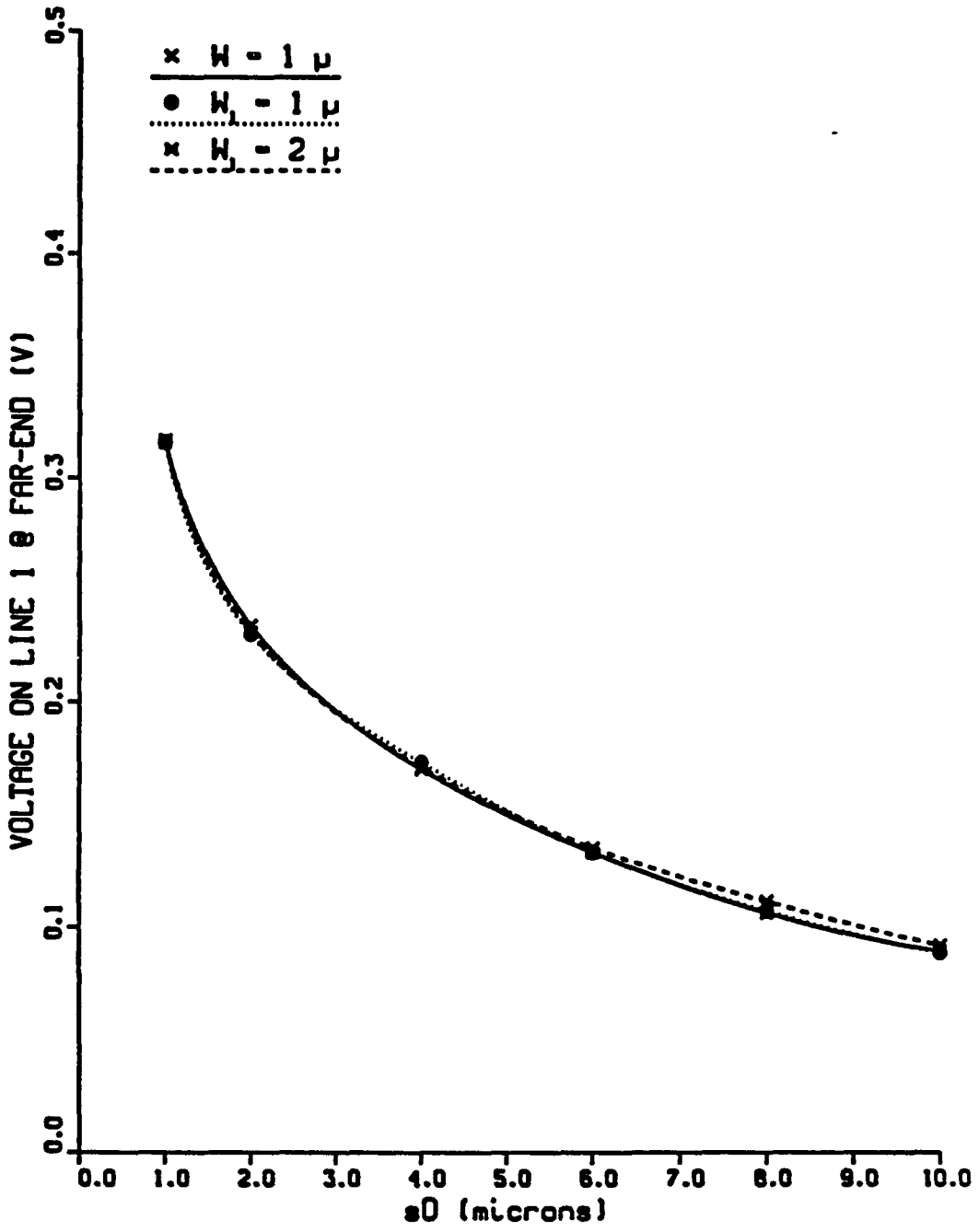


Figure 4-30 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for two-conductor case of Geometry Three. In solid-line case, W_0 = W_1 = 1 micron. W_0 = 2 microns for the other two cases and W_1 equals 1 and 2 microns for the dotted-line and the dashed-line respectively.

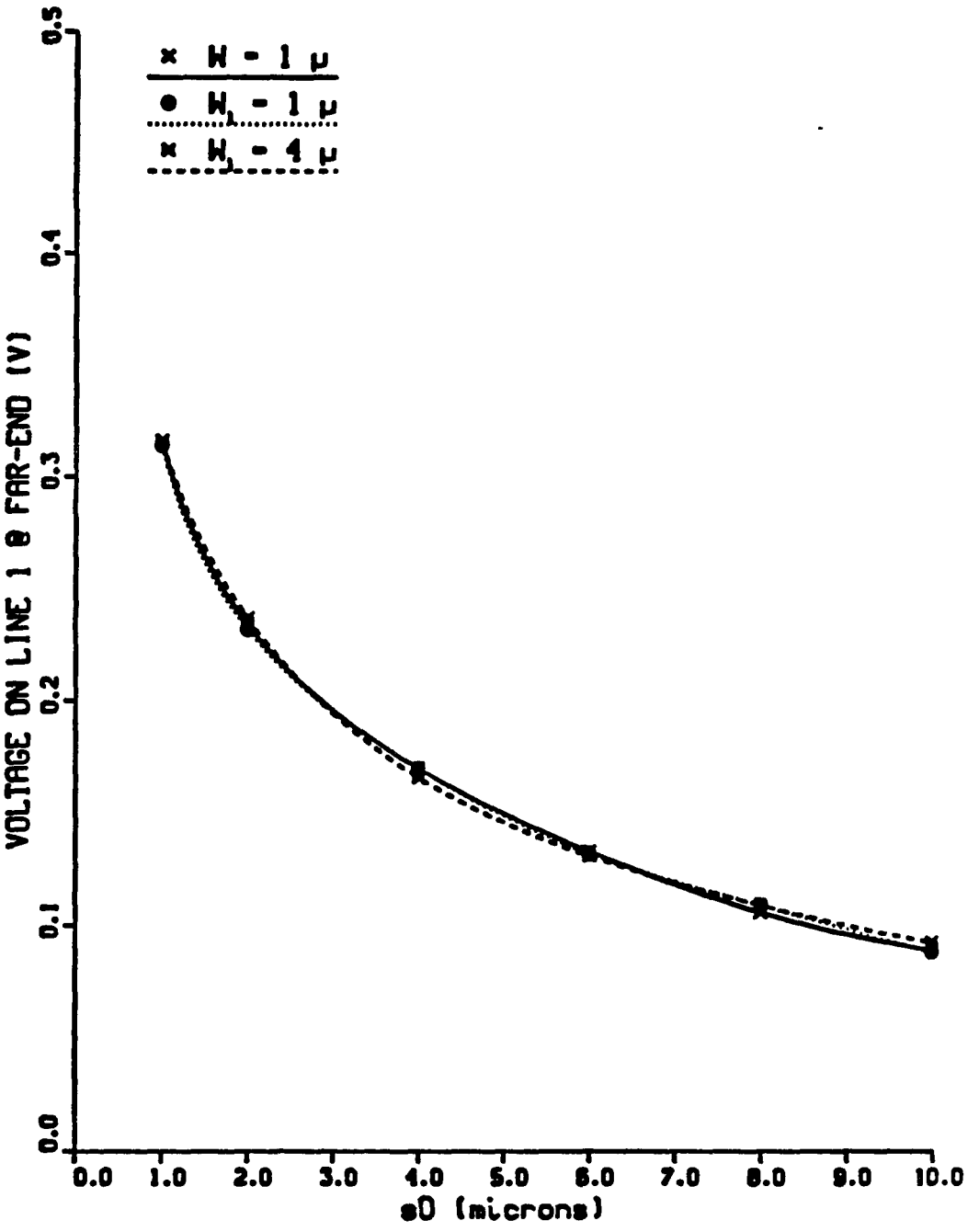


Figure 4-31 Voltage on conductor 1 versus s0, spacing between conductors 0 and 1, for two-conductor case of Geometry Three. In solid-line case, $W_0 = W_1 = W = 1$ micron. $W_0 = 3$ microns for the other two cases and W_1 equals 1 and 4 microns for the dotted-line and the dashed-line respectively.

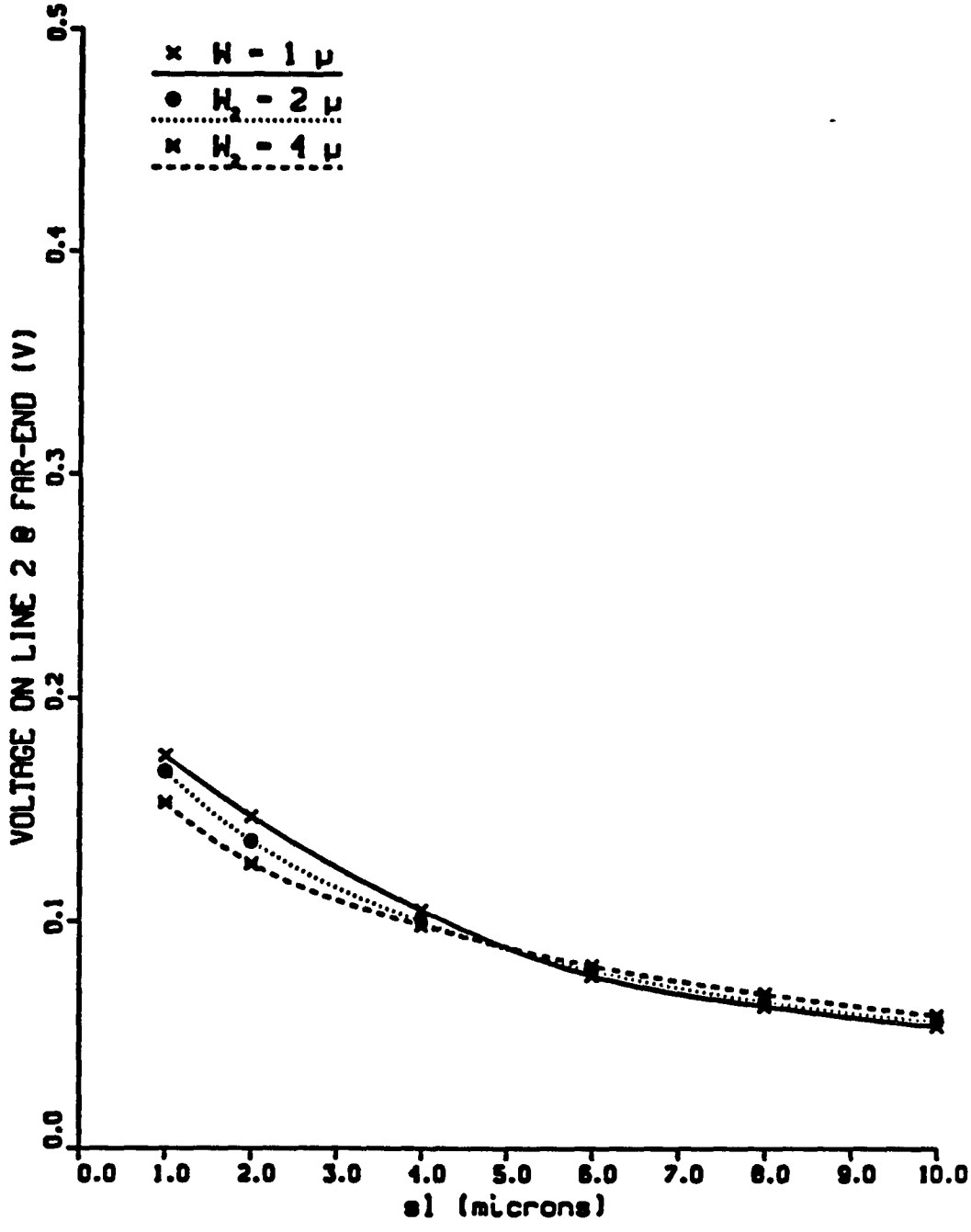


Figure 4-32 Voltage on conductor 2 versus s1, spacing between conductors 1 and 2, for three-conductor case of Geometry Three. $W_0 = W_1 = 1$ micron. W2 = 1, 2, and 4 microns. s0 = 1 micron.

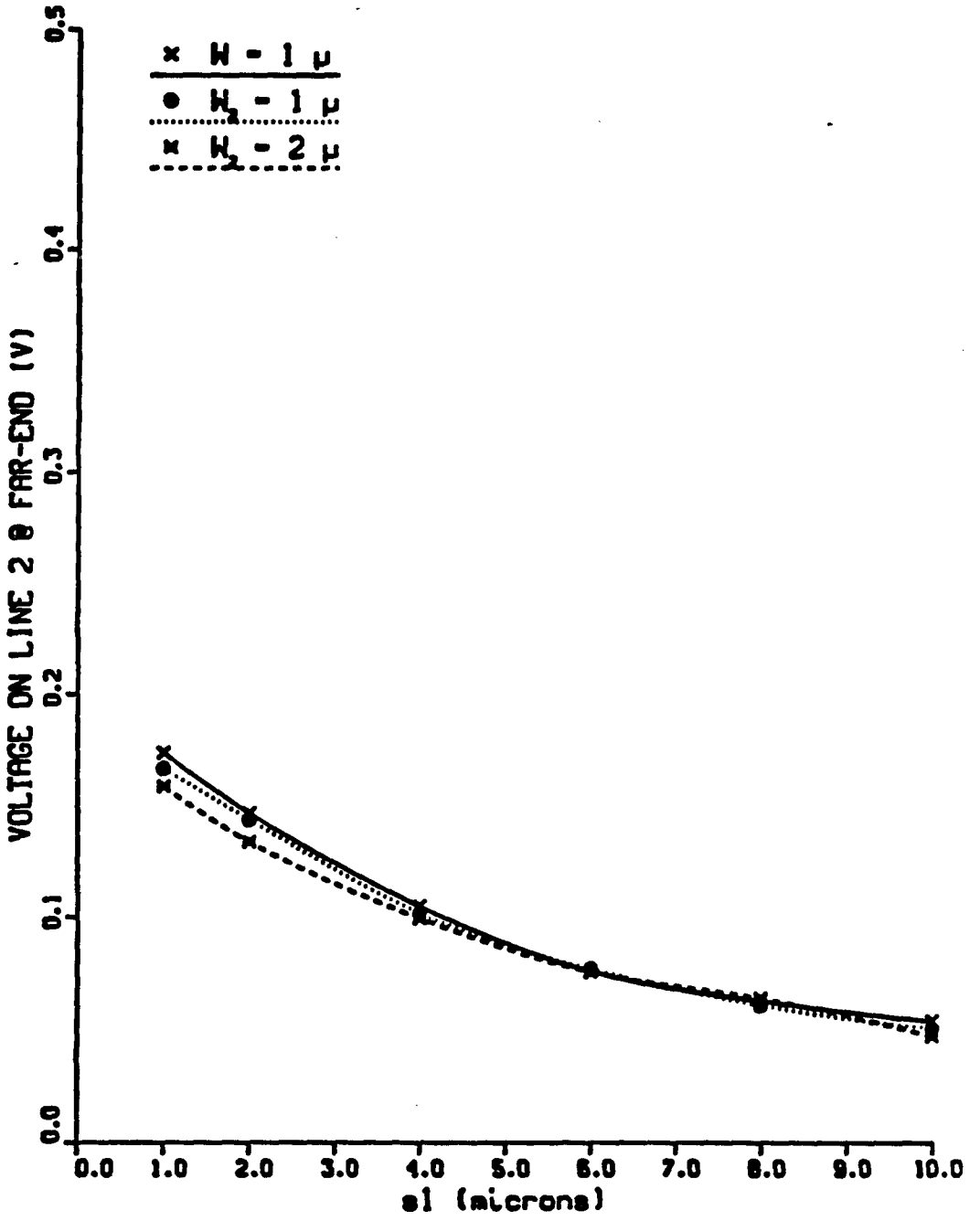


Figure 4-33 Voltage on conductor 2 versus s1, spacing between conductors 1 and 2, for three-conductor case of Geometry Three. In solid-line case, $W_0 = W_1 = W_2 = W = 1$ micron. $W_0 = W_1 = 2$ microns for the other two cases and W_2 equals 1 and 2 microns for the dotted-line and the dashed-line respectively. s0 = 1 micron.

4.5 Conclusion

Based on results presented in Section 4.2.1 it is recommended that to get the worst-case values of FLS and SLS, shieldings should be ignored. Sections 4.2, 4.3, and 4.4 suggested that FLS, SLS, TLS, e.t.c are biggest when the lines have the smallest possible width. Depending on the geometry, voltage on even the sixth conductor away from the active conductor may have a voltage greater than 0.1 V. Whatever the case, FLS, SLS, TLS (third-line separation), e.t.c should be calculated for minimum allowed widths of the conductors and domain truncation done on their basis.

CHAPTER 5

CONCLUSION

The theory behind UAC and UACSL was discussed in Chapter 2 and Chapter 3 respectively. Chapter 4 contains the results of extensive simulations carried out on primarily two basic geometries. A philosophy regarding Analysis Domain Truncation was developed and presented in Chapter 4. Basically, the gist of the discussion was that the worst-case distances at which conductors should be chopped off, should be derived from studying conductors which have the minimum possible width.

Several assumptions were made. It was assumed that the minimum allowed width is one micron. The lines are assumed to be of uniform thickness and rectangular in shape. Of course, it was assumed that the mode of propogation was either TEM or quasi-TEM. Only linear termination networks were considered. Only one conductor was assumed to be active at a time. Finally, the assumption that all the conductors lie in either horizontal or the vertical plane was made.

More research could be done by reducing the minimum dimension below one micron and observing the effects. The number of active conductors should be made more than one. Geometries containing more than two dielectric layers should be studied. For a better but may be more complex theory it is recommended that future work allow the presence of conductors in planes other than the vertical and the horizontal plane. It is recommended that a new tool, UANTL, developed at the University of Arizona be used to study nonlinear terminal networks to get a more accurate theory for CMOS networks. Finally, it is recommended that a

transmission-line simulator which allows periodic waveforms be used as the signals in practical world are periodic.

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