

INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps. Each original is also photographed in one exposure and is included in reduced form at the back of the book.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

U·M·I

University Microfilms International
A Bell & Howell Information Company
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
313/761-4700 800/521-0600

Order Number 1349120

Time-interval quantization in a high-density optical data storage system

Tehranchi, Babak, M.S.

The University of Arizona, 1992

U·M·I
300 N. Zeeb Rd.
Ann Arbor, MI 48106

TIME-INTERVAL QUANTIZATION IN A HIGH DENSITY OPTICAL DATA
STORAGE SYSTEM

by

Babak Tehranchi

A Thesis Submitted to the Faculty of the
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
In Partial Fulfillment of the Requirements
For the Degree of
MASTER OF SCIENCE
WITH A MAJOR IN ELECTRICAL ENGINEERING
In the Graduate College
THE UNIVERSITY OF ARIZONA

1992

STATEMENT BY AUTHOR

This thesis has been submitted in partial fulfilment of requirements for an advanced degree at The University of Arizona and is deposited in the University Library to be made available to borrowers under rules of the library.

Brief quotations from this thesis are allowable without special permission, provided that accurate acknowledgment of the source is made. Requests for permission for extended quotation from or reproduction of thesis manuscript in whole or in part may be granted by the head of the major department or the Dean of the Graduate College when in his or her judgment the proposed use of the material is in the interests of scholarship. In all other instances, however, permission must be obtained from the author.

SIGNED: Balab Telli

APPROVAL BY THESIS DIRECTOR

This thesis has been approved on the date shown below:

Ming-Kang Liu
Ming-Kang Liu
Assistant Professor of
Electrical and Computer Engineering

6/12/92
Date

ACKNOWLEDGEMENTS

Special thanks are due to Professor Max Liu for his guidance and patience throughout this project. I am also grateful to Professor M. Mansuripur for equipment support and technical discussions, and to Professor R. Kostuk for the use of laboratory facilities. The author also wishes to thank Sunil Gupta for his assistance in this project. Finally, a note of thanks goes to my parents and my sister for their encouragement and interest.

TABLE OF CONTENTS

LIST OF FIGURES	6
ABSTRACT	8
1 Introduction	9
1.1 Signal Processing and ISI Considerations	11
1.2 Organization of This Thesis	12
2 Data Pattern Generation	14
2.1 Pattern Generation	14
2.1.1 Address Decoder	16
2.2 Pattern Regeneration and Recording	17
3 Peak Detection	19
3.1 Boundary Detection	19
3.1.1 Lowpass Filtering	21
3.1.2 Differentiation	26
3.1.3 Threshold Detection	28
4 Time-Interval Quantizer	34
4.1 Basic Operation	34
4.2 100 MHz Clock.....	35
4.2.1 Design	35
4.2.2 Construction	37
4.3 Quantization	38
4.3.1 Hold/Reset Generator	40
4.3.2 Counter Design	42

	5
4.4 Data Transfer	43
4.4.1 Address Decoder	43
4.4.2 Data Acquisition	45
4.5 Quantization Error	46
4.6 Experimental Verification	47
5 Experimental Setup and Results	49
5.1 Experimental Setup	49
5.2 Data Analysis	52
6 Conclusion and Discussion	56
APPENDIX A Pattern Generation	58
APPENDIX B Quantizer Circuitry	61
REFERENCES	69

LIST OF FIGURES

1.1	Magneto-Optic Recording.	10
1.2	Block Diagram of Mark Size Detection.	13
2.1	Data Pattern Generator.	15
2.2	Pattern Generator Decoding.	16
2.3	Cycle Generator.	18
3.1	Modified Peak Detection Technique.	20
3.2	Block Diagram of Peak Detection.	20
3.3	Second Order Lowpass Filter.	21
3.4	Component Values for Lowpass Filter.	23
3.5	Magnitude and Phase Plots of Second Order Filter.	24
3.6	Magnitude and Phase Plots of Fourth Order Filter.	25
3.7	(a) Practical Differentiator, (b) Frequency Response of the Differentiator.	27
3.8	Component Values for Differentiator.	28
3.9	Frequency Response of Differentiator.	29
3.10	Threshold Detector.	30
3.11	Readback Signal, Threshold Detector Output and Inverted First Derivative ($2\mu m$ spotsize).	32
3.12	Readback Signal, Threshold Detector Output and Inverted First Derivative ($1\mu m$ spotsize).	33
4.1	Time-Interval Quantizer.	35
4.2	(a) 100MHz Clock Circuitry, (b) Schematic of an ECL OR/NOR Gate.	36
4.3	(a) Block Diagram of the Quantizer, (b) Hold/Reset Timing Diagram.	39
4.4	(a) Hold Signal Generation, (b) Reset Signal Generation.	41

4.5	Hybrid Counter System.	42
4.6	Data Transfer to PC.	43
4.7	Decoder Circuitry.	44
4.8	Data Transfer Program.	46
4.9	Test Data for the Quantizer System.	48
5.1	Recorded Pseudo-Random Sequence.	49
5.2	Readback Signal ($2\mu m$ Spot Size).	50
5.3	Readback Signal ($1\mu m$ Spot Size).	51
5.4	Modified Pseudo-Random Sequence	52
5.5	SNR Graphs for Measured Mark Sizes.	54
5.6	AID Mark Size Detection System	55

ABSTRACT

A hardware system for investigating Intersymbol Interference (ISI) in an optical data storage system has been designed and constructed by the author. The system consists of a pattern generator which produces data patterns of variable lengths and bit rates to be recorded on the optical disk. Data marks of the readback signal are quantized by a high-speed clock-counter system, and transferred in parallel to a personal computer. SNR values for collected data are obtained by computing mark size deviations of the readback signal from the original marks. A pseudo-random pattern of 31 bits is used for calculating SNR values for different spot sizes. Finally, Additive Interleaving Detection (AID) technique is implemented to compute another set of SNR values. 3 to 5 dB SNR improvements are observed when the AID technique is used.

CHAPTER 1

Introduction

Optical data storage has become increasingly important in the past few years. A major application for optical storage is the secondary storage of information. In this sense, optical data storage is considered a suitable replacement for magnetic hard disks and storage tapes. Some of the advantages of optical disk systems over conventional magnetic disks include higher data storage density and removability of optical disks [1]. Another strength is that optical disks can support read-only, write-once-read-many (WORM), and erasable/rewritable modes of data storage all in one unit [1],[2]. A major drawback of optical storage systems is longer access times. This problem is largely due to the heavy head mass (~ 100 grams) compared to the light-weight head (5 to 10 grams) for magnetic disk systems [1].

In this thesis, an erasable/rewritable Magneto-Optical (M-O) disk system is used. The basic principles involved in recording, erasure, and read out of the signals in M-O systems can be understood as follows. Recording on a Magneto-Optical (M-O) disk takes place by heating the M-O medium and cooling it down in the presence of an external magnetic field. Fig. 1.1 illustrates the recording process. The coercivity of the M-O material disappears when its temperature is raised above the Curie Temperature, T_{curie} , of the medium. The heat required for this process is produced by a laser beam focused on the M-O thin film. As a result, the region that is heated above T_{curie} loses its previous magnetization. When the laser beam is turned off, this region cools back to the room temperature in the presence of a residual magnetic field. This field is usually supplied by an external

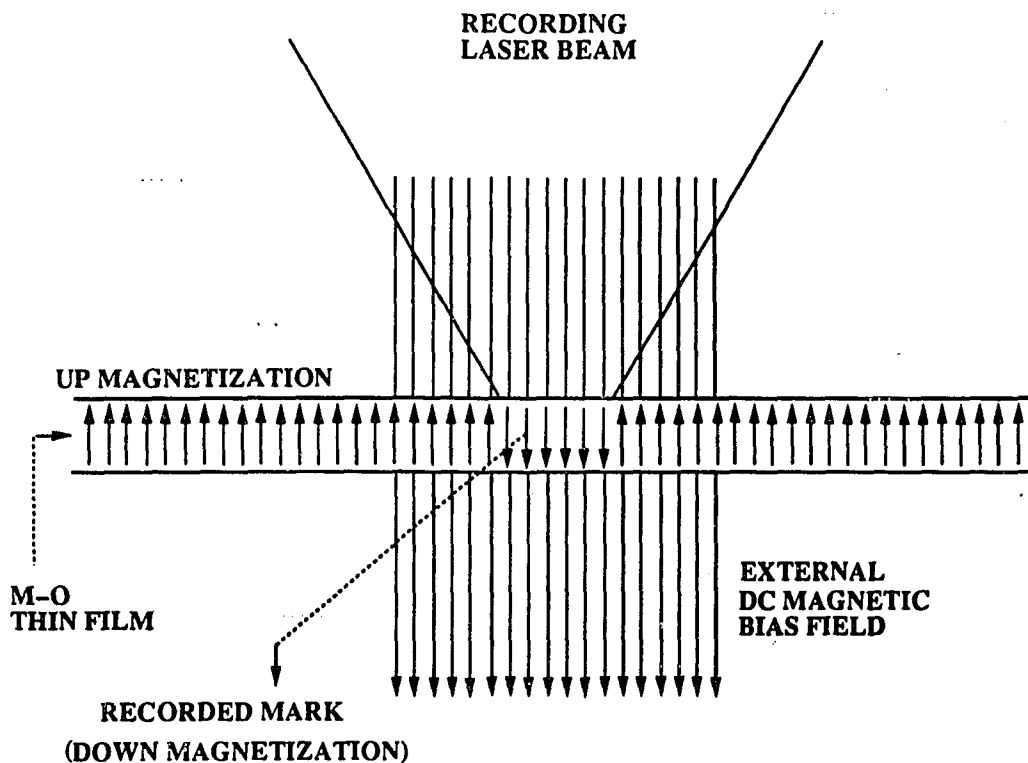


Figure 1.1: Magneto-Optic Recording.

bias magnet and it determines the new magnetization of the region. Erasure is done in a similar fashion except the external magnetic field is applied in the reverse direction.

Signal readback is performed optically using the Kerr or Faraday effects [1]. When an incident polarized laser beam is reflected by the magnetized medium, the reflected beam has an angle rotation in its polarization. The direction of this rotation depends on the magnetic polarization of the medium. Therefore, if the magnetized domains of the M-O film are reversed in polarity, the so-called Kerr angle is also reversed in direction. Detection of this angle in the readback process, leads to the recovery of the stored data bits.

1.1 Signal Processing and ISI Considerations

Higher storage densities in optical recording are often achieved by using modulation codes to store data bits. Modulation codes are used to map input binary bits to specific data patterns that are actually recorded. To fully understand their advantage, one can consider the following example. If a traditional NRZI code is used, data marks can only be integer multiples of the minimum mark size, d_0 , which corresponds to one bit. On the other hand, if a Run-Length-Limited code such as the so-called (2,7) code is used, the minimum mark size, d_0 , corresponds to 2+1 encoded bits. In other words, 3 encoded bits can be stored in the given minimum mark size. Therefore, the storage density is tripled. By including the coding inefficiency of 50%, the actual capacity is 1.5 times that of NRZI [3][4].

After the information bits are encoded, they are ready to be recorded on the optical disk. The process of recording, described in the previous section, introduces various noise elements in the recorded signal. These elements can alter the recorded marks so that the readback signal may be completely different from the original signal. Some of the noise introduced in this process is due to optical and media noise, laser power and beam width fluctuations, servo speed fluctuations, and Intersymbol Interference (ISI) [5].

ISI may contain two components. One is the ISI due to neighboring marks (traditional). In this case, only the two adjacent neighbors are considered and the ISI contributions from the remaining marks are assumed to be negligible. The second factor is the ISI due to the mark size itself, which is called pulse broadening (or shrinking) [6]. This combined ISI can significantly degrade the recorded signal and result in high error detection probabilities. Therefore, it is important to be able to characterize ISI in a M-O recording channel and use effective methods to reduce its adverse effects.

1.2 Organization of This Thesis

In order to investigate ISI, mark sizes of the readback signal must be detected and compared to the original marks. Peak detection techniques are traditionally used to determine the boundaries of a mark by generating two derivatives of the readback signal and detecting the zero-crossings of the second derivative [3].

Once boundaries are detected, mark sizes can be determined either by the traditional time window techniques [7],[8],[9], or by the time quantization method proposed in [5]. In the later technique, time marks are quantized to produce integer numbers proportional to duration of the marks. This quantization is accomplished by means of a high-speed clock-counter combination which is reset at every mark boundary. Therefore, time marks are converted into amplitude marks in this process. One of the advantages of time-mark quantization is that simple signal processing techniques can be used in subsequent steps to recover the recorded signal.

The remainder of this thesis examines hardware implementation for the scheme described above. Fig. 1.2 shows a block diagram of different stages involved in this process. Chapter 2 discusses how different data patterns are generated and recorded on the optical disk. In Chapter 3, peak detection circuitry is described in detail. This peak detection technique is a variation of the method described above. Chapter 4 describes the quantization process and the components involved in performing this task. In Chapter 5, some experimental results are discussed and Signal-to-Noise-Ratio (SNR) computations are performed on collected data. In addition, Additive Interleaving Detection (AID) of marks is presented and SNR values are compared to conventional SNRs. Finally, Chapter 6 presents the conclusion and discussion of some of the relevant issues. Appendices A and B provide detailed pin diagrams of digital logic circuits and some computer programs which are used for data acquisition.

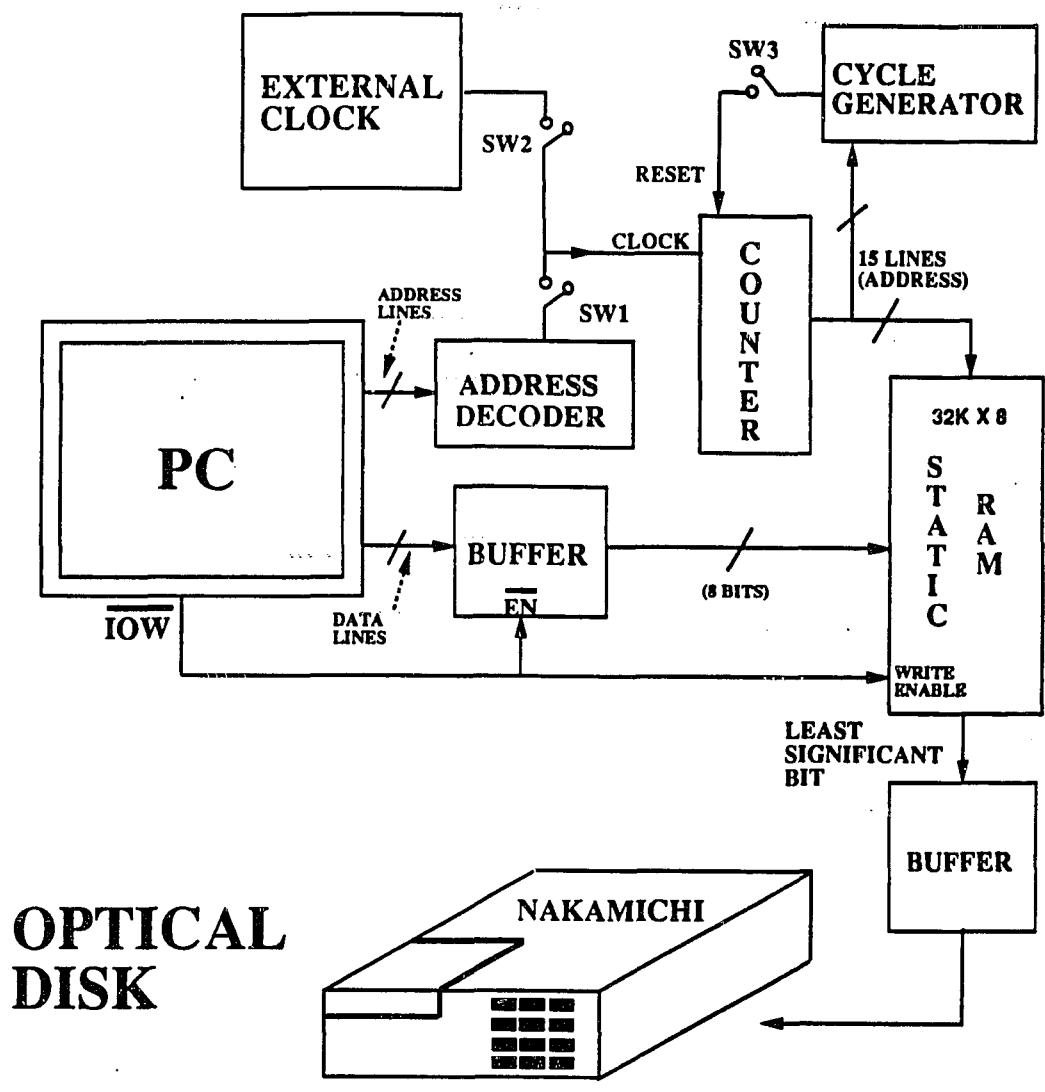
CHAPTER 2

Data Pattern Generation

The first step in ISI investigation is to generate various data patterns and record them on the optical disk. This requires a flexible pattern generator capable of producing variable length data patterns with adjustable mark sizes. A powerful pattern generation scheme can be realized by a combination of software and hardware implementations. The basic idea is to write a computer program to generate an arbitrary number of zeros and ones on a personal computer. These numbers are then transferred to a static RAM on the PC's interface board. The stored pattern is recorded on the optical disk as a continuous signal by means of an external clock. Fig. 2.1 shows a block diagram of this operation. A more detailed diagram of pattern generation and storage circuitry is shown in Appendix A.

2.1 Pattern Generation

A BASIC program is written to generate a sequence of zeros and ones. In order to transfer this pattern to the RAM, the cycle generator and external clock of Fig. 2.1 must be disconnected from the system. Dip switches on the interface board accomplish this task (SW2, SW3 off, SW1 on). The decoder output signal is used to increment the RAM address counter every time a byte of data is transferred. The computer transfers the data pattern into consecutive locations of the RAM. It should be noted that an I/O WRITE transfers 8 bits of data to the I/O port. However, only the least significant bit is used for recording purposes and



Data Generation : SW1 closed, SW2 & SW3 open.
Data Regeneration and Recording : SW1 open, SW2 & SW3 closed

Figure 2.1: Data Pattern Generator.

the remaining bits are discarded. A BASIC program used to generate a pseudo-random pattern is included in Appendix A.

2.1.1 Address Decoder

The IBM PC XT has 20 address lines on its I/O bus ($A0 - A19$). In the decoder design, only the first 10 lines are utilized. Therefore, any combination of $A10 - A19$ would access the I/O ports specified by the lower address lines. This is called redundant addressing and is similar to the I/O address decoding scheme used on the PC system board [16]. This saves extra circuitry required to decode the higher address lines. The I/O addresses $3E8 - 3EF$ were selected for the pattern generator and the quantizer system described in Chapter 4. Consulting the IBM Technical Manual reveals that these addresses are not used by standard devices in the PC, and can be used for external interface devices [17].

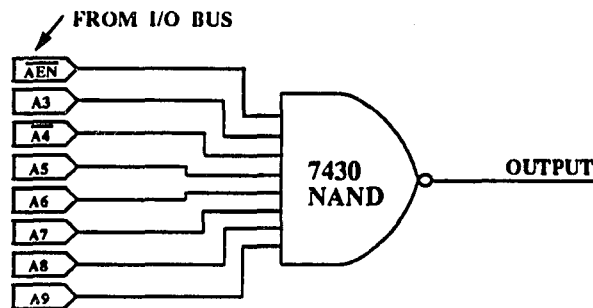


Figure 2.2: Pattern Generator Decoding.

The 8-input 7430 NAND gate, shown in Fig. 2.2, is used for decoding the I/O address lines. Output of the NAND gate is always high unless one of 8 addresses in the range $3E8 - 3EF$ is selected by an I/O READ or WRITE command. The Address Enable (\overline{AEN}) line is used to disable the decoder system during a Direct Memory Access (DMA) transfer. This line is normally low and it

becomes high to allow a DMA transfer. Addresses *3EA* and *3EE* may be used to access the static RAM of the pattern generator. The remaining 6 addresses are reserved for the quantizer circuitry of Chapter 4. The decoding scheme for the quantizer is more complex and requires additional circuitry. These modifications are discussed in Sec. 4.4.1.

2.2 Pattern Regeneration and Recording

Once the data bits are stored in the static RAM, it is necessary to record them as a continuous signal on the optical disk. The external clock and the cycle generator perform this task. First, the address decoder must be disconnected from the system since computer interaction is not required at this stage (SW2, SW3 on, SW1 off). An Hp 81131A Pulse Generator is used as the external clock. The clock rate can be varied as necessary to generate different bit rates.

The Cycle Generator of Fig. 2.3 determines the length of the recorded pattern (in bits). The desired length is selected by 15 dip switches located on the interface board. Depending on the state of these switches (either a '0' or a '1'), any cycle up to $2^{15} - 1 = 32767$ bits can be selected. A 15-bit comparator continually compares the counter output lines to this value. Whenever the two numbers match, a narrow pulse is generated and the counter is reset to zero. As a result, the address counter periodically counts from zero and terminates the count when its output has reached the number selected by the dip switches. This cyclic action is continued as long as the external clock is operating. At the same time, the RAM output and its buffer are enabled and the data pattern is recorded on the optical disk. Recording is done by a Nakamichi optical disk at a write power of 5.0 mw, read power of 1.8 mw, constant linear velocity of 4 m/s, with a diffraction limit of $1\mu m$.

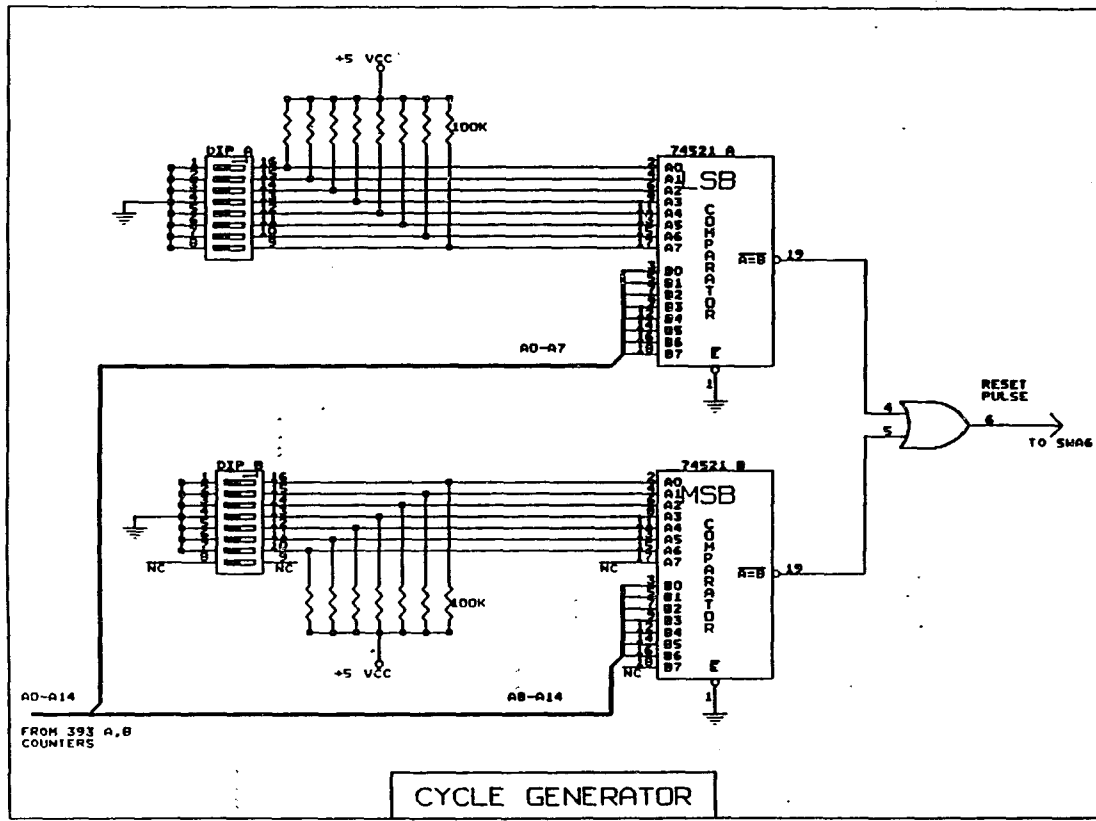


Figure 2.3: Cycle Generator

CHAPTER 3

Peak Detection

ISI introduced in the recorded signal can be measured by determining the mark sizes of the readback signal and comparing them to the original marks. In this chapter, mark sizes are estimated by detecting the boundaries of adjacent marks. The time interval between two such boundary signals would correspond to the mark size of the readback signal.

3.1 Boundary Detection

Boundary detection is often performed by finding the first and second derivatives of the readback signal. The zero crossings of the second derivative would then indicate the boundaries of neighboring marks. The above detection method requires two analog differentiations. Implementing this idea in hardware is quite challenging when narrow marks are being processed. An alternative detection method was used throughout this project. Fig. 3.1 illustrates the modified peak detection technique. In this process, the readback signal is differentiated once, and the peaks of the first derivative are used for estimating the boundary locations. Two threshold detectors are used to produce narrow pulses corresponding to the peaks of the differentiated signal. Fig. 3.2 shows a block diagram of peak detection.

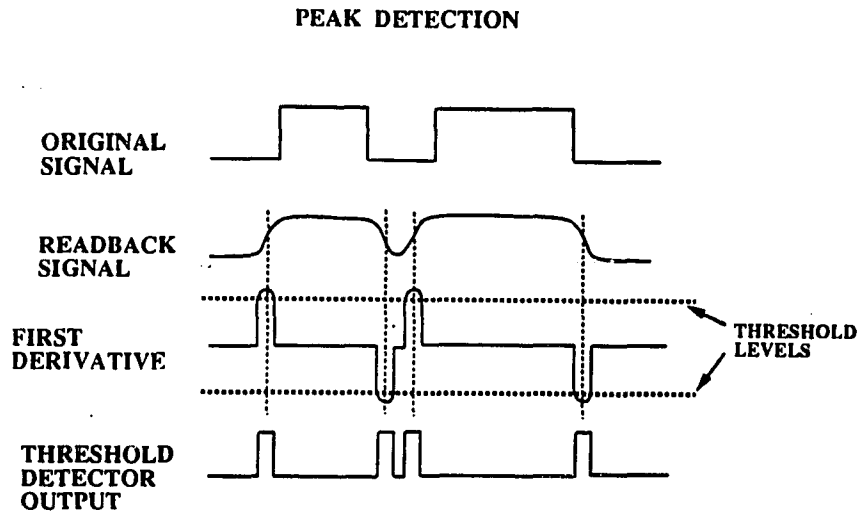


Figure 3.1: Modified Peak Detection Technique.

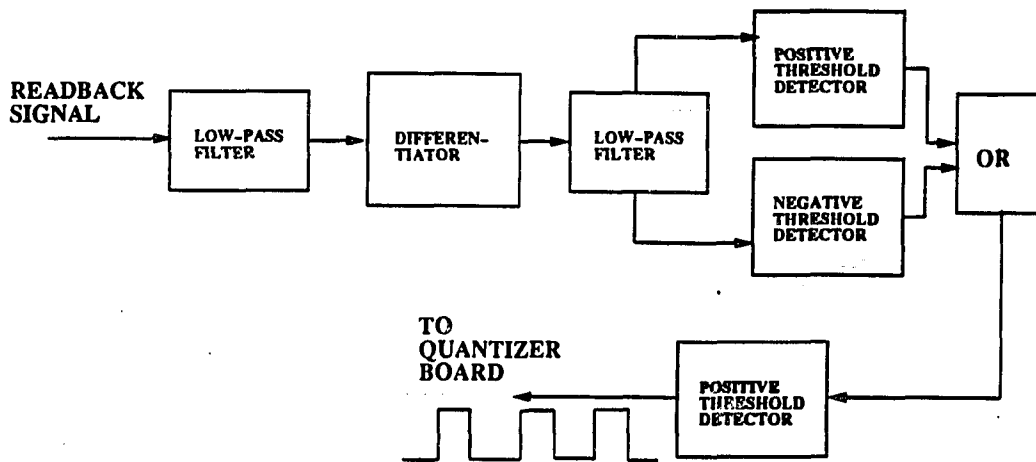


Figure 3.2: Block Diagram of Peak Detection.

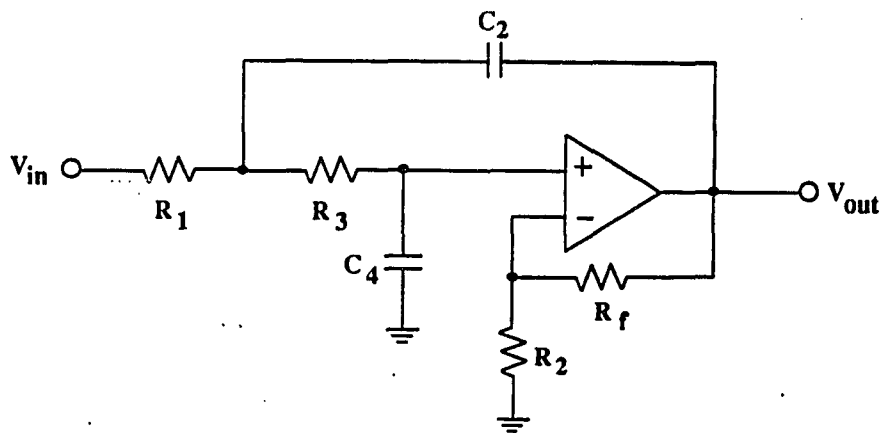


Figure 3.3: Second Order Lowpass Filter.

3.1.1 Lowpass Filtering

Lowpass filters are used to reduce excessive high frequency noise in the detector system. As depicted in Fig. 3.2, lowpass filtering is done at two stages in the peak detection process. A second order lowpass filter is used before differentiation and a fourth order lowpass filter is used after differentiation of the readback signal. Fig. 3.3 shows a schematic of a second order lowpass filter. Implementation of the fourth order filter is accomplished by cascading two second order filters. The transfer function for the second order filter is given by

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K/R_1 R_2 C_2 C_4}{s^2 + s(1/R_3 C_4 + 1/R_1 C_2 + 1/R_3 C_2 - K/R_3 C_4) + 1/R_1 R_3 C_2 C_4} \quad (3.1)$$

where

$$K = 1 + \frac{R_f}{R_2}. \quad (3.2)$$

The cutoff frequency of this filter is

$$\omega_n = \frac{1}{\sqrt{R_1 R_3 C_2 C_4}}. \quad (3.3)$$

The quality factor, Q , is determined by

$$\frac{1}{Q} = \sqrt{\frac{R_3 C_4}{R_1 C_2}} + \sqrt{\frac{R_1 C_4}{R_3 C_2}} + (1 - K) \sqrt{\frac{R_1 C_2}{R_3 C_4}}. \quad (3.4)$$

The design procedure for the lowpass filter is given in various textbooks [10],[11],[12]. The cutoff frequency of the filter was selected to eliminate high frequency noise components without compromising the integrity of the desired signal. Phase delay introduced in the signal was also kept to a minimum. In order to select a suitable cutoff frequency, the power spectrum of the readback waveform was obtained. This was accomplished by sampling the waveform with a digitizing oscilloscope, and transferring the data points to a personal computer [13]. The power spectrum of the waveform with smallest spot size ($0.8\mu m$) indicated that there are no frequency components above $\sim 750KHz$. Consequently, a cutoff frequency of about 7MHz was selected. The phase associated with this filter would start its rolloff at about one decade below the cutoff frequency (750KHz). As a result, frequency components of the desired signal would undergo a very small or zero phase shift.

The DC gain, K , of the filter was chosen as close to unity as possible. To simplify the design procedure, an *Equal-Resistance Equal-Capacitance* network was used where $C_1 = C_2$ and $R_1 = R_3$. The values obtained for various elements are listed in Fig. 3.4. The results of circuit simulation on MICROCAP are shown in Figures 3.5 and 3.6. These figures show magnitude and phase plots for the second order and fourth order lowpass filters. The results indicate desired amplitude and phase behavior at the frequencies of interest.

R_1	1.5K
R_3	1.5K
C_2	15 pF
C_4	15 pF
R_2	1k
R_f	100

f_n	7MHz
K	$1.1 \frac{V}{V}$
Q	0.526

Figure 3.4: Component Values for Lowpass Filter.

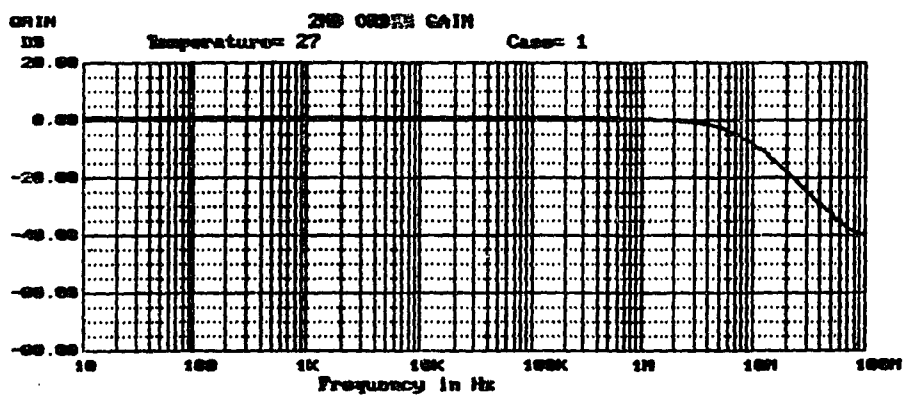
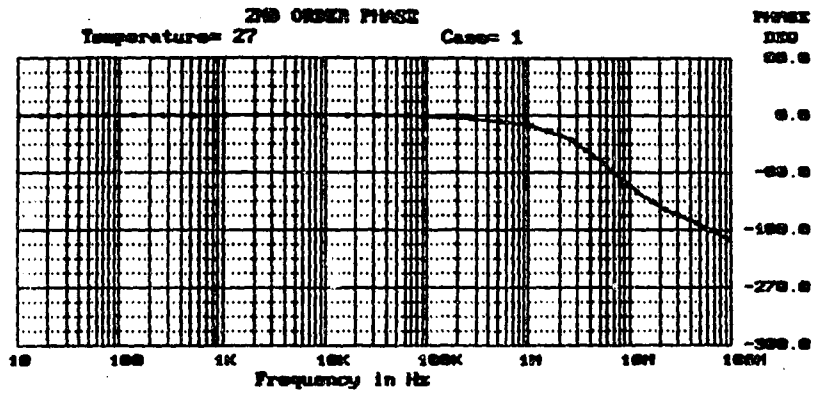


Figure 3.5: Magnitude and Phase Plots of Second Order Filter.

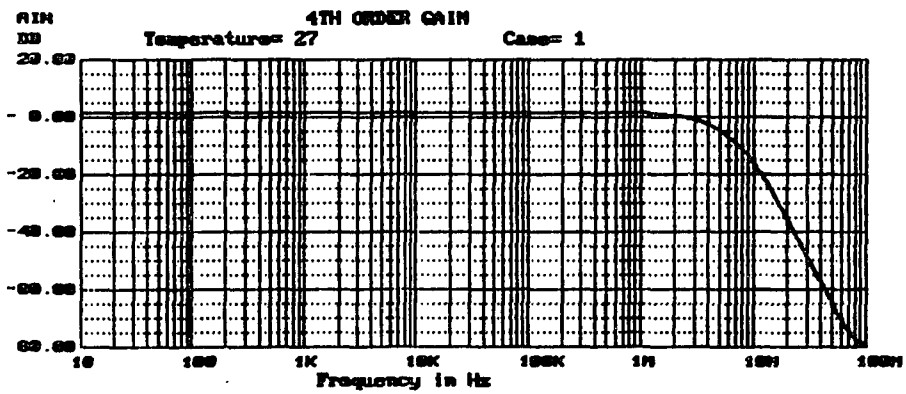
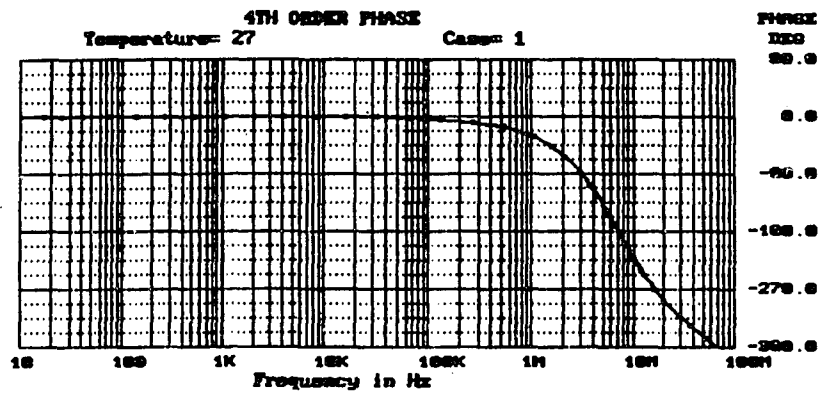


Figure 3.6: Magnitude and Phase Plots of Fourth Order Filter

3.1.2 Differentiation

An ideal differentiator produces an output which is precisely proportional to the derivative of its input signal. The basic circuit requires only an op amp plus C_1 and R_f shown in Fig. 3.7.a. A practical differentiator, however, requires additional components to reduce noise and instability inherent in the basic differentiator circuit. The addition of R_1 and C_f provides a 20 dB/dec rolloff at high frequencies. R_p is added to cancel the effects of the op amp input bias current and C_p is required to bypass the thermal noise of R_p to ground. A detailed discussion of various elements and their effects on differentiation is discussed in [12]. Fig. 3.7.b shows frequency response curves for the differentiator. The *Gain Bandwidth Product (GBP)* of the opamp used in this design is 75MHz. Therefore, the closed loop gain of the differentiator is not limited by the opamp GBP.

Equations 3.4-3.7 describe the relationships between different components and cutoff frequencies depicted in Fig. 3.7.b.

$$f_d = \frac{1}{2\pi R_f C_1} \quad (3.5)$$

$$f_{cp1} = \frac{1}{2\pi R_1 C_1} \quad (3.6)$$

$$f_{cp2} = \frac{1}{2\pi R_f C_f} \quad (3.7)$$

The overall transfer function of the differentiator is given by

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{sR_f C_1}{(1 + sR_1 C_1)(1 + sC_f R_f)} \quad (3.8)$$

From Eq. 3.7 and Fig. 3.7.b it is evident that differentiation occurs for the frequencies below f_{cp1} . Beyond this frequency the circuit acts as an amplifier with progressively lower gain at higher frequencies. Thus, high frequency noise is considerably reduced at the output of the differentiator. The negative sign in front of the transfer function indicates that the differentiator output is inverted.

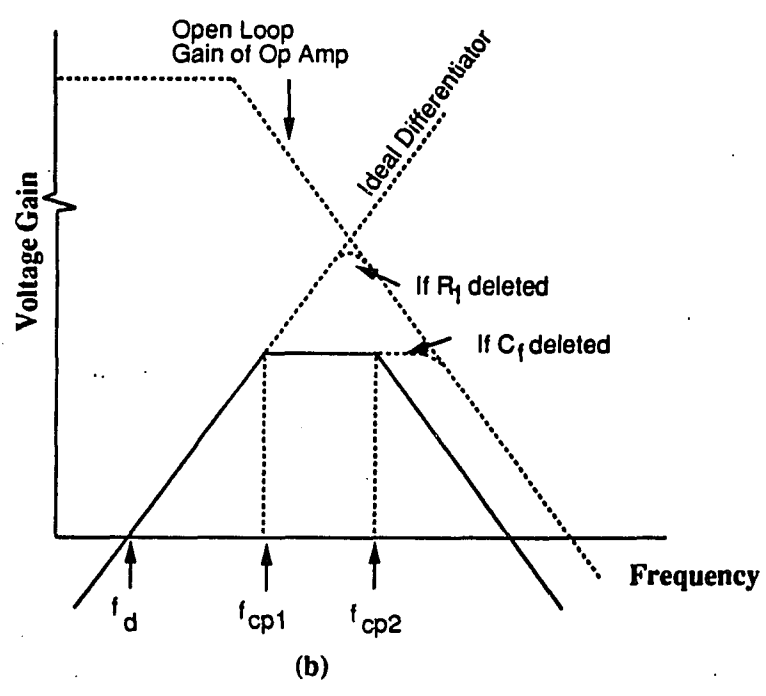
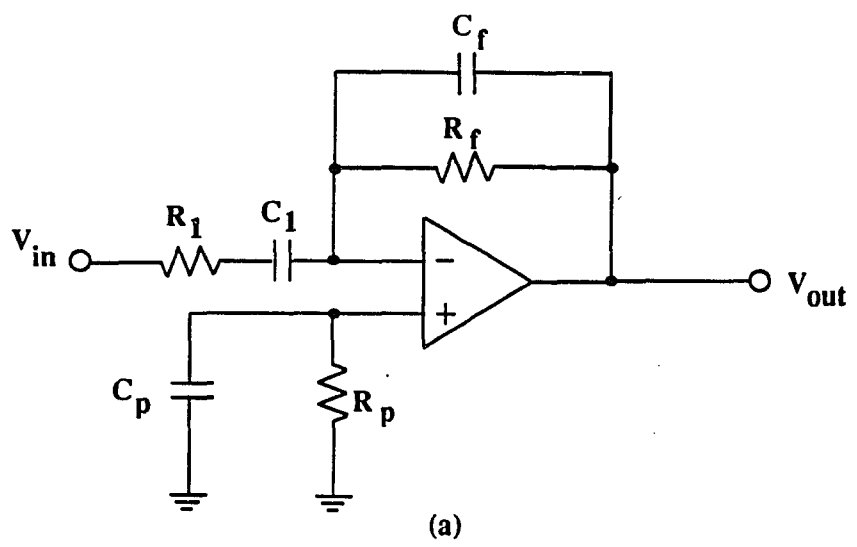


Figure 3.7: (a) Practical Differentiator, (b) Frequency Response of the Differentiator.

R_1	5.6K
R_f	10K
R_p	10K
C_p	5pF
C_1	15pF
C_f	2.5pF

f_d	1MHz
f_{cp1}	1.9MHz
f_{cp2}	6.4MHz

Figure 3.8: Component Values for Differentiator.

f_{cp1} was selected so that the frequency content of the readback signal ($0.8\mu m$ minimum mark width) falls within the useful region of differentiation. The frequency contents were determined by obtaining the power spectrum of the signal as mentioned in Sec. 3.1.1. f_{cp1} was selected in this manner to be 1.8MHz. f_d and f_{cp2} were chosen to be 1MHz and 6.4MHz, respectively. Simulation results for this differentiator are shown in Fig. 3.9. Component values for this design are given in Fig. 3.8.

3.1.3 Threshold Detection

Differentiation of the readback signal produces sharp spikes corresponding to the boundaries of data marks. Due to the inverting nature of this differentiator, a negative spike corresponds to the rising edge and a positive spike corresponds

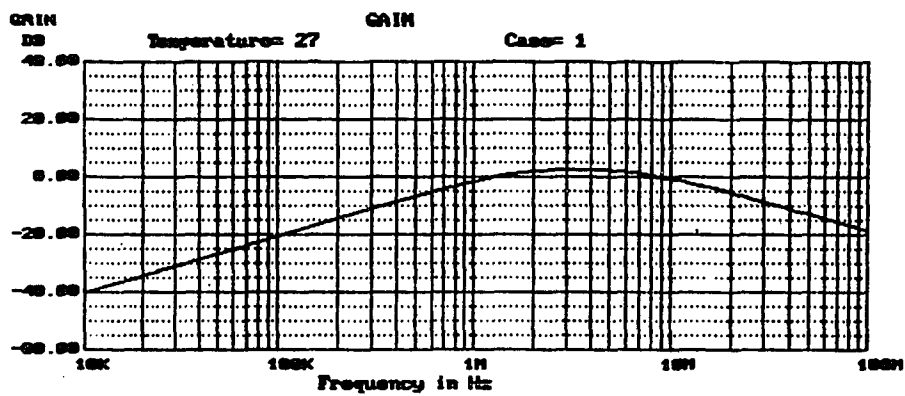
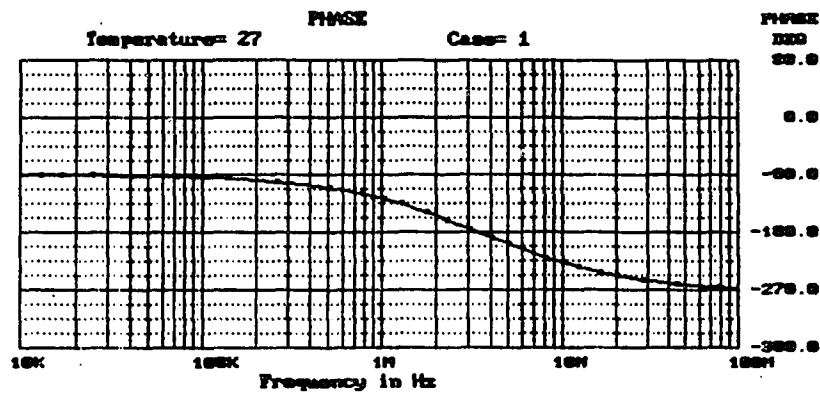


Figure 3.9: Frequency Response of Differentiator.

to a falling edge of a data mark. The conventional method for detecting the boundaries would be to find the second derivative and determine the zero-crossings corresponding to the spikes. A major problem would arise if the above approach were used. Each analog differentiation is accompanied by a considerable amount of noise and finding the proper zero-crossing could be extremely difficult.

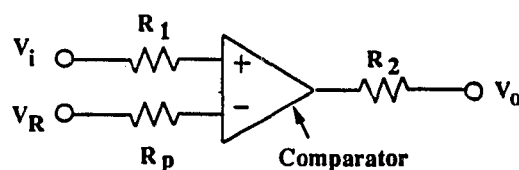


Figure 3.10: Threshold Detector.

An easier way of determining the boundaries of adjacent marks is to detect the peaks of the first derivative. As shown in Fig. 3.2, two threshold detectors can be used to detect positive and negative peaks of the spikes. Threshold detectors produce a "high" output whenever their inputs exceed a preset voltage level. A schematic of a peak detector is shown in Fig. 3.10. When V_i is greater than V_R , V_o approaches the positive rail voltage which is 5V. A negative threshold detector operates in a similar fashion except V_R and V_i are interchanged and V_R is set to a negative voltage. In order to minimize the effects of the input bias current and the input offset current of the comparator, R_p and R_1 are selected to be equal. R_2 is not essential in the operation of the comparator, but proved to be useful in suppressing noise. A detailed design outline for the threshold detector is given in [12].

The outputs of the level detectors, as shown in Fig. 3.2, were 'OR'ed together to obtain a train of narrow pulses which correspond to transition regions of the readback signal. Unfortunately, this signal did not yield consistent results when it was used to trigger the quantizer board. Consequently, another threshold

stage was added. A threshold voltage of about 3 volts was selected to eliminate all low amplitude noise components which may be present in the signal. As a result, the output of the final threshold detector contained narrow pulses with amplitudes of 3 volts or higher. This signal produced satisfactory results when applied to the quantizer circuitry. Figures 3.11 and 3.12 show the actual readback signals for $2\mu m$ and $1\mu m$ spot sizes. The first derivative and the threshold detector output are also included in the figures.

This detection method has two drawbacks. First, it is necessary to visually inspect the differentiator output to determine appropriate threshold levels. Second, narrow pulses produced by the detector system do not precisely correspond to the peaks of the differentiated signal. On the other hand, they do provide a reasonable approximation of the peak locations. In Chapter 6, the experimental results are analyzed and the effects of this approximation are further discussed.

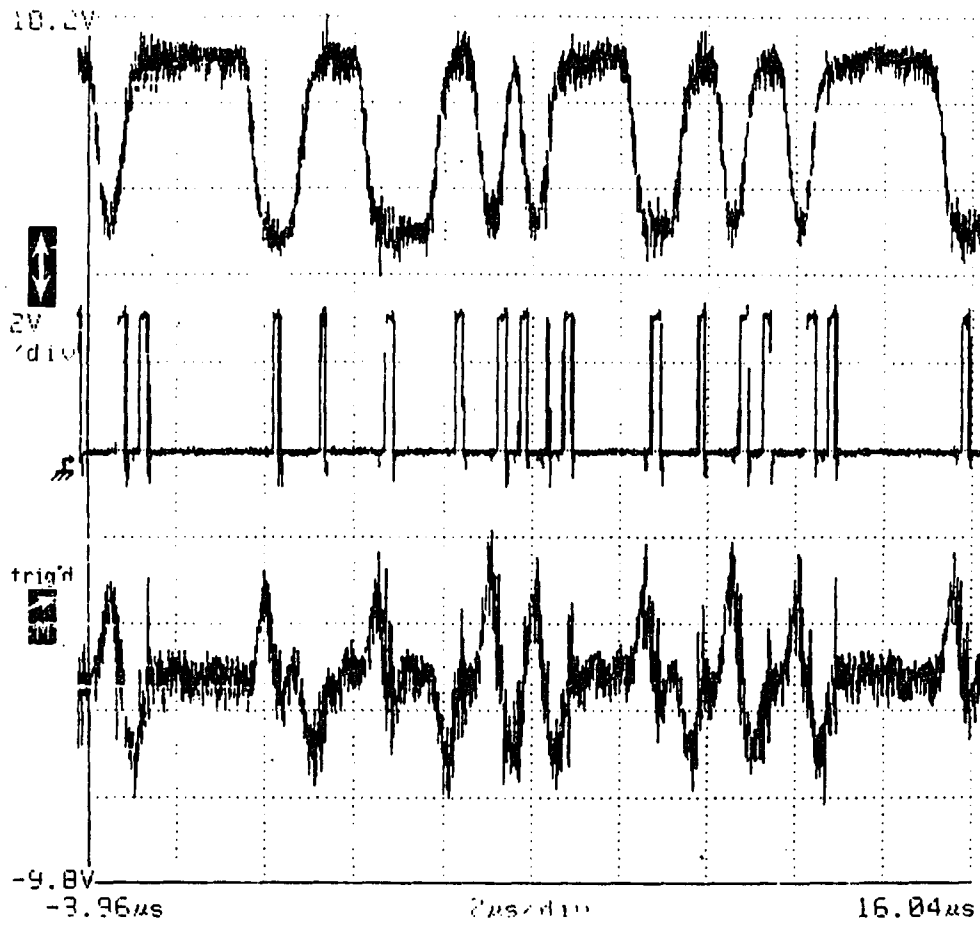


Figure 3.11: Readback Signal, Threshold Detector Output and Inverted First Derivative ($2\mu\text{m}$ spotsize).

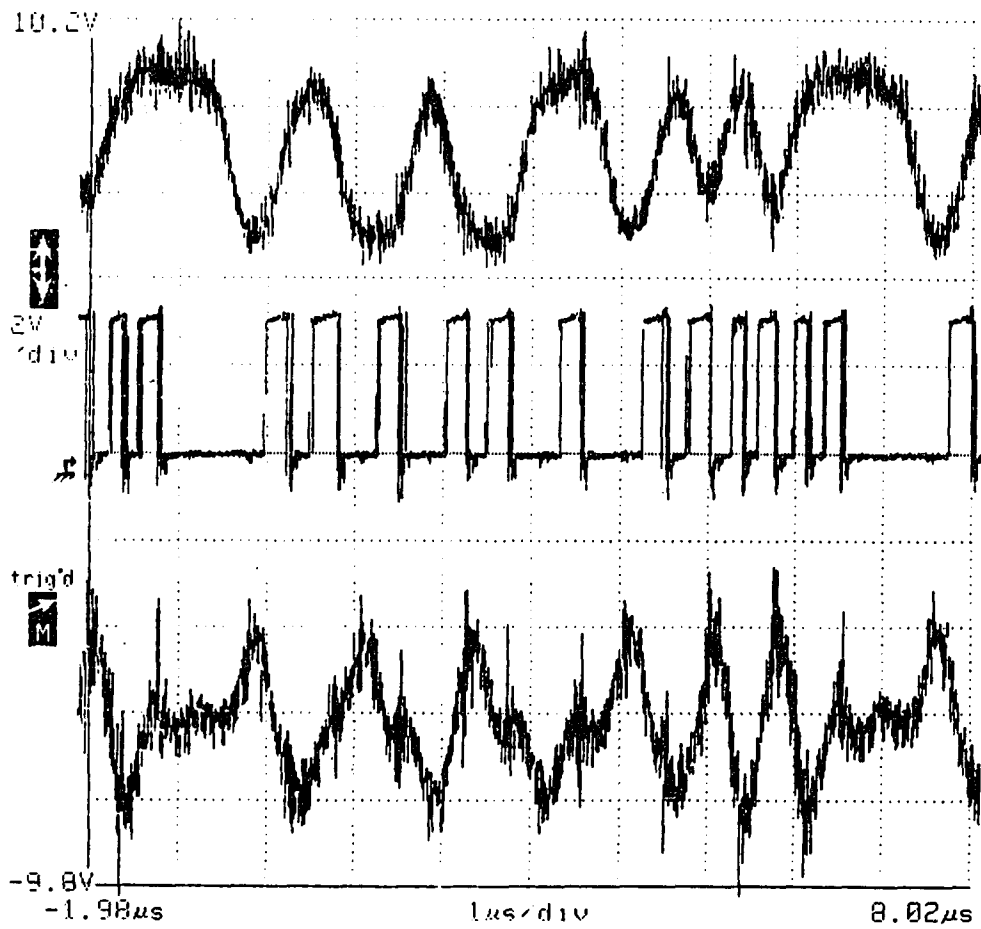


Figure 3.12: Readback Signal, Threshold Detector Output and Inverted First Derivative ($1\mu m$ spotsize).

CHAPTER 4

Time-Interval Quantizer

4.1 Basic Operation

Peak detection circuitry produces narrow rectangular pulses which correspond to positive and negative transitions in the readback signal. The separation between two such pulses is measured by the quantizer. Fig. 4.1 shows an overview of the quantizer operation. A 100 MHz clock is used to operate a 16-bit counter. Upon arrival of a pulse from the peak detection circuitry, the output of the counter is stored in a static RAM and the counter is reset to zero. Thus, the numbers that are stored in the RAM correspond to the interval between two adjacent pulses. The contents of the RAM are then transferred to a personal computer and further analyzed to compute the mark widths of the original data.

Proper timing of the reset signal is essential for obtaining valid results for this type of time-interval quantization. A more rigorous discussion of this topic is presented in Sec. 4.3. A detailed description of the digital logic circuits along with pin connections are given in Appendix B. In the following section, the design and operation of the 100 MHz clock is discussed.

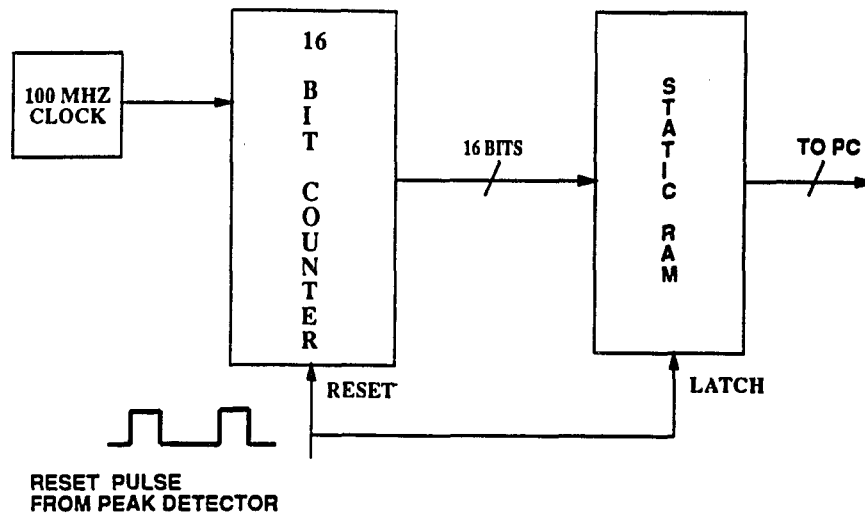
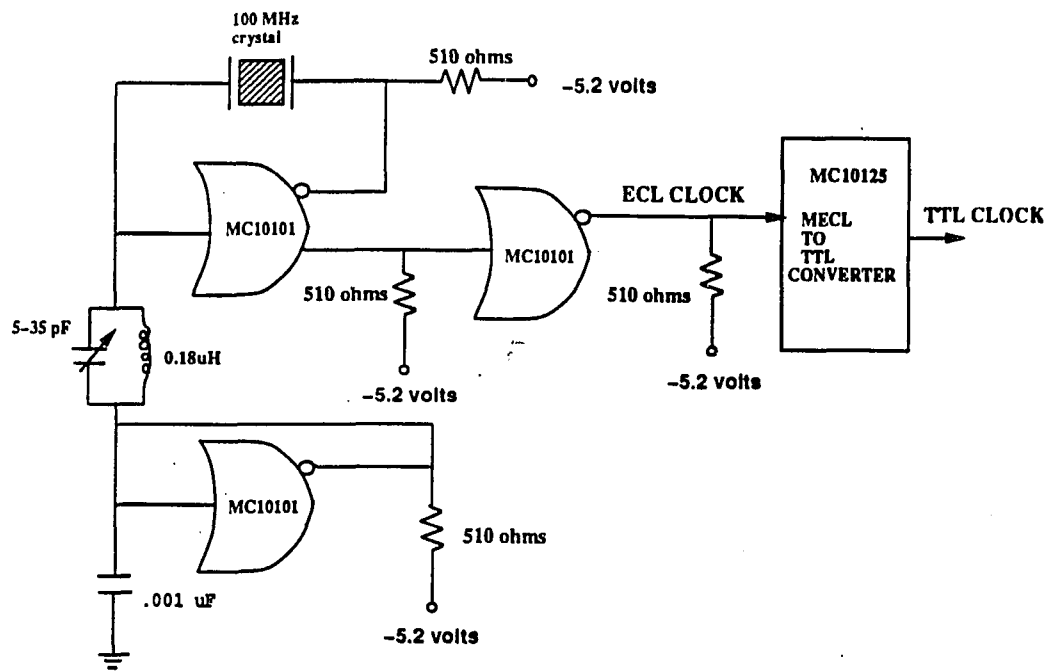


Figure 4.1: Time-Interval Quantizer.

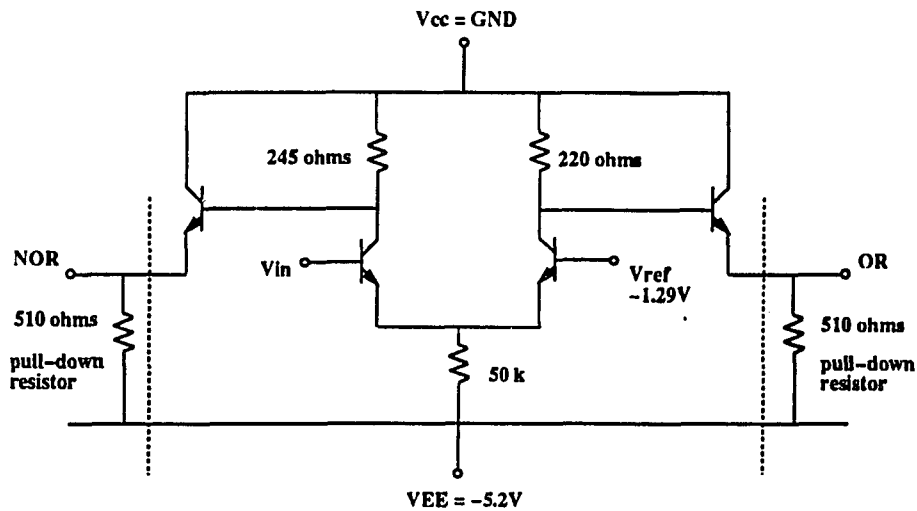
4.2 100 MHz Clock

4.2.1 Design

The circuit to generate the 100 MHz clock is shown in Fig. 4.2.a. In order to produce sustained oscillations, a 100 MHz overtone crystal is placed in the feedback loop of a MC10101 OR/NOR gate. This ECL NOR gate acts as an amplifier capable of producing 360 degrees phase shift from input to output. Fig. 4.2.b shows a schematic of an emitter-coupled logic OR/NOR gate [14]. In this figure only one input is shown to demonstrate the operation of the logic gate as an amplifier. All unused inputs must be kept at a logic level "low" which is -5.2 volts in ECL logic. The basic circuit of Fig. 4.2.b consists of a differential amplifier followed by two emitter-follower stages on either output. V_{ref} is generated internally and is set to the midpoint of the signal logic swing. For the ECL 10,000 family this bias voltage is -1.29 volts. Small excursions of the input around V_{ref} are amplified by the differential amplifier and the inverted output is obtained at



(a)



(b)

Figure 4.2: (a) 100MHz Clock Circuitry, (b) Schematic of an ECL OR/NOR Gate.

the NOR output. In this manner, an ECL NOR gate can be treated as an inverting amplifier.

One portion of MC10101, shown in Fig. 4.2.a, provides proper biasing for the feedback network. By connecting the NOR output to its input, the circuit stays at -1.29 volts which is the center of the logic swing [15]. A $0.001\mu F$ bypass capacitor is added to suppress unwanted oscillations. The purpose of the LC tank circuit is to tune the circuit to the exact oscillation frequency. Since an overtone crystal is used, care must be taken to avoid oscillations at undesired fundamental frequencies. The approximate value of frequency is obtained from

$$f \cong \frac{1}{2\pi\sqrt{LC}} \quad (4.1)$$

A third MC10101 NOR gate is used to buffer the clock output and protect the feedback network from external loading effects. As a final step, the ECL clock is passed through a MC10125 ECL to TTL converter. At this stage, the TTL clock is ready to be distributed to the quantizer circuitry.

4.2.2 Construction

Three ECL gates are used to generate the 100 MHz clock. These gates have small propagation delays (typically 2ns) and provide the high-speed performance required for clock generation. Design guidelines for such ECL circuits are more complicated than their TTL counterparts. In particular, noise reduction techniques must be used to avoid faulty operation of the circuits.

Several design considerations were made to solve the noise problem. A ground plane was used in the back plane and wire-wrap lengths were kept to a minimum. V_{cc1} and V_{cc2} package pins were connected directly to the ground plane as close to the package as possible. In addition, the clock circuitry was completely isolated from the TTL portion and separate power supplies were used for the

ECL board. Twisted-pair lines, approximately 5 inches long, supplied the TTL clock to the quantizer. These considerations, in addition to standard power supply bypassing, provided a reasonably clean clock output.

In compliance with equation 4.1, a $0.18\mu H$ inductor and a 5-35 pF variable capacitor were selected for the LC tank circuit of Fig. 4.2.a. Theoretically, these components can produce frequencies in the range 64-163 MHz. However, the crystal can only oscillate at one or more of its fundamental frequencies. Varying the capacitor value resulted in only one oscillation frequency, namely 111.1 MHz. This frequency was measured by a Tektronix 11402A Digitizing Oscilloscope. The counters of the quantizer circuitry were operational at this frequency and produced the expected results.

4.3 Quantization

Once the 100 MHz clock is available, the quantization of the data mark begins. The peak detector pulse (corresponding to a positive or a negative transition of recorded data) stops the counters and stores their binary outputs in a static RAM. Fig. 4.3.a shows a block diagram of this operation. The components of this system do not have compatible speeds. Therefore, additional latch stages are inserted to ensure proper timing of various parts. For instance, the presence of tri-state flip-flops are necessary to interface the high-speed counter (~ 9 ns per count) to the slower RAM (~ 80 ns setup time).

When a pulse from the peak detector arrives, the Hold/Reset generator produces narrow pulses of duration t_H and t_R , as depicted in Fig. 4.3.b. A delayed version of the peak detector signal is also produced to act as a clock signal for the tri-state flip-flops. The Hold signal prevents any changes from occurring in the counter output while the data is being latched to the RAM data lines. The Reset signal sets the counter back to zero and counting resumes as soon as Reset goes

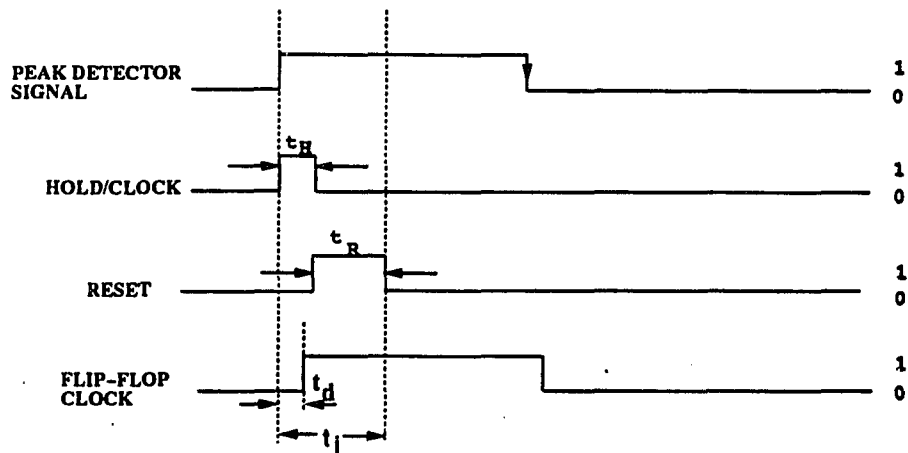
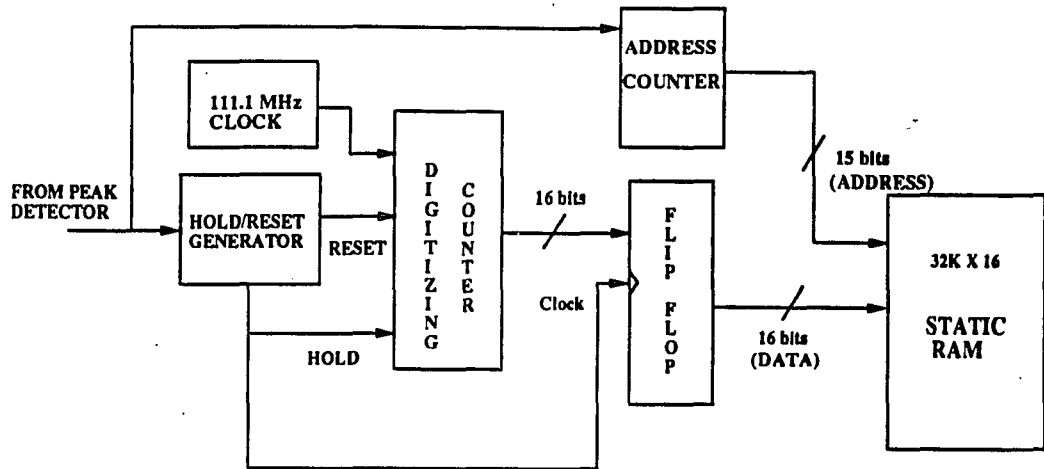


Figure 4.3: (a) Block Diagram of the Quantizer, (b) Hold/Reset Timing Diagram.

low. The falling edge of the peak detector signal increments the address counter of the RAM and the system becomes ready for the next incoming signal from the peak detector.

From the timing diagram of Fig. 4.3.b it is evident that the counter is idle for a time period equal to t_i . To account for this idle time, t_i should be added to the calculated value of the mark size. If we denote the time period corresponding to a stored binary number by t_S , the quantized mark width corresponding to that number is given by

$$t_Q = t_S + t_R + t_H \quad (4.2)$$

$$= t_S + t_i \quad (4.3)$$

where t_S is computed by multiplying the counter output by the time it takes for each count. Mathematically this can be expressed as

$$t_S = N \times \frac{1}{f_{osc}} \quad (4.4)$$

$$= N \times T \quad (4.5)$$

where $T = \frac{1}{f_{osc}} =$ Clock period,

$f_{osc} = 111.1$ MHz = Clock frequency, and

$N =$ Decimal equivalent of numbers in the RAM.

4.3.1 Hold/Reset Generator

Hold and Reset pulses are produced by manipulating an incoming peak detector signal as shown in Fig. 4.4. The basic idea is to invert and shift a relatively long signal and then, "AND" this version with the original signal to obtain a narrow pulse.

Hold signal, depicted in Fig. 4.4.a, is easily produced by first inverting and then shifting the peak detector signal by t_H . Then, the original signal is "AND"ed

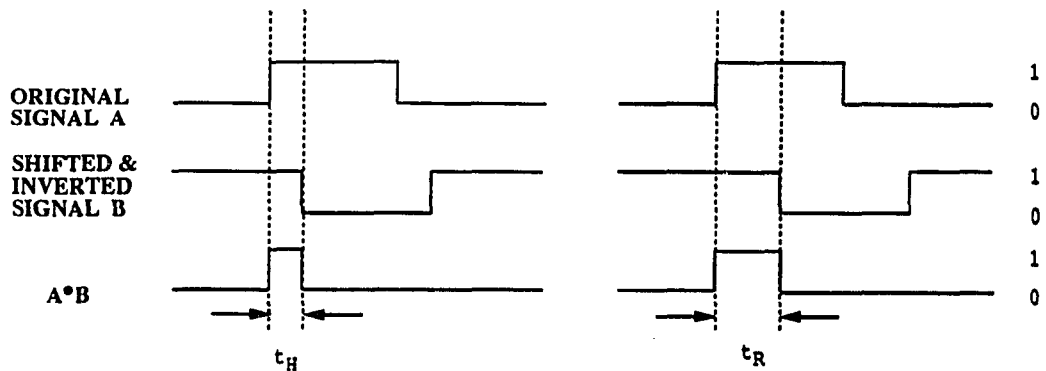


Figure 4.4: (a) Hold Signal Generation, (b) Reset Signal Generation.

with this signal. The result is a narrow pulse of width t_H . The Reset signal is obtained in a similar fashion, except, the time shift is t_R . Reset signal generation is shown in Fig. 4.4.b. The flip-flop clock signal (see Fig. 3.3.b) is just a delayed version of the original signal.

Shifting and inverting is accomplished by passing the signal through inverter gates. The amount of shift can be estimated by knowing the propagation delays of these gates. This information is readily available in TTL data books. However, the actual delays must be verified experimentally since individual inverters may have different characteristics. t_H and t_R are chosen to be as small as possible to reduce the counter idle time and avoid the possibility of signal overlap. Minimum t_H and t_R values obtained from TTL data books are 10 ns and 30 ns, respectively. The experimental t_H and t_R values were measured to be 15 ns and 30 ns. The time delay, t_d , for the flip-flop clock is roughly 8 ns. Generation of these signals required four 7404 inverter chips and one 74F08 AND chip. Detailed pin diagrams of the Hold/Reset Generator are given in Appendix B. An alternative way of producing the required delay is to utilize "Digital Delay Units". These components provide variable length delay periods and can replace several inverter gates in this design.

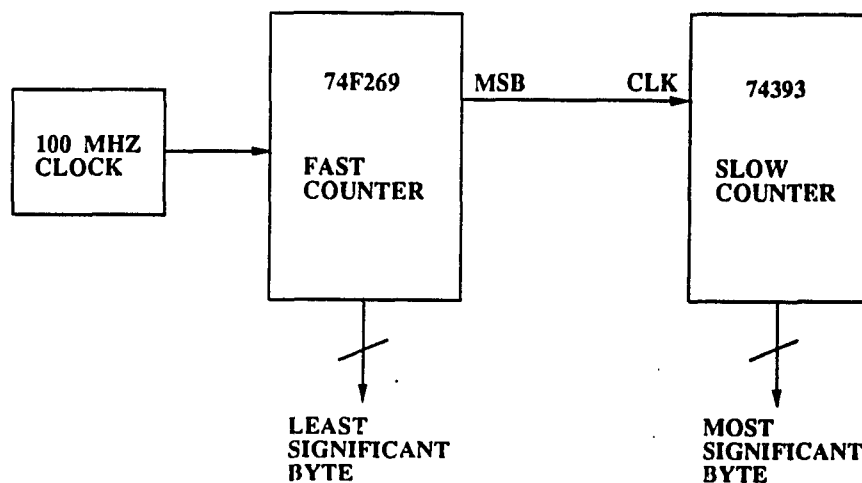


Figure 4.5: Hybrid Counter System.

4.3.2 Counter Design

The 16-bit digitizing counter of Fig. 4.3.a is an integral part of the system. A single 16-bit Fast Counter seems to be the best choice for providing the count. On the other hand, a similar design using a hybrid configuration can replace the 16-bit counter without compromising the accuracy of quantization. This hybrid combination proves to be very cost effective and provides the same service for less than 10% of the cost. Fig. 4.5 shows a diagram of the hybrid counter system. An 8-bit 74F269 counter is used in conjunction with a slower 74393 8-bit counter.

The Fast counter generates the least significant byte while the slow counter provides the most significant byte of the 16-bit number. This is made possible by connecting the most significant bit of the LSB counter to the clock input of the MSB counter. The above system was successfully implemented in the lab and it was fully operational.

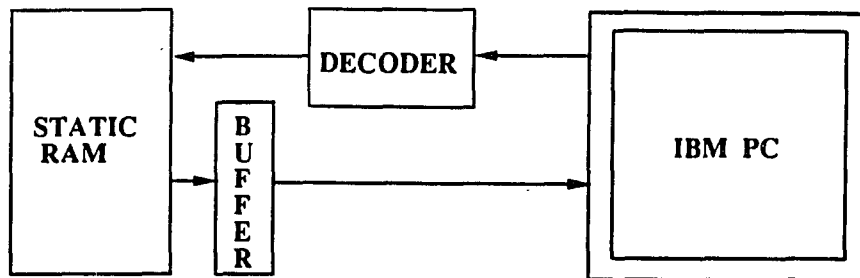


Figure 4.6: Data Transfer to PC.

4.4 Data Transfer

Section 4.3 described various components which performed quantization of data marks and stored the results in a RAM. The next step is to transfer the stored data to a personal computer for further analysis. In order to accomplish this task, the PC must issue a READ command to the I/O address of the static RAM. In addition, the RAM output must be enabled and its address counter should be incremented each time a byte is read. The decoder box, shown in Fig. 4.6, is responsible for routing correct addresses and command signals to their appropriate destination. A BASIC program was written for transferring the data to an IBM PC.

4.4.1 Address Decoder

Fig. 4.7 shows the decoder circuitry for the quantizer board. The decoder output line becomes low when an address in the range $3E8-3EF$ is selected by an I/O READ command. The 8-input NAND gate, as discussed in Sec. 2.1.1, is used for decoding $A3-A9$ address lines. The I/O READ line is passed through a buffer and "OR"ed with the output of the NAND gate. The OR output enables a 74155 3-line to 8-line decoder. $A0, A1,$ and $A2,$ are three low order address lines which

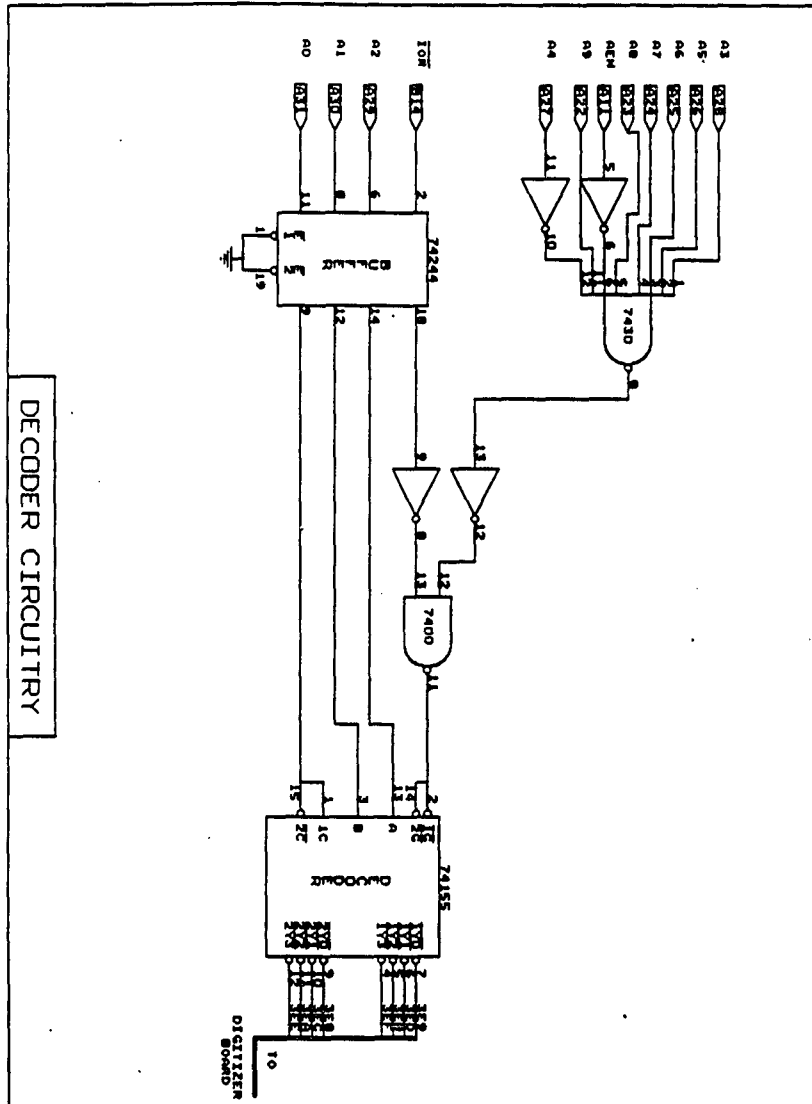


Figure 4.7: Decoder Circuitry

are used as inputs for the decoder chip. The decoder outputs are active low and one of eight output pins are pulled low when the appropriate address is present at its input. The PC can address 8 different external devices through this decoder circuitry. Addresses *3E8* and *3EE* are reserved for the pattern generator and may not be used for the quantizer circuitry.

4.4.2 Data Acquisition

A BASIC program, given in Appendix B, retrieves the stored data from the static RAMs. Dip switches on the quantizer board are set to allow data transfer to the PC. Since there are 8 data lines on PC's I/O bus, the 16-bit number must be transferred one byte at a time. For this purpose, two $32K \times 8$ RAMs are used on the quantizer board, one of which contains the most significant byte (MSB) and the other stores the the least significant byte (LSB) of the number. Each RAM is located at one I/O address of the PC. A third I/O location is designated to reset the address counters at the start of data retrieval.

A few lines of the BASIC program are repeated in Fig. 4.8 to demonstrate data transfer. The execution of this program inputs the LSB and MSB of data and increments the address counter each time through the loop. Data acquisition begins by inputting a byte from location *3E9*. This command enables one of decoder's active low outputs. At this stage, it is not intended to transfer data. The transition caused by *INP(3E9)* is merely used to reset the address counter to zero. The first line inside the loop inputs the least significant byte of data. This command generates a low signal on *3ED* decoder output and enables the LSB RAM and its buffer. *INP(3EB)* on the next line initiates a similar action except this time the MSB RAM is activated. The inverted version of *3EB* decoder output is connected to counter's clock input. Thus, after the MSB is read, a transition on this line increments the counter.

The I/O READ signal has a relatively large pulse width (650 ns) and INP

```

      .
      .
      .
      C%=INP(3E9)
      FOR I%= 1 TO 1000
        A%(I%) = INP(3ED)
        B%(I%) = INP(3EB)
      NEXT I%
      .
      .
      .

```

Figure 4.8: Data Transfer Program.

commands are separated by $\sim 15ms$. These values are considerably larger than the timing requirements for digital circuits on the quantizer board. As a result, no timing complications and signal overlaps were expected for the design. The above data transfer system was built and tested. Some of the results are given in Sec. 4.6.

4.5 Quantization Error

One disadvantage of this system is the presence of quantization noise. This error is due to the fact that the quantized marks can only be an integer multiple of the clock period. The quantization error, q , can be considered a random variable given by

$$q = x - \hat{x} \quad (4.6)$$

where x is the actual time mark and \hat{x} is the quantized mark. In the ideal situation, q is a random variable existing in the range $[-\frac{T}{2}, \frac{T}{2}]$, with T being the clock period.

Under the assumption that q is equally likely to lie anywhere in this interval, a uniform Probability Density Function is obtained for q [18]:

$$p_q(q) = \frac{1}{T}. \quad (4.7)$$

By noting that $\bar{q} = 0$, the mean square expression for quantization error is obtained as follows:

$$\sigma^2 = \overline{q^2} = \int_{-\frac{T}{2}}^{\frac{T}{2}} q^2 p_q(q) dq \quad (4.8)$$

$$= \frac{1}{3} q^3 p_q(q) \Big|_{-\frac{T}{2}}^{\frac{T}{2}} \quad (4.9)$$

$$= \frac{T^2}{12}. \quad (4.10)$$

For a data mark of duration T_m , Signal-to-Noise-Ratio is calculated by [5]

$$SNR = 10 \log_{10} \left(\frac{(T_m)^2}{\sigma^2} \right). \quad (4.11)$$

The clock period, T , is 9ns (Sec. 4.2). For a T_m of 200ns, the SNR is approximately 1500 or 32 db. This value can be considerably improved by selecting a faster clock rate for quantization. The choice of T_m in these calculations was determined by the actual time marks used in the experimental setup (Chap. 5).

4.6 Experimental Verification

The system of Fig. 4.3.a was assembled and tested to verify its operation. An 81131A Hp pulse generator was used to simulate the incoming peak detector signal. Five different test pulses were used. Fig. 4.9 shows the results of data collection. Column 2 represents the binary outputs of the digitizing counters in 1000 trials. Column 4 calculates the time mark by using Eq. 4.3. In column 5, mark size deviations from the original marks are calculated. This difference is primarily due to the quantization noise. These results indicate that the quantizer system operates as expected.

ACTUAL PULSE SEPARATION t_A (ns)	COUNTER OUTPUT N	COUNTER IDLE TIME t_I (ns)	AVG PULSE SEPARATION t_Q (ns)	DEVIATION $ t_A - t_Q $ (ns)
200	17-18	45	202	2
250	22-23	45	252	2
333	32-33	45	337	4
500	50-51	45	504	4
999	104-106	45	998	1

Figure 4.9: Test Data for the Quantizer System.

CHAPTER 5

Experimental Setup and Results

5.1 Experimental Setup

The complete system of Fig. 1.2 was constructed and used to collect data. A pseudo-random sequence of zeros and ones was recorded on the optical disk at four different clock rates. These rates were selected so that the minimum mark sizes of $2\mu m$, $1.33\mu m$, $1\mu m$, and $0.8\mu m$ were produced. The length of this pattern was set by the cycle generator to 31 bits. Fig. 5.1 shows the original sequence of recorded marks. Figures 5.2 and 5.3 show the actual readback signals for $1\mu m$ and $2\mu m$ spot sizes. Evidence of signal degradation is observed in these figures, especially at smaller spot sizes.

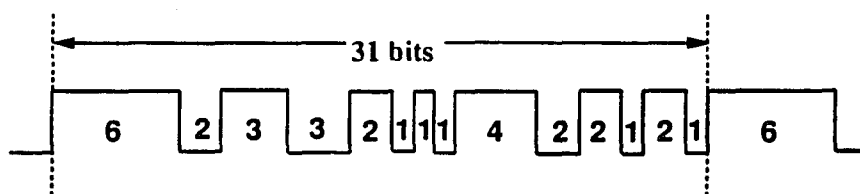


Figure 5.1: Recorded Pseudo-Random Sequence.

Readback signals were passed through the peak detector and digitizer boards. Peak detection was not very effective at $1\mu m$ and $0.8\mu m$ spot sizes. Due to the small amplitude of bit 18 (center mark in '1-1-1' sequence), the differentiator could not produce large enough spikes to mark the boundaries of this bit.

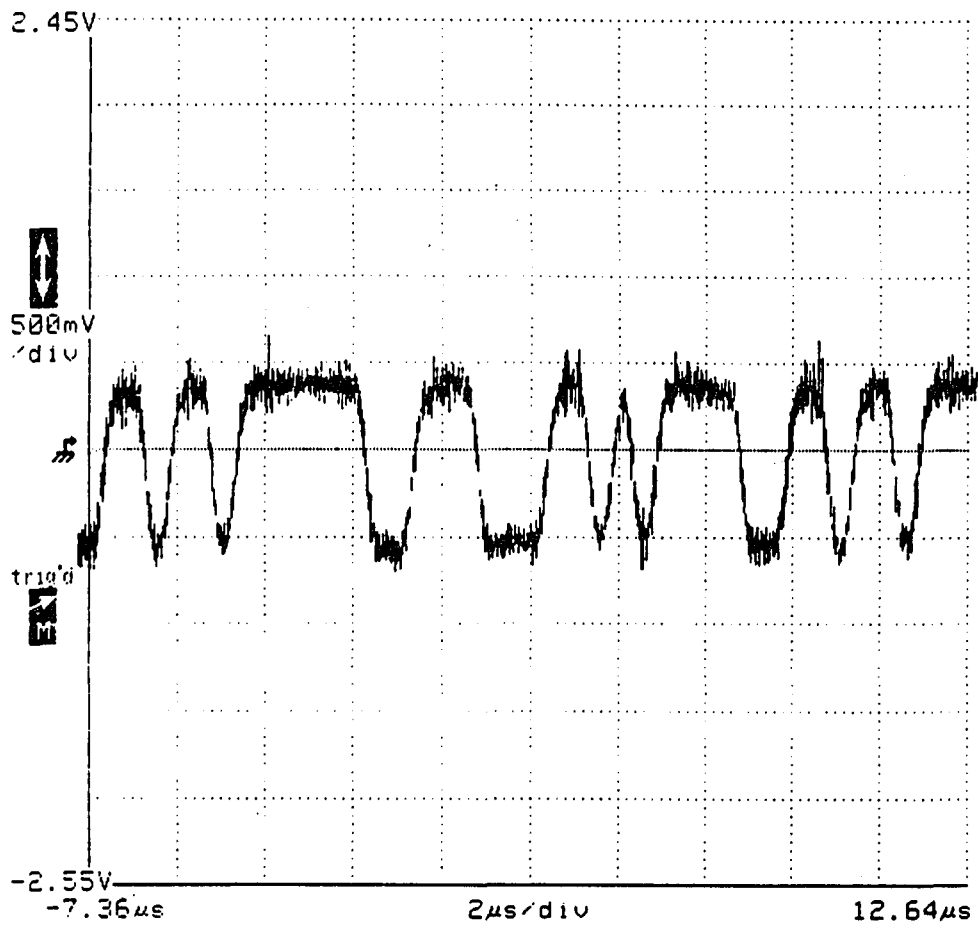


Figure 5.2: Readback Signal (2μm Spot Size).

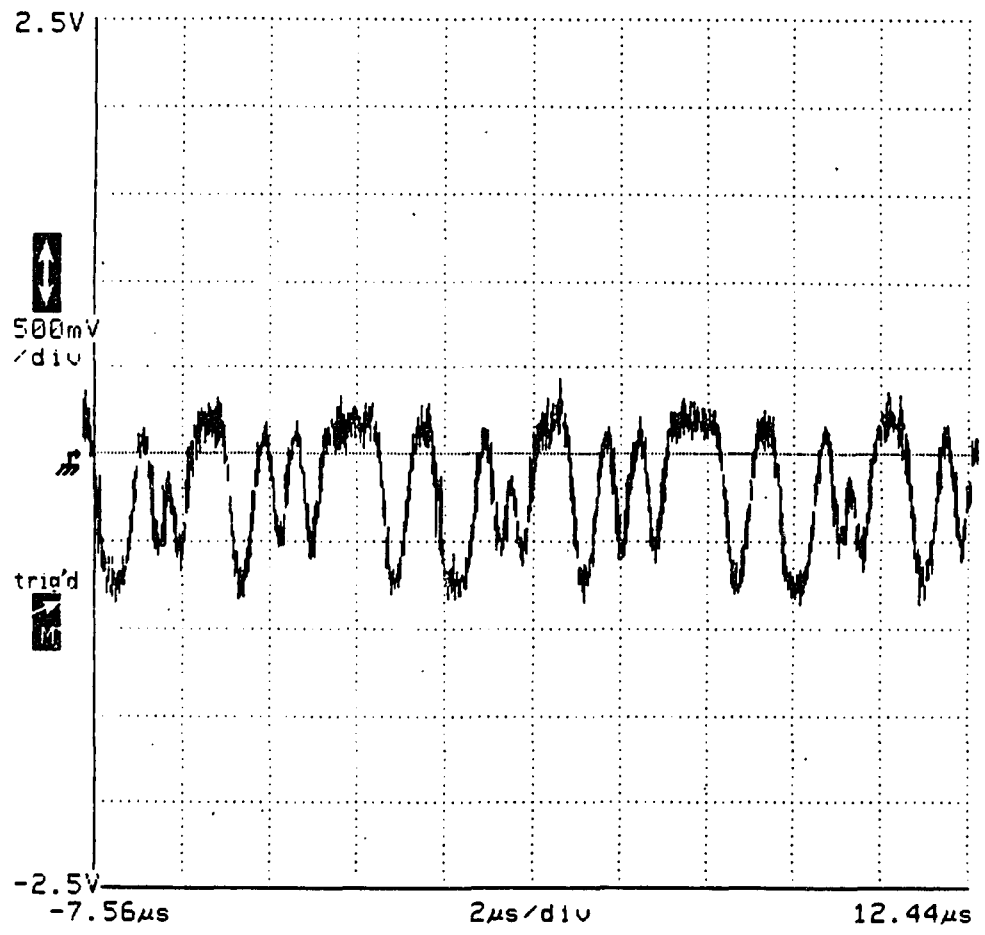


Figure 5.3: Readback Signal (1μm Spot Size).

Consequently, the pseudo-random sequence was slightly modified to accommodate this limitation. The new sequence is shown in Fig. 5.4.



Figure 5.4: Modified Pseudo-Random Sequence

The feedback resistor, R_f , of the differentiator (see Fig. 3.7) was also replaced by a variable resistor. Since differentiation is strongly frequency dependent, the value of R_f had to be adjusted so that data patterns with different spot sizes ($0.8\mu m - 2.0\mu m$) could be effectively differentiated. For each spot size 1000 quantized marks (~ 32 cycles) were collected and stored in the RAM chips of the quantizer board.

5.2 Data Analysis

The collected data were transferred to the PC and mark sizes of the readback signal were determined. Signal-to-Noise-Ratio's were computed by first calculating mark size deviations from the original mark sizes. This deviation can be expressed as

$$d_i = W_i - \hat{W}_i, \quad i = 1, 2, \dots, N \quad (5.1)$$

where W_i = Original Mark Size Recorded on Disk, and

\hat{W}_i = Measured Mark Size of Readback Signal.

The variance is defined as

$$\sigma^2 = \frac{1}{N} \sum_{i=1}^N d_i^2 \quad (5.2)$$

and SNR computed as

$$SNR = 10 \log_{10} \left(\frac{W_{unit}^2}{\sigma^2} \right) \quad (5.3)$$

where W_{unit} = Minimum Spot Size Recorded

From Eq. 5.3, several SNR values are calculated. Fig. 5.5 shows four different SNR curves. SNR for high marks is computed by considering only the high bits. Similarly, the low SNR is computed by only accounting for low bits.

Another SNR computation is done for Additive Interleaving Detection (AID) [5]. With this detection technique every other transition edge is detected so that W_i or \hat{W}_i in Eq. 5.1 is actually the summation of two adjacent marks. AID mark widths would then become:

$$W_j^{AID} = W_i + W_{i+1} \quad (5.4)$$

$$\hat{W}_j^{AID} = \hat{W}_i + \hat{W}_{i+1} \quad (5.5)$$

Hardware implementation of the AID technique can be accomplished by making a few modifications to the original circuits. Referring to the peak detector of Fig. 3.2, a simple modification requires the removal of the 'OR' gate. In this case, two set of reset pulses are produced. One corresponds to the positive transitions and the other corresponds to the negative transitions of the readback signal. In addition, the quantizer of Fig. 4.3.a is duplicated to facilitate collection and quantization of data marks. Fig. 5.6 shows a block diagram of the modified AID circuitry. SNR computations are carried out according to Eq. 5.3 with modified mark sizes given by Eqn. 5.4 and 5.5.

SNR results for the AID technique are graphed in Fig. 5.5 along with previous SNR curves. Improvements in Signal-to-Noise-Ratio's are observed consistently for different spot sizes. This can be explained by noting that adjacent marks have correlated ISI characteristics. As a result, when a high mark is detected together with its neighboring low mark, some of the ISI effects are cancelled. Fig. 5.5 indicates 3 to 5 dB SNR improvements due to the AID technique.

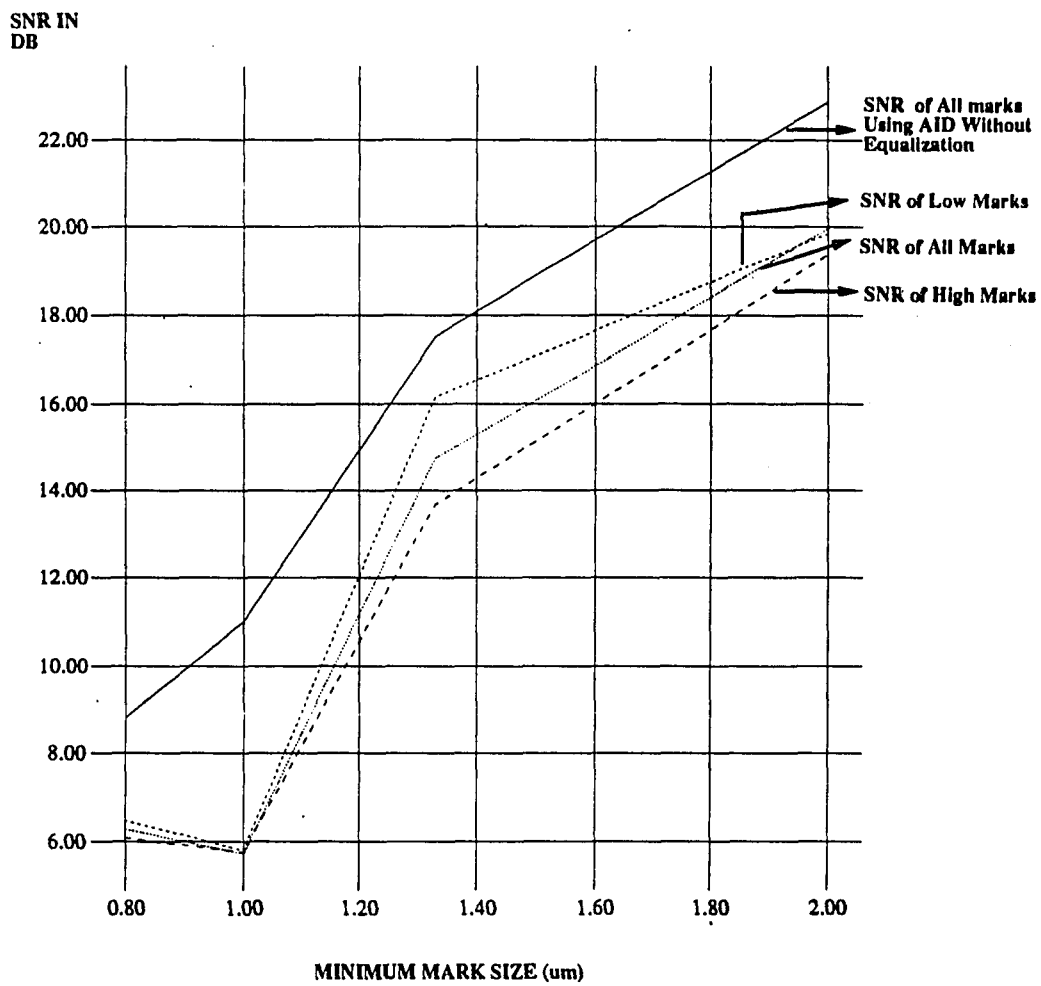


Figure 5.5: SNR Graphs for Measured Mark Sizes.

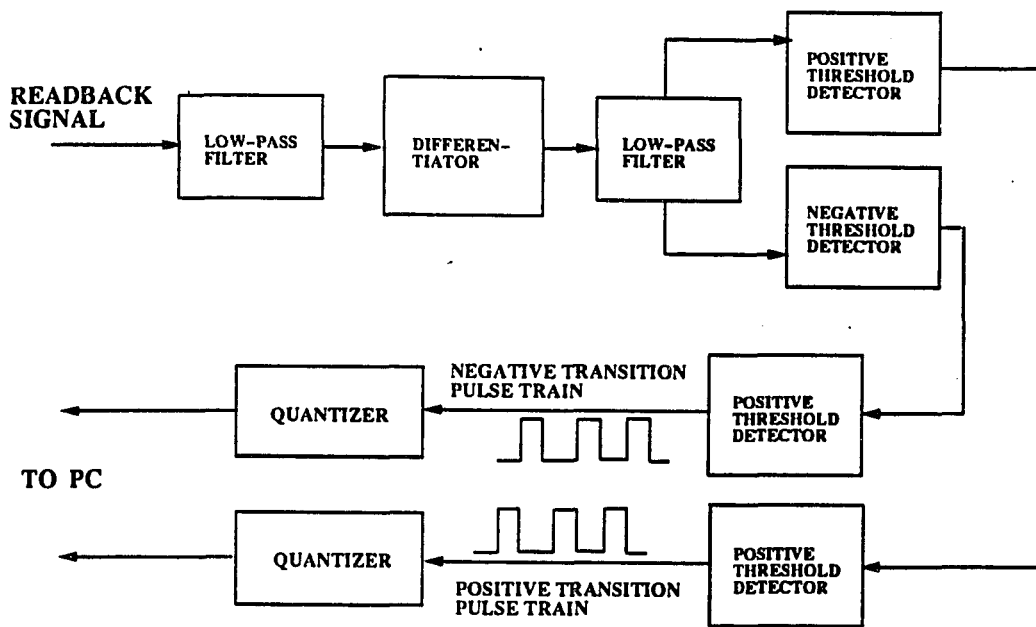


Figure 5.6: AID Mark Size Detection System.

CHAPTER 6

Conclusion and Discussion

The objective of this thesis was to develop a hardware system to measure mark size deviations of the readback signal from the original marks in an optical storage system. This system, depicted in Fig. 1.2, was built and tested for a pseudo-random data pattern. SNR computations were done for different spot sizes of the recorded signal. The results obtained by this system were consistent with conclusions reached by software methods [9]. These results indicate that SNR values decrease as the spot size decreases. Additive Interleaving Detection of marks proved to yield improved SNR values. This improvement was in the range 3 to 5dB for minimum mark sizes $0.8 - 2.0\mu m$.

SNR values may be further improved by selecting a better peak detection technique. Due to a considerable amount of noise in the differentiation process, a modified peak detection method was used. This modification required visual inspection of the differentiated signal for setting threshold levels. This task became more complicated when the differentiated signal contained narrow pulses with different amplitudes. As a result, the transition regions detected by this technique were only estimates of true boundary locations. Nevertheless, they provided a reasonable approximation and the final results were very consistent. Peak detection can be improved by mounting the components and integrated circuits on a multi-layered printed circuit board. This reduces noise and interference in the signal. In order to reduce operator interaction, the feedback resistor of the differentiator may be replaced by a *digital potentiometer*. This potentiometer may be controlled by the computer and is adjusted automatically for various readback signals with

different frequency components.

The overall system performance is also limited by the quantization error ($\text{SNR} \leq 32\text{db}$). In calculating this upper bound (Sec. 3.5), the minimum mark duration was selected to be 200ns. This corresponds to the smallest possible mark (1 bit) with $0.8\mu\text{m}$ spot size. SNR values obtained for this spot size were much lower than this limit. Thus, one can conclude that quantization noise did not play a major role in experimental results. Quantization error can be further reduced by increasing the clock rate.

The quantizer system designed in this thesis can be used to study ISI in many different data patterns. Once ISI characterization is complete, signal processing algorithms can be implemented in digital logic circuitry to reduce the ISI effects. For instance, read and write equalization techniques can be developed to compensate for ISI in the signal. The final system may be realized in a single VLSI chip to provide a compact and economical package.

APPENDIX A

Pattern Generation

A typical program to generate a pattern of zeros and ones is included in this appendix. The Pattern Generator circuitry is shown following the BASIC program.

DIM a%(40)

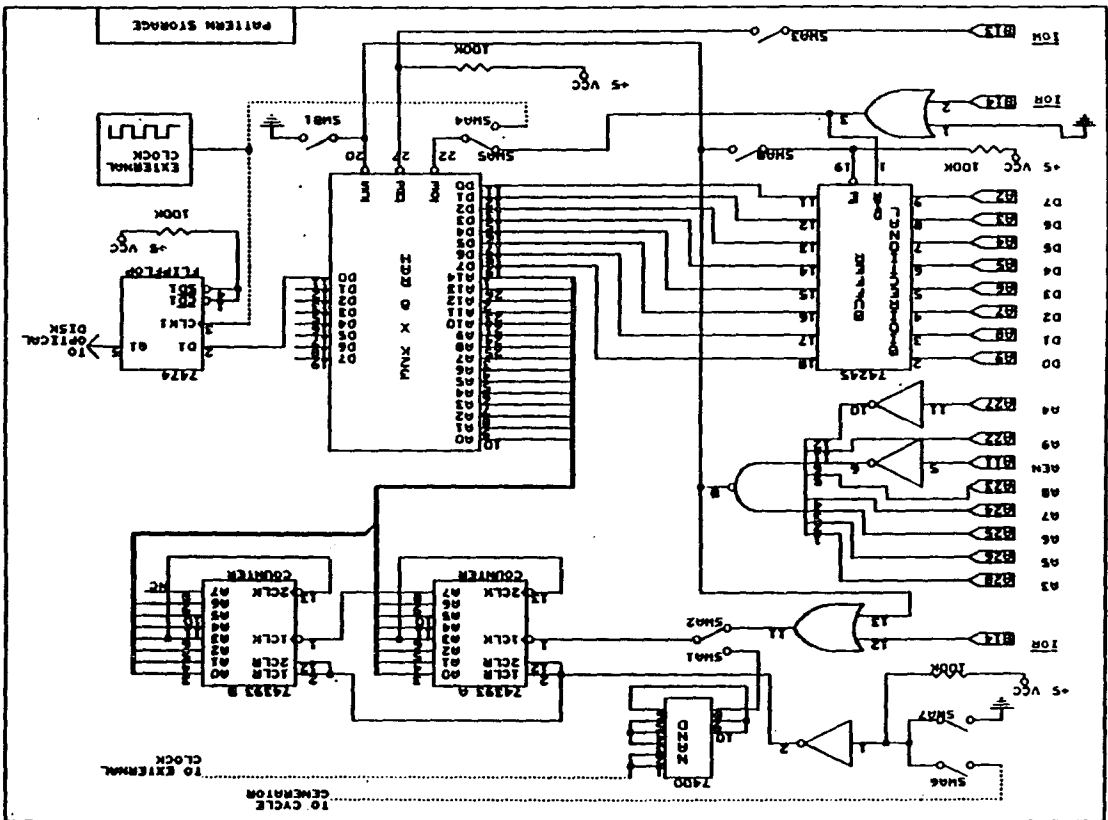
a%(1) = 1
a%(2) = 1
a%(3) = 1
a%(4) = 1
a%(5) = 1
a%(6) = 0
a%(7) = 0
a%(8) = 1
a%(9) = 1
a%(10) = 1
a%(11) = 0
a%(12) = 0
a%(13) = 0
a%(14) = 1
a%(15) = 1
a%(16) = 0
a%(17) = 1
a%(18) = 0
a%(19) = 1
a%(20) = 1
a%(21) = 1
a%(22) = 1
a%(23) = 0
a%(24) = 0
a%(25) = 1
a%(26) = 1
a%(27) = 0
a%(28) = 1
a%(29) = 1
a%(30) = 0
a%(31) = 1
a%(32) = 1
a%(33) = 1

FOR J% = 1 TO 33

OUT &H3EA, a%(J%)
PRINT "THE NUMBER STORED IN THE RAM IS: ", INP(&H3EA)

NEXT J%

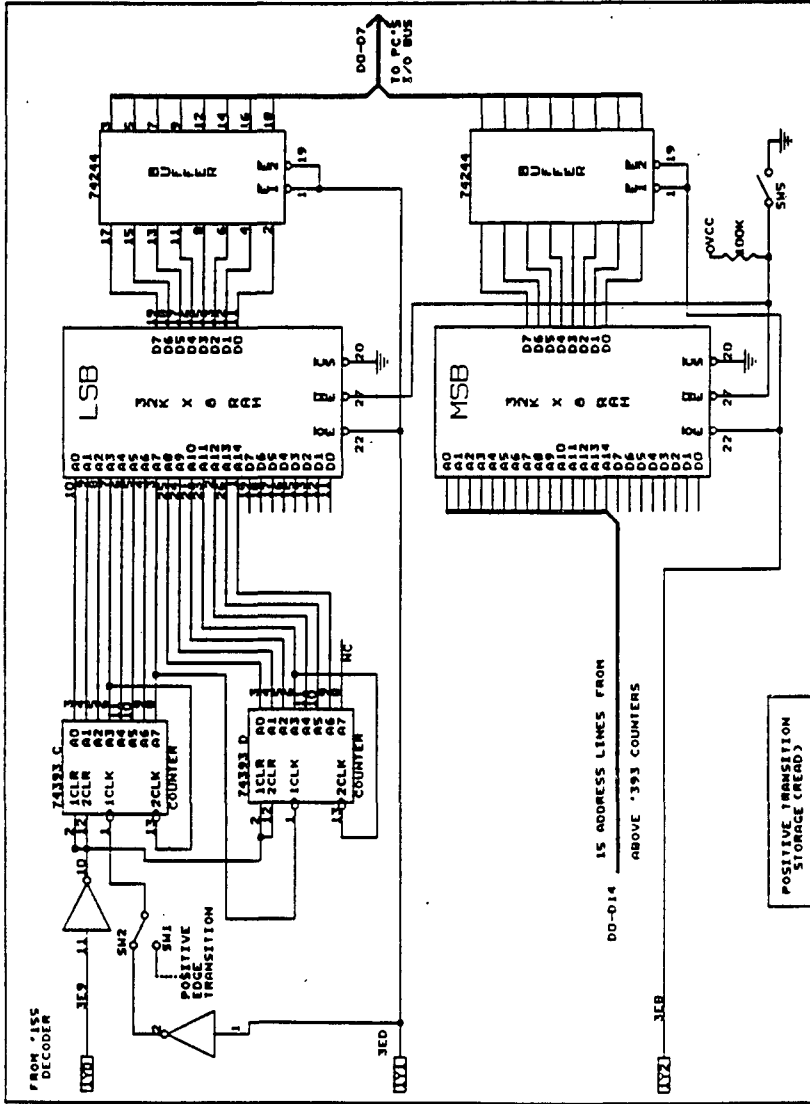
END



APPENDIX B

Quantizer Circuitry

Detailed pin diagrams of various components of the Digitizer board are presented in the following pages.



FROM '155
DECODER

3E9

3E8

3E7

3E6

3E5

3E4

3E3

3E2

3E1

3E0

3E0

3E1

3E2

3E3

3E4

3E5

3E6

3E7

3E8

3E9

3EA

3EB

3EC

3ED

3EE

3EF

3F0

3F1

3F2

3F3

3F4

3F5

3F6

3F7

3F8

3F9

3FA

3FB

3FC

3FD

3FE

3FF

400

401

402

403

404

405

406

407

408

409

40A

40B

40C

40D

40E

40F

410

411

412

413

414

415

416

417

418

419

41A

41B

41C

41D

41E

41F

420

421

422

423

424

425

426

427

428

429

42A

42B

42C

42D

42E

42F

430

431

432

433

434

435

436

437

438

439

43A

43B

43C

43D

43E

43F

440

441

442

443

444

445

446

447

448

449

44A

44B

44C

44D

44E

44F

450

451

452

453

454

455

456

457

458

459

45A

45B

45C

45D

45E

45F

460

461

462

463

464

465

466

467

468

469

46A

46B

46C

46D

46E

46F

470

471

472

473

474

475

476

477

478

479

47A

47B

47C

47D

47E

47F

480

481

482

483

484

485

486

487

488

489

48A

48B

48C

48D

48E

48F

490

491

492

493

494

495

496

497

498

499

49A

49B

49C

49D

49E

49F

500

501

502

503

504

505

506

507

508

509

50A

50B

50C

50D

50E

50F

510

511

512

513

514

515

516

517

518

519

51A

51B

51C

51D

51E

51F

520

521

522

523

524

525

526

527

528

529

52A

52B

52C

52D

52E

52F

530

531

532

533

534

535

536

537

538

539

53A

53B

53C

53D

53E

53F

540

541

542

543

544

545

546

547

548

549

54A

54B

54C

54D

54E

54F

550

551

552

553

554

555

556

557

558

559

55A

55B

55C

55D

55E

55F

560

561

562

563

564

565

566

567

568

569

56A

56B

56C

56D

56E

56F

570

571

572

573

574

575

576

577

578

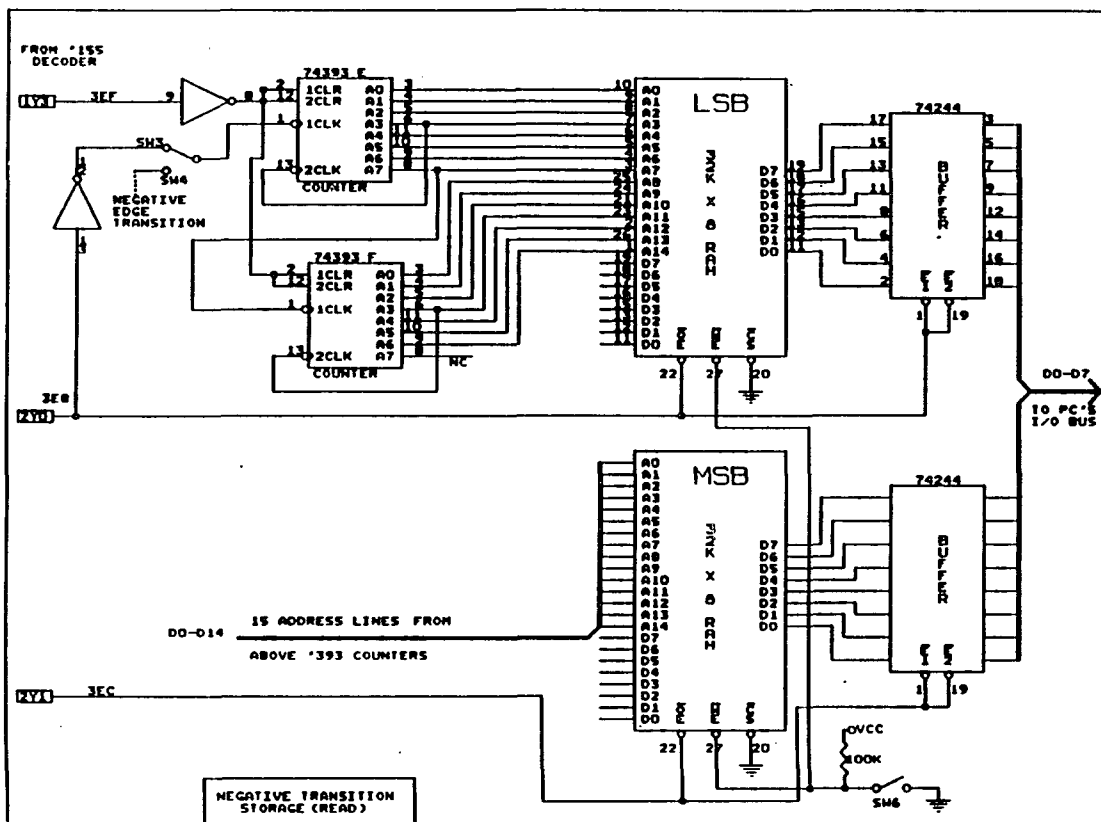
579

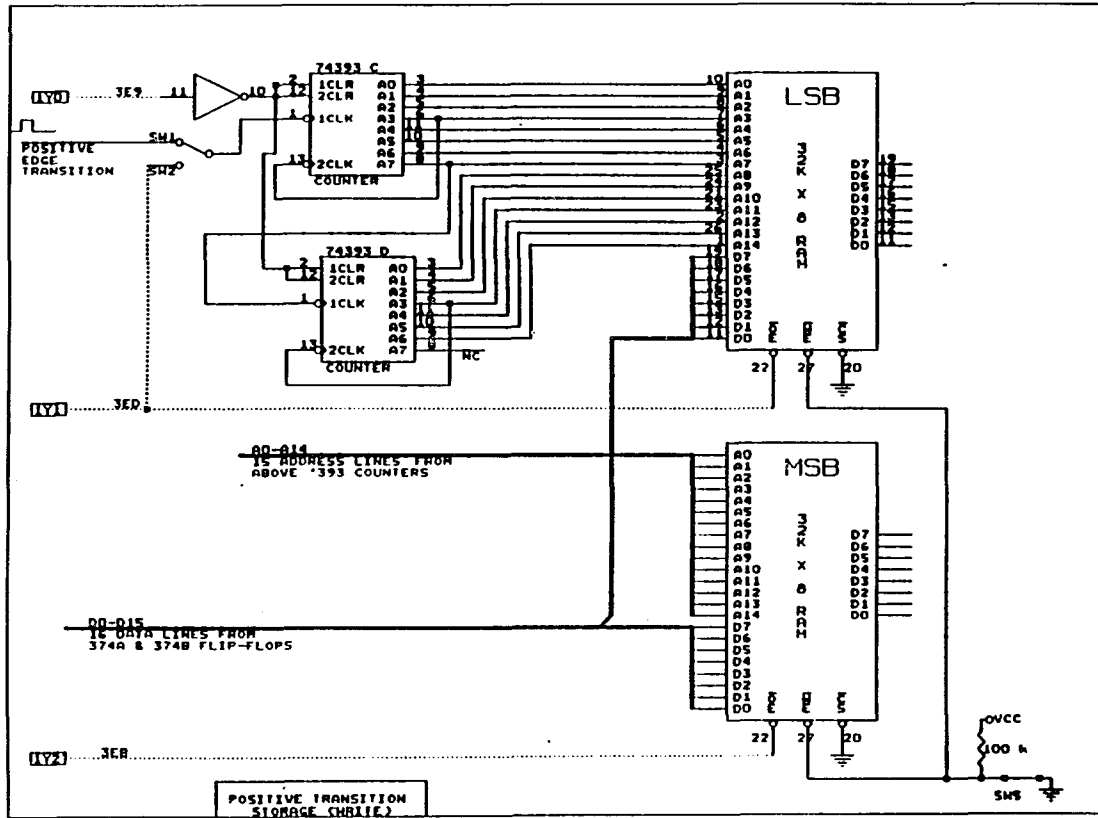
57A

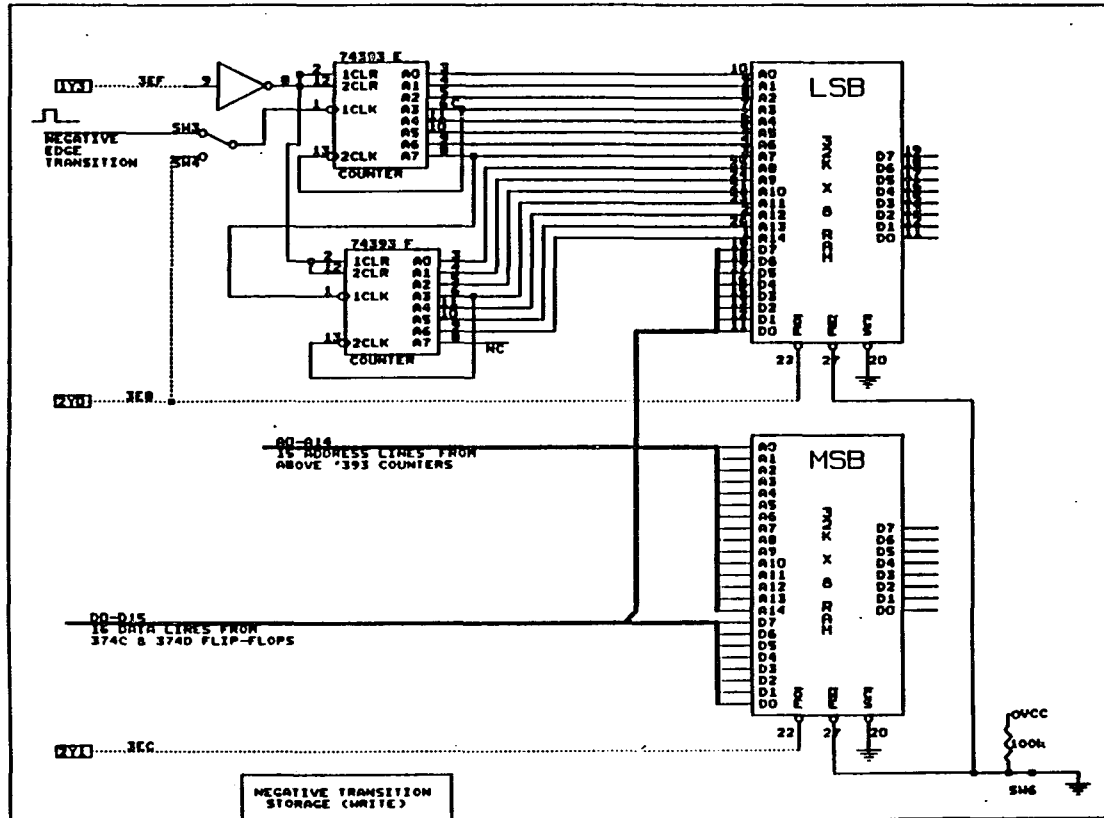
57B

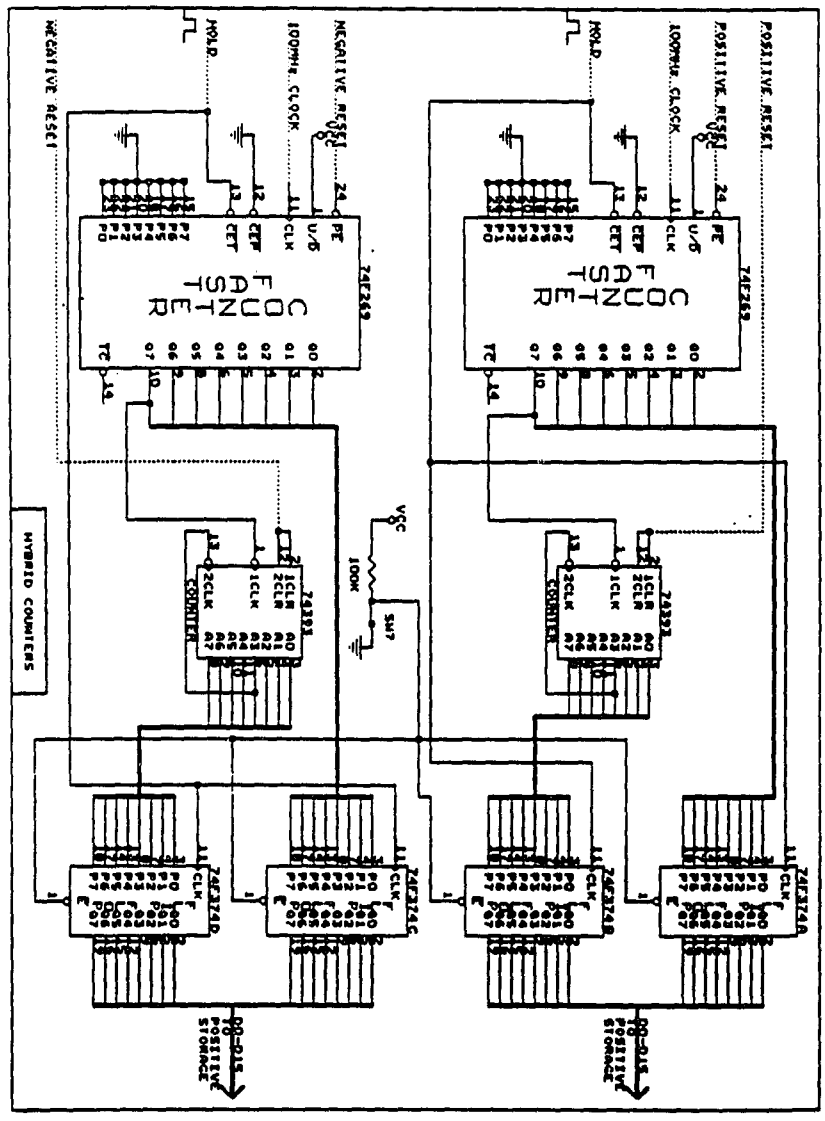
57C

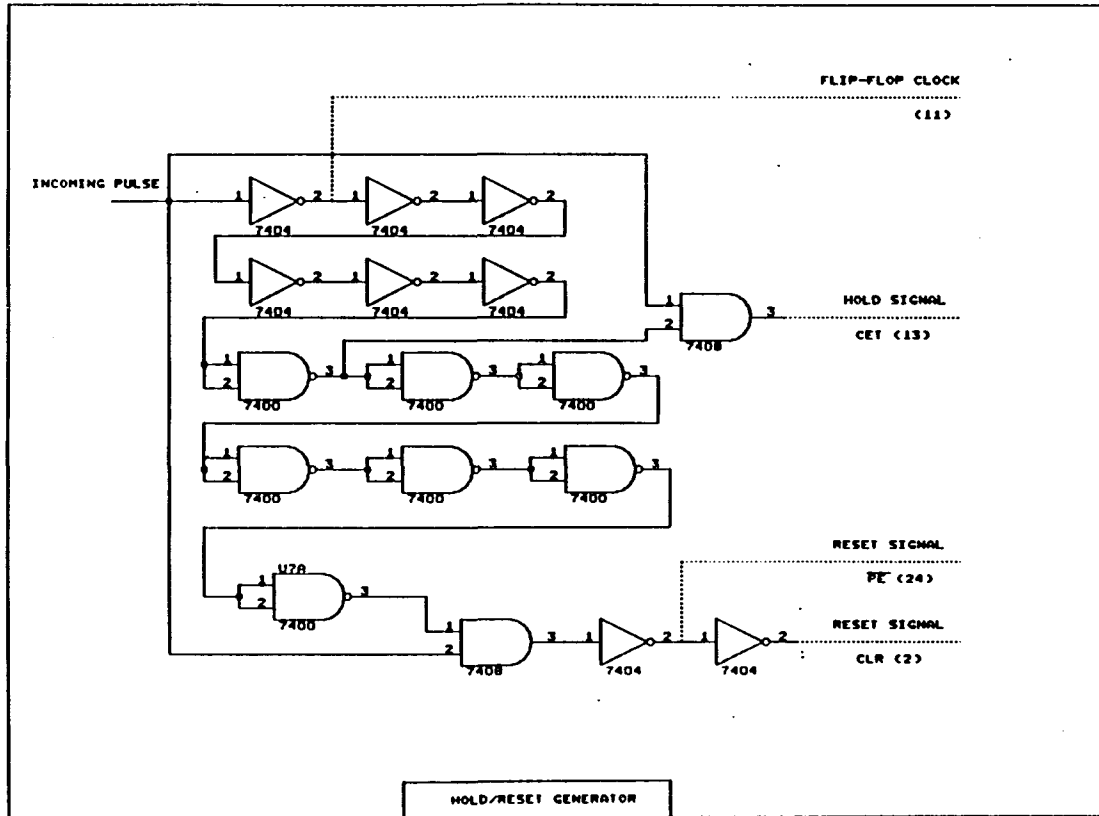
57D











This program is used to retrieve quantized mark size values from the Digitizer board.

```
DIM A%(1000), B%(1000)
OPEN "Data.out", FOR OUTPUT AS #1
C% = INP(&H3E9)
  FOR I% = 1 TO 1000
    A%(I%) = INP(3ED)
    B%(I%) = INP(3EB)
    PRINT #1, A%(I%), B%(I%)
  NEXT I%
CLOSE # 1
END
```

REFERENCES

- [1] A. B. Marchant, *Optical Recording, A Technical Overview*, Addison-Wesley, New York, 1990, ch. 4.
- [2] M. Mansuripur, *Principles of Optical Data Storage*, ch. 1, to be published in May 1992.
- [3] E. A. Lee and D. G. Messerschmidt, *Digital Communication*, Kluwer Academic Publishers, Boston, 1988.
- [4] R. L. Adler, "Algorithms for Sliding Block Codes, An application of Symbolic Dynamics to Information Theory," *IEEE Trans. Inform. Theory*, Vol. IT-29, pp. 5-22, Jan, 1983.
- [5] M. K. Liu, "Jitter Model and Signal Processing Techniques for High Density Optical Data Storage," *IEEE J. Selec. Areas in Comm.*, Vol. 10, No. 1, Jan. 1992.
- [6] M. K. Liu, S. Gupta, and B. Tehranchi, "Intersymbol Interference Characterization and Equalization for High-Density Optical Data Storage," paper submitted to *IEEE Global Telecom. Conference*, Apr. 1992.
- [7] R. Wood, "Magnetic and Optical Storage Systems: Oppprtunities for Communications Technology," in *Proc. ICC '89*, 1989, pp. 1605-1612.
- [8] D. G. Howe, "Signal-to-Noise (SNR) for Reliable Data Recording," *SPIE, Optical Mass Data Storage II*, Vol. 695, pp. 255-261, 1986.
- [9] H. Burkhardt, "Phase Detection with Run-Length-Limited Codes," *IBM Tech. Disclos. Bull.*, Vol. 24, no. 1B, p. 683, June 1981.
- [10] L. P. Huelsman and P. E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill, New York, 1980.
- [11] L. P. Huelsman, *Basic Circuit Theory*, Prentice-Hall, Englewood Cliffs, N.J., 1984.
- [12] D. F. Stout and M. Kaufman, *Handbook of Operational Amplifier Circuit Design*, McGraw-Hill, New York 1976.
- [13] S. Gupta, *ISI Characterization and Equalization for High Density Optical Data Storage*, Masters thesis submitted to the University of Arizona, May 1992.
- [14] W. R. Blood Jr., *MECL System Design Handbook*, Motorola Inc., 1971.
- [15] W. L. Hunter, *Master Handbook of Digital Logic Applications*, Blue Ridge Summit, PA, 1976.

- [16] M. Sargent and R. L. Shoemaker, *The IBM PC From Inside Out*, Addison-Wesley, New York, 1986.
- [17] *IBM PC Technical Reference*, IBM Corporation, Boca Raton, FL, 1985.
- [18] B. P. Lathi *Modern Digital and Analog Communication System*, Holt, Rinehart, and Winston, New York, 1983, Ch. 5.