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Analysis of plasma etch defects utilizing a comb test structure

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ANALYSIS OF PLASMA ETCH DEFECTS UTILIZING A COMB TEST STRUCTURE

by

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ABSTRACT

Three metal compositions are patterned via plasma etching into comb structures. The comb structures have pitches of 4 μm, 5 μm, 7 μm and 12 μm, with a line width of 2 μm, on a field oxide of 8,000 Angstroms thickness, using <111> p - type substrates. These comb test structures have been used to determine the number of bridges, and thus the yield, of the metal compositions: pure aluminum, silicon(2%)-aluminum, and copper(0.5%)-silicon(2%)-aluminum. Bridge failures are photographed and classified according to the source of the defect. The defects due to plasma particles are used to determine a yield model for this etch process. Through the use of yield model and test structure data the etch process is evaluated for the different metal systems. This allows a quantitative comparison of the systems in terms of defect clustering, defect density and defect size distribution, and hence projections for the best yielding process via the yield model.

CHAPTER 1

INTRODUCTION

Particles and process defects are some of the largest yield inhibitors within any integrated circuit fabrication plant. Defects can be reduced to manageable levels with the use of yield enhancement test structures. These test structures consist of measuring short-circuit bridges between conductors or open-circuits in conductors, and using one of several established yield models to predict future yield as well as monitoring yield improvement. The model used depends upon the size of the defect monitor and the amount of defect clustering in the product measured.

Plasma etch defects are one of the greatest areas of difficulty in integrated circuit manufacturing. With device geometries shrinking, the need for more accurate etch processes is growing. Thus, plasma metal etch is virtually a certainty for many I.C. manufacturers. The defects associated with plasma etching are becoming one of the greatest problems in manufacturing high density integrated circuits.

The focus of this paper is to utilize a comb test structure to locate and analyze the defects found on plasma etched silicon aluminum, copper silicon aluminum

and pure aluminum. A yield model is then utilized to accurately predict future yields for these metallization processes and determine if any defect clustering occurs for these processes.

1.1 Yield Models

During the past 25 years several yield models have been developed for use in industry, especially with application to modeling yields in wafer fabs. The most popular models include the Poisson Model, the Seeds/Price Model, and the Stapper Model. Another method of defect analysis recently introduced is the correlation function.

Following is a brief review of these models for their comparison later in this text.

1.1.1 Poisson Yield Model

One of the first yield models used to predict integrated circuit yields began with work by Hofstein and Heiman [1] in 1963 on circuits containing field effect transistors. In their research Hofstein and Heiman proved that low yields due to pinholes in the gate oxides of field effect transistors could be modeled by the Poisson yield model:

$$Y = e^{-NA_GD} \qquad (1)$$

Where N = the number of FET transistors, A_G = gate area of each transistor, and D = defect density. This model has become known as the Poisson yield model, and has proven to be very accurate in predicting yield for die with area below approximately 0.25 cm^2. In order to use the Poisson statistics for this model, defects must be randomly and uniformly distributed, but this assumption does not hold true when defects are clustered in regions on a wafer. Defect clustering can cause areas of a wafer to have fewer defects, (and thus higher yield), than would otherwise be predicted by a random yield distribution [2].

1.1.2 Seeds/Price Yield Model

In 1964 B.T. Murphy of Bell Labs [3] noted that since defect and particle densities vary widely from run to run, the assumption of uniform defect densities for Poisson statistics was not valid. He then proposed summing the defect densities on all wafers using a normalized probability distribution function of defect densities f(D). This resulted in eq. (2).

$$Y = \int_0^\infty e^{-AD} f(D)\, dD \qquad (2)$$

In 1967 R. B. Seeds analyzed wafer maps of die consisting of four logic gates [4] using a window method, where the yields for blocks of two, four, nine, and sixteen die were combined to develop a general yield model. Seeds determined that his yields consisted of a large number of die with low defect densities and a small number of die with high defect densities. He then used an exponential defect density distribution, f(D), as a normalization function to account for the varied (nonrandom) defect distributions:

$$f(D) = \frac{e^{-D/D_0}}{D_0} \qquad (3)$$

in Murphy's yield model, eq. (2), resulting in:

$$Y = \frac{1}{1 + AD_{av}} \qquad (4)$$

D_{av} is the average defect density and A is the critical chip area. This model predicted higher than actual yields for Seeds' own data, but is still used in industry today - perhaps by overzealous yield engineers. In 1970 John Price of Hewlett Packard [5] determined that this model

could also be derived from Bose - Einstein statistics assuming that particles and defects are indistinguishable. Price's yield model is:

$$Y = \frac{1}{(1 + AD_0)} \qquad (5)$$

or, generally, with n = the number of critical mask levels:

$$Y = \frac{1}{(1 + AD_0)^n} \qquad (6)$$

For increased area or defect density, the Seeds/Price model predicts yield to drop less rapidly than the Poisson model, but again the yield is optimistic even in the presence of defect clustering.

1.1.3 Negative Binomial (Stapper) Model

Localized groups of three or more adjacent failing test sites in this study are defined as defect clusters. Defect clusters cause a variation in defect densities across the wafer and thus create error in the Poisson and Seeds/Price models. The yield models noted in (1), (4) and (5) are accurate until severe defect clustering occurs. Defect clustering can occur due to complex integrated circuit manufacturing processes, or due to

dirty integrated circuit fabricators [6]. The negative binomial model uses the ratio of the square of the defect density to the variance in the defect density as a cluster parameter, α, to describe clustered defects in the yield model. In July 1973 C.H. Stapper of IBM, published a paper [7] presenting the derivation of the negative binomial yield model:

$$Y = (1+AD_0/\alpha)^{-\alpha} \qquad (7)$$

where

$$\alpha = \frac{D_0^2}{var(D)} \quad ,$$

$$var(D) = \frac{var(\lambda)-\lambda}{A^2} \quad , \qquad (8)$$

$$D_0 = \frac{\lambda}{A}$$

and λ = number of defects per die.

Here α is the cluster parameter, increasing with decreasing variance in the distribution of defects, D. This model is derived by substituting the gamma distribution function into Murphy's original yield model eq. (2):

$$f(D) = \frac{1}{D_0^{\alpha}\Gamma(\alpha)} D^{(\alpha-1)} e^{-(D/D_0)} \qquad (9)$$

The gamma function by definition is:

$$\Gamma(\alpha) = \int_0^{\infty} x^{\alpha-1} e^{-x} dx \qquad (10)$$

It is interesting to note that if the variance of the average number of defects per die is low and the defects have little clustering, α is high and the gamma distribution approaches that of the Poisson distribution. If the variance of the defects is high the defects are highly clustered, and α is small. In this case the distribution predicts a higher probability of a greater number of die with fewer defects overall, and the yield is greater. A typical value of $\alpha \approx 2$ has been reported [8-10] for a variety of logic circuits. Note also that for $\alpha = 1$ the negative binomial yield model is equivalent to the Seeds/Price Model in eq. (4).

1.1.4 Correlation Function Technique

One final method for defect cluster yield analysis, but not specifically used in this study, is the correlation function technique for characterization of defect clustering [11]. The models previously discussed do not specifically model the width of the defect cluster, as might be needed in the design of redundant circuits such as memories. Correlation functions are applied on redundant chips to determine the width of the defect cluster, in order to better plan the distance needed between redundant pairs to avoid a possible defect cluster. This method is not a model for defect clustering, but rather a statistical tool for use in planning redundant circuits.

The correlation function, P(R), describes the probability that two defects are separated by a distance R.

$$P(R) = \frac{K}{R}\int_{-\infty}^{\infty}\int f(x_0,y_0)\cdot(f(x_0 + x, y_0 + y)\,dx_0 dy_0$$

$$R = (x^2+y^2)^{0.5}$$

Where K is a normalizing constant and (x_0,y_0) is the location of a defect. $P(\infty)=(D\cdot dA)^2$ because the probability of one defect occurring is the product of the defect density and the incremental area, dA. The probability of the second defect at $R=\infty$ is also $D\cdot dA$, thus the probability of both defects is the product of the two probabilities, $(D\cdot dA)^2$. If clustered defects are present, as R decreases, P(0) may be many times its $P(\infty)$ value. P(R) can be applied to defect maps and histograms of defects per unit distance to determine the amount of clustering for a given process or wafer lot.

1.2 Plasma Particles and Contamination in Dry Etching Aluminum and Aluminum Alloys

Past studies [12] have shown that pure exposed aluminum will easily etch with Cl or Cl_2 to create $AlCl_3$, with or without a plasma. The thin (25 Angstroms) native oxide Al_2O_3, however, will not react with Cl or Cl_2. Dry etching aluminum has thus become a four stage process [13] including removing the native oxide layer, etching the underlying aluminum, overetch to remove residual aluminum, resist strip and passivation for corrosion resistance.

1.2.1 Aluminum Etch Overview

The initial stage of aluminum etching is commonly referred to as the *initiation* step [14]. Typically in this stage native aluminum oxide is removed by sputtering with reactive ions (RIE) and by chemical breakdown. BCl_3 and CCl_4 are typical compounds used to reduce the oxide by dissociation, for example:

$$Al_2O_3 + 2BCl_3 \rightarrow 2AlCl_3 + B_2O_3$$

or

$$Al_2O_3 + 2CCl_3 \rightarrow 2AlCl_3 + CO + CO_2$$

Unfortunately oxidation of the resultant compounds, $AlCl_3$ and $SiCl_4$, can cause particulate formation in the form of Al_2O_3 and SiO_2 [13]. These particles can be

deposited on the etch surface and cause etch blockage or metal bridging.

The second stage in aluminum etching is the *bulk aluminum etch* [14]. In this stage chemistries of BCl_3, N_2 and Cl_2 are often used to accelerate the aluminum etch to a point where the outer edge of the wafer begins to clear. In stage three, the *overetch* stage, low flows (5-15 sccm) of Cl_2 at low pressure (75-125 mTorr) are typically used to clear any residuals at a fast etch rate (>3000 Ang./min.) [14,15].

Stage four, the final stage, is a resist strip and wafer passivation stage used to plasma ash the resist in an O_2/N_2 plasma, and passivate the wafer with the electrode chuck at an elevated temperature (300°C), using CF_4 or CHF_3 for passivation to protect against post-etch corrosion.

Post-etch corrosion is a typical problem in etching aluminum [16]. Corrosion is a result of hydrolysis of chlorine or chlorine containing residues (i.e. $AlCl_3$) which remain on the resist or film after etch. These residues can form HCl and corrode the aluminum:

$$2Al + 6HCl \rightarrow 2AlCl_3 + 3H_2$$

Thus more $AlCl_3$ is produced to fuel the corrosion further. Several methods have been developed [13] to alleviate corrosion, they include:

1. Rinsing the material with cold deionized water after etch to clean the chlorine off the wafers.
2. Plasma ashing resist with O_2 in the etch chamber to remove chlorinated resist and restore the aluminum passivation Al_2O_3.
3. Exposing the aluminum to fluorine plasma (i.e. CF_4) before removal from the chamber to passivate the aluminum. CF_4 is thought to passivate aluminum by replacing the chlorides with noncorrosive fluorides, through production of nonhydroscopic AlF_3 [13,16]. CHF_3 deposits a polymer film over the aluminum sealing it against moisture [13].

One or two atomic percent silicon is often added to the aluminum to prevent aluminum from spiking through shallow junctions. The result is that chlorine and silicon combine to form $SiCl_4$, which is volatile at room temperatures, thus SiAl is easily etched in chlorine containing gases. A small amount of copper, however, is also added to prevent electromigration at high current densities, and Cu is relatively nonvolatile below

temperatures of approximately 175°C [13] when combined with chlorine (CuCl). Thus either higher power and higher pressure ion bombardment is used to etch CuSiAl, or the substrate temperature is increased to increase the volatility of CuCl. One result of these steps is resist erosion and resist sputtering onto the etch surface, perhaps preventing etching and causing bridging. Another common occurrence due to copper's nonvolatility are copper nodules on the etched surface that can cause severe bridging. An example of a copper nodule can be seen in Fig. 1.1. The etch byproduct $AlCl_3$ can also attack the resist and cause damage to the wafer surface, although deep ultraviolet resist treatment will harden the resist and help prevent resist attack.

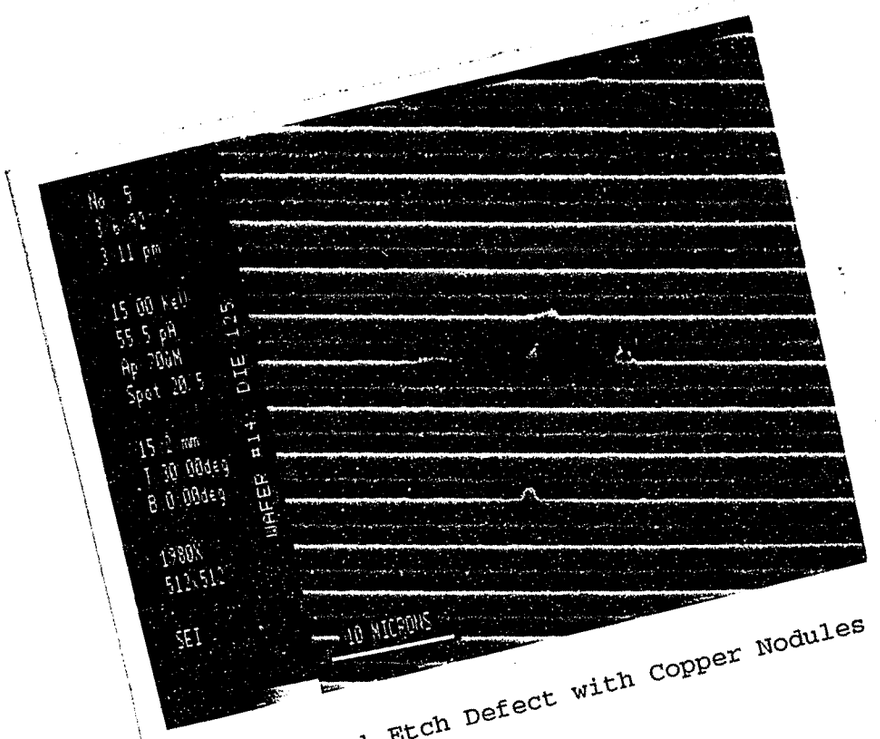

Figure 1.1 Etch Defect with Copper Nodules

1.2.2 Plasma Particle Trapping and Deposition

Particle trapping and deposition in a plasma has been the topic of several recent studies [17-21]. Dense clouds of particles have been observed suspended at the plasma/sheath boundary above the wafer in parallel plate rf generated plasmas [18]. The particles have been found to be negatively charged [19] and thus electrostatically trapped in clouds whose shape is determined by the electrode topology and material. Laser light scattering measurements have been utilized to observe a ring of particles around the edge of the wafer, 5-6 mm above the wafer, and extending 1-2 cm out from the edge of the wafer [20], as well as a dome of particles in the center of the observed wafer [20] 5-6 mm above the wafer, extending up approximately 5-6 mm. These particles range in size from tenths of μm to tens of μm, and the number and size of particles has been shown to vary according to plasma processing conditions [21]. Particle concentration in the traps above the wafer in the plasma has been shown to change linearly with rf power. As rf power is decreased, the particles gradually leave the trap and are carried to the pump port. If the rf were to be turned off altogether the particles would drop on the wafer causing particulate contamination [21]. Also, if the number of particles

deposited on a wafer were as large as those seen by [21], this could be catastrophic. Particle densities in the plasma as high as 10^7 cm^{-3} for particles 0.2 μm in diameter have been observed in [18].

According to a study in the May 1985 edition of Semiconductor International [22], particulate contamination can also occur in a plasma from wafer transport materials and operation, paper products near the etchers as well as the environment.

All the studies noted above used unpatterned wafers as test vehicles in the plasma. This study is unique in that it utilizes patterned wafers.

CHAPTER 2

EXPERIMENTAL METHODS

2.1 The Test Structure

The comb test structure used in this study consists of two interdigitated comb structures, as shown in Figure 2.1.

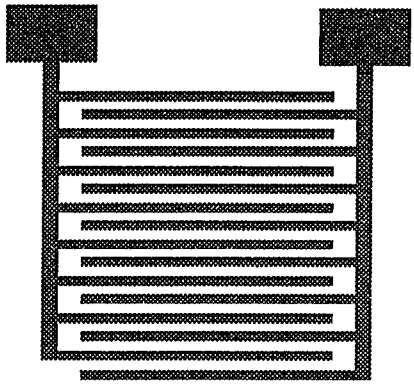

Figure 2.1 Comb Structure

This structure has been used for many years by the semiconductor industry to monitor defect levels in single process steps or in multiple process steps. Comb test structures are usually described by their area and pitch, where pitch is the width of the metal line plus the space between metal lines. In this study the test structure consists of a minimum line width of two μm, with four separate stacks of eight combs, with pitches of four μm, five μm, seven μm and twelve μm to account for a large array of defect sizes.

The structures were arranged in stacks of eight in order to use a windowing technique to determine the defect density (i.e. defects/cm^2), and to eventually establish a yield model.

Following are the processing steps included in the manufacture of these monitors:

1. Grow 8,000 Angstroms thermal oxide on 100 mm <111> p - type substrates.
2. Sputter deposition of the metal using a Varian 3290. All metals were deposited in a magnetically confined Ar plasma at 7 mTorr to prevent collisions in the chamber. The etcher conditions are noted in Table 2.1:

METAL	**SiAl**	**CuSiAl**	**Al**
Temp.	325°C	200°C	275°C
RF bias	no	yes	no
Thickness	9000A	7000A	11000A

Table 2.1 Etcher Conditions

3. Photolithography via Perkin Elmer 240 projection aligner with 1.15 μm HPR504 positive resist baked at 115°C for 60 s., and deep UV treatment to 200°C.
4. Plasma etch via Drytek Quad Plasma Etcher. An etch process similar to that described in section 1.2.1 was utilized for this study, including resist strip and passivation. The etch procedures for each material are shown in Tables 2.2 to 2.4.

A. Silicon Aluminum

(all flows in sccm)

Parameter	Step 1	Step 2	Step 3	Step 4	Step 5
BC13	50	50	50		
C12		18	8		
N2		40	40		
N2H2				400	
O2				4000	
CF4					100
Power(W)	125	125	125	µW	µW
Pressure(mT)	300	300	300	3000	1000
Time(min:sec)	:15	:53	1:00	:30	:45

Table 2.2 Silicon Aluminum Etch Procedure

B. Copper Silicon Aluminum

Parameter	Step 1	Step 2	Step 3	Step 4	Step 5
BC13	50	50	50		
C12		18	8		
N2		40	30		
N2H2				400	
O2				4000	
CF4					100
Power(W)	125	125	125	µW	µW
Pressure(mT)	300	275	275	3000	1000
Time(min:sec)	:15	:48	:41	:30	:45

Table 2.3 Copper Silicon Aluminum Etch Procedure

C. Aluminum

Parameter	Step 1	Step 2	Step 3	Step 4
BC13	50	50	50	
C12		18	8	
N2		40	40	
N2H2				400
O2				4000
Power(W)	125	125	125	µW
Pressure(mT)	300	300	300	3000
Time	:15	1:00	1:15	:30

Table 2.4 Aluminum Etch Procedure

µW = Microwave strip and passivation with no power setting

The system parameters for this study included an electrode spacing of 6.985 cm, with the upper electrode temperature 70 °C and the lower electrode temperature 50°C. The chamber wall temperature was 80°C, with the strip chamber electrode temperature 300°C. The etcher showerhead array was 2.92 cm with a hole diameter of 0.762 mm.

As a test of the structures, yield models, and the metal deposition process itself, the structures were fabricated using three typical metal compositions used in semiconductor processing: 11,000 Angstroms film of pure Aluminum (Al), 9,000 Angstroms of Silicon Aluminum (SiAl) and 7,000 Angstroms of Copper Silicon Aluminum (CuSiAl). All metals were etched to specifications including less than 0.1 µm critical dimension loss, with ±5% critical dimension uniformity, and ±5% etch rate uniformity. The resultant etch profile in all cases was specified to be greater than 85 degrees, and with selectivity to resist maximized at 7:1. The maximum substrate removed during the etch was specified at 200 Angstroms.

The comb test structures were printed across an entire 100mm wafer, for a total of 222 die sites. Each die site contained eight individual comb structures at each of the four pitches. Three wafers of each metal composition were manufactured resulting in a total of 5,328 test structures for each of the metal compositions.

The structures were tested for metal shorts, or bridging, by forcing 5 V. across one comb structure, and measuring the leakage current between the adjacent interdigitated comb. Empirically it was determined that leakage greater than 10 nA is a short between the two combs, and thus was used as the limit for the Keithley parametric tester model 350i.

A wafer map for each wafer was generated to help locate the defects. Die sites were inspected for as many of all types of defects as possible, to identify their source. Careful inspection of the defects through an optical microscope and/or a scanning electron microscope (SEM) was required to determine the cause for each defect and categorize it appropriately.

After each defect was categorized, the plasma etch defects were used to gather yield model data and to evaluate the etch process. This provided a better understanding of how to model yields due to plasma etch and to utilize the window methodology in determining a yield model for fitting to the Stapper yield model.

2.2 Defect Types

The types of defects found on metal comb test structures can be categorized as etch defects, photolithographic defects or oxide defects. Figures 2.2 to 2.4 give examples of each of these types of defects. Etch defects occur when particles fall onto the wafer prior to etch, or during etch, blocking the plasma etch process. Etch defects are characterized by the resist pattern in relief in the area of the defect, with no distortion. These occur if a resist pattern had been masked by an etch particle during the etch. The outer edges of an etch particle tend to be thinner than the immediate area surrounding the particle. Two possible reasons for this are undercutting around the particle due to isotropic etch, and partial etching of the masking particle itself [23].

Photolithographic defects consist of resist blobs and planar defects. Resist blobs are characterized by distorted pattern lines in the region around the defect, with no particle visible within the defect structure. These may be due to lumps of dried photo resist on the wafer, or due to resist blobs deposited onto the wafer during resist spinning. Planar defects are smaller defects that can result from "anomalies in the positive photoresist pattern after the development stage" [23]. These areas of

undeveloped resist will block the plasma etch process and create a bridge in the pattern.

Particles from the underlying oxide can be coated with metal; but if large enough, a particle may protrude through the metal film. The particle protrusion may cause resist pooling, and distort the intended pattern.

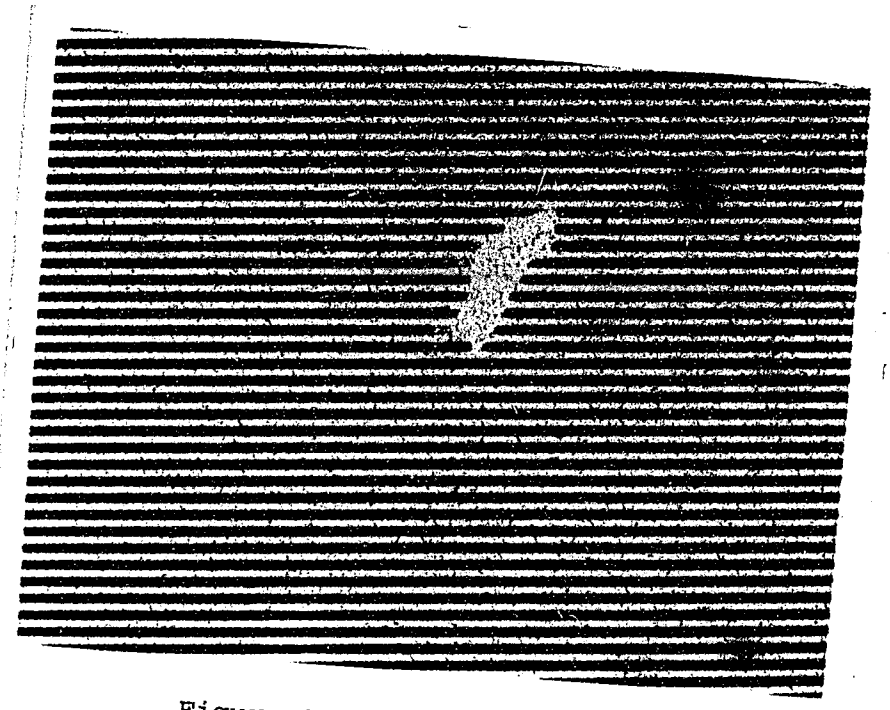

Figure 2.2 Etch Defect Example

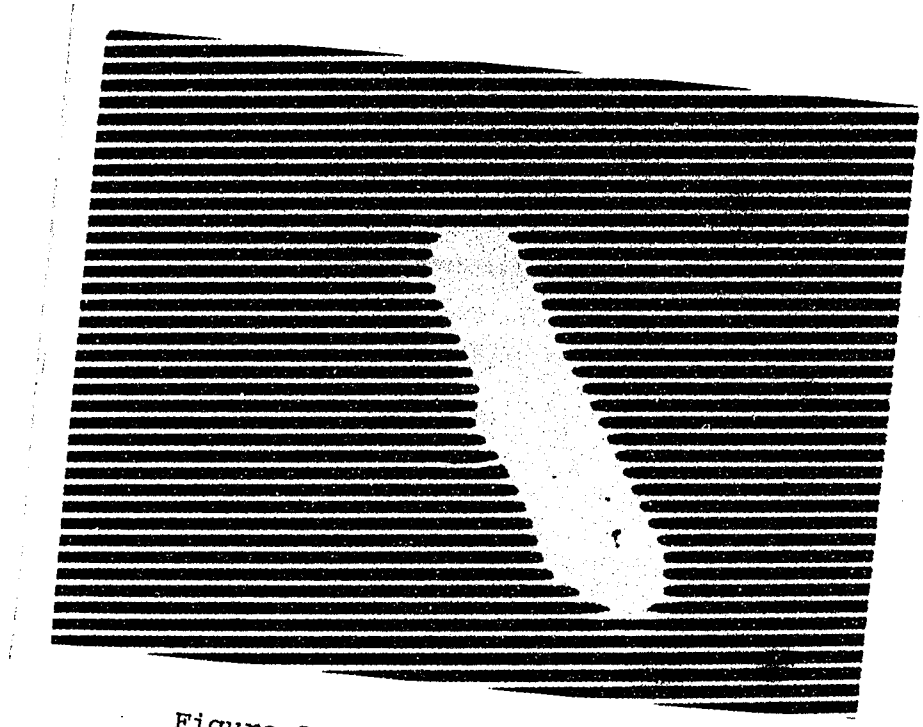

Figure 2.3 Photo Defect Example

Figure 2.4 Oxide Defect Example

CHAPTER 3

RESULTS AND DISCUSSION

The following calculations compare the yields using the models discussed. It will be shown that the Stapper model gives the best predictions for the yield of the test structure. Two effects are readily apparent upon observation of the data. First, the test structure is very small compared to a typical VLSI logic chip, and thus its yields are very high. Second, with a die so small, most yield models will be accurate. CuSiAl yield monitors yielded slightly below the SiAl yield monitors due to an etch residue. X-ray analysis of the residue indicated the presence of copper, and the problem was unresolved at the end of this study, although the yields for CuSiAl monitors still averaged over 95%. This may indicate a problem with this etch recipe and metal composition. Further work may prove this metal composition requires a different etch system or recipe.

It should be noted that the ring and disk particle structures discussed in 1.2.2 were not evident on the wafer yield maps. The particles, in this case, may have been smaller than the resolution of the test structure (2 μm) and thus were not measured as bridges. It was noted in [20], however, that the "ultimate disposition of particles is, in part, determined by the materials, design and operation" of the plasma tool.

3.1 Types of Defects and Defect Charts

Defect cause charts were generated after evaluation of each defect. The maps are given on the following pages as Figs. 3.1, 3.2 and 3.3. It can be seen that the majority of the defects are either etch defects or photo defects. Examples of etch defects, photo defects and particles are given in Figs. 3.4, 3.5, and 3.6. Fig. 3.5 gives an example of a photo defect traced to be a mask defect. Most of the pre - etch defects were identified as scratches on the resist before etch, as shown in Fig. 3.7, and resist scalloping, shown in Fig. 3.8, due to transportation of the wafers to Drytek Corporation, in Wilmington, Massachusetts for plasma etch. Resist defects, such as resist blobs, also comprised a large portion of the photo defects. These were due to splashback from the coaters in resist deposition, because of an exhaust problem in the resist coater.

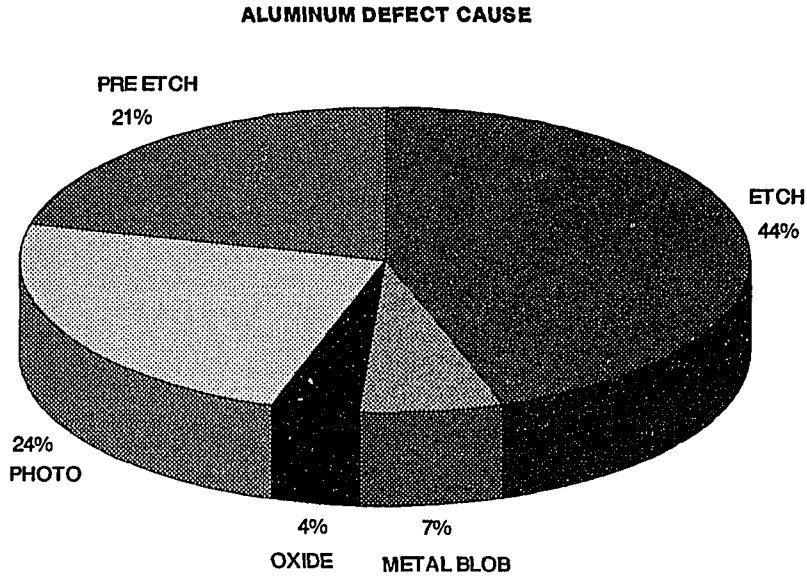

Figure 3.1 Defect Cause Map - Aluminum

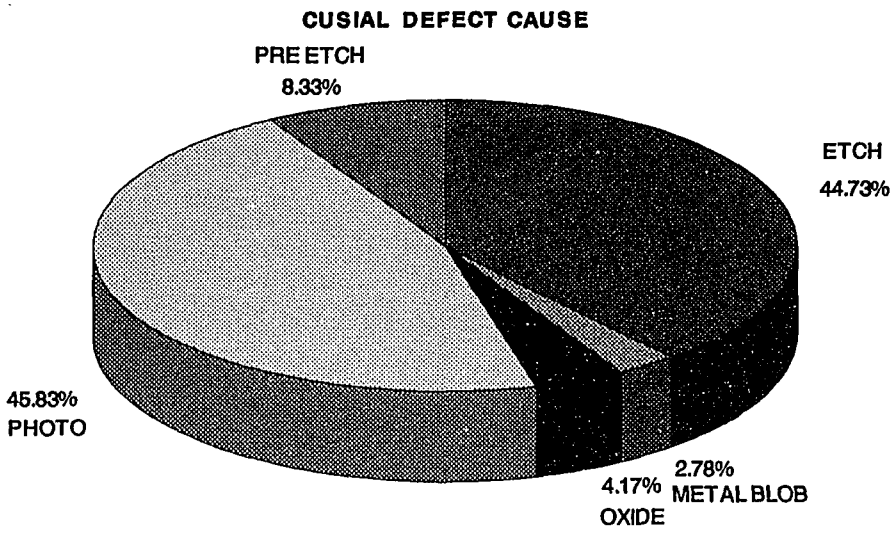

Figure 3.2 Defect Cause Map - Copper Silicon Aluminum

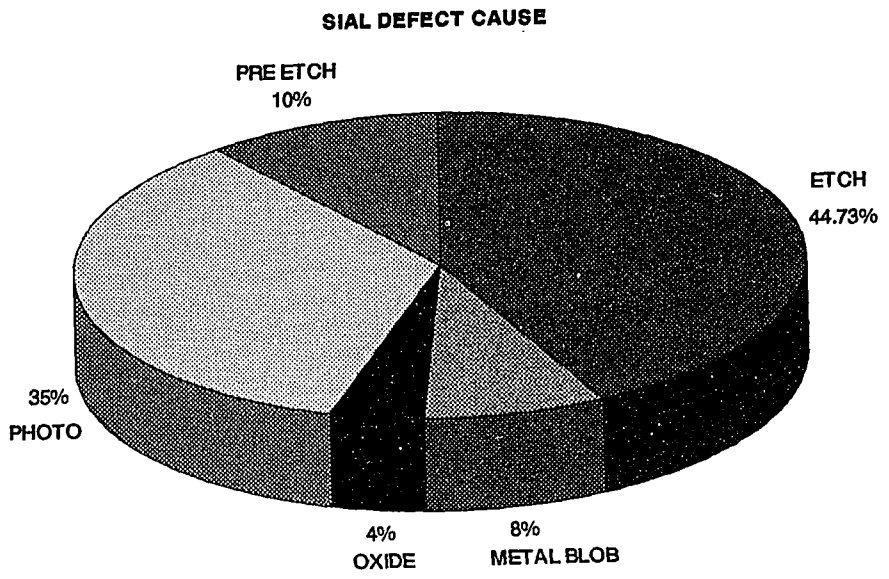

Figure 3.3 Defect Cause Map - Silicon Aluminum

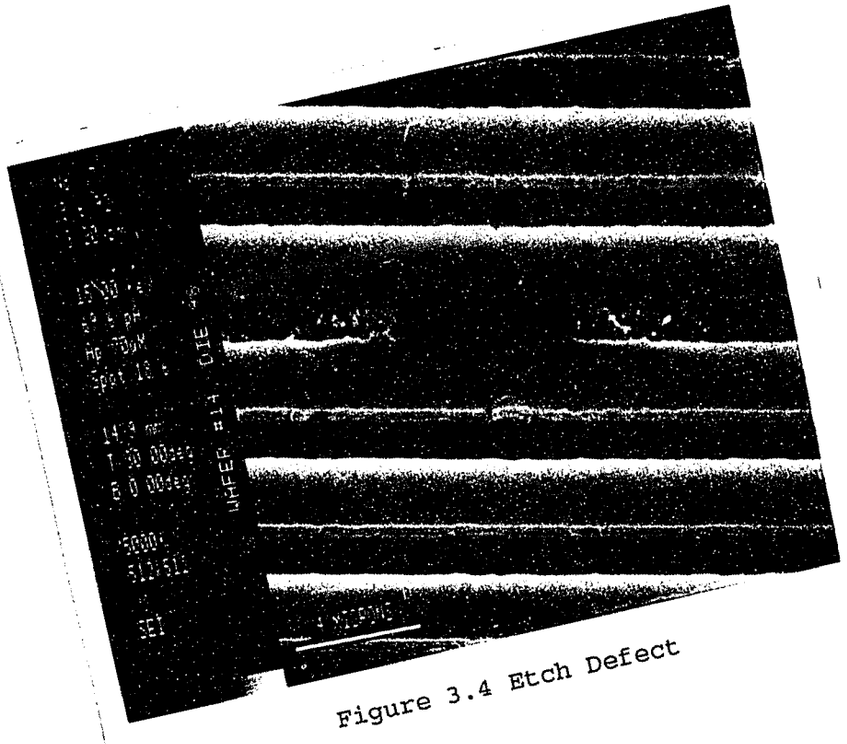

Figure 3.4 Etch Defect

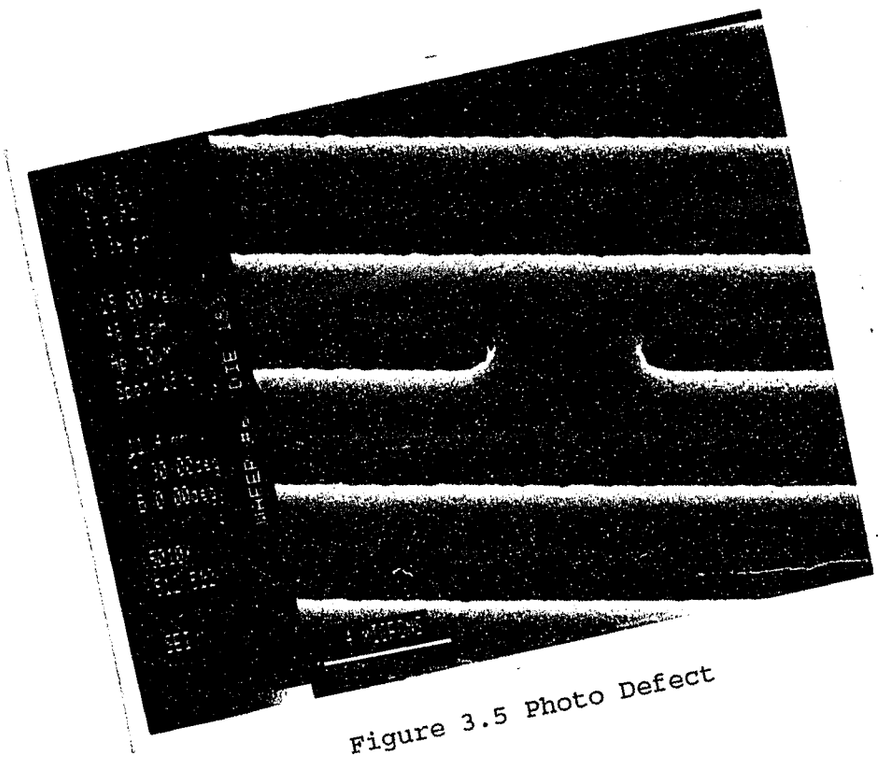

Figure 3.5 Photo Defect

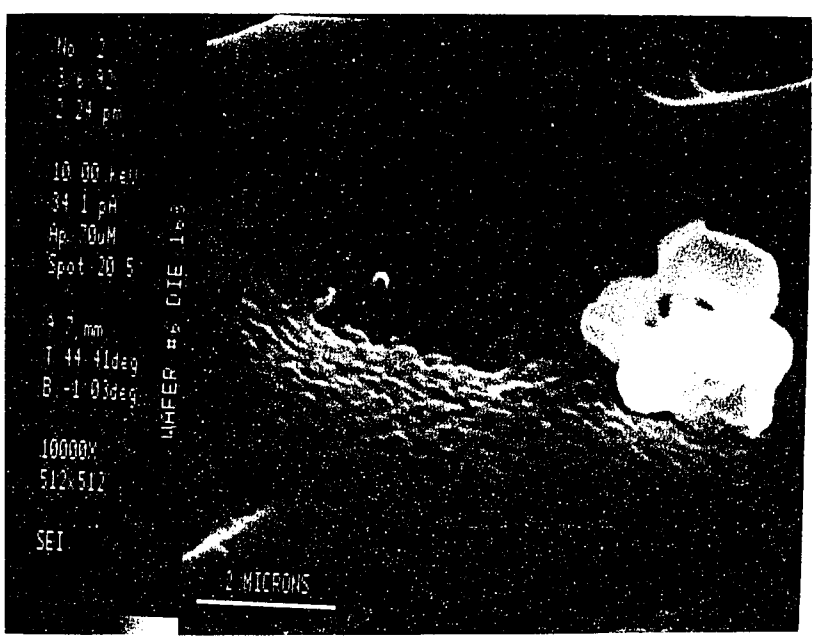

Figure 3.6 Particle Defect

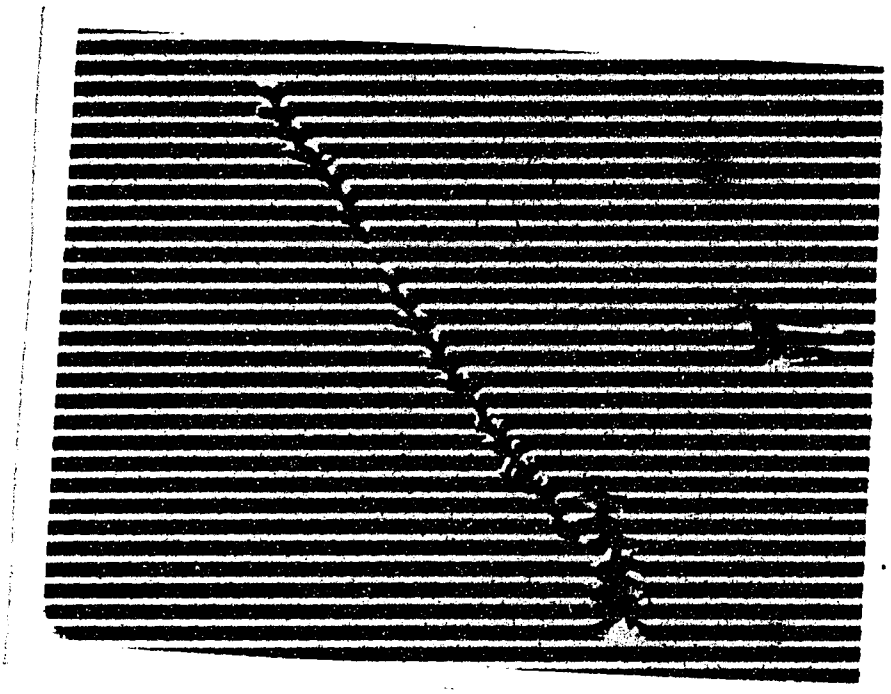

Figure 3.7 Pre Etch Scratch Defect

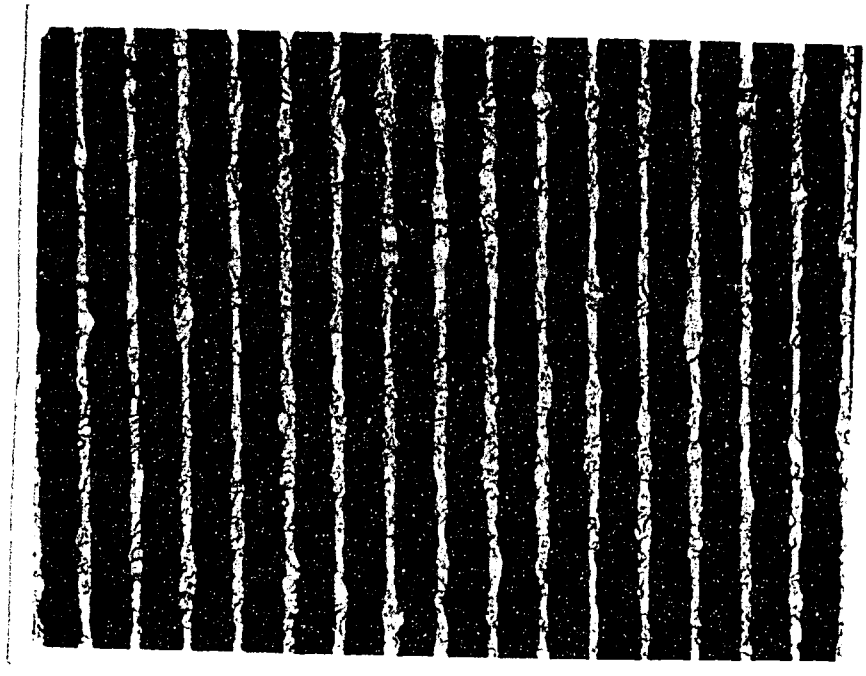

Figure 3.8 Scalloping

3.2 Yield Calculations and Model Comparisons

Yield calculations were done to investigate the accuracy of the various yield models. To obtain a complete synopsis of a process, it is important to develop yield models for stages within the process contributing to the majority of yield loss. The yield model for each individual stage within a process will help predict the yield for the overall process, and point out problems within the process.

Plasma etch defects and photo defects were found to be the largest yield inhibitors in this experiment, and thus their yield models, as well as the overall yield model, were investigated. In section 3.2.1 we will perform a sample calculation of the Stapper model for all defects in SiAl. Tables 3.1, 3.2 and 3.3 summarize the Stapper model parameters for all defects, plasma etch defects and photo defects. For all defects alpha averaged 0.038, indicating defect clustering, and for plasma etch defects alpha averaged 0.013, also indicating defect clustering. Photo defects had no clustering, with an average alpha of -1, indicating all the defect clustering in the overall yield model is from the plasma etch defects alone. In fact, with an alpha of -1, the Stapper model for photo defects becomes a binomial model (1 - AD). For large sample sizes and low defect probabilities, binomial distributions become very close approximations of Poisson distributions.

Metal	Di	Var(λ)	Var(D)	α
SiAl	1.212	0.0564	59	0.02489
CuSiAl	3.362	0.208	267	0.0423
Al	3.969	0.256	337	0.0467

Table 3.1 Stapper Model Data Summary for All Defects

Metal	Di	Var(λ)	Var(D)	α
SiAl	0.337	0.011	6	0.0189
CuSiAl	1.479	0.143	221	0.0099
Al	1.345	0.107	155	0.0116

Table 3.2 Stapper Model Data Summary for Plasma Defects

Metal	Di	Var(λ)	Var(D)	α
SiAl	1.140	0.025	-1.27	-1.025
CuSiAl	2.020	0.043	-3.95	-1.030
Al	1.140	0.025	-1.27	-1.025

Table 3.3 Stapper Model Data Summary for Photo Defects

This is seen in the model comparisons in section 3.2.2. These points are also graphically demonstrated later, in section 3.3.

3.2.1 Yield Model Calculations

SIAL:

The defect density can be calculated by dividing the total number of defects by the area:

$$D_i = \frac{\lambda}{A_R} = 1.212 \text{ defects/cm}^2$$

The variance in the number of defects:

$VAR(\lambda) = 0.0564$

is used in the equation for the variance in the defect density, eq. (8):

$$VAR(D) = \frac{0.0564 - 0.027027}{(0.0223)^2} = 59$$

to get a unitless measure of the defect density variation, α:

$$\alpha = \frac{D_i^2}{VAR(D)} = \frac{1.212^2}{59} = \underline{\mathbf{0.024}}.$$

3.2.2 Comparison of Calculated to Actual Yields

Tables 3.4 to 3.9 compare the yield models for the three defect types. The Stapper model is an excellent fit to the data when clustering is present, as indicated in Tables 3.5 and 3.7. As mentioned in the introduction, and verified here, with severe defect clustering the Poisson and Seeds/Price (S/P) models predict lower than actual yields whereas the Stapper model is very accurate.

Without defect clustering, such as the photo defects in this experiment, all three models predict yields very close to the actual results as seen in Tables 3.8 and 3.9.

METAL	ACTUAL YIELD %	POISSON CALC %	DELTA %	STAPPER CALC %	DELTA %	S/P CALC %	DELTA %
SIAL	98.2	97.3	-0.9	98.2	0.0	97.4	-0.8
CUSIAL	95.6	92.8	-2.8	95.8	+0.2	92.5	-3.1
ALUM	95.5	91.5	-4.0	95.2	-0.3	91.9	-3.6

Table 3.4 Yield Comparison for All Defects

	POISSON	STAPPER	SEEDS/PRICE
AVERAGE DELTA	-2.6%	-0.033%	-2.5%

Table 3.5 Average Yield Delta From Actual Yield for All Defects

METAL	ACTUAL YIELD %	POISSON CALC %	DELTA %	STAPPER CALC %	DELTA %	S/P CALC %	DELTA %
SIAL	99.4	99.3	-0.1	99.4	0.0	99.3	-0.1
CUSIAL	98.5	96.8	-1.7	98.6	+0.1	96.8	-1.7
ALUM	98.8	97.1	-1.7	98.5	-0.3	97.1	-1.7

Table 3.6 Yield Comparison for Plasma Etch Defects

	POISSON	STAPPER	SEEDS/PRICE
AVERAGE DELTA	-1.12%	-0.067%	-1.17%

Table 3.7 Average Yield Delta From Actual Yield for Plasma Etch Defects

METAL	ACTUAL YIELD %	POISSON CALC %	DELTA %	BINOMIAL CALC %	DELTA %	S/P CALC %	DELTA %
SIAL	97.4	97.5	+0.1	97.5	+0.1	97.5	+0.1
CUSIAL	95.5	95.6	+0.1	95.5	+0.0	95.7	+0.2
ALUM	97.4	97.5	+0.1	97.5	+0.1	97.5	+0.1

Table 3.8 Yield Comparison for Photo Defects

	POISSON	BINOMIAL	SEEDS/PRICE
AVERAGE DELTA	+0.100%	+0.067%	+0.133%

Table 3.9 Average Yield Delta From Actual Yield for Photo Defects

3.3 Yield to Area Curves and Failure Log Maps

Defect clustering can be seen in yield to area curves. Yield to area curves for plasma etch defects are shown in Figs. 3.9 to 3.12. The curvature arising from defect clustering is apparent in these plots. The calculated alpha for plasma etch defects for all three metals is much less than 0.1, indicating severe defect clustering. As seen in Figs. 3.9 to 3.11, comparing the resultant curves for plasma etch defect data to a Stapper model distribution with α = 100 (no defect clustering) highlights the effects of severe clustering in the etch defects. Fig. 3.12 plots yield vs. area for etch defects on all three metals for typical VLSI chip areas up to 2 cm^2. Note that the curves cross for die sizes larger than approximately 0.4 cm^2. Even though SiAl resulted in the best yield for this project, Fig. 3.12 indicates CuSiAl would yield best, under these conditions, for die at VLSI sizes. This is of utmost importance. Defect density alone cannot be used to determine which process would result in the largest yield. It is only through the use of defect clustering in the yield model that the largest yielding metal process can be chosen for this experiment. Thus an evaluation of a VLSI process/metal system based only on defect density and a Poisson distribution would not result in the appropriate conclusion as to which system is best. In Fig. 3.13 as defect clustering becomes more severe, alpha becomes smaller,

bending occurs in the yield vs. area curve, and it eventually becomes virtually parallel to the x-axis. Thus, for a given D_0 the yield for a process may be much higher with defect clustering, as opposed to a purely Poisson distribution of defects with no defect clustering.

The failure log maps in Figs. 3.14, 3.15 and 3.16 are another example of defect clustering. It can be seen from these maps that most die with defects tend to have more than one defect.

Yield vs. Area curves for photo defects are given in Fig. 3.17. The calculated alpha for all three metals is less than 0, indicating a binomial distribution with no defect clustering.

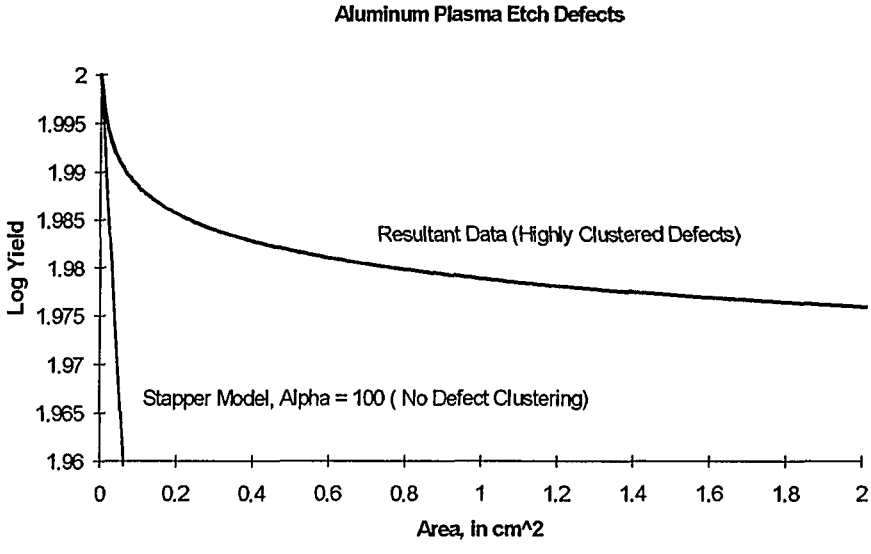

Figure 3.9 Yield vs. Area Etch Defects - Aluminum

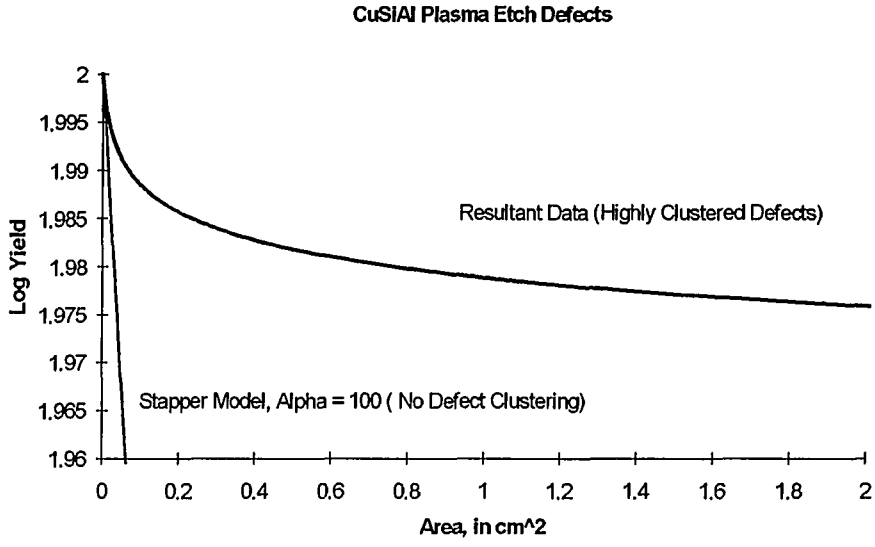

Figure 3.10 Yield vs. Area Etch Defects-
Copper Silicon Aluminum

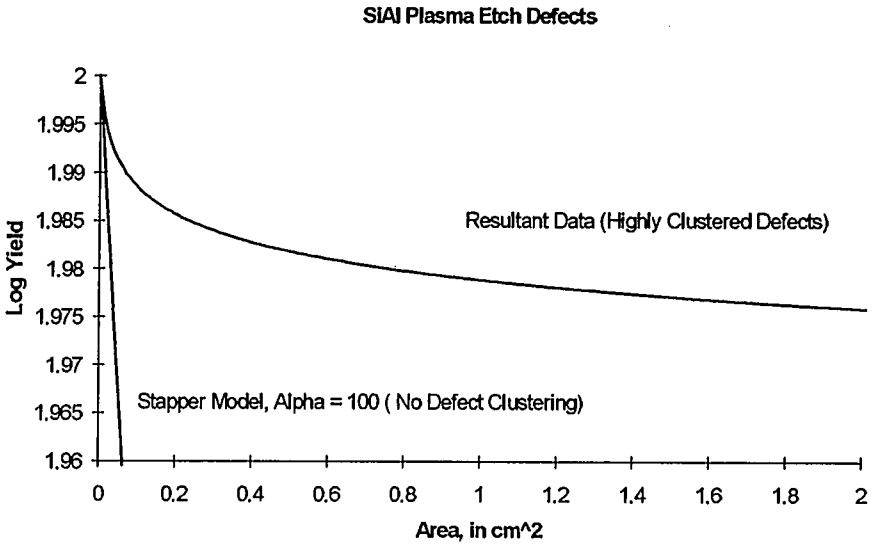

Figure 3.11 Yield vs. Area Etch Defects-
Silicon Aluminum

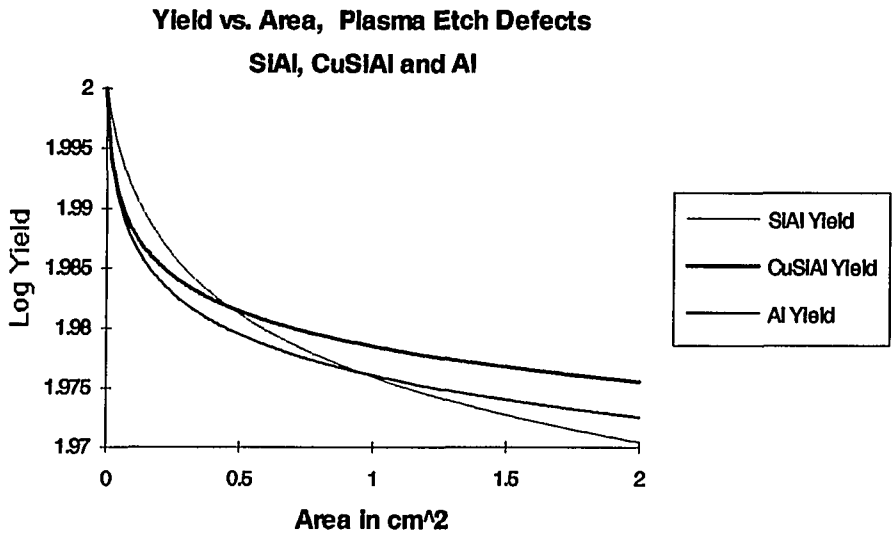

Figure 3.12 Yield vs. Area Etch Defects For All Metals

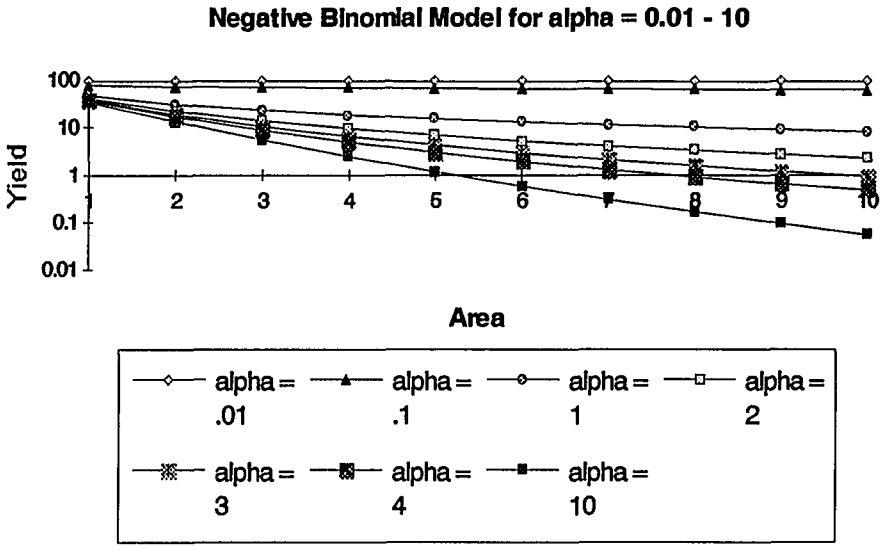

Figure 3.13 Stapper Model With Varying α

ALUMINUM FAILURE LOG MAP

```
    1 2 3 4 5 6 7 8 9 1 0 1 2 3 4 5 6 7 8 9 2 0
                      0
 1
 2
 3            * * * * * * * * * *
 4          * * * * * * * * * * * *
 5        * * * * * * * 0 2 * * * * * *
 6        * 2 * * * * * 1 * * * * * * *
 7      1 * * * * * * * * 7 * * * * * * 1
 8      * * * * * * * * * * * * * * 1 *
 9      * * * * * * * * * * * * * * * *
10      * * * * * * * * 1 * * * * * * *
11      * * 0 * * * * * 0 * * * * 0 * *
12      * * * * * * * * * 3 1 * * * 1 *
13      * * * * * * * * * * * * * * * 2
14      * * * * 3 * * 4 5 * * * * * * *
15      * * * * * * 4 * 1 * * * * * * 1
16        * * * * * * * * * * * * * * *
17        1 * * * * * * 0 * * * * * * *
18          * * * * * * * * * * * * *
19              * * * * * * 1 1 1
```

* = good die

\# = number of defects at this site

0 = blank space

Figure 3.14 Failure Log Map - Aluminum

CUSIAL FAILURE LOG MAP

```
                                1                   2
    1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0
 1
 2
 3          * * * * * * * * * *
 4      * * * * * * * * * * *
 5        * * * * * * 0 * * * * * * *
 6        * * * * * * * * * * * * * *
 7    * * * * * * * * * * * * * * * *
 8    * * * * * * * * * * * * * * * *
 9    * * * * * * * * * * * * * * * *
10    * * * * * * * * * * * * * * * *
11    * * 0 * * * * 0 * * * * 0 * 8
12    * * * 1 * 3 * * * 3 * * * * *
13    * * * * 3 * * * * * * 5 * * *
14    * * * * * * 1 * * * * * * * *
15    1 * * * * * * * * * * * * * * *
16      * * * * * * * * * * * * * *
17      1 * * * * * 0 * * * * * * *
18        * * * * * * * * * * * *
19          1 2 1 1 * * * * 1
```

* = good die

\# = number of defects at this site

0 = blank space

Figure 3.15 Failure Log Map -
Copper Silicon Aluminum

SIAL FAILURE LOG MAP

```
                                 1                   2
    1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0
 1
 2
 3           * * * * * * * * * *
 4         * * * * * * * * * * * *
 5       * * * * * * 1 0 * * * * * *
 6       * * * * * * * * * * * * * *
 7     * * * * * * * * * * * 1 * * * *
 8     * * * * 1 * * * * 1 * * * * * *
 9     * * * * * * * * * * * * * * * *
10     * * * * * * * * * * * * * * * 1
11     1 * 0 * * * * 0 * * * 2 0 * * *
12     * * * * * * * * * * * * * * * *
13     1 * * 1 * * * * 4 * * * * * * *
14     * * * * * * * * * * * * * * * *
15     * * * 2 1 * * * * * 2 * * * * *
16       * * * 1 * * * * * 1 1 * * *
17       2 * * * * * 0 * * * * * * *
18         * * * * * * * * * * * *
19           * * * * * * * * * *
```

* = good die

= number of defects at this site

0 = blank space

Figure 3.16 Failure Log Map - Silicon Aluminum

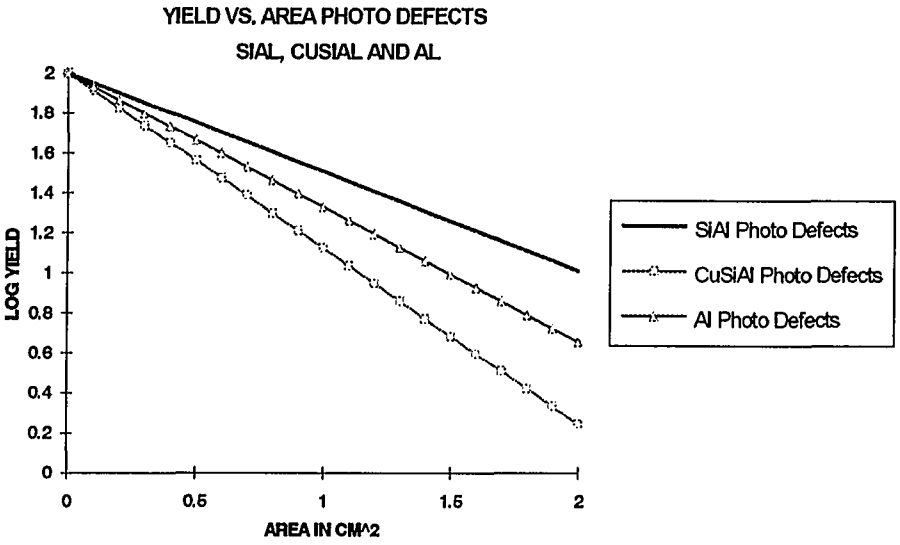

Figure 3.17 Yield vs. Area Photo Defects For All Metals

3.4 Defect Distributions

In 1970 I.F. Chang investigated the relationship between defect size distributions and yield [24] by evaluating distributions of the form e^{-X}, $1/X$, $1/X^2$, $1/X^3$ and $1/X^4$. This work determined that the type of defect size distribution a process exhibited had an impact on yields [24]. Several studies [24,25,26] have developed defect distributions of the form $1/X^n$ where n ranges from two to four.

Stapper has developed hypothetical distributions [26] of the form

$$D(x) = \overline{D} \cdot h(x)$$

$$h(x) = \frac{2(n-1)x}{(n+1)x_0^2} \text{ for } x<x_0$$

$$h(x) = \frac{2(n-1)x_0^2}{x^n} \text{ for } x>x_0$$

for n=3 these become

$$D(x) = \frac{x\overline{D}}{x_0^2} \text{ for } x<x_0$$

and

$$D(x) = \frac{x_0^2\overline{D}}{x^3} \text{ for } x>x_0$$

Stapper reports [27] the defect size distribution of $1/X^3$ has been used for yield predictions at IBM for more

than twenty years, although he is careful to note that the distributions are process dependent and will vary accordingly.

Defect size distributions are used to determine the average number of failures on a monitor for a given particle or defect size. For a $1/X^3$ distribution, as shown in Fig. 3.18, the defects peak at a value of X_0. Below X_0 the test structure cannot resolve the defects. Above X_0 the relative defect densities decrease, with increasing monitor yield. The test structures should be designed to resolve the minimum particle size to be monitored in the process.

Defects measured using a comb test structure will be cumulative defect data, unless the defects are visually binned according to size. A failure measured on a comb test structure X results because the defect is larger than or equal to the pitch at the measurement. Thus as pitch increases, defects - or fail sites - decrease as $1/X^2$. Mathematically, cumulative data for a $1/X^3$ distribution would be

$$\int X^{-3} dX \approx X^{-2}$$

$1/X^3$ DISTRIBUTION

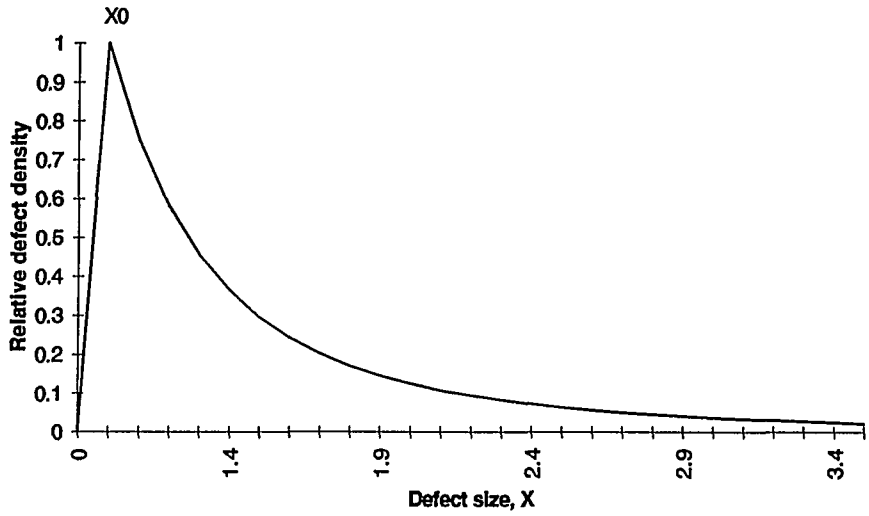

Figure 3.18 $1/X^3$ Distribution

After nonlinear regression on the defect count vs. defect size data using a p.c. version of Statgraphics, it was found that aluminum was an excellent fit to the curve:

$Y = 100/X^2$

where:

Y = number of defects

X = defect size

R = correlation coefficient = 0.998

Similar curve fitting for CuSiAl resulted in:

$Y = 84/X^2$

and

R = 0.945

These plots along with the plot for the SiAl defect distribution are shown on the following pages in Figs. 3.19, 3.20 and 3.21.

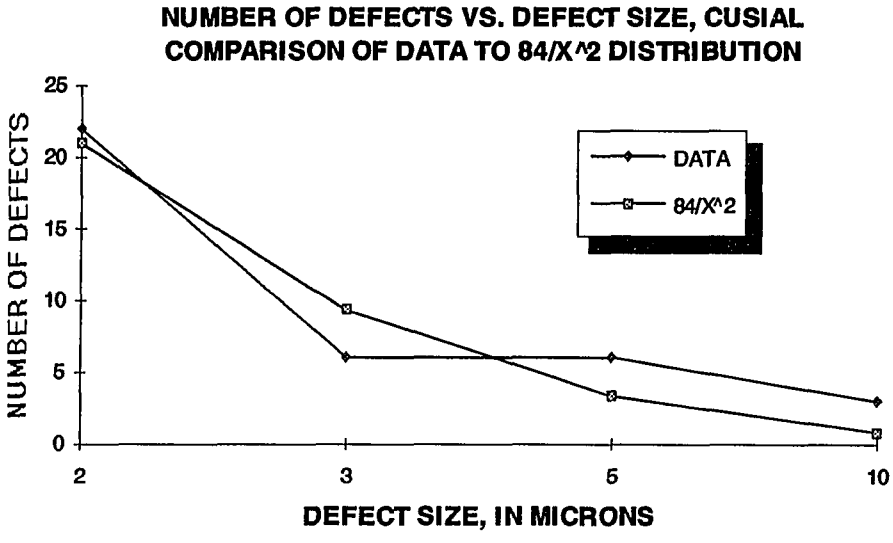

Figure 3.19 CuSiAl Defect Distribution

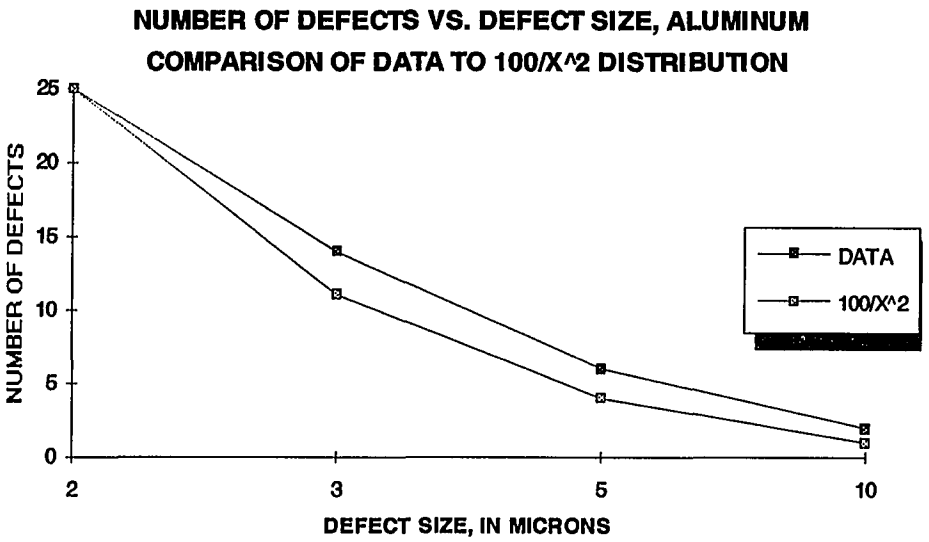

Figure 3.20 Aluminum Defect Distribution

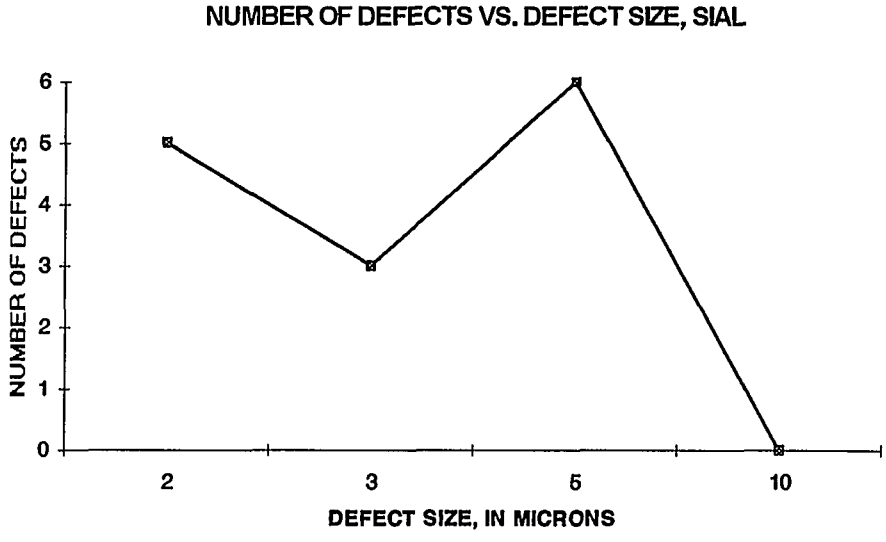

Figure 3.21 SiAl Defect Distribution

The defect distribution in Fig. 3.21 approaches that described by Parks and Burke [28]:

$$Y = C_1/X^3 + C_2/X$$

although the number of defects in Fig. 3.21 are too small to fit to a distribution, and appear to be below the "resolution" of the defect density plot. Perhaps if more defects existed in the data the plot would be more informative and fit the bimodal defect size model. The yields were simply too good for silicon aluminum. The etch process used was optimized for silicon aluminum and it obviously gave the best results.

It can be seen, however, that the data for copper silicon aluminum and the data for aluminum fall within the range of the distribution $1/X^n$ for n = 2 to 4.

CHAPTER 4

CONCLUSIONS

Yield model analysis for three different metal compositions was investigated. High yields with a large amount of defect clustering were found, and it was determined that the Stapper model best described this sample of wafers, due to the high degree of defect clustering. Etch defects were found to be the greatest yield problem, and resist blobs due to splattering were also found to be yield inhibiting. A major result of this paper is that it is imperative to consider clustering in detail when evaluating defects. Only through consideration of clustering in the yield model can the largest yielding metal process be chosen for larger VLSI size chips. Thus an evaluation of a VLSI process/metal system based only on defect density and a Poisson distribution would not result in the appropriate conclusion as to which system is best.

The results of this thesis show the usefulness of these yield models in industry to plan product yields and determine production costs as well as an aid to scheduling future product starts.

A yield model including multiple mask levels would be helpful. An additional project may be to perform a

similar experiment under more difficult circumstances, such as depositing the metal over steep first level metal and poly steps to look for step coverage and/or etch problems. Due to the excellent results of this experiment, the Drytek Quad plasma etcher used in this study would make a good tool for further particle contamination studies.

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