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**Simultaneous switching noise and its impact on CMOS digital systems**

**Nimmagadda, Srinivas, M.S.**

**The University of Arizona, 1992**

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Ann Arbor, MI 48106



**SIMULTANEOUS SWITCHING NOISE AND ITS  
IMPACT ON CMOS DIGITAL SYSTEMS**

by

Srinivas Nimmagadda

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A Thesis Submitted to the Faculty of the  
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING  
In Partial Fulfillment of the Requirements  
For the Degree of  
MASTER OF SCIENCE  
WITH A MAJOR IN ELECTRICAL ENGINEERING  
In the Graduate College  
THE UNIVERSITY OF ARIZONA

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## ABSTRACT

Simultaneous switching noise was calculated for a number of CMOS drivers switching together. CMOS receiver noise immunity and the feed through of simultaneous switching noise from a D.C. "ON" driver were studied. The effects of skewing output driver switching on the simultaneous switching noise were explained. The performance trade-offs in using a damping resistor to minimize switching noise were analyzed. A distributed lumped equivalent model has been developed to model signal propagation over noisy reference planes, and thereby to accurately predict the overall noise levels in a system. The impact of package pin distribution on noise on the reference plane was analyzed.

## CHAPTER 1

### Introduction

In high speed VLSI systems, many output drivers switch at the same time. The simultaneous switching of these output drivers causes the total current through the  $V_{dd}/V_{ss}$  chip-package connections to change in a short amount of time. This rate of change of current gives rise to power supply fluctuations due to the inductance of the  $V_{dd}/V_{ss}$  connections. The voltage dropped across the inductance of the  $V_{dd}/V_{ss}$  connections due to simultaneous switching of outputs is called the simultaneous switching noise or  $\Delta I$  noise or ground bounce [1], [2]. The simultaneous switching of output drivers is shown in Figure 1.1. Simultaneous switching noise for the worst case analysis is modeled in [3]. The maximum switching current through the ground path when  $n$  number of similar drivers are switching together is [3]

$$I_t = n \frac{k}{2} [V_{in} - V_t - V_n]^2, \quad (1.1)$$

where  $V_t$  and  $k$  are the threshold voltage and the transconductance parameter respectively of the NMOS transistor,  $V_{in}$  is the input voltage, and  $V_n$  is the switching noise produced. Ignoring the effect of  $R_{pkg}$  in Figure 1.1, switching noise can be calculated

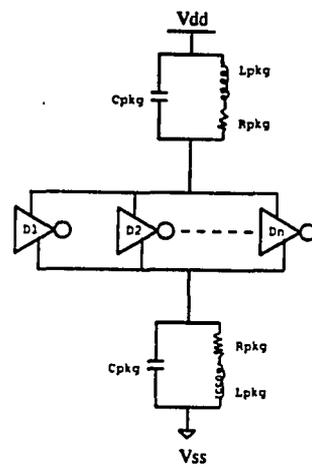


Figure 1.1: Simultaneous switching of output drivers

as [3]

$$V_n = L_{pkg} \frac{dI_t}{dt} \approx L_{pkg} \frac{I_t}{T}, \quad (1.2)$$

where  $T$  is the time taken for the switching current to travel from zero to its maximum value. From equations 1.1 and 1.2, switching noise as a function of number of simultaneously switching drivers can be described as [4],

$$V_n^2 - 2V_n[V_{in} - V_t + \frac{T}{nkL_{pkg}}] + [V_{in} - V_t]^2 = 0. \quad (1.3)$$

It can be seen from equation 1.3 that switching noise is not a linear function of the number of simultaneously switching outputs. This is because the switching current decreases when the ground bounce increases [4].

Simultaneous switching noise has several effects on the system performance. It increases driver delays because of the reduced  $V_{gs}$  of the driver transistors ( lesser driver current ). It feeds through quiet drivers and might cause false switching at their receivers. Switching noise might cause false switching of any internal devices that are connected to the noisy  $V_{dd}/V_{ss}$  chip-package connections.

Simultaneous switching noise appears at the  $V_{dd}/V_{ss}$  nodes of a receiver owing to the sharing of the  $V_{dd}/V_{ss}$  busses between the drivers and the receivers. Note that even if separate  $V_{dd}/V_{ss}$  busses are used for drivers and receivers on the chip, they might be connected through the same  $V_{dd}/V_{ss}$  plane connections in multi-layered packages. Hence decoupling the receiver circuit  $V_{dd}/V_{ss}$  connections from the driver circuit  $V_{dd}/V_{ss}$  connections is difficult. This could cause false switching of the receiver.

In a system, some drivers could be D.C. "ON" ( quiet ) and they might be connected to the noisy  $V_{dd}/V_{ss}$  connections. Switching noise feeds through these quiet drivers onto their outputs and might cause false switching at their receivers. In chapter 2, receiver noise immunity and the feed through of switching noise from a quiet driver are studied.

One method to control switching noise is by increasing the number of bond pad connections or package pins. This reduces the effective inductance of the  $V_{dd}/V_{ss}$  path, and thereby switching noise is reduced. However, if the system is bond pad or package pin limited, the designer might have to resort to other methods to control switching noise. In chapter 3, the effects of skewing and damping switching noise waveforms to reduce simultaneous switching noise are explained.

In chapter 4, a distributed lumped equivalent circuit model is developed for coupled lines over noisy ( time varying voltage ) reference planes to model the overall noise levels in a system. Results obtained using this model are compared with those obtained using the conventional "isolation" model. The impacts of package-pin distribution on noise on the reference plane are analyzed.

## CHAPTER 2

### Receiver Noise Immunity Studies

#### 2.1 Introduction

Simultaneous switching noise can cause false switching of a receiver. It appears at the  $V_{dd}/V_{ss}$  nodes of a receiver owing to the sharing of the  $V_{dd}/V_{ss}$  busses between the drivers and the receivers. Even if separate  $V_{dd}/V_{ss}$  busses ( for the receivers ) are used on chip, they may be connected through the same  $V_{dd}/V_{ss}$  plane connections in multi-layered packages. Typical receiver immunity characteristics to switching noise at the  $V_{dd}/V_{ss}$  nodes is shown in Figure 2.1 [5]. Switching noise also appears at the input of a receiver by feeding through a quiet driver ( D.C. "ON" ) onto the interconnect connecting the quiet driver and the receiver. This might cause false switching of the receiver. In this chapter, receiver immunity to switching noise at its input, and the feed through of switching noise from a D.C. "ON" driver are explained.

#### 2.2 Driver Selection Criteria

The final stage of a CMOS output driver ( an inverter ) was selected for this study. The driver device sizes (  $W_P/L_P$  and  $W_N/L_N$  ) were chosen using SPICE simulations

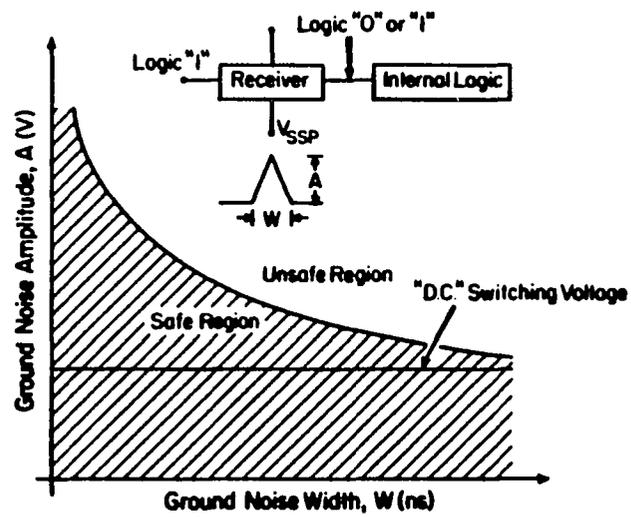


Figure 2.1: Typical receiver noise immunity characteristics to switching noise at the  $V_{dd}/V_{ss}$  nodes

to drive a 25 pF load with a 2 ns average delay time, given the ( default ) threshold voltages  $|V_{TP}| = V_{TN} = 0V$ .

Here,  $W_P$  and  $L_P$  are the width and length of the P-channel transistor,  $W_N$  and  $L_N$  are the width and length of the N-channel transistor respectively, and  $V_{TP}$  and  $V_{TN}$  are the threshold voltages of the P-channel and N-channel transistors respectively. The widths of the PMOS and NMOS transistors corresponding to channel lengths of  $5 \mu m$ ,  $2 \mu m$ ,  $1 \mu m$ ,  $0.5 \mu m$  and  $0.25 \mu m$  were selected to meet the above design criteria. The circuit simulated in SPICE is shown in Figure 2.2 and the results are summarized in Table 2.1. A piece-wise-linear waveform with rise and fall times of 1 ns was selected as the input transient. The delay was measured at 50% points of the voltage swing. (This is reasonable because the typical switching point for a CMOS inverter with  $V_{dd} = 5V$  is around 2.2 V - 2.8 V).

### 2.3 Simultaneous Switching Noise

Three packages were selected for this study, two pin grid array packages and a dual-in-line package. The lumped equivalent circuit that represents the package parasitics ( package pin +  $V_{dd}/V_{ss}$  plane + bond connection ) associated with each  $V_{dd}/V_{ss}$  connection is shown in Figure 2.3 and the lumped package parasitic parameter values used in this study are shown in Table 2.2 [6]. The lumped equivalent circuit that represents the output signal path connections is shown in Figure 2.4 and the lumped parameters used in this study are given in Table 2.3 [6].

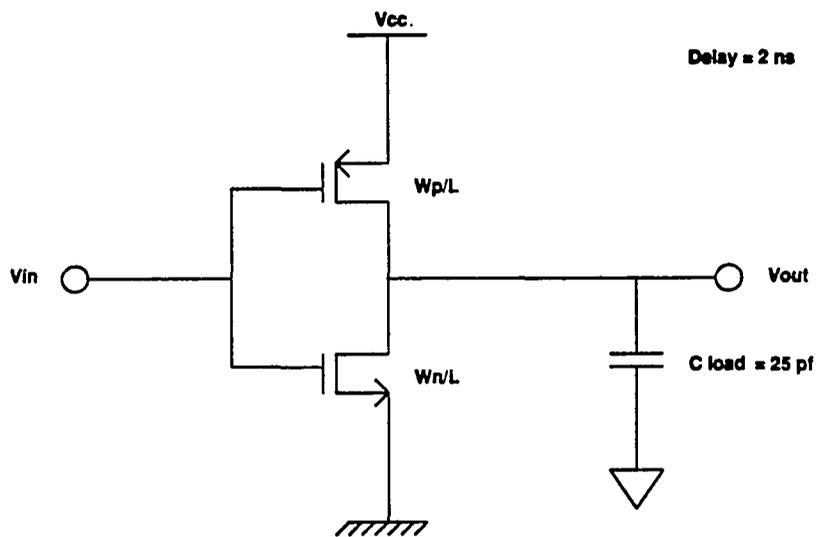


Figure 2.2: Final stage of a CMOS output driver

L	$W_p$	$W_n$	$C_{load}$	$\langle t_{PLH} + t_{PHL} \rangle / 2$
5 $\mu m$	750 $\mu m$	441 $\mu m$	25 pF	2 ns
2 $\mu m$	303 $\mu m$	196 $\mu m$	25 pF	2 ns
1 $\mu m$	150 $\mu m$	100 $\mu m$	25 pF	2 ns
0.5 $\mu m$	75 $\mu m$	50 $\mu m$	25 pF	2 ns
0.25 $\mu m$	38 $\mu m$	30 $\mu m$	25 pF	2 ns

Table 2.1: Driver Sizes

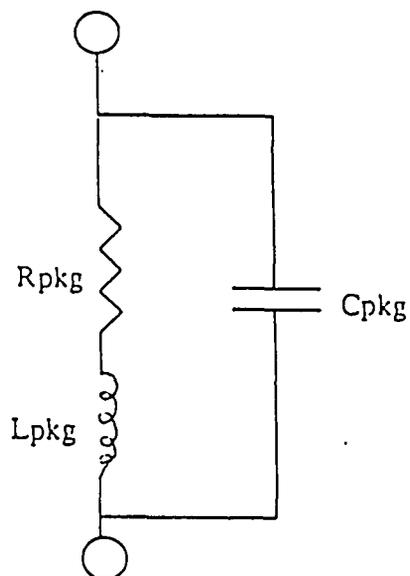


Figure 2.3: Lumped equivalent model for the package/plane parasitics

Package	$L_{pkg}$	$C_{pkg}$	$R_{pkg}$
PGA1	5 nH	5 pF	2m $\Omega$
PGA2	2 nH	2 pF	2m $\Omega$
DIP	7 nH	5 pF	4m $\Omega$

Table 2.2: Package parasitics

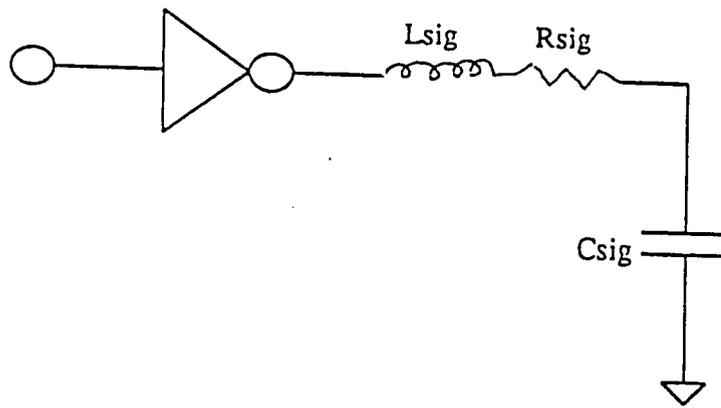


Figure 2.4: Lumped equivalent model for the output signal path connections

Package	$L_{sig}$	$C_{sig}$	$R_{sig}$
PGA1	5 nH	5 pF	2m $\Omega$
PGA2	2 nH	2 pF	2m $\Omega$
DIP	7 nH	5 pF	4m $\Omega$

Table 2.3: Output signal path parasitics

Simultaneous switching noise was evaluated using SPICE for 2, 4, 8, 16 and 32 drivers switching simultaneously. As expected, the maximum amplitude of the switching noise has a non-linear behavior with respect to the number of simultaneously switching drivers. It was found that switching noise exhibits an underdamped oscillatory behavior in time [5]. This is because the lumped parasitic model is an R,L,C circuit satisfying the underdamped condition,

$$R^2 - 4\frac{L}{C} < 0. \quad (2.1)$$

The switching current obeys the following equation.

$$L\frac{d^2I(t)}{dt^2} + R\frac{dI(t)}{dt} + \frac{I(t)}{C} = 0, \quad (2.2)$$

where  $I(t)$  is the switching current through the driver. The non-linear behavior of the switching noise with respect to the number of drivers is due to the negative feedback effect [4]. Figure 2.5 shows the magnitude of switching noise generated as a function of the number of simultaneously switching drivers [5].

#### 2.4 Switching noise feed through from a D.C. “ON” ( quiet ) driver

The simultaneous switching of output drivers causes the the  $V_{dd}/V_{ss}$  busses to be noisy. In a system, some drivers could be D.C. “ON” ( not switching ) and they might be connected to the noisy  $V_{dd}/V_{ss}$  busses. The feed through of switching noise from such quiet drivers ( either P-channel or N-channel device acts like a resistor ) are studied in this section. The circuit illustrating the ground noise feed through from

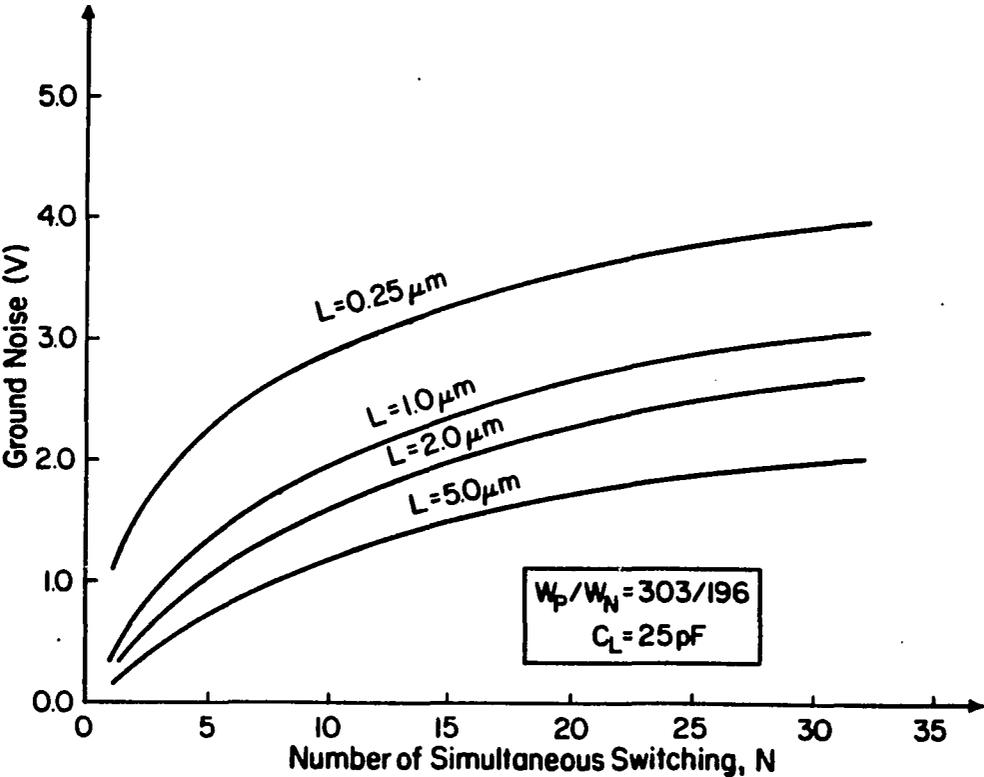


Figure 2.5: Switching noise vs Number of simultaneously switching outputs

a D.C. "ON" driver is shown in Figure 2.6. Here, the N-channel device of the quiet driver is in the linear region and acts like a resistor. Figure 2.7 illustrates the effects of switching noise feeding through such a quiet driver. In obtaining Figure 2.7, the quiet driver was connected to a TTL compatible receiver ( an inverter ) with input switching point at 1.4 V. The receiver input was at logic "0" and its output was at logic "1" if no noise pulse exists. A triangular pulse was applied at the source end of the quiet driver NMOS transistor ( the input of the quiet driver is connected to 5V DC ). SPICE simulations were performed on the network and the amplitude and width of the pulse were increased till the output of the receiver changed from logic "1" to logic "0". This was done for different driver sizes with results as shown in Figure 2.7. Switching noise with smaller pulse widths requires larger amplitudes to switch the receiver compared to noise with larger pulse widths. The exact point at which this switching takes place varies for different technologies. This is because of the dependency of this point on the parasitics associated with the device. For example, a driver with  $5\mu m$  channel length has a larger resistance than a driver with  $2\mu m$  channel length and hence lesser noise feeds through the  $5\mu m$  driver compared to the  $2\mu m$  driver, if all other parameters are constant. The curves shown in Figure 2.7 for different channel lengths take into account driver parameter trends.

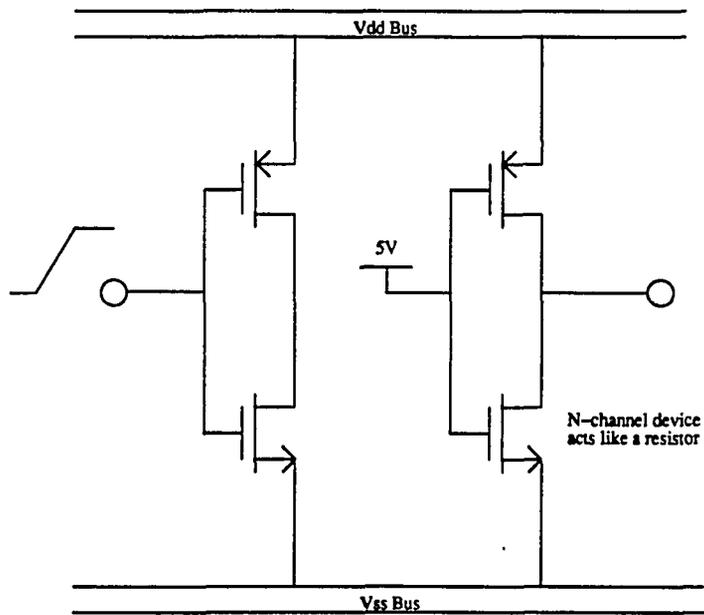


Figure 2.6: Switching Noise feed through from a D.C. "ON" Driver

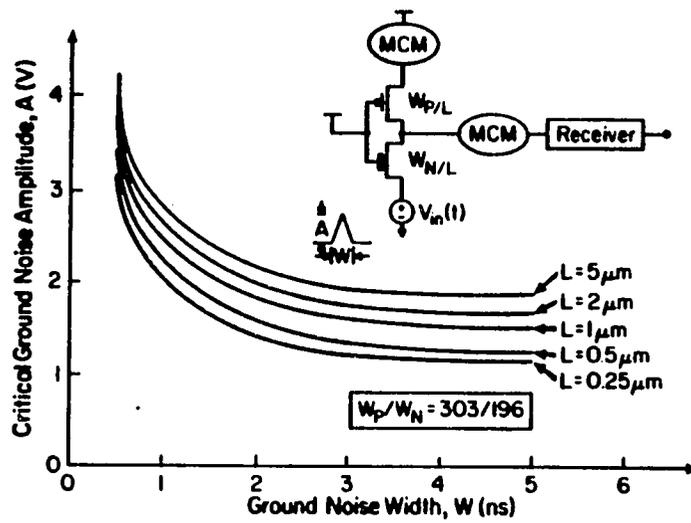


Figure 2.7: Effects of switching noise feed through from a D.C. "ON" driver, TTL output logic voltage level

Type	$L$ ( $\mu m$ )	$W_P$ ( $\mu m$ )	$W_N$ ( $\mu m$ )
TTL compatible	5,2,1,0.5,0.25	20	12
TTL compatible	5,2,1,0.5,0.25	40	25
CMOS compatible	5,2,1,0.5,0.25	10	35
CMOS compatible	5,2,1,0.5,0.25	20	60

Table 2.4: Receiver Device Sizes

## 2.5 Receiver Noise Immunity Characterization

The noise immunity of a typical receiver circuit such as is shown in Figure 2.8 was evaluated. Using SPICE simulation, the amplitude and width of the input pulse were varied till the receiver output changed from logic "1" level to logic "0" level. Figure 2.9 shows TTL level compatible CMOS receiver noise immunity characteristics. The receiver was presumed to be connected to internal logic. A CMOS inverter ( switching point at 2.5 V ) was used as a representative of the internal logic. The receiver device sizes used are shown in Table 2.4. Typical lumped package parasitics (  $R = 1m\Omega$ ,  $L = 5nH$  and  $C = 1pF$  ) were used for the SPICE simulations. Note that the critical noise amplitude and width on the curve is the point at which the receiver triggers the internal logic. The region above the curve will lead to false switching, while below the curve it is safe. The noise immunity depends both on the pulse width and the pulse amplitude. Noise with smaller pulse width ( higher frequency signal ) requires larger amplitude to switch the receiver compared to noise with larger pulse width. This is because of the gain-bandwidth limitations of the receiver circuit. Note that the values of the threshold voltages of the N-channel and P-channel transistors

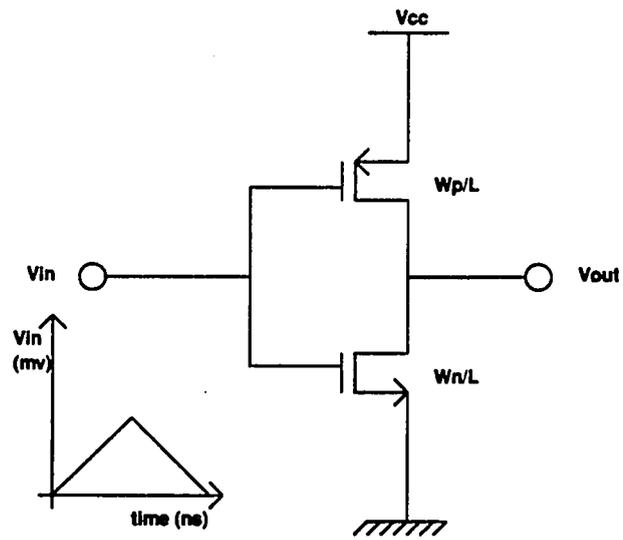


Figure 2.8: Typical CMOS receiver circuit

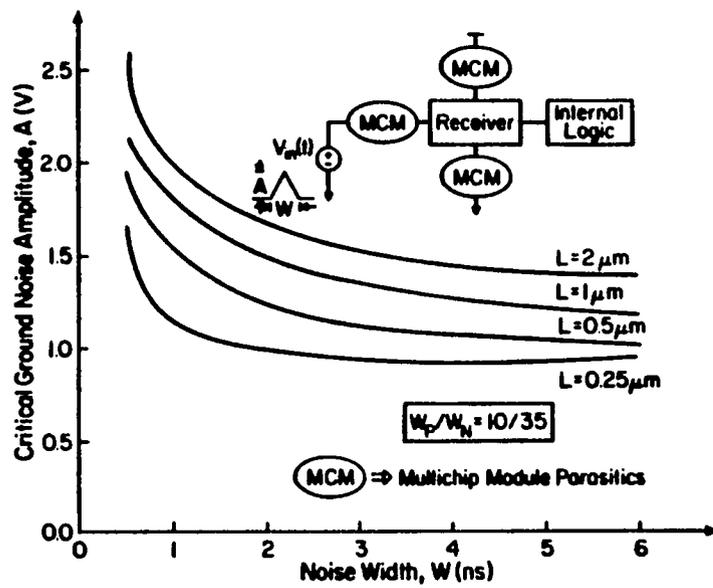


Figure 2.9: Receiver immunity to switching noise at the input

used in this study were  $V_{TN} = |V_{TP}| = 0V$ . The curves in Figure 2.9 shift upwards with non-zero threshold voltages. This is because the receiver becomes more immune to noise with increase in threshold voltage.

## **CHAPTER 3**

### **Effects of Skewing/Damping on Simultaneous Switching Noise**

#### **3.1 Introduction**

Simultaneous switching noise can be reduced by increasing the number of bond connections or package pins connected to power and ground [5]. This reduces the effective inductance of the power/ground path, and thereby switching noise is reduced. However, if the system is bond pad or package pin limited, the designer might not have the freedom of increasing the number of bond connections or package pins. In this chapter, methods of minimizing switching noise by skewing ( delaying the switching of some of the outputs ) and damping ( using a damping resistor at the source ends of the driver transistors ) are studied and the trade-offs involved are explained.

#### **3.2 Effects of Skewing Output Driver Switching on the Simultaneous Switching Noise**

Simultaneous switching noise can be reduced by delaying the switching of some of the outputs ( skewing ). When the outputs are skewed, the current through the

“early” switching drivers does not totally overlap the current through the “late” switching drivers. This reduces switching noise compared to the case where all the drivers are switching at the same time. Figure 3.1 illustrates the concept of skewing. In Figure 3.2, ground noise due to the switching of 12 drivers with the switching time of the last four simultaneously switching drivers skewed relative to the switching time of the first eight simultaneously switching drivers is shown. It can be seen that the total ground noise in this case is smaller compared to the case where all the 12 drivers are switching together. If the switching noise is a periodic wave form, one would get minima in the magnitude of the switching noise when the skew time is  $T$ ,  $3T$ ,  $5T$ ,  $\dots$ , where  $T$  is the time taken for the switching current to travel from zero to its maximum value.

However, because of the resistive component present in the package parasitics, the switching current exhibits a damped quasi-periodic behavior ( amplitude and period decrease with time ) [5]. The switching current  $I(t)$  obeys the following differential equation:

$$L \frac{d^2 I(t)}{dt^2} + R \frac{dI(t)}{dt} + \frac{I(t)}{C} = 0, \quad (3.1)$$

where  $R$ ,  $L$  and  $C$  are the lumped package parasitics. For most package parasitics,

$$R^2 - 4 \frac{L}{C} < 0. \quad (3.2)$$

Hence the switching current exhibits an underdamped oscillatory behavior. This underdamped waveform damps out with a damping coefficient of  $R \exp \frac{-Rt}{2L}$ . The

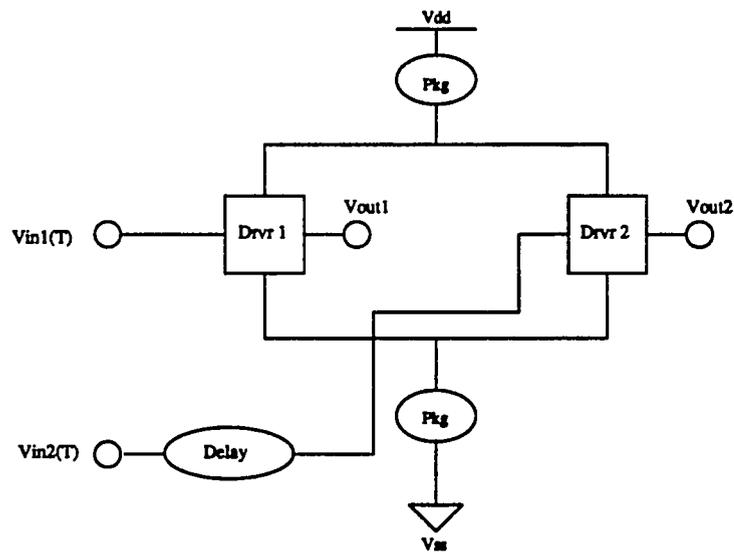


Figure 3.1: Skewing the switching of outputs

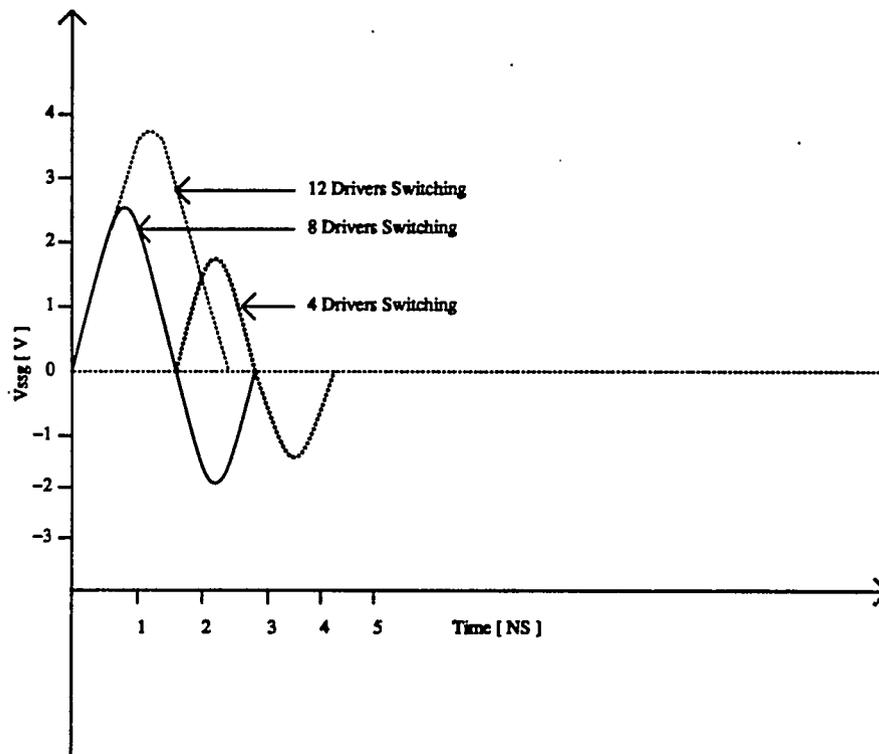


Figure 3.2: Effect of skewing the switching of outputs on the total ground noise

period of this waveform decreases with time. The quasi-period for an impulse response is

$$T_d' = 2\pi \sqrt{\frac{LC}{1 - \frac{R^2C}{4L}}}, \quad (3.3)$$

where the quasi-period is defined as the first ( maximum ) period of the underdamped current waveform [5]. Since switching noise is a derivative of the switching current, the corresponding quasi-period for damped switching noise ( $T_d$ ) is

$$T_d = T_d' / 2. \quad (3.4)$$

When the outputs are skewed, since switching noise is a quasi-periodic waveform, there will a global minimum followed by several local minima. This is because the magnitude of an underdamped waveform decreases with time. To minimize switching noise by skewing, it is necessary to accurately calculate the appropriate skew time ( $\Delta T_s$ ) considering the underdamped characteristics of switching noise. For quasi-periodic underdamped oscillations described previously, the global minimum occurs at  $\Delta T_s$ , where

$$\Delta T_s = \frac{1}{2} \left[ T + \frac{T_d'}{2} \right]. \quad (3.5)$$

To demonstrate the effects of skewing, several driver configurations were simulated in SPICE. Figure 3.3 shows the case of eight similar outputs ( with the device parameters given in the Figure ) switching. In this example, four outputs switch simultaneously at  $T_0$  and the other four outputs switch simultaneously at  $T_0 + \Delta T$ . Using the equations given above and with lumped package parasitics  $R = 1 \text{ m}\Omega$ ,  $L = 5 \text{ nH}$  and

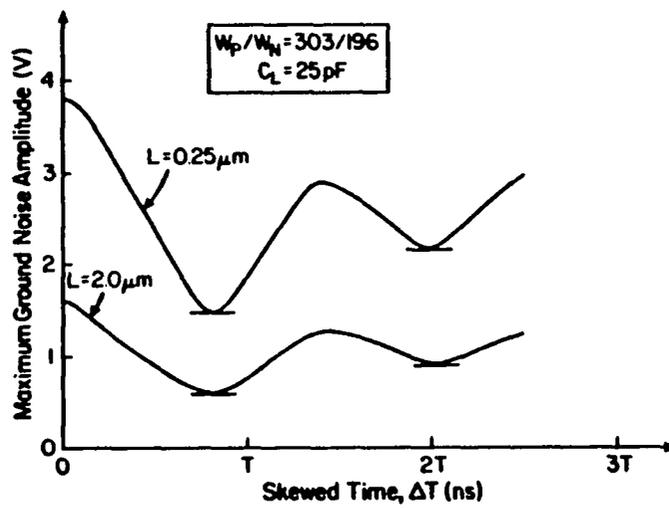


Figure 3.3: Effects of skewing in minimizing switching noise

$C = 1 \text{ pF}$ , the optimal skew time can be calculated as  $\Delta T_s = 0.78 T$ . In Figure 3.3, switching noise is plotted as a function of  $\Delta T_s$ . Note that in Figure 3.3 the value of  $T$  for  $2.0 \text{ }\mu\text{m}$  and  $0.25 \text{ }\mu\text{m}$  channel lengths is different. Results from SPICE simulations agree quite well with the results from the use of quasi-periodic waveform technique. For commonly used packages and typical drive strengths,  $\Delta T_s$  is in the order of 1 - 2 ns. When the output switching speed increases,  $T$  decreases and thereby  $\Delta T_s$  decreases.

### **3.3 Effects of Damping the Output Driver Waveform on Simultaneous Switching Noise**

If the system design does not permit skewing the switching of the outputs, damping resistors can be used at the source ends of the driver transistors to minimize switching noise. These damping resistors can be used to control switching noise without any trade-off in speed [5]. However, the driver sizes need to be increased in order to achieve the desired speed. Also, the damping resistors occupy some area on the chip. These damping resistors ( usually in  $10 - 100\Omega$  range ) can be realized either in silicon as diffusion resistors or in polysilicon as poly interconnect resistors. Without damping resistors, switching noise can be minimized by decreasing the device sizes. However, this increases driver delays. To illustrate the advantage in using a damping resistor, a CMOS driver was simulated in SPICE with and without damping resistors with different device sizes. In this example, the channel length of the devices was

held constant at  $1.0\mu m$  and  $W_p$  and  $W_n$  are varied keeping  $W_p/W_n = 1.54$ . The results obtained from SPICE simulations are shown in Figure 3.4. It is clear from Figure 3.4 that without a damping resistor, the speed vs switching noise trade-off is limited by the upper curve. Use of additional damping resistors minimizes switching noise without decreasing the speed. However, the device sizes have to be increased to achieve the desired speed.

The effect of using damping resistors in minimizing switching noise is illustrated in Figure 3.5 [5]. In obtaining Figure 3.5, two simultaneously switching drivers were simulated in SPICE. The driver sizes ( $W_p = 303\mu m$ ,  $W_n = 196\mu m$  and  $L = 1.0\mu m$ ) were selected to drive  $C_{Load} = 25$  pF with an average delay  $[\frac{(t_{PLH}+t_{PHL})}{2}]$  of 2 ns. It can be seen from Figure 3.5 that switching noise is reduced by 40% when a  $50\Omega$  resistor is used, and by 75% when a  $100\Omega$  resistor is used. Even with  $100\Omega$  damping resistor, to drive the same load ( $C_{Load} = 25$  pF) in 2 ns average delay time, the driver sizes only need to be increased to  $W_p = 345\mu m$  and  $W_n = 224\mu m$ .

Switching noise is plotted as a function of the number of outputs switching simultaneously for different values of damping resistor in Figure 3.6. Considerable reduction in switching noise is obtained when larger resistors are used [5]. However, there is a trade-off in delay and driver device sizes need to be increased accordingly to achieve the desired speed. One has to consider the maximum allowable switching noise, driver speed and area of the resistor while deciding on the value of damping resistor.

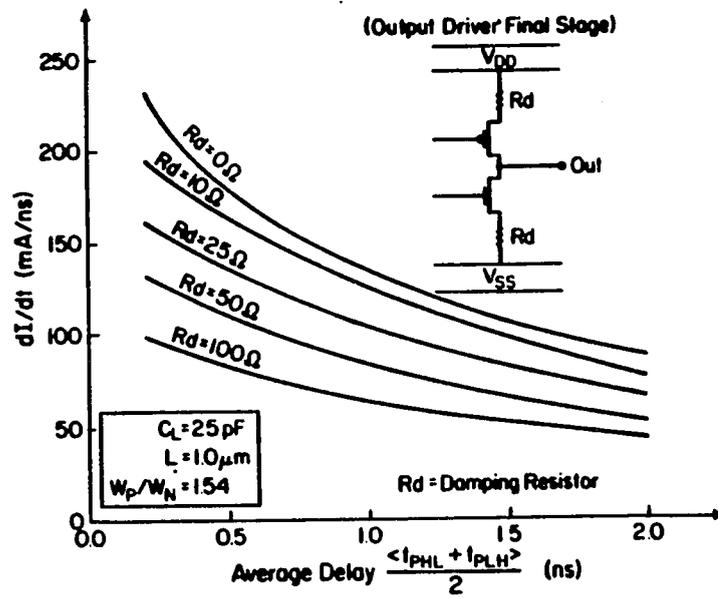


Figure 3.4: Performance vs Switching noise limitations on output drivers

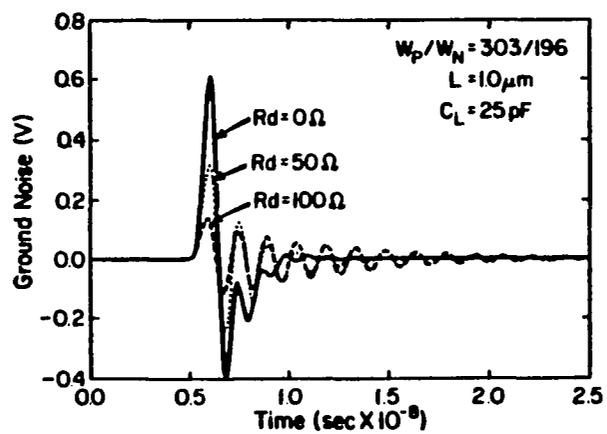


Figure 3.5: Underdamped oscillatory ground noise behavior

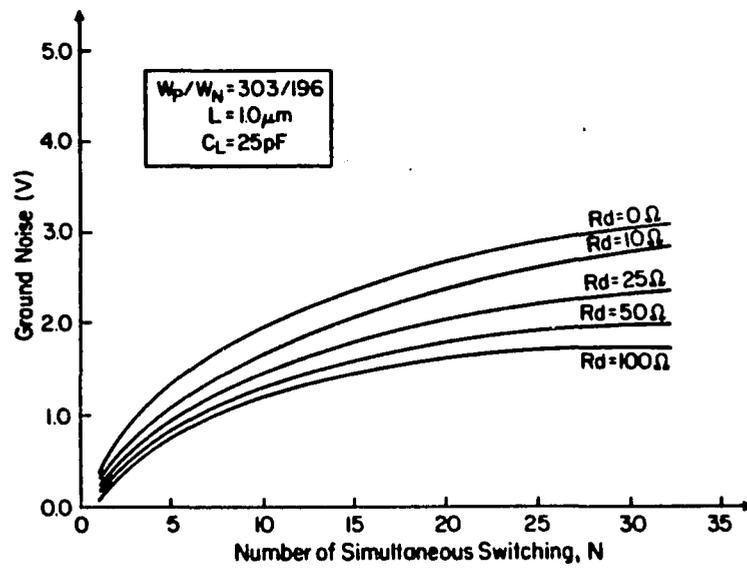


Figure 3.6: Effects of damping resistor on the switching noise

## CHAPTER 4

# Modeling and Simulation of Coupled Lines over Noisy Reference Planes

### 4.1 Introduction

Often, in practice, simultaneous switching noise and coupled noise are calculated in isolation and added together to obtain the overall noise levels in a digital system [1]. However, this method might not predict the noise levels accurately because of the interactions between switching noise and coupled noise [7]. For example, in a multi-layered package, output driver  $V_{dd}/V_{ss}$  terminals are connected to  $V_{dd}/V_{ss}$  planes and, because of simultaneous switching of output drivers, these planes are at a time varying voltage. This disturbs signal propagation over these noisy  $V_{dd}/V_{ss}$  planes. So, it is essential to model the overall noise level with the actual driver/receiver circuits and using a detailed chip-package interface model. Conventional transmission line simulators cannot be used to model signal propagation over noisy reference planes [7]. This is because these simulators require the ground plane to be at a constant voltage. A distributed lumped equivalent model has been developed to simulate coupled lines over noisy reference planes in SPICE. The results obtained using this model were

compared with those obtained using the conventional “isolation” ( switching noise isolated ) model. Effects of package pin distribution on noise on the reference plane were analyzed for various package pin placements.

#### **4.2 “Isolation” and “Plane Connected” Models**

The conventional “isolation” ( IS ) model ( switching noise is isolated from the signal transmission through the interconnects ) that is used for modeling the overall noise levels in a system is shown in Figure 4.1. However, this model does not account for the effects of a noisy ground plane on signal propagation. In the model shown in Figure 4.2, output driver  $V_{ss}$  terminals are connected to the ground plane. When these drivers switch simultaneously, switching noise is created on the ground plane and, thereby the signal propagation through the interconnects is affected. So, one can accurately predict the overall noise levels in a system using this model. This model is referred as “plane connected” ( PC ) model in this study.

#### **4.3 Distributed Lumped Equivalent Model Development**

Conventional TEM-mode transmission line simulators, such as UANTL [8], calculate transient response for coupled lines using a set of coupled transmission line equations. In deriving these equations, it is assumed that the reference plane is at a constant voltage. Because of this limitation, these simulators cannot be used to model coupled lines over noisy reference planes. A distributed lumped equivalent

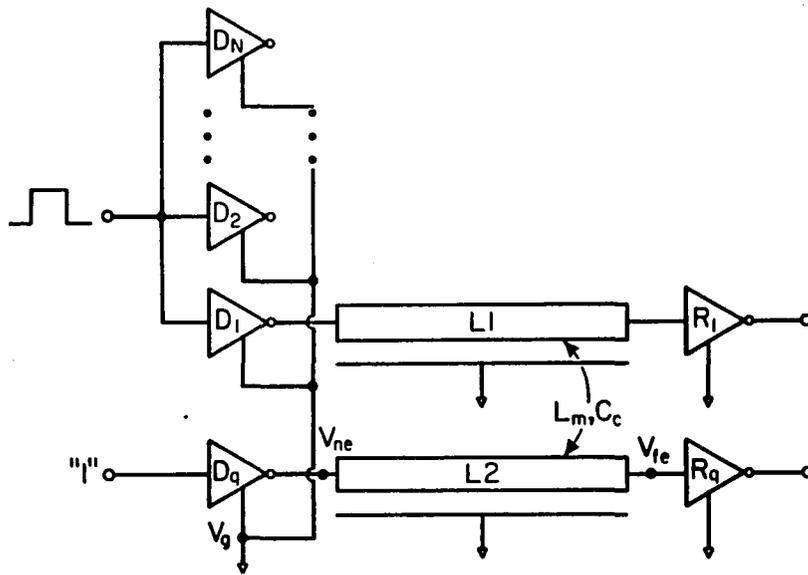


Figure 4.1: "Isolation" model

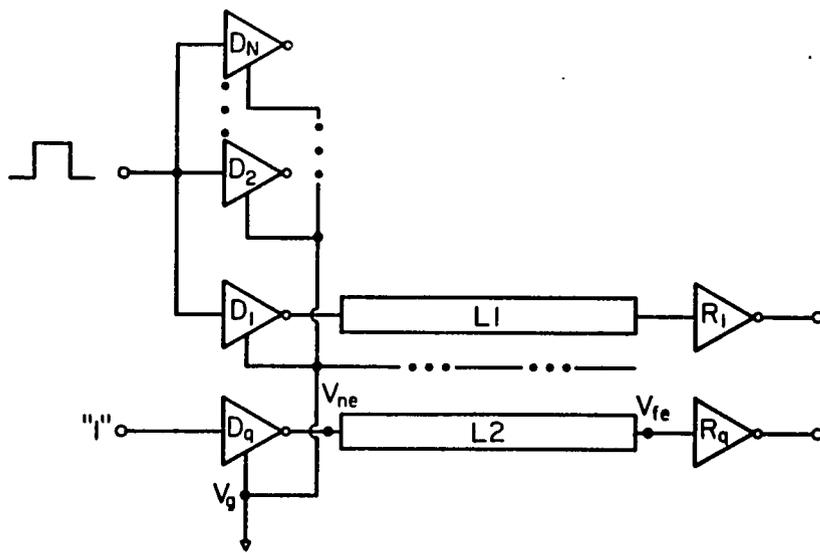


Figure 4.2: "Plane Connected" model

model has been developed to simulate coupled lines over noisy reference planes using SPICE. Because of the symmetry between  $V_{dd}$  and  $V_{ss}$  planes, only the analysis for interconnects over  $V_{ss}$  planes is shown here. It is essential to include both the  $V_{ss}$  plane parasitics, and coupling parasitics to signal interconnects in the model because of the noisy  $V_{ss}$  plane. To calculate these self and coupling parasitics between conductors and the conductor- $V_{ss}$  plane, the plane was modeled as a very wide conductor as shown in Figure 4.3. For a single line over a noisy reference conductor, the following equations can be written in the sinusoidal steady state [7];

$$\frac{dV_{12}}{dZ} = -j\omega(L_1^p + L_g^p - 2L_{1g}^p)I_1 = -j\omega L_{11}I_1, \quad (4.1)$$

$$\frac{dI_1}{dZ} = -j\omega C_{11}V_{12}. \quad (4.2)$$

Here,  $L_1^p$  is the partial self inductance of the signal conductor,  $L_g^p$  is the partial self inductance of the noisy ground conductor,  $L_{1g}^p$  is the partial mutual inductance between the signal conductor and the ground conductor,  $L_{11}$  is the equivalent lumped inductance, and  $C_{11}$  is the self capacitance of the signal conductor.  $L_{11}$  is calculated using UA2DL [9]. The partial self inductances are calculated using A.E. Ruehli's equations ( given in the Appendix ) [10]. The partial mutual inductance can then be obtained from equation 4.1. This methodology can be extended to coupled lines. From equation 4.1, the following equations can be written for the coupled interconnect structure shown in Figure 4.3 [7];

$$L_{11} = L_1^p + L_g^p - 2L_{1g}^p, \quad (4.3)$$

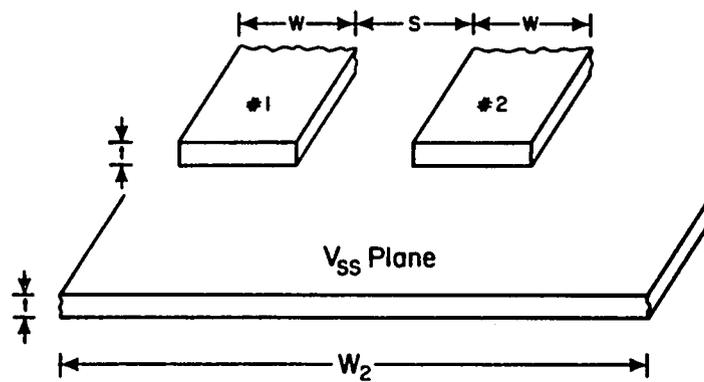


Figure 4.3: Coupled lines over a reference plane treated as a wide conductor

$$L_{22} = L_2^p + L_g^p - 2L_{2g}^p. \quad (4.4)$$

Here,  $L_{11}$ ,  $L_1^p$ , and  $L_{1g}^p$  are as defined earlier with respect to conductor 1, and  $L_{22}$ ,  $L_2^p$ ,  $L_{2g}^p$  are the corresponding parameters for conductor 2.  $L_{1g}^p$  and  $L_{2g}^p$  are obtained from equations 4.3 and 4.4. To calculate the partial mutual inductance ( $L_{12}^p$ ) between the signal conductors, the structure shown in Figure 4.4 is simulated using UA2DL. Here, the second conductor is treated as a ground conductor. From equation 4.1,

$$L_{11}' = L_1^p + L_2^p - 2L_{12}^p. \quad (4.5)$$

Here,  $L_{11}'$  is the total inductance calculated using UA2DL,  $L_1^p$  and  $L_2^p$  are the partial self inductances of conductors 1 and 2 (calculated from A.E. Ruehli's equations) respectively.  $L_{12}^p$  is calculated from equation 4.5. The appropriate connection for  $L_{12}^p$  in the equivalent circuit is shown in Figure 4.5. To calculate the capacitance matrix, UAC [11] is used treating the noisy ground conductor as a perfect ground conductor. The following capacitance matrix was calculated;

$$\begin{bmatrix} C_{ij} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \text{ pF/cm.}$$

Here,  $C_{11} = C_{1g} + C_{12}$  and  $C_{22} = C_{2g} + C_{21}$ , where  $C_{1g}$  and  $C_{2g}$  are the self (two-terminal) capacitances of conductors 1 and 2 respectively. The distributed lumped equivalent model shown in Figure 4.5 was set up for SPICE simulations. The self and coupling inductances and capacitances were calculated for various dimensions

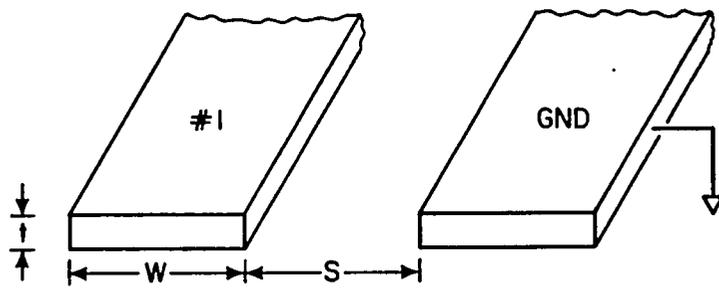


Figure 4.4: Coupled lines treating one conductor as ground conductor

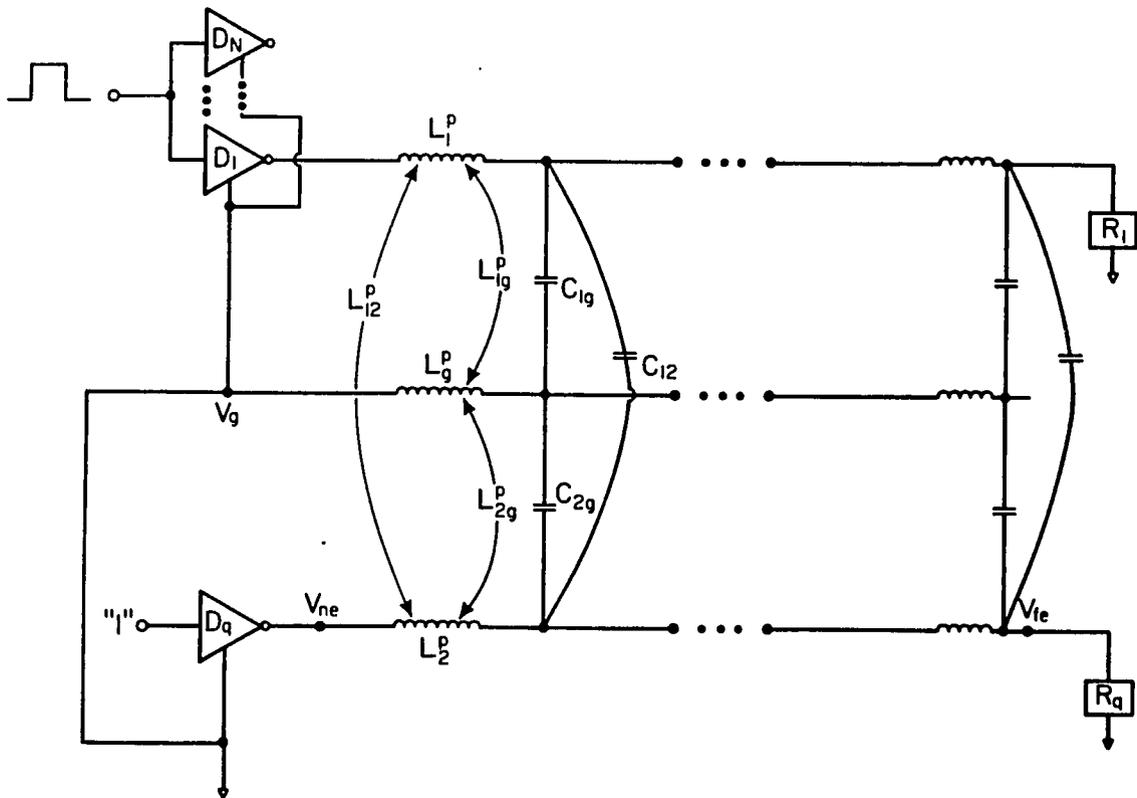


Figure 4.5: Distributed lumped equivalent model for coupled lines over noisy reference planes

Type	S	$W_{sig}$	$W_{gnd}$	T	$\epsilon_r$
Thin film	5, 10, 20, 30 ( $\mu m$ )	5 $\mu m$	600 $\mu m$	2 $\mu m$	3.9
Thick film	3, 6, 9, 15 (mils)	3 mils	100 mils	1 mil	3.9

Table 4.1: Interconnect geometries

of the interconnects shown in Table 4.1. In Table 4.1,  $S$  is the spacing between conductors,  $W_{sig}$  is the width of the signal conductor,  $W_{gnd}$  is the width of the ground conductor,  $T$  is the thickness of the signal and ground conductors and  $\epsilon_r$  is the dielectric constant of the medium.

As an example, the calculation of circuit element values for the thin film case with two conductors and  $S = 5 \mu m$  is shown here. Parameter values for all the other cases are given in Tables 4.2 and 4.3.

The following capacitance matrix was computed using UAC;

$$\begin{bmatrix} C_{ij} \end{bmatrix} = \begin{bmatrix} 0.648 & 0.180 \\ 0.180 & 0.647 \end{bmatrix} pF/cm,$$

For the same structure, the inductance matrix was calculated using UA2DL at  $f = 1$  GHz;

$$\begin{bmatrix} L_{ij} \end{bmatrix} = \begin{bmatrix} 5.697 & 2.071 \\ 2.071 & 5.696 \end{bmatrix} nH/cm.$$

Partial self inductances for signal and ground conductors were calculated using A.E. Ruehli's equation. Since this equation requires a finite length, 10 cm long conductors were used and the results were converted back to per-unit-length values.

Lumped Elements	S = 3 mils	S = 6 mils	S = 9 mils	S = 15 mils
$C_{1g} = C_{2g}$ (pF/cm)	0.359	0.394	0.419	0.449
$C_{12} = C_{21}$ (pF/cm)	0.209	0.121	0.079	0.038
$L_1^p = L_2^p$ (nH/cm)	16.070	16.070	16.070	16.070
$L_g^p$ (nH/cm)	9.577	9.577	9.577	9.577
$L_{1g}^p = L_{2g}^p$ (nH/cm)	9.776	9.755	9.669	9.519
$L_{12}^p$ (nH/cm)	12.648	11.755	11.155	10.321

Table 4.2: Thick film interconnect lumped element values

The following partial inductances were obtained;

$$L_1^p = L_2^p = 21.62 \text{ nH/cm}, \text{ and } L_g^p = 12.5 \text{ nH/cm}.$$

Using equation 4.3 and  $L_{11} = 5.697 \text{ nH/cm}$ , the partial inductance value between signal conductor and the ground conductor is  $L_{1g}^p = 14.212 \text{ nH/cm}$ . Because of symmetrical signal conductors,  $L_{2g}^p = 14.212 \text{ nH/cm}$ .

To calculate  $L_{12}^p$ , the structure shown in Figure 4.4 was simulated using UA2DL at  $f = 1 \text{ GHz}$ . The loop inductance was calculated to be  $L_{11}' = 7.574 \text{ nH/cm}$ . Using equation 4.5,  $L_{12}^p = 17.835 \text{ nH/cm}$ . The self capacitances were calculated from the capacitance matrix shown on the previous page. Thus,  $C_{1g} = C_{11} - C_{12} = 0.468 \text{ pF/cm}$ . Because of symmetry,  $C_{2g} = 0.468 \text{ pF/cm}$ . The mutual capacitance is  $C_{12} = 0.18 \text{ pF/cm}$ . Using the above methodology, parameters were calculated for all the other cases and the results are summarized in Tables 4.2 and 4.3.

Lumped Elements	$S = 5 \mu m$	$S = 10 \mu m$	$S = 20 \mu m$	$S = 30 \mu m$
$C_{1g} = C_{2g}$ (pF/cm)	0.472	0.519	0.564	0.579
$C_{12} = C_{21}$ (pF/cm)	0.178	0.089	0.029	0.013
$L_1^p = L_2^p$ (nH/cm)	21.620	21.620	21.620	21.620
$L_g^p$ (nH/cm)	12.501	12.501	12.501	12.501
$L_{1g}^p = L_{2g}^p$ (nH/cm)	14.212	14.247	14.312	14.315
$L_{12}^p$ (nH/cm)	9.776	9.755	9.669	9.518

Table 4.3: Thin film interconnect lumped element values

#### 4.4 Simulation Results

In all the simulations, input transients to the output drivers ( $D_1, D_2 \dots D_N$ ) shown in Figure 4.2 were low-to-high, and the output transients were high-to-low. Hence, the primary switching noise pulse is positive ( driver outputs are switching from high to low leading to ground bounce ) and the near-end noise is negative ( since the signal on the active line is making a high-to-low transition and since inductive and capacitive crosstalk add at the near end ). For all the interconnect geometries considered, far-end noise is positive. In the “plane connected” model, in addition to coupling from the active line ( crosstalk ) and the D.C. “ON” driver ( switching noise ) as in the “isolation” model, there is additional coupling from the noisy ground plane onto the quiet line. In Figures 4.6 and 4.7, switching noise ( $V_g$ ), measured at the source end of the output driver N-channel transistor, is plotted as a function of interconnect spacing for different numbers of simultaneously switching outputs, for thin and thick film interconnect technologies respectively. When the number ( $N$ ) of outputs switching simultaneously is equal to 16, the switching noise ( $V_g$ ) generated

is larger compared to near-end noise (  $V_{ne}$  ), and  $V_g$  is not affected by  $V_{ne}$ . Both the models generate the same amount of switching noise. However, for  $N \leq 4$ ,  $V_g$  is perturbed by  $V_{ne}$ . This perturbation is more for the case of  $N = 1$  because the magnitude of switching noise generated is lesser in this case compared to the other cases. Between the ( IS ) and ( PC ) models, the effect of  $V_{ne}$  on  $V_g$  is more for the ( PC ) model. This is due to the additional coupling from the noisy ground conductor in the ( PC ) model. As evident from Figures 4.6 and 4.7, for the  $N=1$  (PC) case,  $V_g$  is negative in magnitude ( note that the primary switching noise pulse is positive ).

In Figures 4.8 and 4.9, near-end noise (  $V_{ne}$  ) is plotted as a function of interconnect spacing and for different numbers of simultaneously switching outputs, for thin and thick film technologies respectively. As the number of simultaneously switching outputs increase,  $V_g$  increases and dominates the overall near-end noise. When  $N \geq 4$ ,  $V_{ne}$  is positive in magnitude ( note that the near-end noise due to crosstalk is negative ) because the magnitude of switching noise generated ( positive in magnitude ) is larger compared to near-end noise magnitude ( negative in magnitude ). When  $N = 1$  ( switching noise is smaller ), and when the interconnects are closely spaced ( near-end noise is larger ),  $V_{ne}$  is negative. In Figures 4.10 and 4.11, far-end noise (  $V_{fe}$  ) is plotted as a function of interconnect spacing for different numbers of simultaneously switching outputs, for thin and thick film technologies respectively. When  $N$  is equal to 16,  $V_{fe}$  is dominated by switching noise. The ( IS ) model under-estimates

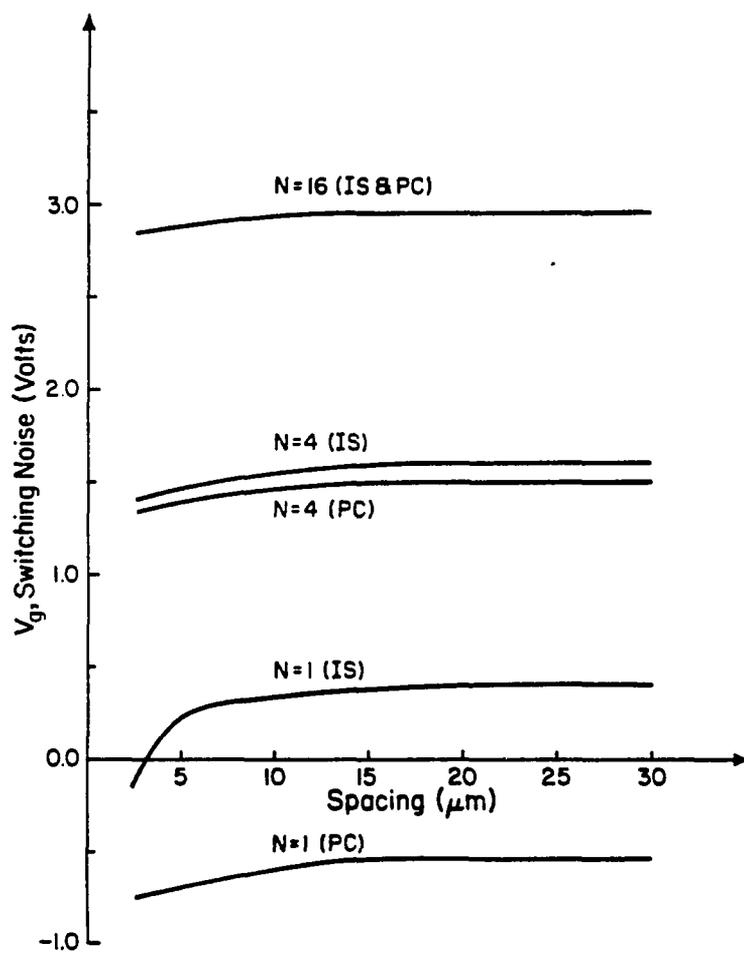


Figure 4.6: Switching noise vs interconnect spacing ( Thin film )

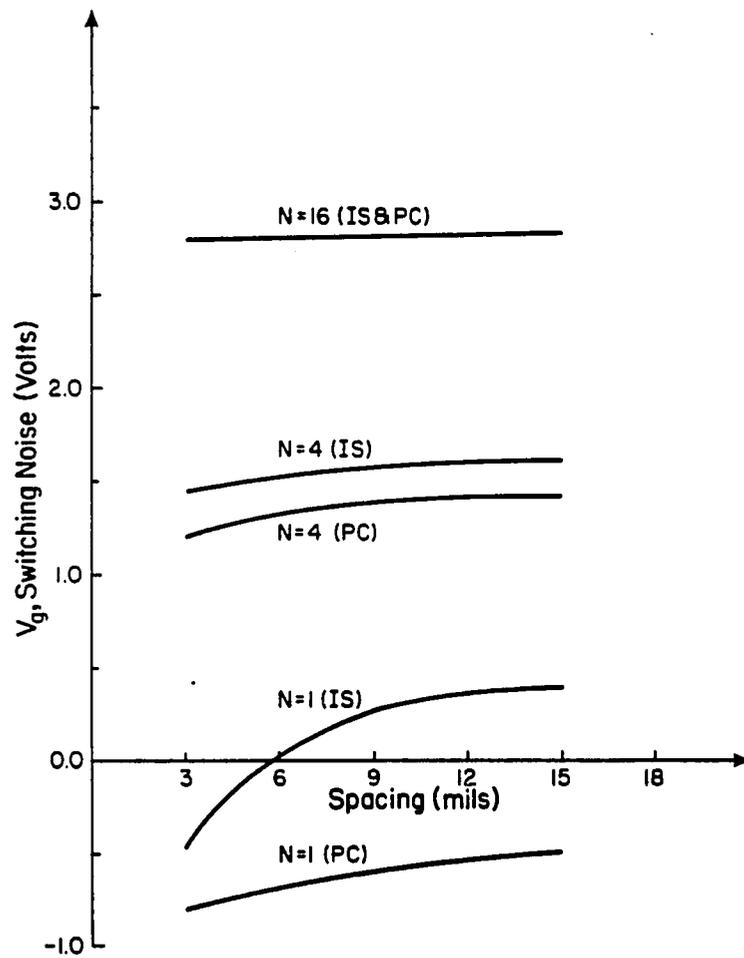


Figure 4.7: Switching noise vs interconnect spacing ( Thick film )

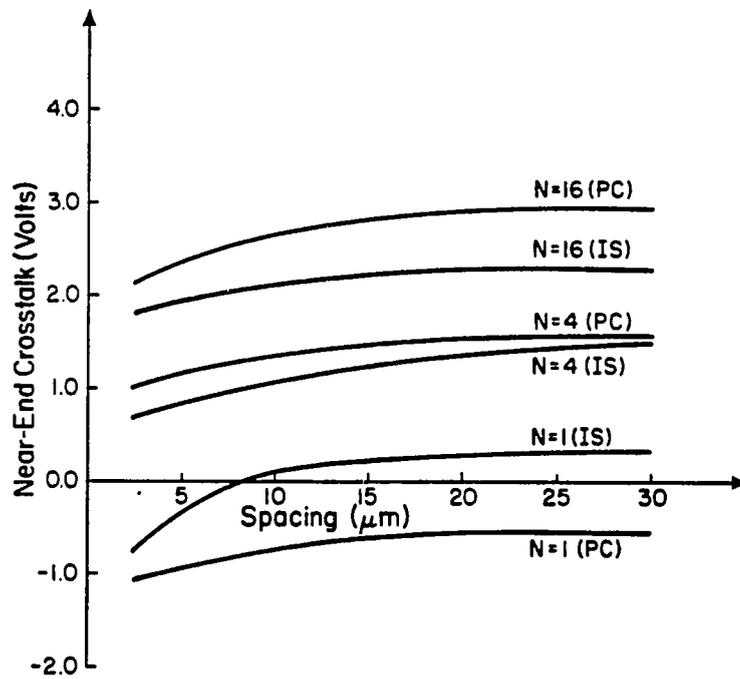


Figure 4.8: Near-end noise vs interconnect spacing ( Thin film )

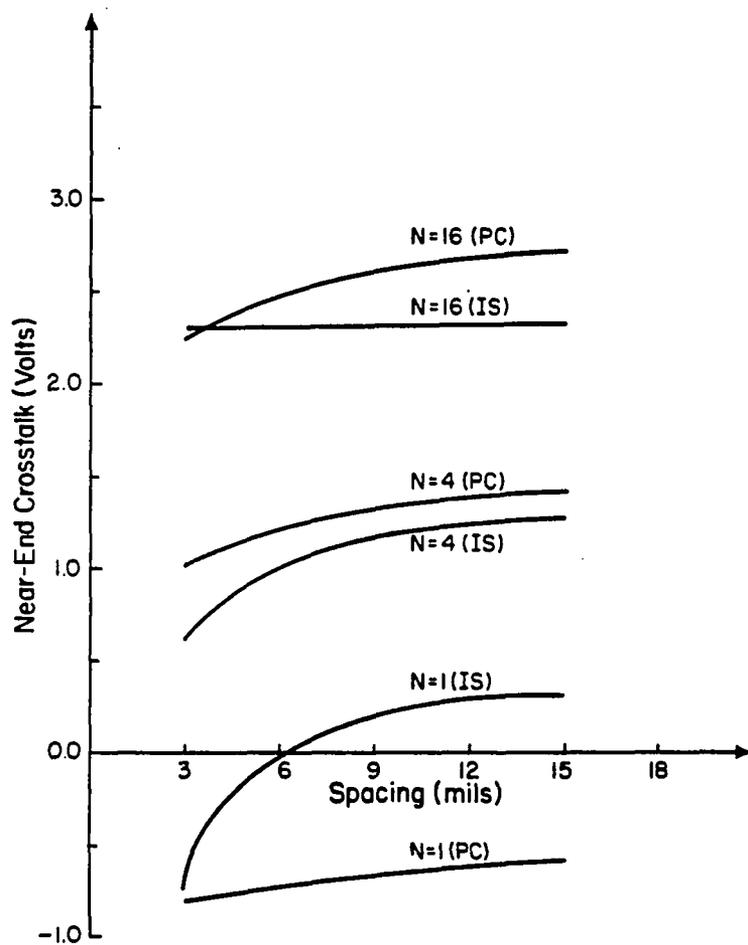


Figure 4.9: Near-end noise vs interconnect spacing ( Thick film )

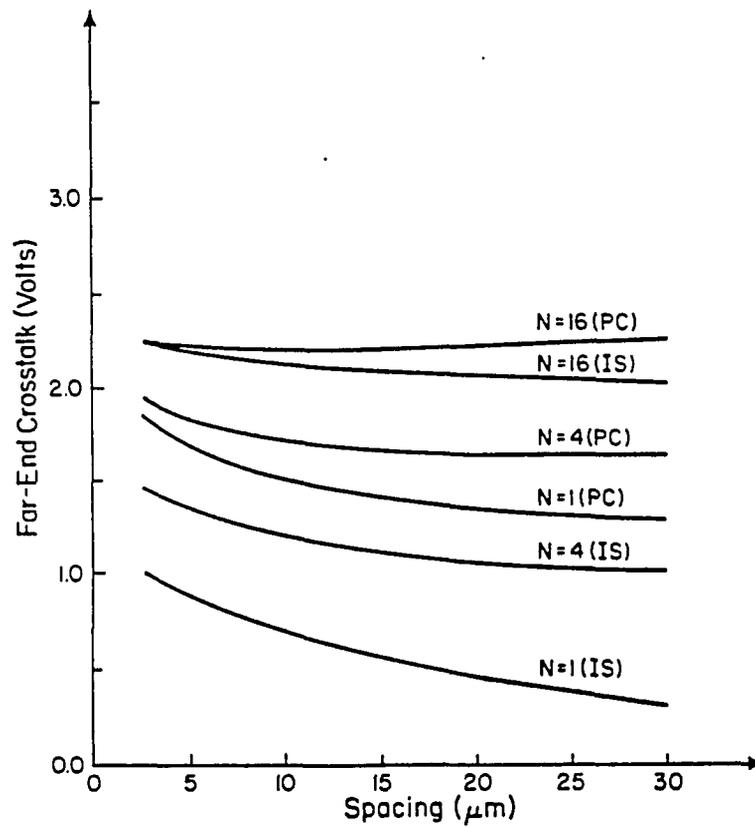


Figure 4.10: Far-end noise vs interconnect spacing ( Thin film )

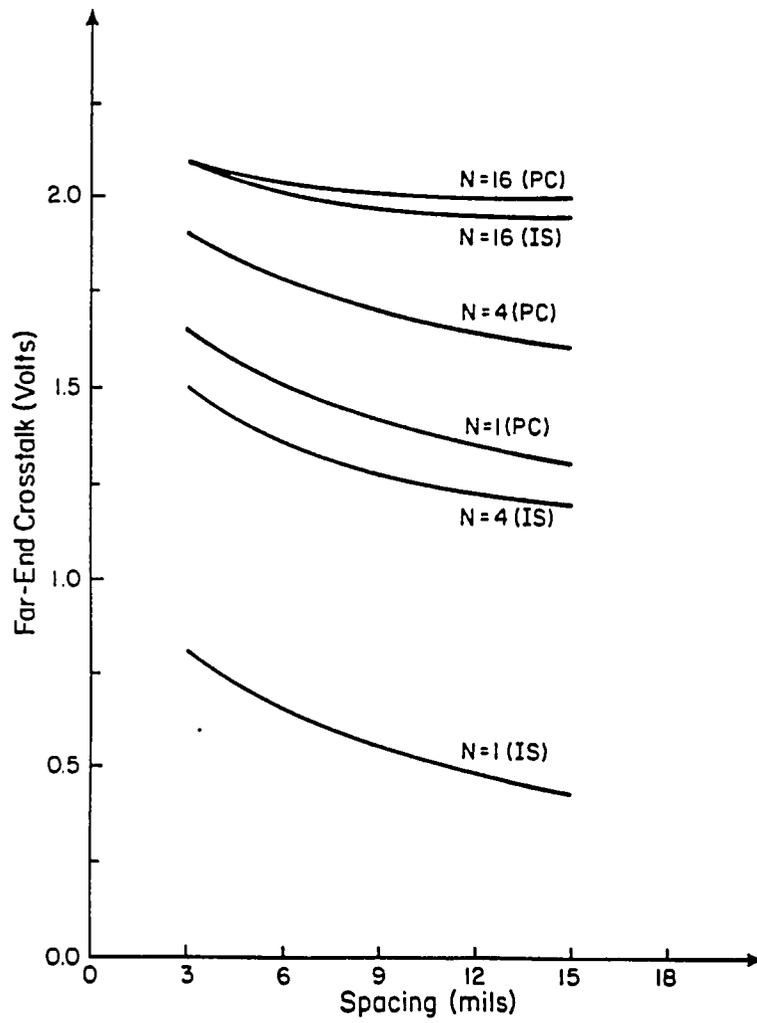


Figure 4.11: Far-end noise vs interconnect spacing ( Thick film )

$V_{fe}$  for all the cases because there is no coupling from the noisy ground conductor. Results from this study have demonstrated that switching noise, near-end noise and far-end noise characteristics are different for ( IS ) and ( PC ) models. This is due to the additional coupling from the ground plane in the ( PC ) model.

#### 4.5 Impact of $V_{ss}$ Package-Pin Placement on Noise Characteristics

In reality, there are localized  $V_{ss}$  pins ( or  $V_{ss}$  via connections ) on the  $V_{ss}$  plane. In Figure 4.12, coupled transmission lines over a noisy reference plane with package pin connections ( directly beneath or very near the L1 signal line and near the L2 quiet line ) are shown. The  $V_{ss}$  pins are modeled as R,L,C lumped circuit elements. The “ON” or “OFF” state of A, B, and C switches in Figure 4.12 denotes the “existence” or “non-existence” of that  $V_{ss}$  pin at that particular location on the  $V_{ss}$  plane. In Figures 4.13, 4.14 and 4.15, switching noise on the  $V_{ss}$  plane was plotted for (110), (101) and (111) package pin placements ( 110 means that the switches at A and B are “ON” and the switch at C is “OFF” ) for the thin film case with S equal to  $5\mu m$  and N equal to 16. For the (111) configuration, switching noise is reduced all the way from the near-end to the far-end, and reduced significantly at the far-end.

Package pin placement on the  $V_{ss}$  plane has an impact on the overall far-end noise values. To demonstrate this impact, in Figure 4.16,  $V_{fe}$  was plotted for the ( IS ) model and ( PC ) models with package pins. In the ( PC ) model, switching noise on the ground conductor is suppressed due to the path to a perfect ground through

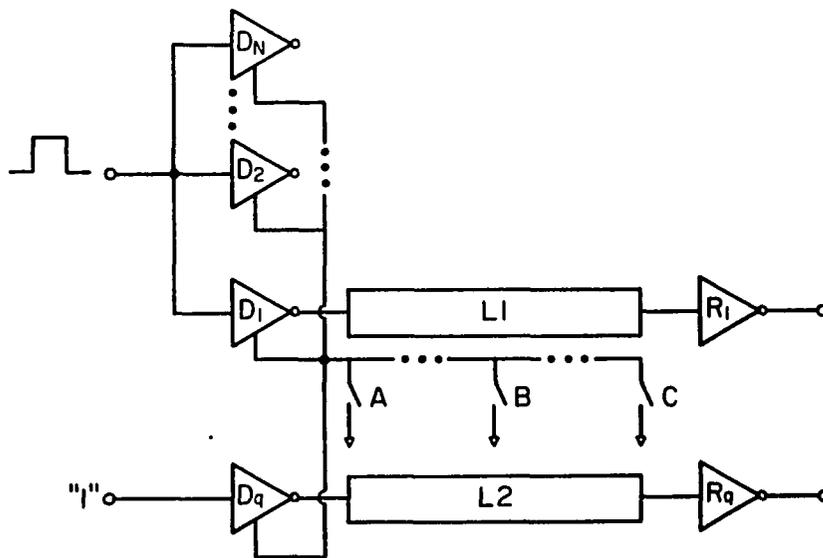


Figure 4.12: Package pin placement on the  $V_{ss}$  plane

the pins. In the ( IS ) model, noise on the  $V_{ss}$  plane is not suppressed and hence this model gives worst case far-end crosstalk values. It is clear from this study that  $V_{ss}$  package pins on the plane suppress the fed through switching noise from the quiet driver and the  $V_{ss}$  plane, and this reduces the overall noise at the far-end.

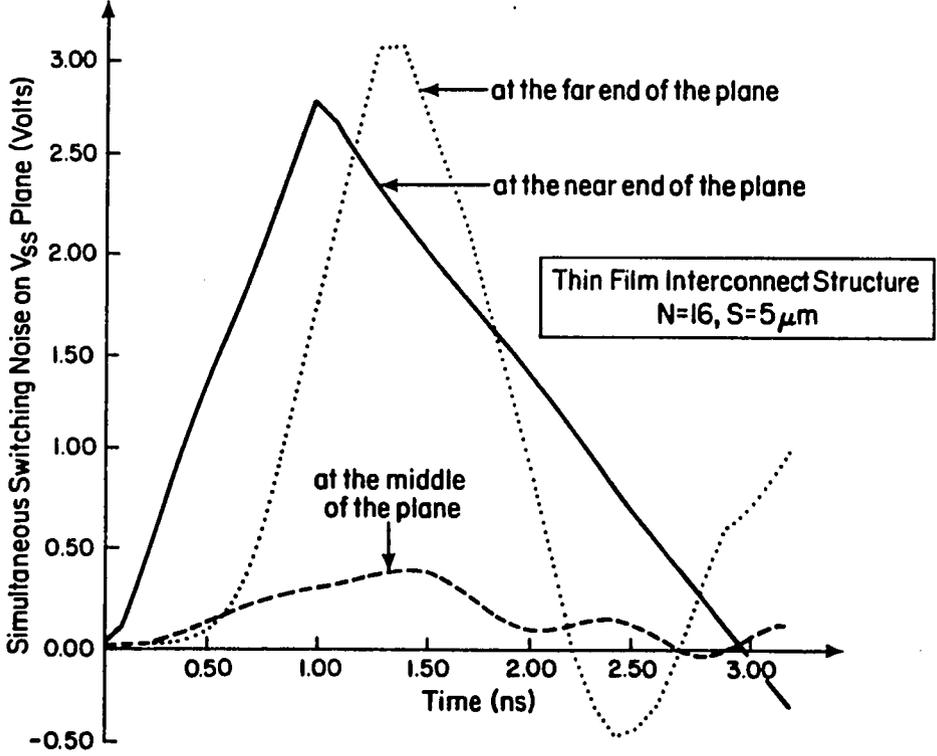


Figure 4.13: Effect of (110) package pin placement on noise on the  $V_{ss}$  plane

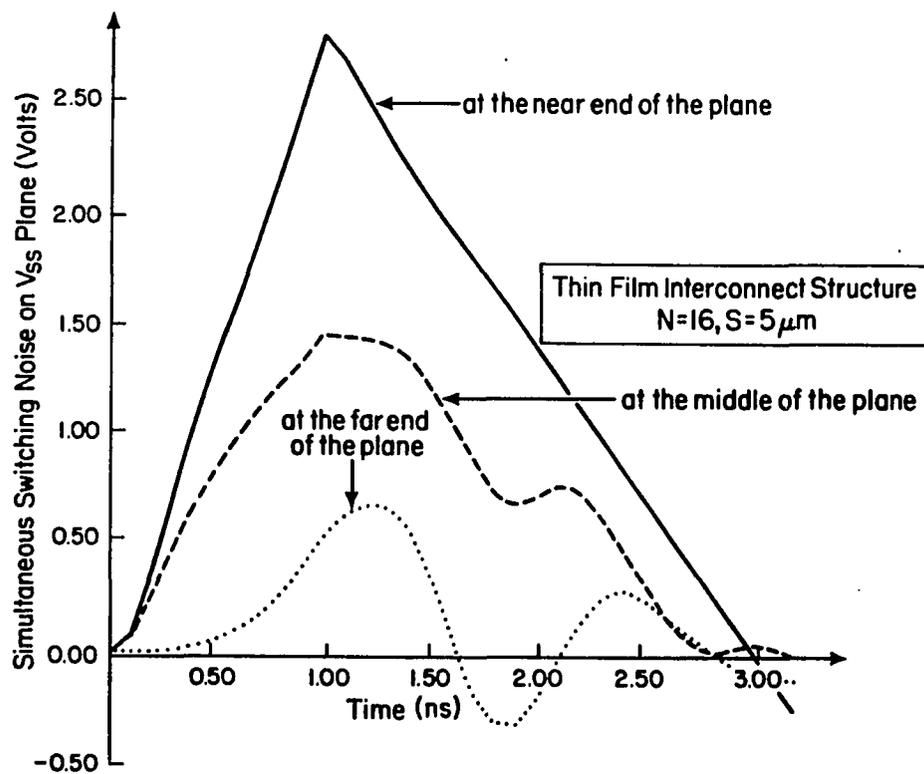


Figure 4.14: Effect of (101) package pin placement on noise on the  $V_{ss}$  plane

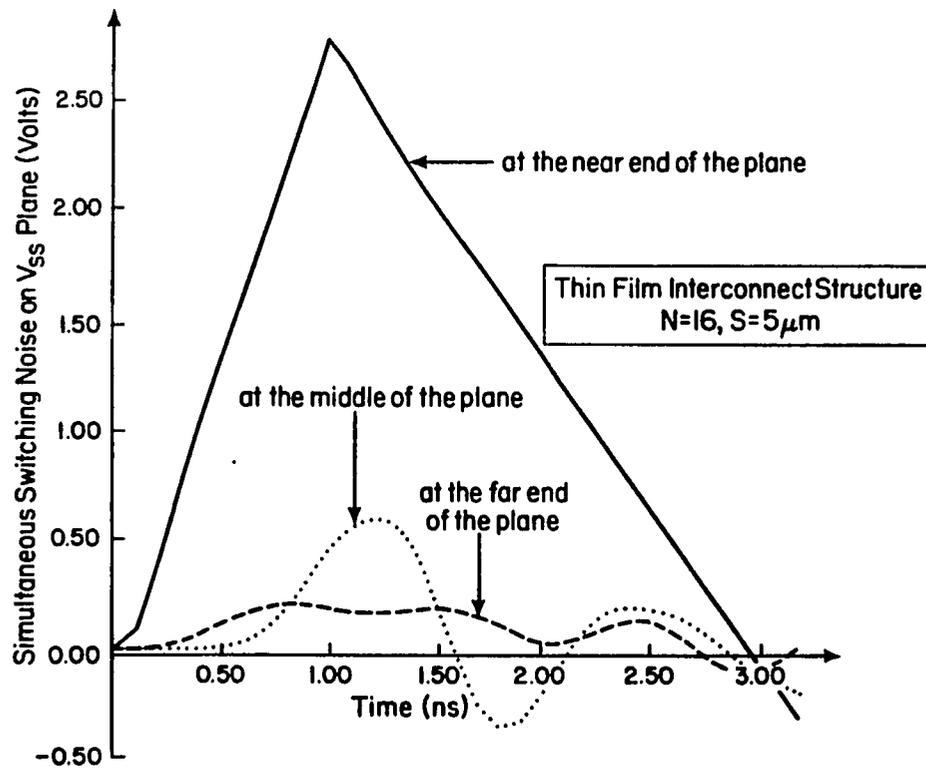


Figure 4.15: Effect of (111) package pin placement on noise on the  $V_{ss}$  plane

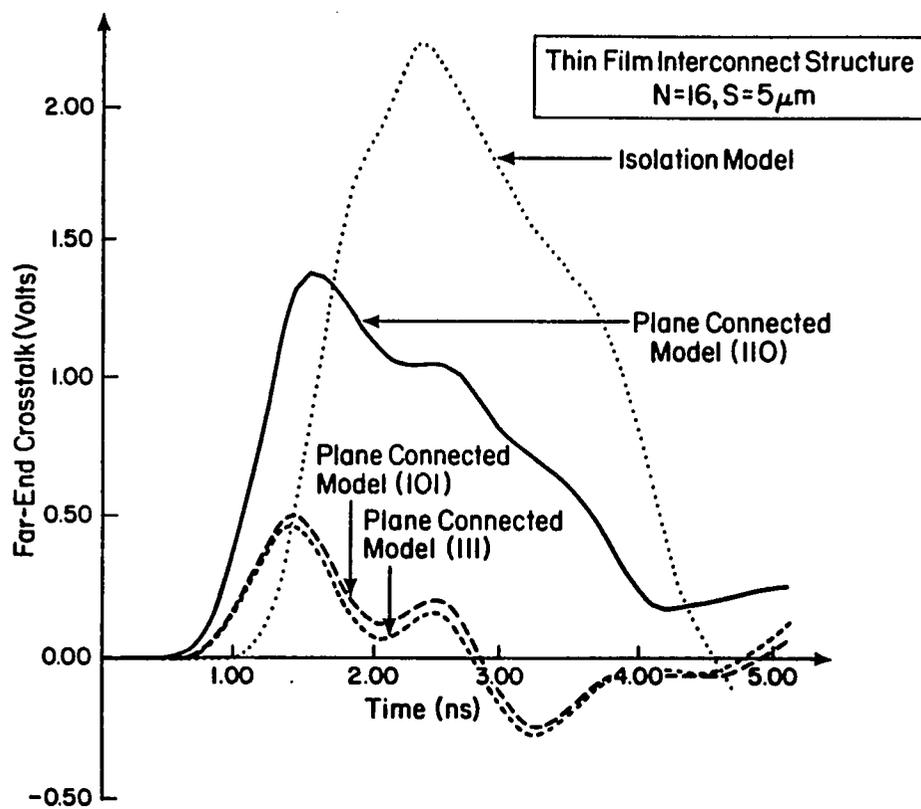


Figure 4.16: Far-end crosstalk for the "Isolation" and "Plane Connected" models

## CHAPTER 5

### Conclusions

It has been found that simultaneous switching noise has an underdamped oscillatory behavior and that the receiver noise immunity depends on both the width and the amplitude of the noise pulse. Guidelines for skewing the switching of the outputs to minimize simultaneous switching noise were developed considering the underdamped characteristics of switching noise. Design curves, illustrating performance trade-offs, were given for using damping resistors to minimize simultaneous switching noise without any trade-off in the driver delays. A method to model and simulate coupled lines over noisy reference planes has been presented. Using this model, the effect of a noisy reference plane on signal propagation through the interconnects above the plane was studied. The overall noise levels obtained using this model were compared with those obtained using the conventional "isolated" (switching noise isolated) model. Significant differences were found in the near-end noise, far-end noise and switching noise characteristics and, were explained. It was shown that proper distribution of  $V_{cc}$  package pins can improve the noise budget of a system significantly.

## Appendix A

A. E. Ruehli's equation that was used for calculating the partial self inductances in Chapter 4 is given below [10].

$$\begin{aligned} \frac{L_{p_{ii}}}{l} = & P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 - P_8 + P_9 + P_{10} + P_{11} - P_{12} + P_{13} \\ & + P_{14} + P_{15} + P_{16} + P_{17} + P_{18} + P_{19} + P_{20}, \quad (\text{A.1}) \end{aligned}$$

where

$$P_1 = \frac{2\mu}{\pi} \frac{\omega^2}{24u} [\ln(\frac{1+A_2}{\omega}) - A_5],$$

$$P_2 = \frac{1}{24u\omega} [\ln(\omega + A_2) - A_6],$$

$$P_3 = \frac{\omega^2}{60u} (A_4 - A_3),$$

$$P_4 = \frac{\omega^2}{24} [\ln(\frac{u+A_3}{\omega}) - A_7],$$

$$P_5 = \frac{\omega^2}{60u} (\omega - A_2),$$

$$P_6 = \frac{1}{20u} (A_2 - A_4),$$

$$P_7 = \frac{u}{4} A_5,$$

$$P_8 = \frac{u^2}{6\omega} \tan^{-1}\left(\frac{\omega}{uA_4}\right),$$

$$P_9 = \frac{u}{4\omega} A_6,$$

$$P_{10} = \frac{\omega}{6} \tan^{-1}\left(\frac{u}{\omega A_4}\right),$$

$$P_{11} = \frac{A_7}{4},$$

$$P_{12} = \frac{1}{6\omega} \tan^{-1}\left(\frac{u\omega}{A_4}\right),$$

$$P_{13} = \frac{1}{24\omega^2} [\ln(u + A_1) - A_7],$$

$$P_{14} = \frac{u}{20\omega^2} (A_1 - A_4),$$

$$P_{15} = \frac{1}{60\omega^2 u} (1 - A_2),$$

$$P_{16} = \frac{1}{60u\omega^2} (A_4 - A_2),$$

$$P_{17} = \frac{u}{20} (A_3 - A_4),$$

$$P_{18} = \frac{u^3}{24\omega^2} \left[ \ln\left(\frac{1+A_1}{u}\right) - A_5 \right],$$

$$P_{19} = \frac{u^3}{60\omega^2} [(A_4 - A_1) \text{ and}$$

$$P_{20} = \frac{u^3}{60\omega^2} [(A_4 - A_1) + (u - A_3)],$$

where

$$A_1 = \sqrt{1 + u^2},$$

$$A_2 = \sqrt{1 + \omega^2},$$

$$A_3 = \sqrt{\omega^2 + u^2},$$

$$A_4 = \sqrt{1 + \omega^2 + u^2},$$

$$A_5 = \ln\left(\frac{1+A_4}{A_3}\right),$$

$$A_6 = \ln\left(\frac{\omega+A_4}{A_1}\right) \text{ and}$$

$$A_7 = \ln\left(\frac{u+A_4}{A_2}\right),$$

where  $u = \frac{l}{W}$  and  $\omega = \frac{T}{W}$ . Here  $l$  is the length,  $W$  is the width and,  $T$  is the thickness of the interconnect respectively.

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