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The electrical properties and reliability of solder bump interconnections

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THE ELECTRICAL PROPERTIES AND RELIABILITY OF SOLDER BUMP INTERCONNECTIONS

by

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Date

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ABSTRACT

The electrical properties (resistance, capacitance, and inductance) of spherical solder bumps are computed. The solder bump is modeled using a finite, lossless transmission line model. The resistive, capacitive, and inductive effects are calculated separately then combined using superposition. The transmission line impedance for a 300 μm solder bump is calculated and the effect on a 100 nsec rise time signal is computed. Several methods to calculate fatigue lifetime are examined then related to reliability and design parameters. Methods to improve reliability are examined and their impact on electrical performance discussed.

CHAPTER 1

INTRODUCTION

Solder bumps have been used to attach IC chips to substrates since 1964. While some significant research was published by IBM in the late 1960's, current developments, trends, and electronic packaging philosophy warrants a new look at solder bumps. Other companies have recently employed solder bumps in their package design so research literature, mostly concerning fatigue lifetime, has blossomed again. Electronics, especially packaging, has changed dramatically since the late 1960's, solder bumps should be examined from a total packaging performance perspective.

Packaging has four major functions:

1) supply electrical power for circuit operation,
2) distribute electrical signals carrying information,
3) remove heat generated by these circuits, and
4) provide mechanical support and protection for the chip.

Solder bumps impact each of these to some extent. Very little work has been published on the electrical characteristics of solder bumps (Tummala and Rymaszewski 1989; Sasaki, Kishimoto, and Matsui 1987; Temmyo et al. 1983). It is believed that solder bumps don't have a significant affect on electrical

performance. However, as operating speeds increase and the minimum feature size decreases, the package engineer must be increasingly diligent concerning each aspect of packaging. An excellent means of capturing "the big picture" is through a system performance perspective.

The packaging performance of an electronic device has four major components:

1) cost, Q,
2) electrical performance, E,
3) reliability, R, and
4) geometric dimensions / weight, V.

Each of these has a weighting factor, w, dependent on its relative importance. The overall performance, M, is a function of these components and weighting factors and can be written (Palusinski 1993)

$$M = f(Q, E, R, V). \tag{1-1}$$

The function f can be a linear and algebraic combination of reliability and electrical performance divided by the product cost and volume such as

$$M = \frac{w_e E + w_r R}{QV} \tag{1-2}$$

or a linear combination of them. This relationship could easily be applied to individual components with the design. Two components, electrical performance and reliability, are

examined herein. Evaluating the cost component which is equally important is beyond the scope of this paper.

The electrical performance of solder bumps is characterized by their effect on signals and power distribution. First the resistance, capacitance, and inductance are calculated. Then the effect on transmission line operation is examined. The reliability is examined from two perspectives: lifetime prediction models and methods to improve reliability. Reliability prediction has long been a problem with solder joints in general. Solder bumps pose a greater concern since solder is used as a structural member and for electrical bonding. The complex microstructure and low melting point present challenges from a structural reliability standpoint.

CHAPTER 2

ELECTRICAL PROPERTIES

This section examines the basic electrical characteristics: resistance, capacitance, and inductance, of solder bumps. Methods used to calculate these properties are described and the results discussed.

2.1 Solder bump geometry

Before the properties can be calculated, the geometry of the bumps must be defined. When solder bumps were initially designed their shape was greatly influenced by reliability. An article by L.S. Goldmann (1969) describes the method for optimizing solder bump geometry for reliability. Optimization occurs when there is an equal probability of bump failure (fracture) at the chip/bump interface or the substrate/bump interface. The actual method involves three steps: 1) determine the value of K, the ratio of ultimate shear strengths of the chip/bump interface to the bump/substrate interface, experimentally. 2) Determine the appropriate value of β, the constant in the shear stress-strain relationship $\tau = A\gamma^{\beta}$. 3) Calculate the optimum solder volume. Since reliability is still a key issue this optimization method will

be used to generate bump geometry. To simplify matters somewhat, the calculations and figures will be done for 95/5 Pb/Sn solder. Also, the optimization parameters, β and K, were readily available for this solder. The methodology used is applicable to other solders. The resistivity of solder is 19.5 mΩ-cm as given in the ASM Materials Handbook (1978).

Determining solder geometry per Goldmann's method uses a set of three equations relating the chip pad size to the substrate pad size then calculating the bump height and volume. The pad sizes are related by the following relationship:

$$r_c = \frac{r_s}{\sqrt{K}} \qquad (2\text{-}1)$$

where r_c is the bump radius on the IC chip pad,

r_s is the bump radius on the substrate pad.

K is a function of manufacturing process parameters. A value of 1.59 was obtained from experimental data by Goldmann (1969) and will be used here.

The optimum solder bump height is found using the following relationship (Goldmann 1969)

$$h = \sqrt{\frac{3\beta}{2-\beta}\left(r_s^2+r_c^2\right)} \qquad (2\text{-}2)$$

A value of .58 will be used for β which is valid for 95/5 Pb/Sn and chips ranging from 40 to 120 mils on a side (Goldmann 1969). The volume of solder is the last parameter for optimization. The optimum volume is determined by the following formula (Goldmann 1969)

$$V = \frac{\pi}{2-\beta}\left(\frac{3\beta}{2-\beta}\right)^{\frac{1}{2}}\left(r_s^2 + r_c^2\right)^{\frac{3}{2}} \quad . \qquad (2\text{-}3)$$

The amount of solder deposited determines the height of the solder bump so this is an important parameter for manufacturing and reliability.

Typical solder bump geometry is shown in figure 2.1 with the basic dimensions of r_s, r_c, and h. To simplify analysis the bumps were assumed to be cylindrical with a radius r_c. The term "bump diameter" refers to the substrate pad footprint: $D_{bump} = 2r_s$. Typical solder bump size ranges from 100 μm to 200 μm in diameter. Since the trend is to arrays with a greater quantity of bumps, this paper will use a range of 25 μm to 300 μm to cover a broad spectrum of sizes. The substrate footprint diameter which is equal to $2r_s$, will be the referenced bump diameter for all plots.

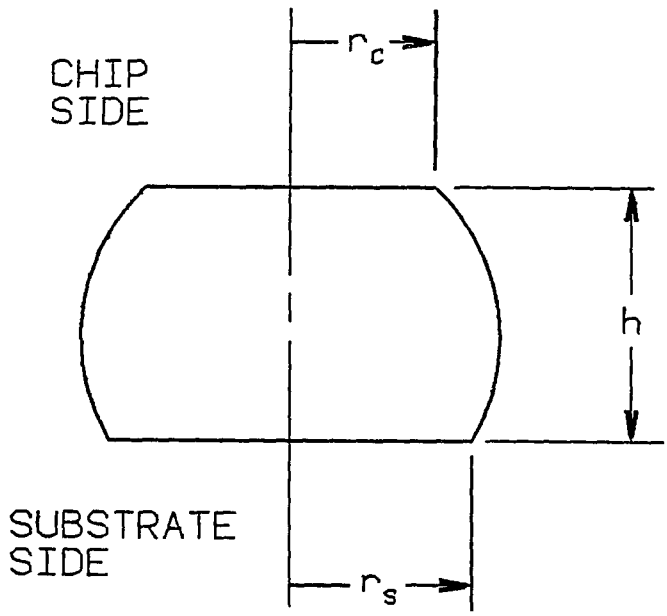


Figure 2.1 Solder bump geometry

2.2 Solder bump resistance

The d.c. resistance of a solder bump is determined from the simple formula

$$R = \rho \frac{l}{A} \qquad (2\text{-}4)$$

where ρ is the resistivity,

A is the cross-sectional area, and

l is the conductor length.

For solder bumps the length, l, is the optimum height, h. The cross-sectional area at the chip pad is used for A since it yields the minimum area. Substituting 2-2 into 2-4 yields the following relationship

$$R = \rho \frac{\sqrt{\frac{3\beta}{2-\beta}\left(r_s^2 + r_c^2\right)}}{\pi r_c^2} \quad . \qquad (2\text{-}5)$$

Simplifying 2-5 by using 2-1 yields equation 2-6 which shows the resistance to be inversely proportional to r_s

$$R = \rho \frac{\sqrt{\frac{3\beta}{2-\beta}\left(1+\frac{1}{K}\right)}}{\frac{\pi}{K} r_s} \quad . \qquad (2\text{-}6)$$

Figure 2.2 shows d.c. resistance as a function of bump diameter. Note that the maximum calculated resistance is only 11 mΩ for a 25 μm bump.

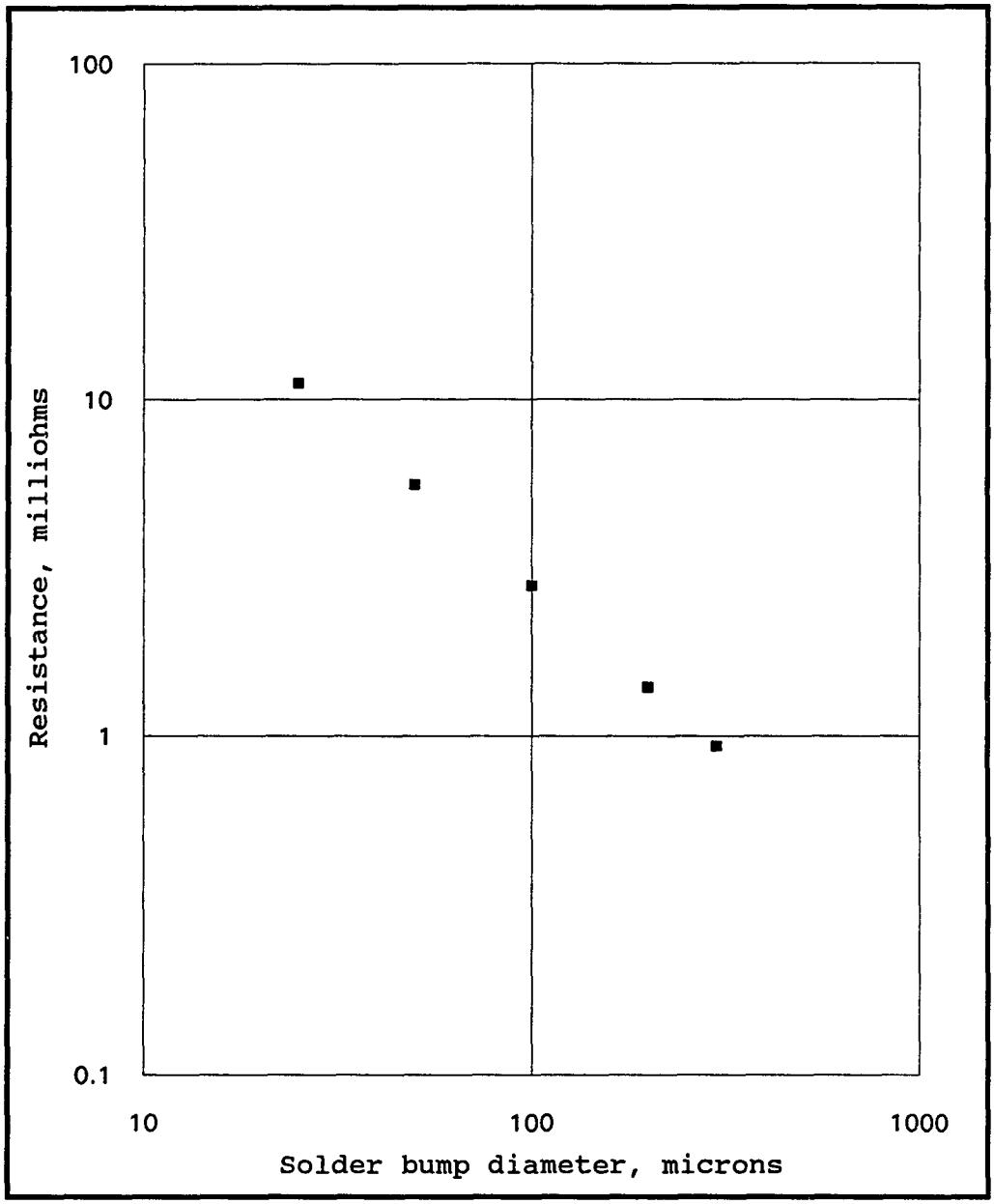


Figure 2.2 Solder bump d.c. resistance

The a.c. resistance of solder bumps is affected by the skin effect phenomenon. Alternating currents and fluxes tend to concentrate themselves towards the surface of a conductor. The relationship of conducting skin depth to signal frequency is

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \qquad (2\text{-}7)$$

where δ is the skin depth,

f is the signal frequency,

μ is the permeability of the conductor, and

σ is the solder conductivity.

Equation 2-7 is derived from uniform plane wave theory. The assumptions made are that the conducting plane is flat, infinite, a good conductor, the free space has approximately zero conductivity, both parts are a linear, isotropic, homogeneous medium, and the net free charge in the region is zero. It is further assumed that σ, μ and ϵ are independent of frequency. Before skin effect can be applied the quality of conductivity must be established. At high frequencies the following relationship must hold to show unqualified good conductivity (Paul and Nasar 1987)

$$\frac{\sigma}{\omega\epsilon} >> 1 \quad .$$

For 95/5 solder at 100 GHz $\sigma/\omega\epsilon$ is equal to 9.23×10^5 sec/Ω-F-rad qualifying it as a good conductor. Application of the skin depth formula is restricted by geometry. Since

equation 2-7 was derived for planar applications it may be used for cylindrical conductors only if the ratio of the conductor radius is large (>3x) compared to the skin depth so the curvature is negligible (Rama, Whinnery, and Van Duzer 1984). Figure 2.3 shows the critical bump diameter, D_B^*, at which skin depth is equal to one third the chip pad radius, r_c, versus frequency. In this case the conducting cross-section of the bump can be assumed to be an annular ring. The resistance for cases where the skin depth is small (less than .33 r_c), is found using (Paul and Nasar 1987)

$$R = \rho \frac{h}{\pi (2\delta r_c - \delta^2)} \quad . \tag{2-8}$$

For frequencies where the skin depth is not as pronounced ($r_c > \delta > .33 r_c$) the resistance can be found using 2-9, derived from applying Bessel functions to 2-7 (Carter 1967) obtaining

$$R = \rho \frac{h}{\pi r_c^2} \left[1 + \frac{1}{192} \left(\frac{r_c}{\delta} \right)^4 \right] \quad . \tag{2-9}$$

Figure 2.4 shows the theoretical frequency dependency of solder bump resistance for several bump diameters. Note that this is total resistance since the bump height is optimized for a given bump diameter. The d.c. resistance values are shown for comparison at a frequency of 1 MHz. The a.c. resistance curves for the various solder bump sizes start at different frequencies. This is because the skin effect

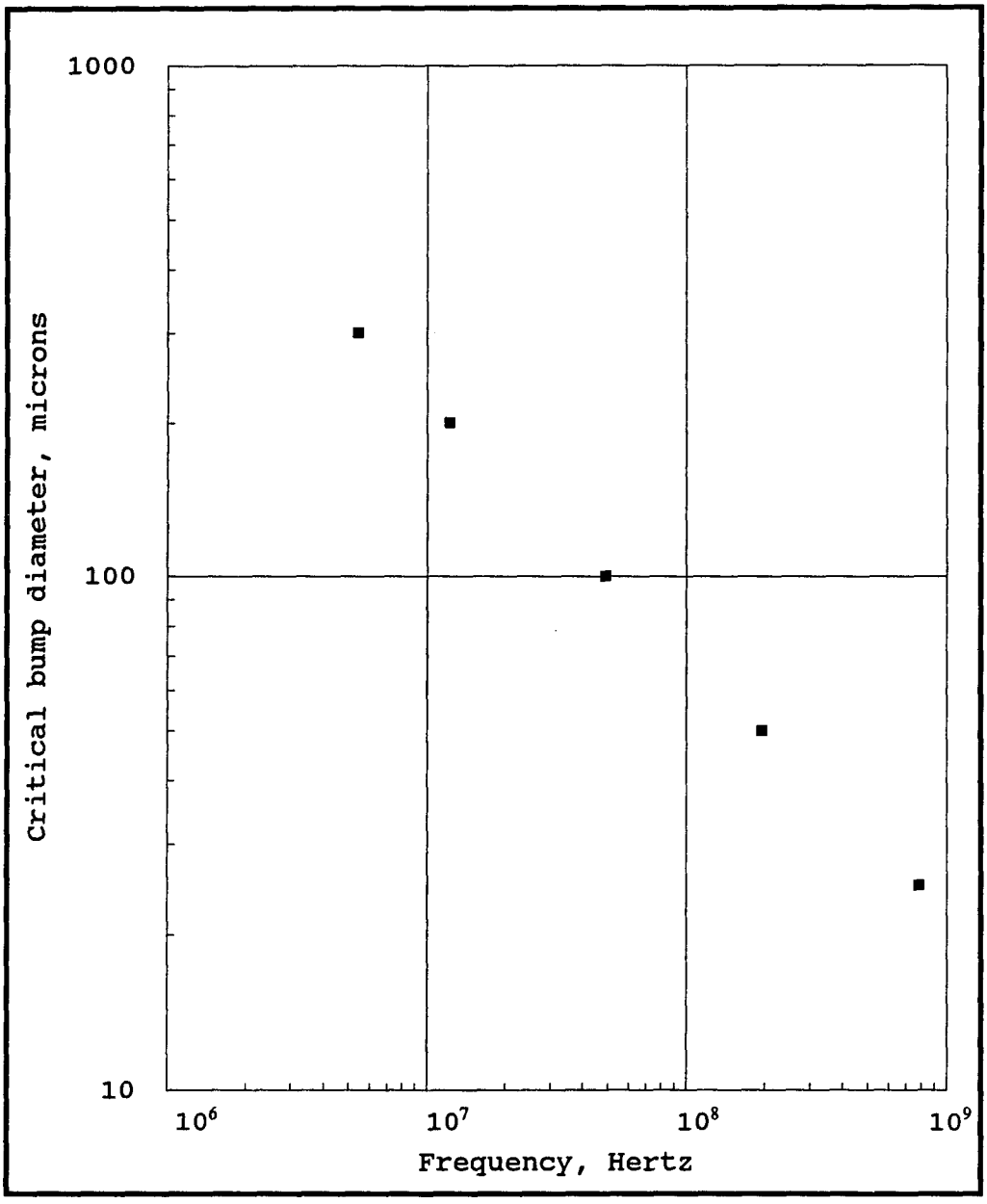


Figure 2.3 Critical bump diameter for skin effect

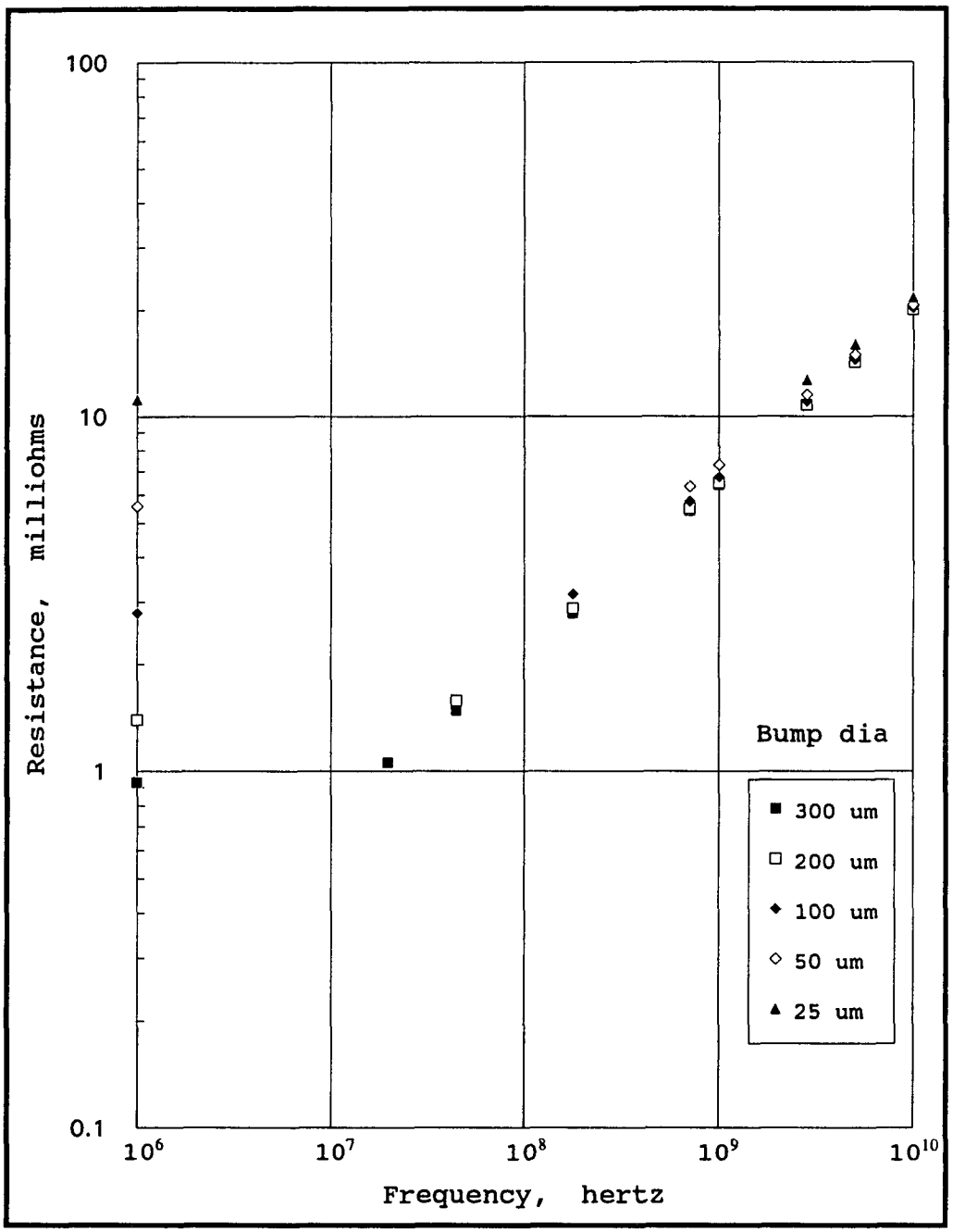


Figure 2.4 Solder bump a.c. resistance

frequency increases exponentially as the solder bump diameter decreases as shown in figure 2.3. For a 300 μm bump the skin effect approximation (equation 2-8) can be used when $f \geq 20$ MHz but for a 25 μm bump f must be larger than 3 GHz. Figure 2.4 points out a couple interesting items. First, at a frequency of 10 GHz the bump resistance is still only 20 mΩ. Second, the bump resistances converge as frequency increases and the skin depth becomes small. This can be predicted by using equation 2-8 and substituting equation 2-2 in for h. Ignoring the δ^2 term which is very small compared to $2\delta r_c$, equation 2-8 simplifies to

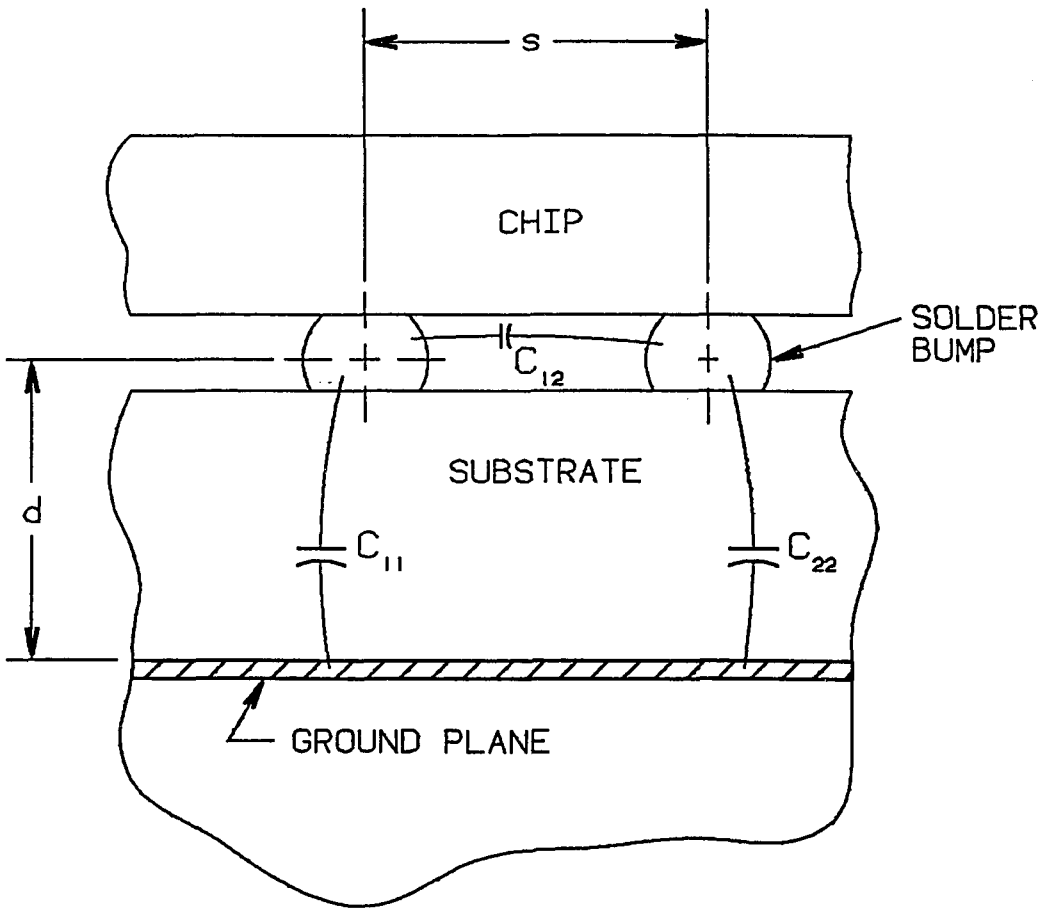
$$R \approx \left[\left(\frac{3\beta}{2-\beta}\right)(1+K)\,\frac{\mu\rho}{4\pi}\,f\right]^{\frac{1}{2}} \qquad (2\text{-}10)$$

for high frequencies. The only variable in this equation is the frequency!

2.3 Solder bump capacitance

The capacitance of solder bumps is dependent on other conductors within the chip/substrate structure. To isolate the effects of solder bumps the method of partial capacitance developed by Ruehli (1972) will be used. Only a small portion of the conductor is modeled at a time thus the term partial. The total capacitance of a system is the combination of the capacitance with respect to a common datum, self capacitance, and the capacitance with respect to other elements, the mutual capacitance(s). Figure 2.5 shows the elements and geometry associated with partial inductance for solder bumps. For two conductors the total capacitance is the capacitance between the two conductors, in parallel with the series combination of the common datum node capacitance. For solder bumps the common node will be assumed to be the ground plane. Ruehli's method assumes the mode of propagation is a quasi-TEM type and holds few restrictions. There is a retardation time that must be considered if the structure size is not small compared to the wavelength or the internal delay times are not small compared to the rise time of the applied pulse.

To accurately describe the total capacitance of solder bumps it is necessary to develop a matrix accounting for the mutual capacitance with every conductor in the system. Two



C_{11} & C_{22} common datum capacitance (self capacitance)

C_{12} mutual capacitance between bumps

Figure 2.5 Partial capacitance terms

significant terms in this matrix will be the ground/power plane quantity and capacitance with other bumps with dissimilar charges (voltage). Computing all the mutual capacitances can lead to a large matrix and cumbersome analysis so it may be expeditious to consider only the most significant quantities.

The self capacitance of a solder bump with respect to other solder bumps can be found by assuming they are adjacent, parallel, cylindrical conductors and is given by

$$C = \frac{\pi \epsilon h}{\ln \frac{s}{r_s}} \qquad (2\text{-}11)$$

where ϵ is the permittivity,

s is the centerline distance between bumps,

h is the solder bump height, and

r_s is the bump radius.

This expression is adequate for first order calculations and is influenced by the position of the bump on the pad, the number of bumps, and the relative permittivity of the material between the bumps.

The capacitance of a solder bump with respect to a ground plane can be determined from (Smythe 1950)

$$C = 4\pi \epsilon r_s \sinh \alpha \sum csch\, n\alpha \qquad (2\text{-}12)$$

where α = acosh d/r_s, d is the distance between the center of the bump and the top of the plane; the summation is taken from n = 1 to ∞. This equation is the formula for the capacitance between a sphere and an infinite plane which is accurate enough for a first order approximation. This capacitance is chiefly dependent on the size of the bump. The ground plane effect is only noticeable when the distance between the plane and the bump is less than one bump diameter. As the distance increases beyond one bump diameter the mutual capacitance approaches the "self capacitance" of a sphere given by (Harrington 1958)

$$C_S = 4\pi\epsilon r_s \quad . \qquad (2\text{-}13)$$

He defined "self capacitance" as the capacitance an object has with respect to a sphere of infinite radius.

The capacitance with respect to a ground / power plane datum is shown in figure 2.6. The solder bump "self capacitance" as given by equation 2-13 versus solder bump diameter is shown in figure 2.7.

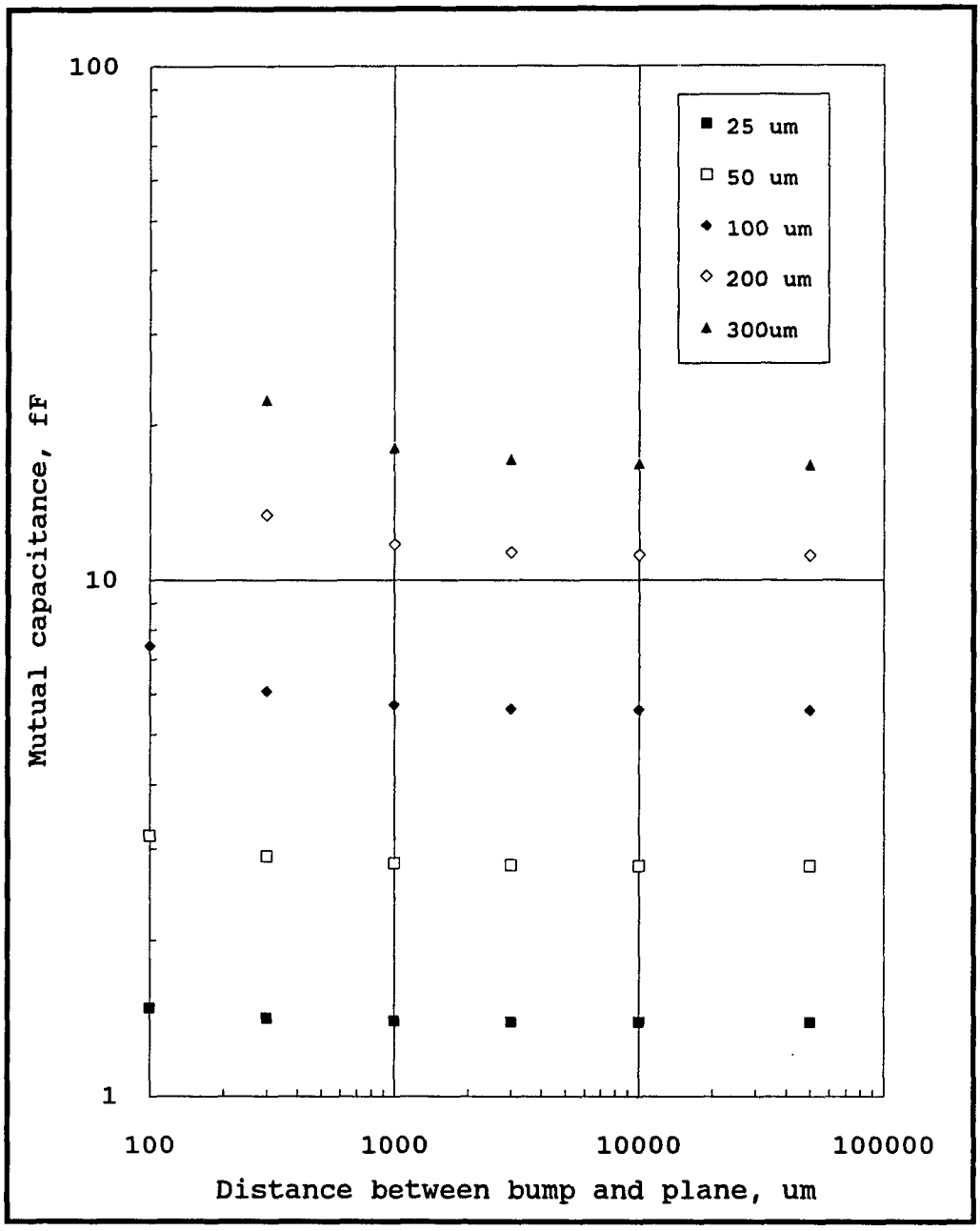


Figure 2.6 Solder bump capacitance with respect to a ground/power plane.

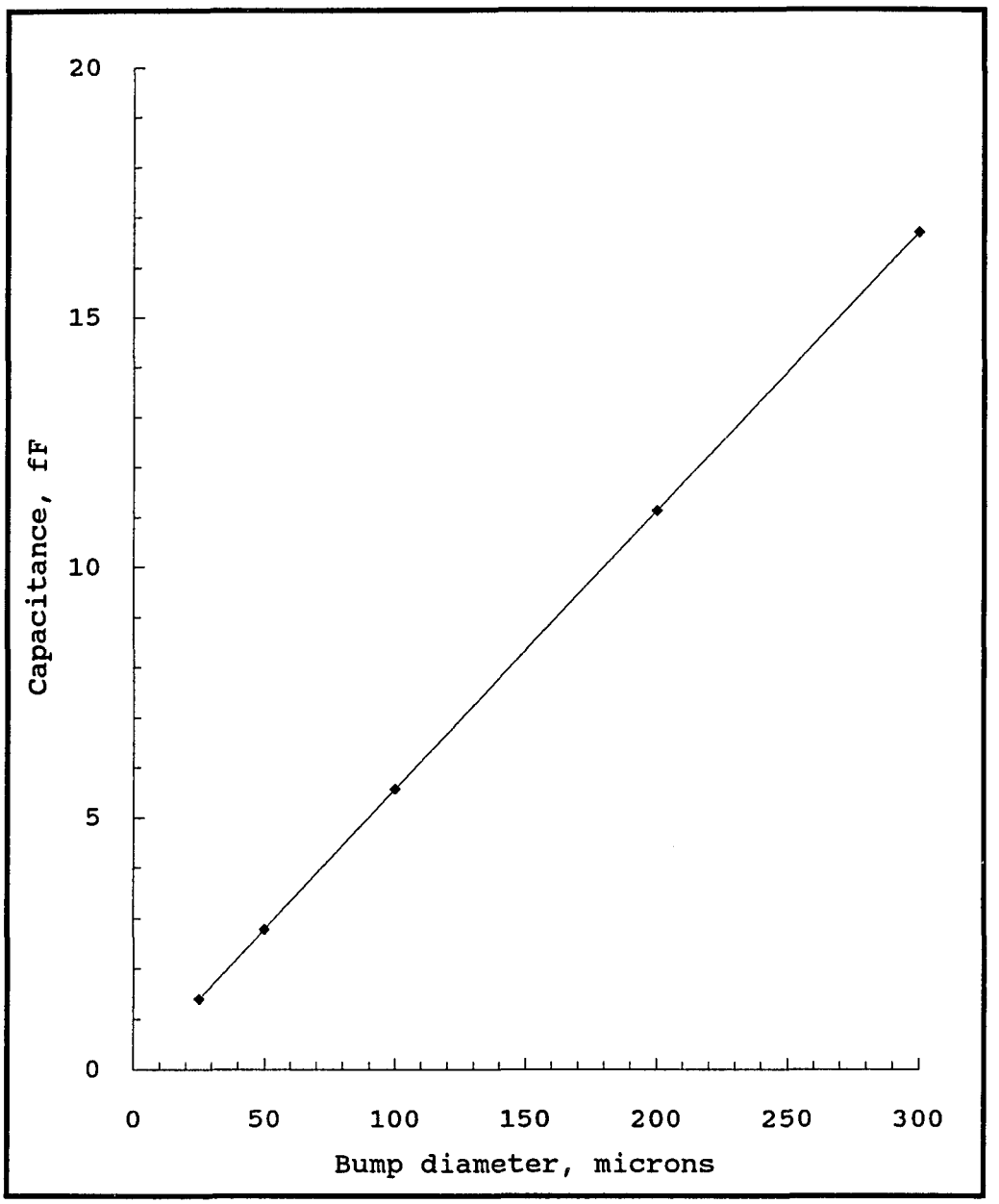


Figure 2.7 Solder bump "self capacitance"

2.4 Inductance of solder bumps

The inductance of solder bumps and their impact on electrical performance is evaluated using the method of partial inductances developed by Ruehli (1972). Ruehli's work is in turn based on work done by Grover (1973). Grover did extensive study into calculations of self and mutual inductance. These two parameters were developed because they are independent of the current magnitude making them useful for transmission line application, among others. Formulas for self and mutual inductances are valid for the following conditions. As with capacitance, the frequency is assumed to be low. However, the skin effect on inductance is small so the impact of frequency is small. For high frequency cases the presence of a nearby conductor (the spacing is small compared to the diameter) the current and therefore, flux will not be evenly distributed. For high frequency cases the inductance per unit length is equal to the inverse of the capacitance per unit length (Grover 1973). From Ruehli's work the following important and useful concepts arise. First, for partial inductance the current loop does not have to be closed. Secondly, conductors are locally decoupled if they are perpendicular to each other. Third, most common cross sections can be approximated accurately by a single rectangular conductor. Also, the partial mutual inductance is

a weak function of the conductor cross sections. Lastly, the current crowding effects are small, i.e., the current is uniform in the conductor. This last condition is not as significant as the others because the flux area doesn't change drastically so the inductance change will be small.

The two components of partial inductance are the self inductance and the mutual inductance. Partial inductance is useful because the conductor is broken down to arbitrary segments. The choice of segments usually coincides with corners in the conductor. For a given "loop" the inductance is represented as a matrix of self inductance (on the diagonal) and mutual inductances (off diagonal terms). The self inductance is the parameter a conductor has due to its own magnetic field. The mutual inductance is the inductance due to the flux from another conductor either in the same or separate circuit. The self inductance of solder bumps can be calculated using two means. If the solder bump is assumed to be a short segment of cylindrical wire of length h the self inductance is given by

$$L_{SI} = \frac{\mu}{4\pi} h \quad . \qquad (2\text{-}14)$$

Note that the diameter of the solder bump does not impact the self inductance directly. Substituting 2-1 and 2-2 into 2-14 bears out the relationship r_s has through the optimization of

the height shown in the following equation

$$L_{SI} = \frac{\mu}{4\pi} r_s \sqrt{\frac{3\beta}{2-\beta}\left(1+\frac{1}{K}\right)} \quad . \tag{2-15}$$

Grover (1973) states that the self inductance of a wire is independent of shape and can be approximated by a filament. For short wires he gives the self inductance in μH as

$$L_{SI} = .002h\left(\ln\frac{2h}{r_s} - .75\right) \quad . \tag{2-16}$$

Again, making the appropriate substitution for h in 2-16 yields

$$L_{SI} = .002 r_s \sqrt{\frac{3\beta}{2-\beta}\left(1+\frac{1}{K}\right)}\left[\ln\left(2\sqrt{\frac{3\beta}{2-\beta}(1+K)}\right) - .75\right] \tag{2-17}$$

noting that the term in brackets and inside the radical are constants and the self-inductance is a linear function of the bump diameter as in 2-14. Figure 2.8 shows the plot of self inductance versus bump diameter and points out the validity of the third assumption.

Solder bumps have a partial mutual inductance with any conductor that is parallel to it and carrying current. This includes other solder bumps, substrate vias, substrate pins, and IC vias. Due to the number of variables involved the partial mutual inductance is not calculated or plotted.

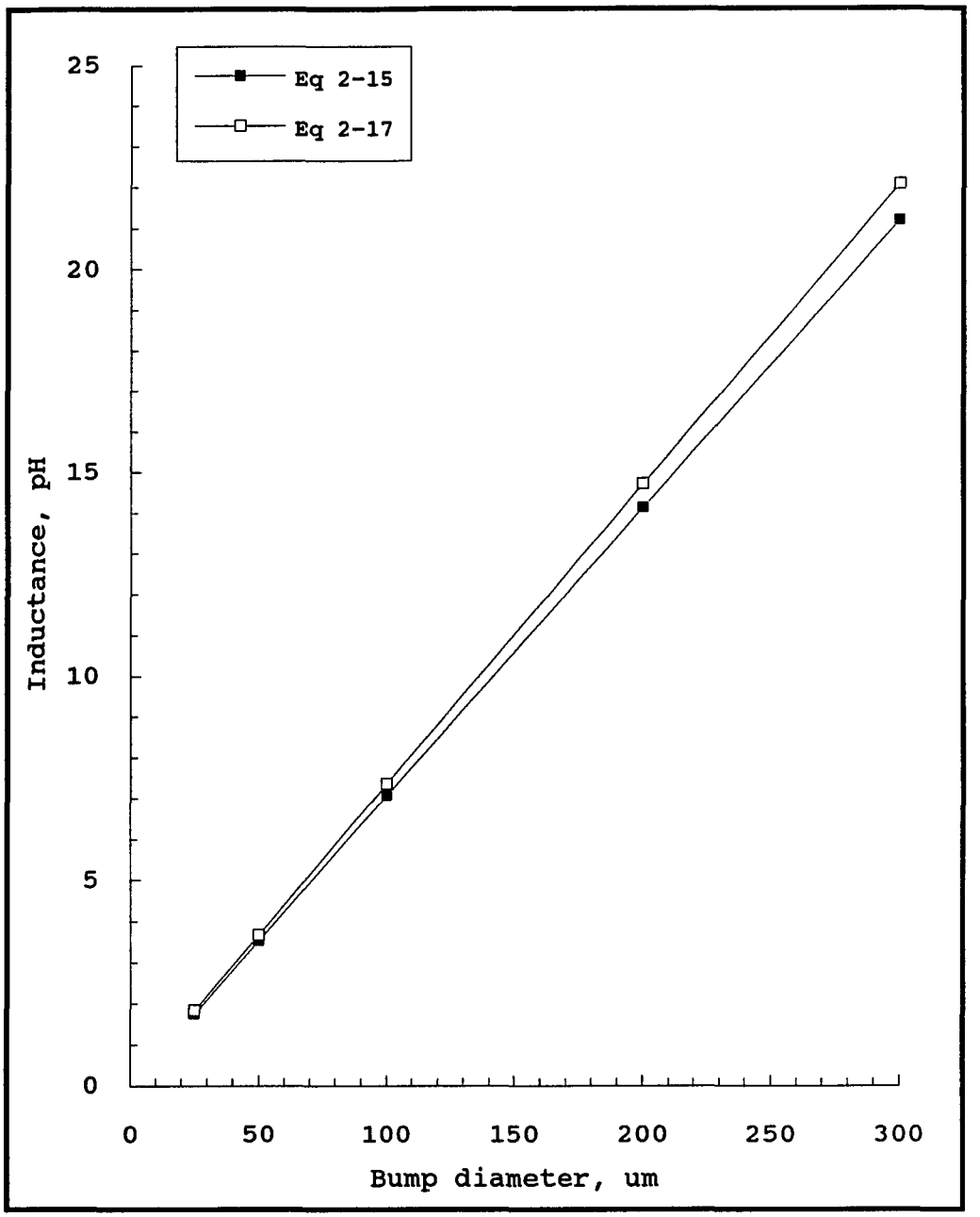


Figure 2.8 Solder bump self inductance

2.5 Concluding remarks

The calculated resistance of solder bumps was very small. D.C. values ranged from 1 mΩ for a 300 μm bump up to 11 mΩ for a 25 μm bump. Actual measurements of 50 μm bumps taken by Warner et al. (1991) showed the resistance to be about 5 mΩ. For comparison, a 1 mil diameter gold wirebond that is 100 mil long has a d.c. resistance of 110 mΩ. The a.c. resistance increased exponentially with frequency but was still only 20 mΩ at 10 GHz. These calculated numbers weren't correlated with experimental data or published data because none could be found.

The capacitance of solder bumps was separated into two parts: the self and mutual capacitance. The self capacitance ranged from a minimum of 1.5 fF for a 25 μm bump up to 18 fF for a 300 μm bump depending on distance to the ground plane. Again, very small numbers when compared with other IC components; a typical gold wirebond would have a 147 fF self capacitance. The total capacitance of a solder bump depends on the surrounding structure and was not calculated. The capacitance between stacked solder bumps and a ground plane was calculated by Sasaki, Kishimoto, and Matsui (1987) using finite element method analysis and was reported to be around 5 pF for 300 μm bumps. Their calculations included the effect of the mounting

pads which wasn't included here.

Inductance calculations were patterned after Grover and Ruehle and consisted of two components: self and mutual inductance. The self inductance ranged from 2 pH to 22 pH, increasing linearly as the diameter increased. Experiments by Jones and Herrell (1980) showed solder bump self inductance was 28 pH ± 2 pH for a 125 μm bump.

CHAPTER 3

TRANSMISSION LINE CHARACTERISTICS

3.1 Transmission line model

In a typical application such as a multichip module (MCM), the solder bump is best modeled as an intermediate discontinuity in the signal transmission line. As developed in chapter 2, solder bumps have resistive, capacitive, and inductive components. The comprehensive transmission line model with all these elements is shown in figure 3.1. The analysis will be performed assuming a finite lossless line with matched impedances.

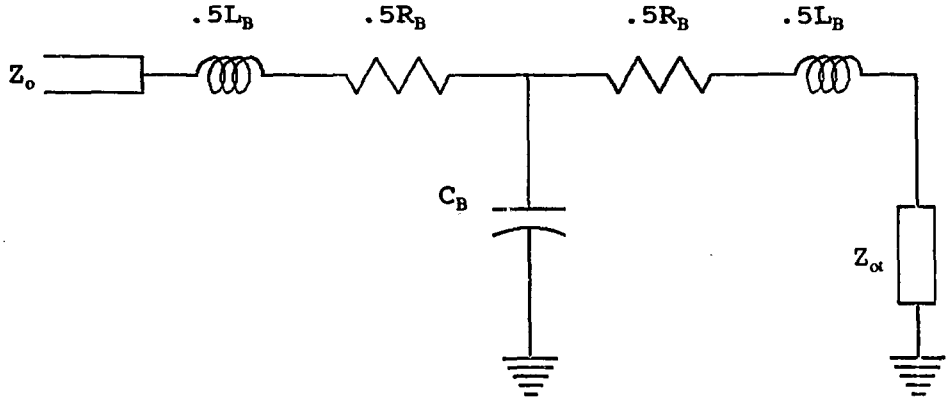


Figure 3.1 Solder bump transmission line model

3.2 Finite lossless line characteristics

The effect of an intermediate discontinuity in a lossless line can be determined by the amount of reflection generated by the discontinuity. A lossless line will have a series of reflections as the signal reflects off the discontinuity back to the source then returns to reflect again. In these series of reflections the initial reflection is the greatest so only the first reflection term will be considered in the solution to the ideal telegrapher's equation

$$\frac{\partial^2 v}{\partial x^2} = LC\frac{\partial^2 v}{\partial t^2} \qquad (3\text{-}1)$$

Assuming the line is distortionless and has real terminations, the solution with the first reflection only is (Menezes 1992)

$$V(x,s) = \frac{Z_o}{Z_o+Z_i}\mathcal{L}\{v_o(t)\}\left[e^{-sx/u} + \rho_t e^{-s(2l-x)/u}\right] \qquad (3\text{-}2)$$

where Z_o is the characteristic impedance of the line,

Z_i is the characteristic impedance of the near end termination,

l is the length of the line, and

ρ_t is the far-end reflection coefficient.

The far-end reflection coefficient is given by

$$\rho_t = \frac{Z_t - Z_o}{Z_t + Z_o} \qquad (3\text{-}3)$$

where Z_t is the far-end termination impedance.

To obtain the solution to equation 3-2 at the far end of the line, x/u is replaced by τl, resulting in

$$V(s) = \mathcal{L}\{v_o(t)\}\,[1+\rho_t]\,e^{-s\tau l} \quad . \tag{3-4}$$

The reflected signal from the far end is given by

$$V_r(s) = \mathcal{L}\{v_0(t)\}\,\rho_t \quad . \tag{3-5}$$

The effect of solder bumps on transmission line signals can be quantified using equations 3-3 and 3-5.

3.3 Analysis of an intermediate resistive discontinuity

The equivalent circuit of the solder bump resistive discontinuity is shown in figure 3.2.

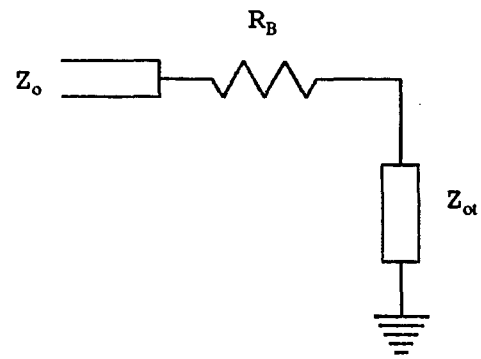


Figure 3.2 Equivalent circuit of resistive discontinuity

The termination impedance is simply the two impedances in series, $Z_t = Z_{ot} + R_B$. The reflection coefficient from equation 3-3 is

$$\rho_t = \frac{R_B + Z_{ot} - Z_o}{R_B + Z_{ot} + Z_o} \quad . \tag{3-6}$$

For a transmission line with equal impedances ($Z_o = Z_{ot}$) on either side of the intermediate discontinuity, equation 3-6 simplifies to

$$\rho_t = \frac{R_B}{R_B + 2Z_o} = \frac{1}{1 + \frac{2Z_o}{R_B}} \quad . \tag{3-7}$$

When $R_B << Z_o$ as it is with solder bumps then $2Z_o/R_B >> 1$ and equation 3-7 can be further simplified as

$$\rho_t = \frac{R_B}{2Z_o} \quad . \tag{3-8}$$

The reflection coefficient in equation 3-8 is positive meaning the reflection has the same sign as the signal. If the line impedance, Z_o, and the termination impedance, Z_{ot}, aren't perfectly matched then a reflection occurs and these parameters will determine the magnitude and sign of the reflected signal.

3.4 Analysis of an intermediate capacitive discontinuity

The equivalent circuit of the solder bump capacitive discontinuity is shown in figure 3.3.

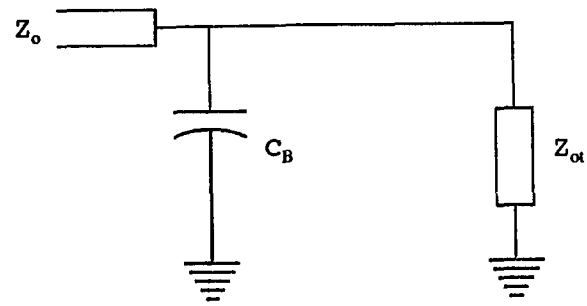


Figure 3.3 Equivalent circuit of capacitive discontinuity

The termination impedance is C_B in parallel with Z_{ot} and is

$$Z_t = \frac{Z_{ot}}{1 + Z_{ot} C_B s} \qquad (3\text{-}9)$$

where C_B is the common datum capacitance between the bump and the ground plane. The distance between the bump center and ground plane is assumed to be greater than one bump diameter. For ease of algebraic manipulation it is assumed that Z_o is equal to Z_{ot}. The far-end reflection coefficient is found using equation 3-3 again and is

$$\rho_t = \frac{-\frac{Z_o C_B}{2} s}{1 + \frac{Z_o C_B}{2} s} \quad . \qquad (3\text{-}10)$$

The input signal is assumed to be a ramped step function as shown in figure 3.4.

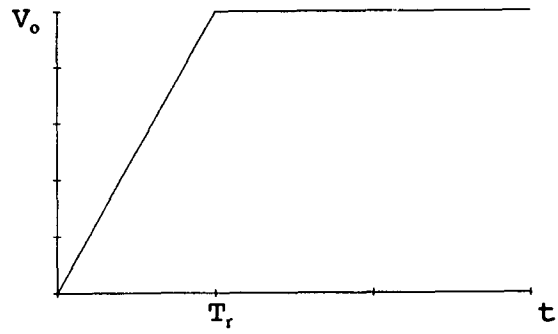


Figure 3.4 Input signal

The signal is further assumed to have a linear rise time to keep analysis manageable. The input signal is represented in the time domain by the formula

$$v_o(t) = \frac{V_o}{T_r}\{tu(t) - (t-T_r)u(t-T_r)\} \qquad (3\text{-}11)$$

and in the frequency domain by

$$\mathcal{L}\{v_o(t)\} = \frac{V_o}{T_r}\frac{1}{s^2}[1 - e^{-sT_r}] \quad . \qquad (3\text{-}12)$$

The reflected signal at the discontinuity is found by substituting equations 3-10 and 3-12 into equation 3-5 obtaining

$$V_r(s) = -\frac{V_o}{T_r}\frac{Z_o C_B}{2}\left(\frac{1}{s} - \frac{\frac{Z_o C_B}{2}}{1 + \frac{Z_o C_B}{2}}\right)(1 - e^{-sT_r}) \quad . \qquad (3\text{-}13)$$

Converting equation 3-13 to the time domain yields

$$v_r(t) = -\frac{V_o}{T_r}\frac{Z_o C_B}{2}\left[\left(1-e^{-\frac{2}{Z_o C_B}t}\right)u(t)-\left(1-e^{-\frac{2}{Z_o C_B}(t-T_r)}\right)u(t-T_r)\right]. \quad (3\text{-}14)$$

Finally, the transmitted signal, $v(t)$, can be expressed in the time domain as

$$\begin{aligned} v(t) &= \frac{V_o}{T_r}\left(tu(t)-(t-T_r)u(t-T_r)\right) \\ &-\frac{V_o}{T_r}\frac{Z_o C_B}{2}\left[\left(1-e^{-\frac{2}{Z_o C_B}t}\right)u(t)-\left(1-e^{-\frac{2}{Z_o C_B}(t-T_r)}\right)u(t-T_r)\right]. \end{aligned} \quad (3\text{-}15)$$

The graph of the transmitted signal and the reflected signal is shown in figure 3.5.

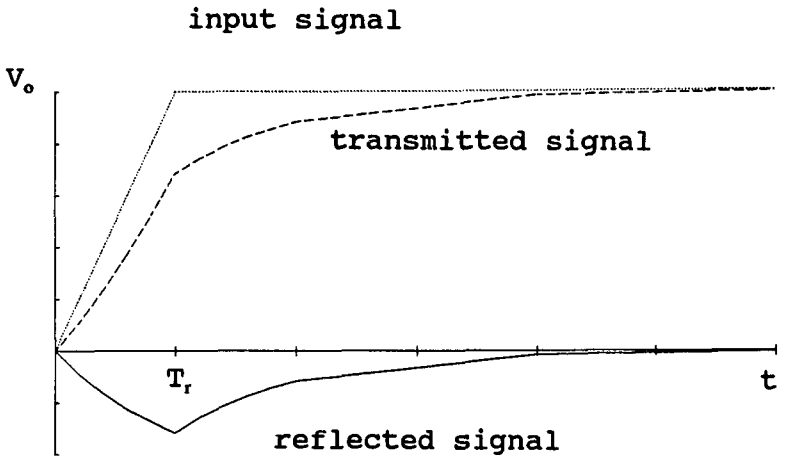


Figure 3.5 Graph of capacitive discontinuity effect

3.5 Analysis of an intermediate inductive discontinuity

The solder bump inductive discontinuity is represented by the equivalent circuit shown in figure 3.6.

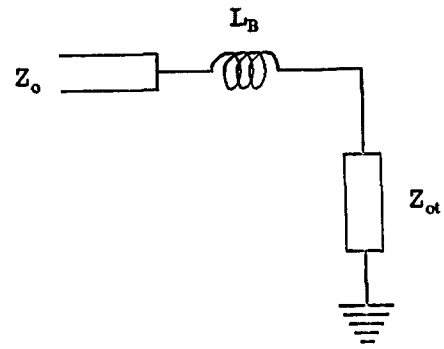


Figure 3.6 Equivalent circuit of inductive discontinuity

The termination impedance is the series combination of L_B and Z_{ot} and is $Z_t = Z_{ot} + L_B s$. The solder bump inductance is assumed to be the self inductance for simplicity and any mutual inductances are negligible. The far-end reflection coefficient is

$$\rho_t = \frac{\frac{L_B}{2Z_o}s}{1+\frac{L_B}{2Z_o}s} \quad . \tag{3-16}$$

Using the same input signal as described in equation 3-11 and 3-12 the far-end reflected signal found from equation 3-5 is

$$V_r(s) = \frac{V_o}{T_r}\left[\frac{1}{s}\left(\frac{1}{s+\frac{2Z_o}{L_B}}\right) - \frac{1}{s}\left(\frac{1}{s+\frac{2Z_o}{L_B}}\right)e^{-sT_r}\right] \quad . \tag{3-17}$$

In the time domain the reflected signal is

$$v_r(t) = \frac{V_o}{T_r}\frac{L_B}{2Z_o}\left[\left(1-e^{\frac{-2Z_o}{L_B}t}\right)u(t) - \left(1-e^{\frac{-2Z_o}{L_B}(t-T_r)}\right)u(t-T_r)\right] . \quad (3\text{-}18)$$

It is interesting to note that equations 3-14 and 3-18 have the same form; the differences are the sign and the constants: $Z_oC_B/2$ and $L_B/2Z_o$. The transmitted signal, $v(t)$, can now be written as

$$\begin{aligned} v(t) &= \frac{V_o}{T_r}\left(tu(t) - (t-T_r)u(t-T_r)\right) \\ &+ \frac{V_o}{T_r}\frac{L_B}{2Z_o}\left[\left(1-e^{\frac{-2Z_o}{L_B}t}\right)u(t) - \left(1-e^{\frac{-2Z_o}{L_B}(t-T_r)}\right)u(t-T_r)\right] . \end{aligned} \quad (3\text{-}19)$$

The reflected signal from the inductive component is additive; figure 3.7 shows the reflected and transmitted signals.

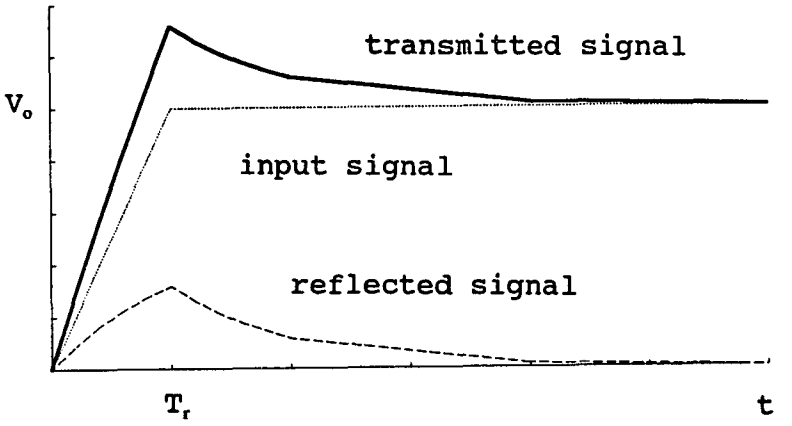


Figure 3.7 Graph of inductive discontinuity effect

3.6 Combined effects of resistive, capacitive, and inductive discontinuities

Using superposition the effects of resistive, capacitive, and inductive discontinuities can be determined separately then added together. The resulting equation, which algebraically combines equations 3-8, 3-15, and 3-18 is

$$\begin{aligned} v(t) = {} & \frac{V_o}{T_r}\left(1+\frac{R_B}{2Z_o}\right)\left(tu(t) - (t-T_r)u(t-T_r)\right) \\ & + \frac{V_o}{T_r}\frac{L_B}{2Z_o}\left[\left(1-e^{\frac{-2Z_o}{L_B}t}\right)u(t) - \left(1-e^{\frac{-2Z_o}{L_B}(t-T_r)}\right)u(t-T_r)\right] \\ & - \frac{V_o}{T_r}\frac{Z_oC_B}{2}\left[\left(1-e^{-\frac{2}{Z_oC_B}t}\right)u(t) - \left(1-e^{-\frac{2}{Z_oC_B}(t-T_r)}\right)u(t-T_r)\right] . \end{aligned} \tag{3-20}$$

The effects of the inductive and capacitive elements would negate each other if

$$\frac{Z_oC_B}{2} = \frac{L_B}{2Z_o} \quad . \tag{3-21}$$

Rearranging equation 3-21 to simplify the relation slightly yields

$$Z_o^2 = \frac{L_B}{C_B}$$

which is more easily recognizable as the characteristic impedance if it is written

$$Z_o = \sqrt{\frac{L_B}{C_B}} \quad . \tag{3-22}$$

Another method to determine the combined effects of the three elements (R_B, C_B, L_B) is to do an analysis of figure 3-1. This results in a very complicated second-order equation for the terminal impedance

$$Z_T = \frac{\frac{C_B L_B}{2} s^3 + C_B L_B (R_B + Z_O)\, s^2 + \left(\frac{C_B L_B}{2} (R_B + 2 Z_O) + 2 L_B \right) s + 2 (R_B + Z_O)}{C_B L_B s^2 + C_B (R_B + 2 Z_O)\, s + 2} . \quad (3\text{-}23)$$

The far-end reflection coefficient becomes third-order and is given by

$$\rho_t = \frac{\frac{C_B L_B}{2} s^3 + C_B L_B R_B s^2 + \left[\frac{C_B R_B}{2} (R_B + 2 Z_O) - C_B Z_O (R_B + 2 Z_O) + 2 L_B \right] s + 2 R_B}{\frac{C_B L_B}{2} s^3 + C_B L_B (R_B + 2 Z_O)\, s^2 + \left[\frac{C_B R_B}{2} (R_B + 2 Z_O) + C_B Z_O (R_B + 2 Z_O) + 2 L_B \right] s + 2 (R_B + 2 Z_O)} .$$

(3-24)

The equations for the reflected and transmitted signals were not pursued further.

3.7 Application of transmission line model

By applying the quantities calculated in chapter 2 to the relationships developed in the previous sections, the real impact of solder bumps can be quantified. For the following computations a value of 50 Ω will be used for the characteristic line impedance, Z_o. The resistive effect will be looked at first then the combined capacitive and inductive effects will be studied.

The calculated d.c. resistance of solder bumps varied between about 1 to 11 mΩ, increasing as the bump diameter decreased. The worst case impact would be for a 25 μm bump. Using equation 3-8, the reflection coefficient is only .00011, meaning .011% of the input signal will be additively reflected. Even considering the skin effect at high frequency, the coefficient of reflection is still only .02%. at 10 GHz.

The effect of inductance and capacitance on reflected/ transmitted signals will start by examining the relationship described in equation 3-23. To retain some simplicity in modeling and calculations only a single line transmission line will be studied. Using only the self inductance and capacitance, the impedance varies from 32Ω for a 25 μm bump to

36Ω for a 300 μm bump. This does not match the transmission line impedance, Z_o, meaning that the capacitive effect is not balanced with the inductive effect. The domineering effect can be determined by comparing the constants (magnitude and time) in equation 3-20. The capacitive effect will be more prominent when $C_B > L_B/Z_o^2$. Conversely, the inductive effect will dominate when $L_B > C_B Z_o^2$. For the case of a single transmission line where $C_B = 18\text{x}10^{-15}$F, $L_B = 22\text{x}10^{-12}$H, and Z_o = 50Ω, the capacitive effects are greater by a factor of two. Substituting these parameters into equation 3-20 and assuming a rise time of 100 psec, the transmitted signal only had a delay time of .23 psec and a voltage undershoot of 2.3 mV at 100 psec which was difficult to show graphically.

There are three cases that bear further examination: when capacitance is very dominant, when inductance is very dominant, and when each effect is equal (equation 3-21 is satisfied).

Case 1: Dominant capacitive effect

When the discontinuity approaches one of pure capacitance then the transmitted signal can be described by equation 3-15 and figure 3.5 instead of equation 3-20. The primary effects are a delay induced in the transmitted signal and a negative reflection. The magnitude of the delay and the reflection are both dependent on Z_o, C_B, and T_r. If $T_r/Z_oC_B > .8$ then the delay

time is (Menezes 1992)

$$\delta_t = \frac{1}{2} Z_o C_B \left(1 - .35 e^{.2 \frac{Z_o C_B}{T_r} - \frac{T_r}{Z_o C_B}}\right) . \qquad (3\text{-}25)$$

If $T_r/Z_oC_B \leq .8$ then the delay time is

$$\delta_t = \frac{1}{2} \ln\left[\frac{2 Z_o C_B}{T_r} \sinh\left(\frac{T_r}{C_B Z_o}\right)\right] . \qquad (3\text{-}26)$$

Basically if T_r/Z_oC_B is greater than 3 then δ_t is $.5Z_oC_B$ and if T_r/Z_oC_B is less than .1 then δ_t is $.34Z_oC_B$.

Case 2: Dominant inductive effect

For discontinuities that are primarily inductive the reflected signal is positive and thus causes a signal overshoot at the end of the signal rise time. The transmitted signal can be found using equation 3-18. If the rise time is large (slow) compared to the time constant ($L_B/2Z_o$) the inductive effect will be small in magnitude. So the range of inductive effect is bounded on one side. The reflection magnitude will be considered small if it less than .1% of the signal voltage yielding the following relationship

$$\frac{L_B}{2 T_r Z_o} \leq .001 . \qquad (3\text{-}27)$$

This equation shows the inductive effect will be negligible for rise times longer than $10L_B$ when $Z_o = 50\Omega$. As the rise

time decreases the magnitude of the reflection increases, leveling off at a magnitude equal to the incoming signal. If the self inductance of a 300 μm is used for L_B, the rise time must be less than .23 psec for noticeable inductive effects to occur.

Case 3: Equal capacitive and inductive effects

When the capacitive and inductive parameters satisfy equation 3-23 the result is a discontinuity that is transparent to signals. As noted in section 3-6 the terms of equation 3-20 cancel each other so the terminating signal matches the sent signal and no reflection occurs.

3.8 Concluding remarks

The calculated effect of solder bumps on transmission line signals was negligible. The resistive and inductive elements produced a positive reflection while the capacitive element produced a negative reflection. The resulting reflection caused a delay and an brief voltage undershoot; both were minimal. The delay induced on a 1 volt, 100 psec rise time signal was only .23 psec and the voltage undershoot was 2.3 mV. Solder bumps will have a noticeable affect on transmission line properties when the rise time approaches 10 psec.

CHAPTER 4

RELIABILITY MODELS FOR SOLDER BUMPS

4.1 Introduction

The reliability of solder joints is a major area of concern and research among companies using surface mount technology (SMT). Well over 400 papers on this subject have been published to date and there still remains unsolved problems and unmet challenges. Although the failure mechanism has been simply described as "inhomogeneous deformation of the solder microstructure resulting in inhomogeneous recrystallization and softening and thus joint failure" (Morris et al. 1991), quantifying this has proved to be complex. For simple single phase materials there isn't a reliable, predictable theory for thermal fatigue under creep conditions (Morris et al. 1991). Solder is a binary (sometimes ternary) phase material with a low melting point: 183°C for eutectic solder and 312°C for 95Pb/5Sn. The mechanical properties (modulus of elasticity, yield strength, Poisson's ratio) are not only functions of composition and temperature but also microstructure and load application rate. The reliability is complicated by the fact that at room temperature even the highest melting Pb-Sn solder is at $.5T_M$: half its melting point in absolute degrees. This

means that creep characteristics will be dominant life factor at all typical operating temperatures. The fatigue life of solder is a function of microstructure, composition, environment, stress and strain amplitudes, mean stress and strain levels, loading rates and frequency, hold levels and duration, and temperature. Successful reliability prediction/ modeling must take these factors into account or at least the most significant ones. This chapter examines and compares a number of reliability models, discusses factors that influence reliability, and discusses the stress-strain calculations used in lifetime predictions.

4.2 Synopsis of models

There are two basic types of models used to predict reliability: the empirical and the mechanistic model. The empirical model generally uses a single measurable physical quantity to predict lifetimes. The Coffin-Manson relation is the most common of these models. Because it is based on one phenomena and solder reliability has many influencing factors, the Coffin-Manson model has been modified by many to include various effects. Other empirical models that will be discussed in this section include the plane strain, a dislocation pile-up, and a probabilistic method. Their chief advantage is their simplicity. Their disadvantage arises during application; several significant damage mechanisms or factors may not be accounted for and a very conservative lifetime may be determined.

The mechanistic models are based on mathematical relationships of damage mechanisms. They are generally quite sophisticated and because the actual mechanisms are used, may be applicable to a specific solder. The advantages are that one can see how to improve fatigue life and the model can be quite accurate for a variety of geometries. The disadvantage comes from their complexity, composition sensitive application, and the need for many time-dependent material properties.

4.3 Relationship of fatigue life to reliability

The majority of solder bump reliability models calculate fatigue lifetime in cycles rather than actual reliability. The two can be easily related once their definitions are understood. Reliability is defined as the probability that a component will be operating after a time t, defined by (Henley and Kumamoto 1981)

$$R(t) \equiv P(T \geq t) \tag{4-1}$$

where T is the time of failure which is a continuous random variable. There is also a cumulative distribution function, $F(t)$, of the time of failure, T, which is defined as

$$F(t) \equiv P(T \leq t) \tag{4-2}$$

and since T is continuous,

$$F(t) \equiv \int_0^t f(\tau)\, d\tau \tag{4-3}$$

where $f(t)$ is a probability density function of T. The cumulative distribution function, $F(T)$, is the probability that the component will fail by time t. It is easy to see that the reliability and distribution function of the time of failure, T, are related by

$$R(t) = 1 - F(t) \ . \tag{4-4}$$

The other common reliability parameter is failure rate. The definition of failure rate over a given interval of time

t_1, t_2] is the number of failures during the interval divided by the time interval and the number of survivors expressed as

$$FR(t_1, t_2) = \left[\frac{R(t_1) - R(t_2)}{R(t_1)}\right] \cdot \left[\frac{1}{t_2 - t_1}\right] \quad . \tag{4-5}$$

There are specific forms of probability density functions of time of failure, $f(t)$, such as Weibull, exponential, binomial, etc. For solder bumps the failure was found to be wear-out so it is described by a Weibull distribution (Englemaier 1989). The simple exponential form of the probability density function of T can be written as

$$f(t) = h_i e^{-h_i t} \tag{4-6}$$

where h_i is the inverse of the mean time to failure (MTTF). The mean time to failure can be obtained from the mean fatigue lifetime, N_f, and the number of cycles per unit time, n_c, usually hours. The simple conversion can be done using

$$MTTF = \frac{N_f}{n_c} \quad . \tag{4-7}$$

Substituting this expression into equation 4-6 then using equations 4-3 and 4-4 and simplifying the reliability can be expressed in terms of fatigue lifetime as

$$R(t) = e^{-\frac{n_c}{N_f} t} \quad . \tag{4-8}$$

The mean time to failure for a 150 μm solder bump of 95Pb-5Sn was found to be 355,000 hours (Norris and Landzberg 1969); the failure rate was predicted to be 10^{-7}% / 1000 hours. For this MTTF the reliability for one year would be .9756 for one solder bump. Assuming the chip has a bump in each corner the chip reliability is only .9060. A variety of methods could be employed to improve this quantity as described in chapter 5. By stacking solder bumps the reliability could be improved to .9994 for the individual bump and .9975 for the chip.

4.4 Empirical models

The most commonly used empirical model for predicting mean fatigue life is the Coffin-Manson equation, shown below, which relates plastic strain to the number of cycles to failure.

$$N_f = \frac{1}{2}\left[\frac{\Delta \epsilon_p}{2\epsilon_f}\right]^{\frac{1}{c}} \qquad (4\text{-}9)$$

where $\Delta\epsilon_p$ is the cyclically applied plastic strain range,

N_f is the cyclic shear mean fatigue life in cycles,

ϵ_f is the fatigue ductility coefficient (.325 for eutectic solder, and

c is the fatigue ductility exponent (see equation 4-11). This equation has been used to predict solder lifetimes but has limited applications. The Coffin-Manson relation assumes that the plastic component of strain is much greater than the elastic component and is best applied to low cycle fatigue caused by plastic flow. The earliest fatigue life equation for solder bumps was developed by Goldmann (1969) and had a modified Coffin-Manson form. Solder bump optimization was a matter of maximizing compliance and ultimate strength. The mean fatigue lifetime in cycles, N_f, was found to be (Goldmann 1969)

$$N_f = K_T\left[\left(\frac{\tau_U \pi r_f^2}{A}\right)\left(\frac{h^{1+\beta}}{V}\right)\right]^{\frac{m}{\beta}}\left(\frac{1}{\delta}\right)^m \qquad (4\text{-}10)$$

where K_T is a constant ($\approx$ 13) dependent on testing cycle

parameters (strain rate, dwell times and maximum temperature),

τ_U is the ultimate shear strength (3 - 5.87 kpsi),

A and β are constants (see equation 4-30),

r_f is the radius where failure occurs and is either r_c or r_s (see section 2.1),

h is the bump height (see equation 2-2),

V is the bump volume (see equation 2-3),

δ is the joint shear deformation (see equation 4-28), and m is the Coffin-Manson exponent (1.9 for Pb-Sn solder). This relation was not correlated with actual fatigue data but a torque test was developed to provide accelerated test data on solder bumps.

To provide better accuracy, numerous studies have developed factors to modify the Coffin-Manson equation. One of the first modifications for leadless and leaded eutectic lead/tin solder attachments was developed by Englemaier (1989). The following expression was derived for the fatigue ductility exponent (Englemaier 1986)

$$c = -.442 - 6\times10^{-4}\, T_{sj} + 1.74\times10^{-2} \ln\left(1+\frac{360}{t_d}\right) \qquad (4\text{-}11)$$

where T_{sj} is the mean cyclic solder joint temperature, and

t_d is the half-cycle dwell time.

The half-cycle dwell time is the amount of time the solder

joint is at the maximum temperature for thermal cycling or maximum load for mechanical cycling. The chief modification to the Coffin-Manson equation was to account for a Weibull cumulative failure probability distribution function of lifetime cycles. Equations for cyclic strain range were also determined. The distribution is characterized by the following equation

$$N_f = N\left[\frac{-n\ln 2}{\ln[1-F(N)]}\right]^{\frac{1}{\beta}} \qquad (4\text{-}12)$$

where N_f is the design mean fatigue life in cycles,

N is the expected service life in cycles as determined by warranty, contract, or design standard,

n is the number of components,

$F(N)$ is the acceptable cumulative failure probability level after N cycles (a percentage), and

β is the Weibull shape parameter (about 4 for leadless solder attachments).

The reliability of leadless solder joints was found to be

$$N_f(x\%) = \left[\frac{.288h}{L_D \Delta\alpha\, \Delta T_e}\right]^2 \left[\ln\frac{[1-F(N)]}{\ln .99}\right]^{.5} \qquad (4\text{-}12)$$

where $N_f(x\%)$ is the predicted number of operating cycles at x% failure probability,

h is the solder joint height,

$\Delta\alpha$ is the CTE difference between the chip and substrate,

$2L_D$ is the max distance between solder joints, and

ΔT_e is the equivalent temperature range accounting for the temperature gradient due to component power dissipation and is quantified by $\Delta T_e = \frac{|\alpha_s \Delta T_s - \alpha_c \Delta T_c|}{\Delta \alpha}$.

This reliability ($N_f(x\%)$) is the number of cycles it takes to fail x% of the joints tested, e.g., $N_f(1\%)$ is the number of cycles needed to fail one out of one hundred specimens and $F(N)$ is .01. Note that $N_f(x\%)$ increases as x increases. While this equation is simple there are some restrictions. It is only valid for solder joints of 60Sn/40Pb or eutectic solder and where stress relaxation and the creep process are complete. Other applications would need further modification/ additional factors for equation 4-13.

Another supposed Coffin-Manson modification was developed by Norris and Landzberg (1969). In reality, their model provided factors for extrapolation from known data. Three effects were considered: frequency of cycling, max cycle temperature, and cycle temperature difference. To relate test data to hardware predictions the following equation was used (Norris and Landzberg 1969)

$$\frac{N_L}{N_P} = \left(\frac{f_L}{f_P}\right)^{\frac{1}{3}} \left(\frac{\Delta T_P}{\Delta T_L}\right)^2 \Phi\,(T_{\max}) \qquad (4\text{-}14)$$

where N_L is the lifetime found by experiment in cycles,

N_P is the predicted lifetime in cycles,

f is the frequency of cycling,

ΔT is the change in cycle temperature, and

$\Phi(T_{max})$ is a maximum temperature factor.

The subscript L refers to values used during testing while the subscript P refers to values for the prediction. The maximum temperature factor is given by

$$\Phi(T_{\max}) = \frac{N_f(T_{\max L})}{N_f(T_{\max P})}$$

where the lifetime data is taken from the Southern Research Institute (1960).

It was later discovered that experimental data for eutectic solder (63Sn/37Pb) was not continuous over a large total strain range, i.e., .3 to 3% (Cutiongco and Jeanette 1990). They developed the following piecewise Coffin-Manson relationships:

$\Delta\epsilon_p = 12.2\ N_f^{-.48}$ for $.07\% < \Delta\epsilon_p < .22\%$ $(.3\% < \Delta\epsilon_t < .5\%)$

$\Delta\epsilon_p = 114\ N_f^{-.72}$ for $.28\% < \Delta\epsilon_p < 2.55\%$ $(.6\% < \Delta\epsilon_t < 3\%)$

where $\Delta\epsilon_p$ is the plastic strain range, and

$\Delta\epsilon_t$ is the total strain range.

A slightly more sophisticated model was proposed by Darveaux and Banerji (1991). Their procedure involved the use of

finite element analysis (FEA) because they determined that stress relation is the primary factor during typical thermal cycle conditions. Lifetime prediction was a three step procedure. First, the assembly stiffness and the imposed strain per cycle was calculated with FEA. Next the stress-strain hysteresis loops for variations in the ramp rate, dwell time, and temperature range were determined. Lastly, the mean cycles to failure was found using the Coffin-Manson formula. The solder used in this study was 95Pb/5Sn and the results (predicted lifetime versus mean cycles to failure) correlated well with data from Norris and Landzberg (1969).

Probably one of the more sophisticated empirical models was developed by Lau (1992). The model describes thermal fatigue crack propagation using plane strain theory. It could be argued that it is a mechanistic model but since it is based on one phenomenon it fits the empirical definition best. Through the use of FEA, the J-integral and stress intensity factor around crack tips was calculated. The thermal fatigue life was then determined using Paris' law and factors from fatigue crack growth data. The overall procedure was straightforward. First, a FEA on the solder joint was performed. The J-integral was obtained from the FEA then the stress intensity factor, ΔK, was found using

$$\Delta K = \sqrt{\frac{E \Delta J}{(1-\nu^2)}} \qquad (4\text{-}15)$$

where E is the modulus of elasticity,

ΔJ is the J-integral range, and

ν is Poisson's ratio (typically .3).

Next, Paris' law, given in equation 4-15, was used to determine fatigue life from the stress intensity factor (Lau 1992).

$$\frac{da}{dN} = \gamma \Delta K^{\beta} \qquad (4\text{-}15)$$

Where a is the crack length,

N is the number of cycles to failure, and

β and γ are material constants.

Rearranging equation 4-16 and integrating over the initial and final crack length to solve for N yields

$$N = \int_{a_i}^{a_f} \frac{da}{\gamma \Delta K^{\beta}} \quad . \qquad (4\text{-}17)$$

Finally, the mean thermal fatigue life, N_f, was derived from the number of cycles to failure, N, by the simple expression $N_f = \lambda N$; λ was called an acceleration factor. Actually it is a scaling factor that accounts for temperature and loading frequency dependence of β and γ in equation 4-17. The expression for the acceleration factor is (Lau 1992)

$$\lambda = \left(\frac{f_o}{f_t}\right)^{\frac{1}{3}} \left(\frac{T_{tM}}{T_{oM}}\right)^2 \qquad (4\text{-}18)$$

where f_o is the cycling frequency of the design condition,

f_t is the cycling frequency of the test data,

T_{oM} is the max temperature of the design condition, and

T_{tM} is the max temperature of the test data.

This method was claimed to provide results comparable to test data but was only checked for eutectic Pb-Sn solder at one max temperature/cyclic frequency point.

A study by Guo et al. (1992) found that thermomechanical fatigue life prediction could by based on a dislocation pile-up model. Their work was prompted in part because there isn't a single relation to describe the number of cycles to failure versus plastic strain range. When the data is shown on a log-log plot there is a discontinuity at about the point where the elastic strain is equal to the plastic strain ($\Delta\epsilon_p$ = .22% to .28%, $\Delta\epsilon_t$ = .5% to .6%). The model recognized that fatigue is characterized by cyclic softening then grain boundary failure. The grain boundary failure was modeled as two adjacent layers of dislocation accumulation with opposite signs. The number of cycles to failure, N_f, was given as (Guo et al. 1992)

$$N_f = \frac{8\gamma}{(\Delta\sigma - 4\sqrt{3}\,\sigma_f)\,a\left[4\frac{h}{a}\log\left(\frac{8a}{h}\right) + \left(\frac{\Delta\sigma}{G}\right)^2 \pi(1-\nu^2)\right]} \qquad (4\text{-}19)$$

where γ is the surface energy,

$\Delta\sigma$ is the stress range (equal to $\sigma_{max} + |\sigma_{min}|$),

σ_f is the flow stress in tension,

a is the grain size,

h is the spacing between dislocation layers,

G is the shear modulus, and

ν is Poisson's ratio.

While this expression looks relatively simple, one must know the grain size (or assume a typical value), and be able to calculate the stress range, surface energy, and flow stress which requires FEA.

Finally, a model utilizing a purely probabilistic approach was proposed by Arjunan (1991). The goal was to establish a unified model that was general enough to cover a wide range of conditions yet simple enough for a reliability engineer to use. The failure rate of a solder joint was given by

$$\lambda_p = \lambda_b \cdot \pi_E \cdot \pi_Q \cdot \pi_C \cdot \pi_L \cdot \pi_K \cdot \pi_T \qquad (4\text{-}20)$$

where λ_p is the part failure rate, and

λ_b is the base failure rate of the most critical parameter and is the inverse of the mean cycles between failures (MCBF).

The π subscript terms are modifiers dependent on environment (π_E), quality (π_Q), complexity (π_C), learning (π_L), proportion (π_K), and temperature (π_T), respectively. The terms in equation 4-19 are patterned after MIL-HDBK-217 and values for

these modifiers can be found there. The reliability was determined by

$$P(x_c > c) = \exp\left[-\int_0^c r(c)\,dc\right] \qquad (4\text{-}21)$$

where x_c is the number of cycles to failure,

c is the critical number of cycles, and

r_c is defined in equation 4-22.

$$r(c) = \frac{f(c)}{1 - \int_0^c f(c)\,dc} \qquad (4\text{-}22)$$

Where $f(c)$ is the failure density function of cycles to failure which is dependent on solder material properties and joint geometry. This model was not correlated with test data. It was proposed as a general use model in an attempt to put some commonality into an extremely diverse situation.

4.5 Mechanistic models

Mechanistic models are typically more complex than empirical models. They usually involve complex stress calculations, detailed thermal analysis/profiles, and a computer program to perform calculations.

One of the chief factors in solder fatigue is the microstructural changes that occur during thermal cycling. Frost and Howard (1990) discussed the problems faced with modeling the microstructural changes that occur during service conditions and accelerated tests. While there are many interdependent factors and relations they cite two key relationships: one for rate of plastic deformation, and one for damage accumulation rate. The flowchart for their model is shown in figure 4.1. Microstructural changes are influenced by three mechanisms: precipitation, dissolution, and discontinuous coarsening. Depending on the composition, temperature, and thermal cycling frequency the solder alloy may change as the thermal cycle progresses. For alloys with less than 19% wt Sn the microstructure could be a single or double phase. Precipitation removes tin from the lead matrix which reduces strengthening due to the solid solution. But precipitation also increases a strengthening component similar to grain size strengthening. The net impact is dependent on

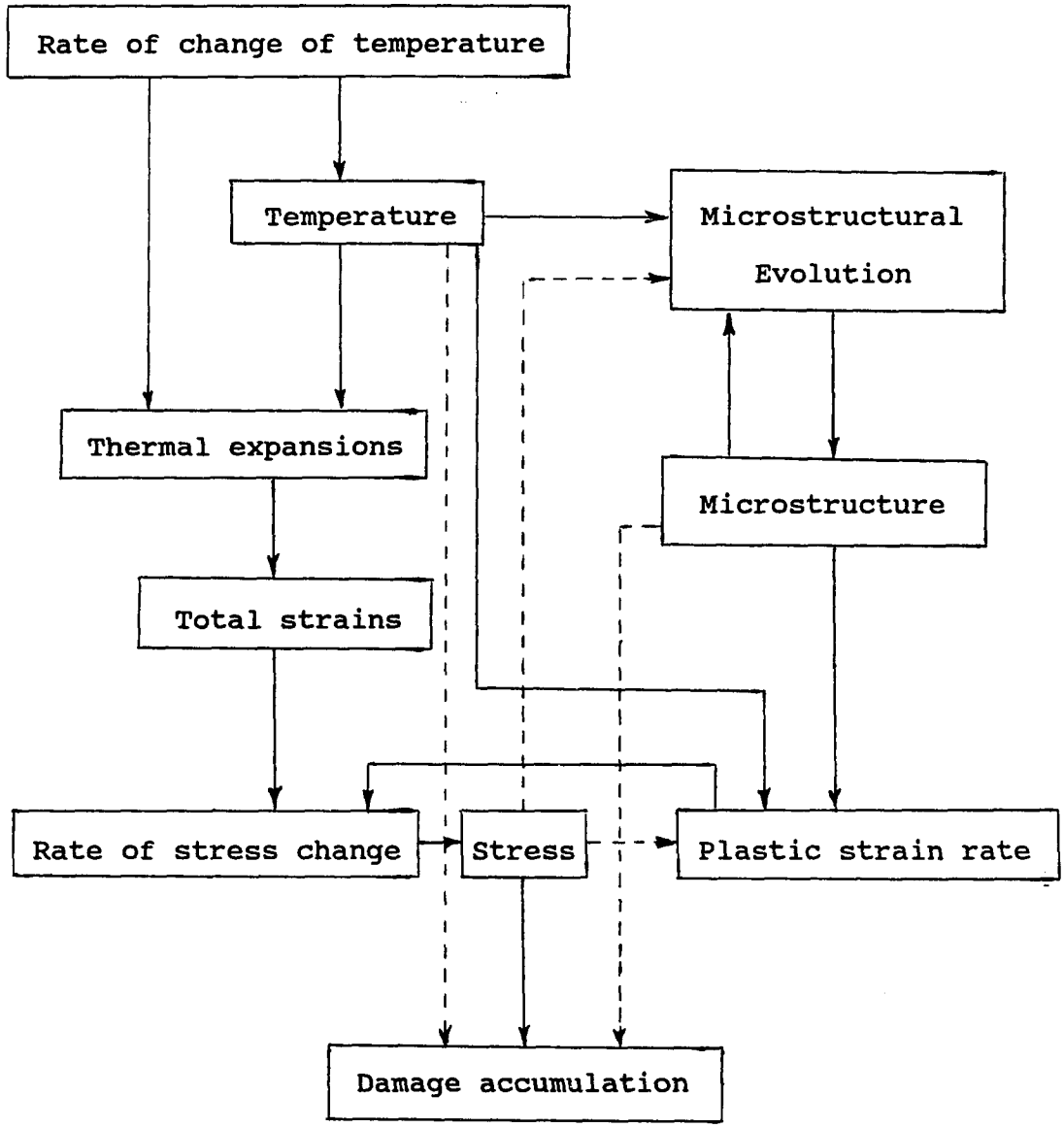


Figure 4-1. Solder joint lifetime calculation model (after Frost & Howard, 1990)

interlamellar spacing. Discontinuous coarsening is a factor when the temperature is below the solvus for extended intervals. While a complete model was never quantified the need for microstructural considerations was emphasized.

One of the simpler mechanistic models were presented by Subrahmanyan, Wilcox, and Li (1989). Calling it a damage integral approach, they postulated that the damage rate is a function of stress, temperature and environment and also that isothermal and thermomechanical fatigue may have the same kinetics. This has been supported by Tribula et al. (1989). Their stress calculations assume that the solder joint was in simple shear which is a good assumption for solder bumps. Their model was simplified by assuming that the crack growth rate was thermally activated and described by an elementary relation. The number of cycles to failure, N_f, was found from $N_f = Z / D$, where Z is the crack length integral characteristic of the initial flaw size and failure criterion, and D is the damage integral. The damage integral was further defined by

$$D = \int_0^{\frac{1}{\nu}} \tau_N^r \, \upsilon_o^* \exp\left(-\frac{Q_c}{RT}\right) dt \qquad (4\text{-}23)$$

where υ_o^* is the crack growth rate parameter,

t is time,

Q_c is the activation energy for crack growth,

R is the universal gas constant,

T is temperature,

τ_N is the nominal shear stress,

r is the crack growth exponent, and

ν is the loading frequency.

The crack growth rate parameter, v_o^*, is dependent on the composition and microstructure of the solder and the ambient environment. The nominal shear stress, τ_N, is equal to P/A_o, where P is the load and A_o is the undamaged area. The crack growth exponent, r, was assumed to be 2.3 because the stress intensity was low (less than .6 MPa$\sqrt{m}$). It was found that r could range between 5 and 9 for higher stress intensities. Although this model seems relatively simple it does contain many potential pitfalls. It was recognized as limited by the crack growth law and that both Q and v_o^* shift for temperature ranges above and below 100°C.

A deeply developed mechanistic model has been evolved by Wong and Helling. Their initial work discussed a creep-rupture model that was based on micromechanics and fracture mechanics (Wong, Helling, and Clark 1988). Reliability was predicted based on the following sequences of events. First, when stress is applied a crack immediately initiates at a microstructural inhomogeneity. Second, cavities nucleate around the small second-phase particles (Pb) on a matrix grain

boundary facet (triple point). Next, the cavities interlink and join the crack. The creep crack growth is therefore piecewise and continuous until elastic-plastic fracture occurs. Cavity growth rate was given as

$$\frac{d\rho}{dt} = \frac{\rho}{2} B\left[\frac{C^*}{I_n B x}\right]^{\frac{n}{n+1}} \qquad (4\text{-}24)$$

where ρ is the cavity radius,

t is time,

I_n is a dimensionless function of n determined for plane stress and plane strain conditions,

C^* is the strain energy rate line integral,

x is the distance from the crack tip, and

B and n are the temperature dependent coefficient and stress exponent in the steady-state power-law creep rate expression $\dot{\epsilon} = B\sigma^n$, respectively.

The time to failure in hours, t_f, was found to be

$$t_f = \left(\frac{n+1}{XY\epsilon_{ss}}\right)\left[a_f^{\frac{1}{n+1}} - a_o^{\frac{1}{n+1}}\right] \qquad (4\text{-}25)$$

where a_o is the initial crack size,

a_f is the critical (final) crack size,

X is a parameter dependent the steady-state creep exponent, the second-phase particle size, and the grain size,

Y is a parameter dependent on geometry and the dominant creep mechanism ($Y = (g/I_n)^{n/n+1}$ where g is a fracture mechanics

parameter determined by FEA (Goldman and Hutchinson 1975)), and ε_{ss} is the steady state creep rate. This model was developed for two-phase eutectic solders and was correlated with test data.

The next model developed was similar to the first and used several terms/factors previously generated. This mechanistic model was also comprised of four parts: a crack initiation model, a crack propagation model, a microstructural coarsening model, and solder deformation analysis during thermal cycling. Crack initiation was seen as a three part thermal process consisting of cavity embryo nucleation, cavity growth, and interlinkage. Cavity growth rate was a combination of creep and shrinkage due to sintering and was given by

$$\frac{d\rho}{dt} = \frac{\rho}{2}\varepsilon_{ss} - \frac{D_{gb}\,\delta_{Sn}\,\gamma_{Sn}\,\Omega}{\rho^2\,\lambda\,k\,T} \qquad (4\text{-}26)$$

where D_{gh} is the diffusion coefficient of tin in tin grain boundary,

δ_{Sn} is the tin boundary width,

γ_{Sn} is the specific surface free energy of tin interface and the tin grain boundary,

Ω is the atomic volume, and

λ is the average spacing between lead-rich particles. Crack propagation was modeled the same as previously. Microstructural coarsening was driven by the tin-rich grain

coarsening and was dependent on the bulk diffusion velocity of the lead solute atoms in the tin grain matrix. This coarsening rate is

$$G = K_3 \frac{D_1}{kT} \frac{1}{C_{Pb}} \frac{\delta U}{\delta x} \qquad (4\text{-}27)$$

where K_3 is the coarsening model coefficient,

D_1 is the diffusion coefficient of lead solute atoms in the tin matrix,

C_{Pb} is the concentration of solute atoms segregated at the boundary, and

$\delta U/\delta x$ is the sum of the plastic strain energy and the grain boundary energy gradients.

The solder joint deformation analysis was performed using FEA. The model showed good correlation with test data although the predictions were conservative.

The third model developed by Helling was very similar to the second model and was specific to solder bumps. A flow chart describing the model is shown in figure 4.2.

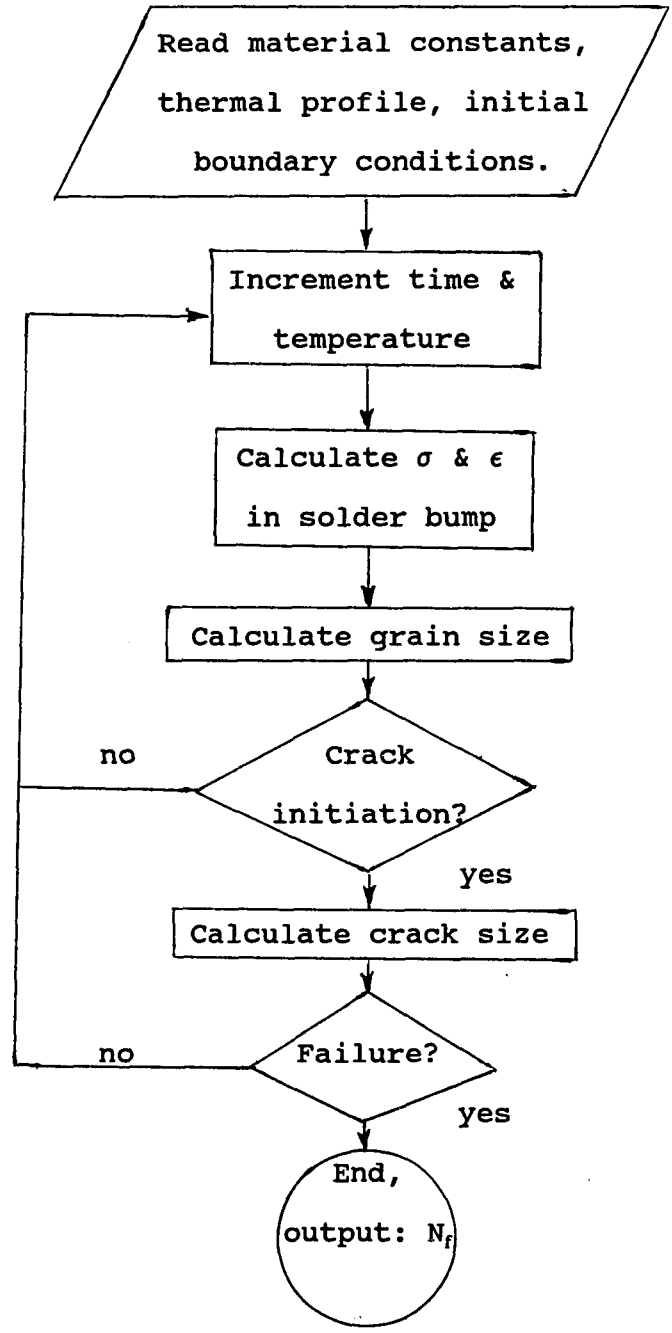


Figure 4-2. Mechanistic model flowchart (after Helling 1992)

4.6 Calculations for stress and strain and their influence on reliability

Most of the reliability models require calculation of the stress, strain, or deformation of the solder bumps. Solder bumps are typically loaded in shear caused by a difference in thermal growth between the chip and the substrate. Thermal growth is given by $\delta = L\ \alpha\ \Delta T$, where δ is the thermal growth, L is the length, α is the coefficient of thermal expansion (CTE), and ΔT is the change in temperature. For flip chips these terms are modified slightly. L is the distance between the bump and a neutral point, L_{dnp}, usually the center of the chip. The CTE term is the difference between the chip and substrate expansion coefficients. The ΔT is still the change in temperature of the system. If there is a temperature difference between the chip and substrate this may warrant another δ term. Using these modifications the shear displacement of a solder bump is

$$\delta = L_{dnp}\,\Delta\alpha\,\Delta T \quad . \tag{4-28}$$

The shear strain, γ, is determined by dividing the shear displacement by the solder bump height and is given by

$$\gamma = \frac{L_{dnp}}{h}\,\Delta\alpha\,\Delta T \quad . \tag{4-29}$$

The shear stress can be calculated using the formula

$$\tau = A\gamma^{\beta} \qquad (4\text{-}30)$$

as previously used in chapter 2. In the elastic range A is equal to G, the shear modulus, and $\beta = 1$. In the plastic range A and β are dependent on the strain rate and temperature (Kachanov 1971). This dependence is the reason why so many models rely on FEA to calculate the stress and strain in solder bumps.

From equations 4-9, 4-10, 4-19, and 4-23 it is evident that the stress and strain affect fatigue life and therefore reliability. The effect is inverse and exponential so decreasing the stress/strain increases reliability. Means to control reliability performance are apparent in equation 4-29. Reliability can be improved by increasing the solder bump height, decreasing the distance from the solder bump to the chip neutral point, decreasing the difference in CTE between the chip and substrate, and/or decreasing the change in temperature. The CTE is determined by the materials selected. The temperature change is a function of the power generated (electrical performance) and the cooling capacity (a combination of material properties and heat removal capability). The neutral point distance is determined by the chip size, IC layout rules, and heat distribution but could be hedged by not using the corner contact pads or making the interconnections through a centrally located array.

4.7 Concluding remarks

Reliability analysis can be a challenging and frustrating procedure. The number of models is excessive considering the simple end result and complexity involved in using most models. To obtain a better overview of the models the more important features and characteristics listed are listed and compared in table 4-1. The model is listed by author, distinguishing modeling characteristic, whether FEA is required, if it is solder specific and to which one, and if it was correlated to test data. Most of the models examined required the use of FEA to determine stress, strain or other factors. While providing (hopefully) more accurate results, this adds a degree of complexity to the model. Englemaier's model was the simplest and could provide results with a hand held calculator.

The packaging engineer has some control over the reliability performance as discussed in section 4-6. The next chapter present methods to improve reliability.

AUTHOR	MODEL TYPE	FEA	SOLDER SPECIFIC	CORRELATED WITH DATA	COMMENTS
Englemaier	Coffin-Manson	no	yes	yes	60Sn/40Pb
Norris & Landzberg	Coffin-Manson	no	no	yes	
Darveaux & Banerji	Coffin-Manson	yes	yes	yes	95Pb/5Sn
Lau	plane strain	yes	no	yes	60Sn/40Pb
Guo et al	dislocation	unknown	yes	yes	63Sn/37Pb
Arjunan	probabilistic	no	no	no	proposal
Subrahmanyan et al	damage integral	unknown	no	yes	60Sn/40Pb
Wong & Helling	fracture mechanics	yes	yes	yes	eutectic
Frost & Howard	microstructural	unknown	no	no	

Table 4-1. Summary of lifetime prediction models

CHAPTER 5

SOLDER BUMP RELIABILITY IMPROVEMENT METHODS

5.1 Introduction

The thrust to improve the fatigue life of solder bumps is driven by two factors: improved reliability and increasing chip size. Reliability improvements extend the service life of the component/system and thus benefit its overall quality. The reliability of solder bumps is a decreasing function of the distance from the chip center. As reliability is improved this distance may be increased keeping pace with the current trend in ICs.

This chapter reviews published methods of reliability improvement, examines some potential means for improvement, and discusses impacts on electrical characteristics. All improvements can be classified by the means used to gain reliability. The improvement will be separated into the following categories: thermal, structural, microstructural, process and environmental.

5.2 Thermal improvements

Since solder bump fatigue life is primarily driven by thermal expansion mismatch between the chip and the substrate there has been much research and effort devoted to this problem. One of the basic rules in package design is to strive for a coefficient of thermal expansion (CTE) match between the chip and substrate. This has been a challenge because silicon has a relatively low CTE ($2.4 \times 10^{-6}/°C$) compared to substrate materials. Some of the best matches can be attained by using SiC (CTE = $3.7 \times 10^{-6}/°C$), cordierite (CTE = $3.3 \times 10^{-6}/°C$), or glass-ceramic (CTE $\approx 3.7 \times 10^{-6}/°C$) (Tummala and Rymaszewski 1989). The ideal solution is to find/ develop/ use materials with a CTE of zero. Regardless of how well the chip and substrate CTEs match, thermal fatigue in solder will continue to exist because of four factors (Englemaier 1989).

1) Material variations produce ranges of CTE.

2) Transient cyclic strains still exist.

3) A CTE mismatch exists between the solder ($\approx 25 \times 10^{-6}$ $/°C$) and the chip/substrate.

4) There is a CTE mismatch between the two phases within the solder. The lead rich phase has a CTE $\approx 15 \times 10^{-6}/°C$ while the tin rich CTE is $\approx 21 \times 10^{-6}/°C$.

There will also be stress/strain induced in the solder bumps due to a temperature gradient from the chip to substrate.

5.3 Structural improvements

Structural improvements to solder bump interconnections can be characterized as methods of altering the joint compliancy. The temperature profile and CTE of the chip and substrate dictate the amount of displacement the solder bump will experience. The shear stress in the bump is a function of this displacement and the bump rigidity. The classic spherical bump shown in figure 2.1 is fairly rigid resulting in high shear stress.

One concept used to reduce stress is to form the solder joint into a column. This has been achieved in two ways: by stacking the bumps as shown in figure 5.1, and by controlling the distance between the chip and substrate to form a hyperboloid, shown in figure 5.2. The stacked bumps are made using a polyimide film with bump-limiting metal pads in between layers to form the stack. One proposed refinement to this concept was the alteration of the top solder bump from 300 μm to 50 μm (Sasaki et al. 1987). Along with a reduction in shear strain there was also a reduction in the joint capacitance. The capacitance decrease was realized because the electric field tended to concentrate at the chip side pad when smaller bumps were used. Tests performed on chips interconnected with double-stacked bumps showed a fatigue

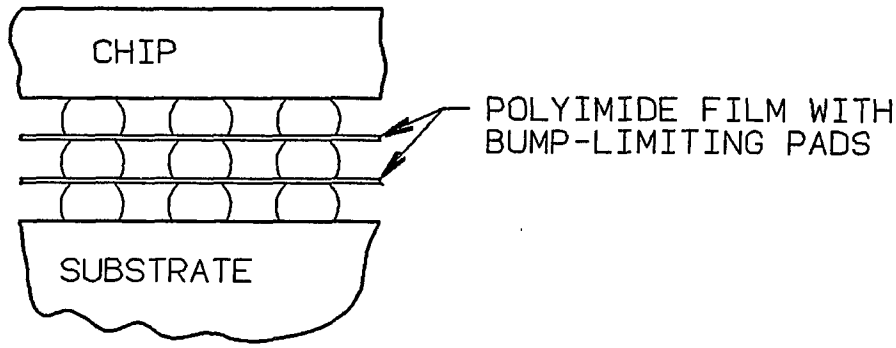


Figure 5.1 Stacked solder bumps.

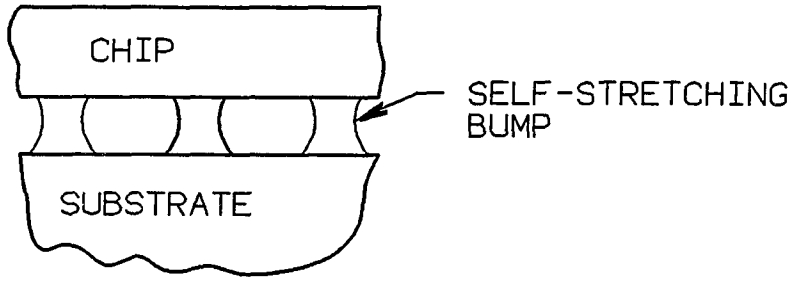


Figure 5.2 Self-stretching solder bump.

lifetime improvement of 60 times over single bumps for a 20 x 20 mm chip with 300 μm bumps (Matsui et al. 1987).

The second method of structural enhancement is achieved by encapsulation. Encapsulation has been done with polymers and epoxy resins. Injecting a material between the chip and substrate and around the solder bumps imposes its own set of problems and requirements. In order to realize a gain in reliability the following capsulent properties are considered crucial (Suryanarayana et al. 1991).

1. Must be free of volatiles which cause voids.
2. CTE should closely match the solder bump CTE.
3. High glass transition temperature (T_g).
4. Low temperature curing.
5. Low viscosity.
6. Low alpha activity (for memory applications).
7. High modulus and flexural strength.
8. Low ionic impurity levels
9. Chemically resistant to humidity and common organic solvents.
10. Good adhesion to packaging materials.
11. Small filler size.

The reliability improvement from encapsulation is optimized when the CTE is matched and the modulus is high providing a mechanical reinforcement of the bumps. In addition, complete

coverage, i.e., no voids, was found to be critical. Fatigue life improvements exceeding 40 times were noted during accelerated testing (Suryanarayana et al. 1991).

While the improvement in reliability is significant there are some inherent disadvantages. They are an increased cost from an additional process, materials, assembly times, inability to inspect product, and loss of reworkability. This concept is covered by two patent claims.

A third means of improving reliability is to overcoat the solder bumps. IBM used a polyamide-imide copolymer that enhanced lifetime by a factor of more than two. The improvement is believed to result from mechanical reinforcement of the bump (Howard 1982). The advantage gain is significantly less than the two preceding methods and the same could be said about cost.

5.4 Microstructural improvements

The reliability of solder bumps can also be improved by altering the solder microstructure. Microstructural changes may impact the coarsening mechanism, crack initiation mechanism and/or the crack growth rate and can be realized by changing the composition of manufacturing process.

IBM began using a 50% In-Pb alloy instead of the standard lead-tin and attained a factor of three improvement in reliability. Concerns about cost, corrosion and intermetallic formation lead to a study on reliability versus indium content (Goldmann et al. 1977; Howard 1982). It was noted that for 5% In-Pb the improvement was more than double, corrosion was almost non-existent for alloys with less than 20% In, and intermetallics were reduced with low In alloys.

Hughes Aircraft has recently disclosed that a solder alloy with improved fatigue life has been developed and is available through a vendor (Hughes 1993). The exact nature of these improvements has not been disclosed but based on research that has been published the alloy must have improved through microstructural means. When developing a mechanistic model for failure prediction it was noted that "By proper alloying of the solder, it may be possible to ... inhibit crack

initiation." (Wong and Helling 1990)

Part of the crack initiation process is grain coarsening. One potential means of retarding coarsening is to develop a solder with a homogeneous microstructure i.e., totally lamellar structure or minimal grain boundaries. This could be accomplished through a process change, a change in the cooling rate following reflow, or through the slight addition of a third element. A study on the impact of cooling rates on solder joint fatigue life was done by Mei and Morris (1992). They found that slowly cooled solder had about half the life of quench-solidified solder. The furnace cooled solder had a microstructure of highly lamella / large colony appearance. The quenched solder had a very fine spaced lamellae with almost indistinguishable colony boundaries. The lamella/ colony structure is inhomogeneous resulting in rapid coarsening under load. The exact reason for the reliability improvement was uncertain but two theories were offered. One is that the deformation mechanisms are "better" for fine grain size solder. The other is the homogeneity of the quenched solder delays coarsening which delays crack initiation and growth.

Crack growth rate is a function of the creep in the tin-rich matrix of eutectic solder (Wong and Helling 1990). Again, a

different alloy may retard the crack growth rate by being creep resistant. By focusing on the single phenomenon of creep a better solder may be developed without doing extensive testing.

In addition to enhancements due to solder content, the metallization thickness of the pads and solder joint positioning on the pads can influence reliability (Nagesh 1982; Capillo 1990). While some improvement may be realized, this situation can be classified as an optimization. The improved reliability is believed to be a result of reduced intermetallic content, attained by controlling the copper layer of the Cr-Cu-Au pad metallization.

5.5 Environmental affects

A study by Lodge and Pedder (1990) examined the effect of packaging, specifically hermeticity, on solder bump fatigue life. The fatigue life improvement realized by sealing the flip-chip devices in dry nitrogen was a factor of roughly three. Actual data showed non-hermetic failures were significant at 1500 cycles while not one hermetically sealed chip experienced a failed bond at 2000 cycles. They believed the cause was due to the absence of oxygen at the crack site. Without oxygen the crack can heal when the deformation cycle is reversed prolonging the fatigue life. When oxygen is present the crack surface forms an oxide film so healing is inhibited. They also noted that two methods believed to be structural improvements, coating and encapsulation as described in section 5-3, may be partially due to the restriction of oxygen at the solder surface. This does seem logical and might warrant further investigation.

5.6 Electrical impact of improvements

The electrical properties of single, truncated-sphere shaped solder bumps were developed in chapter 2. Many of the reliability improvements discussed here have an impact on the electrical properties.

Stacking solder bumps greatly improves the fatigue lifetime but the resistance and inductance will also increase. The d.c. resistance change still won't be enough (55 mΩ maximum for five layers) to warrant concern but the a.c. resistance will increase to 400 mΩ at 100 GHz. The inductance will also increase but non-linearly since the self and mutual inductance is non-linear. The self capacitance will increase but the total capacitance was claimed to decrease (Sasaki, Kishimoto, and Matsui 1987) so this may improve the transmission line performance.

Encapsulation of the chip/solder bumps changes the dielectric constant of the material between the chip and substrate by the relative dielectric constant of the encapsulant. This will affect cross-talk between the chip and substrate and increase the solder bump mutual capacitance. Coating will have a similar affect but to a lesser degree.

Changing the composition of the solder will change the solder bump resistance. This depends on the resistivity change and will likely be minor. Altering the metallization thickness will have a negligible affect the on the resistance. Hermetically sealing the chip will not affect the electrical performance.

5.7 Concluding remarks

A number of different methods have been developed/proposed to improve the fatigue lifetime of solder bump joints used for flip chip mounting. The methods discussed in this chapter are summarized in table 5.1. Some of these methods could be combined to achieve even greater lifetime improvement (e.g. stacking bumps and hermetically sealing). However, one could not combine them all to create a "super" solder joint because some of the mechanisms are identical/overlapping. The improvement benefits and possible electrical performance penalty should be considered using a total performance relation as described in equation 1-1.

METHOD	FATIGUE LIFETIME IMPROVEMENT FACTOR
Stacking bumps	≈ 60 (for two layers)
Self-stretching bumps	unknown
coating	2 - 4
encapsulation	≈ 40
microstructural/composition	1.5 - 11
metallization thickness	≈ 2
hermetic seal	≈ 2.7

Table 5.1 Summary of fatigue lifetime improvement methods

CHAPTER 6

CONCLUSION

6.1 Summary

The electrical properties of solder bumps were found to be small in magnitude. The d.c. resistance was less than 11 mΩ for a 25 μm bump; the a.c. resistance was 20 mΩ at 10 GHz. The induction calculations agreed well with published measurements and were in the 2-18 pH range.

The effect of solder bumps on single transmission line properties was found to be negligible. This was based on a signal with a rise time of 100 psec. However, as clock speed increases and rise time decreases to 10 psec, solder bumps will become noticeable as an intermediate discontinuity. Solder bumps were found to have a single transmission line impedance of about 34 Ω.

Solder bump reliability is a complicated matter and the models examined reflected this complexity. This is because solder properties are dependent on composition, microstructure, temperature, load rate range, and frequency, hold time and duration, and environment. The simple Coffin-Manson relation is adequate for first-order approximations but a mechanistic

model would be better for more accurate results. The package engineer has some control on reliability through certain design parameters such as bump dimensions and material selection.

6.2 Suggestions for future research

Using solder as a structural material presents many complex problems and challenges. Most of the lifetime prediction models were developed for a specific solder composition only. Data for different solder needs to be generated and published so these models can be more widely used. Methods to improve solder fatigue lifetime are another area worth exploration.

There is very little data available on the electrical properties of solder bumps, especially capacitance. It would be beneficial to experimentally examine the transmission line characteristics as a function of rise time. The effects of lossy transmission line properties may also prove interesting. The cost performance of solder bumps has not been explored/ published in any great detail; this knowledge is needed for system performance analysis.

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