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# ACTIVE MICROWAVE ARRAYS FOR MEDICAL HYPERTHERMIA: DEVICE SELECTION, CHARACTERIZATION AND IMPLEMENTATION OF THEIR DRIVE CIRCUITS

by

Michael James Hill

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NOVEMBER 20, 1996

Date

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## 2. ABSTRACT

Significant progress toward a functional 73 element, 730 watt, active microwave phased array has been made. This array, designed for medical hyperthermia applications, has significant size restrictions leading to a novel space conscious design. Unlike other hyperthermia devices, each array element is designed to have full 360° phase control with better than 1° resolution. Full amplitude control, with 10 bit amplitude resolution is implemented. The array is designed to operate in the 2.45 GHz ISM band. Measured operational data is presented and is compared to simulations performed with Compact Software's Microwave Harmonica®.

A sophisticated control system for the array has been designed, built and tested. The system provides 160 computer controlled 10 bit analog control lines to drive the array. Sampling of various system parameters is made possible through the use of a 96 channel, 12 bit analog to digital converter system. This system provides 4 mV resolution and a 440 Hz sampling rate for each of the 96 measurement channels.

## 3. INTRODUCTION

Microwave phased arrays have been used for many years in radar systems. Typically these systems are large and output very high powers. Due to their size and high expense, microwave phased arrays have not had many non-military applications. With the development of Monolithic Microwave Integrated Circuits (MMIC's) it is now possible to produce lower power, small drive modules for use in phased arrays. This opens up the possibility of using phased arrays for many applications that were previously considered unfeasible. Specifically there is a current need in the medical field for controlled hypothermia devices. These devices should be able to heat a specified volume of tissue below the skin by focusing microwaves into that tissue.

A microwave hyperthermia device has several overall system requirements. First the footprint of the device must be small enough to be placed on a patient -- no larger than 8" by 8". Second, the device must be able to output enough focused power to heat the tissue to a desired temperature in only a few seconds. Third, the device must be able to scan the focused 'hot spot' without physically moving the device. These system requirements have led to some more specific electrical requirements, which will be discussed in more detail in section 9.

Typically a phased array uses a number of elements to produce a focused main beam. From basic antenna theory [1] it is known that these arrays often have significant side lobes. For this hyperthermia application it is critical that any side lobes be minimized because these side lobes could

produce undesired heating in the patient. An algorithm for determining the proper magnitude and phase for each array element which minimizes the resulting sidelobes and thus any undesired heating, has been developed [2]. This algorithm leads to the requirement that each element must have a fully adjustable phase (360°) and magnitude. This algorithm and other work by Dr. Richards has also led to the desired number of array elements and the estimated power each element must be capable of producing. Thus it is known that the desired hyperthermia phased array will consist of 73 elements, each capable of producing approximately 10 watts of RF power.

In order for the tissue to be easily heated it must be highly absorptive at the operating frequency of the array. Additionally it is desired that the device operate in an Industrial, Scientific and Medical (ISM) band allocated by the Federal Communications Commission (FCC). Water, which is in high concentration in tissue, is highly lossy above 2 GHz, and 2.45 GHz is the center of an ISM band. Additionally with 73 elements it was determined that 2.45 GHz would provide an adequately small focused hot spot. Thus 2.45 GHz was selected as the operating frequency for the array.

Physically the array system is designed as two 'boxes'. One, a fixed 19" rack style case, contains the control system and power supplies for the array. The other 'box' is the *array head* which houses all the microwave circuitry and the actual patch antenna array.

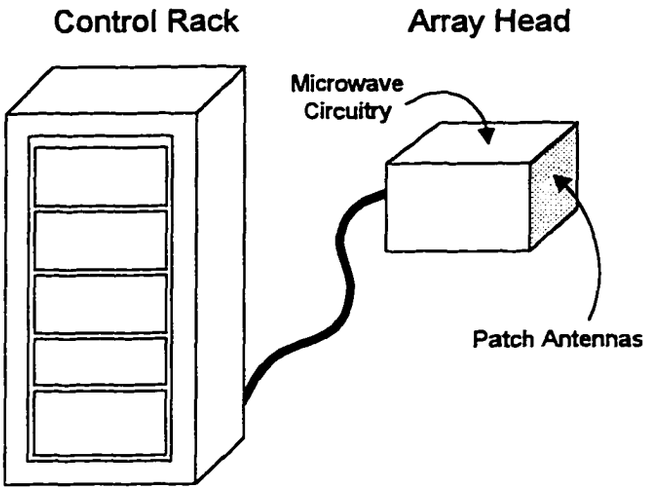



**Figure 3.1: Hyperthermia system**

The locations of the antenna elements on the array head places further requirements on the drive circuitry. A microstrip patch antenna design was selected, resulting in a planar 2 dimensional array of 73 elements. The operating frequency and other factors [2] lead to the following spacing requirements (see Figure 3.2): the center to center width in the X direction of the antenna patch is 0.719" and the vertical center to center width in the Y direction is 0.62" Although there is no electrical issue restricting the depth of the device, it is desired to keep it as small as possible. These requirements place a tight limit on the volume of space the drive circuitry behind each array patch can occupy.

This project has led to the development of all the main subsystems of this hyperthermia system: the control system, power splitters, phase shifters, preamplifiers and amplifiers. These subsystems have been designed to meet the stringent volume and periodicity requirements as previously discussed. Testing to verify proper operation of each subsystem has been performed.

Data will be presented illustrating the operating characteristics of each component.

In the next chapter, the design choices, which have placed further restrictions on the individual subsystems, will be considered. Following that, the design, development and testing of the phase shifters, preamplifier and power amplifier will be addressed. Finally, the design and development of the circuitry used to control the array will be discussed.

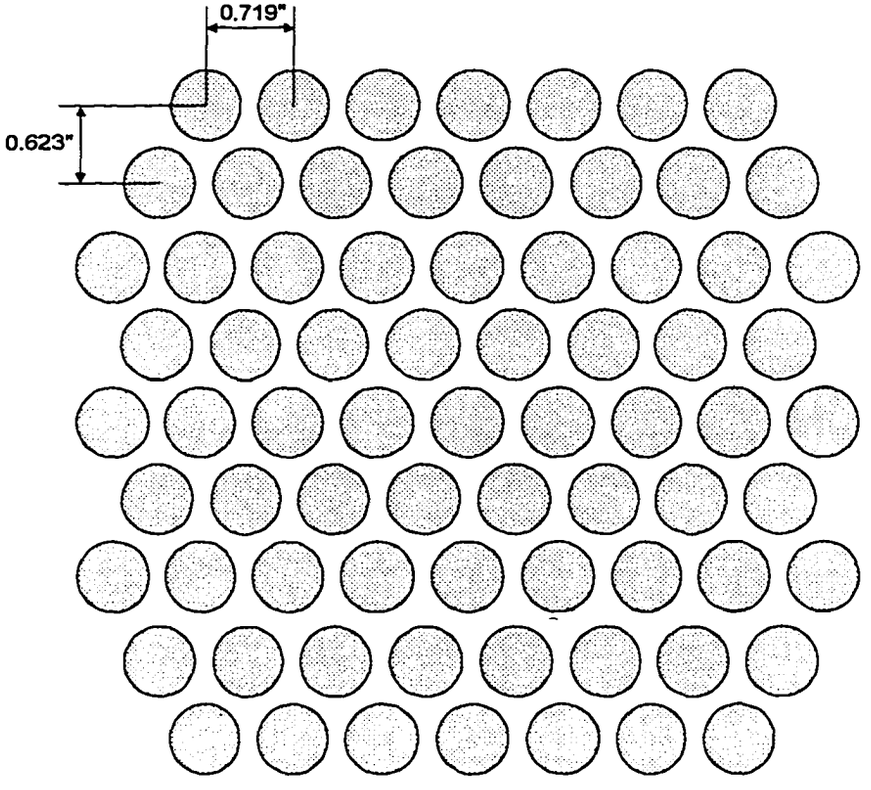



**Figure 3.2: Antenna array**

# 4. DEVELOPMENT

The first step in designing the drive circuitry was planning the basic topology of the system. The basic elements of the drive circuitry are the oscillator, amplifiers, phase shifters and power splitters. Because each element must be phased with reference to the other elements, it is desirable to have only one master oscillator. Once this choice was made, there were several options. One uses a single high power source to drive all the channels (one channel represents one radiating element). Arrays with this topology are often referred to as *passive arrays* [3]. In our case, the output of this single high power source would be divided 73 ways, and sent to the phase shifters and attenuators of each channel (see Figure 4.1). This method would require high-power power splitters, phase shifters, and, in order to control the amplitude of each channel, adjustable attenuators. Given the space requirements and the fact that more power handling capability typically means larger devices, this topology was not selected.

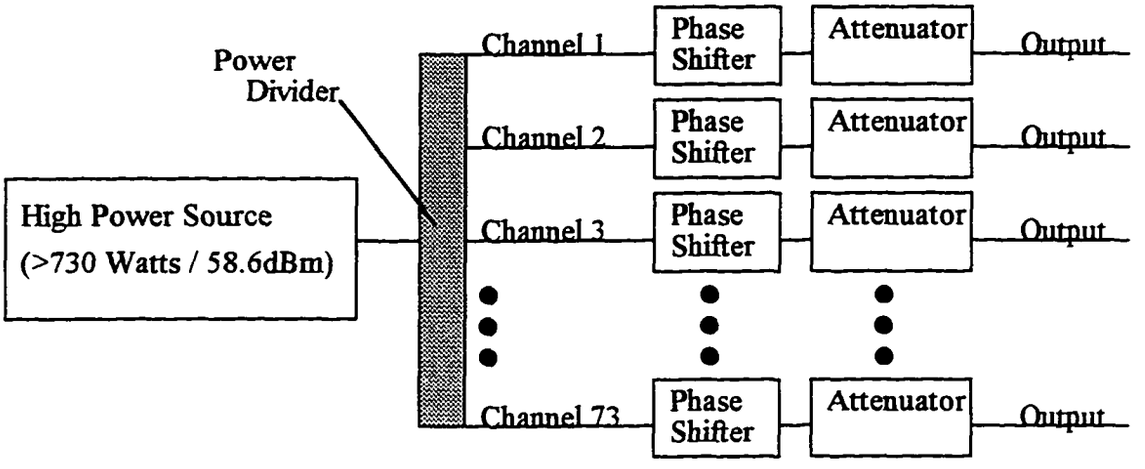



**Figure 4.1: A passive phased array**

Another option uses one low power oscillator. The output of this oscillator is split 73 ways, and directed to an amplifier, phase shifter and attenuator for each channel. In this topology each element of the array has its own amplifier and is thus often referred to as an *active array.* In an active array it is possible to place the phase shifter and attenuator before the power amplifier, thus allowing one to use lower power, smaller devices. Additionally by designing the amplifier as a variable gain amplifier, one can vary the overall output power without the need of a real estate expensive attenuator. With these thoughts in mind the initial topology, shown in Figure 4.2, was chosen.

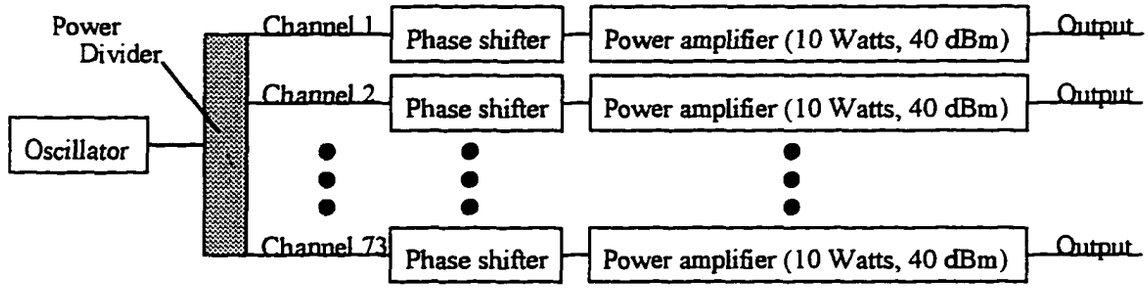



**Figure 4.2: An active phased array - our final topology**

In order to accurately steer the focus of the emitted RF power, the magnitude and phase at the output of the power amplifier must be controllable. Due to phase shifts introduced by each power amplifier, it is not sufficient to know the phase at the output of the phase shifter. Each channel will have its own additional characteristic phase shift relative to the oscillator. This is due to non-uniform transmission lengths between the oscillator and the

channels, and to component variations across the channels. There are two ways to account for these variations and accurately determine the phase and magnitude at the output. The most accurate is to sample the signal that reaches the antenna. If this sample were taken from inside the patch antenna, any phase or amplitude change caused by feedback from other channels could be accounted for in addition to any phase / amplitude variations due to the amplifier channel itself. This method would require the construction of 73 phase and amplitude detectors, 146 (73 * 2) analog feedback lines, and the associated digital circuitry to convert these analog signals to digital signals for processing by the controlling computer. In addition, 146 analog control lines for the phase control and power amplifier control lines would be required. Due to development time and resource restrictions it was decided to attempt to use another, less costly method.

The method chosen involves trying to design the amplifier chain to keep adjustments in magnitude from introducing undesired phase changes and vice versa. Unfortunately, complete separation between amplitude and phase adjustments is not possible. Due to non ideal components and parasitics there will always be some variation in phase when the amplitude is adjusted and vice versa. Any variation which does occur in the system can be characterized and removed. This is done by carefully measuring the actual amplitude and phase at the output of each channel at various power and phase settings. This information can then be used to 'calibrate' the array, and provide knowledge of the true amplitude and phase produced for a given control setting. This method relies on the long-term stability of the amplifier

chain calibration data. Additionally it is desirable that any amplifier chain magnitude and phase variations be smooth. Any small adjustment in the output amplitude should not cause a large change in the output phase.

To better understand these problems we will take a more quantitative look at the devices.

## 5. PHASE SHIFTERS

There are several typical methods for producing a controllable phase shift. For high power applications, ferrite materials are typically used. These ferrite materials typically reside inside a wave guide, and through the use of a DC bias coil, an adjustable phase shift is possible [4]. Because of the array size restrictions, and the fact that our choice of array topology allows the phase shifter to be located on the low-power side of the amplifier chain, this solution was not desirable. Instead a phase shifter based on varactor diodes was designed.

The design goals for this varactor diode phase shifter were: 1) it must provide a fully adjustable 360° phase shift, 2) its magnitude variation with respect to phase shift should be small, 3) it should have a reasonably low insertion loss, and 4) it must have a small footprint. It was decided that a reflection type phase shifter based on a quadrature hybrid could meet these requirements.

The topology of the phase shifter is shown in Figure 5.1.

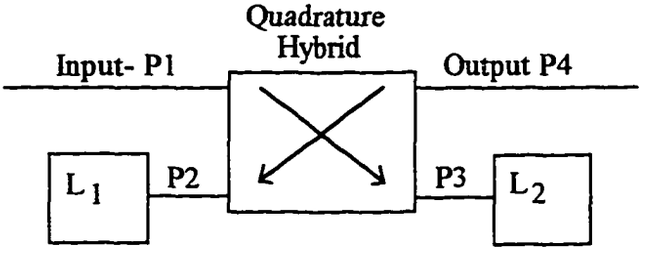



**Figure 5.1: Quadrature hybrid phase shifter topology**

The quadrature hybrid couples the signal at the input to *P3* and to *P2*. The signal arriving at *P2* is 90° out of phase with the signal arriving at *P3* (thus the name 'quadrature' hybrid). If *L1* and *L2* were matched loads, no signal would reach the isolated port, *P4*. The loads *L1* and *L2* are designed to reflect the signals reaching *P2* and *P3*. The reflected signal from *L1* and *L2* add out of phase at the input (*P1*) and in phase at the output (*P4*). This assumes the reflection coefficient of *L1* and *L2* are the same, leading to an important point. For the phase shifter to have a matched input, both *L1* and *L2* should have the same reflection coefficient. In order to produce an adjustable phase shift, the phase angle of the reflection coefficient of *L1* and *L2* must be adjustable. More specifically, if the input signal at *P1* is $V_1^+ = V \cdot e^{j(\Phi_{IN})}$ , then the signals arriving at the loads at ports *P2* and *P3* respectively, are:

$$V_{L1}^+ = \frac{V}{\sqrt{2}} \bullet e^{j\left(\Phi_{IN}+\Phi_c+\frac{\pi}{2}\right)}, \; V_{L2}^+ = \frac{V}{\sqrt{2}} \bullet e^{j(\Phi_{IN}+\Phi_c)}$$

where $\Phi_c$ is an arbitrary fixed phase shift associated with the coupler. As indicated by the magnitudes of $V_{L1}^+$ and $V_{L2}^+$, the coupler also provides a 3 dB power split between the coupled ports. If we assume that $\Gamma_{L1}, \Gamma_{L2} = e^{j\Phi_P}$, then the signals reflected off the loads are:

$$V_{L1}^- = \frac{V}{\sqrt{2}} \bullet e^{j\left(\Phi_{IN}+\Phi_c+\frac{\pi}{2}+\Phi_P\right)}, \; V_{L2}^- = \frac{V}{\sqrt{2}} \bullet e^{j(\Phi_{IN}+\Phi_c+\Phi_P)}$$

These signals pass through the coupler and arrive at $V_{IN}$ (*P1*) and $V_{OUT}$ (*P2*) as:

$$V_{1_{L1}}^- = \frac{V}{\left(\sqrt{2}\right)^2} \bullet e^{j(\Phi_1+2\Phi_c+\pi+\Phi_P)}, \; V_{1_{L2}}^- = \frac{V}{\left(\sqrt{2}\right)^2} \bullet e^{j(\Phi_{IN}+2\Phi_c+\Phi_P)}$$

or

$$V_{IN}^{-} = V_{1_{L1}}^{-} + V_{1_{L2}}^{-} = 0$$

indicating (ideally) a perfect match at the input port. At the output port, the signals due to load 1 and load 2, respectively, are:

$$V_{4_{L1}}^{-} = \frac{V}{\left(\sqrt{2}\right)^2} \bullet e^{j(\Phi_{IN}+2\Phi_c+\pi+\Phi_P)}, V_{4_{L2}}^{-} = \frac{V}{\left(\sqrt{2}\right)^2} \bullet e^{j(\Phi_{IN}+2\Phi_c+\pi+\Phi_P)}$$

where the 90° phase shift is added because of the quadrature nature of the hybrid. This leaves the total signal at the output port:

$$V_4 = V_{OUT} = V \bullet e^{j(\Phi_{IN}+2\Phi_c+\pi+\Phi_P)}$$

where $\Phi_{IN}$ is the input phase to the coupler, $\Phi_C$ is a fixed phase shift, and $\Phi_P$ is the phase of the reflection off the loads. From this it is clear that if *L1* and *L2* are equal and have a reflection coefficient with adjustable phase, a device can be produced that will have a controllable phase shift from input to output [5].

All that is needed to complete the phase shifter design is a reflective load with a controllable phase angle of reflection. This is achieved with varactor diodes. The varactor diode, when used in a reverse biased configuration, acts as a voltage controlled capacitor. By increasing the reverse bias voltage, the depletion region at the *PN* junction is increased. If this depletion region is thought of as the gap between two conducting plates, it can be seen that as this gap increases, the capacitance of the junction should decrease. This is clear from the parallel plate capacitor equation: $C = \varepsilon \cdot Area / Distance$. For commercially available varactor diodes the relationship between the reverse bias voltage and junction capacitance is often specified in terms of the parameters $\Gamma_D$, $C_{T0}$, and $\varphi_{diffustion}$, where

$$C_{Diode} \approx \frac{C_{T0}}{\left(1 - \frac{V_d}{\varphi_{diffusion}}\right)^{\Gamma_D}},$$

and $V_d$ is the reverse bias voltage. Additionally, the capacitance range and maximum reverse bias voltages are specified.

It is known that an LC circuit passing through its resonance exhibits a 180° phase shift. Two LC circuits in parallel, with slightly different resonant frequencies (or in this case resonant bias voltages) can show a 360° phase shift. Using this, and 4 matched varactor diodes as capacitors, the loads for the phase shifters are designed as shown Figure 5.2.

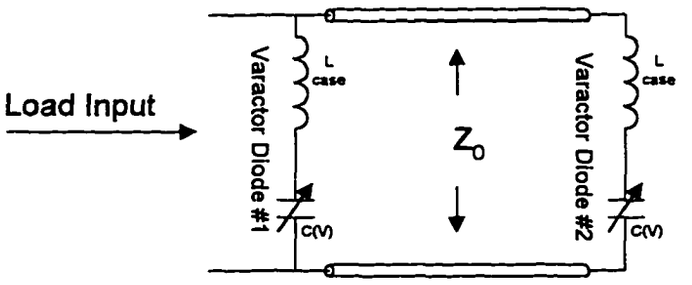



**Figure 5.2: Phase shifter load**

Varactor diodes with capacitances ranging from approximately 0.5pF to 5pF (over a 10 volt bias swing) were chosen. These varactors have case inductances of approximately 0.45nH. The case inductance combined with the varactor diode's capacitance form the desired *LC* circuit. To achieve the full 360° phase shift, the second *LC* combination should begin to resonate where the first *LC* combination finishes its resonant phase shift. Adjustment of this second resonance is easily achieved by adding a length of transmission line between the two varactor diodes. This section of transmission line is

designed to add a series inductance to the second varactor diode, thereby altering the resonant bias voltage. The inductance added to the second varactor diode by this section of transmission line determines how linear the voltage to phase shift relationship is. This inductance also effects the total phase change possible. If the line is too short (too little additional inductance), both *LC* circuits will resonate, and the full 360° phase shift can not be realized. To illustrate this, Figure 5.3 shows the phase of the reflection coefficient (assuming a 50Ω system) for the case where the added inductance of the transmission line section is 5.2 nH (the transmission line parameters are $l \approx 9.5mm$, $\varepsilon_r \approx 4.4$), and the diode case inductance is 0.45 nH (i.e. $L_{total}$=6.65 nH).

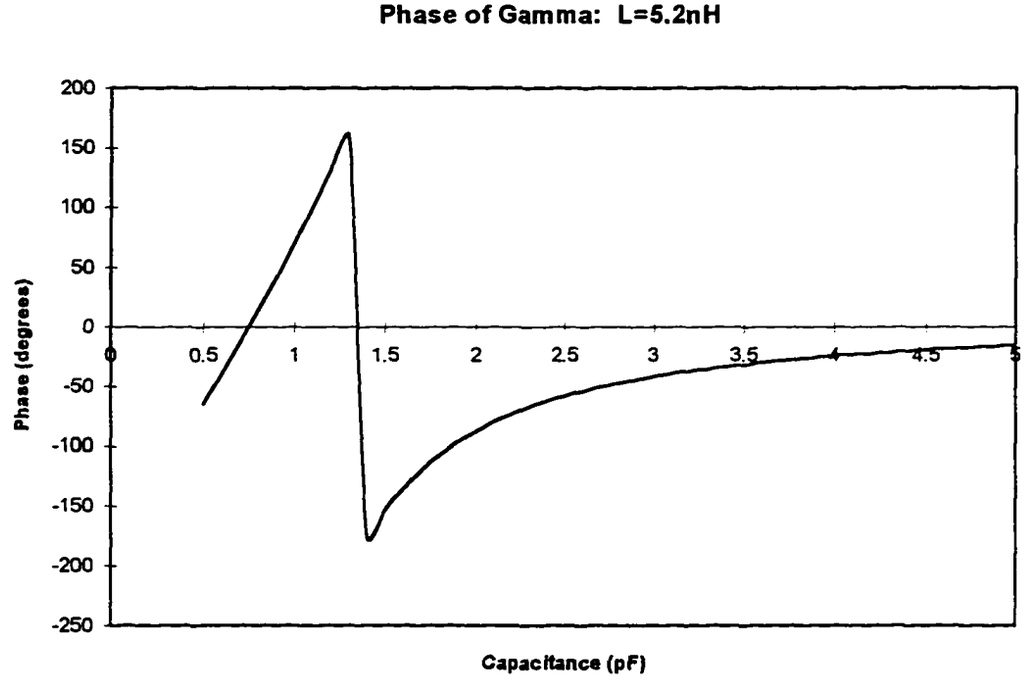



**Figure 5.3: Reflection coefficient phase: L=5.2nH.**

If the transmission line is shortened, so that the resulting inductance is reduced to 0.5nH ($L_{total}$=0.95), the total phase change possible is greatly reduced as illustrated in Figure 5.4.

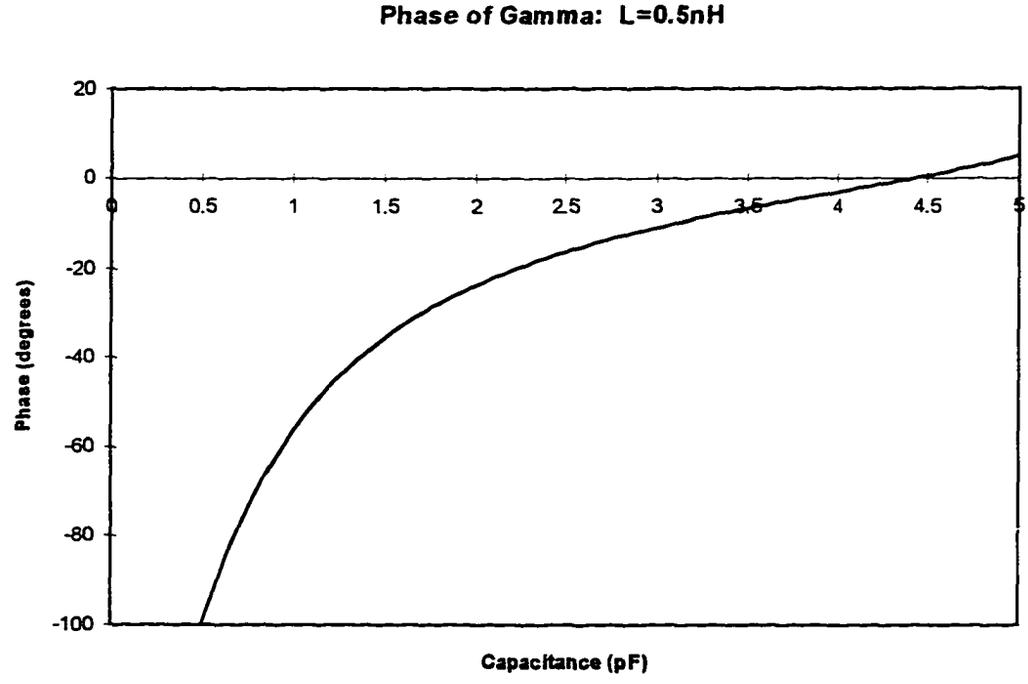



**Figure 5.4: Reflection coefficient phase: L=0.5nH**

When the non-linear capacitance vs. voltage characteristic of the varactor diode is considered and the phase shift (for the nominal case where L=4.5 nH) is plotted as a function of reverse bias voltage, one obtains the relationship shown in Figure 5.5, illustrating a phase shift of more than 360° across the full 10 volt bias range.

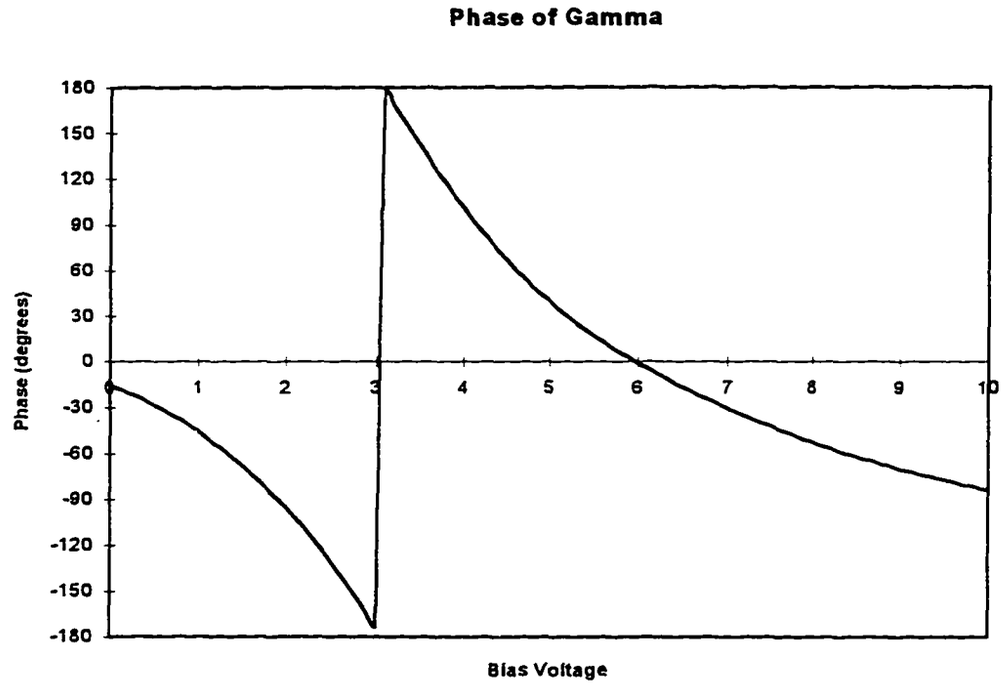



**Figure 5.5: Phase of gamma vs. bias voltage**

It has been assumed so far that the bias voltage required to vary the capacitance of the varactor diodes was simply 'there'. Provisions must be made to supply this bias voltage without altering the microwave properties at the input to the load. Additionally, it is necessary to prevent this DC bias from changing the DC operation of circuits attached to the phase shifter (e.g. it could change the bias on the pre-amplifier). One method that could be used involves using an RF shorted quarter wave choke as the bias feed line. A DC blocking capacitor can then be used to isolate the DC bias. Figure 5.6 illustrates this concept.

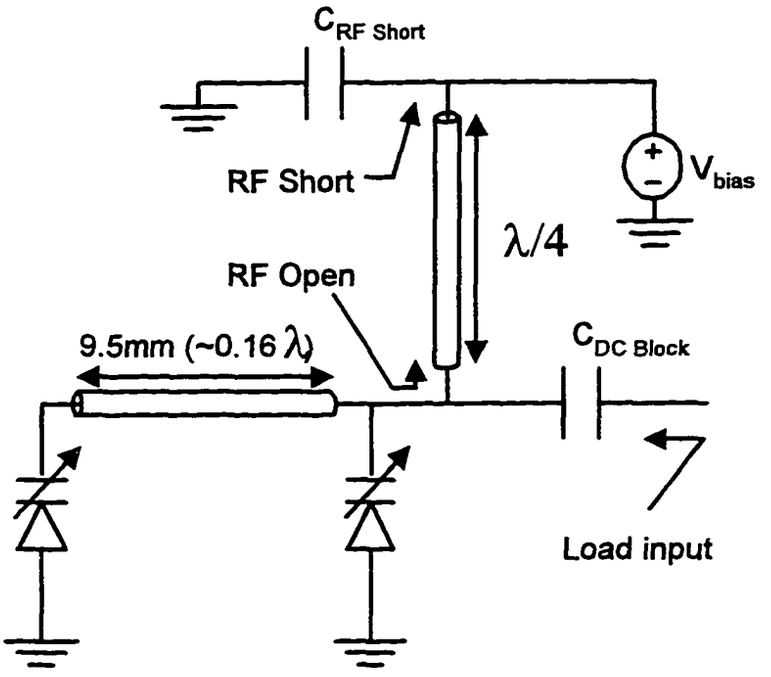



**Figure 5.6: Load with bias circuit**

This topology allows the DC bias voltage to reach the varactor diodes without significantly changing the microwave properties seen at the load input. A microwave grade surface mount capacitor, *C1*, creates an RF short at the end of the quarter wave line. This presents an (ideally) infinite impedance at the load end of the quarter wave choke, leaving the microwave properties of the load unaffected.

The quarter wave choke however, takes up a lot of real estate. Fortunately, since the varactor diodes draw essentially no current, a more space conscious topology can be used. This topology replaces the high impedance quarter wave choke with a high value resistor (Figure 5.7). From a transmission line standpoint, a quarter wave choke looks like an open

circuit. A high value resistor, 910 Ω in our case, looks very much like an open circuit to a 50 Ω transmission line.

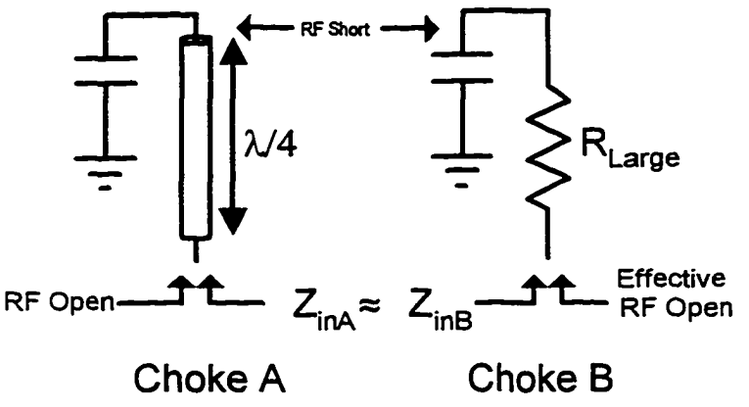



**Figure 5.7: RF blocking resistor**

Because there is essentially no DC current passing through the varactor diodes, there is no DC voltage drop across the blocking resistors. Therefore the RF blocking resistors have no significant effect on the DC biasing of the varactors. Capacitors on the DC side of the resistors force the DC bias input point to be a good RF ground. The resulting phase shifter topology is shown in Figure 5.8.

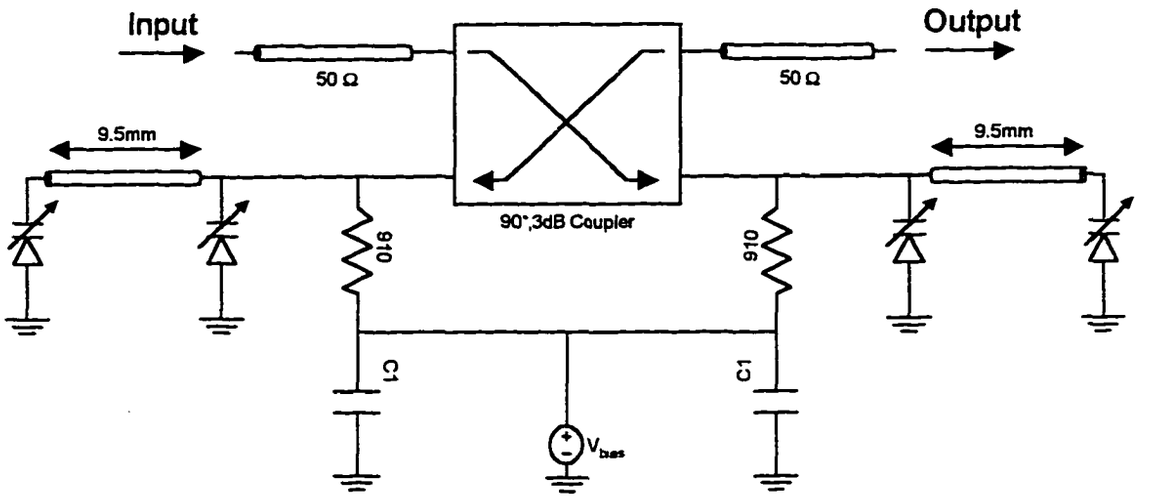



**Figure 5.8: Phase shifter with loads**

Several important issues still need to be addressed. First, the varactor diodes have loss which becomes significant at microwave frequencies. This loss it usually specified in terms of a 'Q'. This loss can be modeled as a resistor in series with the varactor capacitance. Also, it has been assumed that the varactor diodes are identical, and that the coupler is ideal. In reality differences in varactors due to process variations, system losses and, nonidealities in the coupler have significant effects on the operation of the phase shifter. In order to attempt to compensate for these effects, a commercially available software package called Microwave Harmonica® [6] was used to simulate the circuit. The simulation software allows the effects of many of the non-ideal properties to be modeled. The system (as shown in Figure 5.8) has been modeled using a standard hybrid coupler (using the built in model as shown in Figure 5.9) and non-ideal diodes. These simulations have indicated good performance from the phase shifter. Figure 5.10 shows

the simulated S-parameter $S_{21}$ of the phase shifter as the bias voltage is swept from 0 to 10 volts.

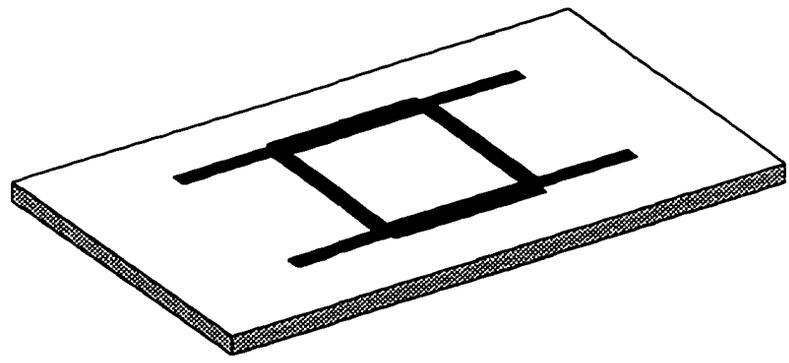


**Figure 5.9: The branch line hybrid coupler**

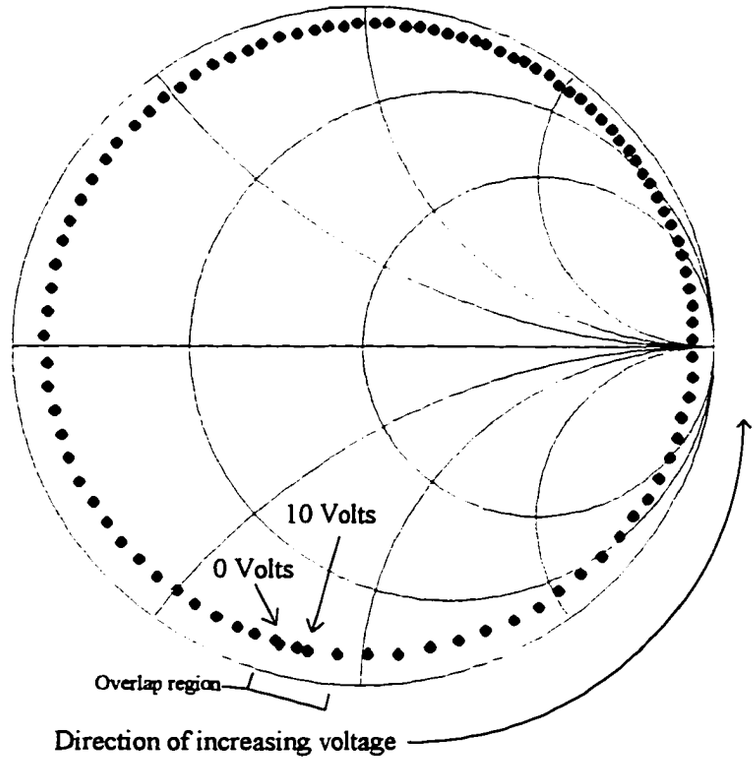



**Figure 5.10: Initial simulation of $S_{21}$**

Unfortunately after constructing and measuring the phase shifter it was found that the device had greater than 6 dB insertion loss, and that the phase shifter exhibited a 3 to 4 dB power variation as the phase was shifted over the 360° range. The measured $S_{21}$ data is shown in Figure 5.11.

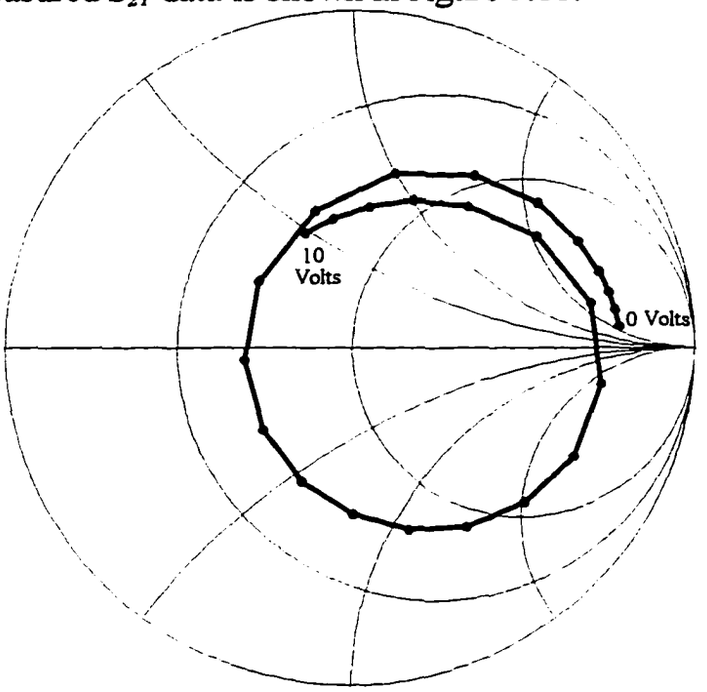



**Figure 5.11: First phase shifter performance**

Many simulations in which the various parameters were tweaked did not resolve the discrepancy between the predicted and measured responses. It was decided that the branch line hybrid coupler should be measured by itself and the measured *S* parameters should placed into the simulation rather than assuming an ideal coupler. A branch line coupler was etched on a PC board (FR-4, same as the phase shifter) without any of the other phase shifter components, and a 4 port test fixture built. Using an HP 8720C network analyzer, *S* parameter data was taken. The measured *S* parameters were then

used in the simulation. It was found that the finite isolation (a measure of signal output at the isolated port of the coupler due to an input signal with all other ports match terminated) of the coupler was not being adequately modeled in the original simulations. The simulator predicted an isolation of more than 60dB, while in reality, the coupler showed only 15dB of isolation. Simulations showed that the isolation of the coupler is an important factor in 'centering' the 'phase circle' on the Smith chart (centering corresponds to a flat magnitude response). Differences in diode parameters were also simulated to determine if this could lead to poor performance. Several simulations and measurements showed that slight differences in load capacitances did not significantly hinder the performance of the phase shifter. It was found experimentally that the lack of good isolation in the quadrature hybrid could be compensated for by adding reactive tuning elements to the hybrid itself. Additionally, through more careful simulation of the components in the phase shifter, it was determined that the Q's of the varactors were low enough at 2.45 GHz to account for the remaining loss in the circuit.

In order to improve coupler isolation and further reduce the footprint of the phase shifter, the quadrature hybrid coupler was replaced with a wireline coupler. The wireline coupler is a commercial product that consists of a section of coaxial cable with two coupled inner conductors (Figure 5.12).

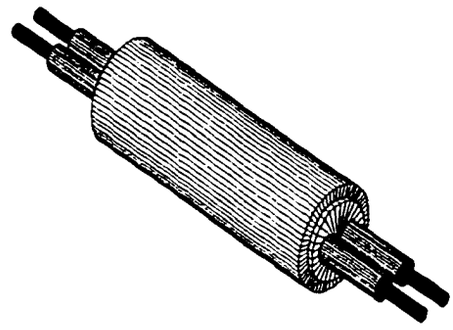


**Figure 5.12: The wireline coupler**

By cutting the wireline to the proper length the desired 3dB coupling can be obtained at 2.45 GHz. The *S* parameters of the wireline coupler were measured for use in the simulation. The wireline coupler showed improved isolation over the branchline coupler; however, it was decided that because the wireline had to be manually trimmed to the proper length, it would be difficult to manufacture in a consistent manner.

Finally, another commercially available product, the Anaren 3dB 90° coupler (Figure 5.13) was identified and tested. This coupler has a very small footprint, and better isolation than the wireline and branchline couplers. The isolation of the Anaren coupler is shown in Figure 5.14.

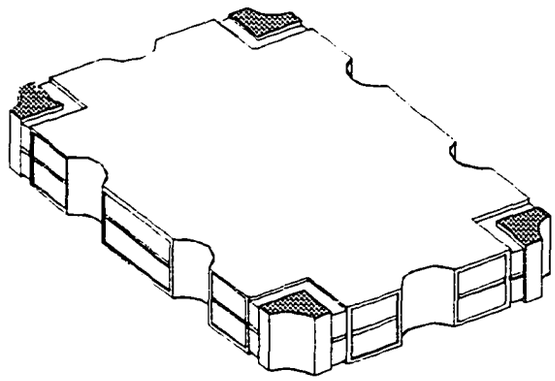


**Figure 5.13: The Anaren coupler, ~3 times actual size**

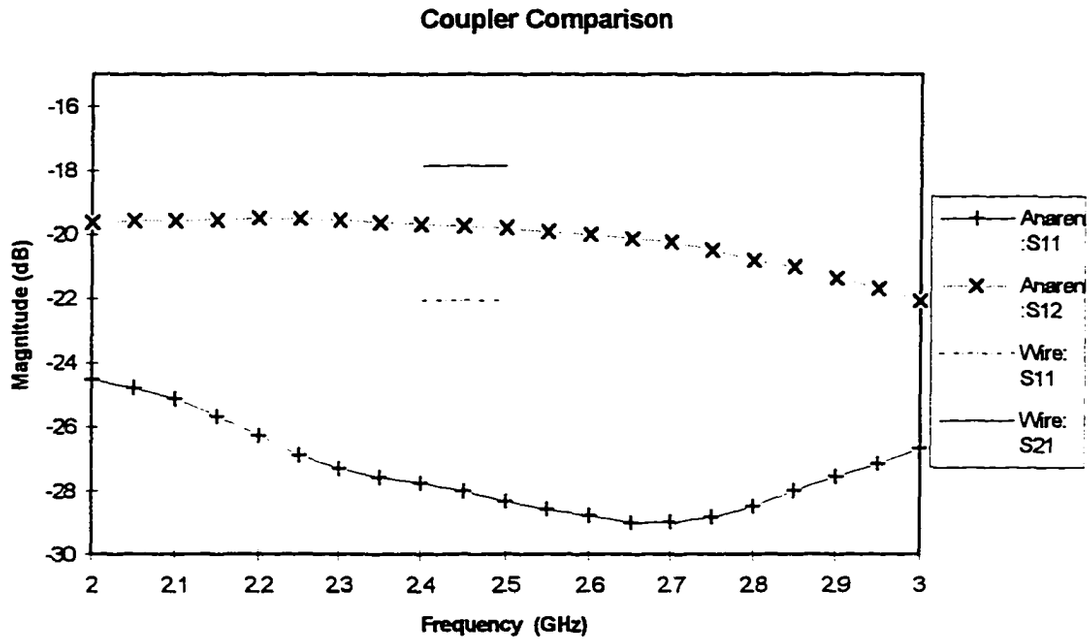



**Figure 5.14: Coupler performance comparison**

Figure 5.14 shows that the Anaren coupler has superior performance at 2.45 GHz. Note that the data for the wireline coupler below 2.4 GHz and above

2.5 GHz was not taken. As shown in Figure 5.15, the Anaren coupler did show slightly more loss. However it had a better power balance between coupled ports. The wireline coupler did provide a better phase balance (with respect to the ideal 90° phase differential between coupled ports) than the Anaren device. This phase balance data is shown in Figure 5.16. Overall, mainly due to the much improved isolation, the Anaren device is favored for this application, and was selected for the final design.

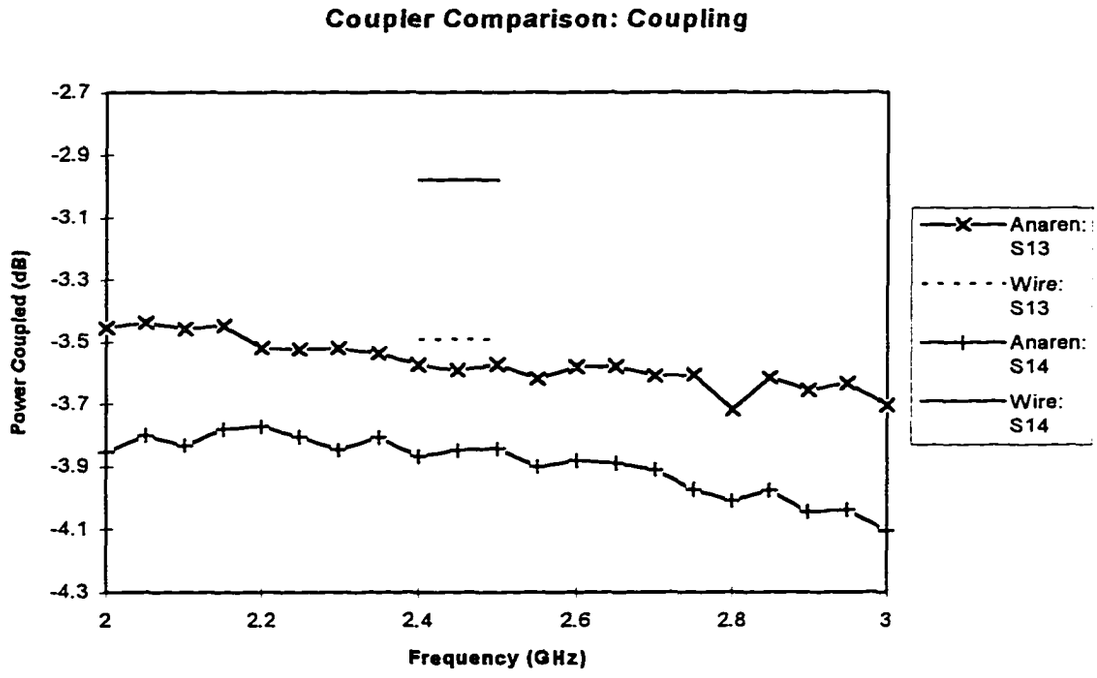



**Figure 5.15: Coupler performance comparison: coupling**

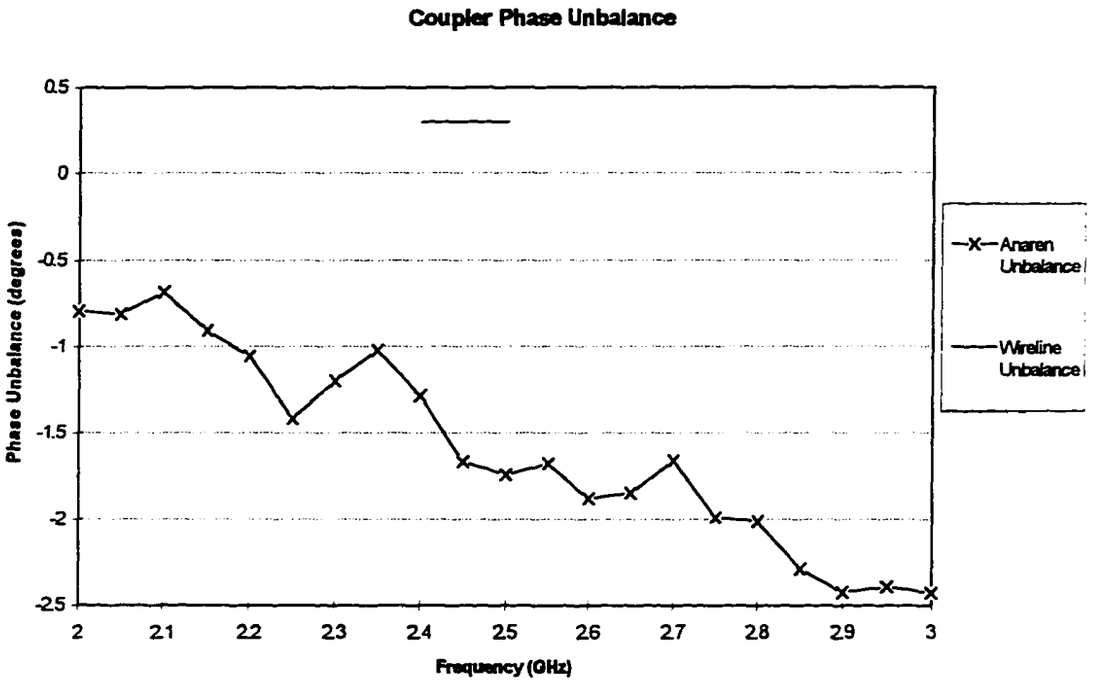



**Figure 5.16: Coupler comparison: phase imbalance**

Several different Anaren couplers were measured, and the average isolation was determined to be approximately -19.5 dB. Using the measured *S* parameter data, the lossy diode models, and the optimization capability of the simulation package, a phase shifter was designed using the Anaren coupler. The optimized simulation data for the S-parameter $S_{21}$ is shown in Figure 5.17 and the associated insertion loss data is shown in Figure 5.18.

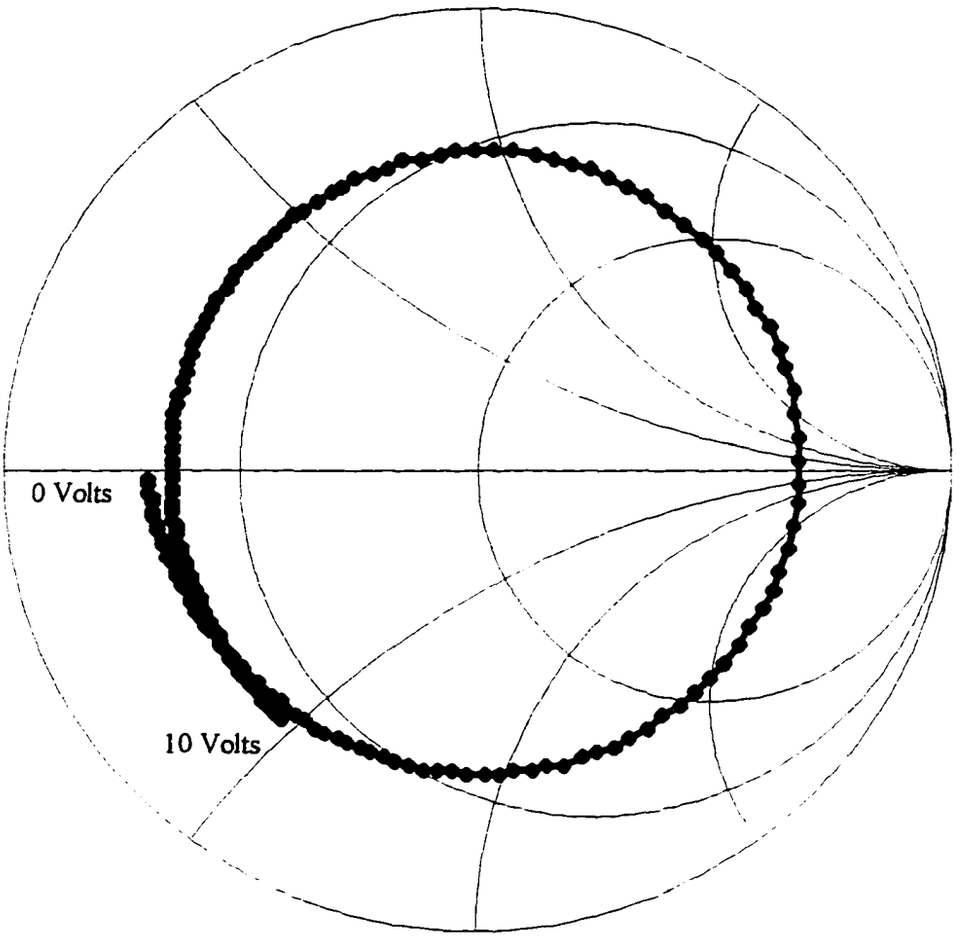



**Figure 5.17: Simulation - improved phase shifter**

As can be seen in Figure 5.18, the simulation predicts a substantial (3-4 dB) loss. However the variation of the magnitude of $S_{21}$ is approximately 0.6dB, significantly better than in the hybrid coupler based phase shifter. Most of the loss results from the loss in the varactor diodes. An effort was made to obtain diodes with higher 'Q' values (less loss). Unfortunately, no diodes were found that a had significantly higher 'Q' at 2.45 GHz.

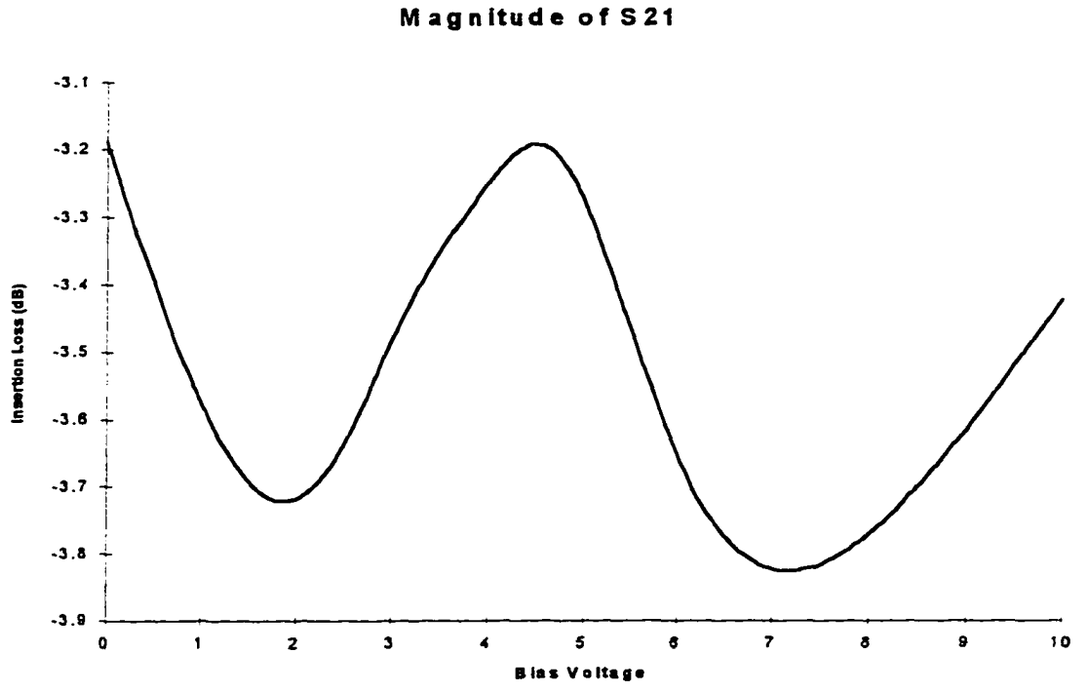



**Figure 5.18: Improved phase shifter loss (simulation)**

The Anaren coupler based phase shifter was constructed and measured. Its performance was significantly better than the hybrid coupler based phase

shifter and more closely matched the simulation data. The measured $S_{21}$ data is shown in Figure 5.19.

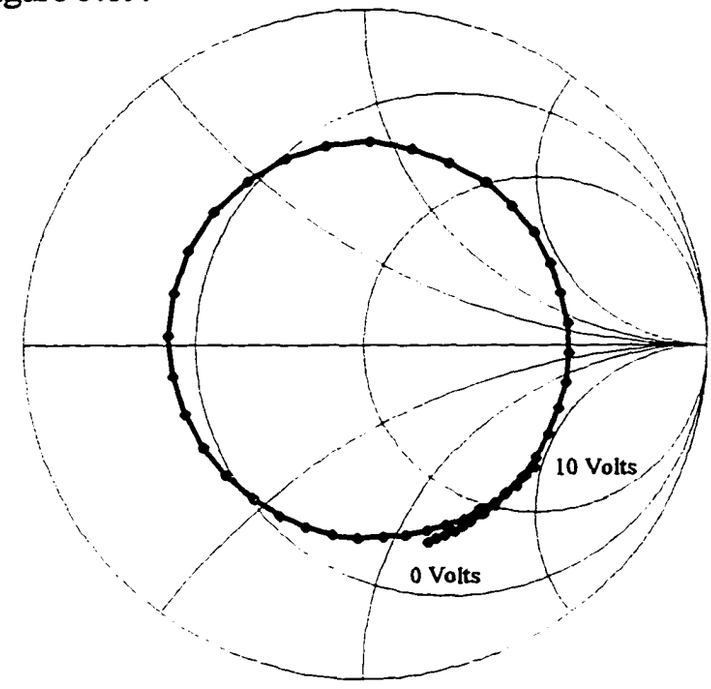



**Figure 5.19: Measured $S_{21}$ of improved phase shifter**

As observed from Figure 5.20, this design exhibited an acceptably flat response across the entire 360° phase shift.


**Figure 5.20: Improved phase shifter - measured insertion loss**

Although these measured results differ somewhat from the simulations, it was decided that the performance of the phase shifter was acceptable. However, some effort was made to reconcile these differences. Solder tests performed on junctions between the APC connectors on the test jig and straight through transmission lines indicated that the solder joints are not only difficult to repeat, but that they also introduce significant discontinuities in the system. It is likely that the many solder joints in the phase shifter contribute to the differences, as these joints can not be readily modeled in the simulator. Additionally, the simulator does not attempt to model radiation losses in the circuit. It is felt however that the radiation losses do not contribute a

significant portion of the discrepancies between the predicted and measured performance.

As a result of the transmission line interconnect solder tests, it was also determined that the loss tangent $\delta$, and relative permitivity $\varepsilon_r$, of the FR-4 board material we were using varied significantly from board to board. Additionally, it is suspected that process variations in the diodes, and differences between the nominal specified 'Q' and the actual 'Q' values for each diode contributed to the differences between the simulated and actual values.

In the final configuration the phase shifters are covered by a ground plane attached to the top of the Anaren couplers. For this reason all the testing was done with a ground plane covering the phase shifter. Simulations were used to select the proper line width, taking into account the effects of a conducting cover in the line impedance. It was found that the cover makes a significant difference in the performance of the phase shifter, and it must be in place before any accurate measurements can be made. This result should be expected as the cover is within 0.070" of the transmission lines, and is in direct contact with the Anaren coupler.

The Anaren coupler phase shifter functioned acceptably. In addition to its electrical performance, the Anaren coupler phase shifter design resulted in a compact footprint. The footprint of the final phase shifter design met, meeting the periodicity requirements of the array. To achieve the 73 element pattern shown in Figure 3.2, we decomposed the element network into 7, 8, and 9 element modules. For ease of assembly and construction of the array, it

was decided that all phase shifters used in a module would be built on a single substrate. Printed circuit layouts for the 7, 8, and 9 element modules were produced and the boards were manufactured. Bias lines for the 9 phase shifters were routed on the board to a surface mount plug which connected to the backplane of the modules, and from there to the controlling computer.

From the difficulties in accurately predicting the performance of the initial hybrid coupler phase shifter design and the subsequent successful simulation of the Anaren coupler phase shifter it is clear that seemingly non-critical details can significantly alter the system performance. This problem is compounded by difficulties in accurately describing devices in built-in simulator device models and the inherent limitations of simulation. However, it is clear that if care is taken to include as much of the non-ideal elements as possible in the simulation, and measured data is used whenever possible, these difficulties can be greatly reduced. It was clear at the end of the design of this phase shifter that the development time can be significantly reduced by spending more time building test fixtures and measuring individual components before simulating and trying to construct a 'one step' design. Although building test fixtures and taking initial measurements can be time consuming, in the end less time will be spent debugging, redesigning and rebuilding the system.

# 6. AMPLIFIER

The signal leaving the phase shifter needs to be amplified to approximately 10 watts. In addition to the output power requirement, it is desired that the amplifier exhibit certain characteristics. Because the array is calibrated and does not have a feedback circuit it is important that the phase shift through the amplifier not vary excessively or unpredictably with a change in signal amplitude. It is also important that the characteristics of the amplifier not change significantly with time or temperature.

Currently there is not a large selection of solid state devices available for the 2.45 GHz Band. After much searching two components were found that would accomplish the task. These two components were arranged as an pre-amplifier / amplifier system. The amplifier that was chosen for the pre-amplifier is the Pacific Monolithics PM2104. The PM2104 is a surface mount microwave amplifier module designed to be used on microstrip. Of the available amplifiers, the PM2104 specifications showed the highest combination of gain and output power for a single chip device. The PM2104 is designed to be used in a saturated gain mode. In this mode the amplifier requires between 5 and 10 dBm input power; and when properly biased, it will produce +31 dBm output power.

## 6.1 Pre-amplifier

To test the amplifier module for the first time, we used a layout provided by Pacific Monolithics. This layout provided a platform to test the amplifier and verify the specifications provided by Pacific Monolithics. The

layout provides electrical connections for a 50 Ω input, 50 Ω output, main power supply, and two gate bias connections. A pad of vias mounted underneath the chip allows for heat dissipation to a metal heat sink / ground plane beneath the circuit board. Although the PM2104 is internally matched to a 50 Ω load on the output side, power supply filtering, RF bias blocking, and low frequency matching components were added to the layout. The input to the chip included a small matching circuit that consisted of an RF shorted matching stub (RF short provided by capacitor C6) which was implemented with part of the DC gate bias supply line. The layout is shown in Figure 6.1.

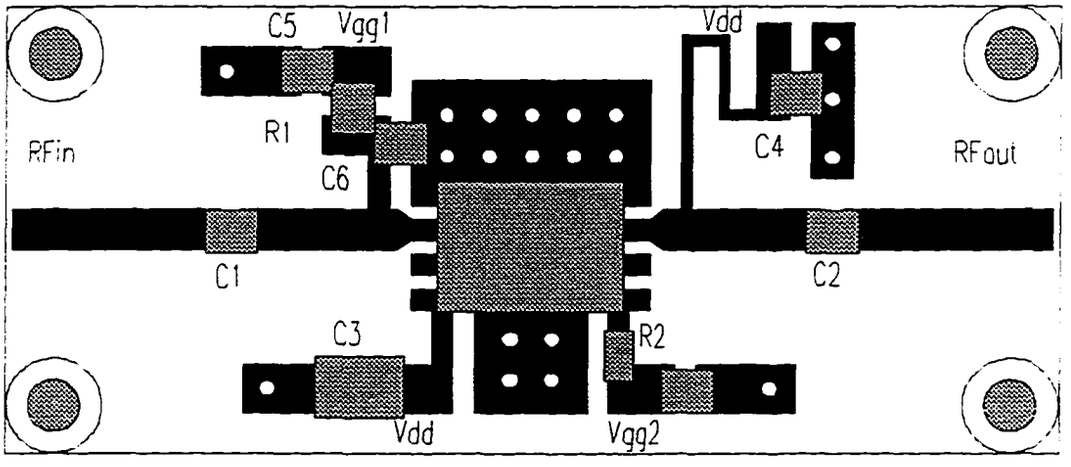



**Figure 6.1: Pre-amp test board**

The resistors R1 and R2 were 50 ohms which, at low frequencies (where the input blocking capacitors open up), make the RF input appear to be a 50 ohm load. This helped prevent oscillations in the amplifier by allowing a (roughly) 50 Ω match to exist all the way down to DC. A quarter wave choke on the output supply blocks the RF output signal from entering the $V_{dd}$ supply line.

Blocking capacitors on the RF input and output prevented DC voltages from entering the network analyzer during the tests.

Measurements taken on the PM2104 led to the conclusion that with proper cooling the amplifier could be over-driven to produce about +32 dBm output power. To accomplish this it was found that the amplifier supply voltage ($V_{dd}$) needed to be changed from +5V to +6.8V. Several 24 hour test cycles were run to determine if this would cause the properties of the amplifier to change significantly. It was determined that overdriving the amplifier did not significantly alter its performance (except, as desired, increasing the output power).

The PM2104 amplifier required two bias voltages, $V_{gg1}$ and $V_{gg2}$. The bias voltage $V_{gg1}$ was fixed and supplied the bias for the input circuitry of the amplifier. The bias voltage $V_{gg2}$ was used as a output power control line. As $V_{gg2}$ became more negative the output power of the amplifier dropped. The specifications of the PM2104 provide no information on the phase response of the amplifier due to changes in the input amplitude. As mentioned previously, it was very important that the amplifier not be particularly sensitive to power changes in the input because the output power of the phase shifter does vary slightly with phase. Also, it was thought that the bias line $V_{gg2}$ on the PM2104 amplifier could be used instead of a variable attenuator to control the amplitude of the amplifier chain. However, there was no data available to show how the phase of the output of the amplifier changed due to a controlled gain change (change on $V_{gg2}$). Using two digital to analog (D-to-A) converters to drive the bias voltages, a computer controlled power supply

to drive $V_{dd}$, a computer controlled network analyzer, and the test circuit board, several tests were performed to determine if the amplifiers could be used in this configuration.

Bias voltage measurements were taken by having the computer sweep $V_{gg2}$ while incrementally stepping $V_{gg1}$. This, in turn, was repeated for a range of input powers. It was found that the amplifier provided maximum power when $V_{gg1}$= -1.0V. The data taken from the network analyzer was processed. Figure 6.2 - Figure 6.4 summarize the operation of the amplifier as several of the input parameters were varied.

Notice that once $V_{gg1}$ was optimized, all subsequent data was taken at this optimized voltage. The data for the variations of parameters shown in Figures 6.2 - 6.4 were obtained while $V_{gg1}$ was fixed at -1.0V.

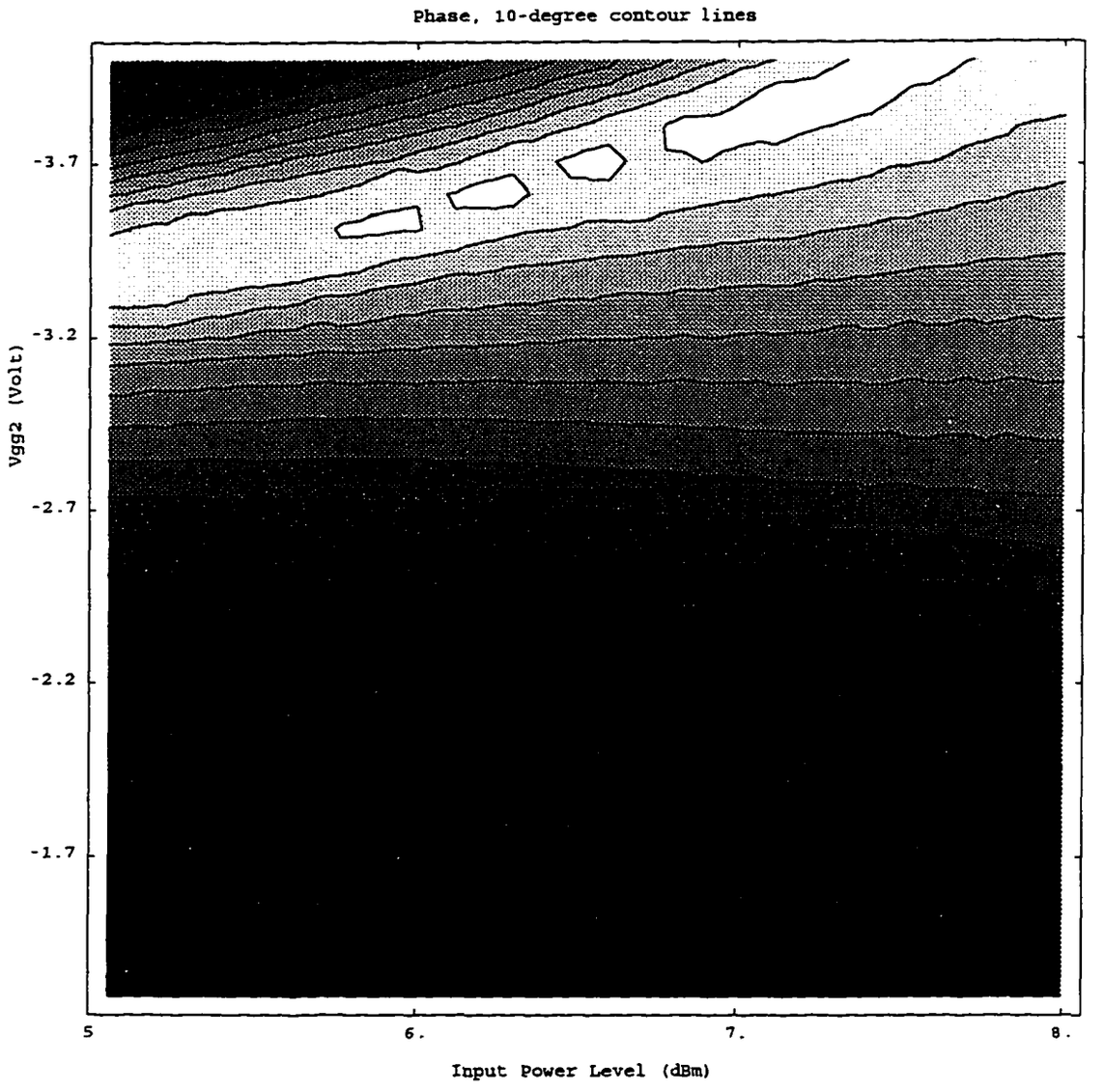



**Figure 6.2: Contour plot, phase as a function of $V_{gg2}$ and $P_{in}$, $V_{gg1}$=-1.0V**

As can be seen from Figure 6.2, at most operating points the overall gain and, thus, the output power of the pre-amplifier was not strongly dependent on the input power. This was extremely advantageous for this application. It meant that small variations in the input power (e.g., due to an unlevel phase shifter

output versus phase change) would have little effect on the phase change through the preamplifier.

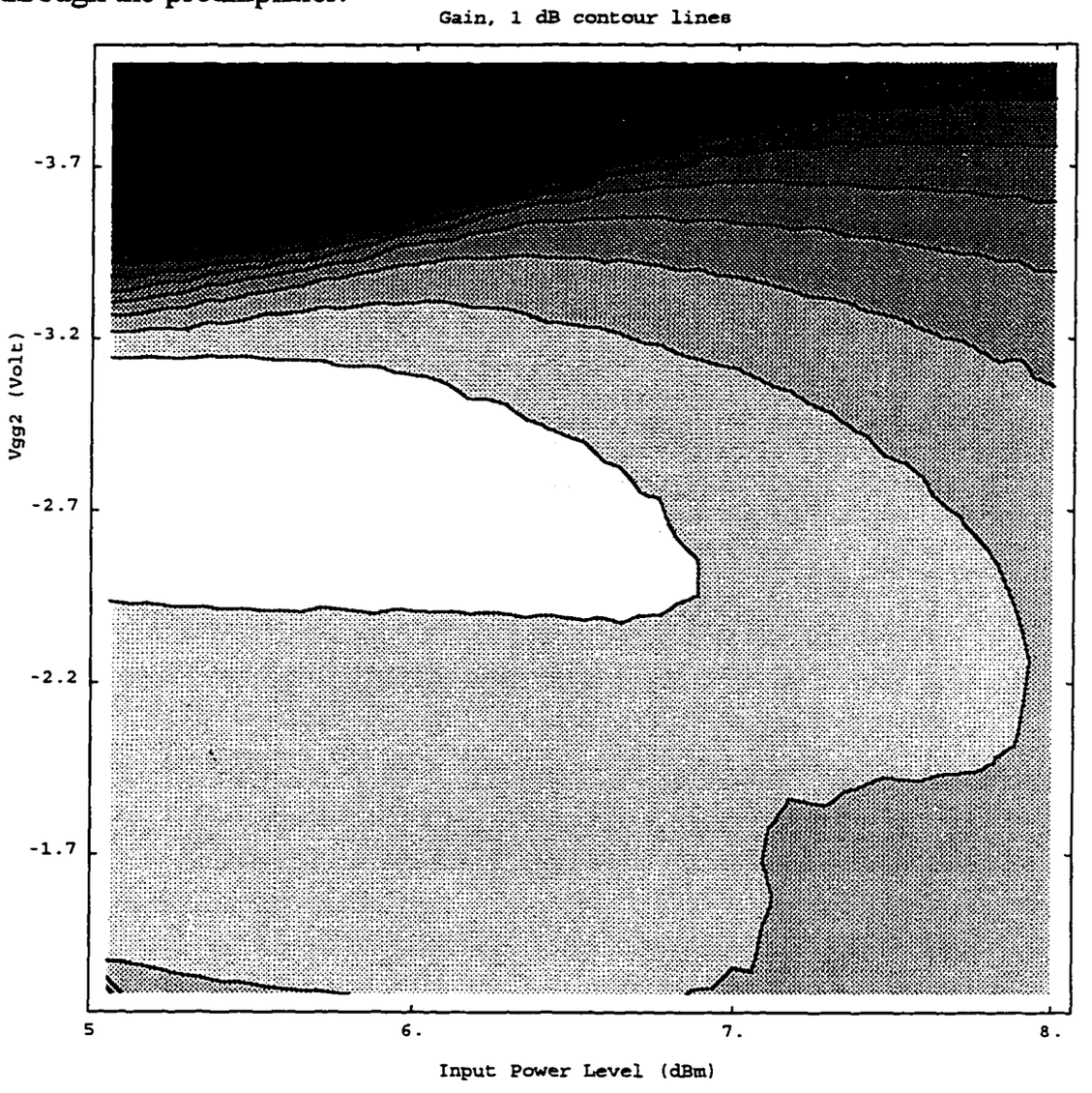



**Figure 6.3: Contour plot of amplifier gain**

From Figure 6.3 it is clear that the gain of the pre-amplifier was relatively insensitive to input power variations. Again, this was advantageous, because

it indicated that the output power of preamplifier would not vary significantly if the input varied a small amount.

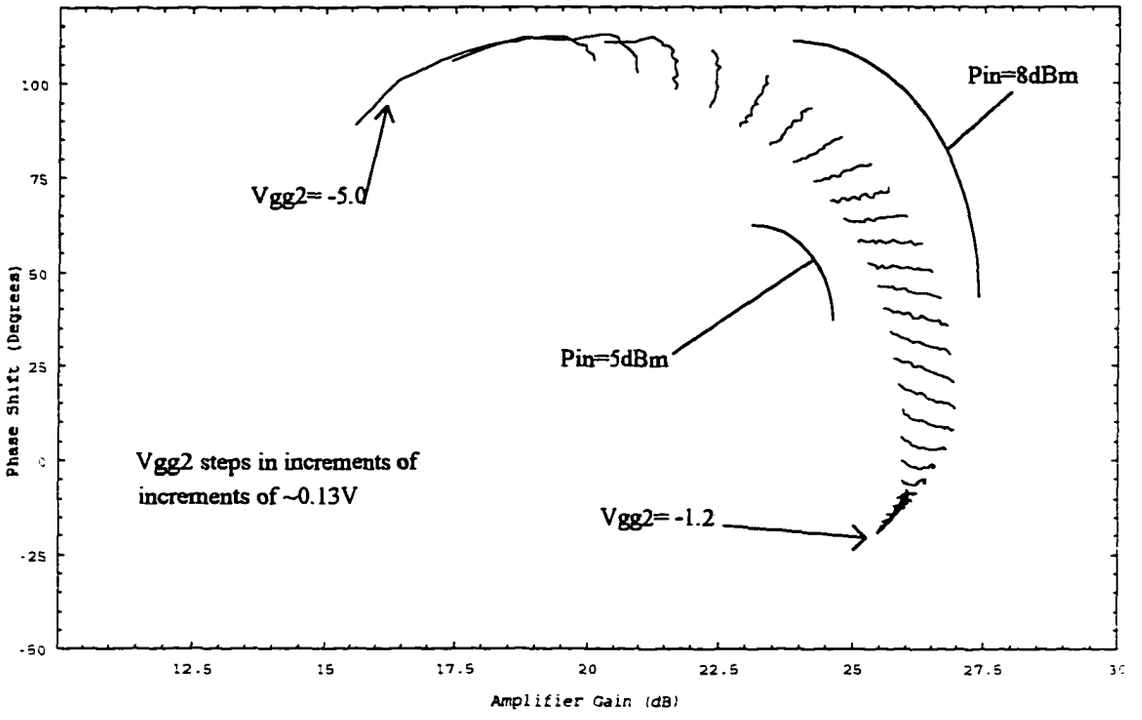



**Figure 6.4: Phase variation vs. amplifier parameters, another view.**

Figure 6.4 further illustrates the smoothness in the output phase shift with parameter variations. Over most of the operating range the phase shifts are subtle, and vary smoothly. Because the phase does not vary wildly, the channel will be easily characterizable.

A solid state cooler was added to the measurement system to control the temperature of the amplifier chip. The above measurements were then repeated at several different times at various temperatures to conclude that the

amplifier characteristics were stable enough (see APPENDIX B) with temperature changes (as much as 20°C change was tested) to use the calibration scheme proposed.

After using the gathered data to approximate a maximum power point, tighter sweeps about that point were made to optimize the output power. It was thus determined that the maximum output power for the PM2104 amplifier occurs at $P_{in}$=5.5dBm, $V_{gg1}$= -1, $V_{gg2}$= -2.4, $V_{dd}$=6.82. At this point the output power was 31.6dBm, which translates to a maximum gain of 26.1dB.

At this power level an 8 hour measurement was performed to determine how much the output power would drift over a long period of operation. Data was taken on the phase deviation over this period as well. The results indicated that the output power is stable to within 0.15 dB and that the phase is to stable within approximately 4°. Both of these values were considered acceptable deviations.

Due to software time out issues on the computer controlling the network analyzer (the system times out after 5 minutes), this 8 hour sweep data could not be downloaded in numerical format. The data only exists as plots produced directly from the network analyzer, which are presented in Figures 6.5 - 6.6. Several things should be noted about these plots. First, the power deviation plot shows the reference power level to be -4.05 dB. This is due to a high power attenuator which was connected to the port on the network analyzer and was used to bring the power level down to an

acceptable level for the network analyzer's test set. The attenuator provided approximately 30dB of attenuation, leaving :

$$[S_{21Meas}]_{dB} \approx -30dB + [P_{Amp}]_{dB} - [P_{In}]_{dB}$$

or,

$$-4dB \approx -30dB + [P_{Amp}]_{dB} - 5.5dB$$

$$P_{Amp} \approx 31.5dB$$

Additional items that should be noted on the power deviation plot are the labels 'PC' and 'C2?'. These labels indicate that a power calibration was performed and that the full 2 port calibration data setting was being used, but was 'questionable'. This deserves some explanation. The power calibration was required in order to ensure that the network analyzer was providing 5.5dBm to the input of the preamplifier. This calibration made use of an external power meter and, through the HP-IB bus on both devices,

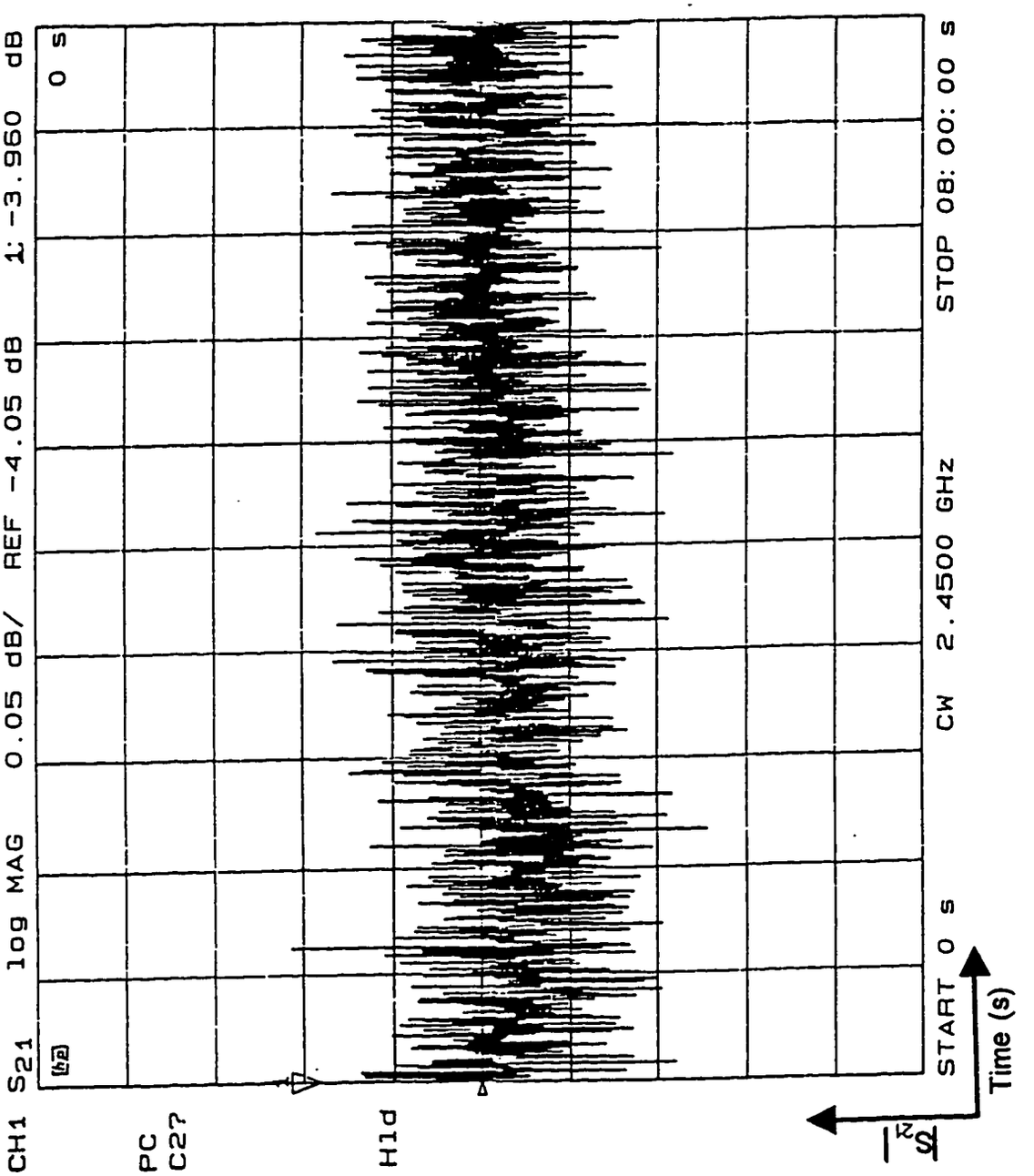



**Figure 6.5: Power deviation of preamplifier**

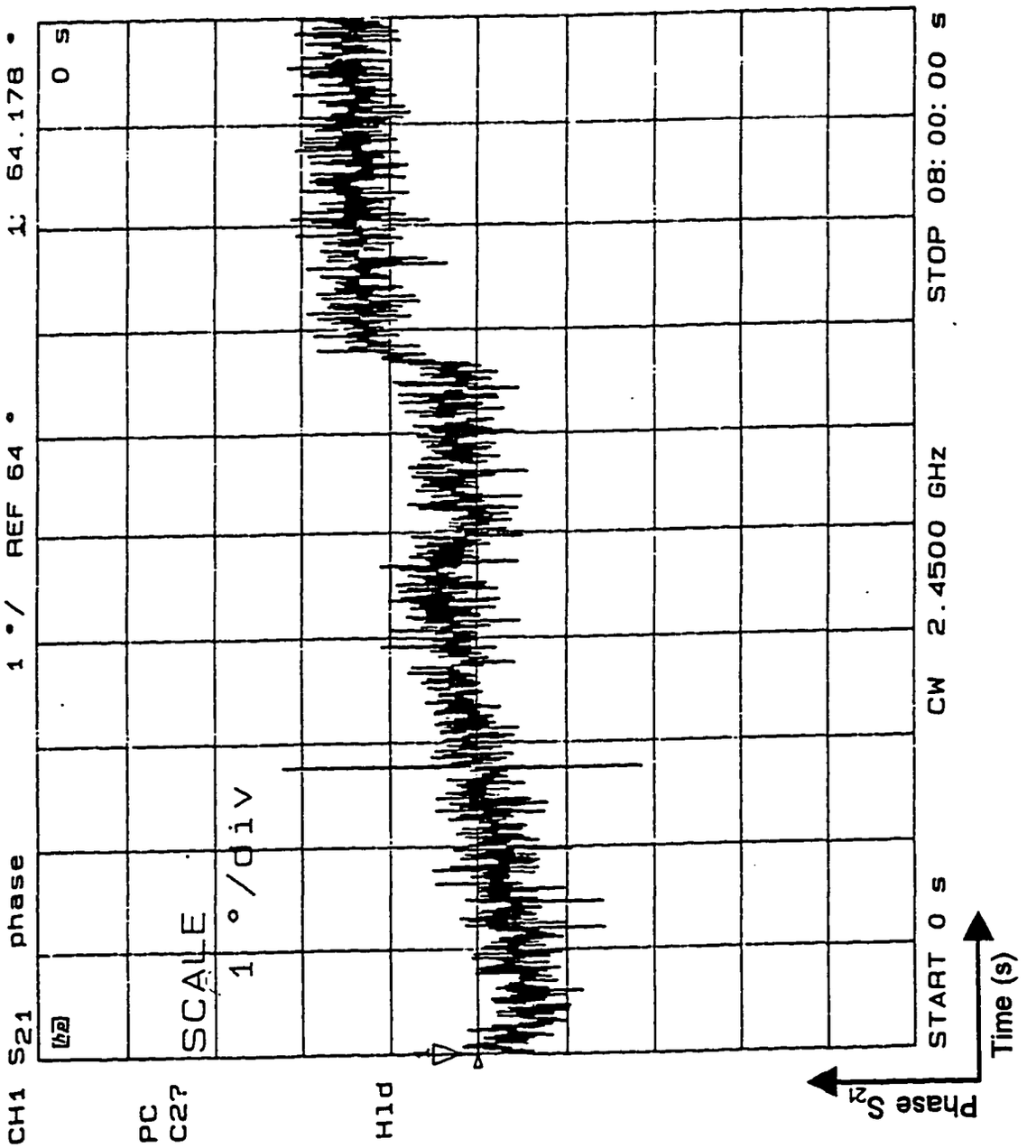



**Figure 6.6: Phase deviation of preamplifier**

corrects the network analyzer's source power until it agrees with the (calibrated) power meter. When a full two port calibration is performed on the network analyzer, all measurement conditions (frequency, sweep time, output power range, number of data points, etc.) must be set exactly as they will be when the actual measurement is taken. Measurements are taken at each data point. When the actual measurement is made, these same data samples are then used to remove the parasitics of the measurement system. If a measurement parameter is changed, the calibration data may become invalid. In our case the analyzer indicated a questionable two port calibration because the calibration sweep time was several seconds, and the measurement sweep time was 8 hours. This was done because an 8 hour calibration cycle would not be any more valid than a reasonably short one. The network analyzer simply was repeatably making the same measurements at different times for this calibration, and, hence, all of the calibration points should have contained the same calibration data. Hewlett Packard's specifications on the HP8720C indicated that once warmed up, the HP8720C's calibration data would remain valid for more than a week (after that internal component drift could possibly cause the measurement error to exceed HP's specified standards for the 8720C). Unfortunately, for this type of long run measurement there was no way, short of performing an 8 hour calibration cycle, to 'convince' the network analyzer that its calibration data was valid. In short, despite the 'C2?' on the plots, the measured data was valid.

Several different chip modules were tested and it was found that the variation between modules was not significant and would not cause any problems. The maximum power point was very consistent from amplifier to amplifier. There were subtle differences in the sweeps but all of the measurements taken led to the conclusion there would be no problem calibrating out the phase shift in the pre-amplifiers as long as each channel was calibrated individually.

The footprint requirements for the preamplifier are similar to the phase shifter in that they both must conform to the element spacing of the antenna array. Unfortunately, the footprint of the test circuit was too wide to meet these space requirements. Some redesign work of the amplifier layout was required to make the preamplifier module fit within the allotted 0.719" channel width. This width was even further reduced by approximately 0.040" to accommodate metal 'fins' which act to shield one channel from the next, thereby reducing any coupling from one channel to another. Without these fins, the metal carrier containing the 9 (7 or 8) channels could act as a resonant cavity, greatly increasing undesired channel coupling. This cavity, inconveniently, happens to be on the order of a wavelength in air (cavity length is approximately 6.5", $\lambda_{air} \approx 4.8$"). Additionally, it was necessary to route the bias and the supply voltage lines to the edge of the circuit board so that convenient and reliable electrical connections could be made to the module. The resulting layout, as shown in Figure 6.7, was significantly more compact than the original and provided for an input signal feed from the output of the phase shifter which could be placed underneath the amplifier.

The layout also contains wiring for protection circuitry (which will be discussed in section 8), holes for screws to hold the board to the carrier, and the matching and input bias circuitry for the power amplifier, which will be discussed next.

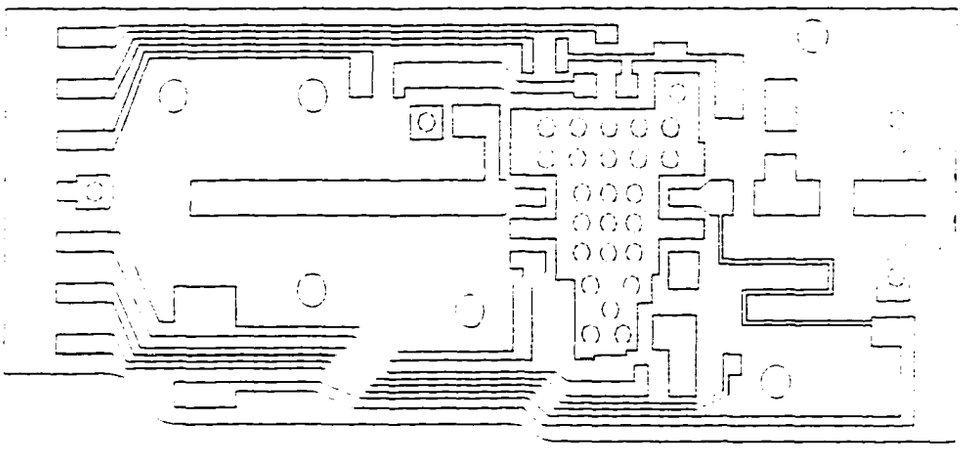


**Figure 6.7: Final preamplifier layout**

## 6.2 Power amplifier

Assuming the required drive of +5.5 dBm can be realized at the input to the preamplifier, we found that the output of the pre-amplifier can then reliably supply up to +31dBm to drive the power amplifier. To achieve the required 10 watts (+40dBm), the power amplifier must have a gain of at least +9 dBm. Although there are several devices on the market which can supply this gain, only one was found that could output 10 watts. This part was the NEC NE6501077. The NE6501077 is a GaAs FET designed to operate CW class A. Unfortunately, the NE6501077 is a relatively new component and,

therefore, there is not a lot of data available on it. Additionally, it is a relatively expensive transistor at $149 apiece. This led to the following two choices. First, the final amplification could be done using power combining techniques which would combine the output power from several lower power output devices to produce the required +40 dBm. Second, the NEC device could be used. Because of the size restriction of the array and the complexity of power combining (leading to increased development time), the power combining option was ruled out, and the NE6501077 was chosen for testing.

Unfortunately, the NE6501077 is not internally matched to 50 Ω on either the input or output side. The only data available for the NE6501077 is a table of *S* parameters at various frequencies, illustrating the severe mismatch of the device. The S-parameter data is summarized in Figure 6.8.

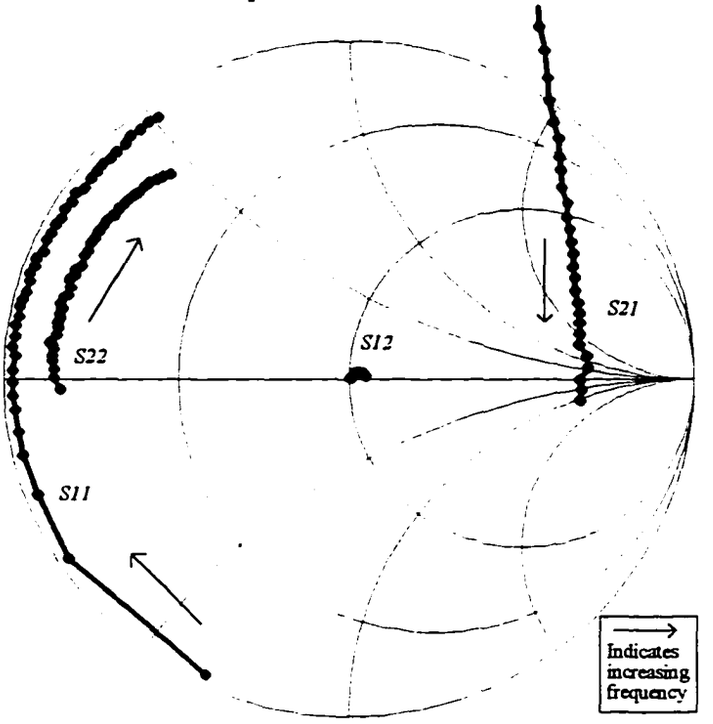



**Figure 6.8: *S* Parameters for NEC power amp**

In addition, there was no test board layout available from the manufacturer that we could use to power up and test the device. In order to verify operation of the device a printed circuit layout was developed for the NE650177.

### 6.2.1 Development of matching network

There are several problems associated with trying to match the NE6501077 input and output circuits. First, the highly reflective input and output ports must be matched to 50 Ω. Secondly, provisions for the supply current and bias voltages must be made. Finally, amplifier stability against oscillation must be maintained.

To begin the discussion on our matching network development, we will first consider the topology for the bias and supply current lines. The GaAs FET operates like any other FET. The gate voltage referenced to the source, $V_{gs}$, controls the drain current, $I_d$ . The RF input also needs to be common to the gate connection so that $I_d$ can be driven by the RF source. Because of this requirement and the fact that a DC source looks like an RF short, it is important that there be an RF block that allows the DC power to reach the gate but prevents the RF signal from traveling back to the DC gate source. Similarly, on the output side, the amplifier's DC supply current must be allowed to reach the drain of the transistor without shorting the RF output signal. These requirements led to topology shown in Figure 6.9.

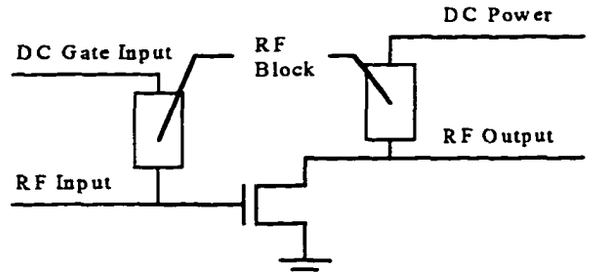



**Figure 6.9: RF power amplifier - DC bias topology**

They also led to the requirement that the DC blocking capacitors be placed between the RF output of the pre-amplifier and the RF input to the power stage. In addition, a blocking capacitor was placed between the RF output of the power stage and the antenna. These blocking capacitors prevent the gate bias voltage on the GaAs FET from shorting out the $V_{dd}$ line on the pre-amplifier. The capacitor on the output also prevents a short on the antenna from shorting out the high current supply for the GaAs FET.

This bias network addresses the DC requirements of the GaAs FET. At this point it does not meet the requirements for preventing amplifier oscillation, nor does it accomplish the task of matching the input and output to a 50 ohm system. These two tasks are inter-related in that the match to a 50 ohm system must also stabilize the amplifier at all frequencies, not just the operating frequency. To accomplish this task we looked at the S parameters of the FET. These *S* parameters are a function of frequency and are listed in APPENDIX A (as measured by NEC).

An amplifier is *unconditionally stable* if the real parts of its input and output impedances remain positive for all passive loads and sources [7]. The conditions for stability for an amplifier are [8]: $|S_{11}'|<1$ and $|S_{21}'|<1$ where

$$S_{11}' = S_{11} + \frac{S_{12}S_{21}\Gamma_{Load}}{1-S_{22}\Gamma_{Load}}, \quad S_{22}' = S_{22} + \frac{S_{12}S_{21}\Gamma_{Source}}{1-S_{11}\Gamma_{Source}}$$

and where $S_{ij}$, $\Gamma_{Load}$, and $\Gamma_{Source}$ are the associated S-parameters of the device, reflection coefficient looking into the load and reflection coefficient looking into the source, respectively. These equations indicate that the amplifier stability is a function of the device S-parameters and the match on the input and output. A stability factor, $\kappa$, can be defined as

$$\kappa = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}||S_{21}|}.$$

For $\kappa>1$ the amplifier is unconditionally stable. For $\kappa<1$ the amplifier is only conditionally stable. This means that if for any frequency $\kappa<1$, the amplifier may oscillate depending on the load and source matches. These conditions for stability can be mapped to a Smith chart, and regions of stability can be defined. These regions indicate what loads will cause the amplifier to oscillate.

Typically if an amplifier is conditionally unstable, there is a trade off between amplifier gain and stability. Gain can be sacrificed to increase stability. On the other hand if it is known that the amplifier will never experience certain values of $\Gamma_{Load}$, stability can sometimes be decreased to increase gain, while maintaining an oscillation-free operation. To illustrate this, consider a particular matching circuit and transistor with the stability

circle of the output load at a given frequency as shown in Figure 6.10 (with the region of instability being inside the shaded circle).

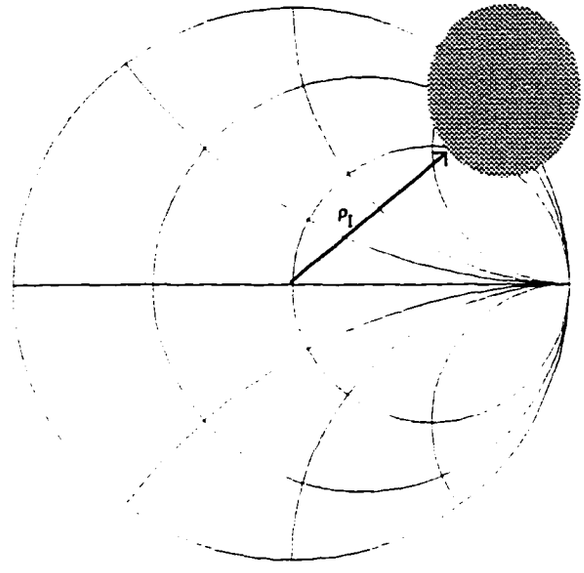



**Figure 6.10: Stability example**

If it is known that the reflection coefficient of the load will always have a magnitude less than $\rho_l$, then this amplifier will not oscillate. However, if it is possible that the amplifier will see a load reflection coefficient that will fall within the unstable region, then an attempt should be made to sacrifice the amount of gain required to push the stability circle outside the Smith chart.

This process of simultaneously matching the input and output while maintaining stability and trying to maximize gain can be tedious if done manually. Fortunately, the simulation software used for the phase shifter has the ability to use the known *S*-parameters in an algorithm which optimizes the element values in a given circuit topology. The supplied *S*-parameters for the NE6501077, Microwave Harmonica® was used to simulate the proposed

matching network. Using this software, stability circle plots can be easily viewed. Optimization options in the software allow for specifying which component values are to be optimized for several input parameters. In this case the optimization was performed for gain.

As the development progressed, it became apparent that we would not be able to get the power we needed from the amplifier and to have it be unconditionally stable. Moreover, because of the nature of the antenna array, it was recognized that it would be possible, under certain conditions, for the amplifier to see an active load. This means that if they are phased properly, other elements of the antenna could radiate back *into* an element. For these reasons it was decided that an isolator would have to be added to each channel of the array between the power amplifier and the antenna array. This would allow the amplifier to see an almost ideal load, i.e., the load reflection coefficient $\Gamma_L$=0.

In many amplifiers stub tuners are used to match the input and output. In this application, where space is an important design factor, it was not possible to use a stub tuner in the circuit with the available space. Lumped element matching was used instead. As mentioned previously, the matching circuitry must coexist with the DC bias circuitry. Keeping this in mind, with the fact that to prevent it from oscillating at low frequencies, the amplifier must 'see' a 50 ohm load on the input and output, the following key points regarding the matching circuit were addressed:

1. At low frequencies, where the DC blocking capacitors become open, the matching / bias circuit must present a 50 ohm load to the input.
2. Outside of the 2.45 GHz band, the isolator can not be relied upon to deliver a matched output load.
3. The current supplied to the drain of the FET is on the order of 4 amps, and therefore the circuit must be capable of handling large currents.

An analysis and design study was performed to address these points and led to the matching and bias network shown in Figure 6.11.

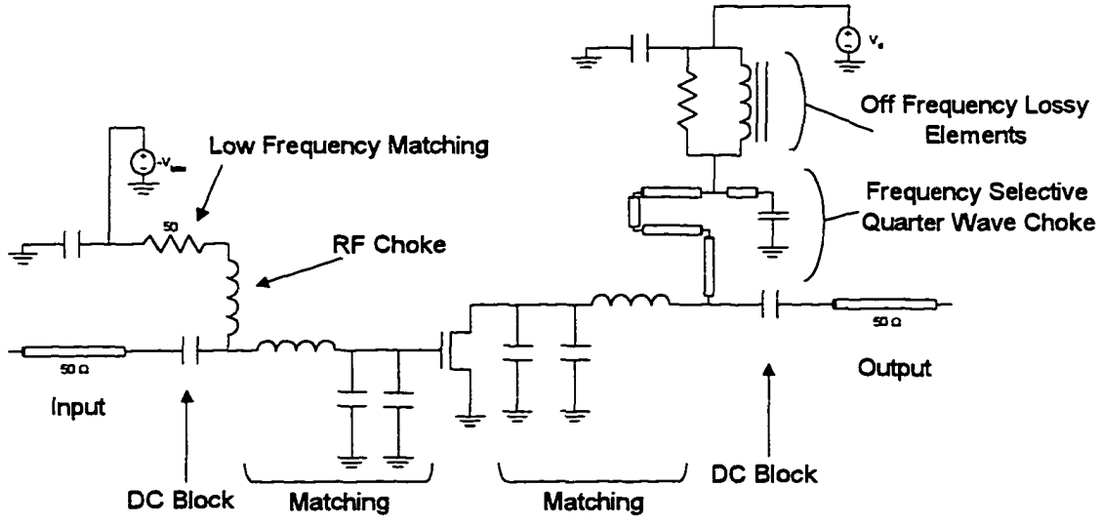



**Figure 6.11: Power amp schematic**

The matching elements for this circuit consist of two surface mount capacitors shunted to ground, with a series loop inductor. Two capacitors were used in

order that fine tuning of the effective capacitance could be achieved (i.e., standard values could be paralleled to create non-standard values). On the input side a surface mount inductor is used as an RF choke. This inductor acts only as a block at high frequencies. At lower frequencies, where the input DC blocking capacitor and this RF blocking inductor begin to become ineffective, a series 50Ω resistor presents to the gate of the FET an approximate 50Ω match which eliminates low frequency instability.

The output side of this circuit could not be biased in the same manner. Due to the high current involved, a low frequency matching resistor could not be used. A frequency selective choke scheme was used instead. At 2.45 GHz this choke is designed to present an (ideally) infinite impedance to the output line of the amplifier. At other frequencies the choke allows RF to pass to a RL tank circuit. This tank circuit is constructed so that at high frequencies the lossy inductor adds loss to the system. At lower frequencies, where the loss of the inductor is less, the resistor adds to the loss. The overall effect is that at frequencies other than 2.45 GHz, loss is added to the system, thus reducing the gain at those frequencies. This helps to ensure stability across the operating frequency range of the FET.

The simulations and optimizations for this circuit predicted the amplifier characteristics shown in Figure 6.12, indicating that the gain of the amplifier at 2.45 GHz is slightly above 10 dB. Additionally, from Figure 6.12, it can be seen that the input return loss ($S_{11}$) should be close to -10 dB. Although in most passive circuits this would not be considered a good match, trade-offs between gain, broadband stability, and input / output match made

the input match difficult to improve. Thus, after optimization attempts failed to improve the match, it was deemed acceptable.

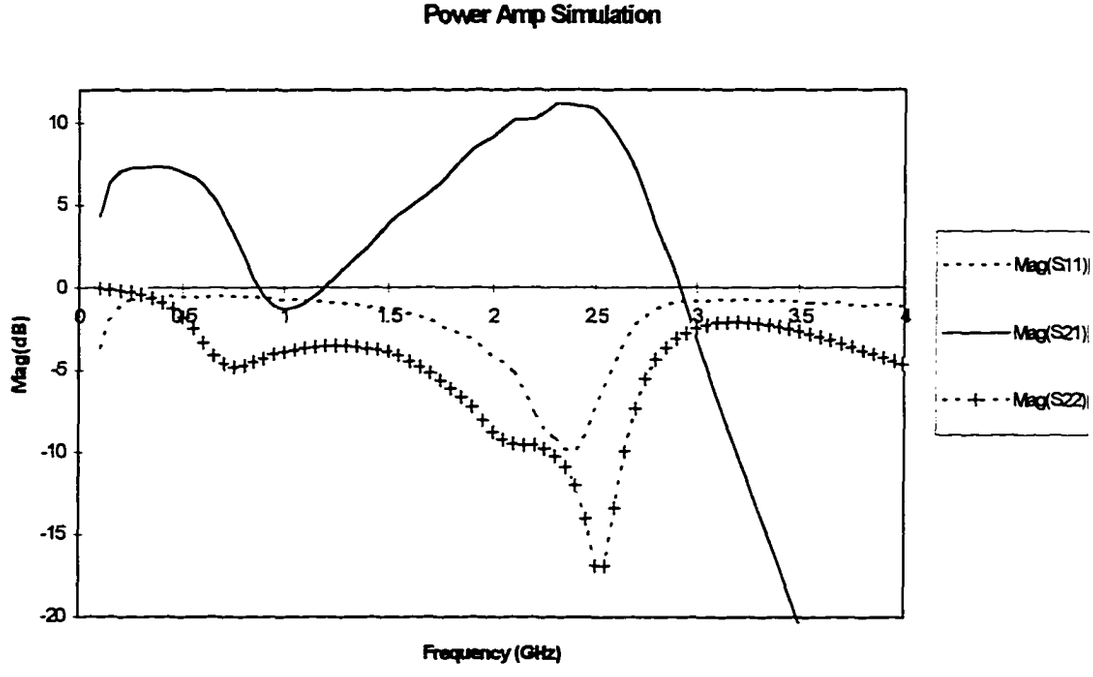



**Figure 6.12: Power amplifier simulation data**

Stability simulations of the optimized amplifier indicated that the amplifier does have a small region of instability, as observed in Figure 6.13. This situation was deemed acceptable because the output match on the amplifier would never reach these values. This behavior will be clarified further with the isolator measurement data to be presented in section 6.3.

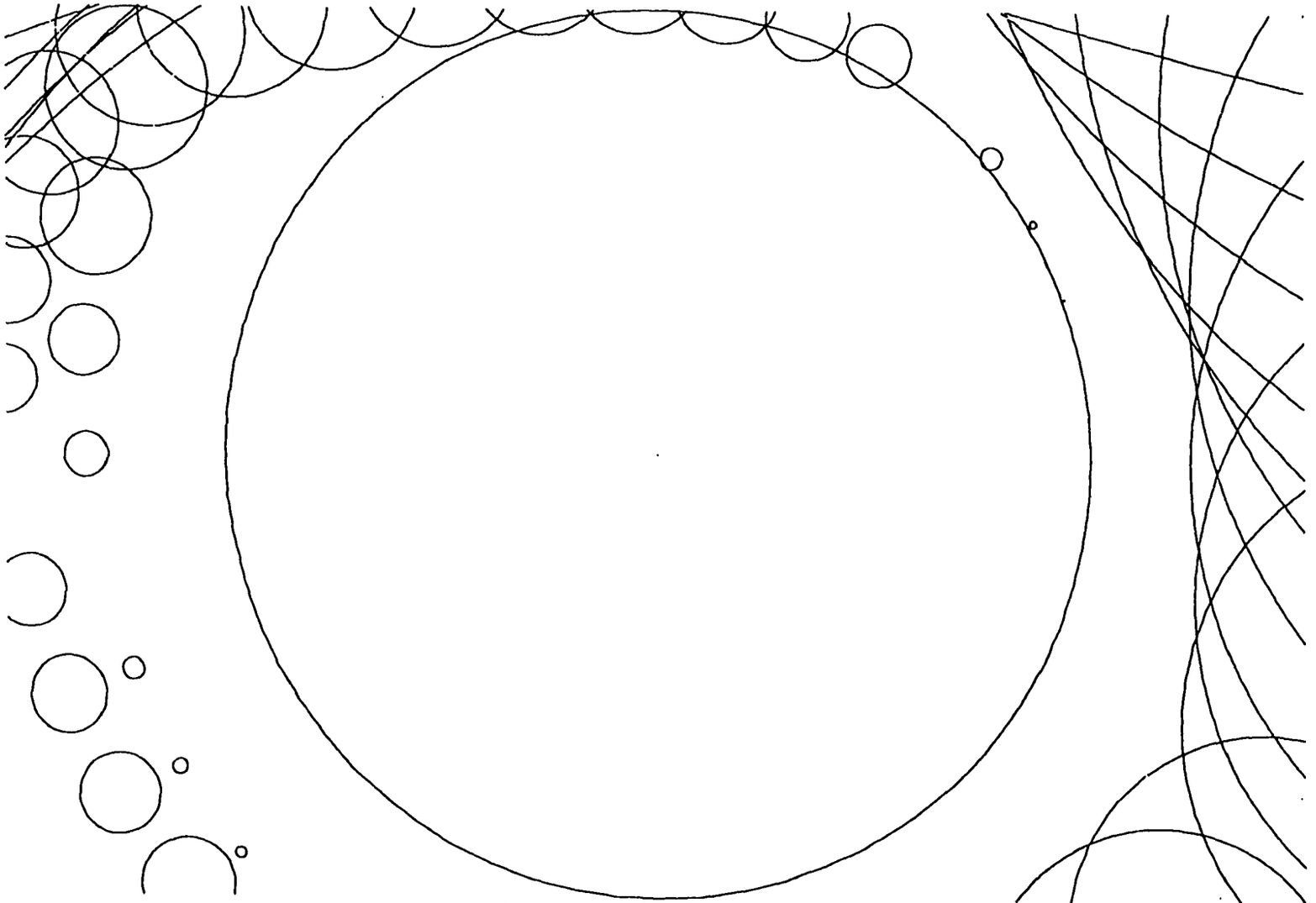


**Figure 6.13: Stability plot**

The actual, measured amplifier performance was not quite as good as the software predicted. The measured gain was approximately 9 dB with a maximum output power of approximately 39.6 dBm. This was achieved after further tweaking of the tuning capacitor values. Due to the power limits of the network analyzer, frequency sweeps of this amplifier were not made. To verify stability, a spectrum analyzer was used. The output power spectrum showed no noticeable oscillations.

Several attempts were made to adjust the circuit to produce more gain. No significant successes were made, and it is believed that the transistor was operating at or close to its maximum output power capability. It is suspected that at these power levels the device is no longer operating strictly Class A and thus the *S* parameters are somewhat different from those used in the simulation. This, along with the variations between solder joints, component values etc., likely make up the bulk of the discrepancies. Thus, 39.6 dBm was thus deemed an acceptable operating value for one channel.

## 6.3 Isolators

As discussed earlier, it was decided that isolators would be placed between the output of the power amplifier and the antenna elements. As with all of the other components in this array, the isolator footprint was a critical factor in selecting an isolator. Antenna simulations indicated that, if phased properly, the antenna array could couple as much as 9 watts into a given element. This indicated that the isolators must be able to withstand both forward and reverse powers on the order of 10 watts. One isolator, Device Technology's S526D14 (Figure 6.14), was found. This isolator met both the

power and space requirements for our application and was designed to operate at 2.45 GHz. For proper operation the device must be secured to a thermally and electrically conductive ground plane.

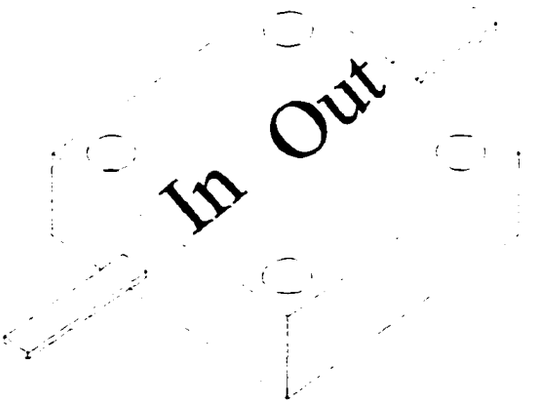



**Figure 6.14: Device Technology's S526D14 isolator**

The S526D14 isolator is a ferrite device, and as such, must not be placed near strong magnetic fields. This led to concerns about the permanent magnets within each isolator changing the operating properties of its nearest neighbor. Detailed specifications from Device Technology were required to conclude that these isolators can be mounted directly next to each other without significantly altering the characteristics of the devices.

In order to verify the operation and specifications of the isolators, a test jig was made and *S*-parameter data was taken. Although exact parameters were deemed not critical, poor isolator performance could lead to poor array operation. Measurements of isolator performance were taken. The results of these measurements are shown in Figure 6.15. All parameters were within

the manufacturer's specifications and were completely acceptable for this application.

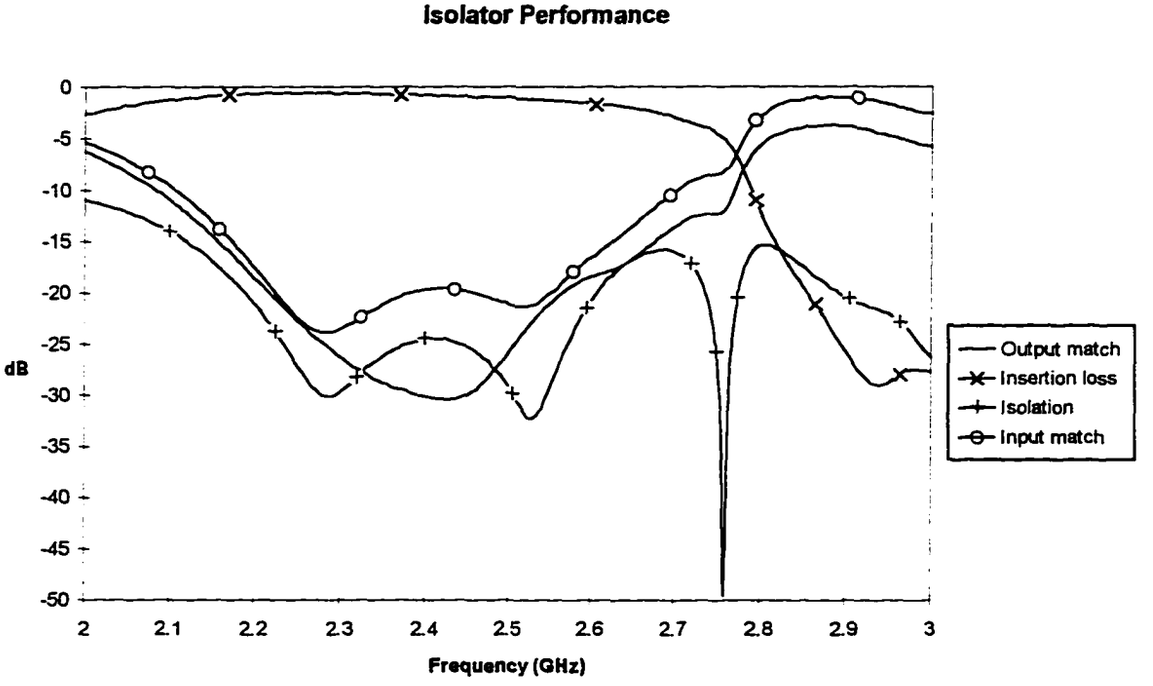



**Figure 6.15: Isolator performance measurements**

At 2.45 GHz the isolator provided 25.2 dB isolation with 0.86 dB insertion loss. This amount of isolation was more than is necessary to prevent oscillation of the power amplifier. If, in a worst case situation, 40 dBm were to couple into an antenna element from other elements, only 14.8 dBm (40 dBm - 25.2 dB) would reach the output of the power amplifier. This would appear to the amplifier as a load with a reflection coefficient. The magnitude of this equivalent reflection coefficient is:

$$\left|\Gamma_{Equivalent}\right|^2 = \frac{P_{Amp\_out}}{P_{Amp\_received}} = \frac{9.12\ \text{W}}{30.1\ \text{mW}}, \text{ or, } \left|\Gamma_{Equivalent}\right| \approx 0.06 \approx -12dB$$

From the stability plot of Figure 6.13 it can be seen that a reflection coefficient of this magnitude will never intersect a region of instability, thus, adding the isolator to the amplifier guarantees oscillation free operation over the operating range of the power amplifier.

# 7. POWER DIVIDERS

In order to provide focusing for the array, each array element must output a signal with a specified phase and amplitude with respect to a common phase reference. Our topology allowed this by having a common signal source. This signal source was the phase reference for the array. Using a single signal source required that the source be divided 73 ways, thus providing one input signal for each phase shifter / amplifier chain in the array. This division could have been made in one step using a custom designed 1 to 73-way power divider, but because the array allowed for a modular design, this method was not selected. The antenna array geometry (see Figure 3.2) allowed for 9 horizontal modules of 7, 8 or 9 channels to be constructed, as shown in Figure 7.1.

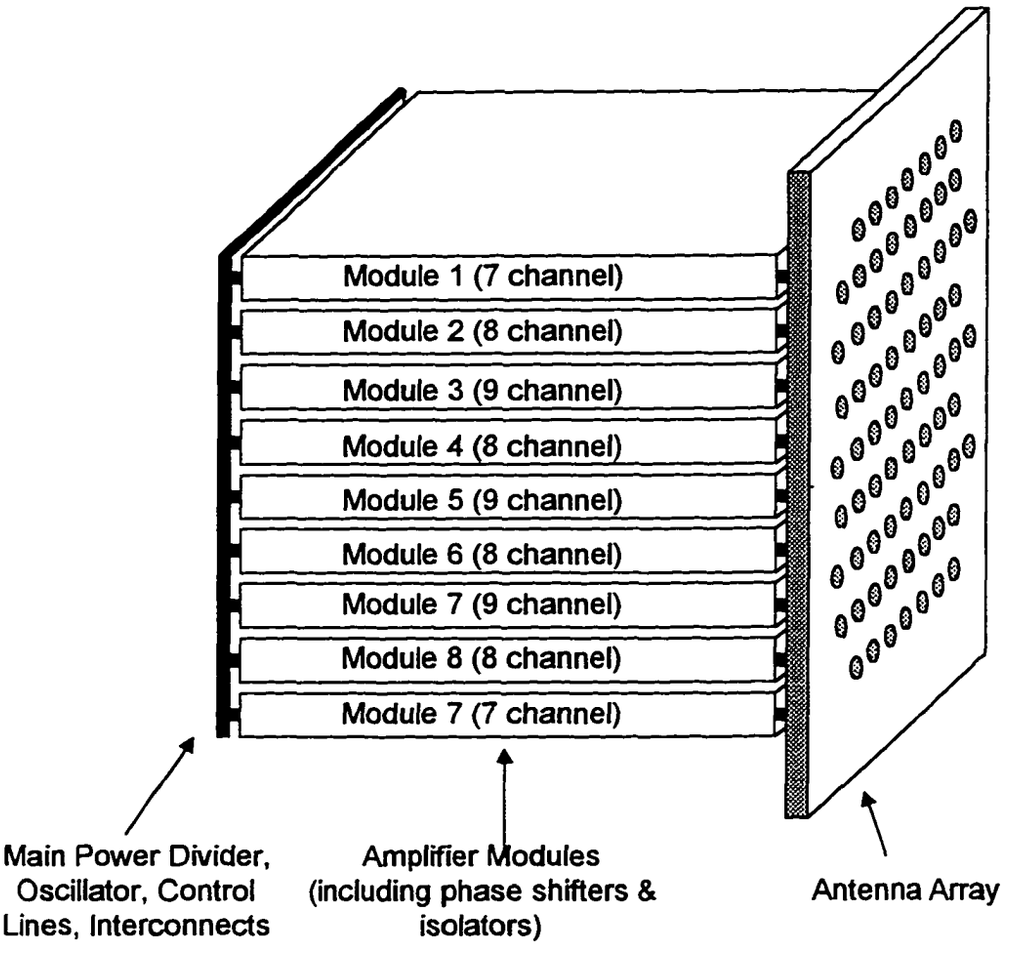



**Figure 7.1: The array, a modular design**

Using this method, one main 9 way power divider is used to divide the main oscillator output and direct it to the 9 amplifier modules. Once inside a module, this power is then split again, either 7, 8, or 9-ways, depending on the 'flavor' of the module.

For proper operation, each pre-amplifier required at least +5 dBm input power. Accounting for approximately 5 dB of loss in each phase shifter, the entire array required 27 dBm of power at the input to the main power divider. Similarly, each 9 element module required approximately 20 dBm input

power. This assumed that the power division is done equally, and that there is no loss in the power divider.

For simplicity it was decided that the Anaren hybrids would be used as elements for all of the power dividers. This would save development time by eliminating the need to custom design 1 to 7, 1 to 8 and 1 to 9-way power dividers. The design of a 3 dB splitter using the hybrid couplers was straightforward. Using one of the four ports of the hybrid as the input, the coupled and through ports became the outputs. For proper operation the isolated port was terminated in a 50 Ω match. Surface mount microwave grade 50 Ω resistors were used as terminations. The basic topology is shown in Figure 7.2.

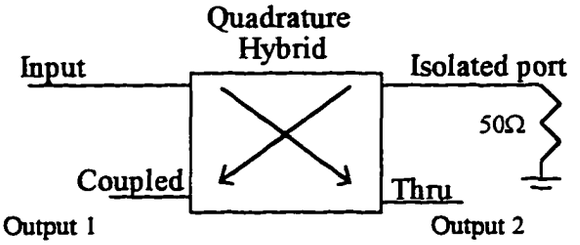



**Figure 7.2: Quadrature hybrid - use as a power divider**

Because the Anaren splitters essentially divide one input into two outputs, equal power division of an odd number of outputs was not possible. Therefore, it was decided that power attenuators would be used along with unequal power division to achieve the 7,8 or 9 equal power outputs. This unequal division brought the total power required at the input of the main power divider to approximately 29 dBm. The topology of the power division strategy is shown in Figure 7.3.

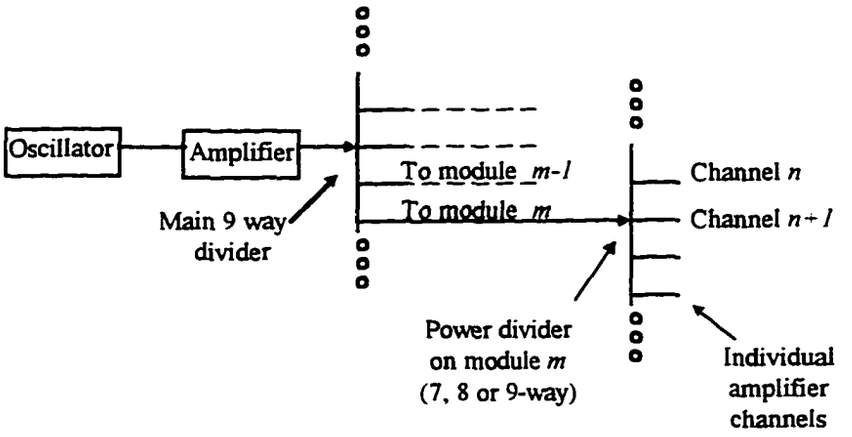



**Figure 7.3: Power dividers in the array**

A 2.45 GHz oscillator was purchased for use as the main oscillator. This oscillator outputs a stable 12 dBm 2.45 GHz signal. To produce the 29+ dBm required to power the entire array, one PM2104 is used immediately following the oscillator in combination with an attenuator to reduce the +12 dBm to around +5 dBm, the value required for the PM2104.

For the 9 element modules, a 9-way power divider was required. A natural topology for a 9-way divider using 1 to 2 splitters in each segment is shown in Figure 7.4,

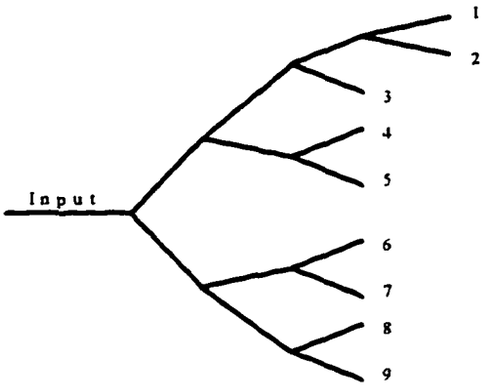



**Figure 7.4: A topology for a 9 way power divider**

where each tee is comprised of an Anaren hybrid splitter. This arrangement divides an input unequally 9 ways. In order to have all of the outputs be equal, it is necessary to attenuate ports 3 to 9. Ports 1 and 2 did not need attenuation because the input to the power divider could have been chosen to give the required 10 dBm output at these ports. It was decided, however, that to ease adjustment of the divider in the final system, attenuators would be added to all ports of the power divider. This way, if necessary, differences between individual Anaren couplers could be taken into account.

Each attenuator used in the power divider consisted of 3 surface mount microwave grade 1/4 watt resistors. The resistor values were chosen to give the appropriate amount of attenuation. The main 1 to 9 power divider distributes roughly 1 watt 9 ways. Therefore, no resistor / attenuator combination could receive more than 1/9 watt. Quarter watt resistors, which are readily available, were therefore acceptable for this power level. The topology of the resistor attenuator selected for our application is shown in Figure 7.5.

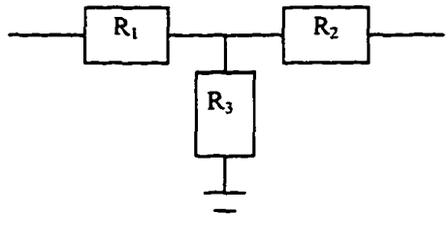



**Figure 7.5: A simple power attenuator**

Component values are selected based on 3 requirements. First, from symmetry it is clear that $R_1$ and $R_2$ must be equal. Second, the impedance

looking into either port of the attenuator must be $Z_0$ (50 Ω). The final condition is the amount of attenuation. This gives two equations and two unknowns. These two equations are:

$$10^{\frac{-\alpha}{10}} = \frac{R_3(50-R_1)}{(R_2+R_1+50)\cdot(R_1+50)} \text{ and } \frac{R_2R_1+R_2\cdot 50}{R_1+R_2+50} = 50-R_1$$

where α is the attenuation in dB. For example, if a 3 dB attenuation is needed, $R_1$, $R_2$ and $R_3$ are found to be 8.55 Ω, 8.55 Ω and 141.9 Ω, respectively.

The spacing requirements for the power splitters are significant to their design. To help reduce the length of the modules, it was decided that the power splitter for each module be placed below the phase shifters on the underside of the carrier. Additionally the power splitter board must have a trace leading from the input of the divider to the input of the module, an OSP microwave connector. Fortunately, the Anaren hybrids are completely symmetrical, allowing several orientations. The layout for the 9-way power divider & associated attenuators is shown in Figure 7.6. It was designed using a 3D computer aided design software package. Assembly of the power divider initially occurred virtually on CAD thereby allowing adjustments to be made so that all of the parts would align properly. The layout also includes mounting holes and alignment boss holes used to mount the board in the carrier.

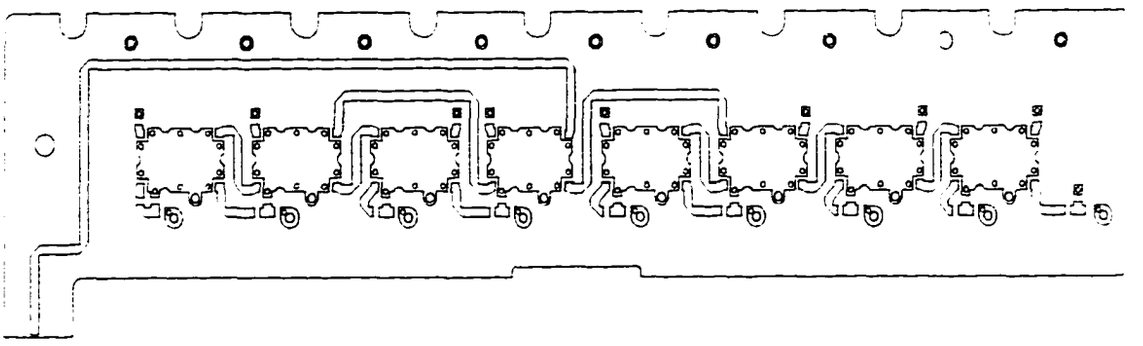


**Figure 7.6: A 9 way power divider**

The power splitters for the 7 and 8 element modules were developed in a similar manner, and were designed to meet respectively, the spacing requirements of the 7 and 8 element modules. The spacing for the main 9-way splitter is somewhat different from the spacing on the 9-way module dividers; however, the topology is similar.

Using the measured data from the Anaren couplers, a 7 way power divider was simulated to investigate the power balance between the output ports. The results of this simulation are shown in Figure 7.7. Note that for clarity only 3 coupling parameters are shown. The other parameters varied in a similar manner.

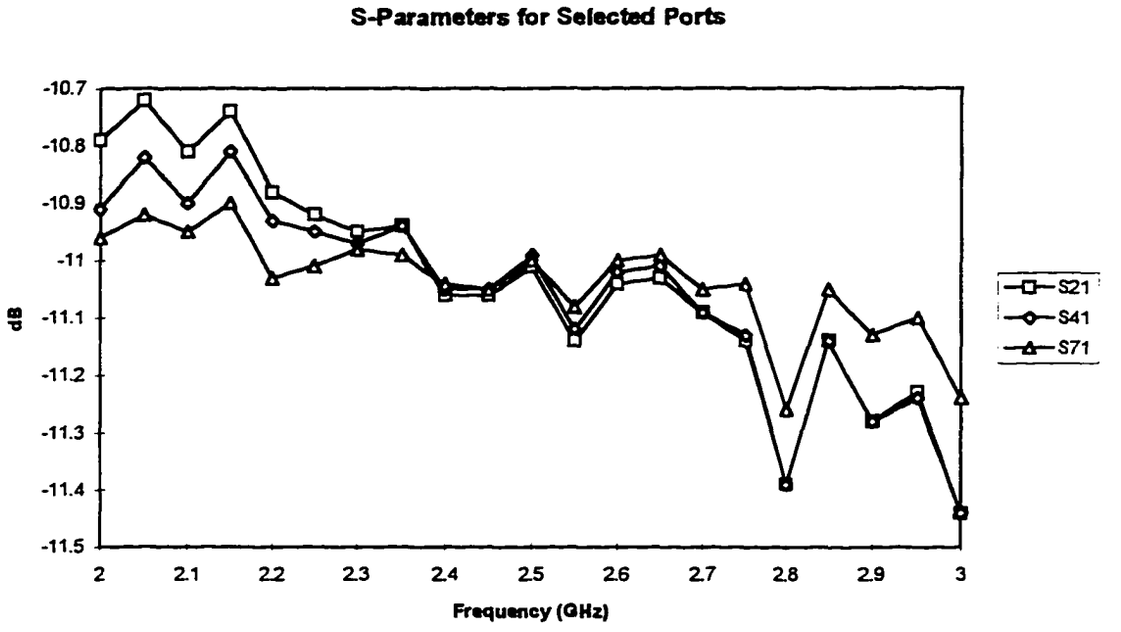



**Figure 7.7: Simulated power balance of a 7-way power divider**

This was deemed an acceptable amount of difference. It is suspected that when it is constructed, the power divider will exhibit more unbalance than the simulation indicated. However, this difference is likely to be reasonably close in magnitude to the simulated value. Any subtle difference in power levels reaching the pre-amplifiers is unlikely to alter significantly the performance of the amplifier, as has been illustrated in section 6.

With the completion of the power divider design, the microwave circuitry for the array is complete. This circuitry, which has been carefully designed to meet the spacing requirements for the array, is mounted in the array head of Figure 3.1. Some of the details surrounding this will now be discussed.

# 8. ARRAY MODULES

As shown in Figure 7.1, the 73 element array has been divided into modules containing either 7, 8, or 9 amplifier channels. This choice was made because the antenna array can be easily sectioned horizontally. For illustration the 9 channel module will be discussed.

Controlling 9 separate amplifier channels required 9 adjustable phase control lines, 9 adjustable magnitude control lines, and 2 fixed gate bias lines (one for the pre-amplifier, and one for the power amplifier). Additionally it was desired that each module have safety circuitry. This safety circuitry was designed not only to protect the array in case of failure (e.g., computer, software, power supply, broken cable etc.) but also to protect the patient being radiated. For example, without any protection circuitry, a short on the power amplifier bias line (causing $V_{gpa}$ to be 0 volts) would cause all the power amplifiers to draw maximum current. With 300+ amps available from the main power supplies, the power amplifiers (possibly all of them) would be quickly destroyed. At a cost of approximately $150 a piece, this single failure could easily cause $11,000 worth of damage. Worse yet, if a failure like this affected only several elements or modules, it could cause undesired hot spots, possibly burning the patient. Therefore it is critical that each module have sufficient circuitry to monitor system failures.

It was decided that only single level failures would be considered. That is, it was assumed that the circuitry would be designed to protect against any single failure, but not multiple varieties of unrelated simultaneous failures. The circuitry must protect against the following failures:

- Catastrophic gate / bias voltage failures on $V_{gg1}$, $V_{gg2}$, and $V_{gpa}$. These failures are defined as failures that would cause any or all of a module's gate voltages to achieve levels which result in the amplifiers being destroyed (i.e., as $V_{gx}$ approaches 0 volts, the amplifier draws more and more current until failure). Failures which would tend to shut off the amplifiers (i.e., $V_{gx}$ becomes more negative than nominal) are not considered catastrophic.

- Power supply failures that could cause the protection circuitry and gate voltages to go off line before the current producing capacity of the power supplies has faded (i.e., $V_{dd}$ goes from 10 to 8 volts, causing the derived $V_{ggl}$ and the protection circuitry to be nonfunctional while maintaining the ability to supply high currents to the power amplifiers).

Additional requirements on the drive circuitry which affected the protection circuitry design included the following:

- The only power (non signal level) voltage supplied to a module was to be +10V.
- All fixed gate voltages (i.e. $V_{ggl}$ and $V_{pa}$) were to be derived from the +10V supply.
- All protection circuitry was to be powered from the +10V supply in such a manner that it will not fail with a +10V supply

failure before monitoring circuitry could shut down the +10V supply.

- The control voltage, $V_{gpa}$'s two levels (corresponding to the ready mode and the firing mode) was to be controllable through a TTL level control line and, while in either mode, the gate was to be protected.
- A watchdog type control must exist for completely removing power from the amplifiers. This control must be hardware driven so as to require no computer intervention should a failure be detected, and should consist of relays (henceforth referred to as safety relays) which must be energized to maintain the array power.

The requirement that all gate voltages be protected led to a significant amount of circuitry. However, an efficient method for providing this protection was developed. This method involved placing a common clamping circuit on each gate voltage source, thus requiring only one diode and one resistor to be added to each gate circuit. In the event of a failure which would tend to bring a gate voltage to 0, the clamping circuit was designed to clamp that gate at a fixed negative value. This was designed to prevent damage due to an over current condition. Additionally, by adding another diode (one more, not one per channel), activation of the protection circuitry can be detected; and this information can be used to de-energize the safety relays. The resulting layout is shown in Figure 8.1.

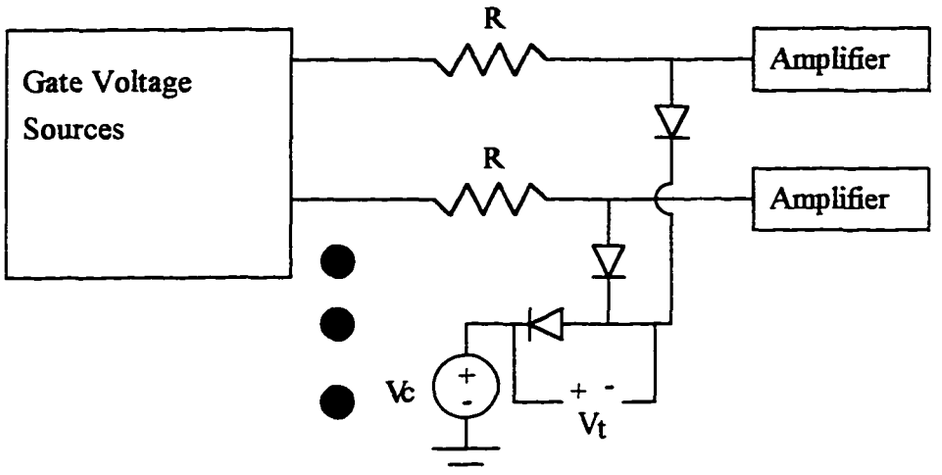



**Figure 8.1: Gate protection circuitry**

As can be seen in Figure 8.1, if a short occurs on the left side of the resistor, the clamping circuitry will act to clamp the gate voltage reaching the amplifier at $V_c+2*V_d$ volts. This will happen as soon as $V_g$ becomes close enough to 0 to forward bias both diodes. For example, if the absolute maximum voltage to be allowed at the gate input to the amplifier is -1.0 volts, then $V_c$ should be approximately -2.4 volts (for $V_d$=0.7 volts). The resistor does not affect the operation of the gate bias, as the gates have an extremely high input impedance. This impedance implies very low gate input current (D.C.) and, therefore, no significant voltage drop across the resistor *R*. The resistor, however, does limit any current through the protection circuitry when the clamping circuit is active. For instance, if the gate voltage source inadvertently became shorted to +10V, the diode clamping circuit would only

have to sink $\frac{10-V_c-2V_d}{R}$ amps, rather than some un-clampable magnitude of current.

When not active, this clamping circuit produces 0 volts across the test point, $V_t$. Upon activation, the voltage $V_t$ becomes $V_d$. A circuit monitoring this test point can detect this voltage, and can use this information to determine if the array needs to be shut down due to a gate voltage failure.

A simulation of this circuit is shown in Figure 8.2. This figure shows the voltage reaching the gate of the transistor as the drive voltage for the gate is lowered towards 0 volts. At approximately -1 volt the clamping circuitry begins to clamp the gate voltage, thus preventing the destruction of the transistor.

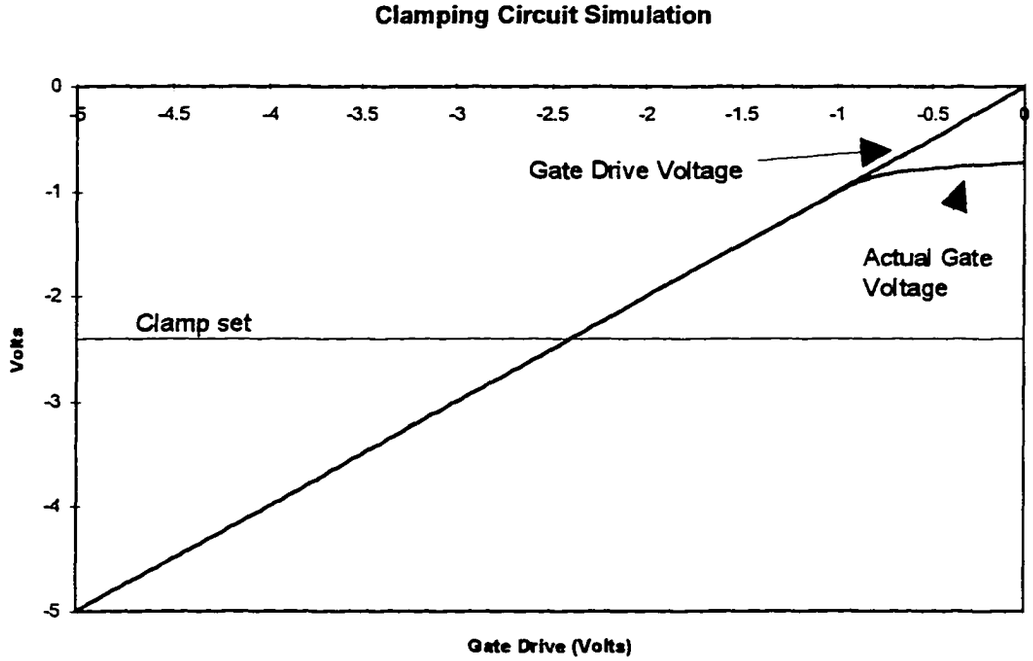



**Figure 8.2: Clamp circuit simulation**

Although this scheme had the disadvantage of not being able to detect which gate voltage failed, it had the significant advantage of only requiring two additional components per bias voltage. Schemes to determine which gate voltage failed would have required a more complicated circuit with significantly more components.

The goal of keeping gate voltages at reasonable levels during a power supply failure required additional circuitry to be added to the protection scheme. To explain the importance of this type of failure, consider the following situation. What happens if the array is functioning normally and then the AC source fails suddenly, e.g., someone trips over the power cord? The computer, which drives all the gate voltages shuts down and ceases to supply negative gate bias voltages. Next, the three 10V power supplies start to shut down. However, before they do (note that they have very large current capability for several seconds after the AC is removed), the protection circuitry goes off-line because the power supply driving the protection circuitry has already powered-down. With the gate voltages and the protection circuitry off-line, the power stored in the power supply's output capacitors is now dumped directly through the transistors, possibly destroying them.

To prevent this or any similar problem, it was decided that all the protection circuitry should be powered by the same supply as that which drives the power transistors. Additionally, this circuitry should remain functional while the 10V voltage supply ramps down. To accomplish this, DC to DC converters were needed to convert the 10V source to a negative

voltage which could be used to protect the gates of the amplifiers. This DC to DC converter could also be used to produce the fixed negative gate voltages. In this manner these voltages could be produced on each module, thereby reducing the number of external connections required. This arrangement can lead to one more possible catastrophic failure. If the DC to DC converter should fail, the protection circuitry, as well as the fixed gate voltages, would fail. This would certainly cause the destruction of all the amplifiers on the module. It was for this reason that two DC to DC converters were ultimately used, one for the protection circuitry and one to produce the fixed gate voltages. The output of all the DC to DC converters are monitored; and if one should fail, the safety relays will open. This scheme prevents any single device failure from destroying an entire module.

In addition to the microwave circuitry, this circuitry is contained in each of the 9 modules. These modules had to have a physical structure to support all of the circuit boards. These structures, which were designed using the 3D CAD software previously mentioned, were each machined from a single slab of stress relieved aluminum. Some of the details of the design will be discussed in the next section.

## 8.1 Carrier design

A sturdy, lightweight structure was needed to contain the circuitry associated with a 9 channel module (8 or 7 in the cases of the other 'flavors' of modules). Because the modules fit against the array in a stack-like configuration (see Figure 7.1), a card rack scheme, somewhat like the cards in

a PC, was used in the design. Therefore each carrier was designed to have slide rails which would align it in the rack, as shown in Figure 8.3.

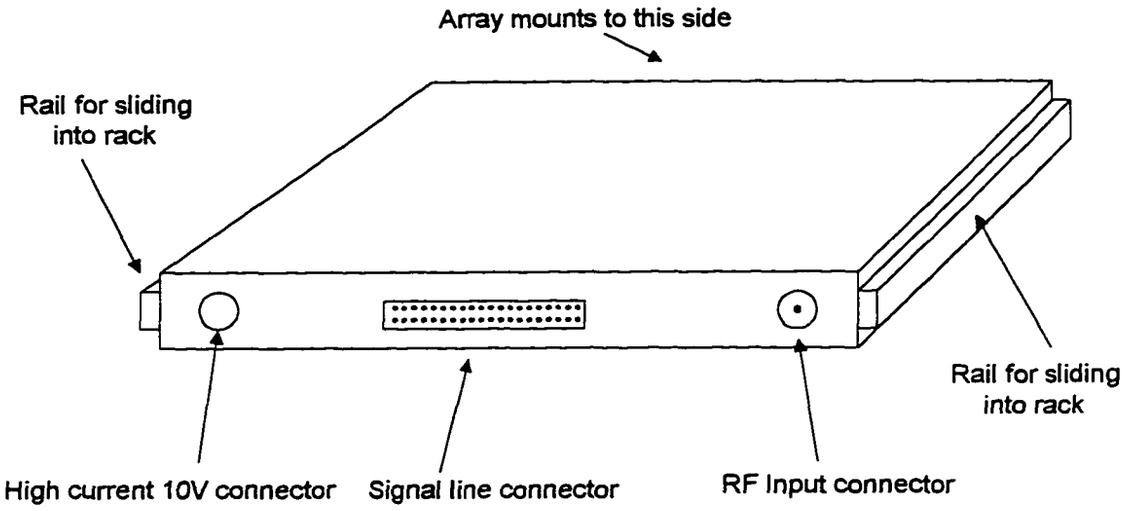



**Figure 8.3: Rack mount carrier**

Because there are 7, 8, and 9 channel modules, there had to be 2 types of carriers, each designed to contain the array circuitry aligned with the row of patches on the antenna. Note that the 7 and 9 channel carriers are exactly the same, except that when assembled as a module, the 7 channel contains two fewer channels.

As mentioned previously, the horizontal spacing between each channel is fixed at 0.719". The vertical spacing requirement leads to a maximum carrier height of 0.62". Because these carriers need to slide in and out of the rack, their height was limited to 0.6" with a 0.008" top and bottom cover (leaving a 0.007" clearance).

Although there was no defined limit on the depth of the carrier (along the axis of the amplifier chain), it was desired to keep this dimension to a

minimum. Keeping the carrier, and thus, the array head, as short as possible helps maintain physical manageability for the operator of the device.

As was briefly mentioned in sections 5 and 7, the phase shifters and the power dividers are located on circuit boards underneath the preamplifier, as shown in Figure 8.4. The metalization on the bottom of the power divider board, which was necessary for the transmission lines on it, also acted as a metal cover for the phase shifter. This conducting cover was in close proximity to the transmission lines and components of the phase shifter. Thus, as discussed in section 5, the phase shifter had to be tweaked to compensate for the electrical effects of this cover. A coaxial line feeds the signal from the bottom side of the carrier (output from the phase shifter) to the topside (input to the amplifier chain). A 1 mm thickness of metal was maintained as the ground plane and the support between the amplifier circuit board and the phase shifter board underneath. This fixed the location of the RF input to the module.

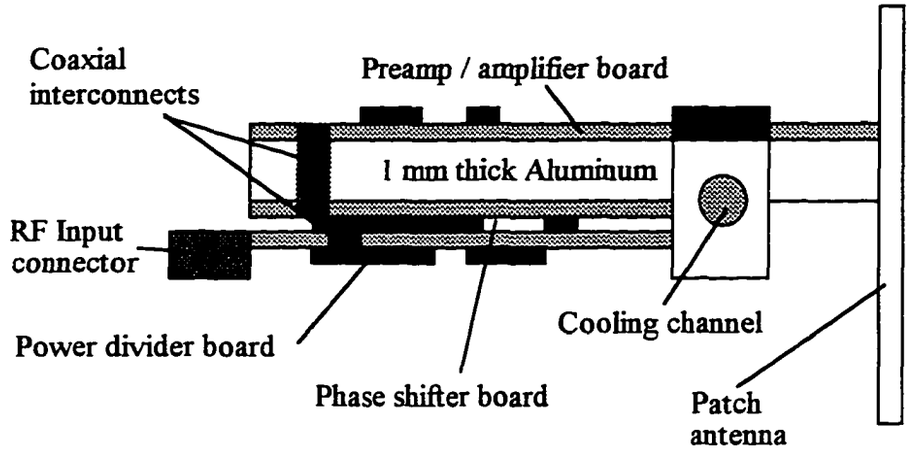



**Figure 8.4: Assembly cross section**

Figure 8.5 shows a 3 dimensional view of the carrier, including the isolation fins discussed in section 6. This figure also demonstrates the complexity of the design. Note that it does not show the mounting for the backplane which contains the safety relays, protection circuitry and signal interconnects. The inclusion of this board will now be addressed.

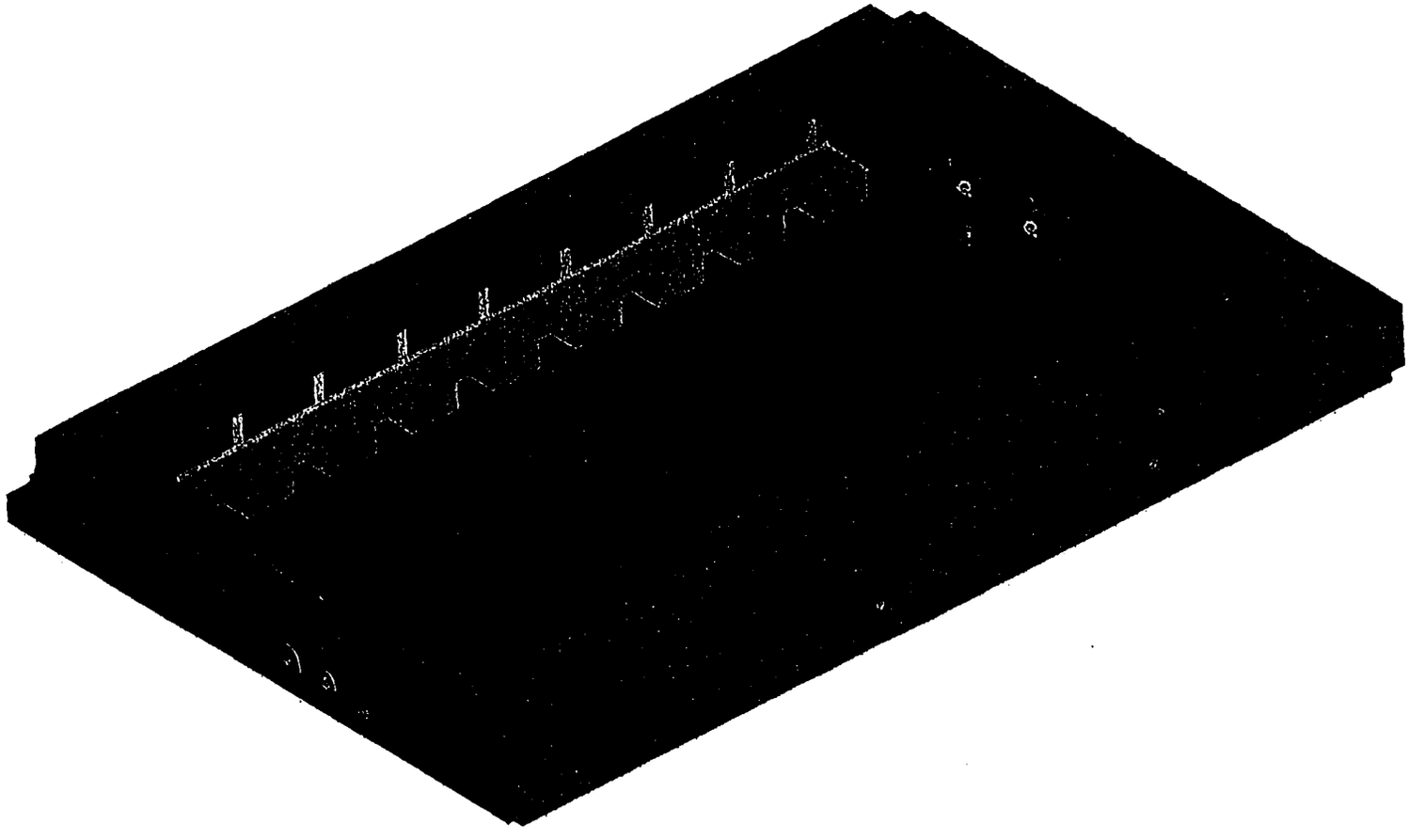


**Figure 8.5: Three dimensional view of the carrier**

## 8.2 Layout of the backplane

As mentioned previously, space is extremely tight in the array modules. The protection circuitry, fixed gate circuitry, stand by/ready control circuitry, safety relays, DC to DC converter and the preamplifier voltage regulators had to fit on a backplane in the module. The space requirements were: a maximum board height = 0.58" and a maximum board width = 7.5". To produce a board layout we found it necessary, because of the space restrictions, to again draw all of the electrical parts in 3D modeling software. We then virtually assembled the backplane in the carrier before actually building the circuit board. In this manner the components could be placed so as to not interfere with each other. The carrier design could then be modified around the circuitry. This design process also allowed for the surface mount connectors, which connect the amplifier sections to the backplane, to be properly placed with respect to the carrier and the amplifier chains.

A rendered three dimensional drawing of the backplane board is shown in Figure 8.6. Connections on the back side of this board connect the module's circuitry to the main array backplane (see Figure 7.1) and then to the array control computer. The digital circuitry necessary to drive all the control lines will be discussed in section 9.

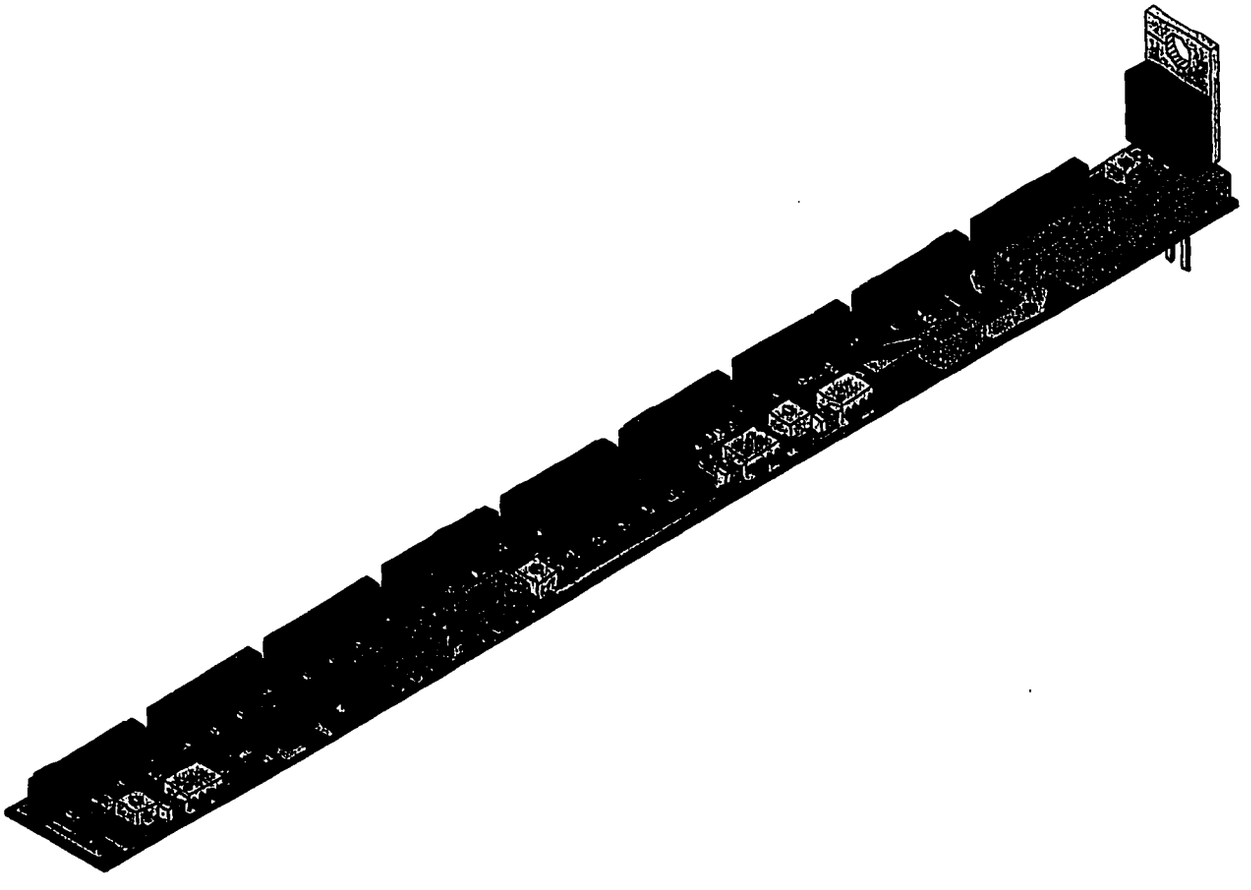


**Figure 8.6: A three dimensional view of the backplane**

# 9. DIGITAL CONTROL CIRCUITRY

The circuitry required to control the array had several requirements. First, the circuitry had to provide two analog signals for each channel. One of these signals was used for the bias line on the phase shifter. The second was used to control one of the bias lines on the preamplifier and, thus, was used to control the output power of the channel. As mentioned previously, the preamplifier has two bias control lines. Fortunately, we found that, one of these lines could be a fixed voltage and could be used to drive all of the $V_{gg1}$ preamplifier lines. With this design the complexity of the drive circuitry was reduced by only requiring one computer adjustable control per preamplifier. Therefore a total of 146 computer controllable analog signal lines had to be produced. These analog lines were produced using a D-to-A converter. It was decided that the controlling line for the preamplifiers should have at least an 8 bit (256 level) resolution; and that in order to achieve better than 1° phase resolution, the phase control line should have 9 (512 level- 0.7°) bit resolution.

To accomplish this task, an address and data bus scheme was developed. The topology of the system is shown in Figure 9.1.

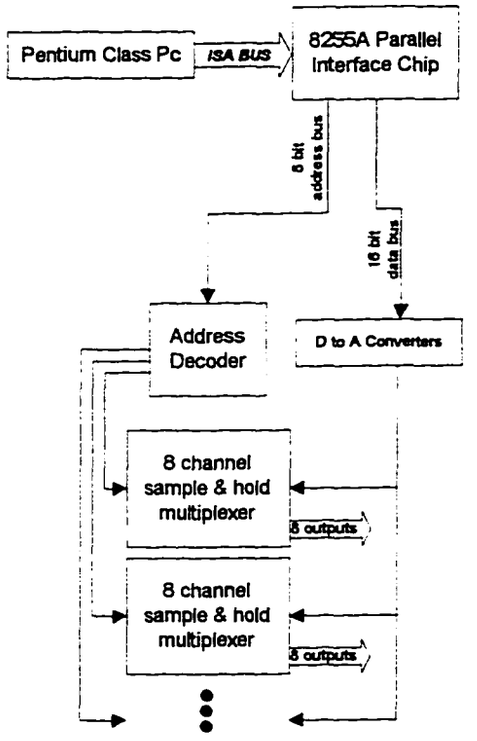



**Figure 9.1: 160 Channel ISA D/A converter**

This topology allows many devices to be attached to an address bus, each performing a specific operation. To produce seventy-three 8 bit analog outputs, ten 8 channel sample and hold multiplexers were used. These chips contained 8 buffered amplifiers that, when addressed and enabled, sampled an input voltage and presented that voltage on the selected output channel. By incrementally writing each channel's address on the address bus and providing a data word to drive the D-to-A converter, each channel of all the multiplexers could be programmed. The multiplexed outputs can maintain the programmed voltage for several seconds. However, they must be refreshed periodically, much like dynamic ram. To produce the seventy-three 9 bit

analog signals, the same bus system was used, except that the input to the multiplexers came from the 9 bit D-to-A converter rather than the 8 bit D-to-A converter. After designing this topology, we decided to use a 10 bit D-to-A converter for both the phase and amplitude control lines. The resolution was not required. However, the availability, low cost, and the fact that no significant extra circuitry was needed to drive a 10 bit D-to-A converter, made the design decision a reasonable choice. This also allowed for the extra analog lines to be used for other purposes which could require more than 9 bit resolution. Seven of these 'extra' analog lines are available, due to the fact that the multiplexers each produce 8 outputs. Therefore, to produce at least 73 outputs, ten chips were necessary. This left seven outputs unused.

Using a similar address scheme on a second ISA PC card, analog to digital (A-to-D) converters could be sampled. These A-to-D's monitored system critical parameters such as coolant temperature and power supply voltages and currents. They were implemented using the Burr-Brown ADC80MAH-12. This A-to-D system uses multiplexed chips similar to those in the other PC card. However, MOSFET buffers were used to increase the impedance of each measurement channel. Overall the card was designed to provide 12 bit (4mV) resolution over a ±10V range. Measurements of the final card verified this design.

Other addresses on the card accessed control ports and error reporting ports. The control ports allowed the computer to control the power supplies, relays, and fixed gate voltages for the array. For example, the data bits $D_0$ - $D_2$ of port address 643 control each of the three 100 amp power supplies.

Writing a logic 1 to $D_0$, the lowest order data bit, of this port would turn on power supply number one. Similarly writing a logic 1 to $D_3$ of the same port would cause the array safety relays to energize, thus turning on power to the array.

The error reporting ports functioned in a similar manner. In the event of a system failure, say a power amplifier gate voltage failure, the monitoring hardware was designed to open the safety relays on the array modules, and to immediately power down the array. This error would then be reported in one of the error reporting ports. The computer, upon sensing the failure, could then read the error ports to determine what kind of failure caused the array to shut down.

Through the control card the computer also had the ability to monitor the temperature of each module. A cooling scheme was designed for the array, and like all aspects of the array operation, this cooling system was designed to be controlled by the PC card discussed in this section. In section 10, this cooling system will be discussed in more detail.

# 10. ARRAY COOLING

Seventy-three amplifier channels operating simultaneously presents a significant cooling issue. As discussed previously, while in operation the power stage of each amplifier can draw up to 4 amps. Running between 25 and 50% efficiency resulted in each power amplifier dissipating approximately 20 watts of heat. Additionally, each preamplifier dissipates approximately 1.5 watts. Therefore, an array cooling system which could dissipate approximately 1570 watts (21.5*73) had to be designed. Due to the limited physical size of the array, it was not possible to air cool the array. Therefore, a water cooling system was devised. Each carrier was machined with a water pipe beneath the power amplifiers as shown in Figure 8.4. This cooling channel also cooled the preamplifiers by conduction through the aluminum carrier. Using heat transfer equations it was determined that between 1 and 2 gallons of water per minute were needed to maintain a reasonable temperature at the array.

A chiller was added to remove heat from the water circulating through the array. Computer control of the water temperature leaving the chiller was desired. By controlling the chiller it was possible to operate the array at a constant temperature. This was desired to help maintain stable device characteristics. Additionally the chilled water was used to cool the antenna in contact with the patient. Hence, control of this temperature aided in the comfort of the patient.

Unfortunately cooling units with computer control built-in were significantly more expensive than those without, so a retro-fit was devised. A

standard water chilling unit was purchased. The mechanical thermostat was removed from the compressor control circuit and an electronic control circuit was installed. The circuit was designed to meet the following requirements: allow computer or manual control of the temperature of the water leaving the chiller, provide a readout displaying either the set temperature or the read temperature, and provide an adjustable hysteresis for the cycle-on cycle-off control of the compressor. In order to achieve these specifications, we designed the circuit shown in Figure 10.1.

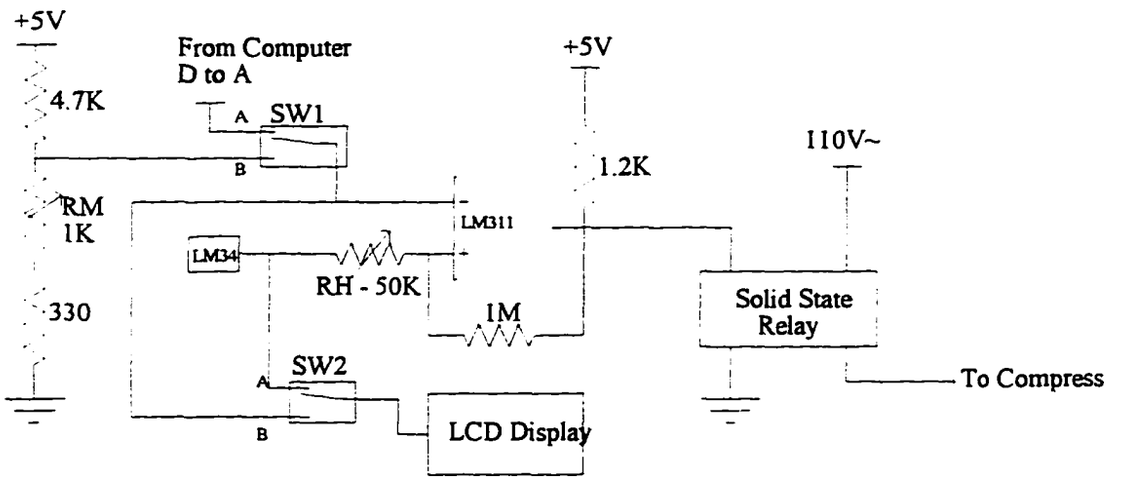



**Figure 10.1: Temperature control circuit**

The circuit operates as follows. If manual operation was desired, switch *SW1* was set to position *B*. The voltage thus applied to the inverting input of the LM311 comparator was a function of the potentiometer *RM*. The voltage divider around *RM* allowed the manual 'set' voltage to be in the range from 328mV to 1.10V. The LM34 was a temperature sensor which produced 10mV/°F. This signal was applied to the positive input of the comparator. If

the measured temperature exceeded the set temperature, the output of the LM311 was designed to become 5V. This 5V signal was then used to turn on the compressor via a solid state relay. When the water returns to a temperature below the set point, the compressor was designed to turn-off. By switching *SW1* to position *A*, the 'set' voltage was derived from a D-to-A converter on the computer control board. This system thus provided computer control of the water temperature. The switch *SW2* controls the LCD Display. The LCD display module displayed the value of an input voltage. By placing *SW2* in position *A*, the system was designed to allow the user to read the temperature of the output water. Similarly by placing *SW2* in position *B* the user could read the current 'set' temperature. Finally, by adding positive feedback to the circuit through *RH* and the 1 MΩ resistor, hysteresis was added to the temperature circuit. By adjusting the potentiometer *RH*, the amount of hysteresis in the control loop could adjusted. This way, if the set temperature was, say, 70° and there was a 20mV hysteresis, the compressor would turn-on when the water temperature reached 71°; and, moreover, would not turn off until the water temperature was 69°.

With the implementation of computer control of the water temperature, complete control of all array operational parameters was accomplished. Software to control these operations is under development.

# 11. CONCLUSIONS

Significant progress toward the construction of this active hyperthermia array has been made. All the major pieces have been designed and tested, and are now in the process of being constructed. Before the array can be powered up for the first time, software must be developed to control the array. This will be a significant time investment. Additionally, a calibration cycle, which will provide the channel specific information needed to allow proper phasing and amplitude control, will be needed. This will be a tedious task, involving making $S_{21}$ measurements for each channel at every phase and magnitude setting. This data will have to be processed and a scheme for efficiently sorting the data to determine parameter settings for a given phase and magnitude output, will have to be developed.

Several significant issues with regard to the microwave circuitry have been noted. First and probably most important, 'everything counts' when dealing with microwave circuitry. Specifically one can not assume that solder joints and interconnects do not matter. In many instances devices completely failed due to a faulty solder connection. Adding a cover, moving a trace, or changing part layout are all bound to have a greater than expected impact on the circuit operation.

Second, a systematic approach to design will yield the quickest final results. Initially we went through many design cycles on several parts because we neglected details. Later we discovered that by carefully measuring each component, then using the simulator with the measured data to arrive at an initial design, better prototypes were obtained. Tweaking was

always necessary. Nonetheless, with a systematic approach, the tweaking can be done in a much easier and more efficient fashion. If all the data was available to the simulator, one could reliably make simulations to aid in tweaking the component values.

Finally, never assume components are the value the manufacturer claims they are. It was expected that resistors and capacitors would not behave as ideal elements. However the extent of this problem was not realized early on. The simulators will have 'ideal' components, but it is best not to use them. We found that it was better to assign each circuit element either measured parameter data, or at least attempt to model the element's parasitics. Some devices (like the diodes) were measured 'on wafer' and then assigned a package inductance. This can be misleading and can lead to poor choices in components. This goes back to the systematic approach. Measuring each component initially takes time, but in the long run will save a significant amount of time and hassle.

Future efforts on this project will be devoted mainly to completing the assembly of the system. Concurrently with the completion of this task, software will be developed to provide control for the array. This software will also have the task of providing a user friendly interface to the array. This interface will allow medical professionals, unfamiliar with the details of the array hardware, to use the system. With the interface in place, we will be faced with the task of proving the physiological benefits of the system.

Should the physiological data be positive, efforts to refine the system will be made. Specifically, more work on size reduction will be done. This

size reduction may be accomplished by increasing the frequency of operation. This would allow smaller antenna patches and devices; however it would dramatically increase the effects of the parasitics in the system and the difficulties associated with designing around those effects. Finally, it may be possible to further reduce the size of the system by using unpackaged devices wirebonded together on a substrate, or by building phase shifters and amplifiers on custom integrated circuit die. These possibilities may be costly to develop, but may significantly reduce cost in a mass produced device.

# 12. APPENDIX A

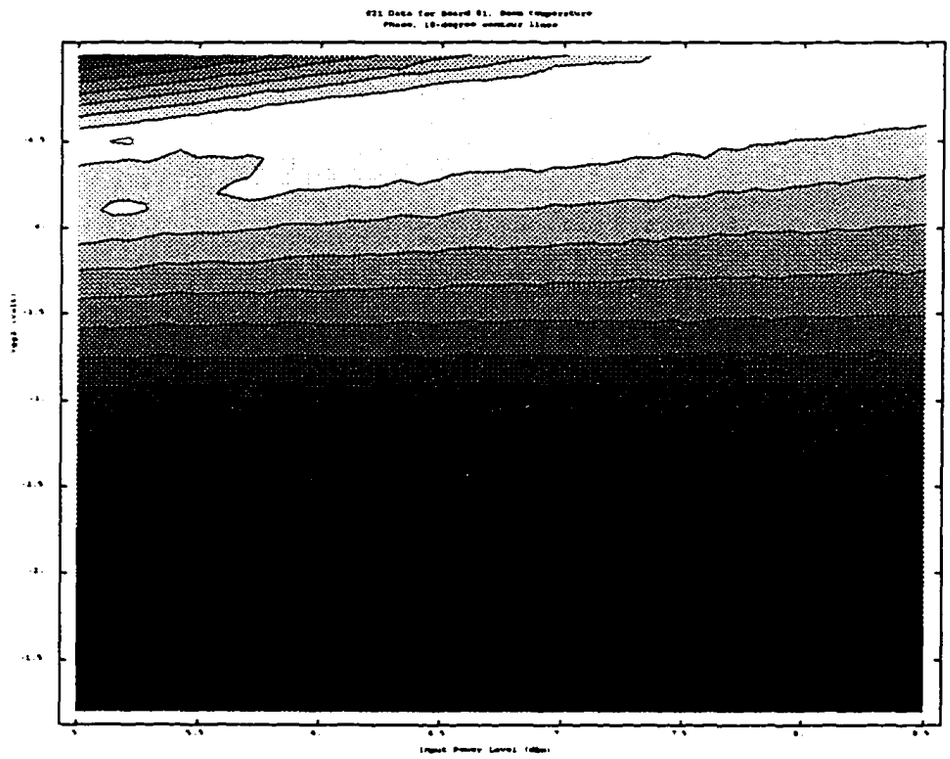
Manufacturer specified *S* parameters for the NEC NE6501077.

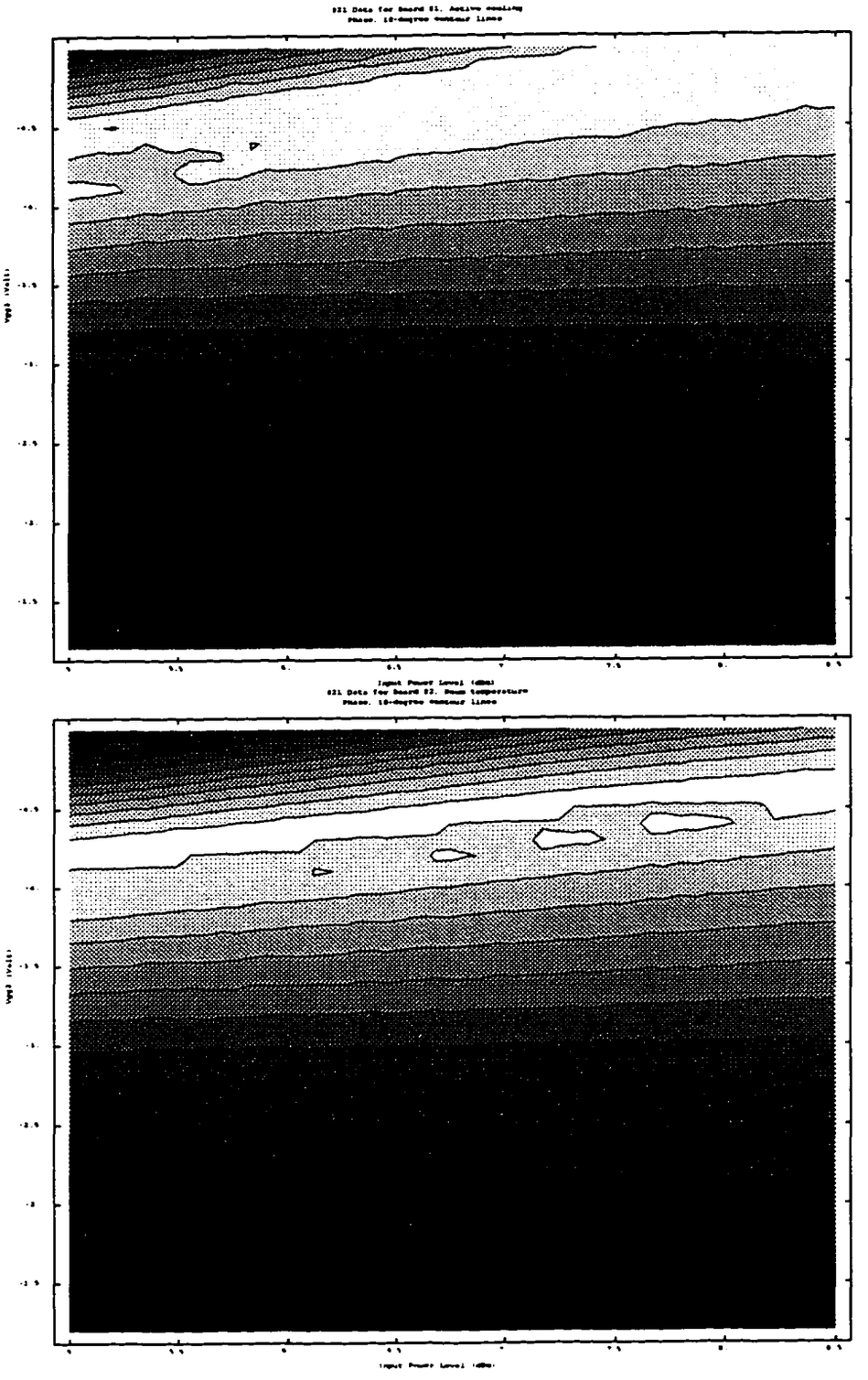
| Freq. | Mag(S11) | Arg(S11) | Mag(S21) | Arg(S21) | Mag(S12) | Arg(S12) | Mag(S22) | Arg(S22) |
|---|---|---|---|---|---|---|---|---|
| 100MHz | 0.971 | -115.5 | 12.812 | 120.5 | 0.005 | 33.6 | 0.835 | -178 |
| 200MHz | 0.97 | -146.6 | 7.272 | 103.1 | 0.007 | 19.6 | 0.854 | 179.6 |
| 300MHz | 0.962 | -159 | 4.953 | 95.5 | 0.008 | 22.5 | 0.854 | 178.1 |
| 400MHz | 0.97 | -166.4 | 3.796 | 90 | 0.008 | 21.7 | 0.86 | 176.4 |
| 500MHz | 0.968 | -170.6 | 3.051 | 86.7 | 0.009 | 25 | 0.86 | 175.5 |
| 600MHz | 0.968 | -174.6 | 2.562 | 83 | 0.009 | 26.9 | 0.858 | 174.1 |
| 700MHz | 0.973 | -177.1 | 2.222 | 80.5 | 0.009 | 31 | 0.863 | 173.4 |
| 800MHz | 0.972 | -179.5 | 1.972 | 77.8 | 0.01 | 33.2 | 0.872 | 173 |
| 900MHz | 0.973 | 178.5 | 1.752 | 75.3 | 0.01 | 33.7 | 0.857 | 171.4 |
| 1000MHz | 0.968 | 176 | 1.583 | 72.1 | 0.011 | 34.4 | 0.854 | 169.9 |
| 1100MHz | 0.977 | 174.5 | 1.46 | 69.7 | 0.011 | 34.6 | 0.859 | 169 |
| 1200MHz | 0.972 | 172.6 | 1.348 | 67.3 | 0.012 | 36.6 | 0.855 | 167.9 |
| 1300MHz | 0.977 | 170.8 | 1.261 | 64.7 | 0.013 | 39.4 | 0.859 | 167.1 |
| 1400MHz | 0.971 | 169.2 | 1.176 | 62.3 | 0.013 | 40 | 0.854 | 166 |
| 1500MHz | 0.976 | 167.4 | 1.121 | 59.9 | 0.014 | 38.9 | 0.864 | 165.1 |
| 1600MHz | 0.973 | 166.1 | 1.057 | 57.3 | 0.015 | 40 | 0.858 | 163.6 |
| 1700MHz | 0.967 | 164.7 | 1.004 | 55.1 | 0.015 | 41.7 | 0.849 | 163 |
| 1800MHz | 0.965 | 162.7 | 0.961 | 52.2 | 0.016 | 40 | 0.849 | 161.5 |
| 1900MHz | 0.972 | 161.4 | 0.932 | 49.7 | 0.017 | 41.5 | 0.859 | 160.2 |
| 2000MHz | 0.968 | 159.9 | 0.891 | 47.3 | 0.018 | 43.3 | 0.849 | 158.9 |
| 2100MHz | 0.972 | 158.7 | 0.867 | 45.3 | 0.019 | 42.2 | 0.853 | 158 |
| 2200MHz | 0.961 | 157 | 0.832 | 42.7 | 0.021 | 39.9 | 0.842 | 156.6 |
| 2300MHz | 0.966 | 155 | 0.815 | 39.5 | 0.022 | 39.3 | 0.847 | 154.7 |
| 2400MHz | 0.962 | 153.5 | 0.789 | 37.3 | 0.023 | 38.5 | 0.846 | 153.5 |
| 2500MHz | 0.963 | 151.9 | 0.774 | 34.8 | 0.024 | 38.3 | 0.848 | 152 |

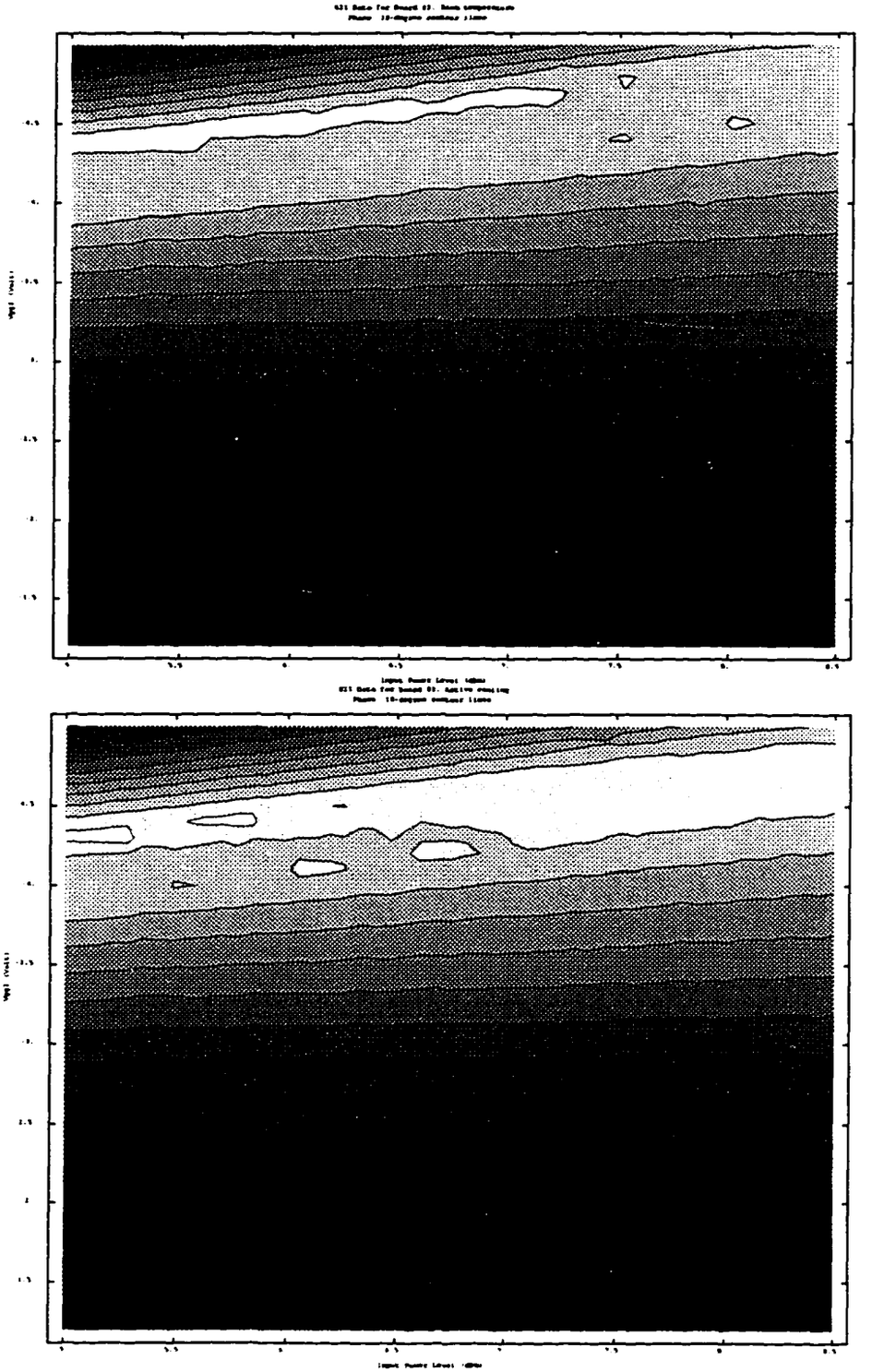
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 2600MHz | 0.958 | 150.3 | 0.756 | 32.3 | 0.026 | 35.6 | 0.845 | 150.6 |
| 2700MHz | 0.961 | 148.6 | 0.743 | 29.8 | 0.027 | 33.9 | 0.846 | 149.2 |
| 2800MHz | 0.957 | 146.9 | 0.726 | 27.1 | 0.028 | 31.3 | 0.843 | 147.6 |
| 2900MHz | 0.962 | 145.3 | 0.717 | 24.6 | 0.03 | 31.9 | 0.844 | 146.4 |
| 3000MHz | 0.952 | 143.7 | 0.701 | 21.7 | 0.031 | 29.2 | 0.836 | 144.8 |
| 3100MHz | 0.954 | 141.7 | 0.697 | 18.7 | 0.033 | 28.9 | 0.836 | 142.9 |
| 3200MHz | 0.953 | 140 | 0.691 | 16.2 | 0.034 | 26.3 | 0.833 | 141.6 |
| 3300MHz | 0.955 | 138.5 | 0.684 | 13.9 | 0.036 | 25.5 | 0.833 | 140.4 |
| 3400MHz | 0.951 | 136.9 | 0.677 | 11.3 | 0.038 | 24.3 | 0.827 | 139.1 |
| 3500MHz | 0.953 | 135.3 | 0.671 | 8.5 | 0.039 | 22.5 | 0.824 | 138 |
| 3600MHz | 0.951 | 133.2 | 0.688 | 5.4 | 0.041 | 20.3 | 0.824 | 136.4 |
| 3700MHz | 0.958 | 131.7 | 0.688 | 2.8 | 0.044 | 18.6 | 0.823 | 135.3 |
| 3800MHz | 0.954 | 129.7 | 0.666 | -0.3 | 0.047 | 15.2 | 0.814 | 133.7 |
| 3900MHz | 0.957 | 127.8 | 0.671 | -2.7 | 0.049 | 13.3 | 0.808 | 132.3 |
| 4000MHz | 0.953 | 125.9 | 0.669 | -5.4 | 0.051 | 10.9 | 0.799 | 131.1 |

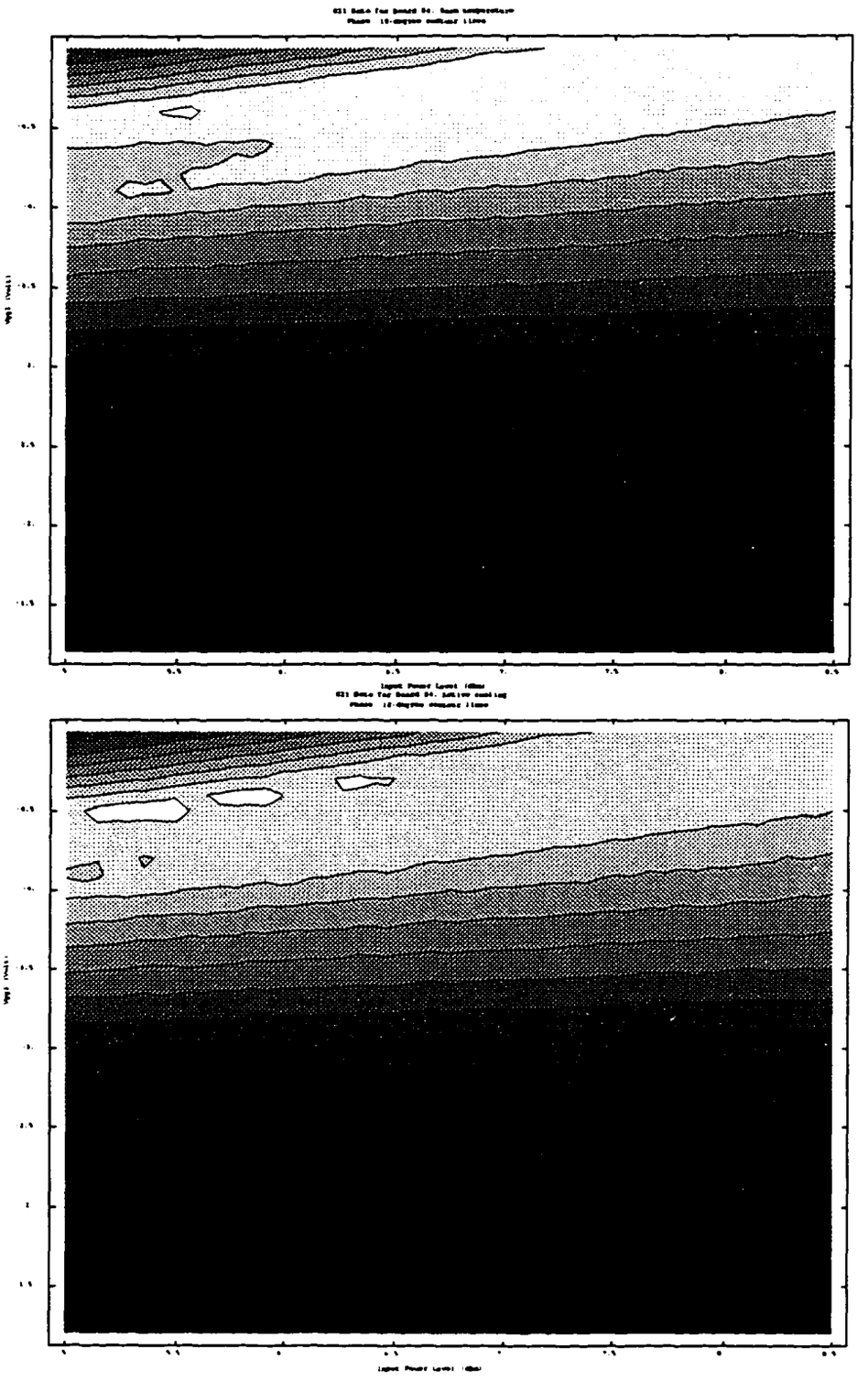
# 13. APPENDIX B: PRE-AMPLIFIER MEASUREMENTS

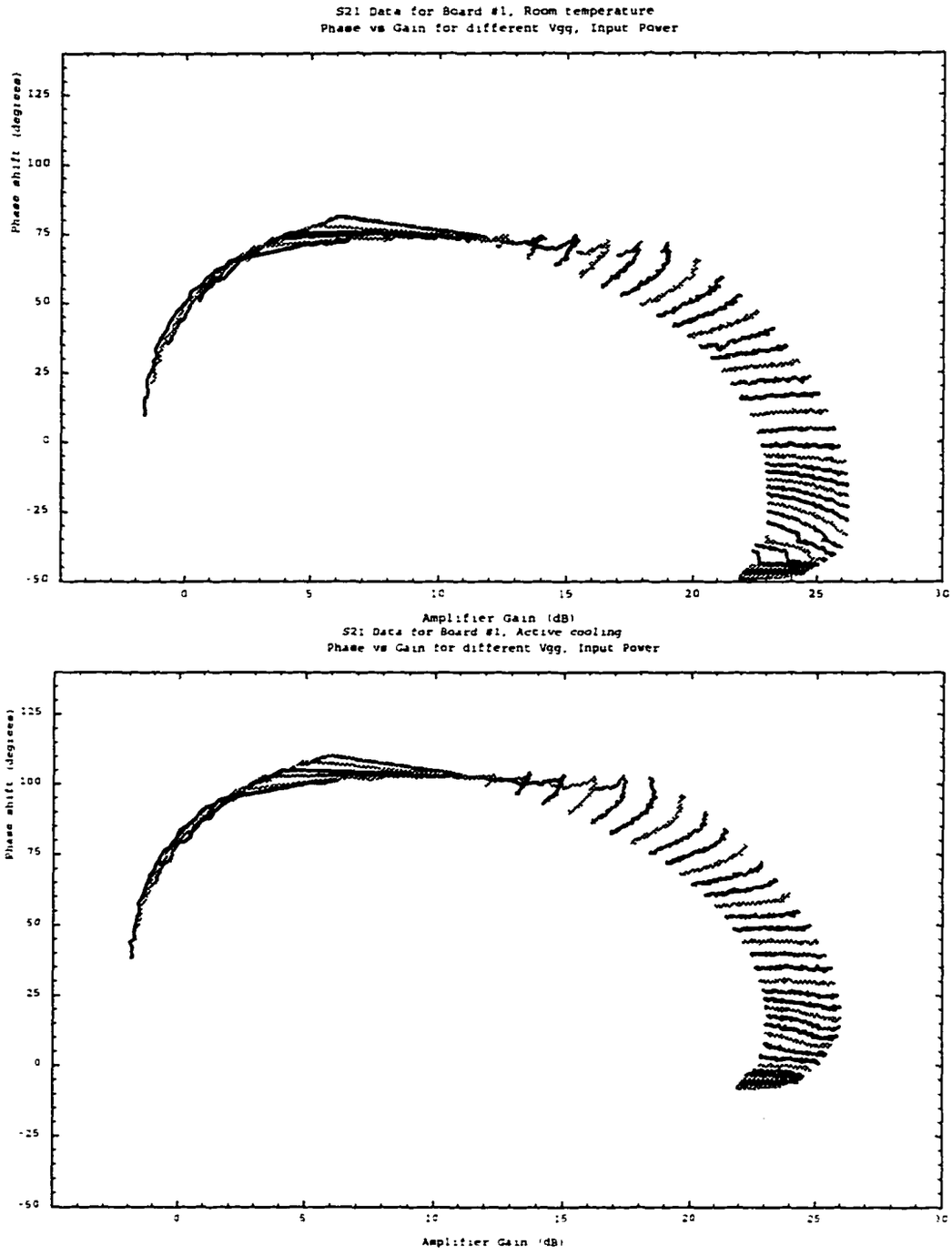
The following plots are included to illustrate the operational parameters of 4 amplifier circuits. Measurements of each amplifier were taken at room temperature and under active cooling. When each plot is compared with the other plots it can be seen that the amplifiers are very consistent with each other, and that their parameters do not vary greatly with a change in temperature.

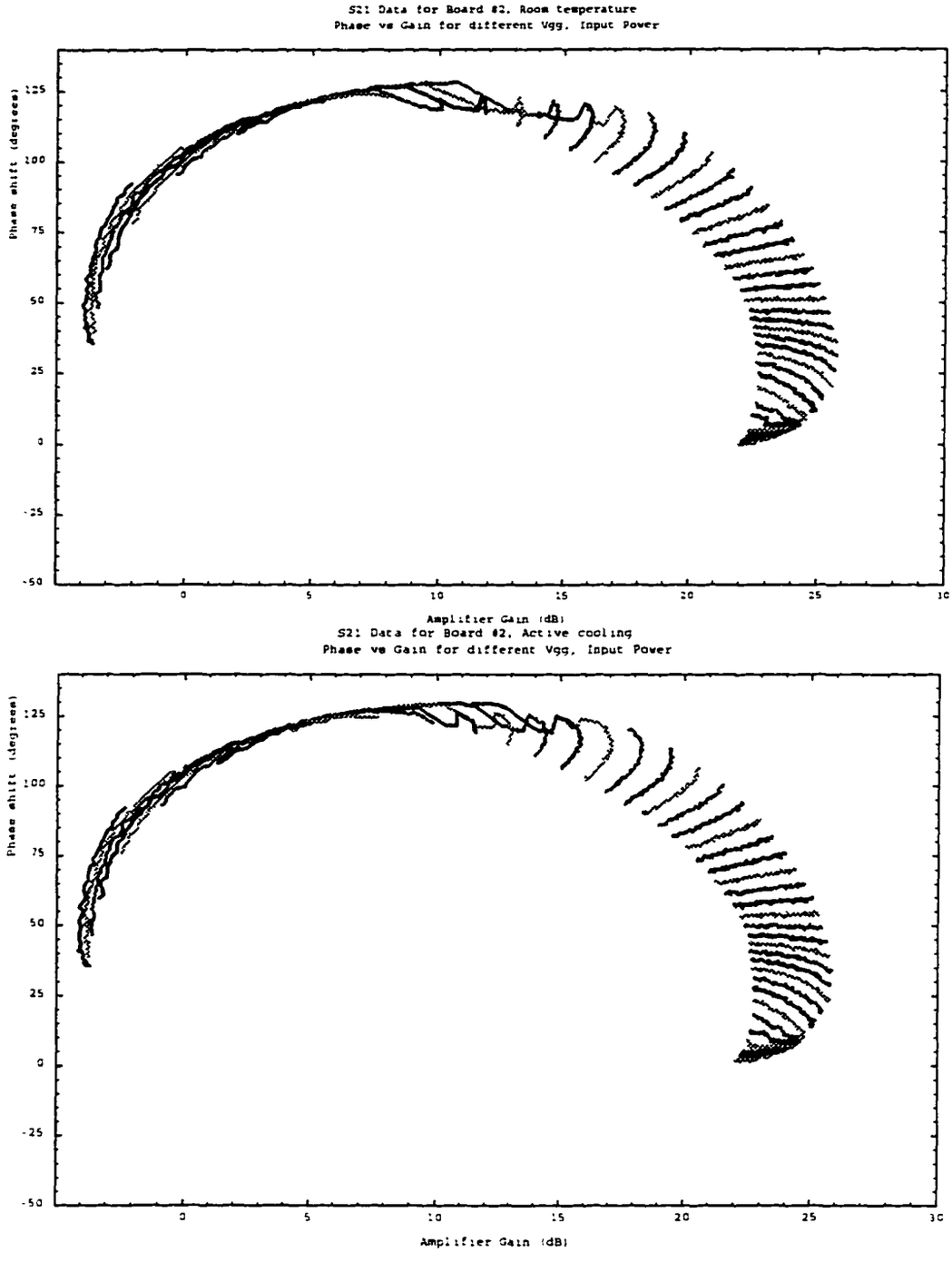


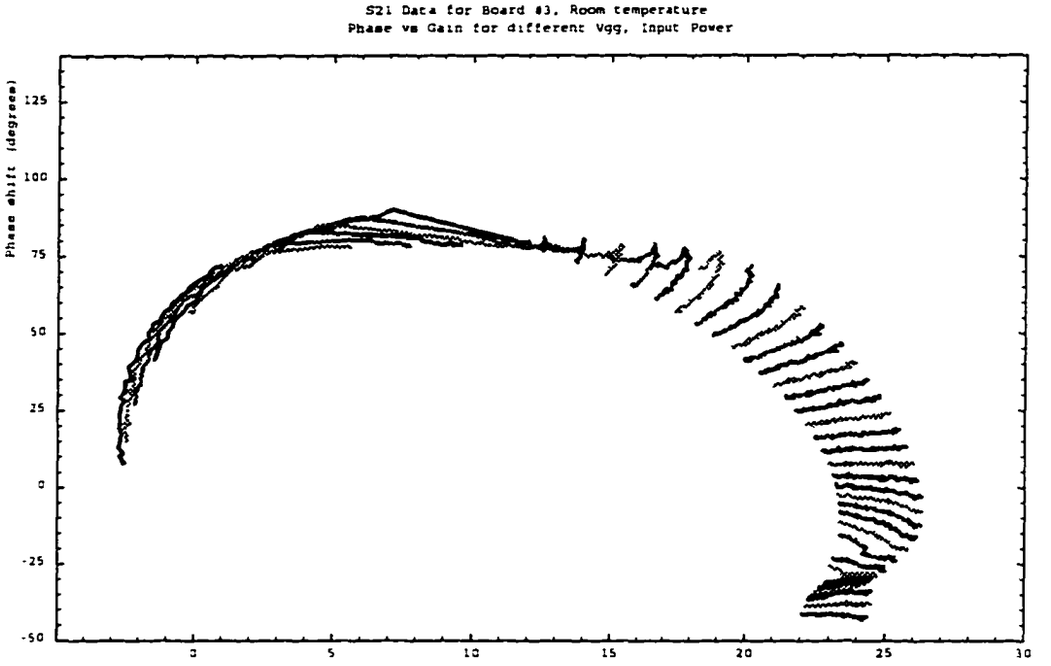


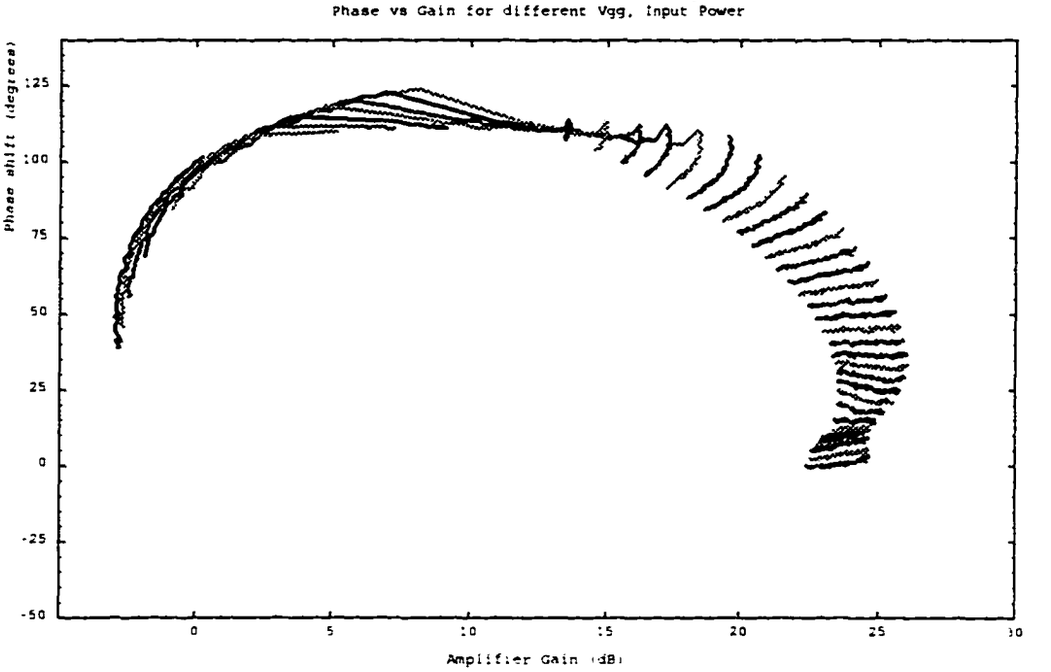


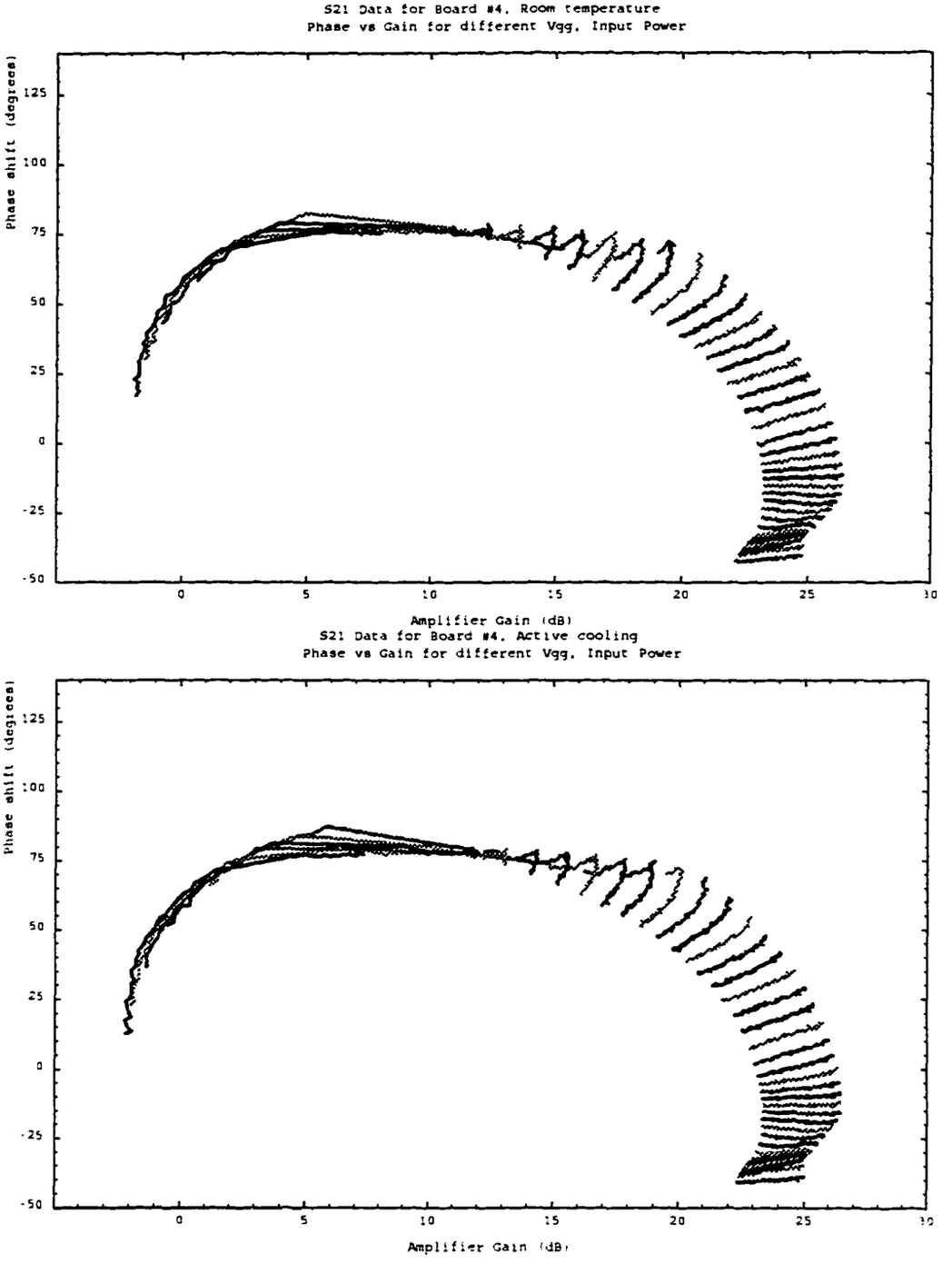



S21 Data for Board #1, Room temperature
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)
S21 Data for Board #1, Active cooling
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)


S21 Data for Board #2, Room temperature
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)
S21 Data for Board #2, Active cooling
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)


S21 Data for Board #3, Room temperature
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)


S21 Data for Board #3, Active cooling
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)


S21 Data for Board #4, Room temperature
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)
S21 Data for Board #4, Active cooling
Phase vs Gain for different Vgg, Input Power
Phase shift (degrees)
125
100
75
50
25
0
-25
-50
0
5
10
15
20
25
30
Amplifier Gain (dB)

## 14. REFERENCES

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