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Characterization techniques for contaminated gate oxide

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CHARACTERIZATION TECHNIQUES FOR CONTAMINATED GATE OXIDE

by

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STATEMENT BY AUTHOR

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This thesis has been approved on the date shown below:

_____ 19 December 1990

J.H.Hohl — Date

Electrical & Computer Engineering

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ABSTRACT

The oxide integrity is one of the most important factors in determining the yield of Very Large Scale Integrated(VLSI) circuits such as megabit Dynamic Random Access Memory (DRAM) devices. The effect of homogeneous contamination on the oxide integrity is studied by electrical measurements. The contamination is introduced in the Buffered Oxide Etchant(BOE) used for the preoxidation clean. The DC parametric test of forcing 1 nA and measuring voltage across the oxide is used to relate contamination to the leakage current and also to the number of failures. The factors affecting the measured voltage such as temperature, light and noise are eliminated so that contamination dominates the change in the measured voltage. The current-transport mechanism through the oxide was found to obey the Fowler-Nordheim equation at high fields. The barrier height at both interfaces was lowered in some contaminated devices. This evidence can be used to explain the increase of the leakage current or the event of low-field breakdown. A technique for measuring the low-field breakdown which is caused by defects in the oxide is developed.

CHAPTER 1: INTRODUCTION

1.1. THESIS OUTLINE

The objective of this thesis is to present an electrical method for detecting contamination introduced in chemicals used for the pre-gate oxidation clean in Metal-Oxide-Semiconductor (MOS) integrated circuits. The focus is on DC parametric measurements of gate-oxide leakage. Methods for measuring the low-field and intrinsic breakdown voltage for the gate oxide are discussed.

The thesis is divided into five chapters including the introduction. The second chapter describes the test system and the test program written for characterizing the devices. A detailed approach is also given for characterizing the stray leakage current of the probe card. Chapter 3 is devoted to the leakage measurements of the gate-oxide. Topics such as the test conditions, the current-transport mechanism, the effect of electrical stressing, detection of contamination, and the study of barrier-height lowering are included. Chapter 4 deals with the low-field and intrinsic-breakdown measurements. Chapter 5 has suggestions for further characterization techniques and software improvements. The conclusions of this thesis can be found in chapter 5.

1.2. EFFECTS OF CONTAMINATION

The dielectric breakdown and the leakage current of the oxide in MOS devices are two of the main factors in determining the yield of very large scale integrated (VLSI) circuits such as megabit dynamic random access memory (DRAM) devices. The premature breakdown, also known as low-field breakdown, of gate-oxide capacitors was reported [1] to be caused by defects and contamination introduced during the device-fabrication processes. It was reported that contamination induces precipitates in the gate oxide [1]. The precipitates are thought to reduce the breakdown strength by inducing defects in the gate oxide.

Thus, by forcing a low-bias current and measuring the voltage, one can investigate the number of defects and relate this number to the contamination level. Also, comparisons can be made regarding the average current versus contamination level. The technique of forcing current and measuring voltage was used to investigate the performance and yield of the gate-oxide capacitors.

1.3. FABRICATION OF WAFERS AND CONTAMINATION EXPERIMENT

Wafers with 6" diameter were processed by an abbreviated CMOS process schedule established by the Sandia National Lab-

oratories. A four way split for the pre-gate oxidation clean was designed to study the effect of iron. The four different splits were immersed in four different Buffered Oxide Etch (B.O.E.) baths with different levels of intentional homogeneous iron contamination. The levels of iron in the bath were 36 ppb, 106 ppb, 225 ppb, and 425 ppb, respectively. The 36 ppb level was that contained in the ultra-clean chemicals used as the baseline [2]. The contaminant levels are measured by means of Inductively Coupled Plasma Atomic Emission Mass Spectroscopy(ICP-MS).

Three patterned wafers were fabricated for each split, in order to investigate the wafer-to-wafer variation. In addition, one unpatterned wafer was produced for analytical characterization. Following the B.O.E. dip, the wafers were rinsed to 15 MΩ-cm resistivity in DI water. The oxide grown immediately after the rinse was 180 Å thick. A second lot was processed with bath levels of 17 ppb and 480 ppb iron, respectively. All the results shown in the thesis were taken from the second lot.

The chips contain comb diodes of different area, capacitors with different perimeter to area ratios, pin-hole array capacitors, and capacitors with different areas. The above structures are specially designed devices very sensitive to contamination. The chip also contains structures for process monitoring such as bridge structures and scratch rings.

1.4. OVERVIEW

The effect of heavy metal contamination on the yield of gate-oxide capacitors can be monitored by using electrical measurements. Heavy-metal contamination such as iron can cause major problems with the oxide integrity and reliability because of structural defect generation in the oxide.

The test system used for performing the electrical measurements in this work is the HP 4062C, which reliably measures currents down to the pA range. Although the manufacturer specifies measurement down to 20 fA, the stray leakage current measured across the pins of the probe card, when no device is connected, limits the measurements to 20 pA. Methods for characterizing and reducing the stray leakage current are presented. It was found that averaging 1024 samples per reading minimizes the noise, and using a 3 s time delay between the forced variable and the measurement eliminates the transient current. The minimization of the stray leakage is very important for the low-bias leakage measurement of gate oxide. A test program is developed and described which performs automatic testing at the wafer level. Large amounts of data can be collected and thus, statistical analysis can be performed.

The simplest electrical measurement on a capacitor for monitoring contamination is forcing current and measuring

voltage. The current forced was 1 nA. If current is expected to increase with contamination at a given voltage, then the measured voltage at a given current must be lower. This simple measurement can be used to relate leakage to contamination. However, if a device contains defects in the oxide, the local thickness is reduced and this will introduce high electric field regions, which might result in catastrophic breakdown. Thus, using this method, one can also relate the number of failures with contamination. The results did not show strong correlation between measured voltage and contamination. However, some contaminated wafers showed a significant number of failures at 1 nA forced current.

The major concern for the above measurement and the measurement discussed later, is the minimization of factors that might change the value of the measured quantity. Factors such as the temperature of the wafer, the light level at the wafer, and the electrical noise were found to affect the measured value. Temperature and light increase the leakage. Therefore, the temperature of the chuck was kept constant and the measurement was done in the dark. Noise is a current component added to the measured leakage. Its effect is minimized by measuring techniques.

Another objective was the investigation of other types of contamination that might interact with the contaminant under examination. Particularly, a search for ionic contami-

nation, which is the most frequent contaminant in MOS capacitors must be done. The method used for investigating ionic contamination is the temperature-stress CV technique. No significant amounts of ionic contamination were found.

The effect of electrical stressing is the next aspect that required attention. Over-stressing the device by applying a certain electric stress, might cause irreversible change to the device characteristics. A method is presented which determines the critical field, after which damage is possible. The critical field causing over-stressing was found to be 8.9 MV/cm.

The fundamental tests of CV and IV characteristics are used for "electrical diagnosis" of the devices before automatic testing. The CV characteristic is used for verifying doping type, oxide thickness and determining the magnitude and polarity of the forcing quantity. The IV characteristic is used to determine the mechanism governing the current transport in the oxide. The current-transport mechanism was found to obey the Fowler-Nordheim equation for electric fields above 6.7 MV/cm. Based on the Fowler-Nordheim equation, a method is presented which evaluates the barrier height of both interfaces of the oxide. The evaluation of the barrier height of the two interfaces is very useful for explaining the increase of leakage or the event of breakdown due to contamination.

Unfortunately, the method of forcing 1 nA and measuring voltage does not measure the field where breakdown occurs, because it is possible that the device breaks down at a lower current. A technique for detecting the critical field was developed. The principle of the routine is that voltage is swept and a failure current is chosen, which is higher by three orders of magnitude than the maximum current measured within the sweep for a good device. If the failure current is reached, the voltage is recorded as the critical electric field for the device. The range of the sweep was 0 to 15 V, which does not cause over-stress. The current at the end of the sweep is about 1 nA for the $1X10^{-4}$ cm^2 capacitors. Therefore, the failure current was chosen as 1 μA. The same setup is used to measure intrinsic breakdown, sweeping the voltage from 20 V to 30 V and by choosing a failure current of 1 mA. The range of the sweep includes the breakdown voltage and the failure current is a current above the onset of breakdown.

CHAPTER 2: TEST SYSTEM AND PROGRAM

2.1. TEST SYSTEM

Contamination studies require an automated test system to collect huge amounts of data, so that statistical analysis can be performed. The test system requires a parametric analyzer which performs electrical testing, an automatic prober which steps across the wafer and makes mechanical and electrical contact to the devices, and a computer which controls the analyzer and the prober.

The test system consists of the HP 4062C parametric analyzer which contains the 4280A capacitance measurement subsystem (CMS), the HP4142B DC subsystem (DCS), and the HP4084B switching controller (SWC). The parametric analyzer is controlled by an HP 310 computer, which also controls an automatic prober. The interaction of the above instruments is shown in Fig. 2.1. The capacitance measurement subsystem provides high speed capacitance and conductance measurement capabilities. Two AC signal levels can be chosen. The highest is 30 mV and the lowest is 10 mV. The testing frequency is 1 MHz which establishes only high frequency capacitance versus voltage characteristics (C-V). The internal DC bias source and timer allow the users to investigate capacitance-versus-time characteristics (C-t). The maximum capacitance-measurement capability of the

system is 1 nF, which is more than adequate for most capacitance measurements of integrated microelectronic structures. For capacitors with 180 Å gate oxide, the 1 nF limit sets a limit on the area of $5.3X10^{-3}$ cm^2.

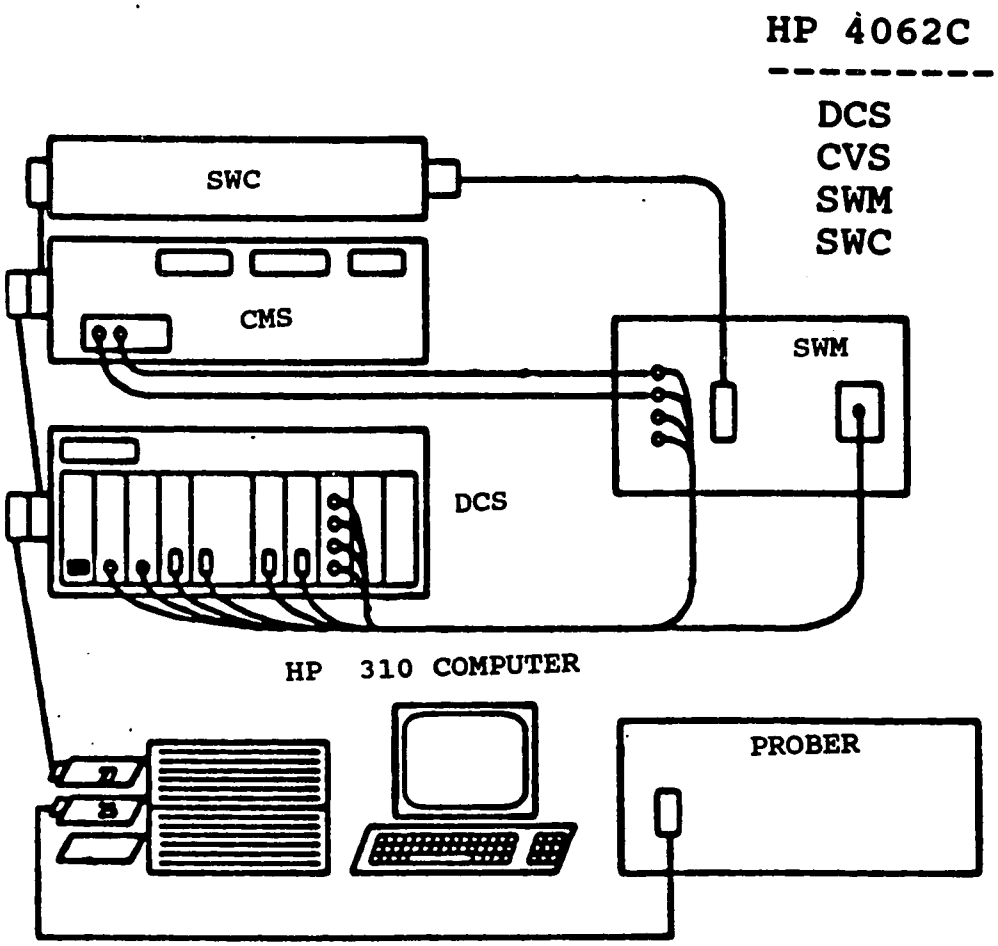


Fig. 2.1: Diagram showing the interaction between the various instuments of the test system.

The DC subsystem is equipped with 4 programmable DC source and monitor units. Each unit can force current and measure voltage or force voltage and measure current and this is shown in Fig. 2.2. One of the units can force and measure current up to 1 A. The same unit can force and measure voltage up to 200 V. This unit can be used for the characterization of power transistors. Two other units can force and measure current up to 100 mA. The force and measurement range is up to 100 V. The fourth unit has the same range as the previous

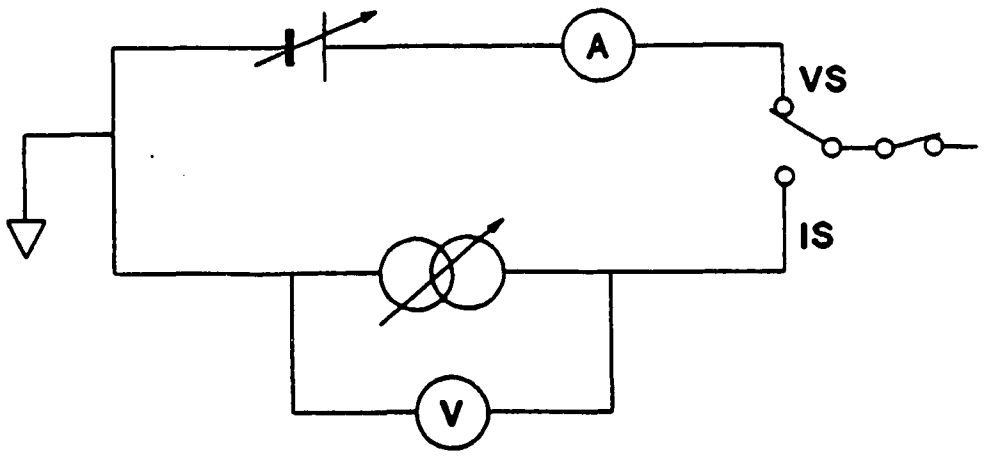


Fig. 2.2: Block diagram of the measuring unit.

two, but it has the advantage of high resolution. The term "high resolution" means that smaller steps of current or voltage can be forced or measured. The smallest step that can be used when forcing current is 50 fA. The smallest step measured is 20 fA. The above specifications are obtained in

the 1 nA range. The 1 nA range is the range used in the low bias leakage measurement. The measure and force resolution specifications for the voltage unit are 100 μV and 40 μV respectively. The above resolutions are obtained in the 2 V range.

The other three units have force resolution of 5 pA and measure resolution of 2 pA in the 100 nA range. The 100 nA range is the smallest range in these units. The force and measure resolution of the other three units is the same as that of the high resolution unit as far as voltage measurement is concerned. The high-resolution unit has also the lowest instrument error, and therefore its use in the low leakage measurement is essential.

Each reading of the measuring unit is the average of a certain number of samples. Each unit has the option of varying the number of samples taken per reading in two ways. The first way is to select one of the three preset numbers: 25, 32, or 512. Because of the sampling, a certain amount of time is required. The 25 samples option is called the short integration time option, the 32 samples option is called medium integration time option, and the 512 samples option is called long integration option. The second way to choose the number of samples is the "manual" option. In this option any number between 1 and 1024 samples can be chosen. For all low leakage measurements, 1024 samples were used in order to

minimize the effect of noise. The integration period for using 1 sample is 246 μs and the integration period for 1024 samples is 246 ms.

The switching matrix controller provides relay control signals and DC power to the switching matrix, thereby reducing the weight of the switching matrix (SWM). The SWM is housed in a box mounted on the automatic wafer prober and determines the connection configuration between the measurement pins and the measuring instruments. It has 24 pins with provisions for expansion up to 48 pins. To minimize stray leakage current, which affects low current-measurement, signal lines inside the SWM are fully guarded. The guarding scheme of the HP 4062C analyzer is shown in Fig. 2.3.

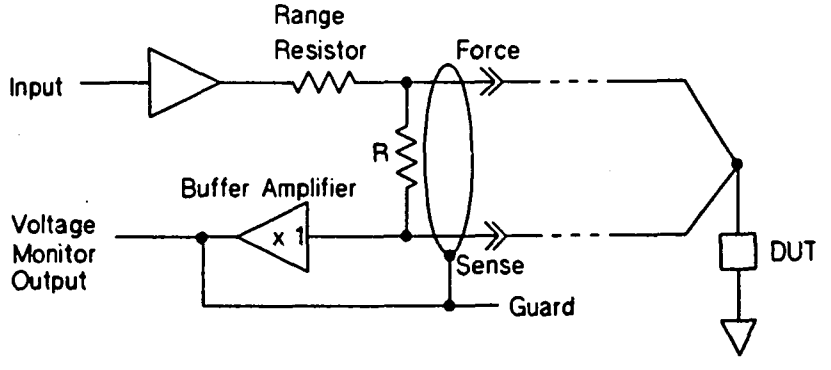


Fig. 2.3: Block diagram showing the implementation of the guarding scheme for reducing the stray leakage current.

To minimize the effects of residual resistance from the measurement, Kelvin connections are implemented at any pin of the SWM. Fig. 2.4 shows the two-wire and four-wire connection, respectively. The elimination of the residual resistance is achieved by the four-wire connection, whereas the two-wire connection compromises the measurement by the residual resistance of the wiring.

Probing of the wafers is performed by the Electroglas model 1034X automatic wafer prober. The prober accommodates a temperature controlled chuck of 4.5" diameter. A disadvantage of this prober is that each wafer must be loaded manually, compared to other probers where a set of wafers can be loaded automatically by means of a casette.

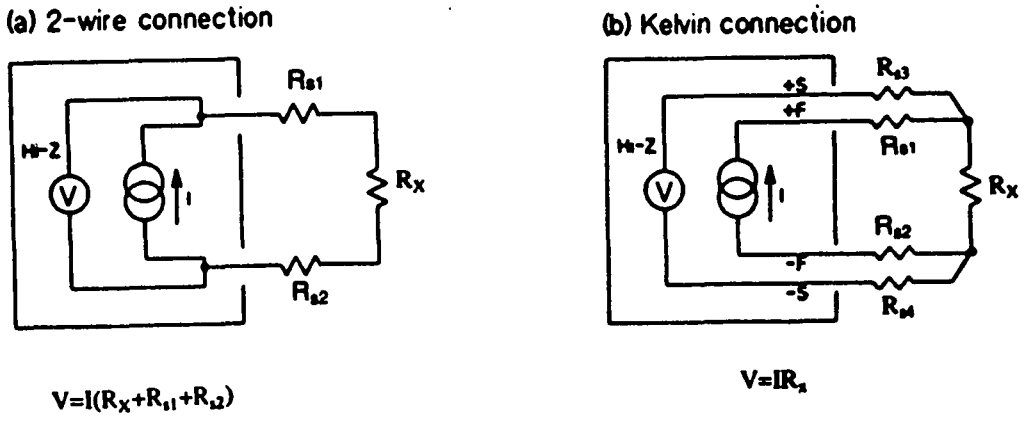


Fig. 2.4: a) Circuit diagram of the two-wire connection, and b) circuit diagram of the Kelvin connection for reducing the residual resistance.

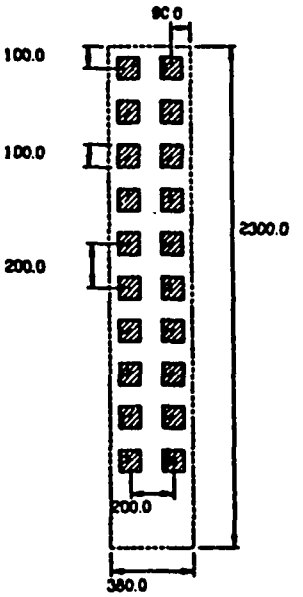
Various terms used in connection with automatic wafer probing are explained below.

PADS: The 100x100 μm^2 square aluminum pad on the wafer connects the device via the probe tip of the probe card to the switching matrix. The pads are sufficiently large compared to the probe tips and therefore reliable probing with no fault is achieved.

DEVICE: Smallest testable structure. Examples are capacitors diodes, transistors etc. All devices are connected to the pads.

STRIP: Next level of hierarchy which establishes the standardized probe card configuration used by the system. The strip is an array of two rows of ten pads. The center to center distance of the pads is 200 μm. The schematic diagram of the strip is shown in Fig. 2.5. In HP programs the term "module" is used for a strip.

FIELD: A 1.5X1.5 cm^2 square area which contains the various strips. The structure of the field is repeated over the area of the wafer. The global layout of the field is shown in Fig. 2.6. Other manufacturers call this entity a chip or die.



Dimensions

in μm.

Fig. 2.5: Diagram of the test strip.

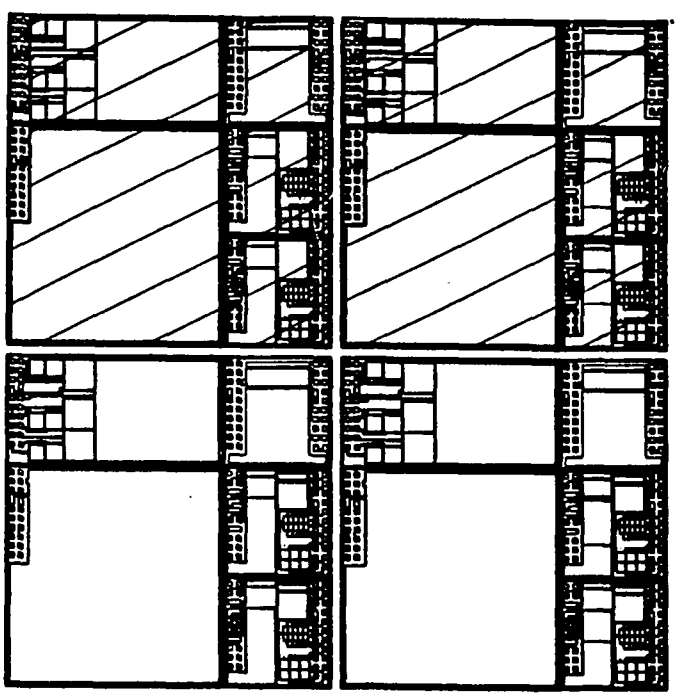


Fig. 2.6 Diagram of the field.

WAFER: The test wafer is 6" in diameter, and accommodates 60 fields.

PINS: Contacts on the switching matrix which connect the parametric analyzer to the probe card via the personality card and interconnecting wires. The pins are numbered with even numbers from 2 to 48. Only 20 of the pins are used to make connection with the probe card.

The electrical connections between the wafer and the personality board of the matrix are made by using a 2x10 probe card with blade-type probes which is compatible with the 2x10 pad configuration of the test strip. Therefore, a single probe card can be used to access all devices in a test strip.

2.2. SOFTWARE USE

The analyzer and the prober are controlled by a computer which requires programming code. Some programs are provided by HP and this saves a lot of programming time. The features of these programs are described next.

The computer controlling the tests is the HP 310 operated by the HP BASIC 5.1 operating system. The automatic test program is written in HP Basic 5.0 which is the latest ver-

sion of programming language used by the 300 series HP computers. The objective of the computer is to control the parametric analyzer's instruments and to control the wafer prober. The program contains subprograms incorporated in the Test Instruction Set (TIS) program provided by HP, which controls the analyzer. Three other programs, also supported by HP, are used to achieve specific functions which are explained later. These are the programs "WAFER", "EGX", and the prober pattern generation "PPG". The interaction between the above programs is shown in Fig. 2.7. The testing objective

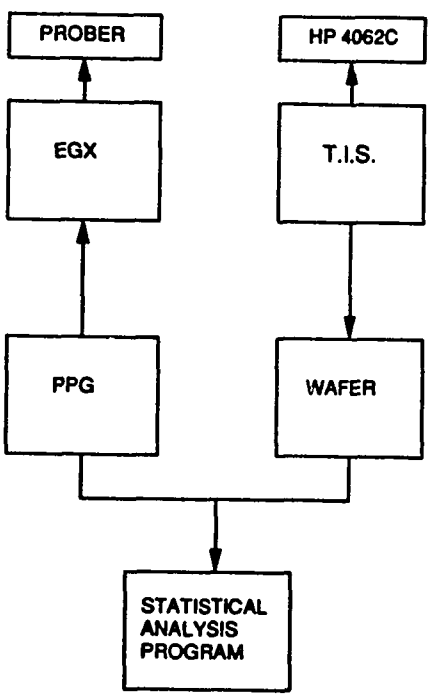


Fig. 2.7: Block diagram of the various programming blocks.

is accomplished with the aid of TIS. The data are stored by the use of the WAFER program. The "PPG" file creates the probing map and then the "EGX" program drives the prober according to the probing map. The data files created by "WAFER" are then transferred to the VAX system where data processing and statistical analysis are performed.

The main use of the BASIC programming codes is to display messages on the screen, prepare and store device-test definitions in Binary Data Files (BDAT), read the test definitions, pass information to TIS commands and other subroutines, translate pad numbers to pin numbers, etc.

The TIS commands are subprograms written in BASIC and are used to control the HP 4062C instruments (DCS,CMS,SWM). The TIS commands require parameters which are specified either in the form of variables or in the form of constants which are specified using BASIC.

The functions of the three programs are very important and save much programming time. The "WAFER" program creates ASCII files in a two or three dimensional array format. One dimension is the variable number and the other is the field number. For example a 2x32 array implies a file with two variables tested in 32 different locations. The two variables can be two different devices or the same device tested at two different biases. For the three-dimensional array one dimension is the variable number or device specification un-

der test, the second is the field number, and the third is the set of values resulting from testing using multiple biasing points. For instance, a 2x32x10 file implies a file with data of two devices, at 32 different locations on the wafer, and 10 measurements at 10 different bias points. The two-dimensional array stores data for single-bias measurements and the three-dimensional array stores data for multiple-bias measurements. The reason ASCII is used as the format of the database is because it is the only available file format which is compatible with other computers such as IBM or VMS/VAX systems. The data are transferred to a VAX system and are processed, using the Statistical Analysis System (S.A.S.) software.

The EGX program controls the movement of the wafer chuck from strip to strip and from field to field. It also moves the chuck up and down. When the chuck is up the probes make contact with the pads. When the chuck is down there is no contact with the pads. The program also moves the chuck to the load position when testing is completed.

The PPG program creates data files for probing control which are read by a subprogram in the WAFER program during its execution. The program asks from the user the wafer diameter and the X and Y dimensions of the field. Thus, a map with fields is created. Then, the user selects the fields that are to be probed. The program also requires the coordinates of the

strips within the field so that the map with strips is created for the field. The user is also asked to choose a probing sequence out of 6 choices.

A typical example illustrating all the above features of the PPG software is shown in the next three figures. In Fig. 2.8 the first page of the PPG file is shown.

```
***** Probing Pattern Generator (PPG) *****

|Wafer file name|A2
|Comment        |FILE FOR PROBING 5 STRIPS.

|PARAMETER                  |VALUE    |   [Probing Sequence] (s:start)
|Wafer size        [inches] | 6.00000 |
|X chip size      [microns] |   14700 |    s----->      <-----     s----->
|Y chip size      [microns] |   14820 |     <-----      ----->      ----->
|Probing Sequence           |       1 |     ----->     <-----s     ----->
|Chip configuration         |FLEXIBLE |       1          2          3
|X module size [microns]    |-------- |
|Y module size [microns]    |-------- |     <-----s     ----->      <-----
|X module number            |-------- |     <-----     ----->      <-----
|Y module number            |-------- |     <-----     s----->     <-----s
                                                4          5          6
```

Fig. 2.8: First page of the PPG file.

This particular application covers all the testing done for this thesis. In this page the wafer size, which is 6," was entered, as well as the X and Y size of the field. The probing sequence chosen is type "1". This means that the top field on the left side is probed first and the probing sequence is from left to right in the top row then from right to left in the second row, etc. The chip configuration was chosen as "flexible" which means that the user can choose randomly the

locations of the strips within the field as desired by a testing application. A typical example is shown in Fig. 2.9, which is the second page of the PPG program. In this case, five strips were chosen for testing and the location within the field is shown. In this page the locations of up to 50 strips can be specified for probing. Finally, in Fig. 2.10 the map for testing is shown. The 32 squares in black represent fields selected for probing. The white squares are fields produced automatically by the software according to the wafer size and X, Y size of the field. These are fields not selected by the user for testing.

[Module Selection]

No.	X	Y	No.	X	Y
1	+0	+0	14		
2	+12130	+0	15		
3	+14020	+0	16		
4	+6670	-4800	17		
5	+12130	-4800	18		
6			19		
7			20		
8			21		
9			22		
10			23		
11			24		
12			25		
13			26		

Fig. 2.9: Second page of the PPG file, showing the strip coordinates.

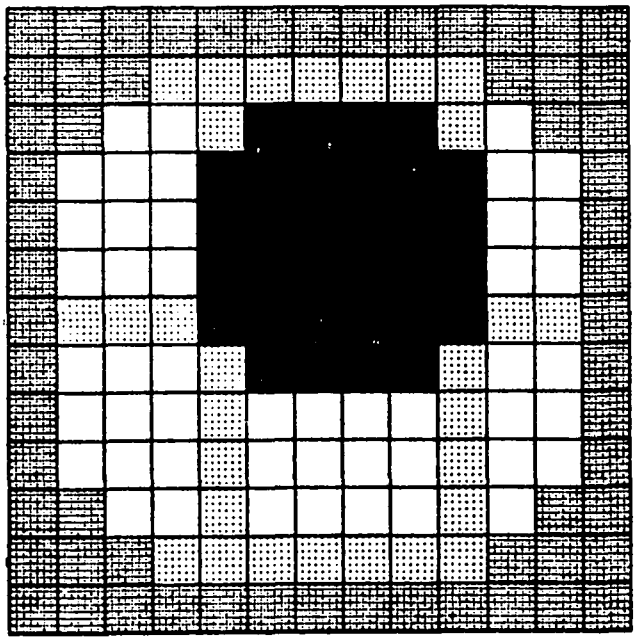


Fig. 2.10: Third page of the PPG file, showing the wafer map and the selected fields for probing.

2.3. TEST PROGRAM

The programs provided by HP are generic programs written to assist the user. For example "PPG" creates the wafer image for probing, TIS performs the measurement, etc. However, additional programming code is needed to accomplish a specific test objective. The additional programming code is linked together with the programs provided by HP to form the test program. The features of the test program are described next.

The most critical testing decisions are performed by the CONFIG file. This file contains records which set the test

objectives. The first record is the mass storage medium in which the data files are to be stored. The second record contains the name of the PPG file which controls the probing sequence created by the PPG program. The third record is the number of fields to be tested. This number must not be greater than the number of the fields selected in the PPG file. However, it can be smaller if not all the fields are required for testing. The fourth record is the number of strips and it must be equal to the number of strips defined in the PPG file. The fifth record is the test-definition library which either exists or does not exist. If it does not exist, it can be created in the subsequent steps of the program. The last record is the file identifier. The file identifier is a letter inserted in front of the wafer number, creating the data file name for the wafer under test. A typical example is shown in Fig. 2.11. In this case the mass storage medium is F, meaning that the data are stored on floppy disk. The

```
SYSTEM CONFIGURATION

MASS STORAGE MEDIUM :        F
PPG FILE            :        A2
# OF CHIPS          :         32
# OF MODULES        :         5
TEST DEF. LIBRARY   :        NEW
FILE IDENTIFIER     :        A
```

Fig. 2.11: Typical display of the CONFIG file.

PPG file is "A2" which was created by the PPG program and is shown in Fig. 2.8. The number of fields is 32 which is the number of fields selected in the map of the PPG file. The number of strips is 5 which is the number selected in the chip configuration of the PPG file shown in Fig. 2.9. The library name is called "NEW"
and thus the directory with the name "NEW" containing the test- definition files for each strip is accessed. The file identifier is "A".

The test-definition library is created using binary data files because of the faster rates of data transfer compared to ASCII files. Before test definitions are created, a test-strip type definition ought to be created. This is done because, for each strip, the corresponding test-definition files should be opened. Therefore, the user is asked to assign a test-definition data file number for each strip. Later, when the program is executed, the appropriate type of file is opened when a strip is to be probed. A typical test-strip definition is shown in Fig. 2.12 where the strips 1 and 3 have test data definition file "1", the strips 2 and 4 have file "2", and strip 5 has file "3".

The next step is the creation of a test-definition for a particular strip. The program asks the user the number of tests required for the particular strip. Then, the program, according to that number, asks the user for two types of res-

MODULE TYPE DEFINITION

MODULE #	MODULE TYPE
1	1
2	2
3	1
4	2
5	3

Fig. 2.12: Typical display of the test-strip definition file.

ponses. The first requires the user to enter the variable number for the test definition as it will be processed by the data-processing and statistical software. In the same ques-- tion the user is asked to enter the type of test definition, which is a three-letter string variable. The first letter represents the type of measurement, the second represents the device type and the third represents the type of electrical quantity measured. For example, if current is forced and voltage is measured, the user should type "LDV". The first letter "L" means that a leakage measurement is performed, the second letter "D" means that the test is done on a diode, and the third letter "V" means that voltage is measured. Another example is "LCI". This is the leakage measurement of a capacitor when current is measured. Finally, in the same question the user is asked the value of two parameters which establish the test conditions. Some examples of parameters are

the forcing function which can be voltage or current, the start voltage, the stop voltage, the step voltage, etc. Sometimes only one parameter is to be specified, so the second parameter is indicated as zero.

In the second type of question the user is asked to enter the pad number for the test definition. Four pad numbers are required, but in most applications of diode and capacitor testing two pad numbers are sufficient. Thus the rest are entered as zeroes. A routine was written which translates the pad numbers to pin numbers according to the correspondence between pad and pin determined by the interconnection of the probe card and the personality board of the switching matrix. This makes test-definition creation easier for the user, since the user has pad-number specifications for device-test definition. Routines have been written to read the pad definition of each strip as well as the pin definitions. A typical example showing the content of the test definition library is shown in Fig. 2.13. The test definition library "NEW" in this case contains the files "1", "2", and "3" as selected in the test-strip-type definition. When the program is run, the user is asked if he wants to modify the CONFIG file or to proceed. Then the user must enter the wafer name. The last question asked regards test definitions. If modification is needed, then the flow goes through the test definition routine; otherwise the program pauses. At this point

the user must align the wafer and probe manually to the first strip of the first field. Then the program is continued.

```
TEST DEFINITIONS
27 Jun 1990  14:22:32
TEST DEFINITION LIBRARY  :    NEW

PAD ASSIGNMENT OF   /USERS/PADS/NEW/1P
-------------------------------------------------
 1        LDI        11        8        0        0        -4        0
 2        LDI        18        8        0        0        -6        0
 1        BVD        11        8        0        0         .001     0
 2        BVD        18        8        0        0         .001     0

PAD ASSIGNMENT OF   /USERS/PADS/NEW/2P
-------------------------------------------------
 1        LDV        12        7        0        0         1.E-9    0
 2        LDV        12        7        0        0        -1.E-9    0
 1        BVC        12        7        0        0         .001     30
 1        COX        1         7        0        0        -10       0

PAD ASSIGNMENT OF   /USERS/PADS/NEW/3P
-------------------------------------------------
 3        LDV        19        5        0        0         1.E-10   0
```

Fig. 2.13: Typical display of the test-definition library.

Probing is done by means of two loops. The first loop functions as the control for testing the strips within a field. Part of the control is the opening of the proper test-definition data file according to the strip-type definition. The strip is tested according to the response during the test definition setup. When a testing function is required then execution is transferred to the routine corresponding to the function. Then, the measurement is performed and the value is stored in a two-dimensional element

containing the variable number and the field number, if a single-bias measurement was specified. When IV or CV plots are to be stored, then the array created is three-dimensional. One dimension is the variable, the second is the field number and the third is the measured current at a specified range of voltage, if IV measurement is required. If CV measurement is required, then the third dimension is capacitance values at a specified range of voltage. The process is repeated until all the definitions of the strip are exhausted.

When all the strips inside a field are probed, then the second loop comes into effect. The objective of this loop is to control the field-to-field testing and probing. There are means to move from a tested field to the next field by using the EGX program. This loop increments by one the second dimension of the data array, which is the field number, when a field is tested. Thus, it contributes to the database creation. When all the fields have been tested, the chuck is moved to the load position.

The program includes testing routines for leakage current and breakdown for both junctions and gate oxides. It also includes routines to measure voltage at a given forcing current for these devices. Process monitor routines for other structures include short-circuit and open-circuit tests, sheet-resistance measurement, line-width measurement, and oxide-capacitance measurement.

2.4. PROBE CARD CHARACTERIZATION

It is very important for low-field leakage measurements to know the level of the stray leakage current measured between two signal lines leading to the probe card tips, when no device is connected. Although the manufacturer specifies that the HP 4062C system can measure down to the fA range, the stray leakage currents impose a limitation of how low one can measure. Therefore, the stray leakage current must be investigated and minimized.

First, the stray leakage current up to the pins of the switching matrix was investigated. This is done by considering the current versus time characteristic. The setup for establishing the I versus t plot is as follows: one pin is grounded and the other pin is connected to a DC voltage source and current monitor. In order to study the no-bias leakage current, the bias of the DC voltage source is 0 V. A waiting time is included and then the current is measured. The I vs t plot gives a good representation of how strayleakage varies with time. Fig. 2.14 shows a plot of leakage current for pins 1 and 8 versus time. One sample is used which accounts for a 246 μs integration period. The waiting time is 754 μs. Therefore, measurements are taken every 1 ms. The current fluctuates between -3 pA and 3 pA with an average current of -211 fA. The variation of current about

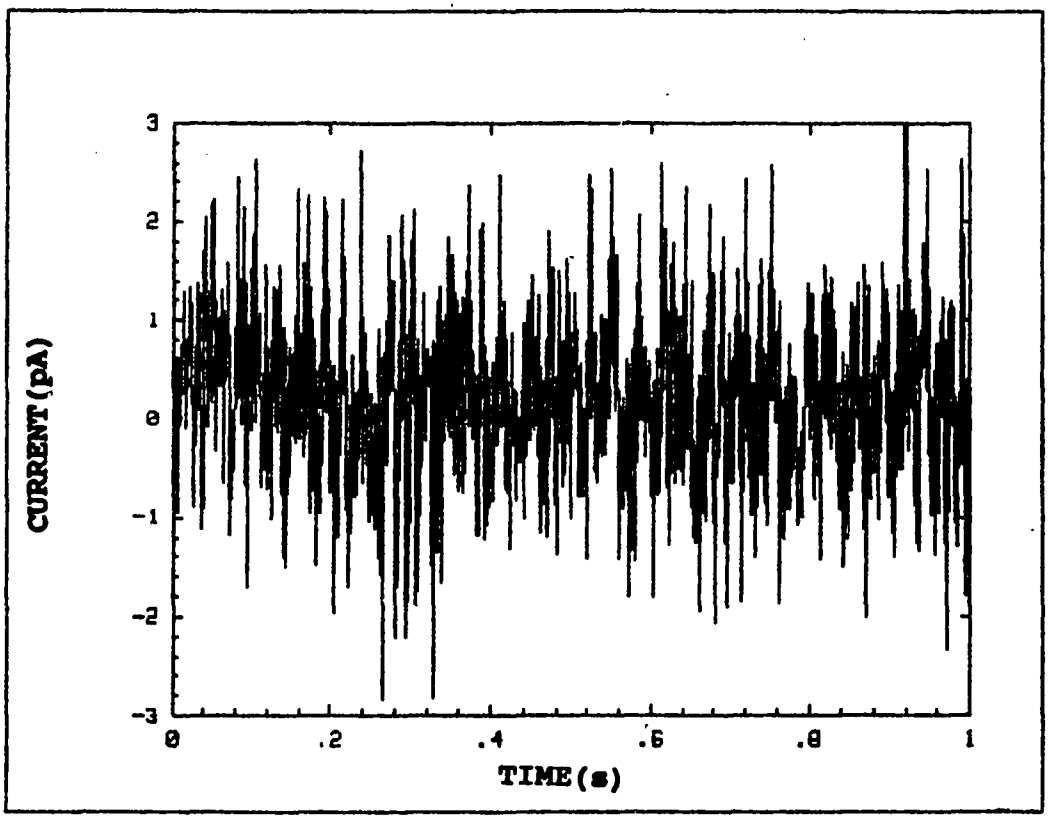


Fig. 2.14: Characteristic of current between two pins of the switching matrix vs. time.

the average is random, with spikes sometimes reaching a magnitude of 3 pA. Other pin combinations show similar current levels with averages from -60 fA to -211 fA.

The additional wiring introduced between the switching matrix and the probes contributes additional leakage current to the system, as expected. Various pin combinations were studied, covering the most important pair combinations. Im-

portant combinations are the arrangement involving distant pins such as 1 and 20, and the arrangement involving adjacent pins such as 1 and 2. Also, some other intermediate combinations such as 10 and 20, or 1 and 7 were investigated.

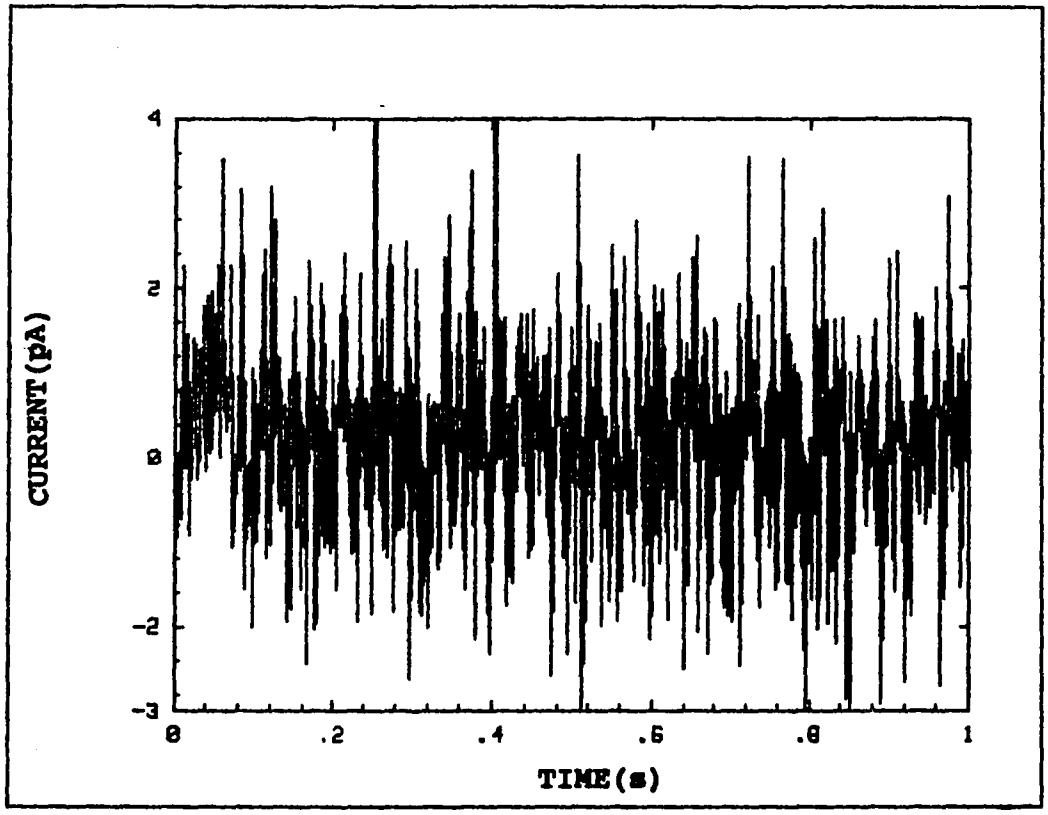


Fig. 2.15: Characteristic of current between two pins of the probe card vs. time.

Again, the I vs. t routine was used to study the leakage of the probe card. A typical plot for probe pins 1 and 8 is shown in Fig. 2.15. The current fluctuates from -3 pA to 4 pA with average of -242 fA. The various pin combinations ex-

amined showed average leakage current ranging from -100 fA to -242 fA.

The effect of integration time upon the stray leakage current can be asserted by considering the I-t characteristics either of Fig. 2.14 or of Fig. 2.15. Since the time interval is from 0 to 1 s, with a step of 1 ms, the number of samples is 1000. The average of the 1000 samples of Fig. 2.14 gives 211 fA. However, if only one sample were taken, the measurement result would be a random value between -3 pA and 4 pA. An experiment was caried out to examine the effect of sampling. Three different numbers of samples were used: 10, 100, and 1000. Fig. 2.16 shows the graph of leakage vs. number of samples for two pins of the probe card, and no bias applied. The leakage decreases with increasing the number of samples. Therefore, to minimize noise, the maximum number of 1024 samples must be used.

The other factor that must be considered is the transient current generated when a forcing voltage is applied. The transient current was first investigated by applying a forcing voltage and monitoring the current every 1 s. The number of was 1024 to minimize the noise. The hold time before measurement starts is defined as the time delay between force and measurement function. The time delay was varied in order to investigate its effect upon the leakage measurement. The time delay was varied from 0 to 5 s with steps of 1 s.

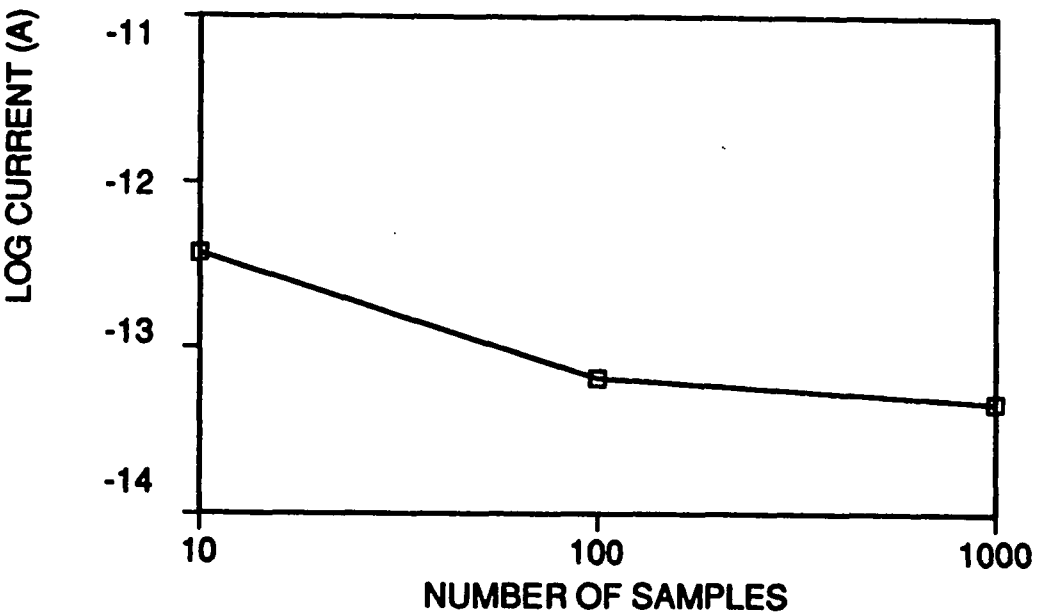


Fig. 2.16: Leakage vs. number of samples for two pins of the probe card.

Fig. 2.17 shows the graph of current measured with 1024 samples at 6 V vs. time delay. The current was measured immediately after the time delay. Above 3 s time delay there is no significant decrease of the average leakage current which means that the transient current has died out.

The main conclusion from the probe card characterization is that the noise current level measured at the switching matrix is approximately 200 fA. The contribution of the probe interface is about 30 fA. This is higher by three orders of magnitude than the specified capabilities of the

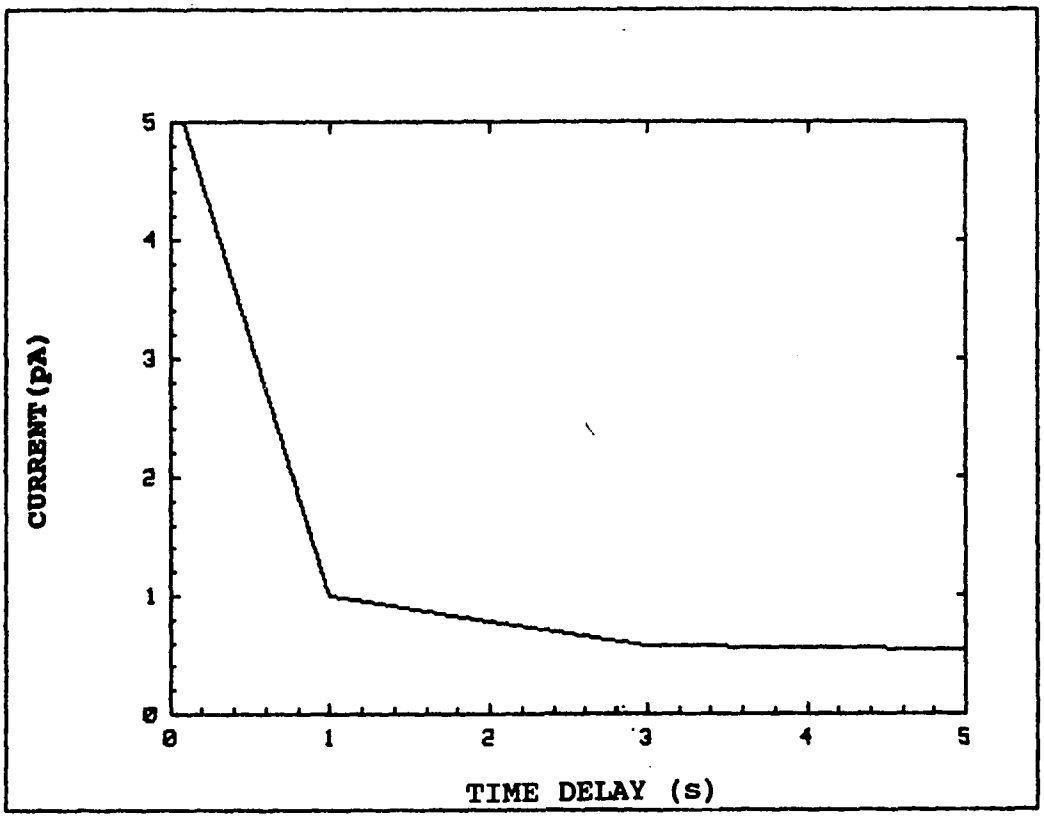


Fig. 2.17: Current at 6 V vs. time delay for two pins of the probe card.

measuring units which can measure down to 20 fA. HP specifies 1 pA maximum offset current across the pins, but experimentally a value of approximately 240 fA was established for the probe card design used on the UA system. A time delay of at least 3 s must be used to eliminate the transient currents due to the turn-on of the forcing function. Finally, the 1024-sample integration option must be used to reduce the

noise to the lowest level possible.

An interface, with the lines not fully guarded all the way down to the probe card, was used previously. The stray leakage of this interface was found to be aproximately 300 fA, which made its performance still better than the specification published by HP.

CHAPTER 3: LEAKAGE MEASUREMENT OF OXIDE

3.1. LEAKAGE MEASUREMENT OF GATE OXIDE

The first mechanism to monitor contamination is the leakage. Defects in the oxide reduce the thickness locally; thus, a higher electric field is created locally. This tends to increase the leakage current. Thus, the leakage is one way to detect contamination.

There are two options to characterize the leakage of a gate oxide. One is to force voltage and measure current and the other is to force current and measure voltage. The second method is preferred because more repeatable results are obtained. Devices were tested at different locations on the wafer. The measurement was repeated four times. The maximum relative error between any two measurements of a device at a given field, when current was forced and voltage was measured was 0.1 %, whereas the corresponding figure when voltage was forced and current was measured was 2 %. The setup for forcing current and measuring voltage is shown in Fig. 3.1. The substrate is grounded and the source unit forcing current is connected to the gate. The voltage measuring unit is also connected to the gate and parallel to the forcing unit. To characterize the oxide, testing with the silicon surface in the accumulation region is required such that all the applied

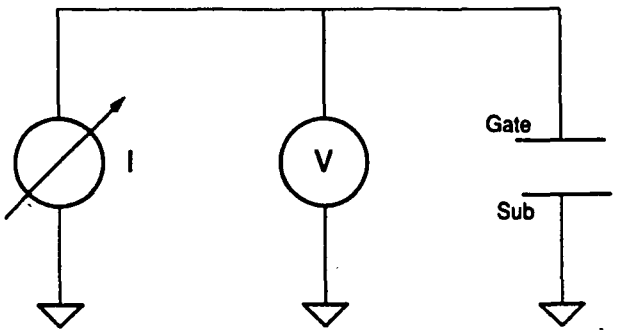


Fig. 3.1: Setup for the force current, measure voltage technique.

voltage appears across the oxide. To achieve this, a negative current needs to be forced for a p-type substrate, in order to measure a negative gate voltage. For an n-type substrate the reverse polarity must be used.

The routine of the leakage measurement can be explained by making use of the flowchart in Fig. 3.2. To perform leakage measurements the corresponding definition is specified in a test-data definition file. The first step is the connection of the measuring unit with the device. The connection is made when the relay of the switching matrix closes, thus connecting the unit with the device through the personality board and the probe.

The second step is the application of the forcing current. This current is specified in the test definition of the device under test. The execution time is 4.5 ms.

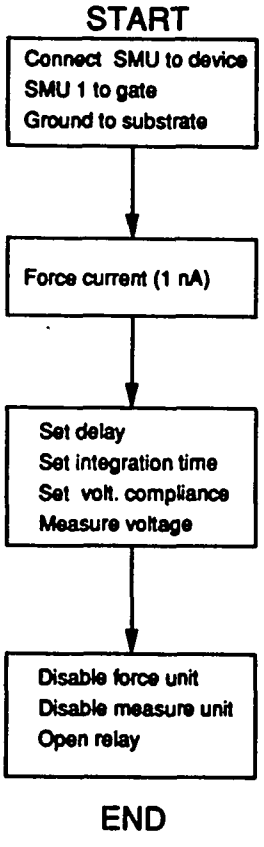


Fig. 3.2: Flowchart of the force current, measure voltage technique.

The third step is the application of the measuring function. The execution time of this function is 6 ms. In this step three parameters need to be specified. These are the time delay, the number of samples, and the compliance voltage. All these parameters are set within the routines and can not be altered during test definition creation. However, the user can modify them by editing the program. For all

capacitors the same values are used. The value of the time delay was established in section 2.4 and is 3 s. The number of samples used is 1024 for low-field leakage measurements, as described in section 2.4. The voltage compliance is set to 25 V. This value is chosen to detect open circuits. The nominal measured voltage for the $1X10^{-4}$ cm^2 capacitor with 3 s delay and 1024 samples is approximately 15 V. In the case of an open circuit, the system will measure compliance. Therefore, the compliance and the nominal value are sufficiently apart so that unambiguous distinction of the two results is possible. Open circuits are the result of bad probing, for example because of poor contact due to insufficient pressure

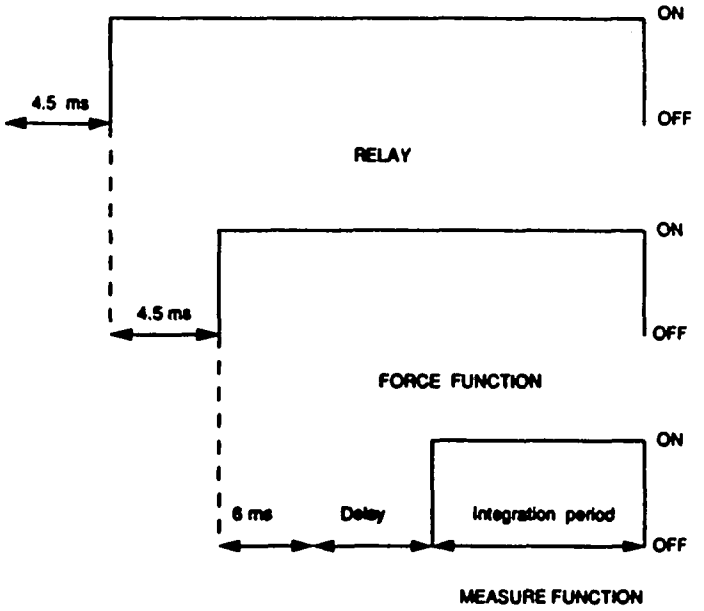


Fig. 3.3: Timing diagram of the force current, measure voltage technique.

of the probes on the pads.

The fourth step is the disabling of the force function, immediately followed by the opening of the relays at the switching matrix. A time diagram realizing the above steps is shown in Fig. 3.3.

3.2. CV CHARACTERISTICS

The very first diagnostic measurement, performed before automatic testing, is the CV plot. From the CV plot, the polarity and magnitude of the forcing function for testing in a certain operating region can be predicted. Although the polarity can be predicted from the device doping, the CV characteristic always must be obtained for verification of the process.

If the device has a p-type substrate, as in the fabrication process described in section 1.3, then a negative forcing polarity drives the silicon surface underneath the gate into accumulation. When the gate voltage is positive, and smaller than the threshold voltage, then the surface is in depletion or weak inversion. The onset of strong inversion occurs when the voltage at the gate is equal to the threshold voltage. When the voltage at the gate is larger than the threshold voltage, then the surface is in strong inversion. A similar argument holds if the device is n-type, but the

polarity of the voltage is reversed.

To characterize gate oxides, the silicon surface must be in accumulation with all the voltage appearing across the oxide. In inversion, approximately 0.8 V is dropped in the silicon substrate across the depletion region.

Among the parameters that can be extracted from the CV plot is the oxide thickness. If C_{ox} is the accumulation capacitance, then the oxide thickness, t_{ox}, is given by:

$$t_{ox} = \frac{\epsilon_{ox} \times A}{C_{ox}} \qquad (3.1)$$

where ϵ_{ox} is the permitivity of silicon dioxide, and A is the area of the capacitor.

A routine has been written which performs the CV measurement. The gate is connected to the low terminal and the substrate to the high terminal of the capacitance meter as

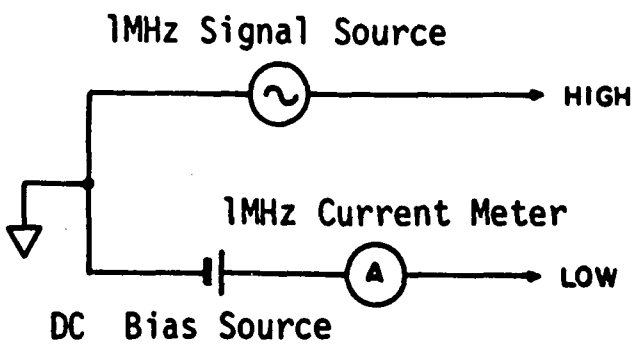


Fig. 3.4: Setup for the CV measurement.

shown in Fig. 3.4. A sweep voltage is applied to the gate starting from an initial value determined by the user and

terminating with a value also determined by the user. The voltage range should be chosen large enough to cover all three regions. Sweeping the voltage from -10 V to 10 V covers all the regions. The testing frequency is 1 MHz. The number of samples is 512, which is the maximum number of samples that can be used for capacitance measurements. It is used to minimize noise voltages or currents. The integration period for the 512-sample option, called long integration by HP, is 100 ms. There is a limitation in measuring low ca-

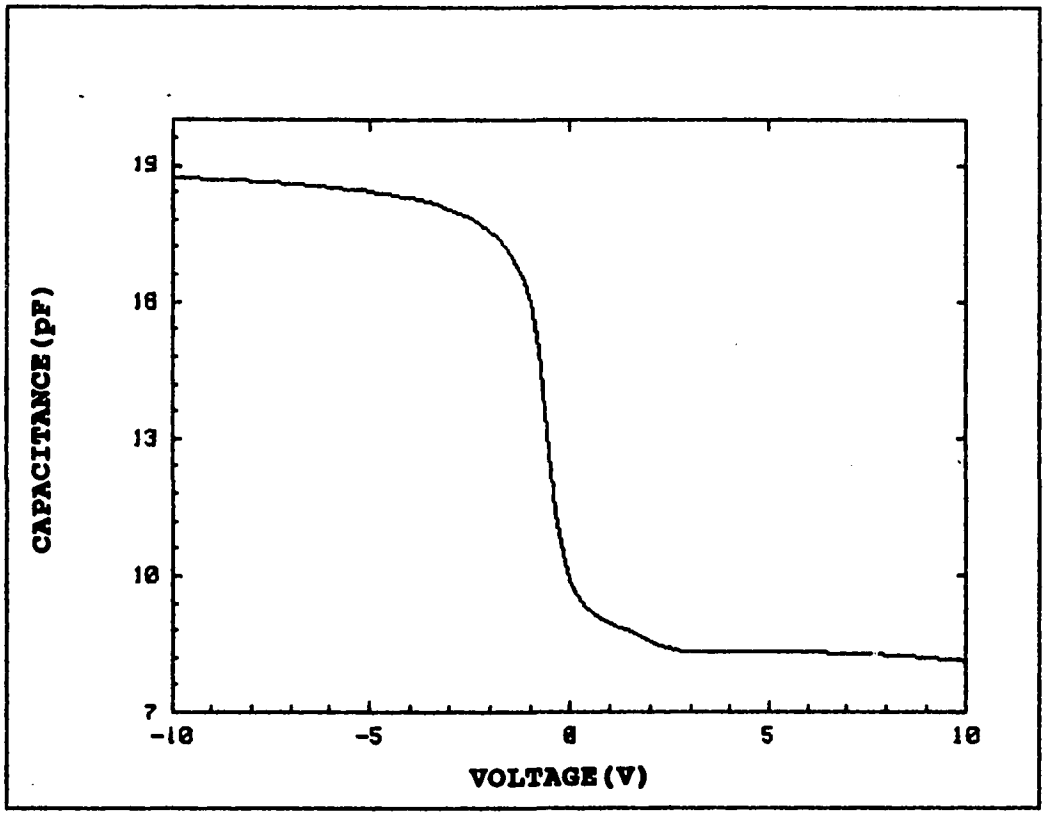


Fig. 3.5: Typical CV characteristic of a $1X10^{-4}$ cm^2 capacitor.

pacitances due to the stray capacitance which appears across the device. Thus, the actual capacitance is the measured value minus the stray capacitance. Typically, the stray capacitance measured is from 0.1 pF to 0.3 pF when no device is connected to the probes. The stray capacitance must be subtracted for capacitance measurements of 10 pF or lower, where it exceeds 1 % of the measured value. For higher capacitance measurements it can be neglected. The system automatically compensates for its internal stray capacitance up to the switching matrix. A typical CV plot for p-type capacitors is shown in Fig. 3.5.

3.3. TEST CONDITIONS

In order to discover the effect of contamination in the measurement of electrical parameters one must minimize the effect of other factors that might shift the value of the measured parameter. If, for example, the value of a measured voltage at a given current of a given device in an uncontaminated wafer is V_1 , then the corresponding value of the voltage V_2 of the corresponding identical device but on a different, contaminated wafer can be assumed to be

$$V_2 = V_1+\Delta V_{cont}+\Delta V_{temp}+\Delta V_{light}+\Delta V_{noise} \qquad (3.2)$$

where ΔV_{cont} is the shift in voltage because of contamination, ΔV_{temp} is the shift in voltage due to temperature differences,

ΔV_{light} is the shift in voltage due to light, and ΔV_{noise} is the shift in voltage due to noise. Therefore, to examine correctly the effect of contamination, all the ΔV components except ΔV_{cont} should be minimized so that variations due to contamination are dominant. The best test to check whether the effect of those factors is minimized is to test the uncontaminated wafer twice and check the repeatability. Since the factor ΔV_{cont} is zero if the repeatability of the measurement is perfect, it means that the other factors do not contribute much. Next, the above factors will be discussed.

The first factor to be considered is the temperature effect. Experiments have been carried out to investigate the

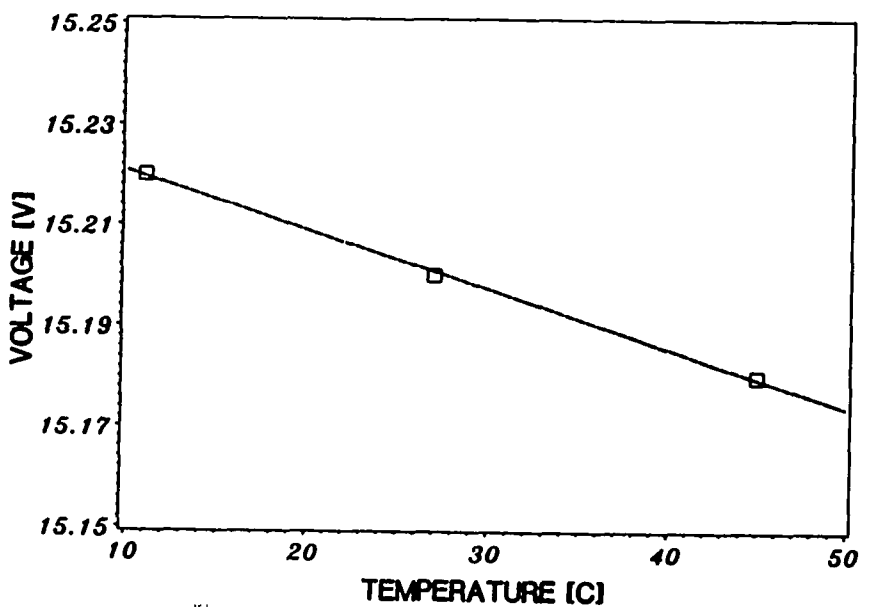


Fig. 3.6: Measured voltage at 1 nA vs. temperature for a $1X10^{-4}$ cm^2 capacitor.

of varying the wafer temperature. Three different temperatures, 11 °C, 27 °C, and 45 °C have been applied. At each temperature the current of a $1X10^{-4}$ cm^2 capacitor was measured at 15 V and the voltage of the same device was measured at 1 nA. The voltage versus temperature plot shown in Fig. 3.6 shows that the voltage at a given current decreases with temperature, as expected. This trend can also be seen if two I versus V plots for different temperatures are drawn as shown in Fig. 3.7 where $T_1>T_2$. Thus, forcing a given current results in smaller measured voltage at higher temperatures.

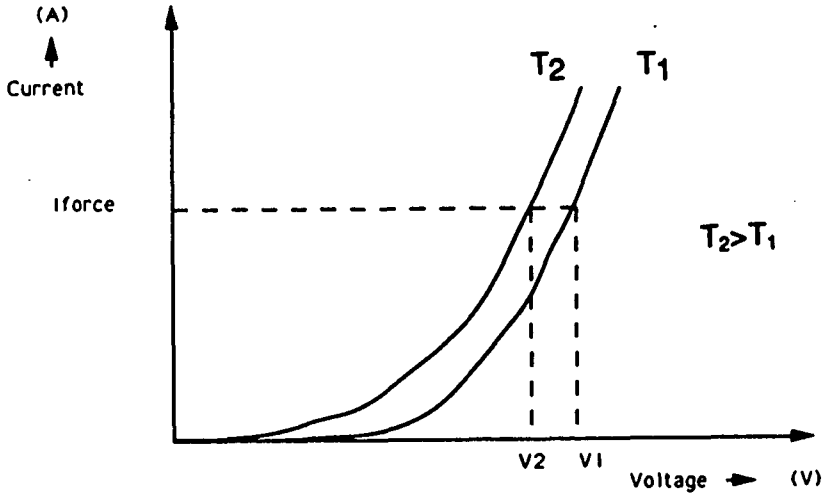


Fig. 3.7: Current vs. voltage characteristics at two different temperatures.

Thus, to reduce the effect of temperature, a temperature-control unit was installed. The unit keeps the temperature of

the chuck constant within 0.1 °C.

The errors due to temperature assuming no temperature control of the chuck, are discussed next. The slope of the current vs. temperature characteristic is 1.76 pA/°C, and the slope of the voltage vs. temperature characteristic is 1.47 mV/°C. The measured current at 15 V is 550 pA, and assuming a 1 °C variation in the chuck temperature, this results in a relative error of 1.76 pA/550 pA which is 0.32 %. At approximately the same conditions, forcing 1 nA and measuring 15.3 V results in a relative error of 1.47 mV/15.3 V which is 0.0096 % with the same temperature variation in the chuck. Therefore, measuring voltage offers a smaller error compared to measuring current for chucks that are not temperature controlled.

The increase of current at with temperature can be explained by considering the barrier height at the oxide-silicon interface. As mentioned in [3], this barrier height is reduced by increasing the temperature. The smaller barrier height causes the leakage to increase at low fields. At higher fields, the current is dominated by tunneling, so that the increase of current due to temperature is not significant anymore.

Another temperature consideration is examined by Monkowski [4] who found that temperature affects the low-field breakdown. Low-field breakdown is defined as a current tran-

sient of 10 nA, when a voltage ramp is applied which generates an electric field rising at 1MV/cm/s. In a 1000 Å gate-oxide capacitor the low-field breakdown decreased from 26 V to 15 V as the temperature was raised from 20 °C to 300 °C.

Therefore, having in mind the temperature dependence of current for the various testing procedures, control of chuck temperature is essential.

The second factor affecting the measurement is light. It was found that light increases the leakage current. This can be explained by the fact that illumination causes carrier generation. The experimental procedure for investigating this factor was to measure the current at a given voltage with light and without light. The test conditions were 3 s delay, 1024 samples, and constant wafer temperature; the same as during device automatic test. The forcing voltage was 15 V and the silicon surface underneath the gate was in accumulation. The nominal current at this bias was approximately 0.5 nA. The current measured with light was higher in most of the fields than the current without light in the same fields. The difference was as high as 1 nA. In some fields no change of current was noted and this is the result of the variation of the light flux of the fluorescent lamp of the room with time. The wafer map in Fig. 3.8 shows the difference between current measured with light and without light. Since the photocurrent adds to the measured current, the dif-

ference is normally positive. In some instances, however, a small negative change on the order of 10 pA was observed.

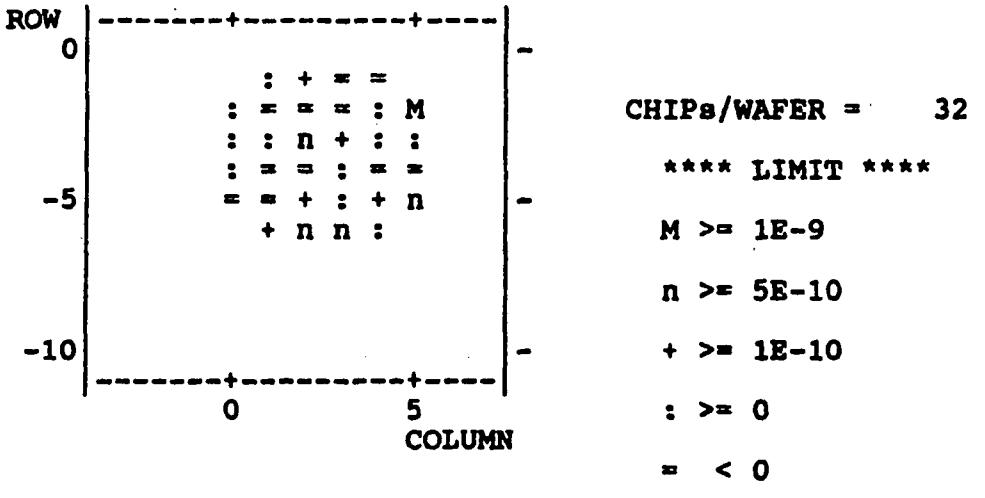


Fig. 3.8: Wafer map of a device showing the difference in current at 15 V with the light ON and the light OFF.

This can be explained by electron trapping which is considered in more detail in section 3.4. The measurement without light was done first and the measurement with light was done second. If there is no light flux, the two currents must be approximately the same. But since some electrons are trapped in the oxide during the first run, the current in the second run will be slightly less. The electon trapping at 15 V affects the device characteristics temporarily. After a short time the device characteristics recover by a detrapping mech-

anism. To avoid the presence of light during tests, the prober is covered with a black opaque plastic foil, thus creating a completely dark environment around the wafer.

The third factor to consider is the noise level. The instruments measure a current I_m where $I_m = I_a + I_n$. The current I_n is the stray leakage current measured when no device is connected and its value has been established to be 240 fA in section 2.4. I_a is the device current. Measurement methods were suggested in section 2.4 for reducing the noise. In addition to that, by measuring at a region of the IV characteristic where the measured current is high compared to the noise, the effect of noise is minimized. If a 100:1 signal to noise ratio is desired, then the measured value must be approximately 24 pA. However, the level of the current is limited by the fact that the device might be over-stressed. Therefore, the effect of over-stressing is investigated next.

3.4 ELECTRICAL STRESSING

Before deciding on a forcing variable, a test must be done to verify that the forced excitation does not produce irreversible changes in electrical characteristics. Such electrical over-stressing of the devices must be avoided, because one would lose control of the contamination monitor-

ing experiment.

The effect of electrical stressing was checked by taking IV plots of a device from 0 to 16 V twice. Capacitors with area of $1X10^{-4}$ cm^2 and $4X10^{-4}$ cm^2 were examined. It was observed that the resulting characteristics were identical except for a four-fold difference in current. Also, no shift was observed in the CV plots of the device taken before and after the IV plot was taken, indicating no change in charge trapped in the oxide.

When the IV plot was extended from 16 to 20 V, i.e. the oxide was stressed up to 11 MV/cm, the current at a given voltage was less in the second plot than in the first, especially beyond 16 V, which corresponds to 8.9 MV/cm. The reduction reached 10% in some cases. In Fig. 3.9 the two IV characteristics of a $4X10^{-4}$ cm^2 capacitor are shown before and after stressing. The CV plot after stressing was shifted to the left, which resulted in a 1 V shift of the flatband voltage. This indicates added positive charge in the oxide.

The effects of electrical over-stressing are also mentioned by Itsumi [5]. He found that after stressing above 8 MV/cm a shift of the CV plot to the left occured. At 9 MV/cm the shift was -5 V and at 10 MV/cm the shift was -10 V.

When VI plots were taken, similar results were seen. The current at a given voltage is lower in the second plot. Charge generation is obtained when a current of 10 nA or hig-

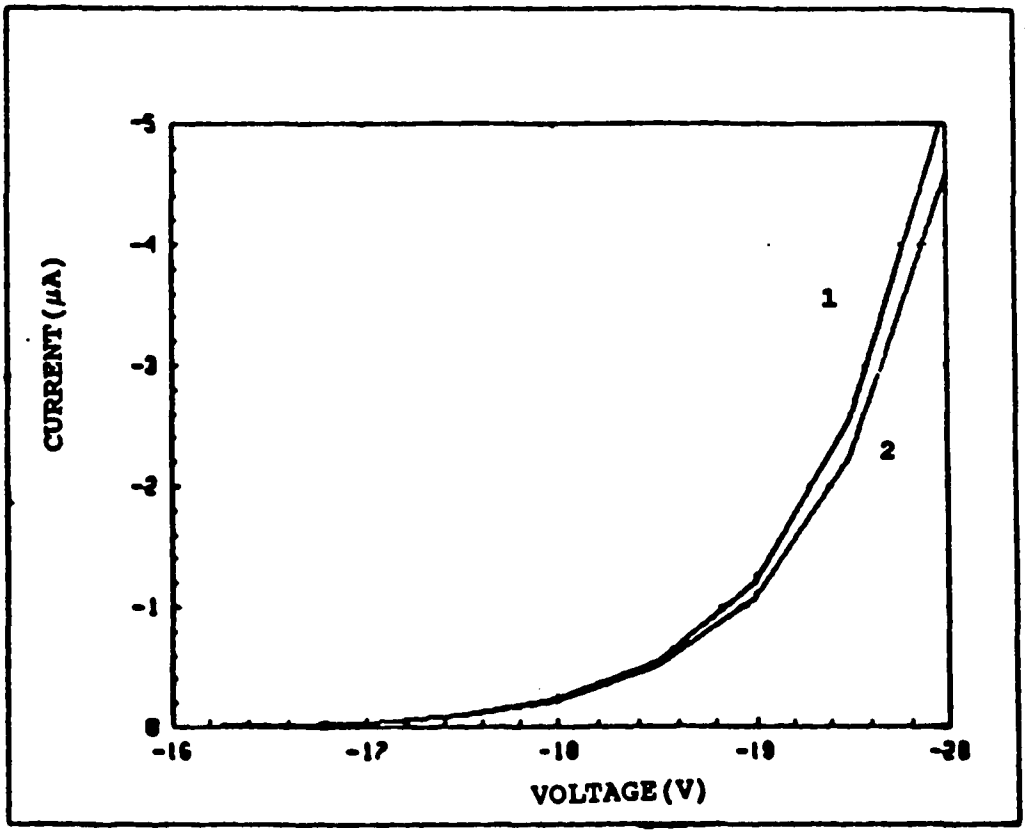


Fig. 3.9: IV characteristics of a $4X10^{-4}$ cm^2 capacitor. Characteristic 1 was taken first, followed by characteristic 2.

her is forced through the $1X10^{-4}$ cm^2 capacitor. It was found also that the $1X10^{-4}$ cm^2 area capacitor breaks down catastrophically when 0.1 mA or more is forced, which corresponds to a current density of 1 A/cm^2.

Therefore, for contamination experiments, measurements are reproducible only at electric fields below 8.9 MV/-

cm. At higher fields the electrical characteristics are affected because charge is generated in the oxide. Therefore, any measurements above 8.9 MV/cm can be done only after all low field measurements for a device have been completed. The very last measurement to be done is the catastrophic breakdown test which can be done only once. The reduction of current above 16 V was also observed when the silicon underneath the gate was in inversion, with the only difference being the slightly higher measured current compared to accumulation.

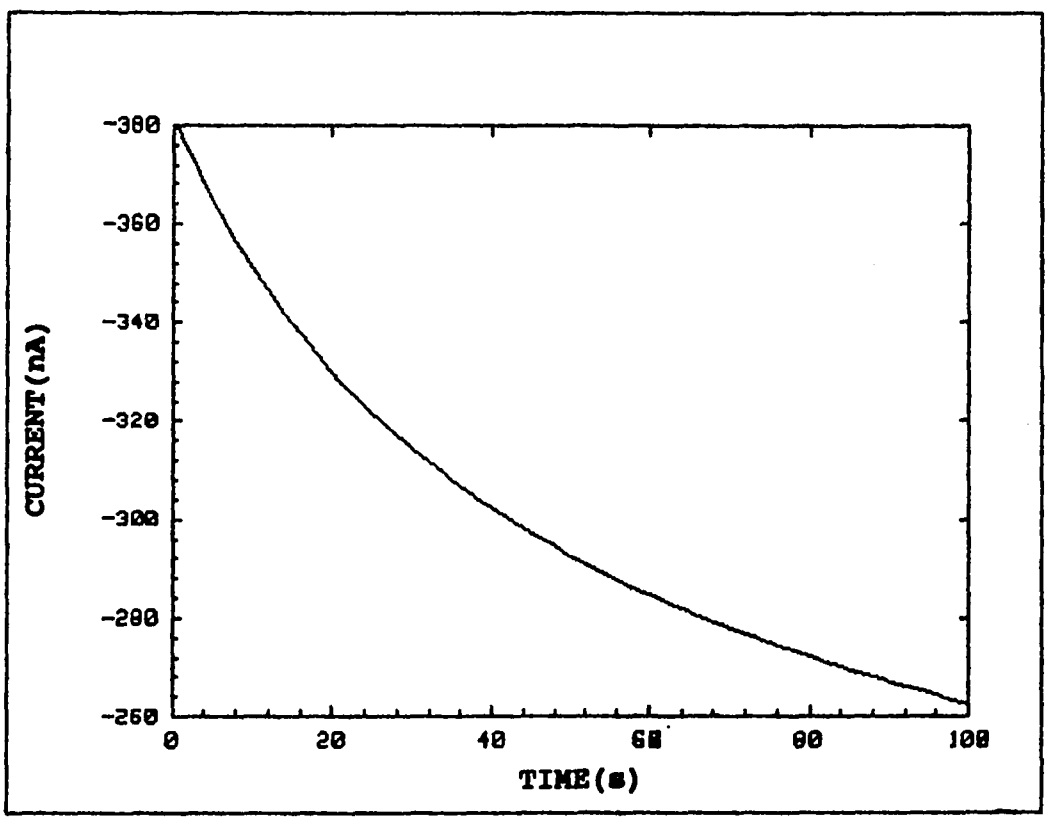


Fig. 3.10: Current at 18 V vs. time characteristic of a $4X10^{-4}$ cm^2 capacitor.

Another point which deserves careful consideration is the current versus time characteristic for the oxide, stressed above 16 V. The procedure for obtaining the I-t characteristic was the same procedure described in section 2.4. The I-t plot at -18 V bias for a $4X10^{-4}$ cm^2 capacitor is shown in Fig. 3.10. One notes that the current decreases from 380 nA to 260 nA in 100 s.

Previous investigators [6] discovered the same behavior. Closer examination of the decay shows that the current fits a relationship with slope of 1/t. No physical explanation was ever found. Similar behavior was seen when the silicon underneath the gate was in the inversion.

The same effect is mentioned by Holland [7]. The applied bias was -16.5 V for a p-type substrate for a 130 Å capacitor which corresponds to an electric field of 12.7 MV/cm. The bias was close to the intrinsic breakdown. The current density was reduced from 1 A/cm^2 to .002 A/cm^2 until the oxide broke down. The oxide broke down after 190 s under the above conditions. The decrease of current with time was explained by Holland as the effect of electron trapping. The same explanation is given by Shinada [8], and Kao [9].

The V-t characteristic shows similar behavior to the I-t characteristic. The voltage increases with time, which is equivalent to saying that the current decreases with time.

3.5 CURRENT TRANSPORT

The diagnostic tool for studying the current transport in gate oxides is the IV plot. The IV plot is a graphical representation of applied gate voltage versus measured current into the gate. From the IV characteristic a voltage can be determined, which gives a current sufficiently higher than the noise level.

A routine was written that forces voltage between the gate and the grounded substrate. The current flowing into the gate is measured. The user can choose the starting voltage, the final voltage, and the step. Choosing a sufficiently high voltage as the final voltage of the sweep, one can find the intrinsic breakdown voltage by measuring the voltage where the resistance becomes very small. Small resistance is measured at the portion of the IV characteristic where the slope is almost infinite, i.e., there is no variation of the voltage with current.

Before current transport is discussed it is important to define the two breakdown voltage categories in the oxide. The first category is the intrinsic breakdown. Intrinsic breakdown voltage is the breakdown voltage of the defect-free oxide. The second breakdown voltage category is the low-field breakdown. This breakdown mechanism occurs at low-field and there is a consensus among researchers that this is

due to defects in the oxide.

A definition of the intrinsic breakdown can be given by considering the electron-avalanche mechanism. A critical electric field exists above which electrons are accelerated to an energy sufficient to break bonds in the silicon dioxide and to produce a destructive electronic cascade, resulting in the destructive breakdown of the oxide [10]. At breakdown, the oxide passes high current which produces a localized destruction of the dielectric. This causes a conductive filament, shorting the polysilicon-gate with the silicon substrate [11].

The intrinsic breakdown can be classified into two categories. The first category is the time-dependent dielectric breakdown (T.D.D.B.) which is obtained at a constant voltage. If a voltage slightly below the breakdown voltage is applied, then after a short time, on the order of one ms the oxide breaks down. Thus, to avoid T.D.D.B. the lowest integration time should be used when measuring the intrinsic breakdown. The second category is the time-zero breakdown (T.Z.B.D.) obtained by applying a voltage ramp as defined by Nguyen [3]. In the experiments described in this thesis the time-zero breakdown is measured. The term "time-zero" is not absolutely correct because of the finite period introduced by the integration time. One sample is used in the measurements, which accounts for 246 μs. To get an estimate of the time

involved to cause breakdown when a constant voltage slightly smaller than the breakdown voltage is applied, data from Kao's [9] work are used. When the applied field was 11 MV/cm the time to breakdown was on the order of $1X10^4$ s. When the electric field was 13 MV/cm the time to breakdown was reduced to 5 s. The closer one moves to the intrinsic breakdown voltage, the smaller the time to breakdown becomes. Hence, as the applied voltage approaches the breakdown it is advantageous to have the smallest possible measuring period in order to minimize the time-dependent effects.

One important fact concerning the thickness dependency of low-field breakdown recovery is stated in Osburn's paper [12]. It is stated that if the oxide is thick, the device can recover from low-field breakdown by self-healing, and therefore the intrinsic breakdown voltage can also be measured. In thin oxides, however, both breakdown categories are destructive. Thus, once a low-field breakdown occurs, the final breakdown can not be measured. Therefore, since the wafers used in this thesis were processed for 180 Å, any low-field breakdown was destructive. In the same paper [12], the doping dependence of the final breakdown dependence is examined. It was shown experimentally that the breakdown voltage decreases with doping and the decrease is more pronounced for phosphorous doping. The effect of doping becomes as large as 20% for oxide thickness of 200 Å. The substrate of

the gate oxide capacitors used in this thesis are doped with boron; therefore a smaller decrease of breakdown is expected due to doping than the case of phosphorous doping.

In order to study the current transport in the oxide, a rough estimation of the intrinsic breakdown is needed to determine the range of the sweep. Initially, the voltage is swept up to 30 V which is high enough to cause breakdown in the 180 Å oxide. A negative voltage was applied to accumulate the silicon surface and apply all the voltage across the

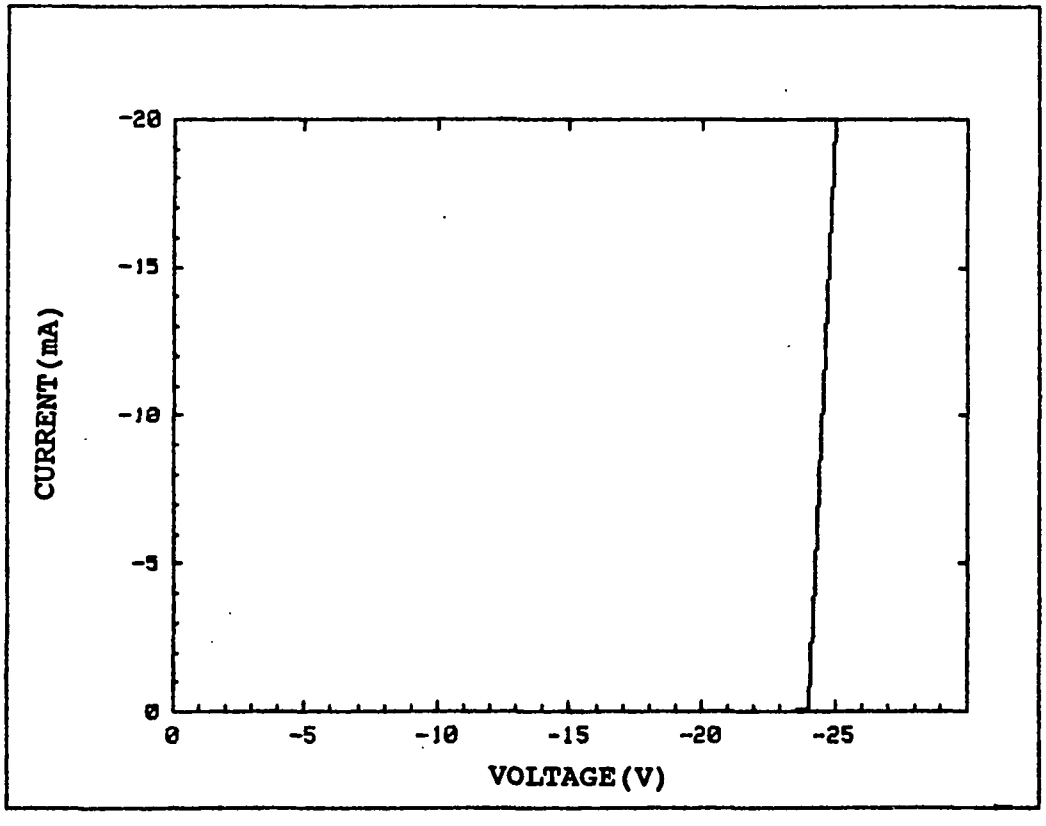


Fig. 3.11: IV characteristic of a $1X10^{-4}$ cm^2 capacitor swept from 0 to -30 V.

oxide. The intrinsic breakdown can be measured, provided that the device does not break down earlier due to defects in the oxide. Voltage was swept from 0 to -30 V with steps of 1 V. The test was done on a wafer with the lowest contamination level, so that the possibility of low field breakdown was minimized. Breakdown voltage was interpreted as the voltage where a transition to the low resistance region was observed. In Fig. 3.11 the IV characteristic of a $1X10^{-4}$ cm^2 capacitor is shown. The capacitor broke down at 24 V. At 24 V there is a small variation of voltage with current, which implies small resistance. Measurements for other types of capacitors were made and it was found that the capacitors break down between 22 V and 25 V, which corresponds to fields from 12.2 MV/cm to 13.9 MV/cm. These values are comparable with values found by Lin [13]. His breakdown-voltage data indicate that the intrinsic breakdown strength is oxide dependent. He found the breakdown was 9 MV/cm for a 500 Å oxide and 15 MV/cm for a 100 Å oxide. Thus, a lower oxide thickness leads to increased breakdown strength. Using the two experimental values and linear interpolation, intrinsic breakdown for the 180 Å oxide was found to be 12.45 MV/cm. If higher breakdowns are measured, this implies better quality oxides. Lower measured breakdown implies devices that are possibly affected by contamination.

Therefore, in order not to destroy the device, the voltage must be kept below 22 V. Characteristics were taken for electric fields ranging from 0 to 6.7 MV/cm. In this region, the current is down in the noise level of the instrument and therefore the fluctuations of current observed were due to the stray leakage current. This region is defined as the "pre-tunneling" region. The pre-tunneling region is also known as the "good quality region" because of the low leakage current.

The Fowler-Nordheim mechanism was observed in the past in thin gate oxides at high electric fields [3], [14], [6], [15], [8]. The current in the region above the pre-tunneling region and below breakdown was found to obey the Fowler-Nordheim mechanism for current transport. In this region, the current density J fits the equation

$$J = AE^2 e^{-B/E}, \tag{3.3}$$

where E is the electric field, A is a constant related to the barrier height and B is a constant related to the electron effective mass and to the barrier height.

The constant A is given by the equation

$$A = \frac{q^3}{8\pi h \phi_B}, \tag{3.4}$$

the constant B is related to the barrier height by the equation

$$B = \frac{8\pi (2m^*)^{1/2} \phi_B^{3/2}}{3hq} = B_0 \phi_B^{3/2}, \tag{3.5}$$

where m^* is the electron effective mass, ϕ_B is the barrier height, h is Planck's constant, and q is the electronic charge.

Equation 3.3 indicates that a plot of log J/E^2 vs. 1/E is a straight line. Therefore, if a straight line with negative slope is shown in such a plot, where J = I/A; E = V/t_{ox}; t_{ox} = 180 Å and A = $1X10^{-4}$ cm^2, Fowler-Norheim tunneling is indicated as the conduction mechanism. Fig. 3.12 illustrates

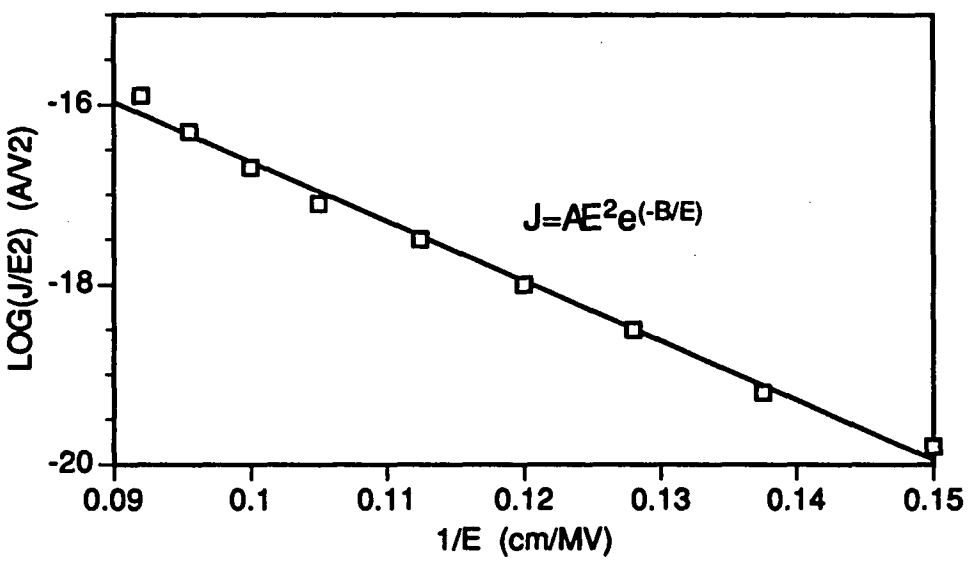


Fig. 3.12: Fowler-Norheim characteristic of a $1X10^{-4}$ cm^2 capacitor showing tunneling above 12 V.

a typical Fowler-Nordheim plot of a $1X10^{-4}$ cm^2 capacitor. The straight line implies that the capacitor current obeys the Fowler-Nordheim equation above 12 V, or when 1/E equals 0.15

cm/MV. The current transport with the silicon underneath the gate in inversion also obeys the Fowler-Nordheim mechanism, but the current level is slightly higher.

Another common way for displaying the various modes of current transport in the oxide is the log(I) vs. V characteristic. This plot has the advantage that a large range of currents can be displayed in the same plot. Linear IV plots display only the region with the highest currents. Fig. 3.13 shows such a characteristic for a $1X10^{-4}$ cm^2 capacitor in an uncontaminated wafer. The current is plotted vs. programmed forcing voltage. The pre-tunnelling region from 0 V to 14 V is distinguished by the fluctuations of the current, since the current in this region is low and close to the noise level of the instrument. The Fowler-Nordheim region is identified easily from the rapid increase of current with voltage from 14 V to 24 V. The oxide broke down at 23.5 V. When the oxide breaks down it conducts a high current which is limited by the compliance setting of the instrument at 20 mA. This prevents the destruction of the probe tips. At the point of breakdown the characteristic is a vertical straight line and the downward projection is the breakdown voltage. Similar characteristics were obtained by Lin [13] in which the current is also parallel to the log(I) axis at the breakdown point of the log(I) versus V characteristic. It is important to note that the "pre-tunneling " region extends up

to 12 V which corresponds to an electric field of 6.7 MV/cm. This shows that the oxide is of good quality, since the low-leakage region is extended up to 50 % of the possible measurable region before breakdown occurs. Other researchers such as Baglee [14] and Itsumi [5] found pre-tunneling regions up to 2.8 MV/cm and up to 6.5 MV/cm, respectively. An important comparison with Itsumi's results is that he found that elec-

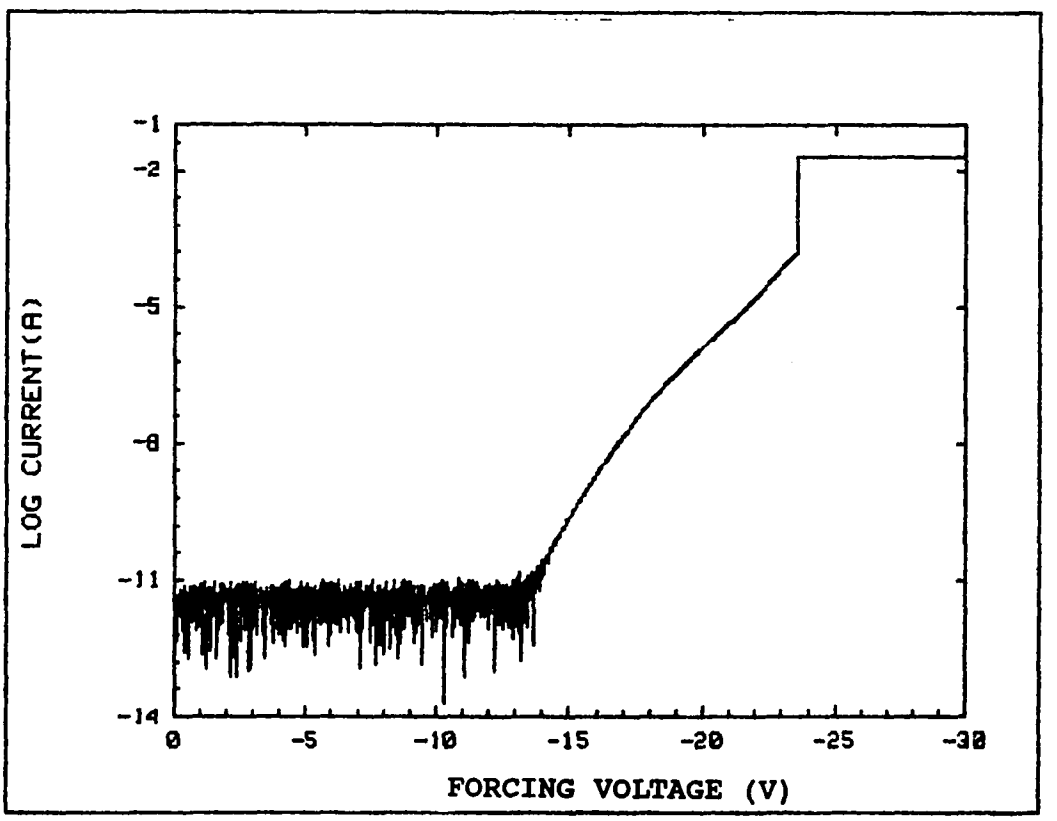


Fig. 3.13: Log(I) vs. forcing voltage characteristic of a $1X10^{-4}$ cm^2 capacitor, displaying the various current transport regions.

tron trapping occurs after 8 MV/cm whereas the tunneling starts at 6.5 MV/cm. In this thesis electron trapping was found to occur above 8.9 MV/cm whereas tunneling starts at 6.7 MV/cm. Therefore, electron trapping in the oxides investigated here starts 1.5 to 2 MV/cm higher than the tunneling emmision.

3.6. DETECTION OF OTHER TYPES OF CONTAMINATION

In the wafers under investigation, the objective is to determine the effects of a specific species of contaminant, namely iron introduced via the BOE. Therefore, other types of contamination should be avoided. One very frequent type is ionic contamination resulting from mobile ions in the oxide, particularly sodium. The absence of these contaminants needs to be established before other investigations are done. The well-known method to detect this type of contamination is the temperature-bias stress and CV measurements.

Sodium ions in the gate oxide cause a shift in the CV curve. Of particular interest is the shift of the flat band voltage which is a measure of mobile ion concentration. If a negative gate bias is applied, all the sodium ions are pushed to the metal-oxide interface and the flatband voltage shift is zero. A positive gate bias pushes the ions to the oxide-

silicon interface and the flatband shift is maximum. The equation of the flatband shift is given by:

$$\Delta V_{fb} = \int_0^{t_{ox}} \frac{x\varrho(x)\,dx}{\epsilon_{ox}\epsilon_0} \qquad (3.6)$$

The time required for temperature stressing is calculated by considering the diffusivity of the ions. In this case sodium is considered. Generally the diffusivity D is given by

$$D = D_0 e^{-E/kT} \qquad (3.7)$$

For sodium in silicon dioxide, D_0equals 6.9 cm^2/s and E = 1.3 eV. The temperature of 164 °C, which is one of the preset temperatures of the temperature control unit, gives a diffusivity of $6.54X10^{-15}$ cm^2/s. Using the Einstein relation, relating the mobility and diffusivity, the mobility can be estimated. Then, the drift velocity for a given field can be found and consequently the time needed for the sodium ions to cross the 180 Å oxide. It was estimated that the sodium ions need 4 s to cross the 180 Å oxide if the applied voltage is 5 V.

The procedure used for detecting mobile ions is as follows:

1) A CV plot is taken at room temperature.

2) Then, 5 V are applied to the gate with the wafer at 164 °C for 8 min to ensure that all the ions cross the oxide. Then, the wafer is cooled to room temperature with the bias still applied. A second CV plot is taken when room temperature is

reached.

3) Then, -5 V are applied to the gate with the wafer at 164 °C for 8 min. Then, a third CV plot is taken after the wafer is cooled down to room temperature. During cool-down the gate voltage remains applied.

Devices were tested, using the above technique. Two different oxide areas were examined. The areas were $1X10^{-4}$ cm^2 and $4X10^{-4}$ cm^2. The test covered five different fields for each different area. No measurable shifts in the CV plot were observed. This proves that no measurable concentrations of mobile ions are present in the wafer.

3.7. STUDY OF THE BARRIER HEIGHT

The study of the barrier height leads to the explanation of change in leakage current or the event of low-field breakdown due to contamination. Previous work by Honda [1] showed that contamination had lowered the barrier height at the oxide-silicon interface. In his experiment, iron ions were implanted and the oxide thickness was 300 Å. In a different experiment, also by Honda [15], the silicon wafer surfaces were intentionally contaminated with iron or nickel or copper. The study showed that the barrier height at the metal-oxide interface was lowered by 1 eV.

The barrier height at the metal-oxide interface is studied by driving the Si surface underneath the gate into accumulation. This requires a negative voltage applied to the gate. The barrier height at the oxide-silicon interface is studied by applying a positive voltage to the gate, which causes inversion of the silicon surface. The definitions of the two barrier heights are illustrated in Fig. 3.14.

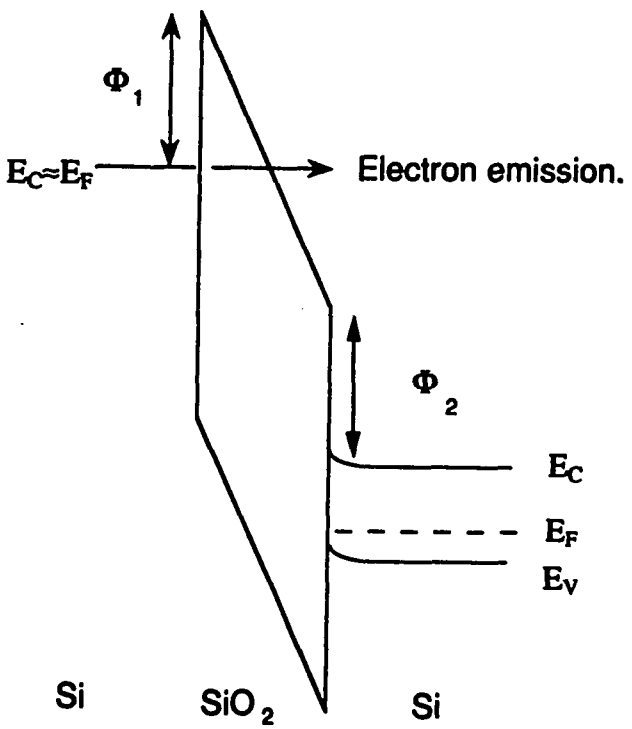


Fig. 3.14: Definition of the barrier heights at the two interfaces of the gate oxide; gate negatively biased.

Fig. 3.14 displays also the tunneling mechanism. When high

electric field is applied to the oxide, the triangular barrier gets thinner and electons penetrate the oxide and reach the substrate. The current density for tunneling is given by Eqn. 3.3. Taking the natural logarithm of both sides yields

$$\ln(J/E^2)=\ln(A)-B/E \qquad (3.8)$$

Converting to logarithms to the base 10 in order to obtain correspondence with the plot of Fig.3.12, leads to

$$\log(J/E^2)=\log(A)-B/2.3E. \qquad (3.9)$$

The slope of the characteristic is then given by the derivative

$$d(\log(J/E^2)/d(1/E)=-B/2.3. \qquad (3.10)$$

The constant A is given by Eqn. 3.4, and the constant B is given by Eqn. 3.5.

The constant B_0 defined in Eqn. 3.6 can be estimated by assuming $m^* = 0.5m_0 = 0.5\times9.11\times10^{-31}$ kg

The value of B_0 is thus estimated to be 7.53×10^{37} $m^{-2}kg^{-1/2}sC^{-1}$. Then, B is given in terms of B_0 and the barrier height Φ by

$$B = B_0\Phi^{3/2} \quad . \qquad (3.11)$$

Eqns. 3.10 and 3.11 can be combined to determine the barrier height from the IV data by the equation

$$\Phi_B = \left[\frac{2.3}{B_0}\times\frac{d[\log(J/E^2)]}{d(1/E)}\right]^{2/3} \qquad (3.12)$$

Eqn. 3.12 gives the barrier height at a specific interface. As mentioned earlier, if the voltage is negative, the barrier height at the metal-oxide interface can be calculated. Positive voltage characterizes the oxide-silicon interface.

To estimate the barrier height lowering, IV plots with the silicon surface in inversion and accumulation were taken with the gate voltage swept from 10 V to 20 V and from -10 V to -20 V respectively. Individual IV plots showed that the oxide shows Fowler-Nordheim tunneling above 12 V. Thus, the initial voltage is 2 V below the onset of tunneling, while the final voltage is 2 V below the lowest intrinsic breakdown observed on other identical devices. Because it was found previously that stressing the device beyond 16 V causes the electrical characteristics to change, this test was done af-

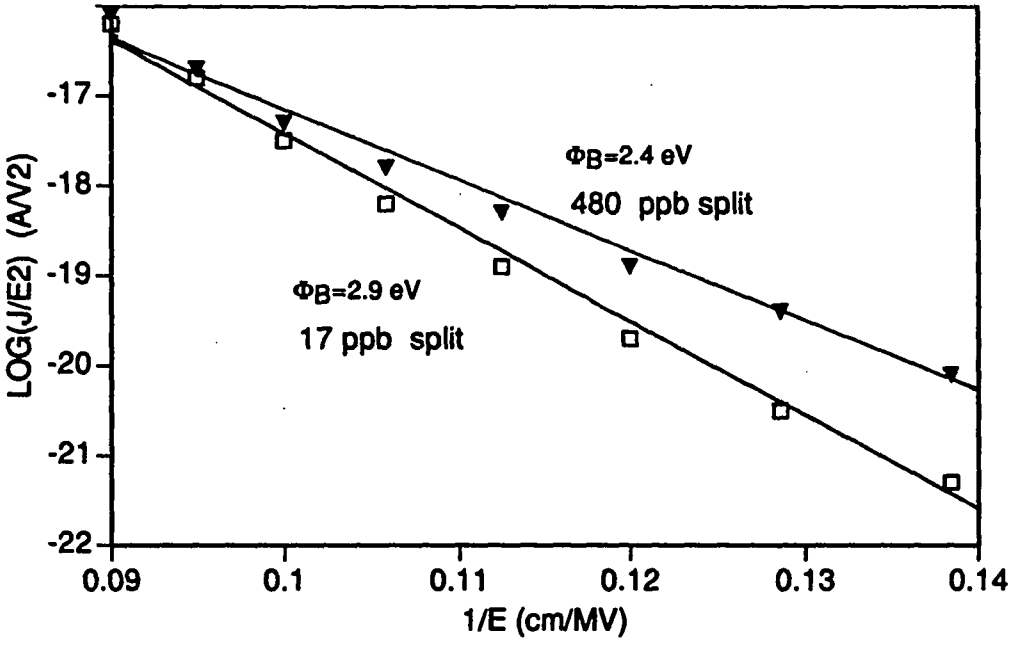


Fig. 3.15: Fowler-Nordheim characteristics of a $4X10^{-4}$ cm^2 capacitor at the 17 ppb split and at the 480 ppb split.

ter all low leakage measurements were completed.

A typical plot of $\log(J/E^2)$ versus $1/E$ for a $1X10^{-4}$ cm^2 capacitor in two wafers is shown in Fig. 3.15. By considering the slopes in accumulation and inversion, the barrier height at the two interfaces can be found. It was found that in some devices the barrier heights had been decreased. The calculation of the barrier height was done using eqn. 3.12 and the straight-line fits shown in the figure. The resulting barrier heights of the two plots of Fig. 3.15 are 2.9 eV and 2.4 eV. The reduction of the barrier height will tend to increase the conductivity, since more current is passed through the oxide.

3.8. RESULTS OF LEAKAGE MEASUREMENT

Automatic testing was performed for the $1X10^{-4}$ cm^2 capacitor. The testing was done on 10 identical devices, in 32 different fields, all 32 located inside the periphery of the chuck. The test conditions were dark environment, and constant wafer temperature. A 3 s time delay was used and 1024 samples were taken. The voltage was measured at 1 nA.

The data were processed by S.A.S. Scatter plots and histograms were obtained. Fig. 3.16 shows the scatter plot of the voltages at 1 nA from 32 different fields of an uncontaminated wafer and Fig. 3.17 is the scatter plot of a con-

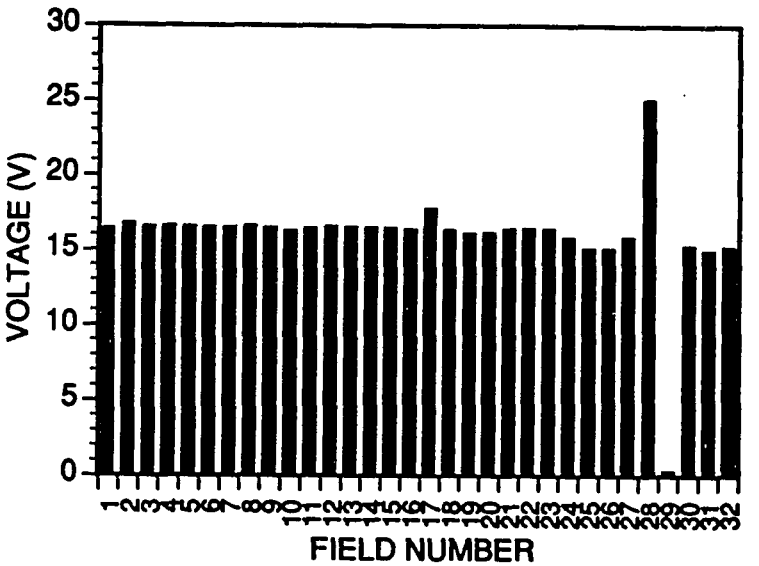


Fig. 3.16: Scatter plot of voltage vs. the field number for a $1X10^{-4}$ cm^2 capacitor at a non-contaminated wafer.

taminated wafer. Voltages of 25 V indicate that the program-med compliance value has been reached because of an open circuit or unsuccessful probing. The rest of the voltages can be classified into two categories. The first category is the category with voltages close to 15 V. These are voltages indicative of good devices. From IV plots taken manually, 15 V is the nominal voltage of a good, defect free device at 1 nA. The second category, devices possibly affected by contamination, shows low voltages below 1 V. The contamination had probably caused those devices to break down at low bias-

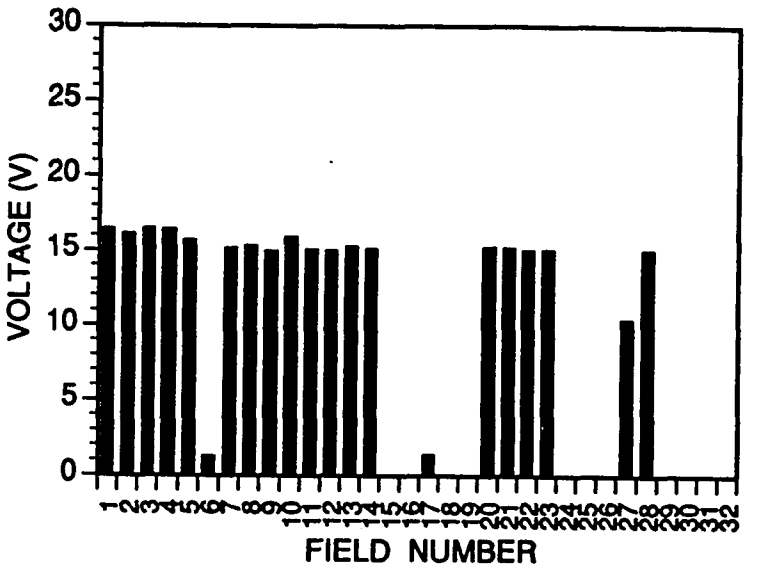


Fig. 3.17: Scatter plot of voltage vs. field number for a $1X10^{-4}$ cm^2 capacitor at a contaminated level.

es. The average measured voltage of a device excluding the low-voltage devices was compared between wafers with different contamination. By this statistic no conclusive correlation was found between leakage and contamination level, either because iron did not penetrate the oxide, or because the amount of iron was not enough to change the leakage. However, taking into account the failures measured, which were possibly the result of the introduced contaminant, makes the technique useful for contamination monitoring.

After the automatic test, devices which showed low-vol-

tage were tested by means of IV plots to examine the electrical characteristics. The devices with measured voltage of 56 mV and smaller showed ohmic IV characteristics with 1.5-56 MΩ resistance. A typical IV plot of a device showing an ohmic relationship between current and voltage is shown in Fig. 3.18. The slope of the characteristic shows a resistance of 5 MΩ. The devices with voltage greater than 56 mV showed IV characteristics indicating Fowler-Nordheim tunneling, but with larger currents than good devices. These devices were

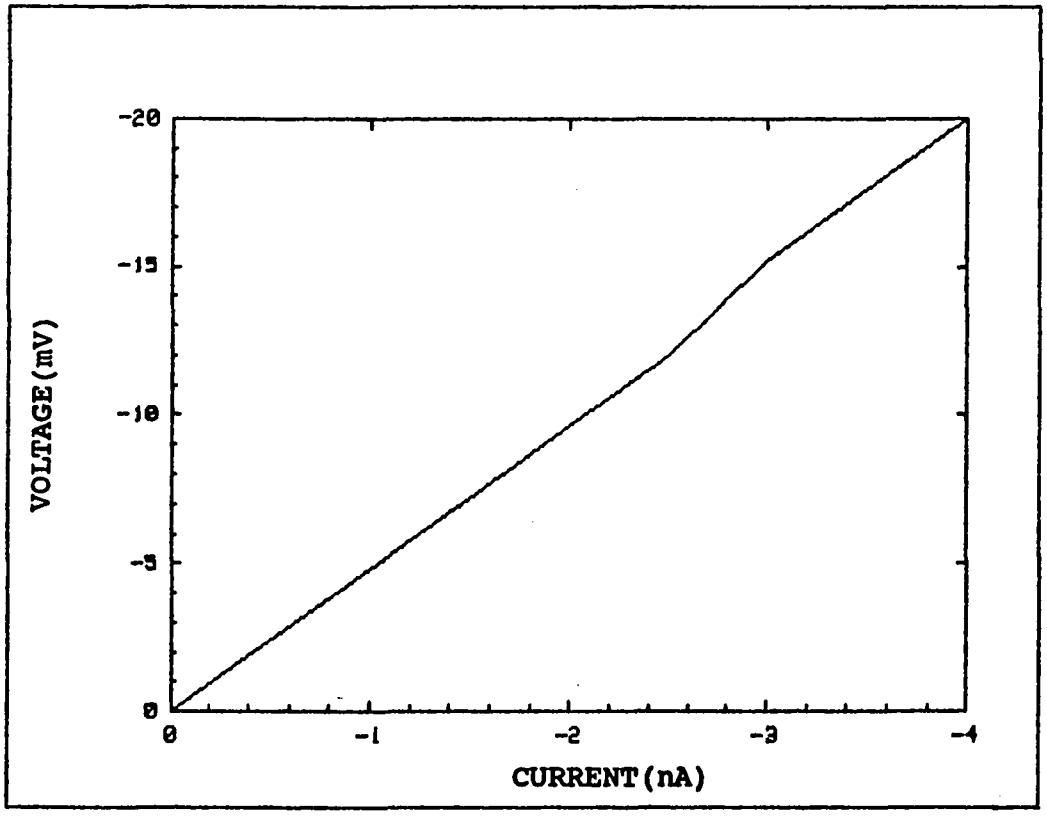


Fig. 3.18: IV characteristic of a $1X10^{-4}$ cm^2 capacitor showing low voltage at 1 nA.

not destroyed catastrophically, but they can be considered defective devices because of the high currents they pass even at low fields. An additional manual test of IV characteristics of the devices of the second category was done on a small sample of devices. To draw statistically significant conclusions, all of these devices need to be examined with a fully automated test of the IV characteristic, which is stored and processed easily by a statistical program.

Forcing 1 nA and measuring the voltage is a simple and fast technique which can be used to determine the yield of a specific process under the influence of a certain contaminant. A lower limit of measured voltage at 1 nA can be selected by the test engineers to define the "good device" region. Devices having voltage less than the lower limit are considered defective. One might include the devices that are short-circuited and the devices that are passing high currents at low fields. This is achieved by accurately defining the lower voltage limit. The forcing current must be scaled according to the area of the capacitor in order to apply the same current density for all capacitors of different area.

The technique of forcing 1 nA does not give the biasing point at which low-field breakdown occurs, because it is possible that a device breaks down at a lower current density. To measure the current density where the oxide breaks down one must sweep the current and monitor the voltage. When the

voltage suddenly drops to a few mV which implies low-field breakdown, then the sweep is terminated and the current is recorded. However, a more useful parameter to measure would be the critical electric field defined in section 1.4. A better technique to measure the critical electric field, is to sweep the voltage, and when a failure current is measured, then the voltage is recorded as the critical electric field causing breakdown. This technique is discussed futher in section 4.2.

CHAPTER 4: MEASUREMENT OF INTRINSIC AND LOW FIELD BREAKDOWN

4.1. ANOTHER METHOD FOR MEASURING INTRINSIC BREAKDOWN VOLTAGE

The intrinsic breakdown was not reported by any researcher to be affected by contamination. However, its value is a very important parameter since the low-field breakdown voltage can be compared to it.

The first method discussed to measure the intrinsic breakdown voltage of the gate oxide was the extraction of the breakdown voltage by making use of the IV plot. The breakdown was the voltage recorded when a transition of current was seen from a low to a high value. However, this method is very slow.

A method which appears to work, but does not, is the method of forcing a current in the breakdown region of the IV characteristic and measuring voltage. Unfortunately, even using only one sample, the measuring time of 246 μs involved to take the sample invalidates the measurement. The measurement fails because when the breakdown phenomenon occurs, the oxide is short circuited and only a small voltage drop is measured across the oxide. Thus, because of the measuring time involved, the system will record the small voltage drop,

which is not the parameter one wants to measure.

A superior technique was introduced which is faster and more accurate. The technique incorporates the use of the analog feedback unit (A.F.U.). The A.F.U. unit is used in conjunction with a voltage source and current monitor unit. The setup is shown in Fig. 4.1. The substrate is grounded, and a voltage source and a current monitor are connected to the gate. The feedback unit is connected across the two

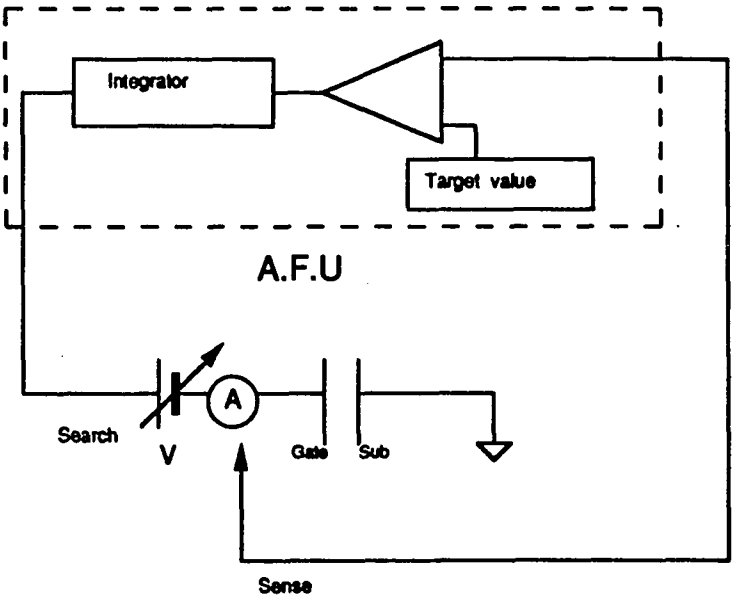


Fig. 4.1 Setup for measuring intrinsic breakdown voltage.

ports and controls the measurement. Voltage is swept from a voltage which is lower than the breakdown voltage, determined

from previous IV plots to be 22 V to 25 V for an uncontaminated wafer. Thus, the voltage is swept from 17 V to 30 V. The increment chosen is 0.01 V to give a maximum error of 0.01 V plus the instrument error. A negative voltage is applied to the gate, so that all the voltage is applied across the oxide.

Using the Log(I) vs. V plot shown in Fig. 3.13, a current value which definitely indicates breakdown is chosen. This failure current is a parameter required by the A.F.U. as a termination condition. The current chosen for the $4X10^{-4}$ cm^2 capacitor was 1 mA, which results in a current density of 2.5 A/cm^2. Voltage is swept and when this current is reached, the voltage is recorded as the breakdown voltage.

Identical devices of the same wafer from different fields showed similar results when the breakdown was measured using the IV plot. The breakdown is a one shot measurement and there is no way to compare the two techniques on one and the same device, but since the measurements taken at adjacent fields gave identical results, this proves that the technique is equally successful to the technique of extracting the breakdown from the IV characteristic. The testing time for measuring the breakdown using the feedback technique is about 4 s when the voltage is swept from 18 V to 30 V.

The above technique can be used to examine the effect of contamination upon final breakdown using the automatic test

program. A test was carried out testing devices with $4X10^{-4}$ cm^2. The voltage was swept from 10 V to 30 V with the silicon in accumulation. The target current was set to 1 mA. The breakdown voltages measured were in the range from 22 to 25 V.

4.2. MEASUREMENT OF LOW FIELD BREAKDOWN

The technique of forcing a current of 1 nA and measuring voltage gives the number of failures for a given device type. However, the current where the failure occurs cannot be found using this technique. As mentioned in section 3.8, it is more desirable to determine the electric field where the failure occurs. These failures were attributed to contamination in the oxide.

Many researchers have approached the problem of low-field breakdown and various test techniques were used. Monkowski [4] measures the low-field breakdown by using a voltage ramp of 1 MV/cm/s and interprets any transient of at least 10 nA as the point where breakdown occurs. In Honda's [1] approach, breakdown is the voltage which gives a current of 50 μA, with oxide area of $4X10^{-6}$ cm^2. In Baglee's [14] aproach, a stress voltage is applied for a short time and then a reference voltage of -1 V is applied to check for oxide short. If the oxide has not broken down, larger stress

is applied, followed by the low reference voltage. When an oxide short is obtained then the stress voltage at that point is recorded.

In this thesis a different approach was used which makes use of exactly the same setup described in section 4.1 for measuring the intrinsic breakdown. The only difference is that the sweep range is modified. Since low-field breakdown is investigated, the voltage is swept from 0 up to 15 V. The voltage of 15 V corresponds to 8.3 MV/cm. The sweep is limited to 15 V, because above 16 V the electrical characteristics change irreversibly, as described in section 3.4. Again, the step of the sweep is 0.01 V, in order to minimize the error. Normally, the nominal current for the 10^{-4} cm^2 capacitor is approximately 1 nA at 15 V. Hence, the current between 0 and 15 V is less than 1 nA. If the oxide breaks down in this region, a high current is passed through it. The failure current is set to 1 μA. When it is reached, the sweeping stops and the voltage is recorded. This voltage is the low-field breakdown. If the oxide is defect free, the 1 μA current is never reached. The instrument will indicate 15 V, which signifies a good capacitor. The failure current must be chosen independently of device area, because after breakdown, all the current passes through a few sites within the device where the breakdown has occurred, regardless of the area of the capacitor. The selection of the same failure

current for any area was investigated by Heiman [16]. Data of breakdown voltage versus area showed no correlation between breakdown voltage and area when the same failure current was selected.

Automatic testing was done for 20 identical devices of 10^{-4} cm^2 in 32 different fields. One contaminated and one uncontaminated wafer were tested. The contaminated wafer showed 252 defective capacitors out of 640, which is 39 % of

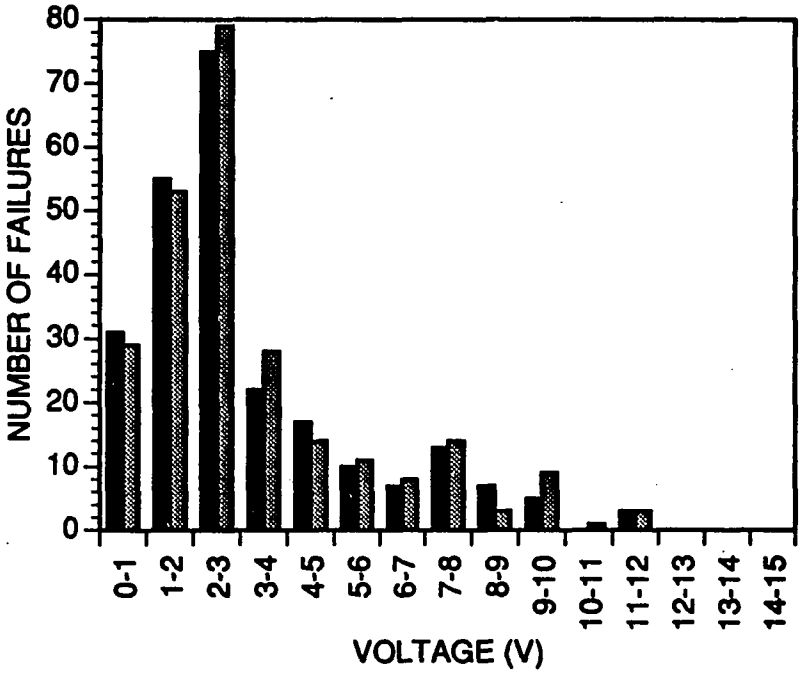


Fig. 4.2: Histogram of number of failures vs. voltage of 640 capacitors from a contaminated wafer. Sweep range was 0-15 V and the failure current was 1 μA. The first run is represented with black and the second run is represented with gray.

the total capacitors. Fig. 4.2 shows the histogram of failures. A defective capacitor is defined as any capacitor having a measured voltage smaller than 15 V, which means that in the interval from 0 to 15 V, the capacitor passed more than 1μA current. The number of failures in a given voltage range differ slightly in the two runs, because devices showing failures near the edge of a specific voltage range, changed voltage range in the second run. The uncontaminated wafer showed only one failure out of the 640 capacitors. Most failures are concentrated between 0 and 6 V, with the peak between 2-3 V.

CHAPTER 5. CONCLUSIONS AND FUTURE WORK.

5.1. CONCLUSIONS

Contamination was found previously to affect the integrity of the oxide of gate oxide capacitors. The effects of contamination can be monitored by electrical methods. The electrical measurements must be done by an automated test system so that large amounts of data are collected for statistical analysis. The system must reliably measure low currents. The HP 4062C test system and the installed interface introduce stray leakage current on the order of 200 fA. Therefore, low-bias measurements are limited to the pA range. The lowest stray leakage current was obtained when a 3 s delay was used and when the number of samples per reading was set to 1024.

The method of forcing current and measuring voltage can be used to relate the leakage to contamination, provided that the device does not break down. If the device breaks down, then comparison of the number of failures with contamination can be made.

The conditions for the above measurement and for the subsequent measurements was constant chuck temperature and

dark environment, since those factors were found to affect the measured values. Of great importance was the effect of electrical stressing. It was found that the application of electric fields higher than 8.9 MV/cm cause irreversible damage to the device characteristics. Other types of contamination should be investigated and especially ionic contamination.

The current transport mechanism of the devices was investigated. The current density at electric fields of 6.7 MV/cm or higher obeyed the Fowler-Nordheim characteristic which is the most common current-transport mechanism in thin oxides. The oxide broke down between 12.2 MV/cm and 13.9 MV/cm. Up to an electric field of 6.7 MV/cm the device current was not above the noise level.

The study of the barrier height is a very important parameter that needs to be investigated. It was found that the barrier height at some devices was lowered. The barrier height can lead to the explanation of the leakage current increase and the event of breakdown.

Due to defects in the oxide, probably introduced by contamination, a device might be destroyed catastrophically at low voltages. A technique is needed to measure the electric field where the failure occurs. The principle of the technique developed is that by sweeping the voltage and setting a failure current higher than the nominal current measured in

the range of the sweep, one can measure the breakdown if the failure current is reached. The same setup can be used to measure intrinsic breakdown by choosing the failure current higher than the current that caused identical devices to break down. Also, the range of the sweep must be wide enough to include the breakdown voltage measured for other identical devices.

5.2. FUTURE WORK

In this thesis, techniques were developed to investigate the effect of contamination upon some electrical parameters. Those techniques were inserted in an automated test program which performs DC parametric testing on wafers. More techniques should be developed to study more electrical parameters that might be affected by contamination. Improvements should be made on the automatic test program.

Time dependent breakdown is a very important electrical parameter for the yield and reliability of gate oxide devices. This parameter is obtained by applying constant voltage and measuring the time to breakdown. The time to breakdown depends on how close the applied voltage is to the intrinsic breakdown voltage. The smaller the difference between the two voltages, the smaller the time to breakdown will be. It is not efficient to test one device at a time, because in

order to measure a statistically acceptable number of devices, a huge amount of time is involved. Thus, the most efficient method is to access simultaneously many devices in various field sites on a wafer. In Boyko's paper [4], a method is described where electrical contact to 1000 capacitors is made by use of a "bed-of-nails" contact fixture. The time to failure is monitored by periodic scanning using a failure criterion of 10 μA. The test requires additional instruments and more programming code which were not available in the test system described in this thesis. This technique would be useful for determining the effect of contamination upon the time to breakdown. Due to defects in the oxide the capacitor is expected to break down earlier than if it were defect free.

A second parameter which is affected by contamination is the generation lifetime and surface generation velocity as reported by Honda [15]. Those parameters are extracted from the C-t characteristic. Contamination decreases the carrier lifetime and increases the surface generation velocity, as reported by Honda [15]. The contaminant used was also iron.

The test program can be improved by making the communication between program and user easier. One way to improve this is to make use of softkeys which make the interaction between computer and user easier. The second improvement is the introduction of error trapping. The program as it is now

does not provide error trapping. In the case of an error the user has to run the program again. This is sometimes confusing for new users. Error messages and codes should be inserted so as to redirect the user to the correct path. The third way the program can be improved is the test definition creation. The program as it is now requires the user to respond to two questions for each device test definition. Each definition requires 4 parameters to be entered. Sometimes only three parameters are required, but the user has to specify with zeroes the parameters that are not required. A more flexible approach would be a test definition system, in which the user responds to only one question per definition.

The program can also be improved by introducing intelligence into the code. For example, let's say a test is performed in which current is forced and voltage is measured in a gate oxide. Some devices would be classified as defective because of failure. The program must be able to open the data file and identify the devices with failures for further investigation. An example of further investigation is IV characterization which leads to the study of barrier height at a specific interface.

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