LILLIS, William Joseph, 1944-  
COMPUTER AIDED DESIGN OF INTEGRATED  
CIRCUITS.  
The University of Arizona, Ph.D., 1972  
Engineering, electrical

University Microfilms, A XEROX Company, Ann Arbor, Michigan

THIS DISSERTATION HAS BEEN MICROFILMED EXACTLY AS RECEIVED
COMPUTER AIDED DESIGN OF INTEGRATED CIRCUITS

by

William Joseph Lillis

A Dissertation Submitted to the Faculty of the DEPARTMENT OF ELECTRICAL ENGINEERING
In Partial Fulfillment of the Requirements For the Degree of DOCTOR OF PHILOSOPHY
In the Graduate College
THE UNIVERSITY OF ARIZONA

1972
I hereby recommend that this dissertation prepared under my direction by William J. Lillis entitled "Computer Aided Design of Integrated Circuits" be accepted as fulfilling the dissertation requirement of the degree of Doctor of Philosophy.

Dissertation Director

Date

After inspection of the final copy of the dissertation, the following members of the Final Examination Committee concur in its approval and recommend its acceptance:

*This approval and acceptance is contingent on the candidate's adequate performance and defense of this dissertation at the final oral examination. The inclusion of this sheet bound into the library copy of the dissertation is evidence of satisfactory performance at the final examination.
PLEASE NOTE:

Some Pages have indistinct print. Filmed as received.

UNIVERSITY MICROFILMS
STATEMENT BY AUTHOR

This dissertation has been submitted in partial fulfillment of requirements for an advanced degree at The University of Arizona and is deposited in the University Library to be made available to borrowers under rules of the Library.

Brief quotations from this dissertation are allowable without special permission, provided that accurate acknowledgment of source is made. Requests for permission for extended quotation from or reproduction of this manuscript in whole or in part may be granted by the head of the major department or the Dean of the Graduate College when in his judgment the proposed use of the material is in the interests of scholarship. In all other instances, however, permission must be obtained from the author.

SIGNED: William Joseph Tellis
ACKNOWLEDGMENTS

The author wishes to express his gratitude to Dr. D. J. Hamilton, Professor of Electrical Engineering at The University of Arizona, for his continued guidance and encouragement during the author's graduate program. The author would also like to thank R. Balda, J. Fossum, and V. Wells for their assistance and advice.
TABLE OF CONTENTS

LIST OF ILLUSTRATIONS ........................................ vi
LIST OF TABLES ................................................ vii
ABSTRACT ................................................................ viii

CHAPTER

1. INTRODUCTION .................................................. 1
2. DERIVATION OF DEVICE PARAMETERS ...................... 9
   2.1 Assumptions and Resulting Device
       Configuration .................................................. 9
   2.2 Derivation of Parameters .................................. 14
   2.3 Choice of Specifications .................................. 19
   2.4 Diffusion Process and Results ......................... 25
3. RELATIONS AND APPROXIMATIONS ......................... 30
   3.1 The Junction Depletion Regions ....................... 30
   3.2 Conductivity as a Function of
       Concentration .................................................. 38
   3.3 Representation of Net Profile .......................... 40
4. THE DESIGN PROCESS .......................................... 53
   4.1 The Design Loop ........................................... 53
   4.2 The Monitor ................................................ 55
   4.3 The Net-Profile Approximation ......................... 57
   4.4 The Depletion-Versus-Voltage
       Calculation .................................................... 62
   4.5 The Placement Routines ................................... 64
   4.6 The Calculation of Sheet Conductance ................ 65
   4.7 Determination of Gaussian Constants ................. 68
   4.8 The Preparatory Operations ............................ 71
   4.9 Pinch-Resistor Initial Estimate ....................... 73
   4.10 Evaluation of Pinch-Resistor
       Structure ...................................................... 75
   4.11 Adjustment of Pinch-Resistor Diffusion .............. 78
   4.12 JFET Initial Estimation of $C_0$ and $Y_0$ ............ 79
   4.13 Evaluation of JFET Parameters ....................... 81
   4.14 Revision of JFET Diffusion Constants ......... 84
# TABLE OF CONTENTS—Continued

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5. EXAMPLES</td>
<td>86</td>
</tr>
<tr>
<td>5.1 The Substrate Pinch Resistor</td>
<td>86</td>
</tr>
<tr>
<td>5.2 The Double-Diffused Pinch Resistor</td>
<td>92</td>
</tr>
<tr>
<td>5.3 The Double-Diffused JFET</td>
<td>96</td>
</tr>
<tr>
<td>6. CONCLUSIONS AND RECOMMENDATIONS</td>
<td>103</td>
</tr>
<tr>
<td>6.1 Summary</td>
<td>103</td>
</tr>
<tr>
<td>6.2 Recommendations</td>
<td>105</td>
</tr>
<tr>
<td>LIST OF REFERENCES</td>
<td>106</td>
</tr>
</tbody>
</table>
LIST OF ILLUSTRATIONS

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Integrated Circuit Channel Devices</td>
<td>4</td>
</tr>
<tr>
<td>2.1</td>
<td>The Geometry of a Simple Rectangular Channel Device</td>
<td>10</td>
</tr>
<tr>
<td>2.2</td>
<td>Channel-Device Regions</td>
<td>12</td>
</tr>
<tr>
<td>2.3</td>
<td>Physical Interpretation of ( g_m ) and ( g_{22} )</td>
<td>18</td>
</tr>
<tr>
<td>2.4</td>
<td>General p-n Junction</td>
<td>22</td>
</tr>
<tr>
<td>3.1</td>
<td>The Gaussian Profile and Its First Two Derivatives</td>
<td>46</td>
</tr>
<tr>
<td>3.2</td>
<td>The Gaussian Profile and Its Approximation</td>
<td>47</td>
</tr>
<tr>
<td>3.3</td>
<td>Detail of Approximation</td>
<td>48</td>
</tr>
<tr>
<td>4.1</td>
<td>The Overall Design Loop</td>
<td>54</td>
</tr>
<tr>
<td>4.2</td>
<td>The Monitor Routine</td>
<td>56</td>
</tr>
<tr>
<td>4.3</td>
<td>Flow Chart of NTPRFL</td>
<td>58</td>
</tr>
<tr>
<td>4.4</td>
<td>Accuracy of 1 Per Cent Profile Fit</td>
<td>61</td>
</tr>
<tr>
<td>4.5</td>
<td>Flow Chart of DPLVSV</td>
<td>63</td>
</tr>
<tr>
<td>4.6</td>
<td>Flow Chart of SHTCON</td>
<td>66</td>
</tr>
<tr>
<td>4.7</td>
<td>Flow Chart of COCY</td>
<td>69</td>
</tr>
<tr>
<td>4.8</td>
<td>Flow Chart of INPUT</td>
<td>72</td>
</tr>
<tr>
<td>4.9</td>
<td>Flow Chart of GUES1</td>
<td>74</td>
</tr>
<tr>
<td>4.10</td>
<td>Flow Chart of TEST</td>
<td>76</td>
</tr>
<tr>
<td>4.11</td>
<td>Flow Chart of FETGS</td>
<td>80</td>
</tr>
<tr>
<td>4.12</td>
<td>Flow Chart of EVAL</td>
<td>82</td>
</tr>
</tbody>
</table>
## LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 P-Type Material Conductivity Approximation Constants</td>
<td>41</td>
</tr>
<tr>
<td>3.2 N-Type Material Conductivity Approximation Constants</td>
<td>42</td>
</tr>
<tr>
<td>5.1 Pinch-Resistor Design Example</td>
<td>87</td>
</tr>
<tr>
<td>5.2 JFET Design Example</td>
<td>97</td>
</tr>
</tbody>
</table>
ABSTRACT

A design process using a digital computer is presented for junction-type channel devices in silicon monolithic integrated circuits. Both the pinch resistor and field-effect transistor are considered. Specified device characteristics are used to determine the parameters of a Gaussian-type top-gate diffusion profile into a known background profile in the wafer.

The characteristics of the device are developed in terms of its physical structure and the terminal voltages. The pinch-off voltage and the transconductance per unit Z/L are chosen as specifications for the field-effect transistor. The small-signal channel sheet conductance and its first derivative with respect to the drain-source voltage are chosen as specifications for the pinch resistor. These specifications are related to the position of the top-gate junction region, which is then related to the top-gate diffusion parameters.

Expressions are derived giving the junction depletion-region boundaries in terms of the net impurity profile and the total junction voltage. The representation used for conductivity as a function of net impurity concentration is given, and the approximation for the various impurity profiles is developed.
A computer-implemented iterative method is described for determining the diffusion parameters based on the above relations. The different segments of the design process and the linkage among them are presented.

The process is demonstrated by designing several pinch resistors and field-effect transistors in typical background profiles. Both substrate and double-diffused devices are considered. Experimental verification of the validity of the design process is demonstrated. The final device characteristics are calculated, as are the sensitivities of the specified parameters to the top-gate diffusion processing operations. The latter indicate the requirements in process control.
CHAPTER 1

INTRODUCTION

Silicon monolithic integrated circuit fabrication imposes many restrictions on the circuit designer. Two of the more formidable restrictions are the small number of device types and the limited range of their characteristics (Fitchen 1970, p. 6). With a processing schedule optimized for the n-p-n transistor, integrated circuits can be designed which successfully perform many operations. Nevertheless, conventional integrated circuits cannot meet several performance criteria, such as low power consumption and high input impedance.

For integrated circuits to meet these criteria, additional device types or an extension of the available device characteristics would be required. In particular, the availability of a range of channel-type devices would remove two of the circuit-design restrictions. Pinch resistors would extend the range of available resistor values, and junction field-effect transistors (JFET's) would be an additional device type.

Because of the importance of the present device characteristics, these channel devices must be incorporated into the existing structure with minimum additional processes.
The minimum number for an integrated circuit is one extra solid-state diffusion. The resulting channel device must have acceptable characteristics and these must be known beforehand. Thus it is necessary to determine the processing parameters of the diffusion into the known structure such that a channel device of specified characteristics results.

The basic junction-type channel device was analyzed first by Shockley (1952). He derived the static characteristics for a simple symmetric structure with uniform channel conductivity and abrupt-junction gates. Dacey and Ross (1953, 1955) extended the analysis of the structure and reported the first experimental confirmation of the analysis. Bockemuehl (1963) analyzed a three-terminal symmetric structure with arbitrary channel doping; Cobbold (1965) and Lindholm and Gray (1966) then analyzed the four-terminal arbitrarily doped structure. They gave the device parameters in terms of integrals over sections of the structure, then solved these equations for some idealized impurity profiles.

Vadasz (1966) examined the use of the surface-type field-effect transistor to obtain pinch resistors in the epitaxial layers of digital integrated circuits. However, the only JFET design aid published (Burger and Donovan 1968, pp. 277-278, 414-416) is for a device having a uniform channel and abrupt gate junctions. This is of little use when considering the integrated circuit structures shown in
Fig. 1.1. In the substrate device, the diffusion forming the top-gate junction extends into the channel, and the junction itself is far from abrupt. In the double-diffused structure, neither junction can be approximated by an abrupt model, nor is the channel uniform.

The primary objective of this study is to develop a design process for the three-terminal channel-device structures shown in Fig. 1.1. Certain device parameters are specified which are used to determine the characteristics of the top-gate diffusion into the known background. Due to the complexity of the expressions for device characteristics, the digital computer is required. Consequently, we develop approximations for the device structures and characteristics. Successful results are rapidly obtained for both device types. Good correspondence is seen between the characteristics of a designed device and measurements on a sample. The resulting prediction for the diffusion parameters can be used as design-center diffusion specifications and can be incorporated easily into the normal process for the circuit.

In the prior art the technique for adding a diffusion to the process schedule is to first estimate the junction depth and surface concentration required. Then experienced fabrication personnel make an educated guess for the diffusion schedule. Finally, the structure is fabricated and testing determines the device parameters. If they exceed the specification tolerances, new estimates for the
Fig. 1.1 Integrated Circuit Channel Devices
surface concentration and junction depth are made and the whole process is repeated.

The design process presented here reduces the number of trial-and-error steps resulting from just an estimation of the junction depth and surface concentration of the top-gate diffusion. The fabrication personnel are given the diffusion parameters as well as the resulting junction depth in the required profile. Their experience then can be directed toward the subtle processing variations necessary to achieve this end.

The accuracy of the design process depends mainly on the accuracy to which the background is known. However, since this is the standard profile of impurity concentration versus distance into the wafer we may expect that it is well known. The design process also indicates the sensitivity of the device parameters to variations in the top-gate diffusion. Thus it predicts the difficulty of successful fabrication. If this is excessive, the decision to modify the specifications can be made at an early stage. In this manner, many processing headaches can be avoided. Finally, certain characteristics of the background profile are calculated which are then available for comparison with the accepted values of these parameters. This tests the accuracy to which the background is known.

The design-process description starts in Chapter 2 with a derivation of the more important device
characteristics from the device structure. A simplified structure is considered, and the device parameters are derived in terms of the physical structure and terminal potentials. We also present the assumptions leading to the above relations and indicate their validity. The limitations of the design process thus are shown.

Next we discuss the relative importance of the device parameters and choose two sets to be used as specifications for the pinch resistor and the JFET. Then, the relation between the diffusion parameters and the quantities determining the device parameters is indicated. We first describe the dependence of device characteristics on the net impurity profile. Next, the net profile is related to the background profile and a Gaussian diffusion profile. The assumptions leading to the Gaussian diffusion profile are presented and we describe the manner in which their validity can be ensured.

We discuss in Chapter 3 three important problems whose solution is required in order to solve the equations for the device parameters. The first problem is to determine the depletion-region boundaries for an arbitrary junction structure. Since the channel boundaries are determined by the gate depletion-region boundaries, determining the device parameters requires that these be known. Also, we show that if the depletion-region boundaries can be
determined from the specifications, the diffusion parameters can in turn be found from these.

The next problem is that of representing the channel conductivity as a function of net impurity concentration in the channel since the equations relating the device parameters to the structure are expressed in terms of conductivity. We present an approximation to the published data on conductivity versus impurity concentration and indicate its accuracy.

The final problem considered in Chapter 3 is the representation of the background, diffusion, and net impurity profiles. We present the approximations used for these and determine the accuracy of the representations. We indicate how the profile approximations simplify the solution of the equations for device parameters as well as those determining the depletion regions.

Based on the techniques described, the equations for the device specifications can be solved to yield the top-gate depletion-region boundaries. These then can be used to determine the parameters of the Gaussian diffusion, which completes the realization of a device satisfying the specifications.

An iterative process implemented on the computer is used to determine these parameters. The specifications predict a depletion region and the required diffusion parameters are found. Then, the resulting device characteristics
are derived and compared to the specifications. If the
errors are intolerable, they determine changes in the top-
gate depletion region. This results in revised diffusion
parameters and a modified structure. Again the device
characteristics are found and compared to the specifications.
This process continues until the errors are within specified
tolerances. Then, the sensitivities of the device param-
eters to diffusion parameters are calculated. The initial
depletion region is predicted by assuming that the diffusion
does not extend into the channel.

We describe the implementation of this iterative
process, using the computer, in Chapter 4. The subproblems
are considered, as are any noteworthy computational
difficulties.

In Chapter 5, examples of the design process are
presented. Pinch resistors and JFET's with varying specifi-
cations are designed and the resulting device parameters
calculated. Significant device characteristics are noted.
Then we demonstrate the correspondence between the charac-
teristics of a designed device and the measured parameters
of a sample device.

A summary and recommendations for further work are
presented in Chapter 6.
CHAPTER 2

DERIVATION OF DEVICE PARAMETERS

This chapter develops the physical structure of the channel device. Equations relating device parameters to the structure are derived, and a set of parameters is chosen as the design specifications. The fabrication of the physical structure is considered, and an expression for the resulting net impurity profile is given. Finally, the dependence of the device parameters on the net impurity profile is indicated.

2.1 Assumptions and Resulting Device Configuration

The device considered in this study is shown in Fig. 2.1. This structure is an approximation to that of Fig. 1.1, resulting from some of the assumptions listed below. The upper and lower metallurgical junctions are at \( y_{j1} \) and \( y_{j2} \). \( V_{j1} \) and \( V_{j2} \) are the voltages across the gate-channel depletion regions at any point along the channel. The upper and lower edges of the undepleted channel are \( b \) and \( a \), respectively. \( W_1 \) and \( W_2 \) are the widths of the depletion regions. The channel has length \( L \) and depth \( Z \). \( V(x) \) is the voltage at any location along the undepleted channel measured with respect to the source. The two terminal voltages, also
Fig. 2.1 The Geometry of a Simple Rectangular Channel Device
measured with respect to the source, are $V_{GS}$ and $V_{DS}$, the gate and drain voltages. The source, drain, and gate contact potentials are $V_{CS}$, $V_{CD}$, $V_{CG1}$, $V_{CG2}$, respectively. Finally, the drain current is $I_D$ and the gate currents are $I_{G1}$ and $I_{G2}$.

The following assumptions are made to simplify the analysis.

1. The gate current is negligibly small compared to the drain current.
2. The channel length is constant.
3. There is no transverse component of the electric field in the undepleted channel.
4. The electric field in the gate-channel depletion regions has only a transverse component.
5.Current flow in the undepleted channel is governed by Ohm's law.

Since the gate junctions are reverse biased, the gate currents are limited to a very small value, typically less than $10^{-9}$ amps. The drain current is much larger than this, typically at least $10^{-5}$ amps. Thus the first assumption is well justified. The second assumption is equivalent to neglecting the effect of the ends of the channel in Fig. 2.2. These ends can be considered as extrinsic series resistances (Grove 1967, pp. 256-257). In the substrate pinch resistor the contribution of the extrinsic resistance
Fig. 2.2 Channel-Device Regions
can be neglected safely since the pinched channel has much more resistance than the ends. The conductivity of a diffused layer increases greatly as the surface is approached. Therefore, the resistance contributed by the channel ends in the double-diffused structures can be neglected.

The next assumption results from the "gradual approximation" of Shockley (1952). This states that where the channel length-to-width ratio is large (as in our case), the width of the depletion region, and hence of the channel, changes gradually with x along most of the channel. For this region the transverse electric field is negligibly small. In our structure, such a condition is assumed to extend along nearly all of the channel.

The fabrication of the gates is such that the electric field in the depletion regions is in the same direction as the change in impurity profile. Thus the fourth assumption is valid over the channel considered here.

The next assumption is valid if diffusion current and field-dependent mobility are not present. The former is certainly negligible in the undepleted channel, but the latter is probably a controlling effect for operation around and beyond pinch-off (Grosvalet, Metsch, and Tribes 1963). However, since the undepleted-channel width must be extremely narrow for this effect to occur, we assume that this effect takes place at a pinch-off condition predicted
in the absence of field-dependent mobility. We also assume that this effect accounts for the drain-current versus drain-voltage characteristics beyond pinch-off.

The effect of the above assumptions is to make two one-dimensional problems of one very complex two-dimensional problem. The voltage in the undepleted channel is a function of x only, and the electric field in the depletion regions is a function of y only. The net impurity profile—the net impurity concentration as a function of distance—varies only in the y direction both in the depletion regions and in the undepleted channel.

2.2 Derivation of Parameters

The equations for the junction voltages are

\[ V_{j1}(x) = -V_{CG1} + V_{GS} + V_{CS} - V(x) \quad (2.1a) \]

and

\[ V_{j2}(x) = -V_{CG2} + V_{GS} + V_{CS} - V(x) \quad (2.1b) \]

In thermal equilibrium \( V_{GS} = V = 0 \) volts; therefore

\[ V_{j1} = V_{Cj1} = -V_{CG1} + V_{CS} \quad (2.2c) \]

and

\[ V_{j2} = V_{Cj2} = -V_{CG2} + V_{CS} \quad (2.2b) \]

where \( V_{Cj1} \) and \( V_{Cj2} \) are the built-in voltages of the junctions.
So

\[ V_{j1}(x) = V_{Cj1} + V_{GS} - V(x) \] (2.3a)
\[ V_{j2}(x) = V_{Cj2} + V_{GS} - V(x) \] (2.3b)

It is well known from semiconductor physics that the widths of the depletion regions, and hence a and b, are functions of the junction voltages (e.g., see Wang 1966, pp. 313-317). These are shown in Eqs. (2.3) to be functions of the channel voltage, which is a function of x, and the bias voltages.

From Ohm's law, the current density in the undepleted channel is

\[ j(y) = \sigma(y) E \] (2.4)

where \( \sigma(y) \) is the conductivity, which from assumption 5 does not vary along the undepleted channel but may vary across it. \( E \) is the magnitude of the electric field in the channel.

Using \( E = -\frac{dV}{dx} \) and integrating across the undepleted channel we get

\[ I_D = Z \frac{dV}{dx} \int_b^a \sigma(y) \, dy \] (2.5)

Integrating over the length of the channel we obtain

\[ I_D = \frac{Z}{L} \int_0^{V_{DS}} \int_b^{a(V,V_{GS})} \sigma(y) \, dy \, dV \] (2.6)

Since a and b are functions of \( V_{GS} \) and \( V \), we now have the drain current as a function of \( V_{GS} \) and \( V_{DS} \).
The small-signal conductance of the channel is defined as

\[ g_{22} \equiv \frac{\partial I_D}{\partial V_{DS}} \quad (2.7) \]

Applying Leibnitz's rule to Eq. (2.6) we get

\[ g_{22} = \frac{a(V_{DS}, V_{GS})}{L} \int_0^{V_{DS}} \sigma(y) \, dy \quad \frac{b(V_{DS}, V_{GS})}{(2.8)} \]

where \( a(V_{DS}, V_{GS}) \) and \( b(V_{DS}, V_{GS}) \) are the channel limits at the drain for a specified \( (V_{DS}, V_{GS}) \). This relation is not valid for operation beyond pinch-off; in this region \( g_{22} = 0 \) for the simplified structure considered here.

An alternate expression for the drain current can be derived from Eq. (2.7).

\[ I_D = \int_0^{V_{DS}} g_{22}(V_d) \, dV_d \quad (2.9) \]

The first derivative of \( g_{22} \) with respect to \( V_{DS} \) is

\[ g_{22} = \frac{\partial g_{22}}{\partial V_{DS}} = \frac{Z}{L} \left[ \sigma(a(V_{DS}, V_{GS})) \frac{\partial a}{\partial V_{DS}} \right. \]

\[ \left. - \sigma(b(V_{DS}, V_{GS})) \frac{\partial b}{\partial V_{DS}} \right] \quad (2.10) \]

The transconductance of the device is defined as:

\[ g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (2.11) \]
Taking the partial derivative of Eq. (2.6) with respect to $V_{GS}$ we get

$$g_m = \frac{Z}{L} \left\{ \frac{V_{DS}}{0} \int \left[ \sigma(a(V, V_{GS})) \frac{\partial a}{\partial V_{GS}} ight. \\
- \left. \sigma(b(V, V_{GS})) \frac{\partial b}{\partial V_{GS}} \right] dV \right\} \quad (2.12)$$

Since $a(V, V_{GS})$ and $b(V, V_{GS})$ are in reality $a(V, j_2)$ and $b(V, j_1)$ and from Eqs. (2.3)

$$\frac{\partial V_{j1}}{\partial V_{GS}} = - \frac{\partial V_{j1}}{\partial V} \quad (2.13a)$$

and

$$\frac{\partial V_{j2}}{\partial V_{GS}} = - \frac{\partial V_{j2}}{\partial V} \quad (2.13b)$$

Eq. (2.12) becomes

$$g_m = \frac{Z}{L} \left[ \int a(0, V_{GS}) \sigma(a) da + \int b(V_{DS}, V_{GS}) \sigma(b) db \right] \quad (2.14)$$

The geometrical interpretation of Eqs. (2.8) and (2.14) is shown in Fig. 2.3. The values of $g_{22}$ and $g_m$ are the conductances of the shaded portions of the channel. It is seen that $g_{22}$ decreases as $V_{DS}$ increases for constant $V_{GS}$; also that $g_m$ is a maximum for $V_{GS} = 0$ volts. It is worth noting that for a given structure and $V_{GS}$, the sum of $g_{22}$ and $g_m$ is a constant. This constant is seen from Fig.
Fig. 2.3 Physical Interpretation of $g_m$ and $g_{22}$
2.3 to be the conductance of the portion of the channel bounded by the gate depletion regions at the source.

Pinch-off occurs when the width of the undepleted channel at the drain goes to zero. For any given $V_{GS}$, this happens when $V_{DS}$ attains the value such that $a(V_{DS}, V_{GS})$ equals $b(V_{DS}, V_{GS})$. The channel depth at which pinch-off occurs is $y_p$. For $V_{GS}$ equal to zero volts, this value of $V_{DS}$ is known as the pinch-off voltage, $V_p$.

We now have relations for $g_{22}$, $g_{22}'$, $g_m$, $I_D$, and $V_p$ for operation up to pinch-off, in terms of quantities which vary in one dimension, $y$. Let us normalize these quantities with respect to $Z/L$. If we examine the normalized relation for $g_{22}$, we see that the result is the reciprocal of the sheet resistance for the layer of material between $y = a(V_{DS}, V_{GS})$ and $y = b(V_{DS}, V_{GS})$. Thus we have expressions for the small-signal sheet conductance of the channel, $\sigma_S$, and its first derivative with respect to voltage, $\sigma'_S$, as well as $I_D$ and $g_m$ per unit $Z/L$.

2.3 Choice of Specifications

The pinch resistor is best specified by its small-signal sheet conductance and the minimum linearity of this conductance. This is so because when it is used to form a high-value load resistance the magnitude of the small-signal output voltage is directly proportional to the small-signal conductance. The linearity of the conductance is a direct
measure of the accuracy of the output signal. The terminal voltages are determined in most cases by circuit or system considerations and so are given. As a rule the device $g_m$ and other parameters such as the junction capacitances are of secondary importance for a pinch resistor.

The drain current is a relatively important parameter but is not chosen as a specification here for two reasons. First, for a pinch resistor operated well below pinch-off the large-signal and small-signal conductances are approximately equal, i.e.,

$$g_{22} \approx G_D = \frac{I_D}{V_{DS}}$$  \hspace{1cm} (2.15)

so $I_D$ is specified implicitly if $V_{DS}$ is known and $g_{22}$ is specified. If operated near pinch-off, the pinch resistor is highly nonlinear and so would find little use as a load but might be used as a bias element. If used for biasing, the device is most often operated near enough to the pinch-off condition that it can be treated as a JFET. Also, when the device is used as a nonlinear load in a switching circuit, one operating point is well below pinch-off and the other beyond pinch-off. Therefore, the omission of $I_D$ from the set of specifications for the pinch-resistor design is not considered to be significant.

The second reason for not using $I_D$ as a specification is that it is not readily accessible. If Eq. (2.9) were used, the $g_{22}$ would have to be known as a function of
If Eq. (2.5) were used, \( \frac{dV}{dx} \) would have to be known; thus the problem would become two-dimensional.

Rewriting Eqs. (2.8) and (2.10) in normalized form, we obtain the equations giving the pinch-resistor parameters used as device specifications:

\[
\sigma_s = \int \sigma(y)dy \quad \text{a}(V_{DS}, V_{GS})
\]

\[
\sigma_s' = \sigma(a(V_{DS}, V_{GS})) \frac{\partial a}{\partial V_{DS}} - \sigma(b(V_{DS}, V_{GS})) \frac{\partial b}{\partial V_{DS}} \quad \text{b}(V_{DS}, V_{GS})
\]

Consider the junction shown in Fig. 2.4. The net profile of impurities is \( N(y) \), the depletion-region edges are \( y_L \) and \( y_R \), and equal total charge exists on both sides of \( y_j \). The capacitance of this structure is

\[
C_j = \frac{dQ_R}{dV_j} = qA N(y_R) \frac{dy_R}{dV_j}
\]

where \( A \) is the cross-sectional area of the junction, \( Q_R \) is the total charge on the right-hand side of \( y_j \) and \( q \) is the magnitude of the electronic charge. The parallel-plate formula is valid for this structure, so

\[
C_j = \frac{\epsilon A}{W}
\]

where \( \epsilon \) is the permittivity of silicon.

Combining Eqs. (2.18) and (2.19) we obtain

\[
\frac{dy_R}{dV_j} = \frac{\epsilon}{qWN(y_R)}
\]
Fig. 2.4 General p-n Junction
It is seen from this that the change in position of a depletion-region edge with voltage is inversely proportional to the width of the region and the net impurity concentration at the edge. If the characteristics of the lower junction, $\sigma(N(y))$, and $N(y)$ in the channel are known, Eqs. (2.16), (2.17), and (2.20) define the lower edge of the upper-junction depletion region and its width for a given $(V_{DS}, V_{GS})$. As is shown in Chapter 3, this information determines the constants of the solid-state diffusion forming the upper junction.

In the case of the JFET, the most important parameter is the pinch-off voltage, $V_p$, since this determines the mode of operation. As in the case of the pinch resistor, the terminal voltages are generally fixed by circuit, rather than device, considerations.

Next in importance are the transconductance and drain current. Of these two, we use the transconductance as a specification because of the difficulty, as described above, in using the drain current. Again gate capacitance is of secondary importance. The channel conductance, $g_{22}$, is assumed to be zero beyond pinch-off in our simple device.

When the device is used as a signal-amplifying element, the transconductance is more important than the drain current since it determines the gain of the device. When a JFET is used as a biasing element providing a bias current, the value of $I_D$ in general need not be known
exactly since requirements in biasing usually are not extremely rigid. An estimate of the drain current for \( V_{GS} = 0 \) volts, \( I_{DSS} \), can be made as follows.

\[
I_{DSS} \approx \frac{V_p}{2} g_m \bigg|_{V_{GS} = 0 \text{ volts}} \tag{2.21}
\]

Also, some source resistance usually is added when using a JFET as a current source. This is the source-follower configuration and for it the \( g_m \) of the device is as important as \( I_D \).

If the JFET is employed as a nonlinear load in a switching circuit, the operating point below pinch-off can be used to specify \( g_m \). The actual parameter of interest is \( g_{22} \) for \( V_{DS} \) equal to a small voltage. Since the sum of \( g_{22} \) and \( g_m \) is a constant for a given \( V_{GS} \), \( g_m \) at pinch-off is approximately equal to such a value of \( g_{22} \). The operating point beyond pinch-off is determined by the drain current, and this can be used to specify \( V_p \) in the manner described above for biasing circuits. For these reasons, omitting \( I_D \) from the specifications is not considered significant.

Let us write Eq. (2.14) in normalized form to obtain \( g_m \) per unit \( Z/L \).

\[
\bar{g}_m = \int_{a(V_{DS}, V_{GS})}^{b(V_{DS}, V_{GS})} \sigma(a) da + \int_{a(0, V_{GS})}^{b(0, V_{GS})} \sigma(b) db \tag{2.22}
\]

where \( V_{DS} \) equals that voltage such that
\[ a(V_{DS}, V_{GS}) = b(V_{DS}, V_{GS}) = y_f \]  \hfill (2.23)

Again, if the characteristics of the lower junction, \( \sigma(N(y)) \), and \( N(y) \) in the channel are known, Eq. (2.23) indicates the lower edge of the upper depletion region at the drain at pinch-off. The lower edge of the upper depletion region operated at \((0, V_{GS}')\) is determined by Eq. (2.22). In Chapter 3 this information is shown to determine the constants in the solid-state diffusion forming the upper junction.

### 2.4 Diffusion Process and Results

The above relations for the device parameters are in terms of integrals of conductivity whose limits are the edges of depletion regions of junctions. It is well known that in silicon the conductivity is a function of the net impurity concentration, \( N(y) \) (Irvin 1962). The positions of the junctions, and the extent of the depletion regions and therefore the edges of the depletion regions, also are determined by the net impurity profile.

As described in Warner (1965, pp. 127-150), the net impurity profile of the device is determined by a diffusion of impurities, \( C(y) \) into a background profile \( B(y) \), which may include the results of other diffusions.

\[ N(y) = B(y) - C(y) \]  \hfill (2.24)
The diffusion process assumed here is the two-step process used almost universally throughout the semiconductor industry for the fabrication of silicon monolithic integrated circuits (Grove 1967, pp 43-58; Warner 1965, pp. 69-75). The results of this process are approximated here by those predicted from a simple model of the process as described below. The first step is called the predeposition. During it the surface of the wafer is exposed to a constant source concentration of a given impurity specie for a specified time at some controlled temperature. This results in the formation of a layer at the surface containing the impurities. The second step is called the drive-in or distribution. During it the wafer is placed in a controlled-temperature environment and the impurities in the deposited layer redistribute themselves.

During both of these steps, the movement of the impurity distribution in the wafer as a function of time, \( t \), is assumed to follow Fick's second law,

\[
\frac{\partial C(y,t)}{\partial t} = D_I(T) \frac{\partial^2 C(y,t)}{\partial y^2}
\]

where \( D_I(T) \) is the diffusivity of the impurity specie in silicon. It is further assumed that \( D_I(T) \) is a function of temperature, \( T \), only and not of \( y \). This implies that \( D_I(T) \) is independent of the background concentration.
The results of the first step are assumed to be a very thin layer at the surface with impurity concentration \( Q \) per unit area. This represents all the impurity atoms deposited and is a good assumption if the predeposition layer is confined to the immediate vicinity of the surface.

During the second step, the deposited impurity atoms are considered sealed in the wafer, i.e.,

\[
\frac{\partial C}{\partial y} \bigg|_{y=0} = 0
\]  

(2.26)

Also the surface is assumed to remain at \( y = 0 \) and the wafer is considered infinitely thick, as far as the deposited impurities are concerned, i.e.,

\[
C(\infty, t) = 0
\]  

(2.27)

The initial condition is

\[
C(y,0) = \begin{cases} 
Q & : y = 0 \\
0 & : y \neq 0
\end{cases}
\]  

(2.28)

The solution to Eq. (2.25) subject to these conditions is presented by Carslaw and Jaeger (1959, p. 50).

\[
C(y,t) = \frac{Qe^{-y^2/4D_I t}}{\sqrt{\pi D_I t}}
\]  

(2.29)

This is the well-known Gaussian distribution and can be rewritten in terms of the surface concentration after drive-in, \( C_0 \), and the characteristic length, \( y_0 \).
It can be shown that if the drive-in step is composed of several steps at different temperatures, each subject to the above restrictions with the exception that the initial condition of each successive step is the result of the preceding step, the final result has the form of Eq. (2.29). The diffusivity in this case is the time-weighted average of the different diffusivities of the many steps, and the time is the total time.

While the above restrictions appear severe, they correspond well with the conditions for device fabrication. The effects of out-diffusion of the impurity from the silicon surface and the surface moving from $y = 0$ (Atalla and Tannenbaum 1960; Grove, Leistiko, and Sah 1964) are more pronounced in the case of the substrate device. For this device these effects can be minimized by delaying the oxidation process until after the drive-in is well underway. The biggest violation of the above assumptions in the case of the double-diffused device is the emitter push effect (Nicholas 1966). It is here assumed that the push exerted by the diffusion forming the top gate on the lower-gate junction is the same as that of a conventional emitter diffusion and so the result is known.
Combining Eqs. (2.24) and (2.30) we have an equation for the net impurity profile in terms of the background profile and two constants of the top-gate diffusion.

\[ \frac{N(y)}{y_0} = B(y) - C_0 e^{-\left(\frac{y}{y_0}\right)^2} \]  

(2.31)

It should be noted that in specifying that the background profile be known, we are specifying that it be known as it appears after all the normal processing steps through emitter drive-in have been performed. The two steps of the extra diffusion used to form either the substrate or double-diffused channel device are to be fitted into the processing schedule during the drive-in times for the normal process, and the effect of these two steps is used to adjust the drive-in times in the normal schedule. Thus the background profile after all steps is the same with or without the extra diffusion.

We now have the equations giving the device performance in terms of terminal voltages and functions of the net profile. The net profile has been related to the background profile and to the two controlling constants of the top-gate diffusion. The next chapter further develops these equations and indicates the dependence of the specified device parameters on the top-gate diffusion constants.
CHAPTER 3

RELATIONS AND APPROXIMATIONS

In this chapter we develop the expressions for junction voltage, depletion-region width, and net impurity profile. Also, the dependence of conductivity on impurity concentration used in the design process is presented. We derive the equations for $C_0$ and $y_0$ in terms of the specifications and background profile. Finally, the approximation used for the net profile is given.

3.1 The Junction Depletion Regions

The general p-n junction is shown in Fig. 2.4. The semiconductor conductivity type changes from p to n in the junction region and the point at which the net impurity concentration is zero is called the metallurgical junction. The depletion region extending on both sides of this point is depleted of mobile carriers, leaving the immobile impurity ions. These latter give rise to a large electric field. Outside of this region is the so-called quasi-neutral region in which no depletion of mobile carriers takes place and the field is assumed to be relatively small. This is the so-called depletion approximation. Applying the divergence theorem to the depletion region, we get.
\[
\frac{d\varepsilon}{dy} = \frac{q}{\varepsilon} N(y) \quad (3.1)
\]

If Eq. (3.1) is integrated across the depletion region, we obtain

\[
\frac{q}{\varepsilon} \int_{y_L}^{y_R} N(y) dy = 0 \quad (3.2)
\]
since the electric field is zero at the depletion-region boundaries, \(y_R\) and \(y_L\). Equation (3.2) implies that a charge balance exists on both sides of the metallurgical junction.

Since \(\varepsilon(y) = \frac{-dV}{dy}\), the difference in potential across the junction is

\[
V_j = -\int_{y_L}^{y_R} \varepsilon(y) dy \quad (3.3)
\]

If we integrate Eq. (3.3) by parts and make use of Eq. (3.1) and the depletion approximation, we obtain

\[
V_j = \frac{q}{\varepsilon} \int_{y_L}^{y_R} yN(y) dy \quad (3.4)
\]

This equation, known as the moment equation, is valid as long as the electric field at \(y_R\) and \(y_L\) is zero, a consequence of the depletion approximation.

It can be shown (Jonscher 1960, p. 13) that the electric field in a region of semiconductor material is
proportional to the gradient of the so-called intrinsic energy level, $E_i$

$$\mathcal{E} = \frac{1}{q} \frac{dE_i}{dy} \quad (3.5)$$

Substituting Eq. (3.5) into Eq. (3.3) and solving, we get

$$V_j = \frac{1}{q} [E_i(y_L) - E_i(y_R)] \quad (3.6)$$

The intrinsic energy level at any location, $y$, can be written in terms of the electron or hole concentration at that location and the quasi-Fermi levels for electrons and holes there (Jonscher 1960, p. 48).

$$E_i(y) = E_{fn}(y) - kT \ln \left[ \frac{n(y)}{n_i} \right] \quad (3.7a)$$

$$E_i(y) = E_{fp}(y) + kT \ln \left[ \frac{p(y)}{n_i} \right] \quad (3.7b)$$

where $n$ and $p$ are the electron and hole concentrations at $y$, $k$ is Boltzmann's constant and $n_i$ is the intrinsic carrier concentration of silicon, and $E_{fn}$ and $E_{fp}$ are the electron and hole quasi-Fermi levels at $y$. Using the hole concentration on the left edge and the electron concentration on the right edge of the depletion region and substituting Eqs. (3.7) in Eq. (3.6), we get

$$V_j = \frac{1}{q} \left[ E_{fp}(y_L) - E_{fn}(y_R) + kT \ln \left[ \frac{p(y_L)n(y_R)}{n_i^2} \right] \right] \quad (3.8)$$
For the p-n junction in reverse bias and low-level forward bias,
\[ p(y_L) = -N(y_L) \quad (3.9a) \]
\[ n(y_R) = N(y_R) \quad (3.9b) \]
because of the condition of quasi-neutrality.

Substituting Eqs. (3.9) in Eq. (3.8) we obtain
\[ V_j = \frac{1}{q} \left\{ E_{fp}(y_L) - E_{fn}(y_R) + kT \ln \left[ \frac{-N(y_L)N(y_R)}{n_i^2} \right] \right\} \quad (3.10) \]

For thermal equilibrium \( E_{fp}(y) = E_{fn}(y) \) and \( V_j \) can be expressed in terms of the net concentration at \( y_L \) and \( y_R \):
\[ V_j = \frac{kT}{q} \ln \left[ \frac{-N(y_L)N(y_R)}{n_i^2} \right] \quad (3.11) \]

where \( V_{Cj} \) is the contact potential of the junction. For any condition of nonequilibrium, the right-hand side of Eq. (3.11) is larger or smaller than the right-hand side of Eq. (3.10), because \( E_{fp}(y_L) \neq E_{fn}(y_R) \).

A similar development can be made for an n-p junction and the result is the negative of the right-hand side of Eq. (3.11):
\[ V_j = V_{Cj} = \frac{-kT}{q} \ln \left[ \frac{-N(y_L)N(y_R)}{n_i^2} \right] \quad (3.12) \]
The absolute value of the contact potential of a junction is then

$$|V_{cj}| = \frac{kT}{q} \ln \left[ \frac{|N(y_L)|}{n_i^2} \right]$$

(3.13)

where $y_L$ and $y_R$ are the edges of the equilibrium depletion region.

It can be seen that if $N(y)$ is known, we can specify $V_j$ and obtain $y_L$ and $y_R$ by solving Eqs. (3.2) and (3.4). The procedure is as follows: we start at the junction, move an increment $dy$ in one direction and solve Eq. (3.2) for the corresponding increment that gives charge balance in the other direction, then solve Eq. (3.4) to obtain the voltage. This process is continued until the specified voltage is reached.

Similarly, if $N(y)$ and the location of either edge is known, the position of the other edge can be found from Eq. (3.2) and then the junction voltage from Eq. (3.4).

The contact potential also can be found by a process similar to that described above for finding the depletion-region edges. The difference here is that at every step Eq. (3.13) must be evaluated and its result compared to that of Eq. (3.4).

If $N(y)$ is not known but its functional form is known, as well as $V_j$ and the depletion-region edges, it may be possible to use Eqs. (3.2) and (3.4) to obtain $N(y)$. 
For the case where $N(y)$ is represented by Eq. (2.31), Eq. (3.2) becomes

\[
\int_{y_L}^{y_R} B(y) dy = C_0 \int_{y_L}^{y_R} e^{-(\frac{y}{Y_0})^2} dy 
\]

By a change of variable this is rewritten as

\[
\int_{y_L}^{y_R} B(y) dy = C_0 Y_0 \int_{y_L}^{y_R} e^{-y^2} dy 
\]

Similarly, Eq. (3.4) becomes

\[
\frac{\varepsilon}{q} v_j - \int_{y_L}^{y_R} y B(y) dy = -C_0 \int_{y_L}^{y_R} y e^{-y^2} dy 
\]

This reduces to

\[
\frac{\varepsilon}{q} v_j + \int_{y_L}^{y_R} y B(y) dy = C_0 Y_0^2 \left[ \frac{-\frac{Y_L}{Y_0}^2}{e} e^{-\frac{Y_R}{Y_0}^2} \right] 
\]

Equations (3.15) and (3.17) can be rewritten in terms of the well-known Gaussian distribution, $g(y)$, and its integral the error function, $\text{erf}(y)$. These are:
If $V_j$, $y_R$, and $y_L$ are known, Eqs. (3.18) and (3.19) can in theory be solved for $C_0$ and $y_0$. The method used here is to evaluate the left-hand sides and then divide Eq. (3.19) by Eq. (3.18) to eliminate $C_0$. The result is

$$2 \gamma = y_0 \frac{\left[ g\left(\frac{y_L}{y_0}\right) - g\left(\frac{y_R}{y_0}\right) \right]}{\left[ \text{erf}\left(\frac{y_R}{y_0}\right) - \text{erf}\left(\frac{y_L}{y_0}\right) \right]} \tag{3.20}$$

where $\gamma$ is the quotient of the left-hand sides. Note that both sides of Eq. (3.20) are greater than zero if $y_0$, $y_L$, and $y_R$ are greater than zero. This equation can be solved as described below and the resulting value of $y_0$ substituted in Eq. (3.18) which is then solved for $C_0$.

The solution of Eq. (3.20) is accomplished by an iterative method. We estimate the value of $y_0$ which satisfies the equation, evaluate Eq. (3.20), and adjust the estimation based on the results of the evaluation. Consider the right-hand side of Eq. (3.20):
\[ f(y_0) = y_0 \frac{\left[ g\left(\frac{y_L}{y_0}\right) - g\left(\frac{y_R}{y_0}\right) \right]}{\left[ \text{erf}\left(\frac{y_R}{y_0}\right) - \text{erf}\left(\frac{y_L}{y_0}\right) \right]} \quad (3.21) \]

The iterative method described above is successful if an interval of \( y_0 \) exists such that \( f(y_0) \) is greater than \( 2\gamma \) at one end and less than \( 2\gamma \) at the other. Also \( f(y_0) \) must be continuous over the interval. It is continuous since it is the sum, product, and quotient of continuous functions of \( y_0 \). The denominator is never zero since \( y_R \) is never equal to \( y_L \).

As \( y_0 \) approaches infinity, Eq. (3.21) is indeterminate. Using L'Hospital's rule and retaining the first two terms of the Taylor expansion about zero for the exponential functions, we obtain

\[ f(y_0) = y_L + y_R \quad (3.22) \]

as \( y_0 \to \infty \).

Equation (3.21) is also indeterminate as \( y_0 \) approaches zero. Again L'Hospital's rule is used and we obtain

\[ f(y_0) = 2y_L \quad (3.23) \]

as \( y_0 \to 0 \). Therefore, if it is possible to ensure that

\[ 2y_L < 2\gamma < y_L + y_R \quad (3.24) \]
Eq. (3.20) can be solved by iteration for a value of $y_0$ between zero and infinity.

In principle, one could test for monotonicity of Eq. (3.21) by examining the sign of its derivative. However, the expression for the derivative is too unwieldy to be of practical use. One must therefore acknowledge the possibility that the value of $y_0$ obtained from the iterative solution of Eq. (3.20) may not be unique. Nevertheless, if $V_j$, $y_L$, and $y_R$, and the background profile are known, values for $C_0$ and $y_0$ can be found which satisfy Eqs. (3.18) and (3.19). The specifications for device parameters and terminal voltages can be used in Eqs. (2.16), (2.17), and (2.22) to determine $V_j$, $y_L$, and $y_R$; then the top-gate diffusion parameters $C_0$ and $y_0$ are determined as described above.

3.2 Conductivity as a Function of Concentration

Since the carrier mobilities are functions of the impurity concentration, the bulk electrical conductivity of silicon is also a function of the impurity concentration. Therefore, to evaluate Eqs. (2.16), (2.17), and (2.22), not only $N(y)$ but also $\sigma(N)$ must be known. The data used to calculate the dependence of conductivity on impurity concentration have been published (Irvin 1962). This information appears as a curve of the resistivity, $\rho$, of homogeneously doped samples of silicon at $300^\circ$ K. As
described (Irvin 1962), it is a hand fit of the data points available and is considered to be accurate within 10 per cent, being least accurate for samples whose impurity concentrations exceed $10^{20}$ atoms per cm$^3$.

The curve is approximated here by straight line segments. To preserve the 10 per cent fit, the line segments are drawn such that they do not deviate from the published curve. To facilitate this process, a hairline on a transparent sheet was used here over the expanded representation of Irvin's curve as published in Research Triangle Institute (1963, pp. 2-4 to 2-7). The result of this procedure is a series of impurity concentration breakpoints separating intervals within which the resistivity curve on log$_{10}$-log$_{10}$ paper is represented by straight lines. Since conductivity is the reciprocal of resistivity, the conductivity approximation within an interval is

$$
\sigma(N) = K_i N^{P_i}
$$

(3.25)

The two constants $K_i$ and $P_i$ are determined for each interval. They are given by

$$
P_i = \frac{-\log_{10}(\frac{\rho_f}{\rho_i})}{\log_{10}(\frac{N_f}{N_i})}
$$

(3.26)
and

\[ K_i = \frac{N_i - P_i}{\rho_i} \]  \hspace{1cm} (3.27)

where \((N_i, \rho_i)\) is the initial point of each straight line approximation and \((N_f, \rho_f)\) is the final point.

The values of the constants were calculated for p- and n-type silicon and are listed together with the final points of the intervals in Tables 3.1 and 3.2.

This approximation is considered to be valid even in the case of compensated material treated here since the impurity scattering is assumed to be caused by ionized impurities at room temperature. Also, since the impurity levels in the channel are much less than \(10^{20}\) atoms per cm\(^3\), the approximation is considered accurate to 10 per cent.

3.3 Representation of Net Profile

Representations of background, diffusion, and net profiles are required to solve the equations discussed above. The approximations for the background and diffusion profiles used here are straight line segments constructed such that at their end points the straight lines coincide with the profiles and the maximum relative error in concentration at any location between end points is specified.

The net profile approximation is also composed of straight line segments. The end points of the segments are obtained using the background and diffusion approximations,
### Table 3.1. P-Type Material Conductivity Approximation Constants

<table>
<thead>
<tr>
<th>( N_f ) (cm(^{-3}))</th>
<th>( K_i ) ( \left( \frac{3p_i}{cm \cdot \text{ohm-micron}} \right) )</th>
<th>( P_i )</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0 ( \times ) 10(^{14})</td>
<td>6.906327 ( \times ) 10(^{-22})</td>
<td>1.071385</td>
</tr>
<tr>
<td>9.0 ( \times ) 10(^{14})</td>
<td>4.478593 ( \times ) 10(^{-21})</td>
<td>1.014613</td>
</tr>
<tr>
<td>2.5 ( \times ) 10(^{15})</td>
<td>2.523430 ( \times ) 10(^{-20})</td>
<td>0.964403</td>
</tr>
<tr>
<td>8.0 ( \times ) 10(^{15})</td>
<td>2.790093 ( \times ) 10(^{-20})</td>
<td>0.961570</td>
</tr>
<tr>
<td>1.5 ( \times ) 10(^{16})</td>
<td>7.248976 ( \times ) 10(^{-18})</td>
<td>0.809734</td>
</tr>
<tr>
<td>6.0 ( \times ) 10(^{16})</td>
<td>7.231607 ( \times ) 10(^{-17})</td>
<td>0.747979</td>
</tr>
<tr>
<td>1.0 ( \times ) 10(^{17})</td>
<td>8.582924 ( \times ) 10(^{-16})</td>
<td>0.683943</td>
</tr>
<tr>
<td>7.0 ( \times ) 10(^{17})</td>
<td>9.757205 ( \times ) 10(^{-15})</td>
<td>0.621844</td>
</tr>
<tr>
<td>1.0 ( \times ) 10(^{18})</td>
<td>1.253273 ( \times ) 10(^{-17})</td>
<td>0.783865</td>
</tr>
<tr>
<td>2.5 ( \times ) 10(^{18})</td>
<td>1.949206 ( \times ) 10(^{-17})</td>
<td>0.662097</td>
</tr>
<tr>
<td>6.0 ( \times ) 10(^{18})</td>
<td>2.490140 ( \times ) 10(^{-17})</td>
<td>0.765024</td>
</tr>
<tr>
<td>1.0 ( \times ) 10(^{19})</td>
<td>1.307479 ( \times ) 10(^{-19})</td>
<td>0.886430</td>
</tr>
<tr>
<td>8.0 ( \times ) 10(^{19})</td>
<td>1.691983 ( \times ) 10(^{-20})</td>
<td>0.933169</td>
</tr>
<tr>
<td>2.0 ( \times ) 10(^{20})</td>
<td>6.751580 ( \times ) 10(^{-22})</td>
<td>1.003459</td>
</tr>
<tr>
<td>3.0 ( \times ) 10(^{20})</td>
<td>4.932887 ( \times ) 10(^{-23})</td>
<td>1.059432</td>
</tr>
<tr>
<td>4.0 ( \times ) 10(^{20})</td>
<td>3.647768 ( \times ) 10(^{-22})</td>
<td>1.016998</td>
</tr>
<tr>
<td>5.0 ( \times ) 10(^{20})</td>
<td>2.047861 ( \times ) 10(^{-24})</td>
<td>1.126246</td>
</tr>
<tr>
<td>7.0 ( \times ) 10(^{20})</td>
<td>5.101492 ( \times ) 10(^{-20})</td>
<td>0.913849</td>
</tr>
<tr>
<td>1.0 ( \times ) 10(^{21})</td>
<td>2.425144 ( \times ) 10(^{-20})</td>
<td>0.833396</td>
</tr>
</tbody>
</table>
Table 3.2. N-Type Material Conductivity Approximation Constants

<table>
<thead>
<tr>
<th>$N_f$ (cm$^{-3}$)</th>
<th>$\frac{3P_i}{cm}$ (ohm-micron)</th>
<th>$P_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$4.0 \times 10^{14}$</td>
<td>$2.989896 \times 10^{-21}$</td>
<td>1.057739</td>
</tr>
<tr>
<td>$2.5 \times 10^{15}$</td>
<td>$1.078427 \times 10^{-19}$</td>
<td>0.951101</td>
</tr>
<tr>
<td>$1.0 \times 10^{16}$</td>
<td>$3.769886 \times 10^{-19}$</td>
<td>0.915801</td>
</tr>
<tr>
<td>$3.6 \times 10^{16}$</td>
<td>$1.058947 \times 10^{-17}$</td>
<td>0.825267</td>
</tr>
<tr>
<td>$8.0 \times 10^{16}$</td>
<td>$1.611961 \times 10^{-17}$</td>
<td>0.814245</td>
</tr>
<tr>
<td>$1.5 \times 10^{17}$</td>
<td>$3.634284 \times 10^{-15}$</td>
<td>0.675036</td>
</tr>
<tr>
<td>$1.0 \times 10^{18}$</td>
<td>$6.807111 \times 10^{-13}$</td>
<td>0.542728</td>
</tr>
<tr>
<td>$2.5 \times 10^{18}$</td>
<td>$3.691364 \times 10^{-13}$</td>
<td>0.557493</td>
</tr>
<tr>
<td>$5.0 \times 10^{18}$</td>
<td>$1.152932 \times 10^{-13}$</td>
<td>0.584962</td>
</tr>
<tr>
<td>$8.0 \times 10^{18}$</td>
<td>$4.500968 \times 10^{-16}$</td>
<td>0.713766</td>
</tr>
<tr>
<td>$1.5 \times 10^{19}$</td>
<td>$3.514267 \times 10^{-17}$</td>
<td>0.772353</td>
</tr>
<tr>
<td>$3.0 \times 10^{19}$</td>
<td>$5.211929 \times 10^{-18}$</td>
<td>0.815575</td>
</tr>
<tr>
<td>$7.0 \times 10^{19}$</td>
<td>$2.230664 \times 10^{-20}$</td>
<td>0.937183</td>
</tr>
<tr>
<td>$1.0 \times 10^{20}$</td>
<td>$5.690800 \times 10^{-17}$</td>
<td>0.765516</td>
</tr>
<tr>
<td>$1.5 \times 10^{20}$</td>
<td>$1.803740 \times 10^{-15}$</td>
<td>0.690466</td>
</tr>
<tr>
<td>$2.5 \times 10^{20}$</td>
<td>$1.629792 \times 10^{-13}$</td>
<td>0.593522</td>
</tr>
<tr>
<td>$5.0 \times 10^{20}$</td>
<td>$1.056418 \times 10^{-10}$</td>
<td>0.455680</td>
</tr>
<tr>
<td>$7.0 \times 10^{20}$</td>
<td>$9.774652 \times 10^{-9}$</td>
<td>0.360686</td>
</tr>
<tr>
<td>$1.0 \times 10^{21}$</td>
<td>$3.911180 \times 10^{-3}$</td>
<td>0.091932</td>
</tr>
</tbody>
</table>
starting from the wafer surface. The y value of the net profile segment end point is that of the current background or diffusion profile approximation segment, whichever is closer. The background or diffusion concentration at this end point is combined with the concentration approximation of the other at this location as obtained by linear interpolation on the profile approximation. We thus obtain the net concentration of the end point of the net profile approximation. This point becomes the near end point of the next segment of the net profile approximation and the whole process is repeated to find the far end point. Thus at each end point of each net profile approximation segment the error is within the maximum relative error specified for the larger of the background or diffusion concentrations. At any location between end points on the net profile approximation, the maximum possible error in concentration is the sum of the two maximum errors specified for the background and diffusion concentrations.

This concentration error appears largest relative to the net profile in the vicinity of the metallurgical junction where the net concentration approaches zero. However, since practical fabrication considerations dictate net profiles with very steep slopes at the junctions, the error in the junction location due to the error in the net profile approximation is minimized. Also, since the net concentration approximation is integrated over a considerable
distance around the junction in Eqs. (3.2), (3.4), (3.14), and (3.16) the large relative error in \( N(y) \) at the junction is averaged with smaller errors over the depletion region and its overall effect reduced.

The above technique for constructing the net profile approximation requires that the background and diffusion profiles be known well enough to be approximated within some specified error in concentration. We must know the background profile accurately enough that the end points of the approximation intervals can be chosen such that the straight line segments between them are no more than the specified amount in error. The composite background profile considered here consists of uniformly doped substrate and epitaxial layers, for substrate devices, with the addition of one diffusion in the epi-layer for double-diffused devices. Obviously no approximation difficulty is presented by the uniformly doped regions and the diffusion in the background can be handled as described below for the top gate diffusion. A problem is posed by the substrate-epitaxial layer junction. The profile in this region has been studied (Grove, Roder, and Sah 1965; Joyce, Weaver, and Maule 1965) and the results for the cases of interest here are known.

Since we assume that the diffusion profile conforms to Eq. (2.30), the problem of approximating this profile reduces to one of approximating the Gaussian distribution.
Let us rewrite and consider Eq. (2.30):

\[
C(y) = C_0 e^{-\left(\frac{y}{y_0}\right)^2} \tag{3.28}
\]

\[
C'(y) = -\frac{2y}{y_0} C(y) \tag{3.29}
\]

\[
C''(y) = -\frac{2}{y_0^2} C(y) \left[1 - 2 \frac{y^2}{y_0^2}\right] \tag{3.30}
\]

In this study, \(y\) is restricted to being greater than or equal to zero. As can be seen in Fig. 3.1, \(C(y)\) starts at \(C_0\) and goes monotonically to zero as \(y\) increases. The slope, \(C'(y)\), starts at zero, attains a maximum negative value at \(y = y_0/\sqrt{2}\), then monotonically goes to zero as \(y\) approaches infinity. The curvature, \(C''(y)\), starts at a negative value, \(-\frac{2C_0}{y_0^2}\), monotonically going to its maximum positive value at \(y = \sqrt{3/2} y_0\), then approaching zero as \(y\) increases.

The technique described above for approximating the diffusion profile results in line segments which lie below \(C(y)\) between end points for \(y < y_0/\sqrt{2}\), and which lie above \(C(y)\) between end points for \(y > y_0/\sqrt{2}\) as shown in Fig. 3.2. A portion of \(C(y)\) for \(y < y_0/\sqrt{2}\) is shown in Fig. 3.3. A line segment, \(\overline{C}(y)\), is also shown which approximates \(C(y)\); the approximation covers the interval from \(y_1\) to \(y_2\). The relative error in the approximation is
Fig. 3.1 The Gaussian Profile and Its First Two Derivatives
Fig. 3.2 The Gaussian Profile and Its Approximation
Fig. 3.3 Detail of Approximation
\[ \varepsilon(y) = \frac{C(y) - \hat{C}(y)}{C(y)} \]  \hspace{1cm} (3.31)

This error reaches a maximum at some location, \( y_m \), in the interval and is zero at the end points. Let us construct another curve, \( \hat{C}(y) \), such that

\[ \hat{C}(y) = (1 - \varepsilon_m)C(y) \]  \hspace{1cm} (3.32)

where \( \varepsilon_m \) is the specified maximum relative error in the straight line approximation. This curve marks the boundary for approximation to \( C(y) \) within error \( \varepsilon_m \).

It can be seen from Eqs. (3.31) and (3.32) that at \( y_m \),

\[ \bar{C}(y_m) = \hat{C}(y_m) \]  \hspace{1cm} (3.33)

Also, since \( \varepsilon(y) \) is a maximum at \( y_m \)

\[ \varepsilon'(y_m) = 0 \]  \hspace{1cm} (3.34)

and so

\[ \bar{C}'(y_m) = \hat{C}'(y_m) \]  \hspace{1cm} (3.35)

Thus the approximation to \( C(y) \) with maximum error \( \varepsilon_m \) has slope \( \hat{C}'(y_m) \) and passes through \( \hat{C}(y_m) \).

A straight line segment from \( y_1 \), whose slope is more negative than \( C'(y_1) \) and less negative than \( \hat{C}'(y_m) \), is contained between \( C(y) \) and \( \hat{C}(y) \) in the interval from \( y_1 \) to its intersection with \( C(y) \), provided \( y < y_0/\sqrt{2} \). Such a line segment approximates \( C(y) \) within \( \varepsilon_m \) relative error. It is
seen in Fig. 3.1 that in this region

$$|\hat{C}'(y)| < |\hat{C}'(y_m)|$$ (3.36)

if \( y < y_m \).

Let us approximate \( \hat{C}(y_m) \) by a first-order Taylor series, and apply the mean value theorem to the formula for the remainder at \( y_1 \). The remainder at \( y_1 \) is then given as

$$R(y_1) = \frac{(y_1 - y_m)^2}{2} \hat{C}''(y_\tau)$$ (3.37)

where \( y_1 < y_\tau < y_m \). Since the first-order Taylor expansion of \( \hat{C}(y_m) \) is \( \overline{C}(y) \),

$$R(y_1) = \hat{C}(y_1) - \overline{C}(y_1) = - \epsilon_m C(y_1)$$ (3.38)

Combining Eqs. (3.37) and (3.38) and using Eq. (3.32),

$$\Delta y^2 = (y_1 - y_m)^2 = \frac{-2\epsilon_m C(y_1)}{1-\epsilon_m \epsilon''(y_\tau)}$$ (3.39)

This equation gives the distance between \( y_m \) and \( y_1 \) in terms of the maximum relative error, the value of \( C \) at the initial end point, and the curvature of \( C \) at some location between \( y_m \) and \( y_1 \).

If the magnitude of the curvature is overestimated, the distance between \( y_1 \) and \( y_m \) is underestimated. For the region \( y < y_0/\sqrt{2} \), the magnitude of the curvature decreases as \( y \) increases, as is seen in Fig. 3.1. Therefore, the
magnitude of the curvature is a maximum, for an interval, at \( y_1 \), the location in \( y \) of the initial end point of the segment. Using \( C''(y_1) \) in Eq. (3.39) we obtain the underestimated distance

\[
\Delta y^2 = \frac{\varepsilon_m}{1-\varepsilon_m} \frac{y_0^2}{1 - 2 \left( \frac{y_1}{y_0} \right)}
\]

If the slope of the straight line approximation is equal to \( \hat{C}'(y_1 + \Delta y) \), and this is greater than \( C'(y_1) \), the resulting approximation is within the specified maximum error as shown above.

For the region \( y > y_0/\sqrt{2} \), a similar technique is used to obtain the straight line segments of the diffusion approximation. The major difference is that in this region \( \hat{C}(y) \) lies above \( C(y) \):

\[
\hat{C}(y) = (1 + \varepsilon_m) C(y)
\]

for \( y > y_0/\sqrt{2} \). Also, for \( y > \sqrt{3/2} y_0 \) the maximum value of \( C''(y) \) is at the initial end point of the interval and Eq. (3.39) becomes

\[
\Delta y^2 = \frac{\varepsilon_m}{1+\varepsilon_m} \frac{y_0^2}{2 \left( \frac{y_1}{y_0} \right) - 1}
\]

However for \( y_0/\sqrt{2} < y < \sqrt{3/2} y_0 \), the maximum value of \( C''(y) \) in an interval is at the final point in the interval. In
this region, the maximum value attainable by $C''(y)$ is used and Eq. (3.39) becomes

$$\Delta y^2 = \frac{e_m}{1 + e_m} \frac{y_0^{2C(y_1)}}{2C(\sqrt{\frac{3}{2}})}$$  \hspace{1cm} (3.43)

It should be noted that since $C''(y)$ changes little over an interval for small $e_m$, the value of $\Delta y$ estimated from Eqs. (3.41), (3.42), and (3.43) is very close to $(y_m - y_1)$ and so $C'(y_1 + \Delta y)$ was never found to be less than $C'(y_1)$.

In the manner described above, the approximation for the diffusion profile is found and combined with the background profile approximation. The resulting net profile approximation is a series of straight line segments. This reduces the computation of Eqs. (3.2) and (3.4) to a series of simple operations. Also, Eqs. (2.16), (2.17), and (2.22) are evaluated easily because $\sigma(N)$ is a known simple expression and the approximation for $N(y)$ consists of the straight line segments described above.

We have derived expressions for the junction voltage and contact potential. Also, we have shown the relation between the top-gate diffusion parameters and the top-gate junction parameters. The representation for the channel conductivity as a function of net impurity concentration has been given. Also, the approximations used for the background and net impurity profiles have been developed.
CHAPTER 4

THE DESIGN PROCESS

In this chapter we describe the manner in which the diffusion constants for the top gate are chosen. We present the design loops for both the pinch resistor and the JFET. The overall problem is partitioned into well-defined smaller problems and the subroutines which solve these are described.

4.1 The Design Loop

The technique used here to obtain the required values for \( C_0 \) and \( y_0 \) is outlined in Fig. 4.1. It is an iterative scheme whereby an estimate of the correct values for \( C_0 \) and \( y_0 \) is made, and the results computed. These results are compared with the specifications, and errors generated. The errors are used to refine the estimation of \( C_0 \) and \( y_0 \). In this manner, successive estimations converge on a pair of values which yield results within tolerance of the specifications.

In this type of scheme it is possible for successive estimates to diverge. For the problem considered here, there is no analytical expression which can be derived and evaluated to indicate convergence or divergence. However, the subprograms are carefully structured such that impossible and impractical specifications are sensed. No case of
Fig. 4.1 The Overall Design Loop
diverging estimates has been encountered. A major reason for this is the accuracy with which the initial estimate locates the channel limits and junction regions. A second reason is the gradual variation of channel conductance with changes in the top-gate diffusion. Therefore, a combination of device characteristics and computational foresight leads to an iterative scheme which has converged or indicated the faulty specification for every case tried.

The entire routine actually consists of two separate loops, one for the pinch resistor and the other for the JFET. Both of these require similar preparatory operations concerning the background, specifications, etc., which are performed prior to entering either loop. During the preparatory and iterative steps, several utility routines are used in both design processes. Also there is a monitor which directs the processes and senses either the successful completion or the occurrence of an error.

4.2 The Monitor

The routine which monitors and directs the design process is outlined in Fig. 4.2. In actuality, the routine only transfers control to several of the subprograms described below, which carry out the processes indicated. On a return from any of these, it determines whether an impossible or impractical specification has been detected. Also, when the successful completion of the design is
Fig. 4.2 The Monitor Routine
indicated to the monitor the job is ended. We next describe the utility routines and, after them, the routines used in the direct process shown in Fig. 4.2.

4.3 The Net-Profile Approximation

Routine NTPRFL constructs the net-profile approximation from the background approximation and the diffusion approximation as described in Section 3.3. A flow diagram of NTPRFL is shown in Fig. 4.3. NTPRFL requires as data the background-profile approximation and the two constants of the diffusion. It computes and stores the net-profile approximation and notes the locations of the metallurgical junctions, if there are any.

The approximation to the diffusion is calculated one end point at a time, and the net-profile approximation for this end point is computed before the next diffusion-approximation end point is calculated. The relative error used here for both the background and diffusion approximations is 1 per cent.

The diffusion-approximation end points are obtained as indicated in Section 3.3. The equations for the approximation to the point of maximum error, Eqs. (3.40), (3.42), and (3.43), are solved in the appropriate regions, and the slope of the approximation is thus found. It should be noted that the boundaries of these regions--\( y = 0 \), \( y = y_0 / \sqrt{2} \), and \( y = \sqrt{3/2} y_0 \)--are used as interval end points.
Fig. 4.3 Flow Chart of NTPRFL
The intersection of $\overline{C}$ and $C$ is found by the well-known Newton-Raphson iteration method (Pennington 1965, p. 236). The intersection point first is estimated to be twice the distance from $y_1$ that the maximum error point is estimated to be. With this technique, convergence always has occurred on the second iteration. The criterion for convergence is an error of no more than 0.1 per cent in concentration. The use of this method for approximating the Gaussian diffusion profile with a maximum relative error of 1 per cent requires less than fifty points for the first five orders of magnitude in concentration.

We obtain the net-profile approximation by subtracting the concentration at the interval end point from that obtained by linear interpolation on the interval extending beyond the end point. In this manner we proceed from the wafer surface.

After each end point of the net-profile approximation has been found, a test is made to determine whether a junction has occurred. Since the net concentration at a metallurgical junction is zero, a net-profile concentration which changes sign over an interval indicates a junction within the interval. If a junction has occurred, its location is noted.

The magnitude of the diffusion concentration decreases monotonically from the wafer surface. Therefore when it drops to 0.001 times the magnitude of the background
concentration, we neglect it at all points further into the wafer. This presumes that the background concentration falls off less rapidly than the diffusion concentration. For all practical situations this is true. Beyond this point of negligible diffusion concentration, the net-profile approximation is made equal to the background-profile approximation.

The accuracy of the net-profile approximation was checked by comparing the results of the approximation to a known net profile at points halfway between interval end points. The resulting error, relative to the known concentration, is shown in Fig. 4.4. The known net profile is:

\[
N(y) = -7.4 \times 10^{19} e^{-\left(\frac{y}{1.65}\right)^2} + 5.0 \times 10^{18} e^{-\left(\frac{y}{2.07}\right)^2} - 9.7 \times 10^{14} \text{cm}^{-3}
\]  \hspace{1cm} (4.1)

As can be seen from Eq. (4.1) this is a double-diffused structure with an initial constant background concentration. The background approximation was first obtained from the initial diffusion and the constant background. The positions of the junctions and the equilibrium depletion widths are shown in Fig. 4.4. As is shown in the figure, except for the immediate vicinity of the junction the accuracy is within 1 per cent.
Fig. 4.4 Accuracy of 1 Per Cent Profile Fit
4.4 The Depletion-Versus-Voltage Calculation

Routine DPLVSV determines the contact potential and the thermal equilibrium depletion-region edges of a junction. It also calculates the edges of the region for a given reverse-bias voltage, \( V_B \), and the first derivative of these edges with voltage. Figure 4.5 shows an outline of the routine.

DPLVSV requires the net profile and, thus, the positions of the junctions to have been found. The particular junction of interest, its reverse-bias voltage, and certain limits must be given. These limits are spatial boundaries beyond which the depletion region is not permitted to extend, e.g., a neighboring junction or the wafer surface. If one of these is exceeded an error is sensed and appropriate action taken.

Referring to Fig. 4.5, we see that a charge balance is obtained in an interval around the junction. This satisfies Eq. (3.2), therefore Eq. (3.4) may be used to determine the voltage difference across the interval. Because we deal with the net-profile approximation, the intervals yield trapezoids in Eq. (3.2) and both the charge balance and voltage calculations are simple.

The magnitude of this voltage is compared to \( |V_{Cj}| \), the evaluation of Eq. (3.13). If it is less than \( |V_{Cj}| \) another increment is made. If \( |V_{Cj}| \) is exceeded, the dimensions are found for \( |V_j| = |V_{Cj}| \). Thus, the contact
Fig. 4.5 Flow Chart of DPLVSV
potential and the equilibrium depletion-region edges are found according to the development of Section 3.1. We determine the correct values for the edges, and hence for $V_{Cj}$, by the Bisection method, as described by Pennington (1965, p. 220), applied to the last interval processed. This method is used because it is known to converge since $|V_j| < |V_{Cj}|$ before the processing of the interval and $|V_j| > |V_{Cj}|$ after the processing.

Once the contact potential has been found, the applied reverse bias is added to it. Then, by a procedure similar to that described above, the edges for the depletion region with this total voltage are determined. In this case, however, the voltage reference is fixed at $|V_j| = |V_{Cj}| + |V_B|$. The first derivative of the left and right depletion-region edges is computed using Eq. (2.20).

### 4.5 The Placement Routines

Two placement routines are used here, SEARCH and LOCATE. Both place a specific value for a variable in an ordered table or array composed of values of that variable. They do this by a variation of the well-known Binary Search technique. (See, e.g., Hellerman 1967, p. 149.)

LOCATE finds the interval in the background or net-profile approximation within which a given spatial value, $y$, lies. The ordered array is composed of the $y$ values of the approximation end points.
SEARCH finds the interval in the conductivity versus net-concentration approximation to Irvin's (1962) curve within which a given value of channel impurity concentration lies. The ordered array is composed of the breakpoints from Irvin's curve obtained as described in Section 3.2. SEARCH also computes the value of conductivity as obtained from the approximation to Irvin's curve for this given net impurity concentration.

4.6 The Calculation of Sheet Conductance

Routine SHTCON calculates the sheet conductance of a layer of the channel. It requires the boundaries of the layer, the net-profile approximation in the channel, and the information in Table 3.1 or 3.2, whichever applies. Figure 4.6 is a diagram of the routine. The layer sheet conductance is calculated by summing the sheet conductances of sub-regions of the channel which compose the layer. We solve equations of the form of Eq. (2.16) for each subregion, making use of the conductivity approximation in Eq. (3.25) and the straight-line approximation to the net profile.

The first step performed in SHTCON is placing the lower boundary in the net profile. SHTCON calls on LOCATE to do this. It then calculates the concentration at the lower boundary by interpolating on the net-profile approximation. SHTCON then calls SEARCH to place this concentration in the conductivity approximation and to determine the
Fig. 4.6 Flow Chart of SHTCON
pair of constants in Eq. (3.25). The far end point of the net-profile interval is chosen as the upper point and compared to the upper boundary.

If the interval end point exceeds the upper boundary, the interval is reduced to the upper boundary and a flag is set. Next, SHTCON checks the concentration at the interval end point to see if it is outside the conductivity-approximation interval. If this is so, the channel interval is reduced to that point where the concentration equals the breakpoint, and the flag, if set, is reset. This process only requires interpolating on the straight-line net-profile approximation.

SHTCON then obtains the sheet conductance of the channel interval. Equation (2.16) for a channel interval reduces to

$$\sigma_{Si} = \frac{K_i}{s} \frac{N_{i+1}}{P_i + 1} - \frac{N_i}{P_i + 1}$$

(4.2)

where $\sigma_{Si}$ is the sheet conductance of the interval; $K_i$ and $P_i$ are the conductivity constants of Eq. (3.25) valid over the interval; $N_2$ and $N_1$ are the net concentrations at the upper and lower end points, respectively; and $s$ is the net-concentration slope in the interval.

If the slope is zero, the following equation is valid:

$$\sigma_{Si} = K_i N_1 P_i (y_2 - y_1)$$

(4.3)
where }y_2\text{ and }y_1\text{ are the spatial variables at the interval upper and lower end points, respectively.}

The next interval is treated and this process continues until the upper boundary is reached, the }\sigma_{Si}\text{ being summed to get the total sheet conductance of the layer.

4.7 Determination of Gaussian Constants

Routine COCY solves Eq. (3.20) for }y_0\text{ and Eq. (3.18) for }C_0\text{. It is diagramed in Fig. 4.7. It requires the background-profile approximation, the junction voltage--}V_j\text{, and the depletion-region edges--}y_L\text{ and }y_R\text{. COCY senses four sources of error, corrects three and takes appropriate action on the fourth. In circumventing the three error conditions, }y_L\text{ is moved closer to the wafer surface. This can be done because the position of the upper depletion-region edge always is estimated for the cases here. Since it never is fixed, it may be moved if necessary to satisfy one of the requirements described below.}

COCY first evaluates the integrals in the left-hand sides of Eqs. (3.18) and (3.19). Then it checks to ensure that:

\[
y_R \left| \int_{y_L}^{y_R} y_B(y) dy \right| > \left| \frac{e}{q} V_j \right|
\]

(4.4)

If this is not satisfied, }y_L\text{ is moved toward the surface. This operation increases the left-hand side of Eq. (4.4). When Eq. (4.4) is satisfied, the quantity }\gamma\text{ described in
Fig. 4.7 Flow Chart of COCY
Section 3.1 is evaluated and the condition of Eq. (3.24) is checked. If this condition is not satisfied, the depletion-region edges are adjusted. This process succeeds because $\gamma$ is not as strong a function of $y_L$ and $y_R$ as $y_L + y_R$ and $2y_L$ are. It should be noted that for all the cases attempted the condition

$$2 \gamma < y_L + y_R$$

(4.5)

was always satisfied.

COCY then solves Eq. (3.20) by an iterative technique. It first does a six-step Bisection iteration (Pennington 1965, p. 220) using the initial interval $0 < y_0 < y_R$. Then the Newton-Raphson iteration method (Pennington 1965, p. 236) finishes the determination of $y_0$ to 0.1 per cent. Next COCY solves Eq. (3.18) for $C_0$. If this value of $C_0$ exceeds a maximum specified value, $y_L$ is moved closer to the surface and the whole process repeated. Reducing $y_L$ has the effect of increasing $y_0$, and thus the value of $C_0$ satisfying Eq. (3.18) is reduced.

If in any of these operations $y_L$ approaches too close to the surface for practical considerations, COCY signals for an error-type termination.

In solving Eq. (3.20), COCY uses the Gaussian and error functions. As $y_0$ becomes small, the numerator of the right-hand side of Eq. (3.20) becomes the difference of small quantities and the denominator becomes the difference
of two quantities which approach unity very closely. COCY anticipates this condition and as $y_0$ gets small the difference between complementary error functions is substituted for the difference between error functions. The former are evaluated using an asymptotic expansion reported by Abramowitz and Stegun (1964, p. 298).

Thus, $C_0$ and $y_0$ are determined and, if necessary, the depletion region is adjusted. This is the last of the utility routines; we now describe the routines in the direct design path shown in Fig. 4.1.

4.8 The Preparatory Operations

Routine INPUT, diagramed in Fig. 4.8, performs the preparatory operations common to the JFET and pinch-resistor design. It assembles the background-profile approximation and reads in the specifications and their tolerances. The conductivity approximation corresponding to the channel conductivity type is stored. In the case of the pinch resistor, INPUT determines the lower edge of the channel at the drain by calling the lower-junction depletion-region edges from DPLVSV. It also stores the net concentration at this point and uses this as a reference to determine whether the top-gate diffusion extends into the lower depletion region, thereby modifying it.

INPUT then calls for the first estimate of $C_0$ and $y_0$ from the routine appropriate to the device type. These are
Fig. 4.8 Flow Chart of INPUT
described below. After this has been done, INPUT returns control to the monitor.

We next treat the two loops in Fig. 4.2 including the routines making the first guess at $C_0$ and $y_0$. The entire pinch-resistor loop receives first consideration.

4.9 Pinch-Resistor Initial Estimate

Routine GUES1, diagramed in Fig. 4.9, makes the initial guess of the diffusion constants based on the device specifications and the background profile. We assume in making the first estimate that the diffusion does not modify the channel profile or the lower-junction characteristics. The channel conductivity is integrated by intervals, as described in Section 4.6, toward the surface. In using SEARCH to find the starting point, $\sigma(a(V_{DS},V_{GS}))$ is found.

The total conductance after each interval has been processed is compared to the specification for $\sigma_s$. If the surface is reached before the specification is satisfied, an impossible specification has been set and appropriate action is taken. When the specification is exceeded, the current interval end point becomes the upper channel edge, $b$. This process overestimates the channel width, which partially offsets the compensation of the channel by the top-gate diffusion.

The contribution of the lower gate to the linearity, $\sigma'_s$, is computed using the lower-gate characteristics
Fig. 4.9 Flow Chart of GUES1
already known. If this exceeds the specification for $\sigma',$ another impossible specification has been set. If the linearity specification is too stringent, appropriate action is taken. If the linearity specification is not exceeded by the lower-gate junction, the width of the upper depletion region is determined from the following equation:

$$W_1 = \left( \frac{e}{q} \frac{\sigma(b)}{N(b)} \right) \frac{1}{\Delta \sigma'_S}$$  \hspace{1cm} (4.6)

The difference between the specified linearity and that of the lower junction is $\Delta \sigma'_S$. Using these values for $b$ and $W_1$, GUESl calculates the upper limit of the top depletion region and calls on COCY to determine $C_0$ and $y_0$. The contact potential of the upper junction is assumed to be 0.7 volts. Control then passes back to INPUT.

4.10 Evaluation of Pinch-Resistor Structure

Routine TEST, diagramed in Fig. 4.10, tests the estimation of the pinch-resistor diffusion parameters by computing the resulting channel sheet conductance and its linearity and comparing these to the specifications. If the specifications are met within the tolerable error, it returns control to the main program. If they are not, it computes error parameters and passes these to subroutine REVISE, which makes the revision of the estimate of $C_0$ and $y_0$. 
Fig. 4.10 Flow Chart of TEST
First TEST checks to see if the lower junction has been modified by the top diffusion. If the diffusion concentration at the old lower channel edge is less than 1 per cent of the background there, TEST decides there has been no appreciable modification. If there has been modification, the lower gate-junction edge, linearity, and edge conductivity are recomputed using DPLVSV and SEARCH.

Next TEST finds the top-junction parameters: lower edge, conductivity, and edge linearity using DPLVSV and SEARCH. Then TEST computes the channel conductance by passing appropriate parameters to SHTCON. The channel-conductance linearity is computed from Eq. (2.17) and the errors associated with $\sigma_S$ and $\sigma_S'$ are determined.

If these errors are within tolerance, the drain current and sensitivities also are computed. The drain current per unit $Z/L$ at $(V_{DS}, V_{GS})$ for the structure is computed from Taylor's expansion of $I_D(V_D)$ about $V_D = 0$ volts.

$$I_D(0) = I_D(V_{DS}) - \frac{\partial I_D}{\partial V_D}|_{V_{DS}} \cdot V_{DS} + \frac{\partial^2 I_D}{\partial V_D^2}|_{V_{DS}} \frac{V_{DS}^2}{2} + \ldots \quad (4.7)$$

The left-hand side of Eq. (4.7) is zero. Making use of Eqs. (2.7) and (2.10), we get

$$I_D(V_{DS}) = \sigma_S V_{DS} - \sigma_S' \frac{V_{DS}^2}{2} \quad (4.8)$$
The sensitivities of $\sigma_S$ and $\sigma'_S$ to the two processing steps are computed as described below. The sensitivities of $\sigma_S$ to $y_0$ and to $C_0y_0$ are defined as

$$S_{\sigma_S} = \left( \frac{\sigma_S}{\partial y_0} \right)^{y_0}$$

and

$$S_{\sigma'_S} = \left( \frac{\sigma'_S}{\partial y_0} \right)^{y_0}$$

Note that

$$C_0 = \frac{2}{\sqrt{\pi}} \frac{Q}{y_0}$$

We evaluate Eq. (4.9) here by increasing $y_0$ and decreasing $C_0$ by 1 per cent and recomputing $\sigma_S$. The relative change in $\sigma_S$ is assumed to be $S_{\sigma_S}^{y_0}$. Similar operations lead to $S_{\sigma'_S}$ and to the sensitivities of $\sigma'_S$.

**4.11 Adjustment of Pinch-Resistor Diffusion**

Routine REVISE adjusting the upper channel edge and the upper-junction width. If the channel conductance does not meet the specifications, the width of the channel is adjusted. In this manner, the upper-edge integration limit in Eq. (2.16) increases or decreases as is necessary. REVISE makes the change in position based on a conductivity
which is the average conductivity of the channel, i.e.,

\[ \Delta b = \Delta \sigma_S \cdot \frac{(a-b)}{\sigma_S} \]  

(4.12)

If the channel linearity does not meet its specification, REVISE increases the upper depletion-region width. Then the new upper depletion-region edges are passed to COCY, which redetermines \( C_0 \) and \( y_0 \). Control then passes to the monitor, which calls TEST. This loop proceeds until TEST indicates to the monitor that a design has been successfully completed or that an error has occurred.

We next describe the design loop for the JFET starting with the routine which makes the first estimate of \( C_0 \) and \( y_0 \).

4.12 JFET Initial Estimation of \( C_0 \) and \( y_0 \)

Routine FETGS, diagramed in Fig. 4.11, is called by INPUT. It makes the initial estimation of the diffusion parameters for the JFET. Using the specifications, FETGS calculates the top-gate depletion-region position and calls on COCY to find the proper values of \( C_0 \) and \( y_0 \). This determination assumes that the diffusion does not modify the channel. FETGS also senses certain errors.

First, FETGS finds the lower-junction parameters. Using DPLVSV it determines the lower depletion-region edge at the drain and source with \( V_{GS} \) and \( V_{DS} \) applied. The transconductance contribution of the lower junction is then
Fig. 4.11 Flow Chart of FETGS
found using SHTCON. Next, in a process similar to that described in Section 4.9, FETGS integrates the channel conductivity until the specification on $g_m$ is satisfied. This point becomes $b(0, V_{GS})$. Again appropriate action is taken if the surface is reached before the specification is satisfied.

Then, FETGS guesses the upper edge of the top depletion region for $(V_{DS}, V_{GS})$ applied. COCY is called to calculate the diffusion constants. FETGS then calls DPLVSV to determine the lower edge of the top depletion region for $(0, V_{GS})$ applied. This is compared to that value for $b(0, V_{GS})$ resulting from the $g_m$ calculation above. If the difference is small enough, control returns to INPUT. If the difference is larger than 1 per cent, FETGS adjusts the value of the upper edge of the top depletion region and the whole process is repeated.

### 4.13 Evaluation of JFET Parameters

Routine EVAL, diagramed in Fig. 4.12, computes the JFET parameters for a given top-gate diffusion. The calculated pinch-off voltage and transconductance are compared to the specifications and the errors are computed. If these errors are too large, EVAL passes them to subroutine ADJUST for a revision of the diffusion constants. If the errors are within tolerance, EVAL computes the drain
start

is low jct. modified?

yes

recompute low jct char.

no

compute high jct. char.

compute $g_m \& V_P$

are specs met?

yes

compute $I_D \&$ sensitiv.

no

revise $C_0$, $y_0$ values

return

Fig. 4.12 Flow Chart of EVAL
current and the sensitivities of the specified parameters to variations in the two steps of the diffusion process.

First, EVAL checks to see if the lower depletion region has been modified by the top-gate diffusion. If the diffusion concentration at the pinch-off point estimated in the absence of the top diffusion is 1 per cent of the background concentration there, EVAL assumes modification has taken place. If there has been modification the lower-junction parameters are recomputed. This redetermines the location $a(V_{DS}, V_{GS})$.

Next the upper-junction parameters are determined. This determines $b(V_{DS}, V_{GS})$. If the difference between $a(V_{DS}, V_{GS})$ and $b(V_{DS}, V_{GS})$ is not sufficiently small, the source-drain voltage is adjusted and $a(V_{DS}, V_{GS})$ and $b(V_{DS}, V_{GS})$ recalculated. When they coincide, the value of source-drain voltage is the actual pinch-off voltage for this structure.

EVAL then calls DPLVSV to get $a(0, V_{GS})$ and $b(0, V_{GS})$. Using these values, SHTCON computes the device transconductance. These actual values for the device parameters are compared to the specifications and the errors computed. If the errors are not within tolerance, EVAL calls subroutine ADJUST to revise the values of $C_0$ and $y_0$. If the errors are small enough, the values of drain current and the sensitivities are calculated. The sensitivity calculations are similar to those described in Section 4.10. The drain
current per unit $Z/L$ of the pinched-off channel at $V_{GS}$ is found by a method similar to that described in that section. Expanding $I_D$ about $V_{DS} = 0$ volts, we obtain

$$
\bar{I}_D(V_{DS}) = \bar{I}_D(0) + \bar{g}_{22} \left|_{(0,V_{GS})} \right. V_{DS} + \bar{g}_{22} \left. \right|_{(0,V_{GS})} \frac{V_{DS}^2}{2} + \ldots
$$

(4.13)

Since the sum of $\bar{g}_{22}$ and $\bar{g}_m$ is a constant,

$$
\bar{g}_{22} \left|_{(0,V_{GS})} \right. = \bar{g}_m \left|_{(V_{DS},V_{GS})} \right.
$$

(4.14)

and

$$
\bar{g}_{22} \left|_{(0,V_{GS})} \right. = \frac{\partial g_m}{\partial V_{GS}} \left|_{(V_{DS},V_{GS})} \right.
$$

(4.15)

Using Eqs. (4.14) and (4.15) we approximate the drain current at pinch-off for a given $V_{GS}$.

4.14 Revision of JFET Diffusion Constants

Routine ADJUST revises the diffusion constants in the JFET structure based on the errors in pinch-off voltage and transconductance. The product of the voltage error and the first derivative of $a$ at the calculated pinch-off voltage yields a change in the position in the channel of the lower edge of the upper-gate depletion region at the pinch-off voltage. The error in $g_m$ can be related to an error in the position of the lower limit of the second
integral in Eq. (2.21). ADJUST uses the error to determine a revised position for the top-gate diffusion. It then calls COCY to evaluate the revised values for $C_0$ and $y_0$ and returns control to the monitor, which calls EVAL. This loop continues until EVAL indicates to the monitor that a design has been successfully completed or that an error has occurred.

The segments of the design process have been described above. We have indicated their functions and have sketched their interconnections. Also, the criteria for satisfying certain relations have been given.
CHAPTER 5

EXAMPLES

This chapter reports the results of the design process for both types of channel devices. We examine the convergence of the design process and some characteristics of the resulting devices.

5.1 The Substrate Pinch Resistor

We begin the design of the pinch resistor with a typical integrated-circuit profile. The background consists of an 8 micron, 0.6 ohm-cm n-type epitaxial layer grown on a 5 ohm-cm substrate. The first set of device-parameter specifications is a sheet conductance of $2.0 \times 10^{-4} \pm 1.0 \times 10^{-5}$ mhos per square with maximum nonlinearity of 15 per cent per volt for $V_{GS} = 0$ and $V_{DS} = 6$ volts.

Table 5.1 lists the results after each iteration in the design process. The process yields the following values for the top-gate diffusion parameters after six steps.

- $C_0 = 4.347 \times 10^{18}$ cm$^{-3}$
- $y_0 = 1.843$ microns
- $y_{11} = 4.611$ microns

The resulting device parameters are:
Table 5.1. Pinch-Resistor Design Example

<table>
<thead>
<tr>
<th>Iteration Number</th>
<th>( C_0 ) (cm(^{-3}))</th>
<th>( Y_0 ) (microns)</th>
<th>( \sigma_S ) (mhos/square)</th>
<th>( \sigma_S' ) (mhos/square-volt)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( 4.947 \times 10^{17} )</td>
<td>1.552</td>
<td>( 4.22 \times 10^{-4} )</td>
<td>( 1.33 \times 10^{-5} )</td>
</tr>
<tr>
<td>2</td>
<td>( 2.863 \times 10^{19} )</td>
<td>1.377</td>
<td>( 3.10 \times 10^{-4} )</td>
<td>( 1.42 \times 10^{-5} )</td>
</tr>
<tr>
<td>3</td>
<td>( 8.932 \times 10^{18} )</td>
<td>1.630</td>
<td>( 2.53 \times 10^{-4} )</td>
<td>( 1.37 \times 10^{-5} )</td>
</tr>
<tr>
<td>4</td>
<td>( 5.791 \times 10^{18} )</td>
<td>1.753</td>
<td>( 2.25 \times 10^{-4} )</td>
<td>( 1.35 \times 10^{-5} )</td>
</tr>
<tr>
<td>5</td>
<td>( 4.727 \times 10^{18} )</td>
<td>1.815</td>
<td>( 2.12 \times 10^{-4} )</td>
<td>( 1.34 \times 10^{-5} )</td>
</tr>
<tr>
<td>6</td>
<td>( 4.347 \times 10^{18} )</td>
<td>1.843</td>
<td>( 2.06 \times 10^{-4} )</td>
<td>( 1.34 \times 10^{-5} )</td>
</tr>
</tbody>
</table>

Device specifications:

\( \sigma_S = 2.0 \pm 0.1 \times 10^{-4} \) mhos per square

\( \sigma_S' < 3.0 \times 10^{-5} \) mhos per square-volt

\( V_{GS} = 0 \) volts

\( V_{DS} = 6 \) volts
\( \sigma_s = 2.057 \times 10^{-4} \) mhos per square

\( \sigma_s' < 7 \) per cent per volt

\( I_D = 1.475 \) milliamps per Z/L

\( S_{\sigma^s}^{Y_0} = 0.2 \)

\( S_{\sigma^s}^{Q} = 0.03 \)

\( S_{\sigma^s}^{Y_0} = 3.1 \)

\( S_{\sigma^s}^{Q} = 0.3 \)

This represents a reduction in the epi-layer sheet conductance by approximately a factor of five. The upper-gate junction depth is at 4.611 microns and the undepleted-channel width at the drain is about 1.5 microns. The top-gate diffusion does not modify the lower junction even though the channel is pinched considerably. The sensitivities of the device parameters to the diffusion parameters are very small. This follows from the relatively wide undepleted channel and the fact that the lower-gate junction is not modified by the top-gate diffusion.

The nonlinearity specification on the above device next is reduced to 5 per cent per volt and the design rerun. After eight iterations, the following diffusion specifications are obtained.
\[ C_0 = 1.672 \times 10^{16} \text{ cm}^{-3} \]
\[ y_0 = 4.262 \text{ microns} \]
\[ y_{jl} = 3.464 \text{ microns} \]

The resulting device parameters are:

\[ \sigma_S = 2.056 \times 10^{-4} \text{ mhos per square} \]
\[ \sigma_S' < 5 \text{ per cent per volt} \]
\[ I_D = 1.414 \text{ milliamps per Z/L} \]
\[ S_{\sigma_S}^{y_0} = 0.2 \]
\[ S_{\sigma_S}^{Q} = 0.1 \]
\[ S_{\sigma_S}^{y_0} = 1.9 \]
\[ S_{\sigma_S}^{Q} = 1.4 \]

The device requires a much wider top-gate junction to achieve the specified linearity. The top-gate junction is at 3.464 microns and the depletion region at the drain extends from 2.158 to 4.783 microns. The lower junction is modified slightly by the diffusion, the metallurgical junction being moved to 7.859 microns, 0.16 microns closer to the surface. The impurity compensation in the channel changes the width of the undepleted channel at the drain to 2 microns. Nevertheless, the drain current remains relatively unchanged. The sensitivities are again very small.
The next step is to reduce the sheet-conductance specification and further pinch off the channel. The specifications are a channel conductance of $1.5 \times 10^{-4} \pm 7.5 \times 10^{-6}$ mhos per square with less than 15 per cent per volt nonlinearity. The background and voltages remain the same. After six iterations the following diffusion constants are specified.

$$C_0 = 4.140 \times 10^{17} \text{cm}^{-3}$$
$$y_0 = 2.448 \text{microns}$$
$$y_{jl} = 4.842 \text{microns}$$

The resulting device parameters are:

$$\sigma_S = 1.546 \times 10^{-4} \text{ mhos per square}$$
$$\sigma_S \leq 9 \text{ per cent per volt}$$
$$I_D = 1.150 \text{ milliamps per Z/L}$$

$$\frac{\sigma_S}{S_{y_0}} = 0.2$$
$$\frac{\sigma_S}{S_{y}} = 0.1$$
$$\frac{\sigma_S}{S_{y_0}} = 4.3$$
$$\frac{\sigma_S}{S_{Q}} = 0.5$$

For this case, the undepleted channel at the drain is reduced to 1 micron and the lower-gate junction very
slightly modified. Also, the sensitivities show little change from the previous example. If the nonlinearity specification is reduced to 5 per cent, the required top-gate depletion region comes too close to the surface for the device to be fabricated. The indicated surface concentration is \( C_0 = 1.093 \times 10^{16} \text{cm}^{-3} \), which is only slightly higher than the background concentration at the surface, \( 0.8 \times 10^{16} \text{cm}^{-3} \).

It should be noted that for the above devices, the difference between the large-signal and small-signal channel conductance is about 10 per cent for the \( 2.0 \times 10^{-4} \) mhos per square devices and about 25 per cent for the \( 1.5 \times 10^{-4} \) mhos per square device. The difference in sheet conductance for the 15 per cent linearity devices can be attributed mainly to the decrease in channel width, the remainder being caused by impurity compensation in the channel. The above examples each required approximately two seconds CPU time on The University of Arizona CDC 6400.

From the above examples, it can be seen that the pinch-resistor structure can be used to reduce the epi-layer conductance with good results. However, certain guidelines are to be followed.

1. The reduction should not exceed ten to one.
2. The linearity specification should be kept loose, approximately 10 per cent or more.
Because the epi-layer is doped uniformly, any channel-conductance reduction is equivalent to a proportional channel-width reduction. A large reduction ratio is difficult to accomplish because of the deep top-gate junction depths required. An alternative is impurity compensation in the channel but this is not very effective and very low surface concentrations result.

5.2 The Double-Diffused Pinch Resistor

For this example we choose a background of 5 ohm-cm n-type epi-layer with a p-type Gaussian diffusion having a surface concentration of $5 \times 10^{18} \text{cm}^{-3}$ and a characteristic length of 2.065 microns. The lower-junction depth is at 6.041 microns and the substrate is assumed to be located far enough away from this to be ignored—4 microns or more. This structure is a deep n-p-n transistor without the emitter diffusion.

The first set of device-parameter specifications is a sheet conductance of $2.0 \times 10^{-3} \pm 2.0 \times 10^{-4}$ mhos per square with maximum nonlinearity of 10 per cent per volt for $V_{GS} = 0$ and $V_{DS} = 1$ volt. After one iteration, the specified diffusion parameters are:

- $C_0 = 1.074 \times 10^{19} \text{cm}^{-3}$
- $Y_0 = 1.486$ microns
- $Y_{jl} = 1.873$ microns
The resulting device parameters are:

\[
\sigma_S = 1.800 \times 10^{-3} \text{ mhos per square}
\]

\[
\sigma_S' < 7 \text{ per cent per volt}
\]

\[
I_D = 1.806 \text{ milliamps per Z/L}
\]

\[
S_{Y_0}^{\sigma_S} = 1.4
\]

\[
S_Q^{\sigma_S} = 1.1
\]

\[
S_{Y_0}^{\sigma_S} = 3.6
\]

\[
S_Q^{\sigma_S} = 1.0
\]

This represents a decrease in layer conductance of approximately a factor of six. The top-gate junction depth is at 1.873 microns, and the lower junction is not modified. The undepleted channel at the drain is 3.4 microns wide. The device-parameter sensitivities are small but not negligible.

The drain voltage is increased to 5 volts and the device redesigned. The results after two iterations are:

\[
c_0 = 2.45 \times 10^{20} \text{ cm}^{-3}
\]

\[
y_0 = 0.966 \text{ microns}
\]

\[
y_{j1} = 2.155 \text{ microns}
\]

The resulting device parameters are:
\[ \sigma_S = 1.897 \times 10^{-3} \text{ mhos per square} \]
\[ \sigma_S' < 1 \text{ per cent per volt} \]
\[ I_D = 9.583 \text{ milliamps per } Z/L \]
\[ S_{\sigma_S} = 0.3 \]
\[ S_{\sigma_S'} = 0.1 \]
\[ S_{\sigma_S} = 2.8 \]
\[ S_{\sigma_S'} = 0.3 \]

The top-gate junction depth is 2.155 microns and the undepleted-channel width at the drain is approximately 3 microns. The lower junction remains unchanged. Even though the channel is narrower for this device than the previous device, the conductance specification is met rapidly due to the lack of significant compensation in the channel. The large-signal and small-signal conductances for these devices differ by less than 2 per cent.

The conductance specification then is reduced to \[1.0 \times 10^{-3} \pm 1.0 \times 10^{-4} \text{ mhos per square}, \text{ linear within 10 per cent per volt for } V_{GS} = 0 \text{ and } V_{DS} = 5 \text{ volts.} \] The diffusion specifications, again found after two iterations, are:

\[ C_0 = 5.826 \times 10^{19} \text{ cm}^{-3} \]
\[ y_0 = 1.294 \text{ microns} \]
\[ y_{jl} = 2.602 \text{ microns} \]

The resulting device parameters are:

\[ \sigma_S = 1.020 \times 10^{-3} \text{ mhos per square} \]
\[ \sigma_S' < 1 \text{ per cent per volt} \]
\[ I_D = 5.194 \text{ milliamps per } Z/L \]
\[ S_{\sigma_S} = 0.1 \]
\[ S_{\sigma_S'} = 0.1 \]
\[ S_{\sigma_S} = 4.9 \]
\[ S_{\sigma_S'} = 0.6 \]

The top-gate junction depth is 2.602 microns and the channel width is 2.5 microns. The lower junction is unchanged and the large-signal conductance is within 2 per cent of the small-signal conductance. The double-diffused pinch resistors required approximately 1.5 seconds CPU time.

These examples show that relatively large decreases in layer conductance are achieved with little nonlinearity for the double-diffused pinch resistor. The resulting devices have small sensitivity to processing variations. This is attributable to the relatively wide channel which remains after the channel has been pinched. The large decrease in conductance with a wide channel remaining
results from the top gate removing the highly conductive upper section of the diffused channel. Therefore, compared to the substrate pinch resistor, the double-diffused device allows a greater relative reduction in channel conductance for a given channel width. Also, because the entire channel region is closer to the surface, double-diffused devices are easier to fabricate.

5.3 The Double-Diffused JFET

The double-diffused structure above can be made as a JFET if the channel is pinched off further. Two examples are considered. The background is the same—5 ohm-cm, n-type epi-layer with a p-type Gaussian diffusion having a surface concentration of \(5 \times 10^{18} \text{ cm}^{-3}\) and a characteristic length of 2.065 microns.

The first set of specifications is a \(g_m\) of \(16 \pm 1.6 \times 10^{-6} \text{ mhos per unit Z/L}\) and \(V_P = 1.7 \pm 0.17 \text{ volts}\), with \(V_{GS} = 0 \text{ volts}\). Table 5.2 lists the results after each iteration in the design process.

The following diffusion parameters are specified after three steps:

\[
C_0 = 5.441 \times 10^{19} \text{ cm}^{-3}
\]

\[
y_0 = 1.689 \text{ microns}
\]

The resulting device parameters for both gates connected together are:
Table 5.2. JFET Design Example

<table>
<thead>
<tr>
<th>Iteration Number</th>
<th>$C_0$ (cm$^{-3}$)</th>
<th>$Y_0$ (microns)</th>
<th>$V_p$ (volts)</th>
<th>$\overline{g_m}$ (mhos)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$9.602 \times 10^{19}$</td>
<td>1.639</td>
<td>1.25</td>
<td>$11.2 \times 10^{-6}$</td>
</tr>
<tr>
<td>2</td>
<td>$4.560 \times 10^{19}$</td>
<td>1.710</td>
<td>1.51</td>
<td>$13.0 \times 10^{-6}$</td>
</tr>
<tr>
<td>3</td>
<td>$5.441 \times 10^{19}$</td>
<td>1.689</td>
<td>1.80</td>
<td>$14.7 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Device specifications:

$$\overline{g_m} = 16 \pm 1.6 \times 10^{-6} \text{ mhos}$$
$$V_P = 1.7 \pm 0.17 \text{ volts}$$
$$V_{GS} = 0 \text{ volts}$$
\[ g_m = 14.7 \times 10^{-6} \text{ mhos per Z/L} \]

\[ V_p = 1.804 \text{ volts} \]

\[ y_p = 5.228 \text{ microns} \]

\[ I_D = 6.735 \text{ microamps per Z/L} \]

\[ S_{Vp} = 64.8 \]

\[ S_{VQ} = 10.1 \]

\[ S_{g_m} = 60.6 \]

\[ S_{y_0} = 5.9 \]

The lower junction is moved to 5.973 microns and the upper junction is at 4.551 microns. The modification of the lower junction is considerable. Because both specified parameters are determined largely by the top-gate diffusion, the parameter sensitivities are very large. It can be seen that the sensitivities to \( y_0 \) are extreme.

The specifications are changed to a \( g_m \) of \( 22 \pm 2.2 \times 10^{-6} \) mhos per Z/L and a \( V_p \) of \( 2.6 \pm 0.26 \) volts. The background and \( V_{GS} \) are unchanged. After two iterations, the specified diffusion parameters are:

\[ C_0 = 1.131 \times 10^{20} \text{ cm}^{-3} \]

\[ y_0 = 1.608 \text{ microns} \]

The resulting device parameters for both gates connected together are:
\[ g_m = 21.1 \times 10^{-6} \text{ mhos per } Z/L \]
\[ V_P = 2.47 \text{ volts} \]
\[ y_P = 5.244 \text{ microns} \]
\[ I_D = 14.093 \text{ microamps per } Z/L \]
\[ V_P S_P = 47.6 \]
\[ S_{y_0} = 47 \]
\[ V_{y_0} = 3.2 \]
\[ V_{Q_0} = 3.2 \]
\[ S_{y_0} = 44.9 \]
\[ S_{Q_0} = 2.9 \]

The lower junction is moved to 6.003 microns and the upper junction is at 4.547 microns. Again the sensitivities of the device parameters to \( y_0 \) are very large.

The above devices indicate some features of the double-diffused JFET structure. The pinch-off point for the first device is closer to the surface than that of the second device even though \( V_P \) is less. This indicates that there is more impurity compensation in the channel of the first device, which is necessary to achieve the \( g_m \) specified. As mentioned in Section 5.1, impurity compensation is not an efficient way to change layer conductance. The result is a top-gate diffusion which extends deep into the wafer causing an appreciable modification of the lower junction. Greater sensitivities of the first JFET parameters to the diffusion parameters also result.
Next, a shallower structure is considered for a JFET. The background is a 1.5 ohm-cm n-type epi-layer with a p-type Gaussian diffusion having a surface concentration of $5.7 \times 10^{18}$ cm$^{-3}$ and a characteristic length of 0.9185 microns. The unmodified lower-junction depth is 2.5043 microns and the substrate is again assumed to be far enough away to be ignored. The structure is a conventional n-p-n transistor without the emitter diffusion. The device-parameter specifications are a $g_m$ of $30 \pm 3.0 \times 10^{-6}$ mhos per unit $Z/L$ and $V_p = 2.4 \pm 0.24$ volts with $V_{GS} = 0$ volts.

After three iterations, the specified diffusion parameters are:

$$C_0 = 1.393 \times 10^{19} \text{ cm}^{-3}$$
$$y_0 = 0.810 \text{ microns}$$

The resulting device parameters for both gates tied together are:

$$g_m = 30.7 \times 10^{-6} \text{ mhos per } Z/L$$
$$V_p = 2.40 \text{ volts}$$
$$y_p = 2.023 \text{ microns}$$
$$I_D = 21.353 \text{ microamps per } Z/L$$
$$V_{P} = 60.4$$
$$S_{Y_0} = 8.2$$
The lower junction is moved to 2.435 microns and the upper junction is at 1.635 microns. Again the sensitivities are high, especially to \( y_0 \). This device has larger \( g_m \) and \( I_D \) for approximately the same \( V_P \) than the preceding device. The cause of this is the larger channel conductance due to the higher impurity concentration in the channel. The higher sensitivities result from the narrower channel. The three JFET designs each required approximately five seconds CPU time.

We now indicate the experimental confirmation of the results of the design process. The last JFET considered above is compared to a device having similar parameters and structure. The background profile is identical and the measured top-gate diffusion parameters are:

\[
C_0 = 4.8 \times 10^{20} \text{ cm}^{-3}
\]
\[
y_0 = 0.625 \text{ microns}
\]

The measured device characteristics are:

\[
g_m = 29.6 \times 10^{-6} \text{ mhos per Z/L}
\]
\[
V_P = 2.43 \text{ volts}
\]
\[
I_D = 37.037 \text{ microamps per Z/L}
\]
The lower junction is at 2.5 microns and the upper junction is at 1.8 microns.

Although the top-gate diffusion parameters of the design example differ from those above, there is a substantial correspondence between the device parameters. This results from the similar channel profile and dimensions. Since the junction positions and background profile are approximately equal, similar device parameters result. Thus we have some verification of the validity of the design process.
CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

In the previous chapters, the design process for integrated-circuit channel devices was presented. This process gives the coefficients of a Gaussian diffusion profile which forms the top gate in an already-existing background containing the rest of the structure. The values of the circuit parameters of the resulting device are within a specified tolerance of a set of parameter specifications. To accomplish this, the equations yielding the device parameters are solved for the integrated-circuit structure.

6.1 Summary

The main objectives of this investigation were to: (1) develop a design process for channel devices in integrated circuits, and (2) investigate the resulting device characteristics. These objectives were achieved.

In particular, the unique contributions of this study are:

1. A rapidly converging iterative design process yielding channel devices with satisfactory characteristics.
a. The solution of the equations describing the device parameters for the integrated-circuit structure.

b. The development of a simple and accurate representation of the net impurity profile.

c. The calculation of the sheet resistance for the various layers found in integrated circuits.

d. The computation of the reverse-biased junction characteristics for the different impurity profiles found in integrated circuits.

2. The examination of certain device characteristics.

a. Demonstration of the relative insensitivity of the pinch-resistor channel conductance to the top-gate diffusion parameters.

b. Demonstration of the extreme sensitivity of the JFET device parameters to the characteristic length, $y_0$, of the Gaussian top-gate diffusion, which occurs even though the top-gate metallurgical junction is relatively insensitive to $y_0$. This information can be used to direct the attention of fabrication personnel toward closely achieving the required value for $y_0$. 

6.2 Recommendations

Further work is indicated in the following areas.

1. The set of specifications should be extended to include parameters which are generally of secondary importance such as gate capacitance, gate leakage current, and junction breakdown voltage. If this is done, devices for special applications, where such parameters must be known, can also be designed.

2. The four-terminal structure should be considered so that closed-geometry configurations can be designed. This would provide even greater flexibility for the device designer since another device of known characteristics would be available.

3. Another interesting problem for study is the design of the diffusion to produce both a channel device and another device of usable quality. Such a device pair is the JFET and "super-β" n-p-n transistor. This requires a design process which includes the n-p-n transistor parameters as well as the JFET parameters. Also, a system for assigning weights to the different parameters should be developed to make the necessary compromises.
LIST OF REFERENCES


