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SYSTEM DESIGN AND DEMONSTRATION

OF A CCD BASED

SOLAR SPECTRORADIOMETER

by

David Alphonse Zielinskie

A Dissertation Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

In Partial Fulfillment of the Requirements
For the Degree of

DOCTOR OF PHILOSOPHY

In the Graduate College

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and recommend that it be accepted as fulfilling the dissertation requirement for the Degree of DOCTOR OF PHILOSOPHY

JOHN A. REAGAN, PH.D. — Date 12/3/01

JO DALE CAROTHERS, PH.D. — Date 12/4/01

EUSTANCE L. DERENIAK, PH.D. — Date 12/3/01

ROBERT A. SCHOWENGERDT, PH.D. — Date

Date 12/3/01

Final approval and acceptance of this dissertation is contingent upon the candidate's submission of the final copy of the dissertation to the Graduate College.

I hereby certify that I have read this dissertation prepared under my direction and recommend that it be accepted as fulfilling the dissertation requirement.

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I would like to thank Professor John Reagan for his continued support throughout my graduate tenure. He encouraged me to do my best during my Masters program and to work even harder during the PhD program. I am fortunate to have been given the opportunity to work on such an interesting project.

To my parents

and

friends

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ABSTRACT

The Atmospheric Remote Sensing Lab at the University of Arizona's Electrical and Computer Engineering Department has been involved with the study and measurement of atmospheric gases and aerosols for many years. The research has been conducted using instruments designed and constructed by the lab. This dissertation presents a system design for the next step in the evolution of spectroradiometers designed by the Atmospheric Remote Sensing Lab. The design draws upon the lessons learned from previous generations of radiometers and from the requirements of ongoing research.

The proposed spectroradiometer uses an inexpensive CCD as the detector and takes advantage of modern processors and re-programmable CPLDs. The new design employs an embedded DSP in a novel way; it provides high level control over the CCD detector, receives serial ADC data and communicates with a Host computer. Through the use of one of the serial channels, the DSP identifies when to accumulate charge in the CCD and when to dump it. This controlled sampling allows charge to accumulate from adjacent cells internal to the CCD, improving the SNR in regions of poor spectral transmission. Since the charge accumulate/reset is controlled by the DSP through software, the sequence is programmable using the host computer interface and can be dynamically re-programmed to accommodate changing atmospheric conditions.

A re-programmable CPLD isolates the DSP from the detector hardware and provides low level control of the detector assembly. The CPLD accepts high level commands from the DSP and generates the low level clocks and control signals used by

the CCD and ADC. This capability permits the CPLD to be re-programmed to accommodate various CCDs and ADCs available today and in the future without altering the Host communication, control or analysis software.

The capabilities of the instrument can be altered by downloading new software to the embedded DSP. Provisions have been made to download software or configuration data to the instrument and execute from RAM. Once correct operation of the software has been verified, it can copied to non-voltile memory.

CHAPTER 1

INTRODUCTION

1.1 Overview

The Atmospheric Remote Sensing Lab at the University of Arizona's Electrical and Computer Engineering Department has been involved with the study and measurement of atmospheric gases and aerosols for many years. The research has been conducted using instruments designed and constructed by the lab [1-7]. This dissertation presents a system design for the next step in the evolution of spectroradiometers designed by the Atmospheric Remote Sensing lab. The design draws upon the lessons learned from previous generations of radiometers and from the requirements of ongoing research. The type of solar spectroradiometers of interest measure the attenuation caused by the various gasses and aerosols on sunlight as the light passes through the atmosphere. The measurements taken are used in retrieving the total optical depths at discrete wavelengths.

The atmosphere is comprised of several gasses and minute suspended particles, generally referred to as atmospheric particulates or aerosol particulates. The aerosols are typically dust, pollen and pollution ranging in size between 0.01 micron to several

microns. They are substantially larger than gasses, but both the gasses and aerosols attenuate the incoming radiation from the sun as it passes through the atmosphere.

Sunlight is comprised of radiation of many frequencies or wavelengths. The difference in the solar flux measured at the top of the atmosphere and on the surface is due to the absorption and or scattering by the gasses and aerosols in the atmosphere. The solar spectroradiometers described in this dissertation restrict the range of measurements primarily to the region around the visible spectrum of light, including parts of the near infrared and ultraviolet. The contribution of attenuation or extinction due to gases or aerosols varies depending on wavelength; the visible, infrared and ultraviolet spectrums can be thought of as "distinct" zones. Molecular and aerosol scattering predominates in the visible spectrum, while gaseous absorption dominates in the ultraviolet (ozone) and infrared (water vapor and carbon dioxide) regions.

Computer programs have been developed to model the spectral transmittance of the atmosphere and one such program is Lowtran [8]. An example of a Lowtran model run of total atmospheric transmittance versus wavelength is shown in Figure 1.1. Lowtran also allows plotting of various constituent transmittances such as ozone, Figure 1.2 and Figure 1.3; molecular scattering, Figure 1.4; carbon dioxide, Figure 1.5; and water vapor, Figure 1.6.

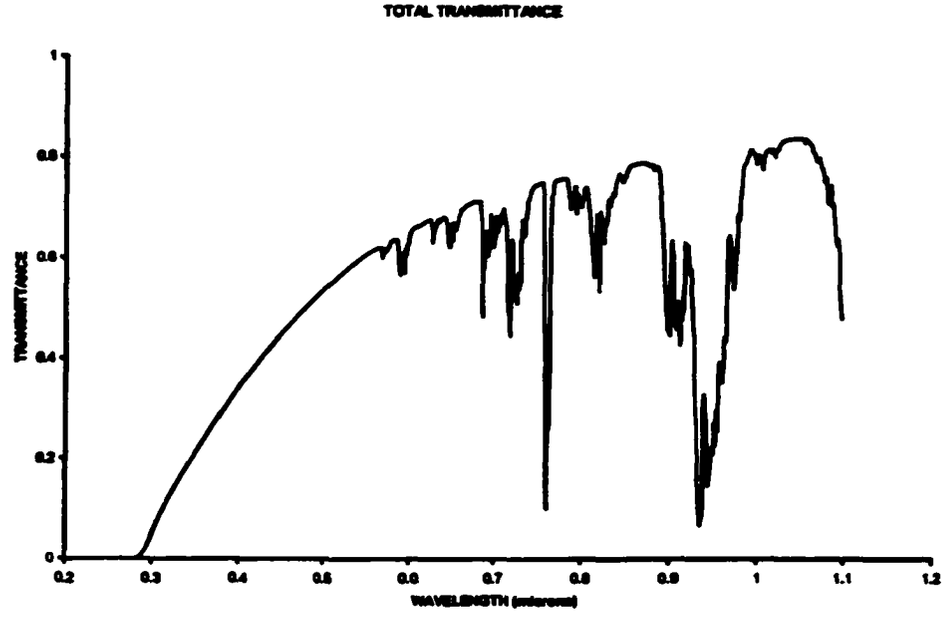


Figure 1.1 Total Atmospheric Transmittance

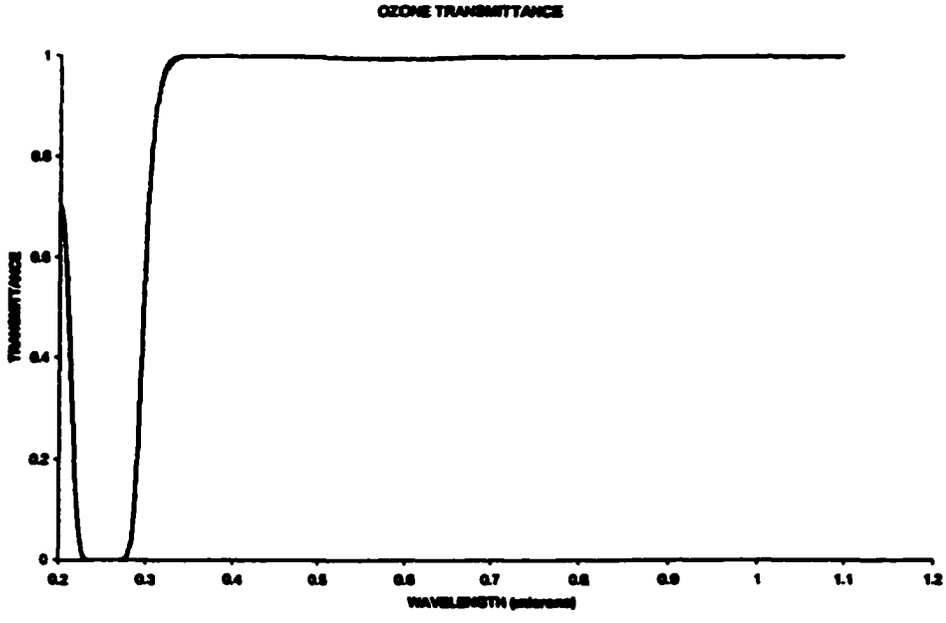


Figure 1.2 Ozone Transmittance

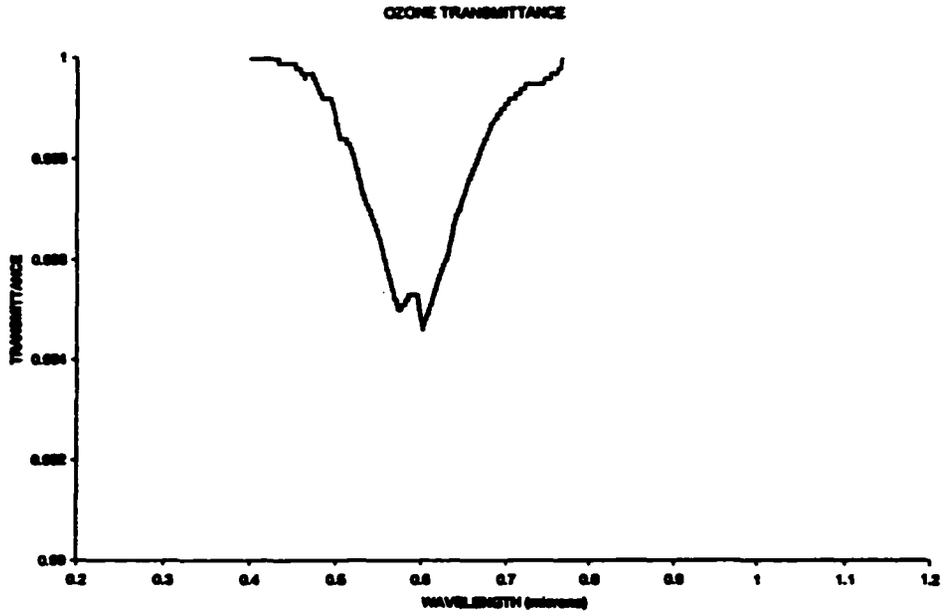


Figure 1.3 Ozone Transmittance, Enlarged

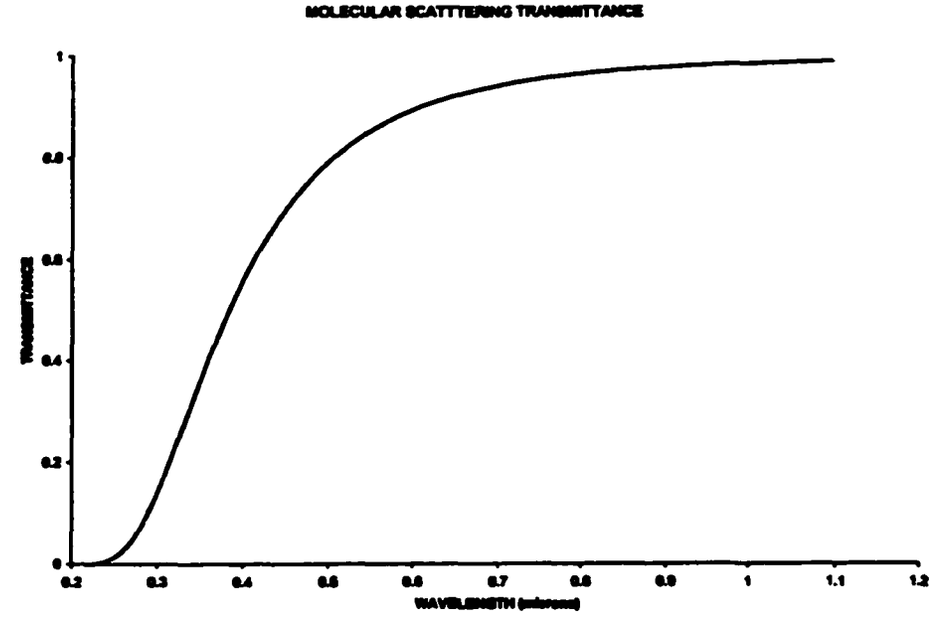


Figure 1.4 Molecular Scattering Transmittance

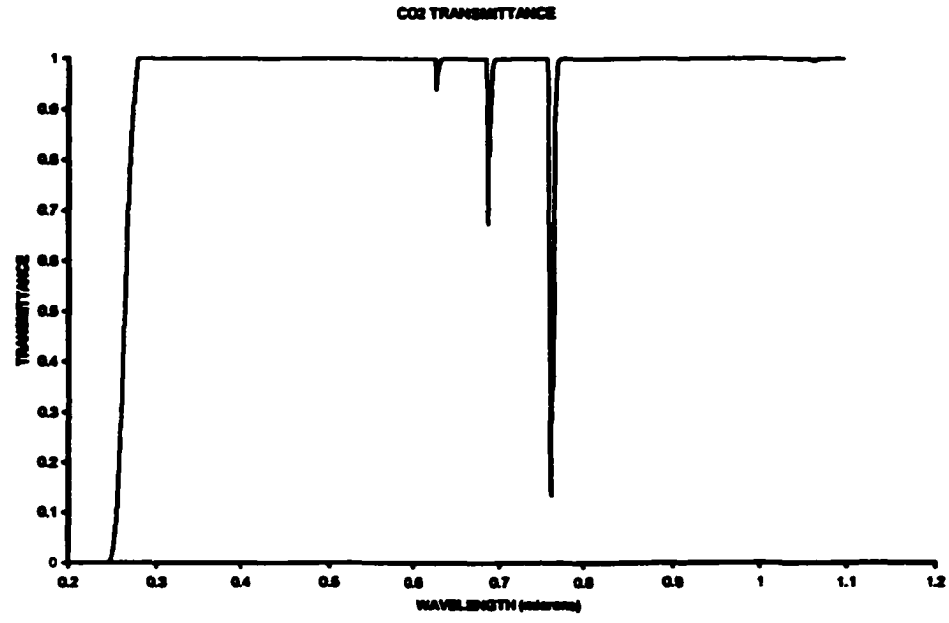


Figure 1.5 Carbon Dioxide Transmittance

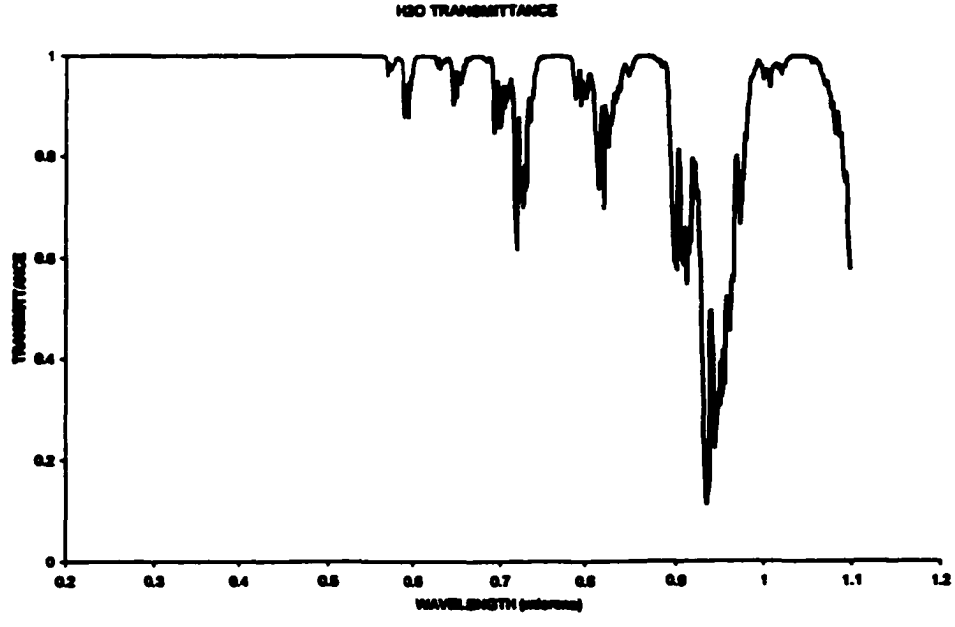


Figure 1.6 Water Vapor Transmittance

Programs such as Lowtran are useful simulation tools to study atmospheric transmittance, but have limitations that are based on our present understanding of the atmosphere. The solar spectroradiometer is one such instrument used to gather real atmospheric transmittance data.

The general makeup of a spectroradiometer system consists of a solar positioning/tracking subsystem, entrance optics, a wavelength selection device, a detector, an electronics measurement and signal conditioning subsystem and a host computer data storage subsystem as shown in Figure 1.7.

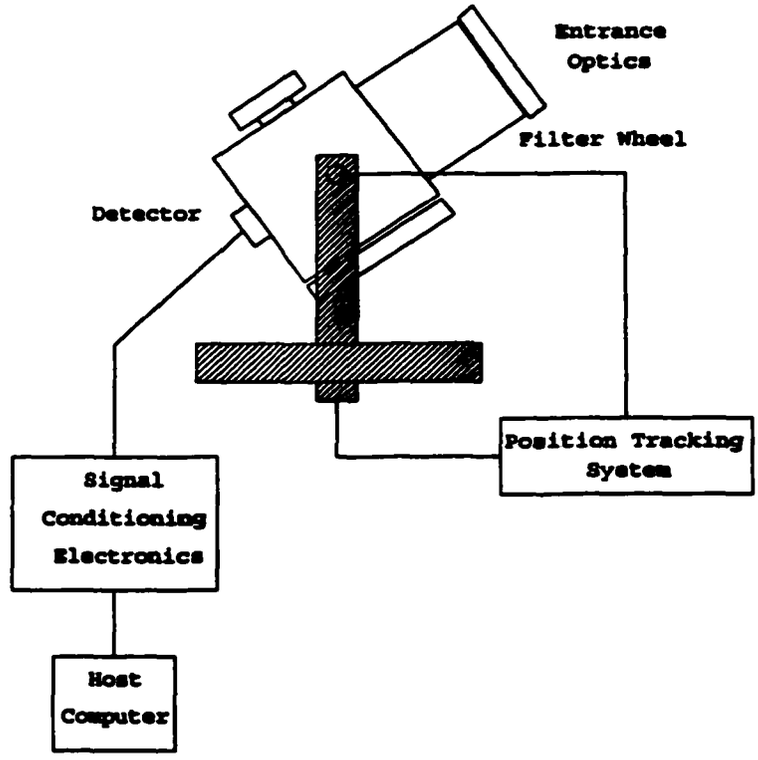


Figure 1.7 Spectroradiometer

The solar tracking system is required to keep the instrument's detector aligned with the energy source, the sun. The tracker can be either manually or automatically positioned. Measurements are taken repeatedly, at some selected rate, over the entire wavelength interval of the spectrometer throughout the day or over some specified period, such as two to three hours after sunrise or before sunset.

The entrance optics sets the field of view for the spectroradiometer and focus the incoming light. The light is then band-pass filtered, directing the desired wavelength(s) to the appropriate detector(s). The detector system converts the light to a voltage or current which is then digitized by the electronics subsystem. The electronics subsystem may perform additional processing on the data before it is finally sent to a host computer for storage.

One of the earlier radiometers employed at the University of Arizona used a filter wheel with ten positions for band-pass wavelength selection and a silicon detector. The filters were narrow band, approximately 10 nm band-pass, permitting effectively quasi-monochromatic measurements at the center wavelength of each filter. The unit operated by manually pointing the telescope towards the sun and rotating the filter wheel to the desired center wavelength. The signal from the detector was amplified and converted for manual recording. The data collected using this type of instrument was proven to be accurate; however, the collection process was tedious and time consuming.

An improved automated solar spectrometer was designed and constructed. The new ten-channel design was automatic featuring a sun-tracker, a motorized filter wheel

and an unattended data acquisition system (DAS). The sun-tracking system had a ±0.05° maximum tracking error. Ten parallel field of view telescopes, with individual interference filters, were pointed towards the sun where a silicon photodiode – op amp circuit converted and normalized the signal. The DAS would then record the data for later retrieval and data processing.

The automatic units are field portable and rugged. The units have the ability to operate unattended for several hours. The size and weight of the filter carousel imposed a limit on the number of channels that could be accommodated by the instrument; ten was found to be a reasonable compromise on the number of channels. To investigate transmittances at different wavelengths the filters in the carousel have to be changed.

These instruments provide quite adequate if the principal interest was to study aerosol spectral optical depth because it is fairly smoothly varying in wavelength, unlike gaseous absorption. A new radiometer design is required to study both aerosol extinction and gaseous absorption. The new design should provide quasi-continuous spectrum coverage from about 300 to 1100 nanometers, and the resolution should be sufficient to reasonably discriminate the spectral structure of significant gaseous absorption bands of the atmosphere.

Simulation results for atmospheric transmittance with a resolution of 100 nm is shown in Figure 1.8. The simulation assumed 100 nm bandwidth filters; hence, the fine detail is missing. By using three or four telescopes with narrow bandwidth filters about a specific spectral region, the detail could be improved to study a particular gaseous region.

Several instruments could then be used concurrently to collect data for a relatively detailed atmospheric study.

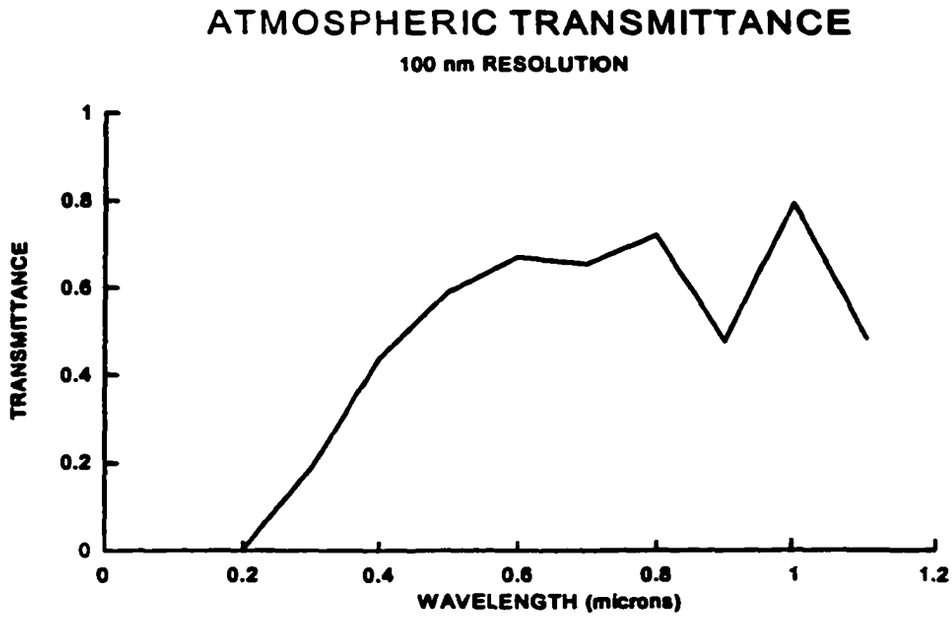


Figure 1.8 Atmospheric Transmittance, 100 nm Resolution

A cluster of spectroradiometers could be used to study select atmospheric transmittance lines shown in Figure 1.9. A more desired approach would be a new instrument that provides complete coverage over the extended visible spectrum, with ample spectral resolution to capture fine atmospheric details and to have sufficient temporal resolution to handle changing atmospheric conditions. The new instrument should also be low cost, rugged and field portable.

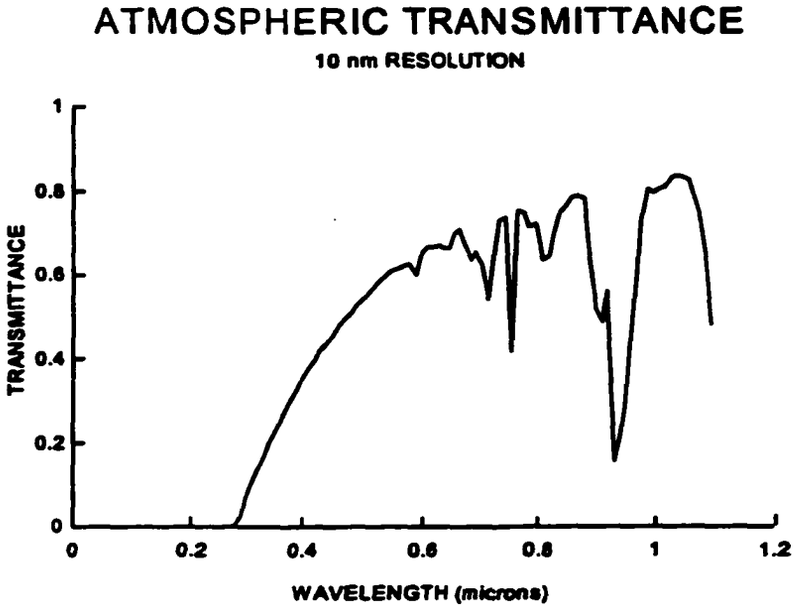


Figure 1.9 Atmospheric Transmittance, 10 nm Resolution

1.2 Objectives

The intent of this dissertation is to design and demonstrate a spectroradiometer that will meet the above mentioned goals. The new spectroradiometer will passively retrieve atmospheric transmittance over a wavelength interval of 300 to 1100 nanometers with a resolution on the order of a nanometer. A high level block diagram of the proposed spectroradiometer is shown in Figure 1.10.

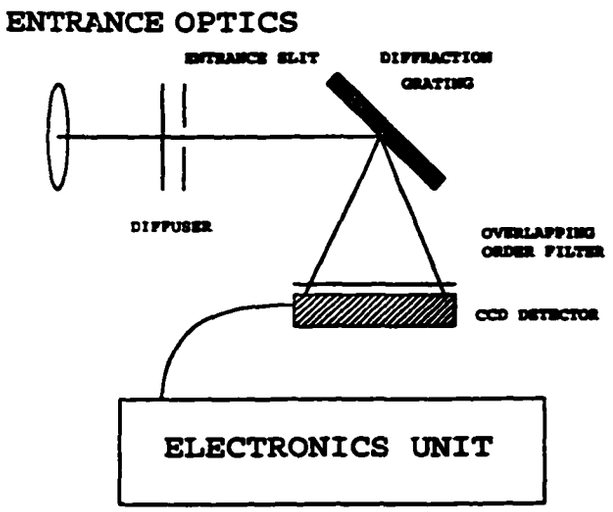


Figure 1.10 Proposed Spectroradiometer

Light enters the spectroradiometer and is focused on the diffuser/collimator before arriving at the entrance slit. The light then hits the dispersing element, a mirrored diffraction grating, where the light is diffracted and arrives focused and linearly separated on the face of the detector. Due to the dispersion caused by the grating and the entrance slit width, the light is distributed in approximately one-nanometer wavelength intervals across the linear array CCD detector. The light is converted by the CCD detector to a voltage, which is then read out by the Electronics Unit. The Electronics Unit stores the data from the detector and may further process the data before transmitting it to a host computer.

The Electronics Unit (EU) controls the entire data sampling process. It generates the clocks for the CCD detector and the analog-to-digital conversion. The EU also

communicates with the sun-tracker to insure that there is no movement during the integration time of the CCD.

The clock generation scheme facilitated by the EU allows for a programmable pixel size, with 1 nanometer being the smallest theoretical increment; this may be viewed as a programmable band pass filter. The detector is a silicon charged coupled device, CCD, sampled using a sixteen bit analog to digital converter, ADC. The entire CCD is read out in approximately ten milliseconds. Multiple lines of data from the CCD may be averaged by the EU before being transmitted to the host computer.

1.3 Outline

The following chapters develop the proposed next generation solar spectroradiometer system in detail. The Chapter 2, System Design, presents the equations governing the retrieval of solar spectrometer data from the instrument. It also presents the design goals for the system. These goals are then used to define the optical and electrical system requirements.

Chapter 3 discusses a basic optical system that will bring light from the sun and direct it to the CCD detector. The optical system includes a single lens telescope, a diffuser, the entrance slit, and a commercial off-the-shelf spectrograph. Additionally, the non-electrical design issues of the CCD are presented, including temperature stabilization and/or monitoring of the detector.

The electrical system is the core focus of the dissertation and the requirements are divided into a hardware and a software chapter. Chapter 4 Hardware Design discusses the partitioning of the two electrical subsystems, the detector/data conversion electronics and the control electronics. It elaborates on the component selection used to meet the system design requirements. The architecture of the ADSP2101 digital signal processor and the application specific integrated circuits, ASICs, are presented. Timing diagrams for the operation of the external data bus, CCD clock generation, and ADC control are cited. The electrical parameters of the CCD are treated. A complete electrical schematic is included in the appendices.

Chapter 5 Software Design discusses the data capture and system control routines used in the spectrometer. This chapter also defines the software and basic hardware requirements for the host computer. The data formats used by the spectrometer are described. The system control and calibration menus are presented and discussed. Typical host application software for communicating with the spectrometer and for analyzing data is presented.

Chapter 6 Operations discusses the basic operations of the instrument. Chapter 7 Calibration describes the various methods used to insure the validity of the measurements made using the spectrometer. The calibration methods describe the use of both lab instruments and atmospheric measurements to calibrate the spectrometer.

Chapter 8 discusses possible improvements for this instrument and for construction of future generations of instruments.

CHAPTER 2

SYSTEM DESIGN

The spectroradiometer is used to gather data on the concentration and type of matter that resides in the column of air bounded by the top of the atmosphere and the Earth's surface. More precisely, the detection region of the instrument consists of the area observed by the optical front end and then imaged on the detector where the photons are converted to electrons and a voltage is finally measured. The spectral resolution of the instrument is determined by the entrance slit width, the choice of diffraction grating and the type of detector. There are other system limitations that affect the signal conversion process such as ADC quantization, temperature effects and system noise. The objective of the system design is to take account of these physical realities and define the boundaries over which the instrument operates with a known accuracy. The emphasis of this dissertation is primarily on the electronic design of the spectroradiometer, however the other system elements shall be presented in sufficient detail to define their constraints and allow the construction of a real instrument.

2.1 Solar Input

The spectroradiometer essentially measures the irradiance incident on the detector. The Bouguer-Lambert Law models the conversion process and is expressed by

$$F_\lambda(\theta) = \left(\frac{Rm}{R}\right)^2 F_{0\lambda} e^{-m(\theta)\tau_\lambda}$$

and

$$F_\lambda(\theta) = F'_{0\lambda} e^{-m(\theta)\tau_\lambda}$$

where,

R_m is the mean Earth-Sun separation,

R is the Earth-Sun separation at the time of the observation,

$m(\theta)$ is the relative airmass at the solar angle θ,

τ_λ is the total optical depth at wavelength λ,

$F_\lambda(\theta)$ is the spectral irradiance on the surface,

$F_{0\lambda}$ is the zero airmass solar spectral irradiance,

$F'_{0\lambda}$ is defined as $\left(\frac{R_m}{R}\right)^2 F_{0\lambda}$.

The above expression relates the spectral irradiance on the surface of the detector to the unattenuated spectral irradiance at the top of the atmosphere. The spectral irradiance is a measure of flux density on a surface; it is the amount of radiant flux at a surface divided by the surface area. The reference to spectral implies a bandwidth for the particular wavelength measured and as the bandwidth approaches zero the light becomes monochromatic [9].

The ratio of the mean Earth-Sun separation to the separation at the time of the measurement is required to account for the drop-off of solar irriadance striking the Earth due to the elliptical shape of it's orbit around the Sun. This value is found using data tables and requires only the date of the measurement.

The airmass is the relative increase of the path length as compared to the zenith path length. The airmass may be approximated by the secant of the zenith angle for angles less than sixty degrees. In practice the airmass is determined using an airmass model. Kasten's Model [10] is an example of an airmass model. It accounts for the path length difference by including such factors as the spherical geometry of the atmosphere as well as refraction effects.

The optical depth is the parameter that accounts for the attenuation of light as it passes through the atmosphere. The total optical depth is comprised of several components, expressed by

$$\tau_\lambda = \tau_{Rayleigh} + \tau_{aerosol} + \tau_{gaseous}.$$

The Rayleigh component of optical depth is the result of molecular scattering, it is dominant at shorter wavelengths and varies as a function of $1/\lambda^4$. The aerosol optical depth results from particulates in the atmosphere such as smoke, dust and pollen. Gaseous optical depth accounts for the absorption by gasses at different wavelengths. The gasses of interest for this particular instrument are water vapor and ozone.

2.2 Solar Tracker

The solar tracker moves the instrument to keep the entrance optics aligned with the sun. The tracker employs azimuth and elevation stepper motors. The optics are designed such that the sun will over fill the entrance optics allowing a ±0.05° maximum tracking error.

The Tracker will coordinate movement with the EU so that the platform will remain stationary during data capture. The interface between the Tracker and the EU consists of two signals, MOVEMENT_REQUEST and MOVEMENT_ALLOWED. The Tracker requests permission to move by asserting MOVEMENT_REQUEST. The EU asserts MOVEMENT_ALLOWED to acknowledge the request and identify that data capture is complete. The Tracker de-asserts MOVEMENT_REQUEST when the platform has finished moving. The EU de-asserts MOVEMENT_ALLOWED and resumes the data capture.

2.3 Optical Subsystem

The optical subsystem brings the light into the instrument and eventually onto the detector where it is readout. The subsystem is made up of the lens, the diffuser, the entrance slit, the grating spectrometer, the higher order optical filter and CCD detector, Figure 2.1. The optical subsystem must operate over the extended visible spectrum of 300 to 1100 nm and be able to provide a desired spectral resolution of approximately 1 nm.

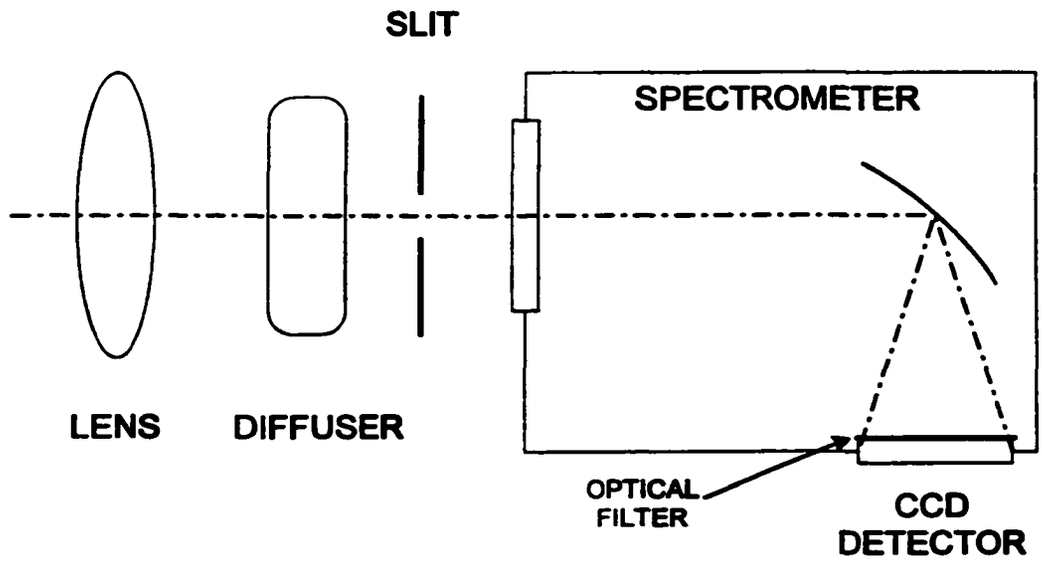


Figure 2.1 Optical Subsystem Diagram

The selection of the detector constrains most of the system parameters for the spectroradiometer. The detector chosen was the TH7811(Z) CCD from Thompson-CSF[11]. It operates over a spectral range of 300 to 1100 nanometers and has 1728 useful cells with 26 reference cells. The device has a guaranteed dynamic range of 3000:1 and a typical dynamic range of 6000:1. The pixel size is 13 by 13 microns. The maximum data transfer clock frequency is 2 MHz and has a maximum output voltage of 11 volts.

The TH7811 CCD has a feature allowing external control over resetting the readout stage. This feature allows the accumulation of charge in the readout stage as adjacent cells are shifted into the readout stage. The spectral range requirement is for 800 pixels with one nanometer resolution. By averaging adjacent cells the TH7811 will provide 1728 / 2 or 864 pixels. This 864 effective maximum number of pixels

corresponds well with the required number of 800 pixels. The 64 additional pixels will be used to accommodate inaccuracies in placement of the CCD in the dispersal beam from the spectrograph and are accounted for in the calibration of the instrument.

Control over the reset of the read-out stage by the EU through software provides for additional capabilities. These capabilities include programmable pixel size, where a pixel is some number of adjacent CCD cells; non-uniform pixel size, each individual pixel can be defined as an arbitrary number of adjacent CCD sells; and dynamically configurable pixel size, where the host computer can re-define the pixel to CCD cell mapping at will.

2.4 CCD Detector

The spectroradiometer being defined here does not directly measure the spectral irradiance on the surface. The detector, a Charged Coupled Device, converts the energy of the photons striking each cell to a charge that is accumulated over a finite time. When the CCD is read, the quantity measured is voltage and this voltage is proportional to the light or flux density on the detector.

The CCD image sensor is an analog integrated circuit that converts light to voltage. CCDs are small, rugged devises that are comprised of a large number of consecutive photosensitive cells or pixels. Their characteristics include an unlimited operating life, low power consumption, and immunity to image burn-in. The pixels have exact field registration and the output signal is low impedance.

The CCD image sensor's light-to-voltage conversion process can be broken down into the conversion phase and the read-out phase. The conversion phase begins with an exposure period. During the exposure period the CCD converts the light incident on the linear array to a proportional quantity of electrical charge, photocharge, for each pixel. It then stores the photocharge from each pixel to an associated MOS capacitor.

The readout phase sequentially shifts the accumulated charge from each MOS capacitor to the readout stage of the CCD. The readout stage converts the stored charge to a proportional voltage where it can be measured.

The conversion of photons to a measured voltage is not perfect. There are error sources that affect the conversion accuracy which include spectral response, charge transfer efficiency, noise sources, and others. These sources of errors will be addressed in the Optics Chapter.

2.5 The Electrical System

The Electrical System primary objective is to measure the voltage at the readout stage of the CCD. The data is processed and then transferred to the Host computer. The Electrical System is divided into two subsystems, the Detector Electronics Board and the Electronics Unit, Figure 2.2. The Detector Electronics Board consists of the CCD detector and the Analog-to-Digital Converter, ADC. The Electronics Unit contains the processor, clock generation circuitry for the CCD and ADC, the voltage reference for the ADC, and the UART for communication with the Host computer.

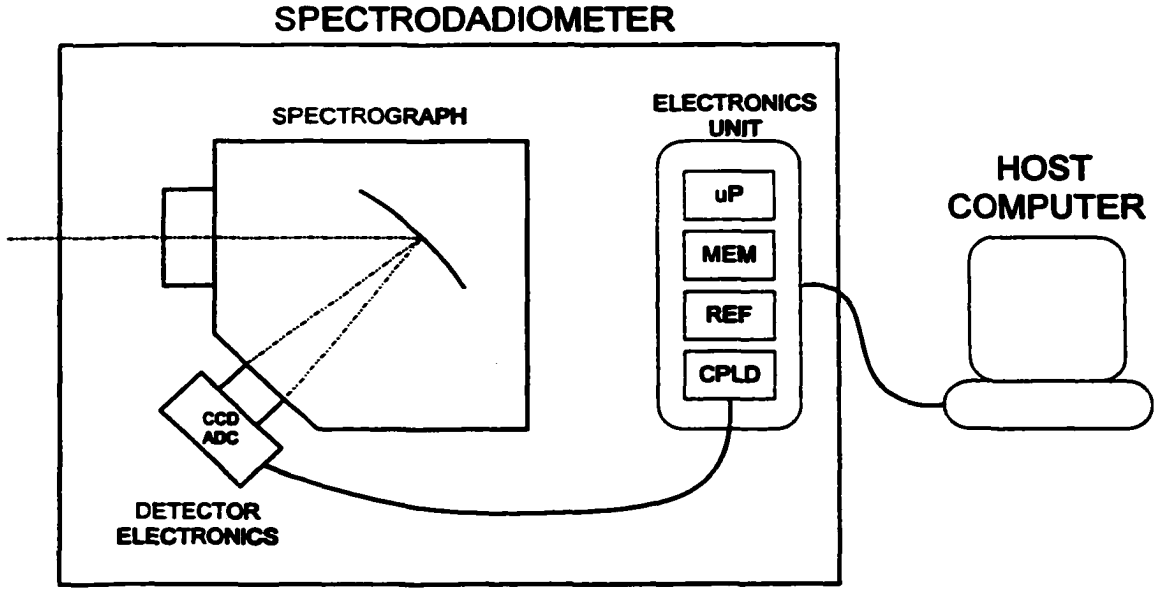


Figure 2.2 System Block Diagram

The Electronics Unit orchestrates the data collection process. It transfers data to the host computer, enables and disables tracker movement, and controls the Detector Electronics board. The interface between the EU and the Detector boards is comprised of the digitized pixel data, clocks for the detector and ADC, the ADC reference voltage and the analog power forms. The analog output from the CCD is sampled and converted by the ADC. The ADC is a serial device and requires a clock and a sample signal from the EU. It provides serial data and a conversion complete signal to the EU. The EU provides three clock signals, Q_P, Q_T and Q_{REXT}, to the CCD that control integration time, charge transfer and charge dump. The reference voltage provided is used by the ADC. Each of these signals will be fully defined in the Hardware Chapter. The interface between the Detector Electronics Board and the Electronics Unit is shown in Figure 2.3.

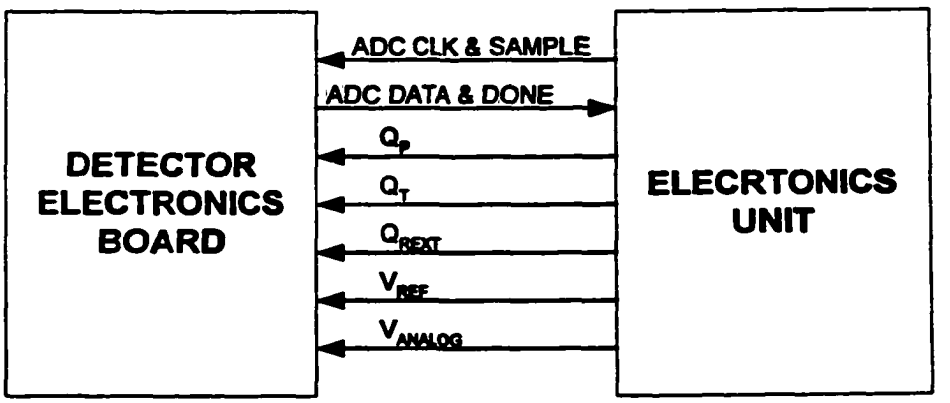


Figure 2.3 Electronics Interface Drawing

2.5.1 Detector Board

The Detector Electronics Board contains the CCD detector and the ADC. These two components are mounted on the same board to minimize noise pick up in the analog video signal of the CCD. The ADC provides a serial data output for the converted signal and a conversion complete signal. All clock signals are generated on the EU board and are synchronous to the master clock.

The choice of the ADC is based on the requirements that the CCD has a typical dynamic range of 6000:1 and the system design requires a set of data every second. The ADC therefore must have at least 13 bits of resolution and have a conversion rate on the order of 100,000 samples per second. This sample rate allows data sets to be averaged, increasing the SNR level of the resultant averaged data set.

The AD1876 ADC from Analog Devices was chosen to sample and convert the output from the CCD detector. It is a 16-bit 100 thousand sample per second converter with a built in sample and hold amplifier. An external voltage reference is required for

the desired conversion accuracy. The voltage reference for the ADC must be able to provide 14 bits of resolution to guarantee ADC conversion accuracy. It must also be stable over the temperature and voltage levels encountered by the system.

2.5.2 Electronics Unit

The EU provides a virtual interface between the CCD detector and the host computer. It controls the timing and operation of the various components and ultimately sends the voltage read from the CCD to the host computer.

The processor chosen for the spectroradiometer system must possess the throughput to accept data from the ADC at a rate of 100,000 sixteen bit words per second, be able to generate clocks to the CCD, perform data averaging and communicate with the host computer. It must be able to address a minimum of 4000 words of data memory which will be comprised of 877 thirty-two bit words of data, 55 sixteen bit words for the CCD pixel map table, and additional space for program variables and data buffers.

The ADSP 2101 digital signal processor from Analog Devices fulfills the above mentioned requirements. It has a throughput of 12 million operations per second when operated with a 12-MHz clock, can generate two independent clock sources for serial transfers and addresses up to 16 thousand words of separate program memory and data memory.

The host computer and spectrometer communicate with each other using an RS-232 serial interface. The host computer primarily accepts data from the spectrometer and stores the data to a file for later analysis. The electronics unit must be able to send

the data to the host before performing another data capture. The data sent to the host will be 16-bit hexadecimal numbers stored as 4 ASCII digits separated by commas. The data set size is variable with a maximum set size of 877 pixels. The total number of bytes sent to the host computer would be 877 bytes x 5 or 4385 bytes. The word size of the UART is 10 bits per word, which includes one start and stop bit. A rate of 38400 baud will be required to transfer the data from the EU to the host computer in approximately one second.

The host computer also uses the RS-232 serial channel to control and reconfigure the spectroradiometer. A menu driven scheme provided by the EU guides the host computer operator through the various control and configuration options. This menu scheme allows wide selection over the choice of host computer. The host computer requirements are that it can communicate using the ASCII character set over a standard RS-232 serial data link.

2.5.3 System Timing

The system timing is derived from a single twelve-megahertz clock, the system clock, on the Electronics Unit. Using one clock provides a number of useful properties that can be exploited. The main advantage is in noise reduction; using one clock frequency eliminates unwanted beat frequencies. Another advantage is the ability to sample the detector synchronously. This allows the choice of when the ADC is sampled and the data converted. The video signal can be precisely sampled at the same time for

each pixel. At worst this allows averaging out the background system noise and at best it permits sampling when the system is 'quiet'.

The system clock is generated by the ADSP 2101 signal processor from a twelve megahertz crystal on the Electronics Unit. Several clocks are used in the system, with each derived from the twelve megahertz crystal. Clocks are required by the Universal Asynchronous Receiver Transmitter (UART) and the Programmable Logic Device (PLD). The PLD generates additional clocks, based upon the system clock, for the CCD and the Analog to Digital Converter (ADC). Figure 2.4 shows the clock scheme used in this design.

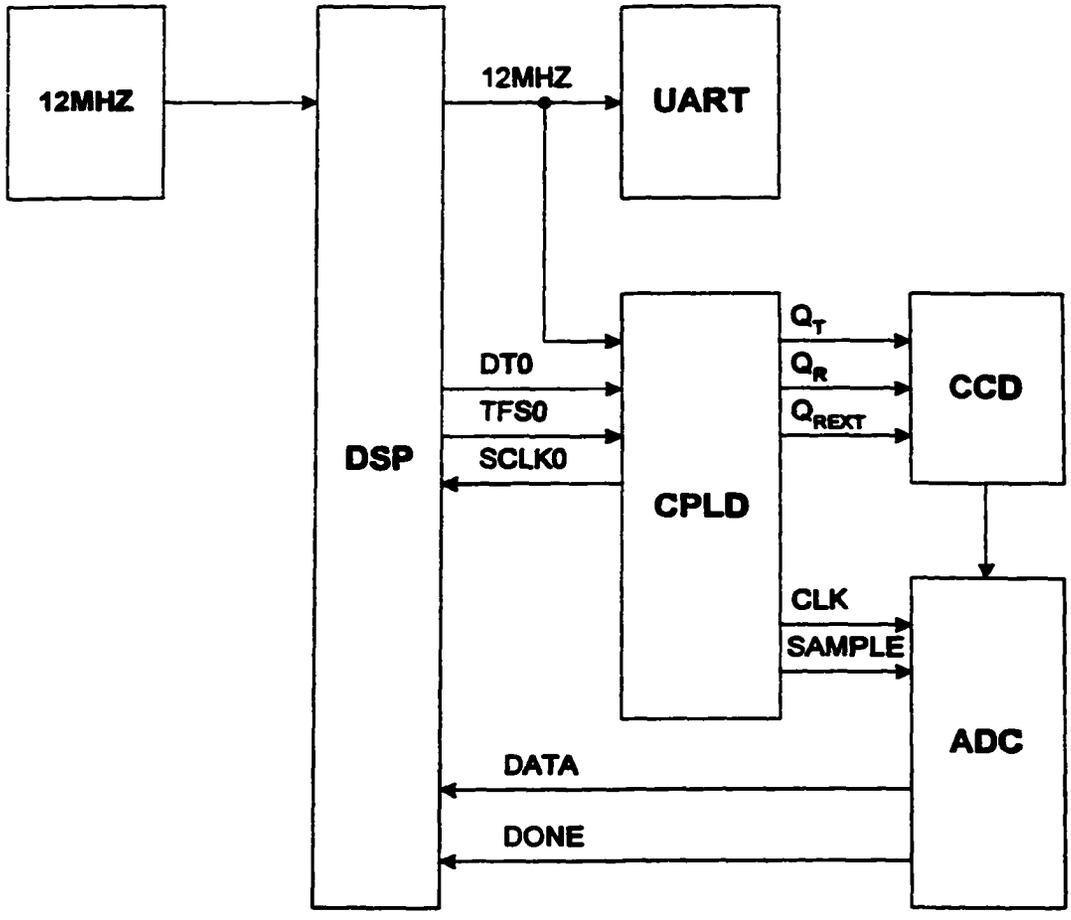


Figure 2.4 System Clock Diagram

The CCD transport clock, Q_T is not directly generated by the processor. The CPLD takes the 12 MHz processor clock and divides it down producing a CCD clock with a frequency of 93.75 KHz. A cell from the CCD is available during both halves of the transport clock. In this work, the smallest pixel will be defined as two CCD cells.

The transport clock is further divided down in the CPLD to allow precise placement of the CCD charge dump signal, Q_{REXT} , and the ADC sample signal. The Timing Diagram for the charge dump and video sampling is presented in Figure 2.5.

Controlling Q_{REXT} through the processors serial port (SPORT) allows programmable control over when the stored charge in the CCD is dumped; i.e., control over the number of adjacent charge cells that are internally averaged to form an output pixel. Areas of poor signal can average several cells internal to the CCD before being sampled by the ADC. This parameter can be optimized depending upon the type of investigation that is being performed.

The simplest type of averaging combines pixels in groups of two, three, four, etc., to improve the signal-to-noise ratio. A more complex form of pixel averaging can be performed by storing the charge dump/reset sequence as a table in data memory and then sending it out the serial port of the ADSP 2101. This allows programmable averaging of any combination of adjacent CCD cells prior to ADC conversion.

The clock frequency for the ADC is 2 MHz and it allows ample time to convert the data from the CCD detector and to serially transfer it to the processor. The ADC clock is gated so that when the ADC is sampling the CCD's output the clock is off.

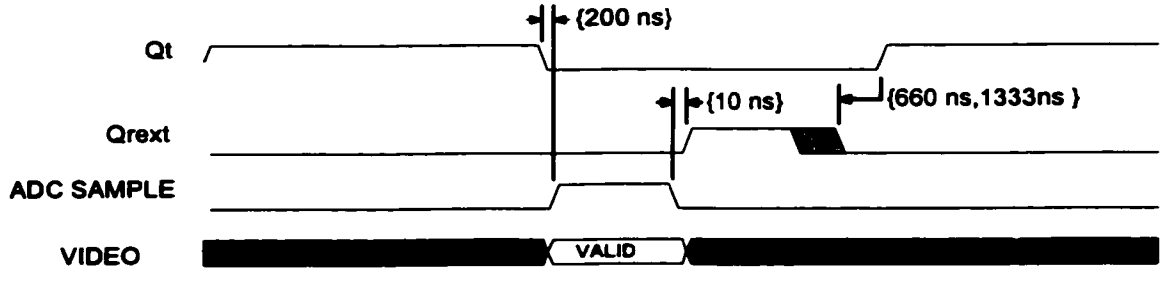


Figure 2.5 Clock Generation Timing Diagram

The Optics, Hardware and Software chapters will expand the topics introduced in this chapter. The details on operating and maintaining the instrument will be presented in the Operations Chapter. Instrument calibration will be presented in the Calibration Chapter.

CHAPTER 3

OPTICAL DESIGN

The purpose of the optical system is to convey the solar flux onto the detector. The energy source, the sun, is not perfect and it will be briefly discussed prior to describing the optical system. The sun is of interest because it is the primary source of energy available for use by passive instruments such as the spectroradiometer design being described in this dissertation. The sun is not a perfect source and these abnormalities must be taken into account when designing a passive instrument.

The distance between the sun and the earth is not a constant. The average distance from the sun to the earth is 1.3914 million kilometers or one astronomical unit (1 AU). This distance varies throughout the year from 0.983 AU to 1.0167 AU. The average angular subtense of the sun when viewed from the earth is 9.3 milliradians.

The radiant spectral flux output from the sun approximates that of an equivalent 6000-K black body source, at visible and near-visible wavelengths. The sun is not a perfect blackbody radiator, and there are several model sources of the sun. Figure 3.1 shows a representative model of the sun based on solar spectral measurements by Neckel[12]. The Labs and Neckel model contains detail not in an ideal blackbody curve, because it is based on actual solar spectral measurements. In addition, the sun is not

uniformly illuminated across its disk, which is why the optics are designed to illuminate the grating entrance slit with light representative of the full solar disk, diffused so as to not be imaging any disk inhomogenities.

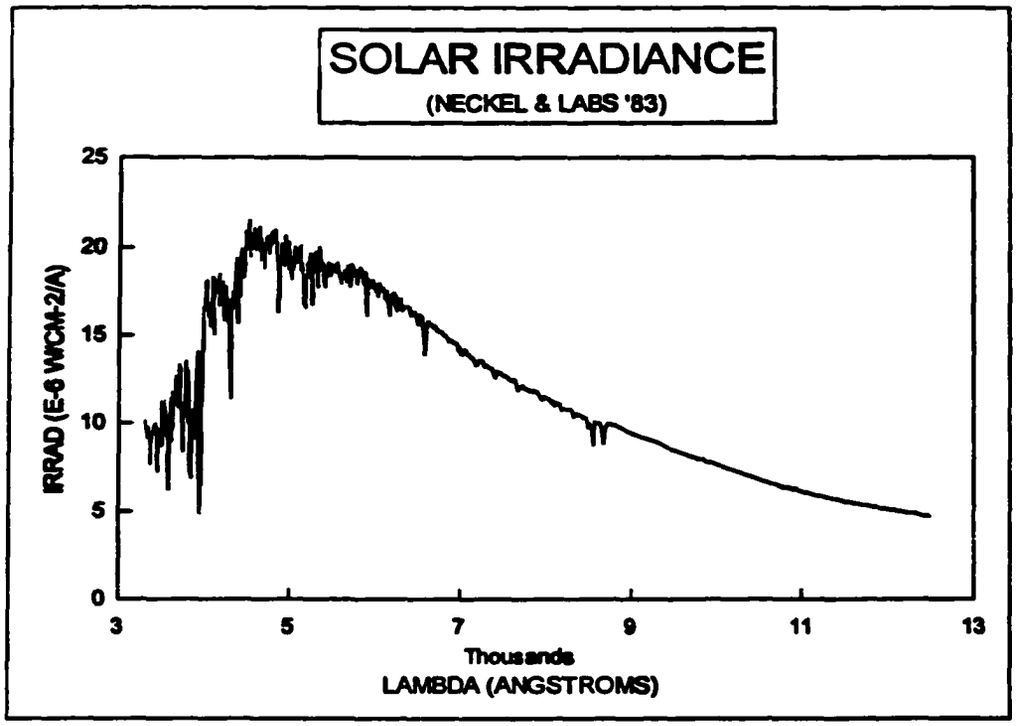


Figure 3.1 Solar Blackody Model

3.1 The Spectrometer Subsystem

The optics subsystem serves to convey the sun onto the detector and to establish the optical resolution limits of the instrument. The optical system of the spectroradiometer consists of several elements. These elements are the lens, the diffuser, the entrance slit, the diffraction grating, multiple order optical filter and the detector. The block diagram of the optical system from Chapter 2 is repeated in Figure 3.2.

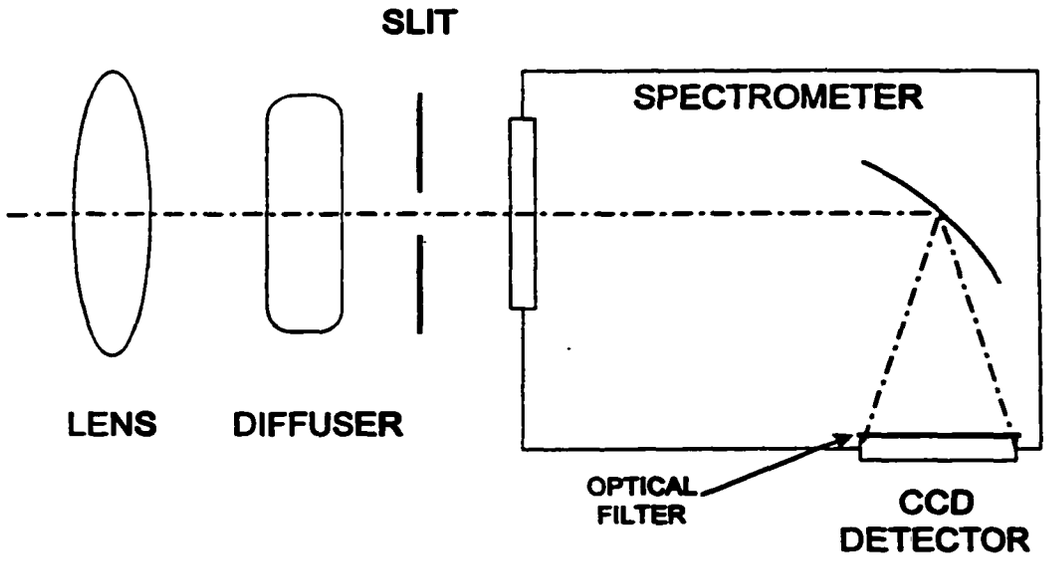


Figure 3.2 Optical System Block Diagram

An additional piece of hardware, a tracker, must be added to keep the spectroradiometer pointed at the sun. As the sun moves across the sky, the tracker must keep the entrance slit fully illuminated by the sun.

3.1.1 The Spectrometer

The spectrometer chosen for this design is a commercial spectrograph purchased from American Holographics of Littleton, Massachusetts. The choice of spectrograph was based on the availability of an inexpensive and standard model. The spectrometer is discussed first because it defines parameters for the remaining parts of the optical subsystem.

The spectrometer chosen from American Holographics is the model number 100S SPECTROGRAPH. The model 100S has been designed to operate over a wide variety of wavelength regions and primarily utilizes linear diode arrays as detectors. American Holographics offers an adapter kit that interfaces the model 100S to CCD type detectors like those used in this design.

The basic spectrograph instrument has a focal length of 0.1 meters. It uses a square concave holographic diffraction grating of 37 millimeters on a side with 27 different grating selections available which cover the visible and near infrared spectrum. The spectrograph has an effective F-number of F/2.5.

This design chose grating 446.50/L. It has an average dispersion of thirty-five nanometers per millimeter at the detector, has a central wavelength at six hundred thirty nanometers, and a wavelength range of one hundred ninety to one thousand sixty-five nanometers [13]. The dimensions of the model 100S spectrograph are shown in Figure 3.3.

The grating design defines the possible maximum resolution of the spectrograph. The theoretical first order spectral bandwidth due to the grating at 600 nm is 0.062 nm. This is a much higher resolution than attainable due to the choice of entrance slit width and will not place limitations on the system.

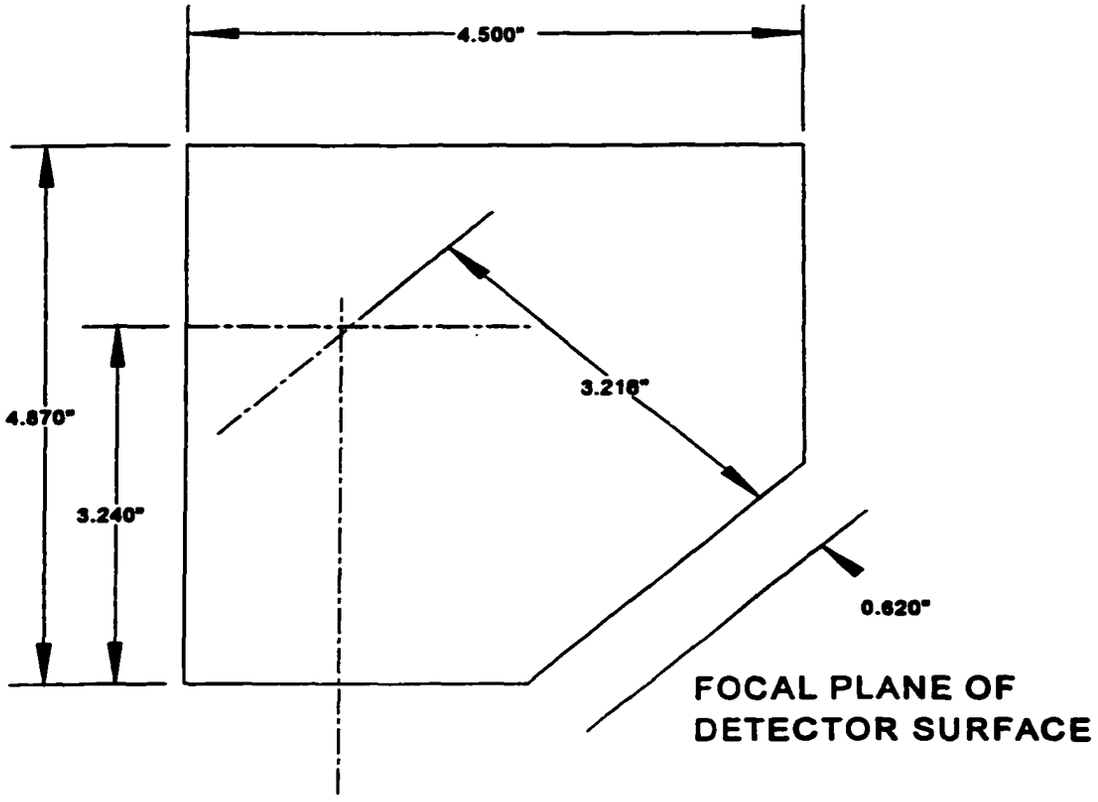


Figure 3.3 Spectrograph Dimensions

The use of a diffraction grating by the spectrometer reduces the optical transmission. The theoretical first-order grating efficiency, provided by the manufacturer, is plotted in Figure 3.4.

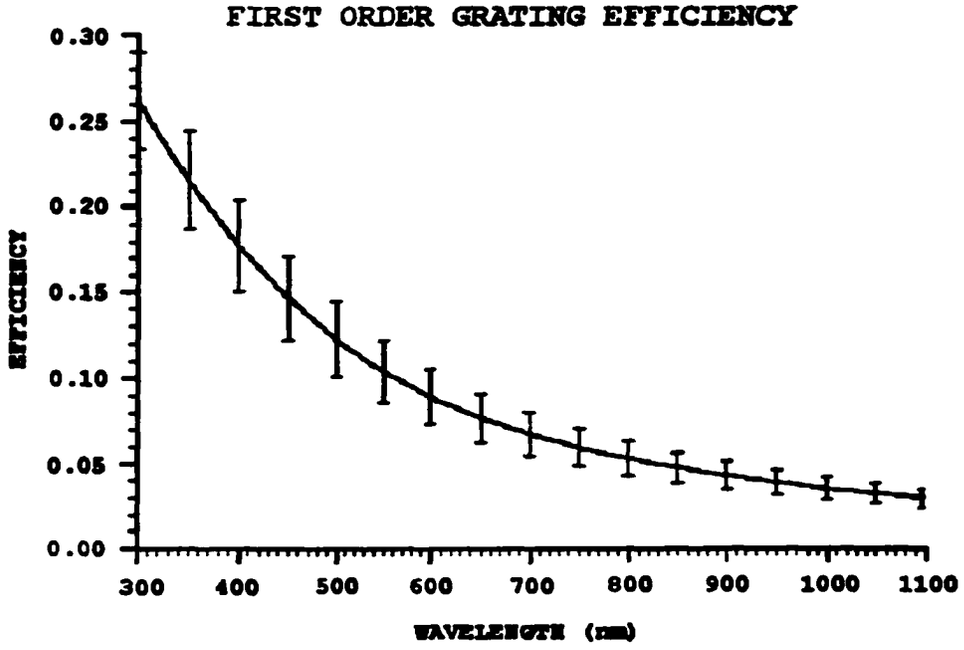


Figure 3.4 First Order Grating Efficiency

The choice of a diffraction grating causes the possibility of spectral overlap due to higher orders. The equation for diffraction is $m\lambda = d(\sin\alpha + \sin\beta)$. Here m is the grating order, λ the wavelength of the diffracted light, d the grating groove spacing, α the angle of incidence, and β the angle of diffraction. The diffracted order, m, always appears as a multiple of the diffracted wavelength [14]. It can be shown that conditions exist for spectral overlap between the first order with the second and third orders. The condition for overlap is $\rho_1\lambda_1 = \rho_2\lambda_2$.

The spectroradiometer wavelength range of interest is from 300 nm to 1100 nm. Spectral overlap occurs at 600 nm through 1100 nm and also at 300 nm through 600 nm.

For example, 900 nm light in the first order diffracts at the same angle as 450 nm light in the second order and as 300 nm light in the third order.

Longwave - sharpcut glass filters are used to eliminate second order and higher order effects. A filter stack is formed containing both the short and long wavelength filters. The longer wavelength filter acts as a high pass filter and is chosen to transmit light at 600 nm and higher. Schott color glass OG 570 has a 90 percent transmission above 600 nm and less than 10E-5 below 550 nm. Light, due to higher order effects, from 300 nm to 550 nm is blocked by this filter that otherwise would appear in the longer wavelength region of interest. The placement of the OG 570 filter is important and it must physically cover the detector starting at the 600 nm pixel and continue covering the detector's higher wavelength pixels.

The selection of the OG 570 glass filter dictated the choice of filter material for the shorter wavelengths. The short wavelength filter must have a high pass cutoff at 300 nm. Schott clear glass WG 320 transmits less than 10E-5 below 299 nm, 40 percent at 320 nm, and 90 percent at 350 nm and longer. This filter blocks the second order light that otherwise would be detected in the shorter wavelength region of the detector.

A third glass, Schott WG 295 is used to fill in the gap in the OG 570 filter layer, Figure 3.5. WG 295 transmits 60 percent at 300 nm and 90 percent at 345 nm and longer. The complete filter stack has a 90 percent transmission above 340 nm. The optical transmission curve for the fabricated filter stack is shown in Figure 3.6.

The filter stack will be bonded directly on the CCD detector and its exact placement is not critical. The glass filter seam where the two pieces come together cause a two nm loss of spectra. The exact position is determined during instrument calibration. Further discussions on placement and alignment will be addressed in the Calibration Chapter of this dissertation.

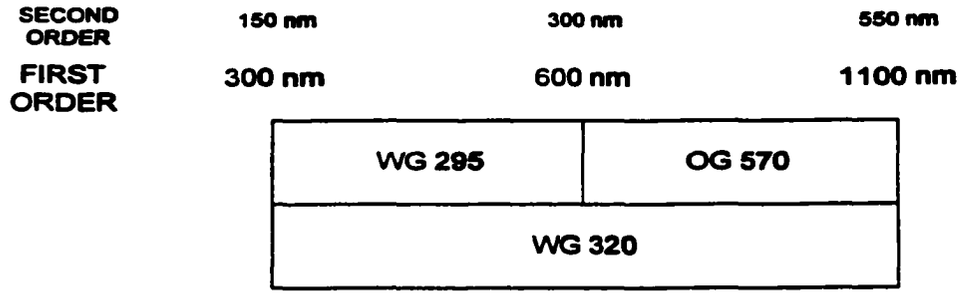


Figure 3.5 Filter Stack

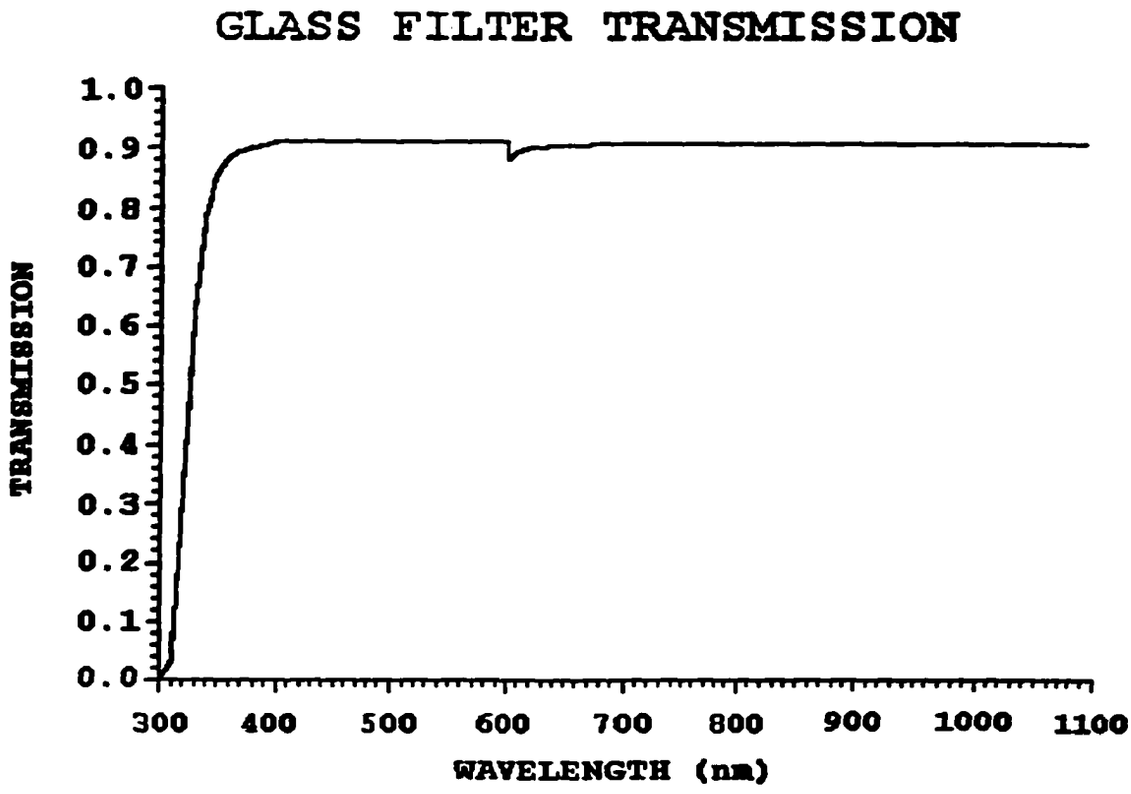


Figure 3.6 Glass Filter Transmission Curve

The total transmission through the spectrograph and filter stack is determined by multiplying the first order grating efficiency curve with the glass filter transmission curve. The results are plotted in Figure 3.7.

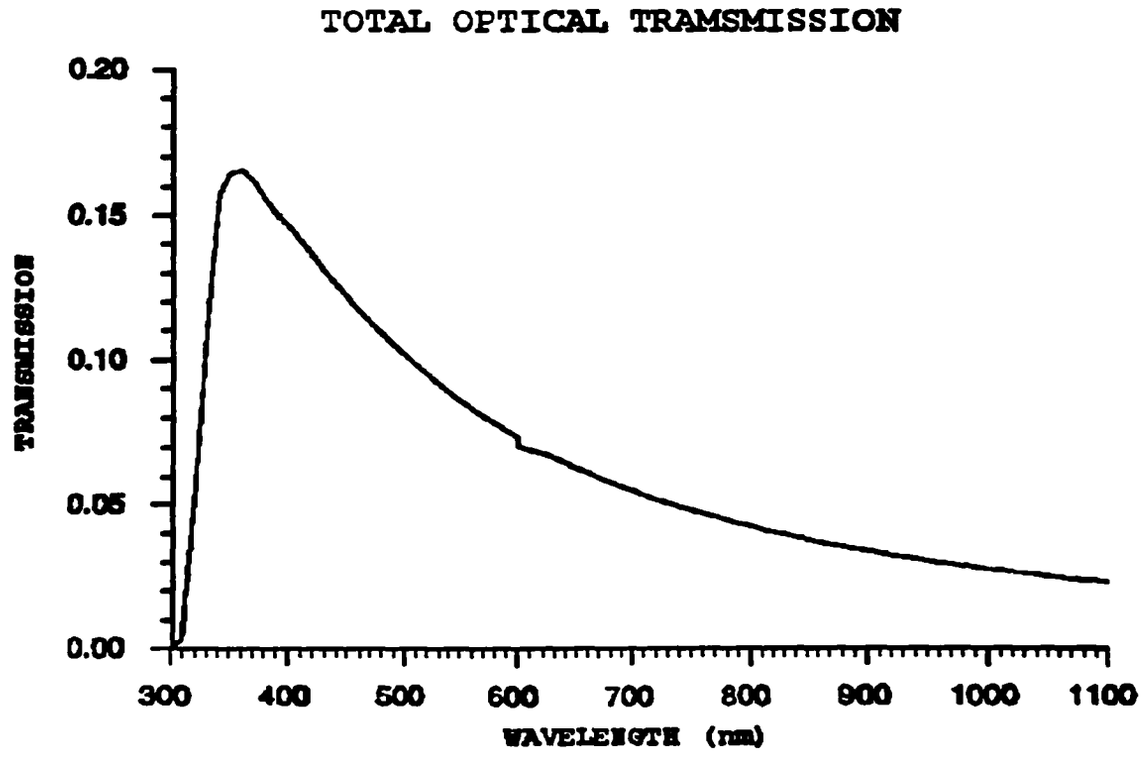


Figure 3.7 Spectrograph Optical Transmission

3.1.2 Entrance Slit

The width of the entrance slit, in part, determines the theoretical resolution of the system. The smaller the slit size the better the resolution. However, the slit can not be made infinitely small or no light will be imaged on the detector. The width of the entrance slit, w_e, is determined by $w_e = \frac{\Delta\lambda}{RLD}$, where $\Delta\lambda$ is the actual resolution bandwidth and RLD is the reciprocal linear dispersion of the grating [15].

For this system, the grating reciprocal linear dispersion is 35 nm per mm and the entrance slit width was selected to be 0.025 mm, which produces a theoretical minimum resolvable wavelength of 0.875 nm or approximately 1 nm. Consultation with representatives from American Holographic suggests that a resolution of 1 nm is possible with a 25 um slit width, although image blurring will limit the resolution.

The resolution limit is approximately twice as large as a physical cell width or pixel size of the CCD detector. For this design one pixel refers to two physical cells in the CCD detector. These cells will be averaged internally using the clocking scheme presented in the System Design Chapter.

3.1.3 Entrance Optics Design

The lens system is designed to partially focus the sun onto the diffuser. It will operate over the visible and near infrared wavelength region, approximately 300 to 1100 nanometers. The primary characteristics under consideration when choosing a lens material are index of refraction and transmission, both vary with wavelength. Optical glass is one choice of lens material because it functions over the selected wavelength range, is stable, readily fabricated, homogeneous, clear, and is economically available [16]. Other materials that have better ultraviolet transmittance properties may be required to improve performance at the short wavelengths.

The f-number of the spectrograph is f/2.5 and, to achieve maximum energy transfer from the entrance optics to the spectrograph, the system geometry defined by the

aperture after the diffuser (diameter 2a) and the aperture to entrance slit separation, b, is selected to yield an effective f-number of f/2.5.

The front end optics design specifications must meet the preceding specifications for optimal optical throughput. The front end optical design is depicted in Figure 3.8.

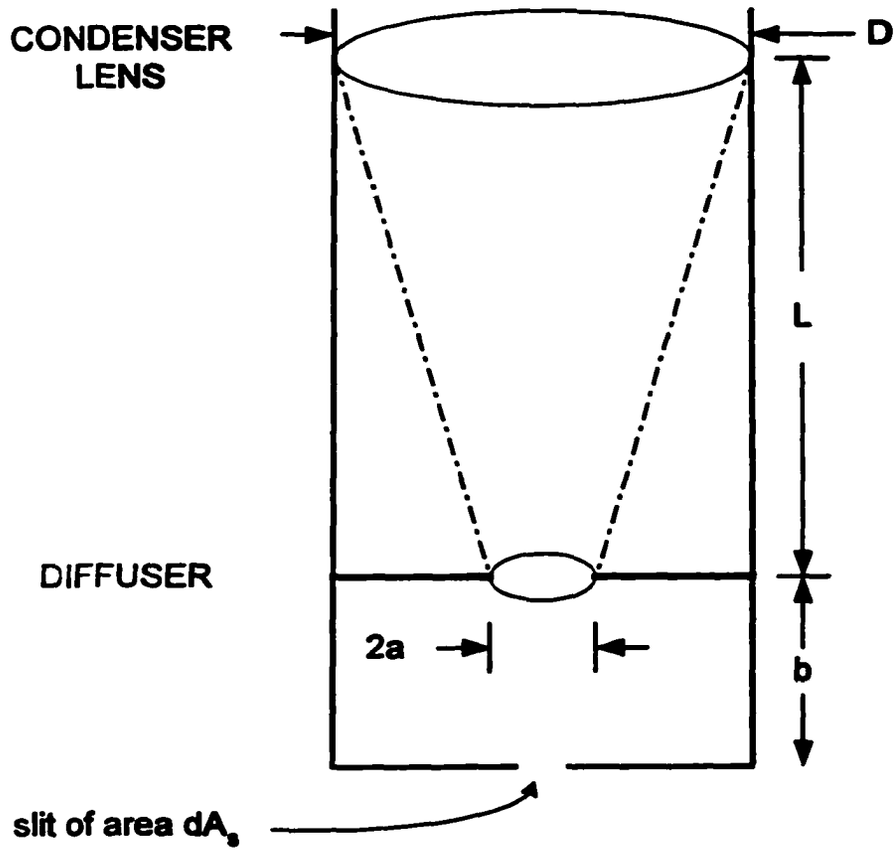


Figure 3.8 Front End Optics

3.1.4 Diffuser

The purpose of the diffuser is to distribute the light falling on the entrance slit so that it appears to have the same brightness regardless of the angle that it enters at or from what angle it is viewed. A perfect diffuser, one that has the same brightness when viewed from any angle, is said to be Lambertion. A Lambertion diffuser does not exist, but several materials behave as though they were Lambertion when used over a limited set of conditions. A diffuser such as matte white paper is an easily procured material that reflects 70 to 80 percent of the incident visible light. Magnesium oxide and magnesium carbonate are often used as diffusers in radiometry because they are 98 percent efficient.

Spectralon was chosen as the diffuser because it has a transmission of greater than 50 percent over the wavelength of interest. A typical transmittance / reflectance curve of Spectralon is shown in Figure 3.9.

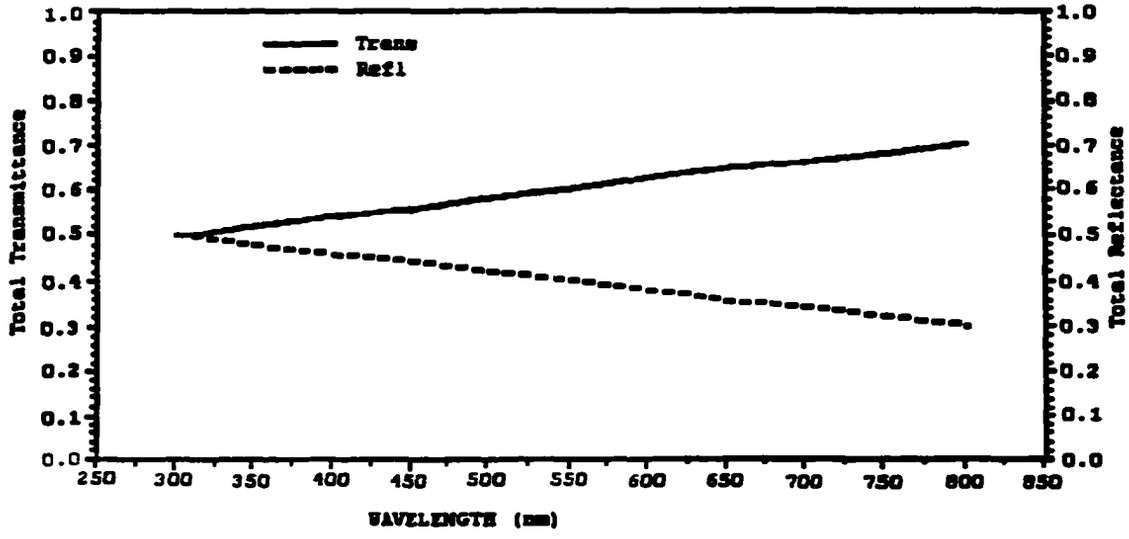


Figure 3.9 Spectralon Characteristics

3.2 The Detector

The detector chosen is the Linear Charge Couple Device Image Sensor, TH7811(Z), from Thomson Composants. It has 1728 active pixels with 26 additional reference cells. The pixel size is 13 x 13 microns and the device is housed in 24-pin ceramic dual inline package. Special factory processes give the device a wide spectral range of 300 nm to 1100 nm.

The Optical Front End and Spectrograph bring the light into the instrument and disperse the light across the detector so each of the pixels of the CCD correspond to a specific wavelength. The TH7811(Z) converts the radiant energy falling on each cell to a voltage.

The CCD image sensor's light-to-voltage conversion process can be broken down into the conversion phase and the read-out phase. The conversion phase begins with an

exposure period, during which time the CCD converts the light incident on the linear array to a proportional quantity of electrical charge (photocharge) for each pixel. After the exposure, the photocharge from each pixel is stored to an associated MOS capacitor.

The readout phase occurs next where the accumulated charge from each MOS capacitor is sequentially shifted to the readout stage. The readout stage converts the stored charge to a proportional voltage where it can be measured.

3.2.1 Conversion Phase

The input of the CCD image sensor is an array of photosensitive cells that convert the incoming light to a charge. The detector has a photoMOS structure arranged in a single line of 1728 pixels with an additional 26 reference cells. When a photon enters the silicon an electron-hole pair is generated. The electron is collected in the depleted zone created by the MOS structure of the CCD, with the hole being re-combined in the silicon substrate.

The photoelement structure of a photoMOS device has a space charge region. The space charge region is induced by a polysilicon gate over a thin oxide layer. After the electron-hole separation, the charge is accumulated in the inversion layer. The photoMOS structure is used to store photoelectrons and to the transfer charges during shifts.

3.2.2 Readout Phase

The readout stage converts the charge to a voltage. The conversion is made using a diode adjacent to the output gate. After the voltage has been read out, charge in the readout stage is removed.

The readout sequence is divided into three stages, diode reset, floating diode, and charge sensing. The diode reset stage sets the reset clock high, switching on the reset MOS transistor. Charges from the previous video signal are conducted through the MOS transistor and are drained by the reset diode.

The floating diode stage returns the output to its low level state and the reset diode is isolated. Due to parasitic coupling of the MOS transistor in the reset circuit, the voltage level in the output circuit decreases.

The charge sensing stage sends charge to the floating diode. The diode voltage decreases by the amount $\Delta V_{signal} = \Delta Q_{signal} / C_L$. C_L is the reverse biased diode's capacitance and ΔV_{signal} is the voltage difference before and after the charge arrives. This voltage is fed to an amplifier before finally arriving at the device output pin.

3.3 CCD Characterization

The CCD has several parameters that are used to characterize device performance [17]. The Responsivity, R, for a particular illumination is the ratio of useful signal voltage to exposure. Responsivity is a function of photoelement sensitivity and charge to

voltage conversion. The responsivity is influenced by photoelement sensivity and the charge-to-voltage conversion efficiency.

The Sensitivity, S, or Quantum Efficiency is the total number of photocharges produced from a certain exposure. It is defined as the ratio of the number of photocharges collected to the number of incident photons for a particular pixel area.

The Charge to Voltage conversion is accomplished by the readout diode. The voltage on the diode, V_L, is Q_l / C_L, where Q_L is the sensed charge value and C_L is the sensing capacitance.

The Spectral Response of the device is usually presented as a plot of relative responsivity to wavelength. The vertical axis represents the relative responsivity and is a unit-less percentage. The horizontal axis represents the wavelength for the measurement.

The Photoresponse Non-Uniformity, PRNU, parameter quantifies the effects of local variations in layer thickness to quantum efficiency. It is the peak to peak difference in response between the most sensitive element to the least sensitive element. Under a uniform illumination this is one half of the saturation voltage. PRNU is expressed as a percentage of output voltage.

The Saturation Voltage, V_{SAT}, is the maximum output signal voltage that can be generated by the device. The voltage is determined by the storage capability of the cell, the output diode capacitance, the reset voltage and output amplifier clipping. The saturation exposure is related to the saturation voltage. The saturation voltage is the maximum output voltage obtained when increasing exposure and the saturation exposure

corresponds to the light level at which voltage saturation occurs. The saturation level depends on the photoelement or shift register capacity and the output capacitance.

Charge Transfer Efficiency, CTE, measures the percentage of charge transferred from one cell to the next. The CTE is a affected by both transfer clock frequency and the pixel pitch.

Dark Signal, V_{DS}, is generated in the silicon by thermal agitation, which energizes some electrons into the conduction band. These energized electrons are trapped in the potential wells and are added to the charge of the incoming signal. The thermal charge is proportional to time and is a function of temperature. The thermal charge is created in both the pixels and in the transfer stages.

Dynamic Range is the ratio of the saturation voltage to the r.m.s. temporal noise. The dynamic range does not include effects of the dark signal. Additional effective dynamic range must be included when computing the number of bits required for an analog to digital conversion or the dark current must be subtracted prior to conversion.

The Maximum Output Data Rate is limited by the output amplifier bandwidth and the speed performance of the internal logic. The transfer registers do not typically impose a limitation on the maximum output data rate.

Over Illumination Resistance or antiblooming is the ability of a saturated photoelement to contain any excess photocharge. Blooming is a localized problem and can arise from long exposure times in areas of high spectral response.

The conversion of photons to a measured voltage is not perfect. There are noise sources that affect the conversion accuracy which include Photonic Noise, Temporal Noise, Fixed Pattern Noise and Bias Charge Noise. Photonic Noise is a result of the corpuscular nature of light and gives rise to shot noise. Shot noise is equal to the square root of the number of electrons in a pixel.

Temporal Noise is due to the fluctuations over time of a pixel signal while in darkness. The major components of temporal noise are reset noise, amplifier noise, dark signal level, and transfer noise. Reset noise is caused when the PN junction of the cell is charged to its reference potential and increases as the square root of temperature. The reset noise is expressed as, $\sqrt{\left(\frac{kT}{C_L}\right)}$ in volts or $\frac{1}{q}\sqrt{kTC_L}$ r.m.s. electrons, where k is the Boltzmann constant, T is the absolute temperature, C_L is the readout capacitance, and q is electron charge. Amplifier noise is the combination of Johnson or thermal noise and 1/f noise.

Dark signal level is due to a random process similar to photon emissions. Its r.m.s. noise contribution is $\sqrt{N_0}$, where N_0 is the number of electrons corresponding to the dark current. The transfer noise is related to transfer efficiency and is given by $\sqrt{\varepsilon N N_S}$, where ε is the charge transfer inefficiency per stage, N is the number of stages, and N_S is the charge transferred.

Fixed Pattern is the total of all time-independent noise contributions by spatial fluctuations in the output signal. The two sources are dark signal non-uniformities due to inhomogenetities in the substrate, such as local crystal defects and spurious transients caused by clocks, power supplies and other switching logic sources.

The CCD detector used in this design is the TH7811(Z). The various electrical and optical parameters associated with the TH7811(Z) device are summarized in Figure 3.10 and Table 3.1.

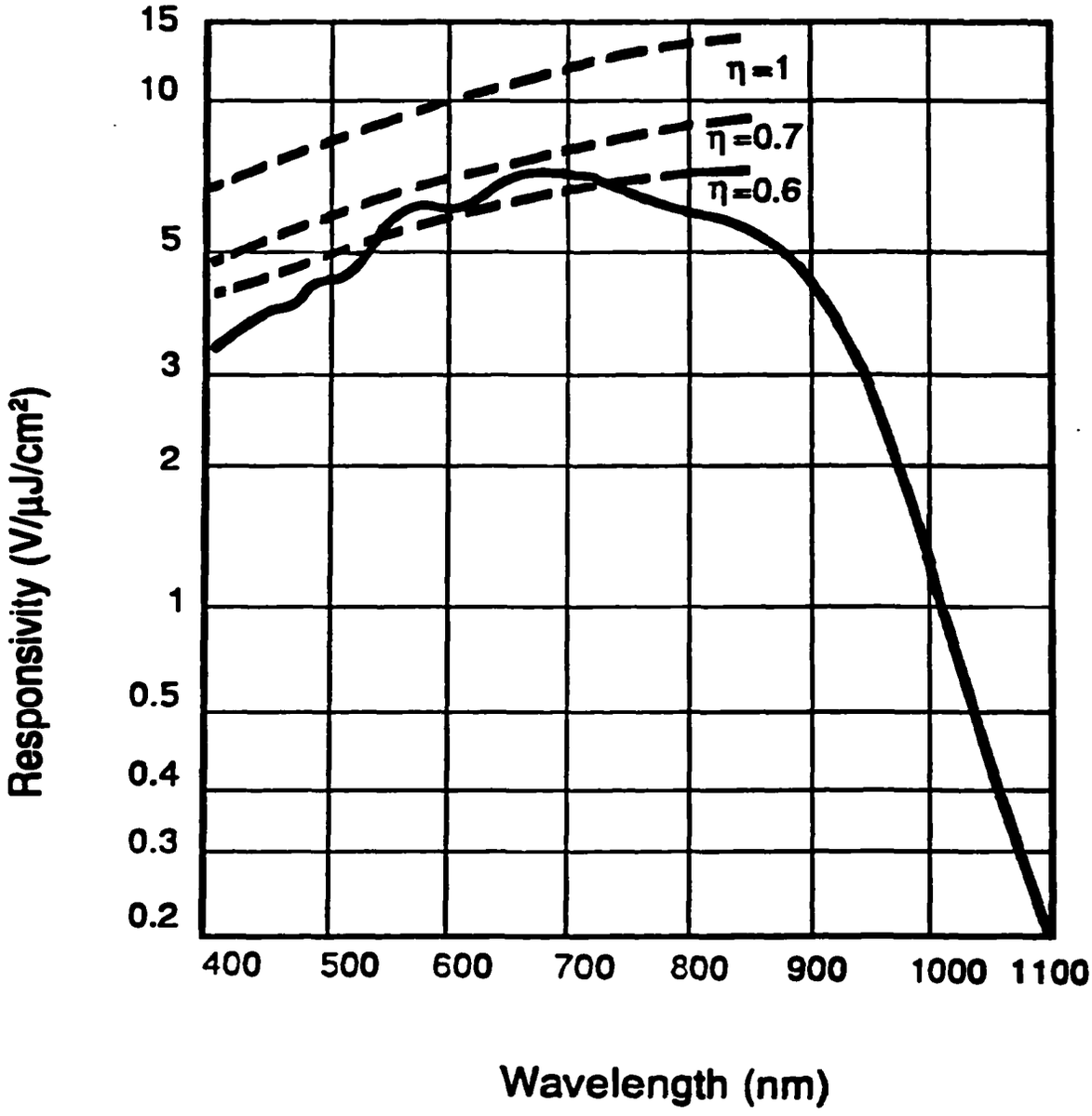


Figure 3.10 Detector Responsivity

Table 3.1Electro-Optical Performance

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Output Level	V_{OUT}	5	8	11	V
Output Impedance	Z_S		500		Ω
Single-stage Transfer Efficiency		99.992	99.998		%
Data Output Frequency		1	2		MHz
Saturation Output Voltage	V_{SAT}	1.3	2.0		V
Saturation Exposure	E_{SAT}		0.33		$\mu J/cm^2$
Responsivity	R	4	6		$V/\mu J/cm^2$
Temporal Noise in Darkness			350		μV(rms)
Dynamic Range	DR	3000	6000		
Average Dark Signal	V_{DS}		0.5	8	mV
Dark Signal Non-Uniformity	DSNU		0.5	8	mV
Amplitude of Signal Defects in Darkness				80	mV
Photo Response Non-Uniformity	PRNU		±5	±15	%V_{OS}

3.3.1 Thermal Control And Monitoring

Detector systems usually incorporate a temperature control system to cool the detector to a known temperature. The detector responsivity of a silicon type device is somewhat thermally sensitive in the shorter and longer wavelength regions. This thermal sensitivity can be compensated for provided the temperature of the detector is known. Cooling is extremely common for IR detectors, due to their higher noise levels, and was first considered for this design.

The proposed design is to be rugged, self contained and portable. These requirements limit the choice of coolers to peltier cells. These devices are solid state heat pumps. Apply a heat sink to one surface, attach the detector to the other surface and, when a voltage is applied to the peltier cooler, the detector side has the heat transferred to the heat sink. Analysis determined that the heat sink required would be extremely large and heavy. The peltier cooler approach was dismissed.

The second design option had the CCD heated so that it would remain at a stable temperature. The stabilized temperature insured a baseline noise figure that could be factored into the detectors output. This approach was dismissed because it introduced more thermal noise to the detector.

The option chosen in this design is to monitor the temperature of the detector and account for the increased current in the CCD's output. There are several unused cells buried in the CDD that will be used to monitor the noise associated with temperature. These cells are the before mentioned 26 reference cells. Their readout voltage will be

converted and stored along with the video readout signal. Processing at the host computer will subtract out these noise sources from the video signal.

There are additional types of noise or error sources associated with the CCD output signal. They are Shot noise, Reset noise, Amplifier noise, Dark Current noise and Bias Charge Error. Each of these noise sources has different dependencies on operating conditions. Shot noise depends only upon signal level. Johnson noise is influenced by variations in temperature. Reset and Amplifier noise are constant for a particular design and are due to readout capacitance and bandwidth.

System design techniques can minimize the effects of these sources of noise. For example, by insuring adequate illumination of the detector, shot noise effects are reduced. Signal averaging reduces Reset and Amplifier noise. Bias error is eliminated by design. The Dark current can be directly measured from the CCD and can be subtracted from the output signal.

CHAPTER 4

SPECTROMETER HARDWARE

The electronic hardware of the spectrometer system basically measures the output of the CCD and sends the data to the Host Computer. The electronics system is divided into two subsystems, which are the Detector Electronics board and the Electronics Unit, Figure 4.1. The Detector Electronics Board contains the CCD detector and the ADC.

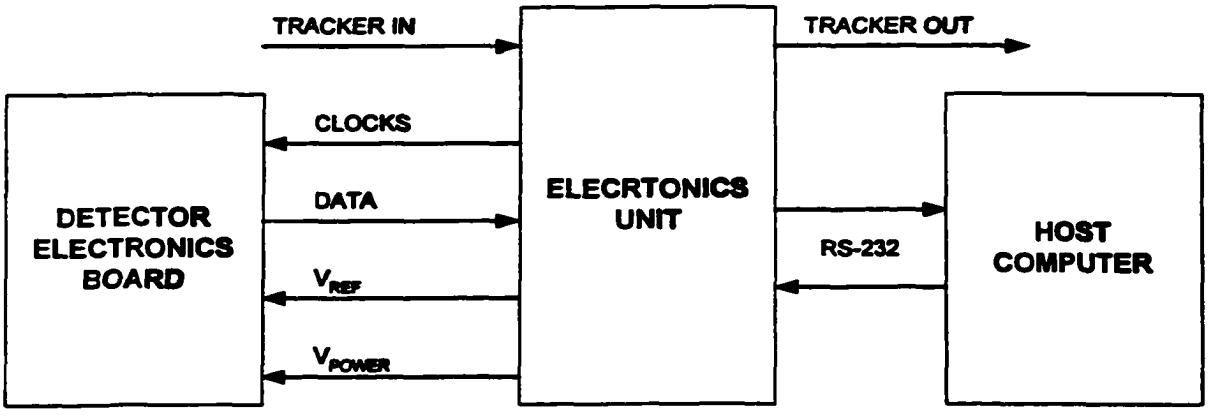


Figure 4.1 Electronics System Diagram

The Electronics Unit (EU) controls the Detector Electronics Board and interfaces with the Host Computer. The Host Computer can be of any type with a standard RS-232 serial port able to operate between 9600 baud and 38,400 baud, for example an Intel x86 PC or an Apple Macintosh.

The EU interfaces to the solar tracker using a simple two-wire interface. The Tracker-In signal is a movement request from the tracker and the Tracker-Out is a movement grant signal from the EU.

The interface between the Electronics Unit and the Detector Electronics Unit is comprised of several signals. These signals are composed of data, clocks, reference voltage and power supply voltages. The data is the converted serial data from the ADC of the output from the CCD detector. The clocks are comprised of both ADC and CCD signals. V_{REF} is the reference voltage required by the ADC. V_{POWER} are the various voltages used by the CCD and ADC.

The modular design of the system provides for a flexible, expandable instrument. The measurement range of the spectroradiometer can be modified by replacing the detector board alone, (also the optics). The same EU board and software would control the new detector board. The interface to the Host computer would likewise remain the same, preserving the software investment on the Host computer.

4.1 Detector Electronics Board

The Detector Electronics board primarily consists of the Charged Coupled Device (CCD) detector and the analog-to-digital converter (ADC). The circuitry was minimized to keep the board size and weight down so the board could be easily interfaced to a sun tracking system. The printed wiring board has been designed to mount directly on the American Holographics Model 100S Spectrometer. A block diagram of the board is shown in Figure 4.2 and a complete schematic for the board is in Appendix A.

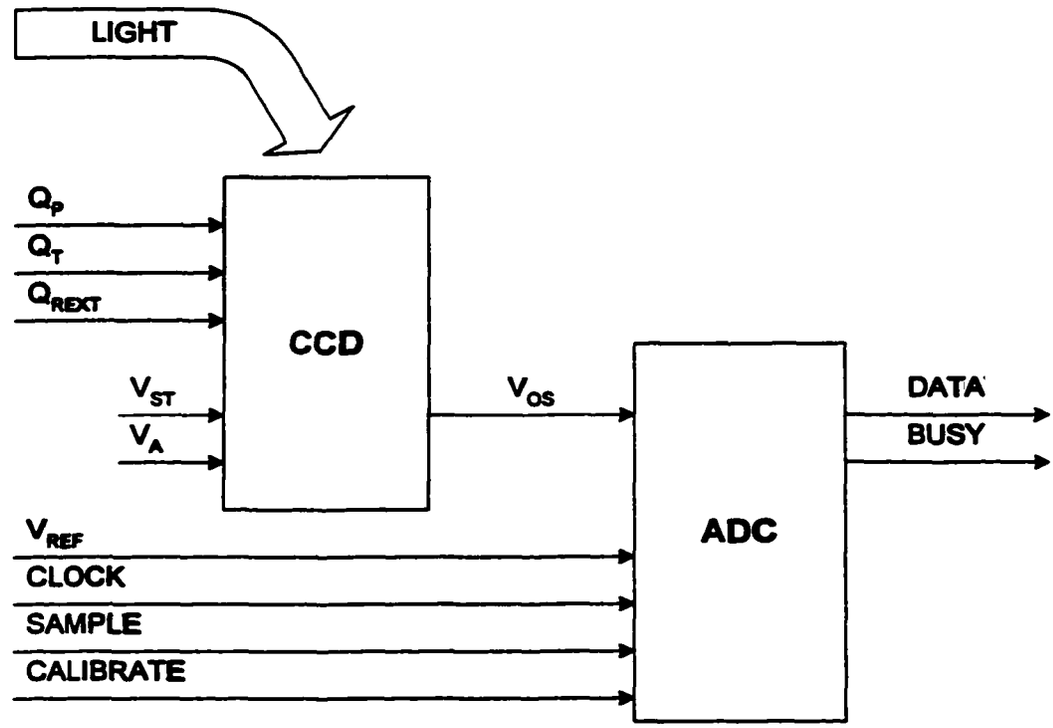


Figure 4.2 Detector Electronics Block Diagram

4.1.1 CCD Detector

The CCD is a model TH7811A Linear CCD Image Sensor from Thomson-CSF of Cedex, France. The TH7811A has one thousand seven hundred twenty-eight pixels with a pixel geometry of thirteen micrometers by thirteen micrometers. The spectral range of this detector is from ultra violet, three hundred nanometers, up to near infrared, one thousand one hundred nanometers. The minimum dynamic range of the CCD is three thousand to one and it has a typical dynamic range of six thousand to one. It has an internal sample-and-hold buffer with a disabling option that can be used to perform on chip pixel averaging to improve the quality of the signal at selected wavelengths.

The total video output stream is comprised of inactive cells, dark reference cells, isolation cells, and useful video. The makeup of the video stream from the start of integration time is eight inactive stages, four dark reference elements, four isolation cells, one thousand seven hundred twenty eight useful video pixels, four isolation cells, four dark reference elements and two isolation cells, as depicted in Figure 4.3.

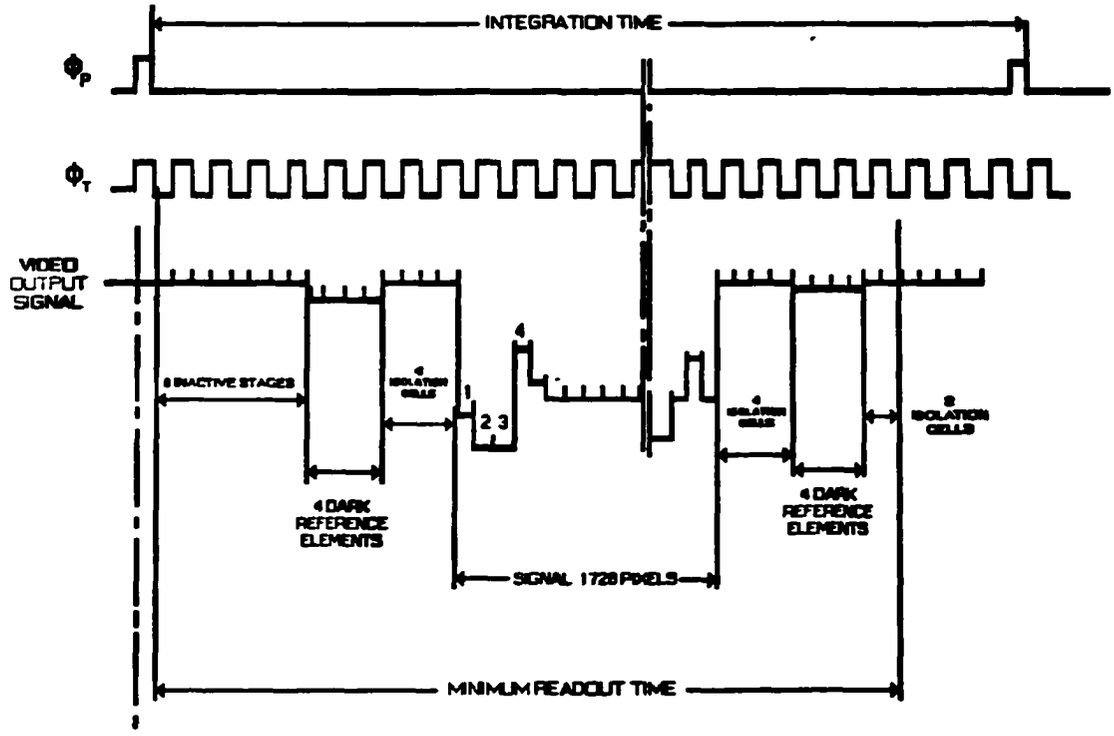


Figure 4.3 Typical CCD Drive Signals

Three drive clocks are required to operate the CCD detector. They are the Transfer clock (Q_P), the Shift Register Transport clock (Q_T), and the External Reset clock (Q_{REXT}). The Transport clock is used to reset all of the analog storage cells in the CCD,

and the time between these clocks is called the integration time. Care must be taken not to saturate cells at peak response wavelengths and at the same time insure that pixels at fringe wavelengths receive enough energy to produce a signal. The second signal mentioned is the Shift Register Transport clock, which is used to move the charge of each cell serially to the output buffer of the CCD. Each edge of this clock, the rising and falling edges, shifts the charge one cell. The last of the three clocks is the External Reset clock. The purpose of External Reset clock is to dump the accumulated charge in the output buffer. By controlling this signal in coordination with the Transport clock, pixel averaging can be accomplished internal to the CCD. An example of the timing is shown in Figure 4.4.

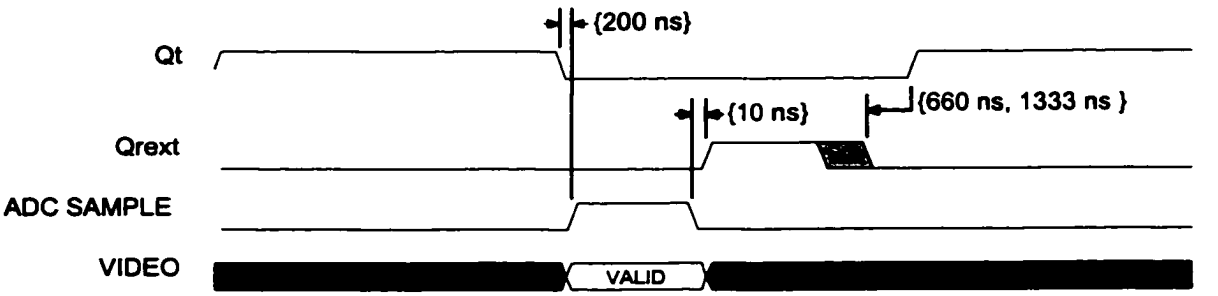


Figure 4.4 Operating Configuration With External Reset

The three clock waveforms used by the CCD are nominally switched between zero and twelve point five volts. The rising and falling edges of the clocks must be controlled to be between fifty and one hundred nanoseconds. This is required to avoid undue switching noise in the CCD.

The TH7811A detector has three complementary operating modes, Table 4.1. The various modes are selected by applying voltage to the pins. The values that are applied to the pins can be, no connection or pin open (NC), 14 volts (V_{DD}) and 0 volts (V_{SS}). Pixel Pairing or Pixel Addition mode is selected using the ADD pin and allows analog addition of odd and even pixels resulting in a video signal corresponding to eight hundred sixty four pixels with a dimension of twenty-six micrometers center to center spacing.

External Sample and Hold operating mode is selected using the $INHQ_{ECH}$ pin and inhibits the internal sampling and holding of the output video signal, V_{OS}. It is then possible to optimize the signal to improve the signal to noise ratio (SNR) by internally adding adjacent pixels in areas of weak signal while not averaging pixels in areas of strong signal. The improvement in SNR is directly proportional to the square root of the number of samples. This means that if one hundred frames were averaged the SNR would be increased by a factor of ten.

The last operating mode is External Reset Clock mode and is selected using the $INHQ_R$ pin. This mode replaces the internal reset clock Q_R with an external generated signal, Q_{REXT}. The external clock provides a tighter control on when the internal charge gets dumped and reset to zero volts, which allows greater freedom and maximum performance in sampling the output video signal with an external analog to digital converter (ADC).

This system takes advantage of the External Clocks mode and the External Sample and Hold mode by selecting these two control modes. It does not require the

Pixel Addition mode because the Electronics Unit controls the resetting of the video output signal and this mode can be duplicated by software.

Table 4.1 Selection Of Operating Modes

Pin Number	1	6	17	23
Designation	Q_{REXT}	ADD	$INHQ_R$	$INHQ_{RCH}$
Un-sampled video & internal reset	NC or V_{SS}	NC or V_{SS}	NC or V_{DD}	V_{DD}
Un-sampled video & external reset	Q_{REXT}	NC or V_{SS}	V_{SS}	V_{DD}
Pixel Pairing	NC or V_{SS}	V_{DD}	NC or V_{DD}	NC or V_{SS}

There are four bias voltage inputs on the CCD, which are V_T, V_{GS}, V_{ST} and V_A. V_T and V_{GS} are the Shift Register and Output Gate DC biases. The manufacturer recommends these signals be tied to TP1, which supplies 6.4 volts. V_{ST} is the Photosensitive Zone DC bias and is set to 6 volts. The last bias voltage, V_A, the Blooming Control DC bias is set to 3 volts which de-activates the anti-blooming control feature.

The Video Output signal from the CCD ranges from 0 volts to 11 volts. The ADC can accept signal levels of up to 5 volts. Scaling resistors are provided to divide the output voltage from the CCD to the 5 volt limit of the ADC.

4.1.2 Serial Analog to Digital Converter

The analog to digital converter chosen is the Analog Devices AD1876. The AD1876 is a sixteen-bit serial output sampling ADC. The format of the serial data out from the ADC is two's compliment format with the most significant bit (MSB) sent first. The ADC uses a switched capacitor/charge redistribution architecture to achieve one hundred thousand samples per second conversion time. This translates to a ten microsecond per sample total conversion time for reading out the entire CCD. The overall performance is optimized by digitally correcting any internal non-linearties through on chip auto-calibration.

The AD1876 includes a sample and hold input circuit, a successive approximation register, ground sensing circuitry, serial output port and a microprocessor controllable auto-calibration circuit. The device uses a successive approximation technique to determine the value on the input analog voltage. Unlike other devices that require precision laser trimmed resistor networks, the AD1876 uses a capacitor array, charge redistribution technique. An array of binary weighted capacitors subdivides the input value to perform the actual conversion. This capacitor array also serves as the sample and hold function. A low impedance drive signal is therefore required to guarantee conversion accuracy.

The internal calibration circuit employs a microcontroller and calibration DAC to measure and compensate for capacitor mismatch. As an error is determined, its value is stored in on-chip RAM. Subsequent conversions use these RAM values to subtract errors

and improve conversion accuracy. The auto-calibration process may be invoked at any time and ensures high performance while eliminating manual external adjustments. The microcontroller also controls the successive approximation routine, the sample and hold operation, and the serial transmission of data from the ADC.

The AD1876 requires an external voltage reference. The input voltage range is determined by the value of the reference voltage. A reference voltage of five volts will result in an input range of plus five volts to minus five volts. The EU will supply the ADC with a reference of five volts.

The analog input to the device is related to the voltage reference. For purposes of ground drop and common mode rejection, the analog input and reference inputs have separate grounds. The voltage reference uses the system analog ground and the input signal has a separate analog ground sense pin. This additional ground allows the AD1876 to use a remote ground sense for the input signal. The two grounds must be within one hundred millivolts of each other to ensure converter performance.

The ADC on the Detector Board interfaces to the processor on the EU. The interface with the processor is accomplished using SPORT 1, a synchronous serial channel in the processor. The processor accepts the data and busy (frame sync) signals from the ADC with the CPLD supplying the sample signal for the ADC and clocks to the processor and ADC.

4.2 Electronics Unit

The Electronics Unit interfaces the Host computer to the CCD detector board. It also controls the data capture and clock generation for the spectrometer system. Figure 4.5 shows a block diagram for the EU and a complete schematic is included in Appendix B. The EU consists of a single clock source, the processor, memory, UART, CPLD, a 4-channel ADC, voltage reference and linear voltage regulators. In addition, there are a power-on-reset chip, LEDs, various buffers and signal conditioners on the board.

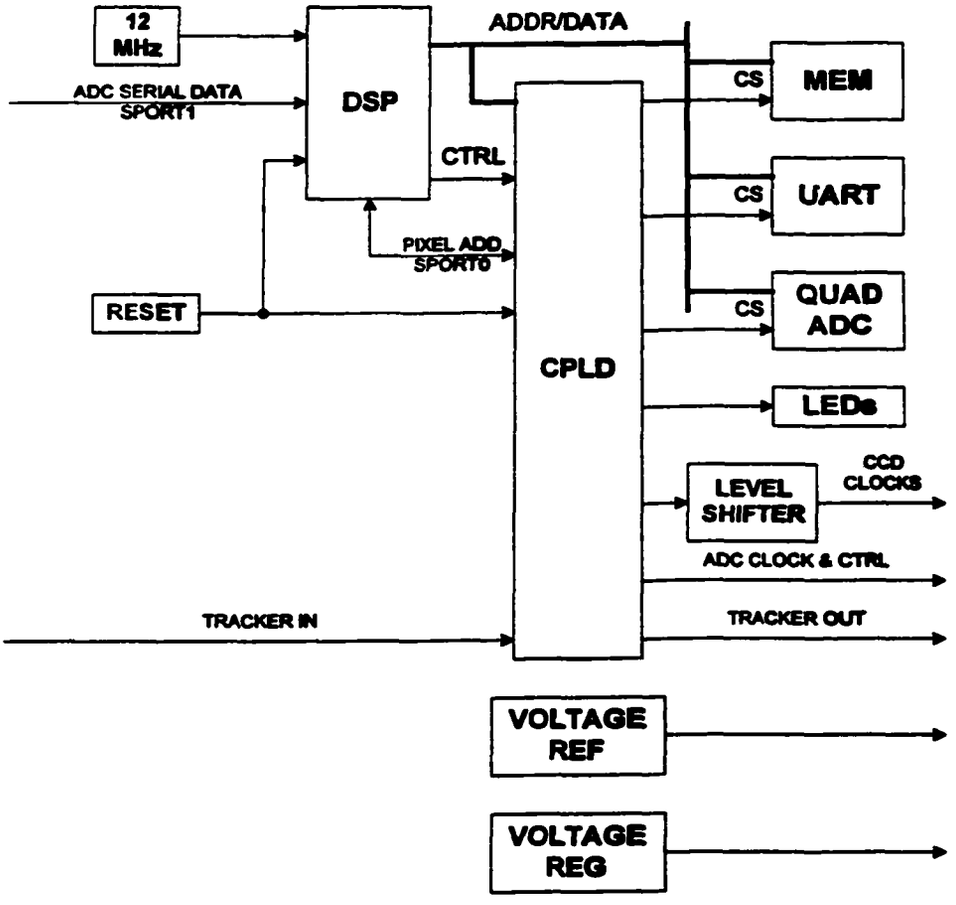


Figure 4.5 EU Block Diagram

4.2.1 Master Clock

There is a single, master clock source for the instrument. It is a 12 MHz crystal that is attached to the processor. All other clock sources used by the Detector Electronics Board and the Electronics unit can be traced back to this clock.

4.2.2 Processor

The processor used on the Electronics Unit is the ADSP-2101 digital signal processor from Analog Devices [18]. The ADSP-2101 is a single chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications. It combines on one chip two independent serial ports, a programmable timer, external interrupts, a programmable wait state generator, data memory and program memory, Figure 4.6. The ADSP-2101 has one thousand twenty four words by sixteen bits wide of on chip data memory (1 Kword) and two thousand forty eight words by twenty-four bits wide of on chip program memory (2 Kwords). Both of these memory spaces can be expanded to sixteen kilowords by using external memories and decode logic.

The architecture of the ADSP-2101 is a modified Harvard Architecture type with cross memory transfer instructions. The architecture supports a high degree of parallelism. The processor can generate the next program address, fetch the next instruction, perform one or two data moves, update one or two data address pointers, perform a computational operation, and receive and transmit data using the two serial ports in one clock cycle. The parallelism of the ADSP-2101 is exploited in this design to

simultaneously send charge dump/retain commands to the CCD, accept data from the ADC, interface with the tracker and communicate with the Host computer.

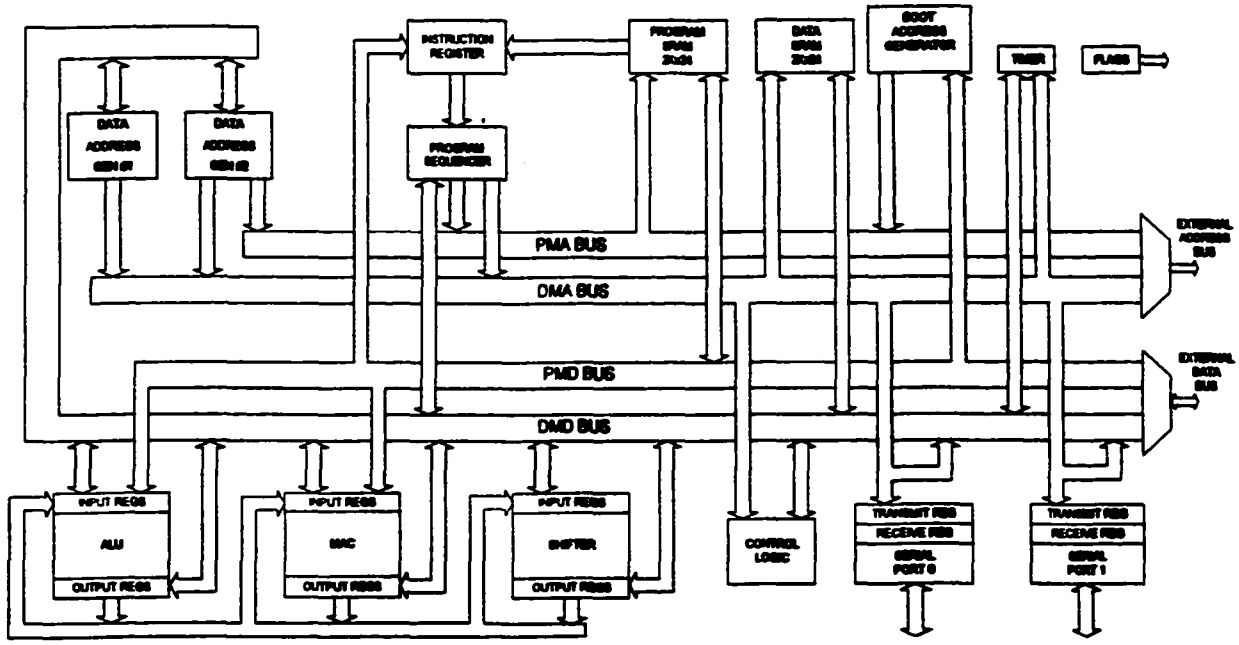


Figure 4.6 ADSP-2101 Internal Architecture

The ADSP-2101 processor is supported by a complete set of tools for software and hardware development. The software tools include a C compiler, an Assembler, a Linker and an interactive Simulator. Included also are utilities for creating boot PROMS and for defining system memory maps. The hardware tools include low cost processor modules with debug monitors and a hardware emulator very similar to the software simulator.

Processor booting is accomplished using a byte wide memory, the lower 8-bit SIMTEK Flash-SRAM device. The memory can contain up to eight separate programs that can be loaded independently to the processors internal program memory. The Boot memory space consists of an external 64 kilobyte space. At processor reset, page zero is automatically loaded using a default values of three wait states. Other boot memory segments can be loaded into internal program memory under software control. In addition, the internal program memory can be partitioned into segments that are preserved during software boot. This feature can allow common routines or data stored in program memory to remain intact and be shared among the different segments. The data memory is also untouched during software booting.

External devices that are interfaced to the processor must meet specific timing parameters for read and write accesses. Wait states may be added by the processor to service slower devices. Each wait state adds one CLOCKOUT cycle, 83 ns, to the access time. The ADSP-2101 can internally generate up to seven wait states per access via software configuration control. This is accomplished by writing to the Data Memory Wait State Control Register. Figure 4.7 and Figure 4.8 show zero wait state read access and write access timings, respectively.

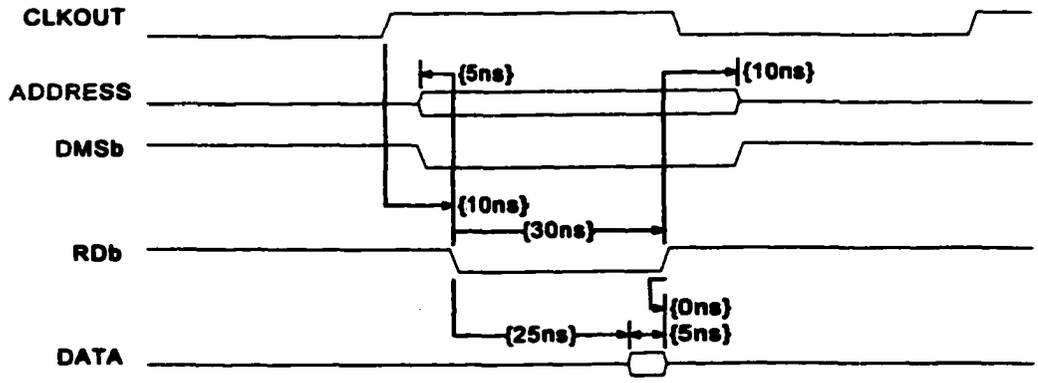


Figure 4.7 Read Access Timing - Zero Wait State

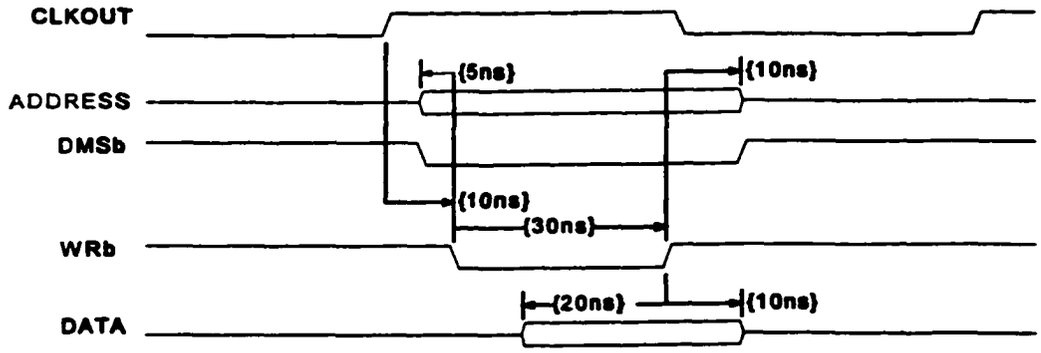


Figure 4.8 Write Access Timing - Zero Wait State

All devices on the processor data bus use Data Memory Strobe, DMSb, and are affected by the data memory wait state register. The processor divides the external memory space into five regions. Each of the regions can have a different number of wait states associated with it. The address mapping for memory space DWAIT0 is 0 through

0x3ff hex, for DWAIT1 is 0x400 hex through 0x7ff hex, for DWAIT2 is 0x800 hex through 0x2fff hex, for DWAIT3 is 0x3000 hex through 0x33ff hex, and for DWAIT4 is 0x3400 hex through 0x37ff hex. Above these external memory areas reside the internal memory space from 0x3800 hex through 0x3bff hex, which includes memory mapped registers and reserved areas.

4.2.3 Memory

The largest region of contiguous memory defined by the system extends from 0 through 0x1fff hex. The memory device used is a SIMTEK nonvolatile static RAM. This device couples an electrically erasable programmable read only memory, EEPROM, and a static random access memory, SRAM, into one part. Upon power up, the contents of the EEPROM are loaded into the SRAM. This occurs prior to the processor reset being released. After the reset goes inactive, the processor loads its internal program memory from the SIMTEK memory and begins execution. The SRAM may now be used for general purpose storage.

The SIMTEK nonvolatile RAM provides software controlled movement of data from the SRAM to the EEPROM and from the EEPROM to the SRAM. The SRAM based boot memory allows a new program to be loaded into the system without removing the actual part and re-programming it in a device programmer. The scenario for loading a new program would be to first load the program into SRAM and then execute a software reset. The program would be loaded into the processors internal memory from the SRAM

and only when its proper execution has been verified would the new program be copied to the EEPROM.

4.2.4 UART

The UART selected was the Intel I82050. This UART is able to provide a standard communications link between the embedded processor and the host computer. The I82050 supports standard data rates up to a maximum baud rate of fifty-six kilobaud. In addition to the transmit and receive signals, the UART has seven input/output pins. These pins may be used to implement modem control functions or as general purpose input/output.

The I82050 is programmed using internal registers. The registers allow access to the various features of the device. These features include the baud rate generator, interrupt enable register, interrupt identification register, line control register, line status register, modem control register and modem status register. It also has a one word of scratch pad RAM. The memory map of the UART is shown in Table 4.2.

The baud rate divisor is computed by taking the system clock frequency, twelve megahertz, and dividing it by sixteen times the desired baud rate. Once this sixteen-bit hexadecimal integer is computed, it is written to the upper and the lower baud rate register. Two registers are required because the registers are eight bits wide and the divisor word is sixteen bits.

Interrupts can be programmed to activate on a receive machine error or break condition, receive data available, transmit data register empty, or with a change of state

on the modem input pins. Since there is only one interrupt pin, the line status register must be read and decoded to identify what particular interrupt was activated.

Table 4.2 UART Internal Registers

REGISTER	ADDR OFFSET	DEFAULT	DESCRIPTION
TXD	0	-	Transmit Data
RXD	0	-	Receive Data
BAL	0	2	Lower Baud Rate Divisor
BAH	1	0	Upper Baud Rate Divisor
IER	1	0	Interrupt Enable Register
IIR	2	1	Interrupt Identification Register
LCR	3	0	Line Control Register
MCR	4	0	Modem Control Register
LSR	5	60h	Line Status Register
MSR	6	0	Modem Status Register
SCR	7	0	Scratch Pad Register

The UARTs external inputs and outputs are translated to RS-232 levels using a Maxim MAX233 interface chip. This chip requires five volts to generate the RS-232 levels of plus ten volts and minus ten volts.

4.2.5 Quad ADC - AD7824

The AD7824 is a high speed, four channel, eight bit analog to digital converter. The device has a built in track and hold circuit and employs a half-flash converter. The conversion time is two and a half microseconds per channel. The AD7824 operates from a single five volt power supply and when using a five volt reference, each channel has a zero to five volt input signal range.

This converter was included in the spectroradiometer design to allow general analog signal measurement, for example, power form monitoring or temperature

measurement. The quad ADC is organized in the memory map as four consecutive data memory addresses following the base address of 0x3008.

4.2.6 Voltage Reference - AD588

The AD588 is a complete high precision monolithic voltage reference that supplies the ADC the required +5 volt reference. The AD588 includes the basic reference cell and three additional amplifiers that provide pin programmable output ranges. The amplifiers are laser trimmed for low offset and low drift to maintain the accuracy of the reference.

The initial accuracy of the AD588 allows it to be used as a twelve bit reference without external trim potentiometers or with the potentiometers to achieve higher resolutions. No external parts are required to configure the AD588.

4.2.7 Voltage Regulators

Three linear voltage regulators are used in this design. They provide proper supply voltages for the requisite devices and they decouple the analog devices from the raw supply voltages provided to the board. The regulators provide +12 volts and -12 volts to power the video ADC, and 12.5 volts to power the buffers that generate the CCD clock drive signals.

The CCD requires an additional power form of 14 volts. It is created from the 15 volt supply using a two diodes that create a 0.9 volt drop.

4.2.8 Complex Programmable Logic Devices

The EU uses a Lattice Semiconductor ispLSI 1024 CPLD[19], Figure 4.9. The ispLSI 1024 is a Complex Programmable Logic Device containing 144 registers, 48 I/O pins, six dedicated input pins, four dedicated clock input pins and a global routing pool (GRP). The GRP provides complete intercommectivity between all of these elements. The ispLSI 1024 features 5-Volt in-system programmability and in-system diagnostic capabilities.

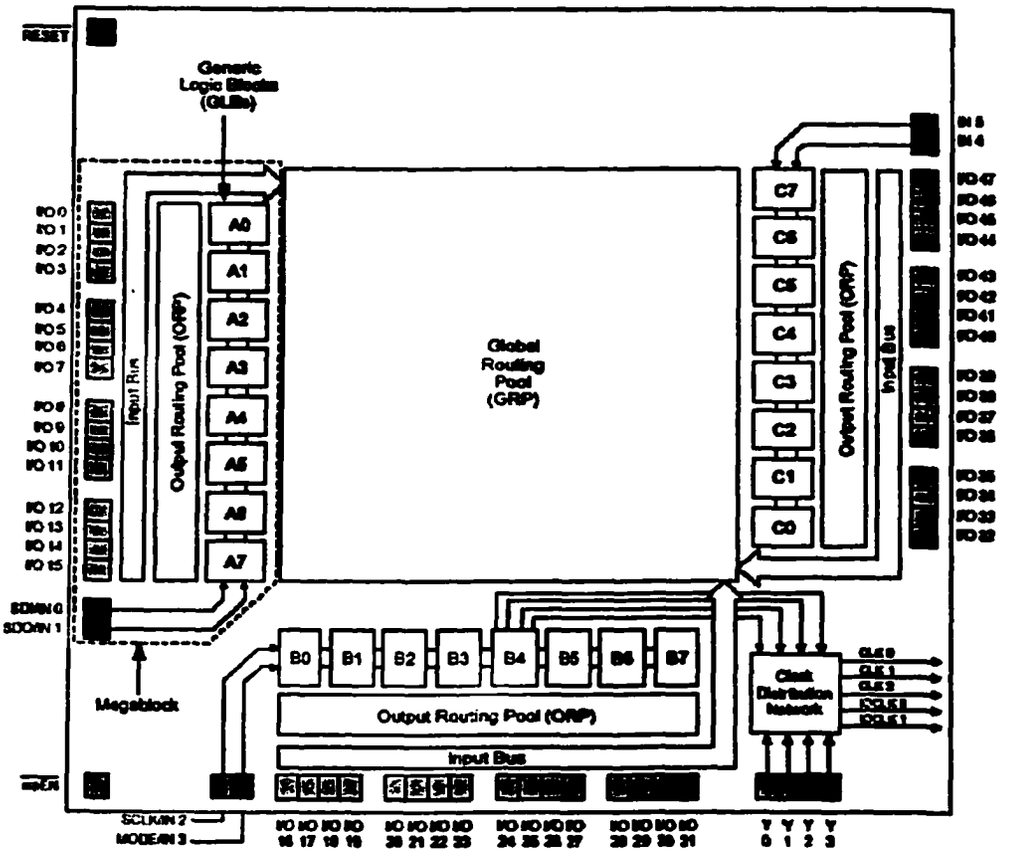


Figure 4.9 CPLD Architecture

The CPLD performs two primary functions. It decodes the DSP address bus to provide control signals for EU peripherals and generates the CCD drive signals. The DSP control signals include the chip enables for the memory, UART, and quad ADC; registered outputs for the status LEDs; and a two signal interface with the tracker. The memory map for the CPLD is shown in Table 4.3.

Table 4.3 CPLD Memory Map

ADDRES	NAME	DESCRIPTION
0x3000	UART	Base address for the UART.
0x3008	ADC	Base address for the quad ADC.
0x3010	RED_ON	Turn red LED on.
0x3011	RED_OFF	Turn red LED off.
0x3012	RED _TOG	Toggle state of the red LED.
0x3014	YEL _ON	Turn yellow LED on.
0x3015	YEL _OFF	Turn yellow LED off.
0x3016	YEL _TOG	Toggle state of the yellow LED.
0x3018	GRN _ON	Turn green LED on.
0x3019	GRN _OFF	Turn green LED off.
0x301A	GRN _TOG	Toggle state of the green LED.
0x301C	TRKRHLD_	Allow Solar Tracker movement.
0x301D	TRKRHLD_	No Solar Tracker movement
0x301E	ADCCAL_L	Stop ADC calibration.
0x301F	ADCCAL_HI	Start ADC calibration.
0x3020	TRKR_IN	Read Tracker request line.
0x3021	ADC_BSY	Read ADC busy line.

The CCD drive logic generates the control signals used on the Detector Electronics board to operate the CCD and ADC. This function was designed as a state machine with four states. These states are CCD_WAIT, CCD_QP, CCD_GO, and

CCD_DONE, Figure 4.10. The timing waveforms of the detailed CCD and ADC signals are shown in Figure 4.11. Appendix C contains the drawings and equations for the CPLD.

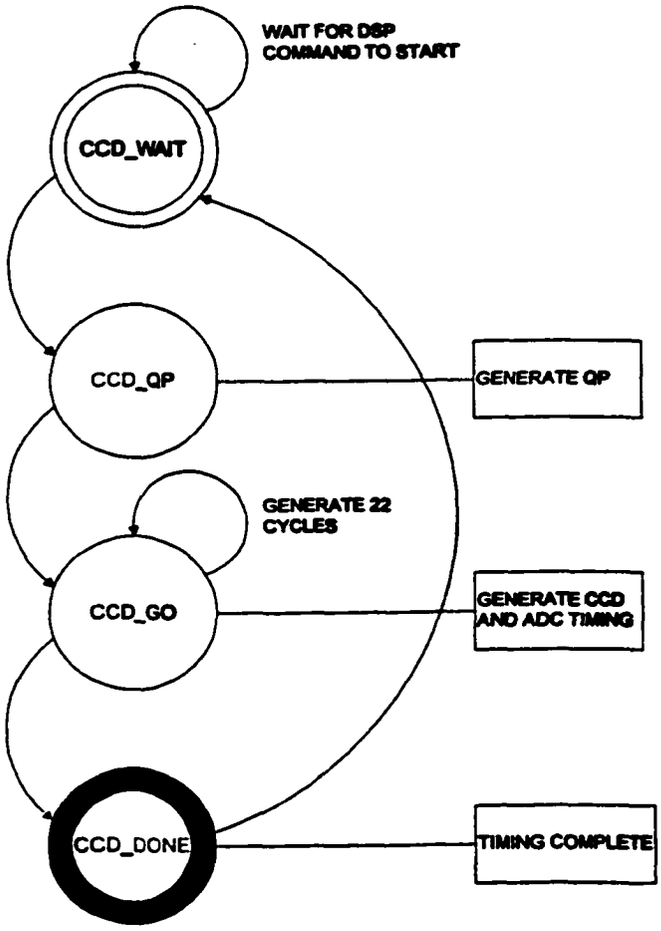


Figure 4.10 CCD Timing State Diagram

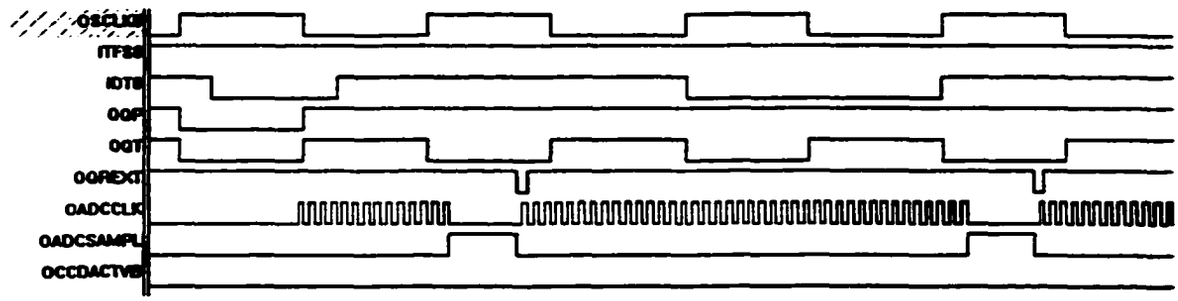


Figure 4.11 CCD-ADC Timing Waveforms

The CCD_WAIT state holds the CCD and ADC inactive, waiting for the DSP to initiate the process. The DSP starts the conversion process by transmitting data using SPORT0. The Transmit Frame Sync, TFS0, goes high causing the state machine to advance to state CCD_QP.

The CCD_QP state activates the Q_P signal on the CCD, which initializes the data shift/conversion process. The state machine then advances to the CCD_GO state.

The CCD_GO state is the state where the data collection and charge shift is controlled. This state is divided in 22 segments for each CCD clock cycle. In segments 0 through 10 the CCD transport clock, Q_T, is low and in segments 11 through 21 Q_T is high.

The ADC clock is active during the conversion process, but is gated off during cycles 13 through 18 where ADC_SAMPLE may be active. ADC_SAMPLE is active during cycles 13 through 18 when the data from the DSP SPORT0, DT0, is high. When ADC_SAMPLE is active, the ADC samples the CCD video output for 6 cycles. The ADC conversion begins when ADC_SAMPLE becomes inactive and the ADC clocking resumes.

Cycle 19 also samples the SPORT0 DT0 pin from the DSP. If the data pin is high, the CCD output is reset, otherwise the charge is allowed to accumulate in the CCD output buffer stage.

The TFS0 signal from the DSP is sampled during cycle 21. If TFS0 is high, the cycle counter is reset to 0 and the CCD_GO state is repeated. TFS0 being low identifies that all of the data has been shifted out of the CCD and the state machine advances to the CCD_DONE state.

The CCD_DONE state initializes all of the signals used in CCD_GO state and then branches back to the CCD_WAIT state. The CCD_DONE state also occupies a possibly unused state and prevents the state machine from becoming unstable.

4.3 Hardware Summary

The system does not require special software to operate and was designed to be easily reconfigured as newer detectors become available, Figure 4.12. The spectroradiometer electronics, Figure 4.13, were partitioned into two boards, a detector board, Figure 4.14, and an EU board, Figure 4.15. The detector board was designed with an on board ADC to reduce noise pick-up and to provide a digital interface with the EU. The signals between the two boards are buffered and allow a separation of approximately five feet.

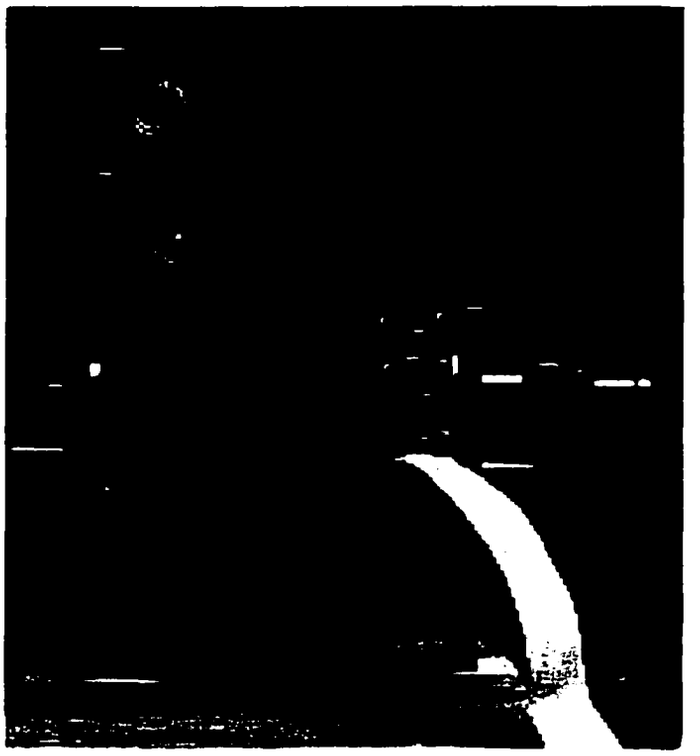


Figure 4.12 Spectrometer Mounted on Tracker

Figure 4.13 Bench Set-up

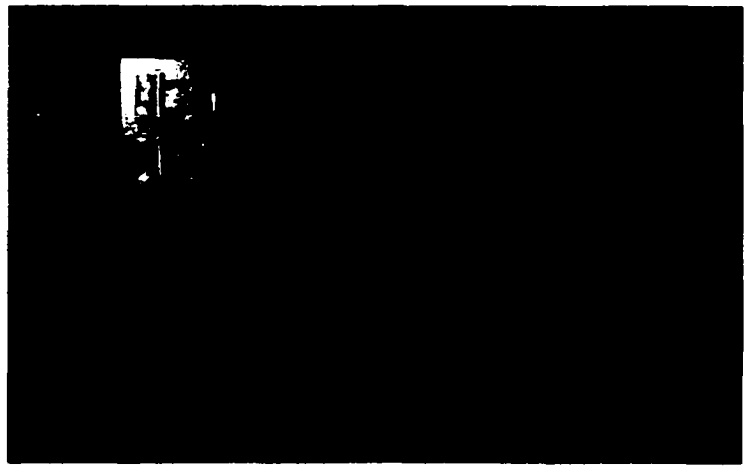


Figure 4.14 Detector Electronics Board

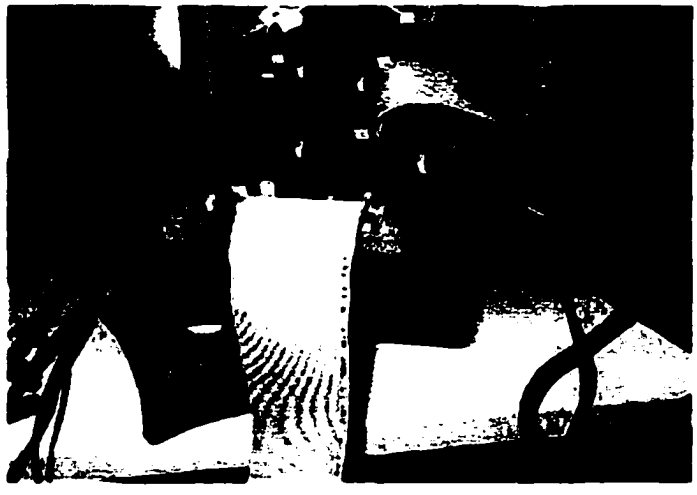


Figure 4.15 Electronics Unit Board

The EU is comprised of two major components, the ADSP-2101 and the CPLD. The DSP communicates with the Host computer and provides high level control information to the CPLD using SPORT0. The CPLD accepts the data from the DSP and generates all of the low level signals required by the CCD and ADC. The following four

figures are oscilloscope screen captures showing Q_P on trace 1, Q_T on trace 2, Q_{REXT} on trace 3, and the ADC sample signal on trace 4. Figure 4.16 shows a close up of the first cycle. Figure 4.17 shows the waveforms required to generate single pixel data collection. Figure 4.18 shows the waveforms required to generate two pixel data averaging. The last shot, Figure 4.19, shows the waveforms required to generate complex pixel averaging.

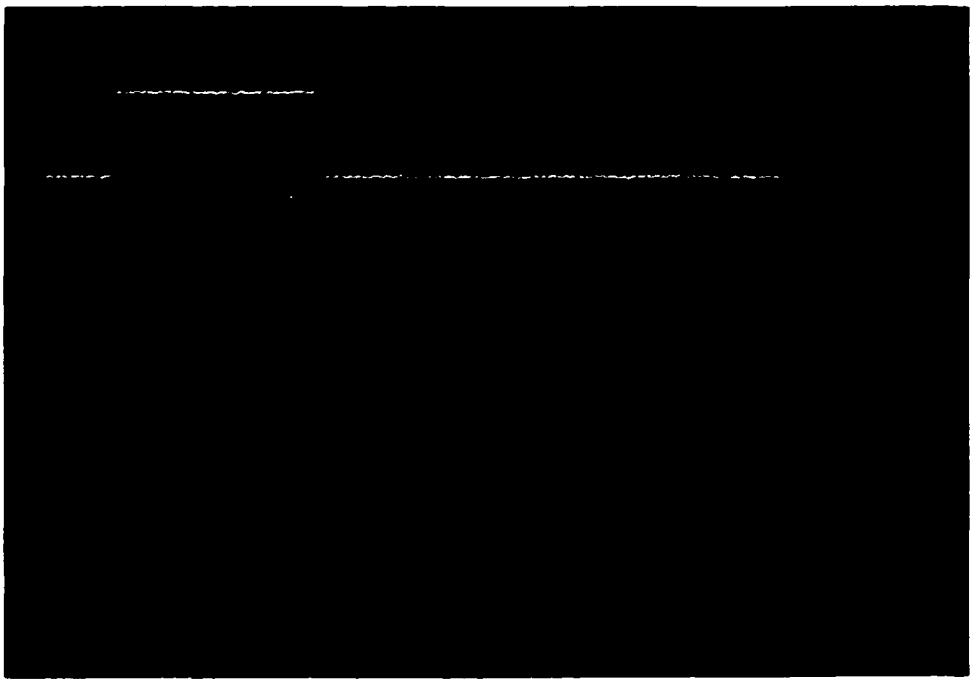


Figure 4.16 Close up Scope Photo of First CCD Pixel Cycle

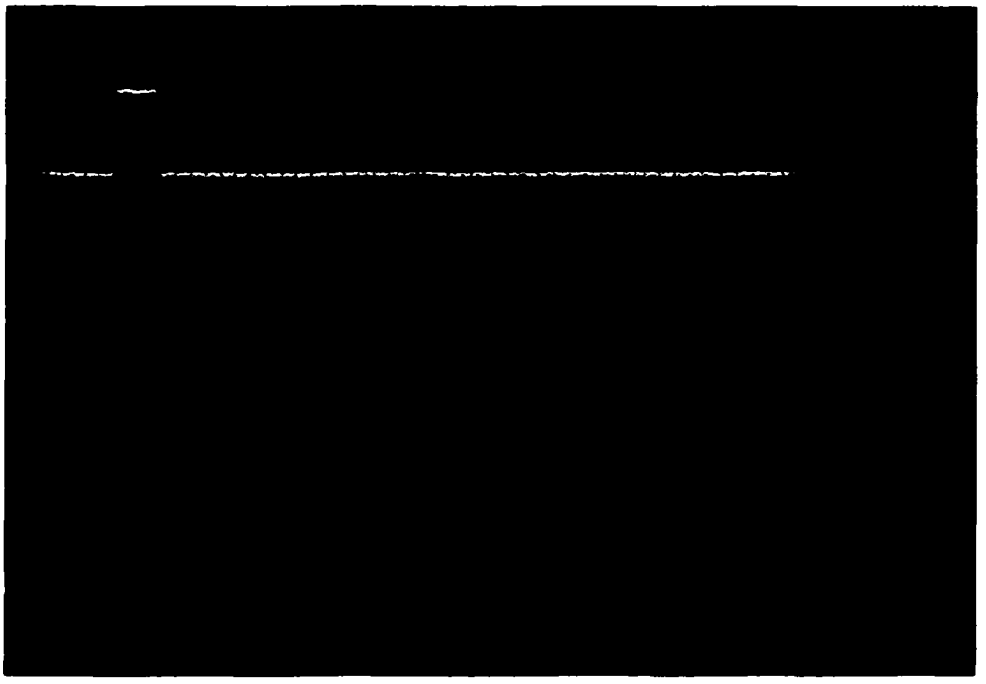


Figure 4.17 Scope Photo of 1-Pixel Data Collection

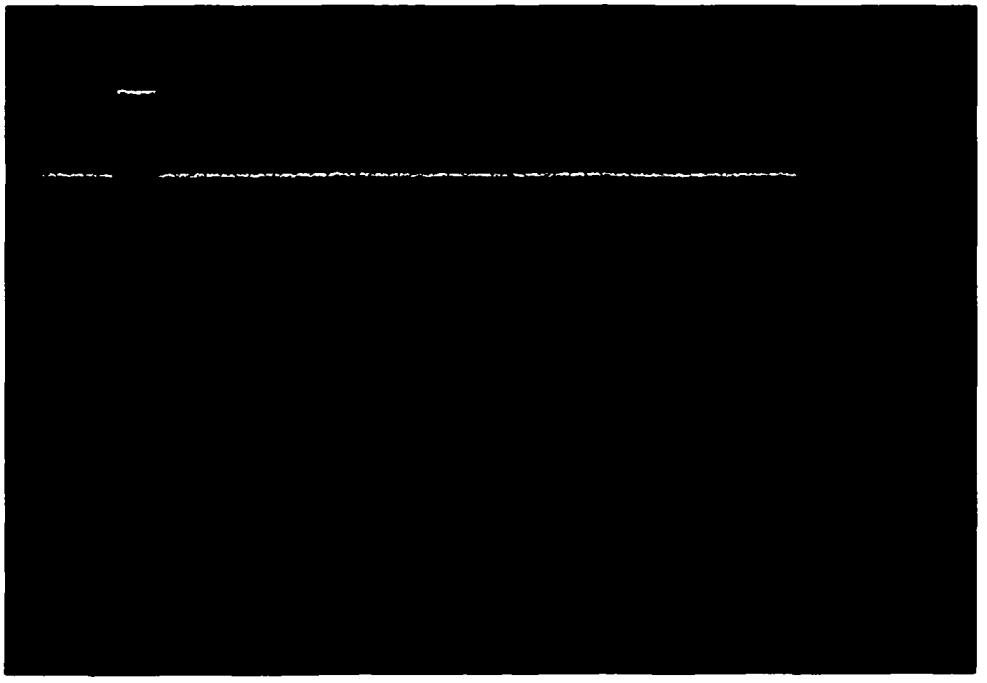


Figure 4.18 Scope Photo of 2-Pixel Averaging

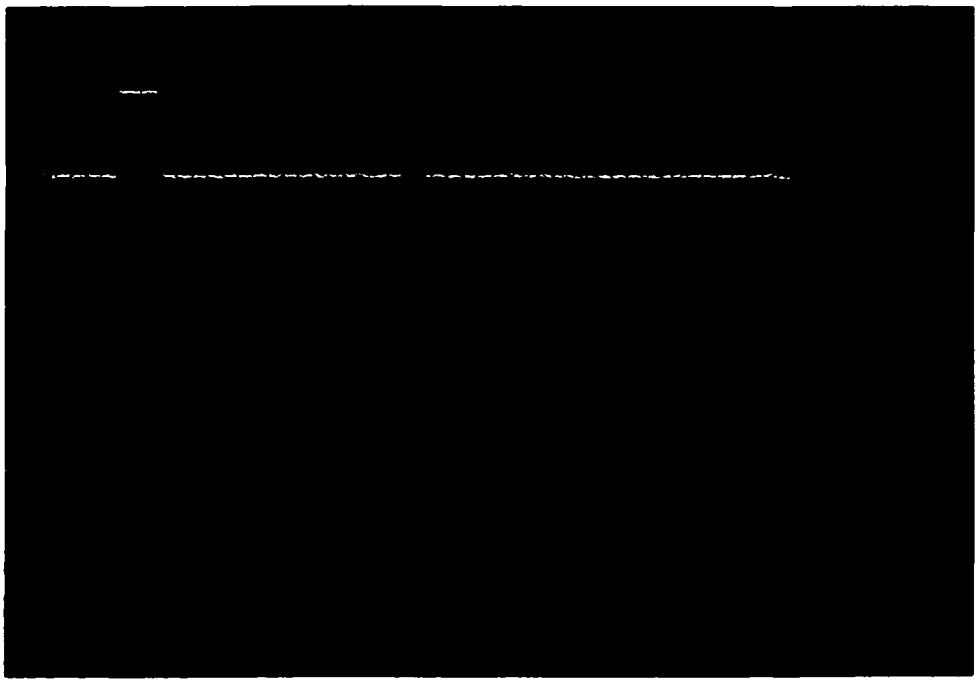


Figure 4.19 Scope Photo of Complex Pattern Pixel Averaging

CHAPTER 5

SOFTWARE

The software for the spectrometer is presented separately from the hardware, but each must be regarded as an extension of the other. Both pieces are integral to the operation of the instrument. The design of the spectroradiometer system takes full advantage of the embedded processor. The processor gives the system abilities that otherwise would require either special interface software designed for a particular Host computer or more extensive hardware to likewise control the system. The embedded processor runs tasks that both communicate with the Host computer and control the data capture process of the instrument.

The Host computer to spectrometer interface is An RS-232 serial data link. The serial link allows the instrument to be conveniently placed for making solar measurements while the Host computer can be located in a more pleasant environment whether it is 25 feet away using a direct connection or placed remotely, communicating using a modem.

The user interface is a menu command structure that is presented by the embedded processor. These menus allow selection of all relevant parameters and functions, such as starting the data capture, setting retrieval profiles, and even downloading a different program to the processor. By using the menu scheme to control the instrument, no

special software is required to run on the Host computer; all that is required is a commercial communications program.

The communications protocol employed by the instrument uses the ASCII character set for commands, messages and data. By using plain ASCII text messages any computer using a simple terminal emulator program can operate the spectrometer and collect data.

5.1 Operational Software Menu Structure

The Spectrometer menu structure is easy to understand and use. When power is applied or a processor reset occurs, the Main Menu is displayed, Figure 5.1. The seven menu choices are described in the following paragraphs.

```
Spectrometer Main Menu (Rev 1.0)
0) RESUME
1) Download to RAM (Intel HEX)
2) Upload from RAM (CSV)
3) Xfer RAM -> EEPROM
4) Xfer EEPROM -> RAM
5) SETUP

7) REBOOT
```

Figure 5.1 Main Spectrometer Menu

5.1.1 RESUME

Resume causes data capture to start or stop. If zero is pressed when the main menu is displayed, the message "Capturing Data" is briefly flashed on the terminal followed by data scrolling quickly by. Pressing zero while data is being captured stops the instrument and displays the main menu.

Before starting the data capture on the radiometer, enable the data capture function on the terminal emulator program so that the data is written to the hard disk and not simply flashed by on the computer screen.

5.1.2 DOWNLOAD

The DOWNLOAD option causes the processor to accept a program from the Host computer and store it to the external SRAM. This new program can be executed from SRAM rather than from EEPROM, thereby guaranteeing proper operation of the new program before commitment to permanent storage. If the new program does not operate as expected, a power-on-reset will re-load the old program stored in EEPROM. This process of executing a new program from the temporary working area, the SRAM, before committing it to EEPROM ensures that a faulty program does not hang up the instrument requiring it to be brought back to the lab for service.

The file format used for downloading is the Intel Hexadecimal Object File Format. Intel hex was chosen as the file format because it is an industry standard and that the ADSP-2101 linker is able to produce this type of file format.

5.1.3 UPLOAD

The UPLOAD function allows the transfer of data from the spectrometer to the Host. The data can be stored in either internal or external data memory. The format of the data is the same as the radiometric data format that the spectrometer sends to the Host during data capture mode. The numbers are hexadecimal sixteen bit numbers separated by commas. The values are in ASCII format and may be captured by the terminal emulator program for off-line review.

The user is prompted for start address, in hexadecimal, and also for the number of words to upload to the Host. A new line, carriage return and line feed, is generated for every eight words sent out to aid in the data presentation.

5.1.4 TRANSFER - RAM TO EEPROM

The external memory used in the spectrometer is actually an array of SRAM and EEPROM housed in a single chip. The programmed movement of data from SRAM to EEPROM is accomplished using option RAM to EEPROM. Data stored in external SRAM is transferred to the underlying EEPROM. The whole array of memory is transferred at one time, no partial segments can be stored. If only a portion of RAM is desired to be stored to EEPROM, then the entire EEPROM must be recalled, the part of memory to be updated must be written to the SRAM and then the entire SRAM contents are written to EEPROM.

Transfer of data from RAM to EEPROM is accomplished by performing the read sequence shown in Table 5.1. This action must be followed exactly with no other

operations occurring between reads. The processor interrupts must be disabled during these instructions.

Table 5.1 RAM to EEPROM Programming Sequence

ADDRESS (HEX)	DESCRIPTION
0x000	Valid READ
0x555	Valid READ
0x2AA	Valid READ
0x7FF	Valid READ
0x0F0	Valid READ
0x70E	INITIALIZE READ CYCLE

5.1.5 TRANSFER - EEPROM TO RAM

The transfer of data from the EEPROM to the SRAM is accomplished like the transfer between RAM to EEPROM as described above. The transfer of data from EEPROM to RAM is accomplished by performing the read sequence of Table 5.2. This action must be followed exactly with no other operations occurring between reads. The processor interrupts must be disabled during these instructions

A special case of the data transfer occurs at device power up, when the boot program stored in EEPROM is copied to SRAM. The transfer takes a maximum of twenty microseconds and occurs while the processor is held in reset, a minimum of 150 milliseconds. After the reset is released the processor moves the contents of the SRAM

to internal program memory and then starts executing the code. The external SRAM is now able to be used for general purpose data memory by the processor.

Table 5.2 Recall EEPROM to RAM

ADDRESS (HEX)	DESCRIPTION
0X000	Valid READ
0X555	Valid READ
0X2AA	Valid READ
0X7FF	Valid READ
0X0F0	Valid READ
0X70E	INITIALIZE READ CYCLE

5.1.6 SETUP

Altering the data collection process is accomplished using SETUP. SETUP prompts the user to input a 16 bit hex value that will be stored as a simple pixel averaging constant. An example of simple averaging would be to average pixels in groups of four. A value of 0x8888 would cause four adjacent pixels to be internally summed in the CCD and produce one value that would be read by the ADC and stored in an array.

5.1.7 REBOOT

The REBOOT option performs a software boot of the system. This option is primarily used to execute software that was downloaded to SRAM. Once the software is thoroughly tested it can be stored to EEPROM for automatic boot load at power on.

5.2 Embedded Software

The processor used by the spectroradiometer is the ADSP-2101 from Analog Devices. The software tools used to develop code include a C compiler, a C-like macro assembler and linker. A simulator is available to aid in code checkout, as is a hardware emulator.

The task of coordinating the various processes that exist in the system is accomplished using interrupts. The ADSP-2101 processor has several built-in and external interrupts that allow simple context switching. Data tables are likewise easily handled using the built-in circular buffer support.

The processes that run on the ADSP-2101 are the Host Communications Task, the CCD Charge Dump Task, the ADC Read/Averager Task, and the Data Upload Task, Figure 5.2. These routines work in concert to provide the CCD with information necessary to control the charge dump feature and to read that voltage using the ADC when the conversion is complete. While these low level data tasks are running, a data averager task accepts the new data and processes it. The end result is an improved signal to noise ratio for the processed data. When the pre-determined SNR improvement has been reached, through data set averaging, the data is sent to the Host computer via the RS-232 serial port and the Movement Request line from the tracker is checked. The Host communications task waits for a user request to stop data gathering and a confirmation order to stop.

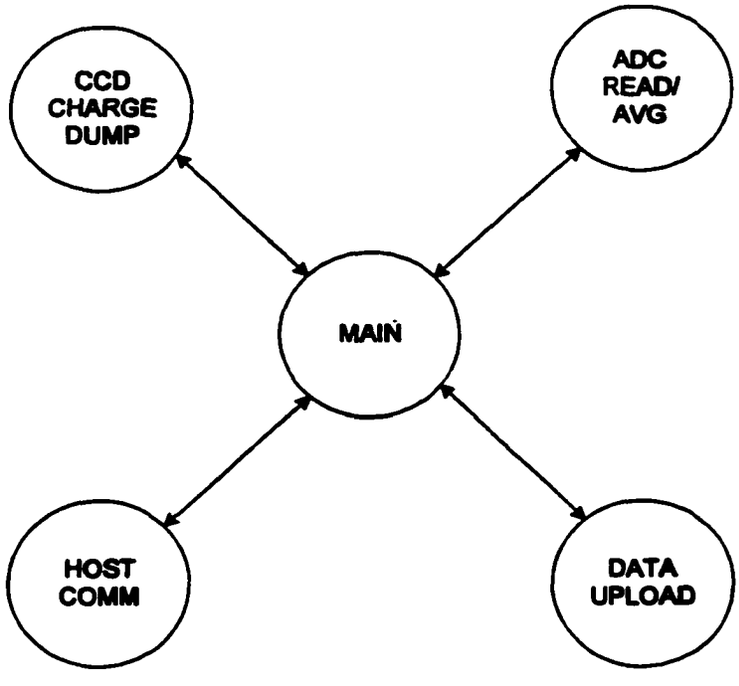


Figure 5.2 Software Tasks

5.2.1 CCD Charge Dump Task

Serial port zero on the ADSP-2101 is used to send charge dump commands to the CPLD. The data line of the serial port controls the CCD charge dump. Each bit of the data corresponds to two cells or one pixel of he CCD. The maximum serial word length of the ADSP-2101 is sixteen bits. This allows 16 pixels to be controlled by each 16 bit word output from the ADSP-2101, (charge dumping controls the internal pixel averaging in the CCD). The CPLD accepts this data and generates the necessary signals to insure proper timing criteria are met.

The data bits from SPORT0 are sent least significant bit, LSB, first. Averaging two adjacent pixels would result in a data word of 0xAAAA. For larger numbers of adjacent pixels to be averaged together it would require zero value words to be sent out between the "dump" word. Since the processor is capable of sending a table of values out of the serial port, any pattern of pixel averaging can be employed. By taking advantage of the circular buffer mechanism built into the ADSP-2101, this data averaging control table could be replayed with little processor overhead.

The data averaging table contains a complete charge dump pattern used to control the CCD. The data table is stored in internal RAM and is initialized as a circular buffer and pointed to by an indirect register. The automatic "increment by one" feature is enabled and the length of the data table is registered. The transmit serial port zero interrupt is activated.

The process begins by sending the first word manually. The process continues automatically, with the data table pointer being automatically incremented to the next word. When the entire data table has been sent an interrupt is generated.

The interrupt service routine sets a flag to indicate that this task has finished, resets the data table pointer and exits. This task will be reactivated by the ADC task after all of the CCD data have been read.

5.2.2 ADC Service Task

The ADC service interrupt routine accepts serial data from the analog to digital converter, ADC, using serial port one of the ADSP-2101. The sample pin of the ADC is controlled by the state machine in the CPLD. The sample pin is slaved to the CCD charge dump clock. This is done to insure that the CCD analog output is sampled by the ADC per the data sheet specifications.

The ADC generates an interrupt to the ADSP-2101 whenever the SPORT1 receive buffer is full. This interrupt activates the ADC task. Once activated, the ADC task retrieves the data from the serial port. The data is summed into a table of previous values as part of a running average which will be used to increase the SNR of the spectrometer data.

The ADC task also checks to whether the CCD Dump task has finished. The data averaging will stop when the pre-set number of averages has been attained and the data transmit task would be activated. Otherwise, the ADC task re-starts the CCD Dump task and another line of CCD data is retrieved.

5.2.3 Data Send Task

The data send task is activated by the ADC routine after the data set size limit has been reached. There are a maximum of eight hundred and seventy seven pixels that may be transferred. Each of these words is comprised of two bytes of data and is separated by a comma (one byte). The total number of bytes of data sent is two thousand six hundred and thirty three bytes. This includes a one byte header and a comma character as a separator. The time to transfer this data to the Host at a particular baud rate is shown in Table 5.3.

The data is sent to the Host computer in ASCII format. The data is sent without handshaking so the Host computer must be setup to receive and store the data. Terminal emulation programs such as Procomm and Telix are acceptable for data capture and will work at the required baud rates.

Table 5.3 Data Transfer Time

Baud Rate	Transfer Time (Sec)
9,600	2.74
19,200	1.37
38,400	0.69
76,800	0.34

During the Data Send task the spectroradiometer checks the tracker interface *Request Movement Flag,* the Tracker_In pin. If the flag is set, the sun tracker is requesting to move and data capture must be halted. The spectroradiometer acknowledges the request, allowing movement, by asserting the *Movement Allowed Flag,*

the Tracker_Out pin. The data transfer with the Host is started. After the transfer, the spectroradiometer waits until the *Request Movement Flag* is cleared. The spectroradiometer then clears the *Movement Allowed Flag*, signaling to the tracker that data capture has resumed and no movement may occur, Figure 5.3.

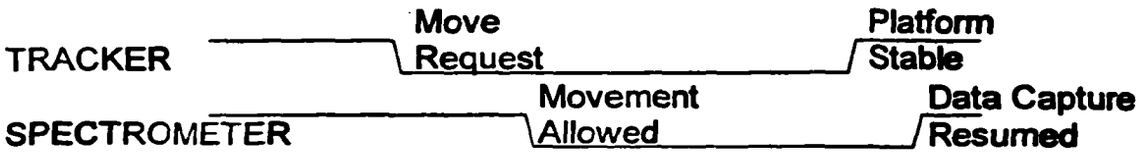


Figure 5.3 Tracker Interface

5.2.4 Host Communications Task

The Host Communications Task is very simple. During data capture the Host Communications task waits for the zero key to be pressed. Pressing 0 stops the data collection and returns the instrument to user control. The current line of data is processed before the data collection stops and the main menu is displayed.

5.3 Host Computer Requirements

The Host computer requirements are very minimal. The Host must be able to transmit and receive ASCII data at a minimum of 19.2 kilobaud for a sustained time. Because these requirements are met with a large variety of commercially available software no unique Host software was written to control the spectrometer. Additionally,

no particular type of Host computer needed to be specified. What is required by the Host computer to communicate with the spectrometer is a terminal emulator program that is able to accept ANSI screen commands, store the data received to disk, and to download ASCII data stored on disk to the spectrometer. Examples of acceptable programs for x86 class machines running MS DOS or Windows are Telix, Procomm, and Crosstalk; similar Apple computer terminal emulators are Versa Term and Claris.

Once the data have been stored to disk the results can be analyzed and displayed. Some examples of programs that are available to perform these functions are the spreadsheet programs Excel, Quattro Pro, and LOTUS 123. These programs will take the data and display it as a table and allow the data to be graphed. If the Windows or Macintosh environments are used then the graphs can be pasted into reports.

Other commercial programs exist that allow further analysis of the data. Examples of these programs are Math Cad and Mathematica. The results of these simulations can likewise be plotted and incorporated into documents.

5.3.1 Communications Protocol

The communications protocol requires that the Host computer be able to communicate with the spectroradiometer using an RS-232 serial channel. The physical parameters of the link are to use a baud rate of between 9600 and 38400 baud, a data word width of 8 bits, use 1 stop bit and not use parity checking. No hardware handshaking is implemented so the Host computer must be able to sustain these data transfer rates.

5.4 Software Summary

The software exploits the ADSP-2101's features both in spectrometer control and user interface. The processor is employed as both a programmable state machine, controlling the ADC and CCD, and also as a data processor. The novel use of the two synchronous serial ports as the high level control interface for the CCD and ADC minimized the necessary hardware while adding the flexibility of arbitrary pixel group sizes.

The menu scheme for the instrument makes the requirement of a specific type of Host computer arbitrary. It further acts as an on-line users manual, with all of the commands to operate the spectrometer available as simple menu choices. Additional features may be added to the menu or run as auxiliary programs that are downloaded when needed.

CHAPTER 6

SYSTEM OPERATION

The Systems Operation chapter combines the concepts presented in the hardware and software chapters, and describes the operation of the spectroradiometer as a whole entity. The physical instrument is, after all, an amalgamation of both hardware and software. The following sections discuss host computer serial communications set-up, instrument operation using Telix, instrument operation using Procomm Plus, plotting retrieved data using Excel, and data analysis using Math Cad.

6.1 Host Serial Communications

The spectroradiometer communicates with a host computer using a standard RS-232 serial channel. Initial communications with the spectroradiometer require that the host serial port be set with a baud rate of 19,200 baud, 8 data bits per word, one stop bit per word and parity checking disabled. The instrument uses a menu scheme to present choices to the operator which makes use of non-printing escape sequences to perform tasks such as cursor positioning, clear screen, highlighting, etc. The terminal emulation program running on the host computer must be set to ANSI Terminal for the menu presentation to appear correct on the screen.

The use of a menu scheme to communicate with the instrument allows for a wide choice of host computer types. Any computer with a serial port and a terminal emulation

program will suffice. Intel processor based computers, which are used by the Atmospheric and Remote Sensing Lab, were selected to interface with the spectroradiometer. Other types of host computers, SUN, APPLE, or other brands, can be used provided an ANSI terminal emulator program is available.

The operating system used by the x86 based computers in the Atmospheric and Remote Sensing Lab is DOS or Windows. Computers using the DOS operating system will use Telix as their terminal emulation program, while computers using the Windows operating system will use PROCOMM Plus for Windows.

6.2 TELIX

Telix is a DOS based communications program. Once Telix is configured it can be used to communicate and control the spectroradiometer. Telix is started by typing, "TELIX O", from the DOS prompt. The 'O' option informs Telix not to send a modem initialization string when it is started. The spectrometer could be placed in an undesired mode if it is sent a modem initialization string.

Telix begins operation in what is called terminal mode. While in this mode any characters typed on the keyboard will be sent to the spectrometer via the serial port, and any characters sent from the instrument will be displayed on the monitor. Telix program commands are initiated from this terminal mode. Most commands to Telix, not the spectroradiometer, require pressing two keys simultaneously. For example, to access the Telix HELP screen, hold down the Alt key and press the Z key (ALT-Z).

6.2.1 Telix Configuration

Configuring Telix to communicate with the spectrometer is accomplished using the Parameters menu. The Parameters menu is selected by pressing the ALT-P keys. This option allows modification of the serial data word format used by the host computer. After pressing ALT-P, a menu is displayed on the screen showing the serial port parameters currently in effect and the options available for modifying the serial word format, Figure 6.1.

```
Comm Parameters
 Current: 19200,N,8,1,COM1

  Speed          Parity          Data

 A: 300          J: None         Q: 7
 B: 1200         K: Even         R: 8
 C: 2400         L: Odd
 D: 4800         M: Mark         Stop
 E: 9600         N: Space
 F: 19200        S: 1
 F: 38400        T: 2
 F: 57600        O: N-8-1
 F: 115200       P: E-7-1

 1: COM1  3: COM3  5: COM5  7: COM7
 2: COM2  4: COM4  6: COM6  8: COM8

 Choice, or <Enter> to exit?
```

Figure 6.1 Telix Communications Parameters

There are a number of parameters that can be changed from the Parameters menu. The baud rate is the speed at which the serial port operates. Telix supports baud rates up to 115,200 baud. Parity is a form of data word error checking. Allowable parities

choices are None, Even, Odd, Mark and Space. Data bits specify the number of bits used to form a character. Allowable values for data word size are 7 or 8 bits. Finally, the stop bit parameter can be set to either 1 or 2 stop bits. The Parameter menu also allows the selection of the host communications port, usually COM port 1 or COM port 2.

Communication with the spectroradiometer requires that the baud rate be set to 19,200 baud, with 8 data bits per word, one stop bit per word and no parity checking. The appropriate serial port of the host computer must also be selected.

The configuration selected using the Parameters menu is in effect only for the duration of this communication session. The Options menu is used to define the default Telix configuration. The Options menu is selected by pressing ALT-O. Select "Terminal Options" and enter the Com port parameters. The terminal type should be set to ANSI and the Backspace key should send a "BS". The configuration should be written to disk so that the options selected will remain in effect each time Telix is invoked.

6.2.2 Receiving Data With Telix

Receiving data from the spectroradiometer requires TELIX to have the capture option turned on. The Capture option is invoked by typing ALT-L and specifying a file name. When the Capture option is active, all data typed on the keyboard or received by Telix will be stored to the named file. Pressing ALT-L a second time disables data capture. Remember that if data capture is reactivated and the same file name is given, the old data will be over written.

6.2.3 Sending Files To The Spectroradiometer Using TELIX

The primary use in sending files to the spectroradiometer is to download a program to the embedded processor. The new program is first compiled and linked on the host computer and then downloaded to the external RAM on the processor board. A software reset transfers the downloaded program to the internal program memory of the processor and then executes it.

The file download is a two step process. First, the spectroradiometer must be informed that a file is going to be sent and second, Telix must know how to send the file. The spectroradiometer is informed to expect a new file by selecting "Download to RAM (Intel HEX)". The instrument will now wait for a properly formatted Intel HEX file.

Telix file transfer commands are issued from the Send File menu, which is invoked by pressing Alt-S. The file transfer begins after the ASCII transfer protocol and the filename are specified. A status line is displayed on the screen during the file transfer. The file transfer can be stopped by pressing the Escape key.

Once the file has been downloaded to the instrument, it can be executed directly from RAM or saved to EEPROM. Executing from RAM allows the new program to be tested prior to storing to EEPROM. Only once the program has been thoroughly tested should it be saved to EEPROM.

6.3 Configuring Procomm Plus for Windows

Windows has become the de facto standard operating system for x86 based machines. One terminal program able to operate the spectroradiometer under Windows is Procomm Plus for Windows.

Procomm Plus for Windows is started by double clicking the Procomm icon. Procomm must be configured prior to use with the spectroradiometer. Configuration of Procomm Plus is accomplished using menus and the setup procedure is only required the first time Procomm is invoked. The process begins by defining a direct connection to the serial port where the spectroradiometer is attached. Click 'Options' from the Procomm menu bar, select 'System Options' and click the 'System' tab. Select 'Modem Connection' and choose not to automatically detect a modem. Select the first choice in the list, 'Dial-Up Networking Serial Cable Between Two Computers'.

The serial port settings are defined from the Data Terminal screen. This window is similar to a conventional terminal. The blue center area displays text received from the radiometer and characters typed on the keyboard. The options bar under this window selects the communication port parameters. Click on the desired parameters and set the port for 19,200 baud, eight data bits, one stop bit and no parity. Press the space bar one time and the opening menu will be displayed.

The last parameter to configure is the file transfer protocol used for downloading a new program to the spectroradiometer. The screen is accessed by selecting the OPTIONS – DATA OPTIONS – GENERAL from the main window. Select the options shown in Figure 6.2

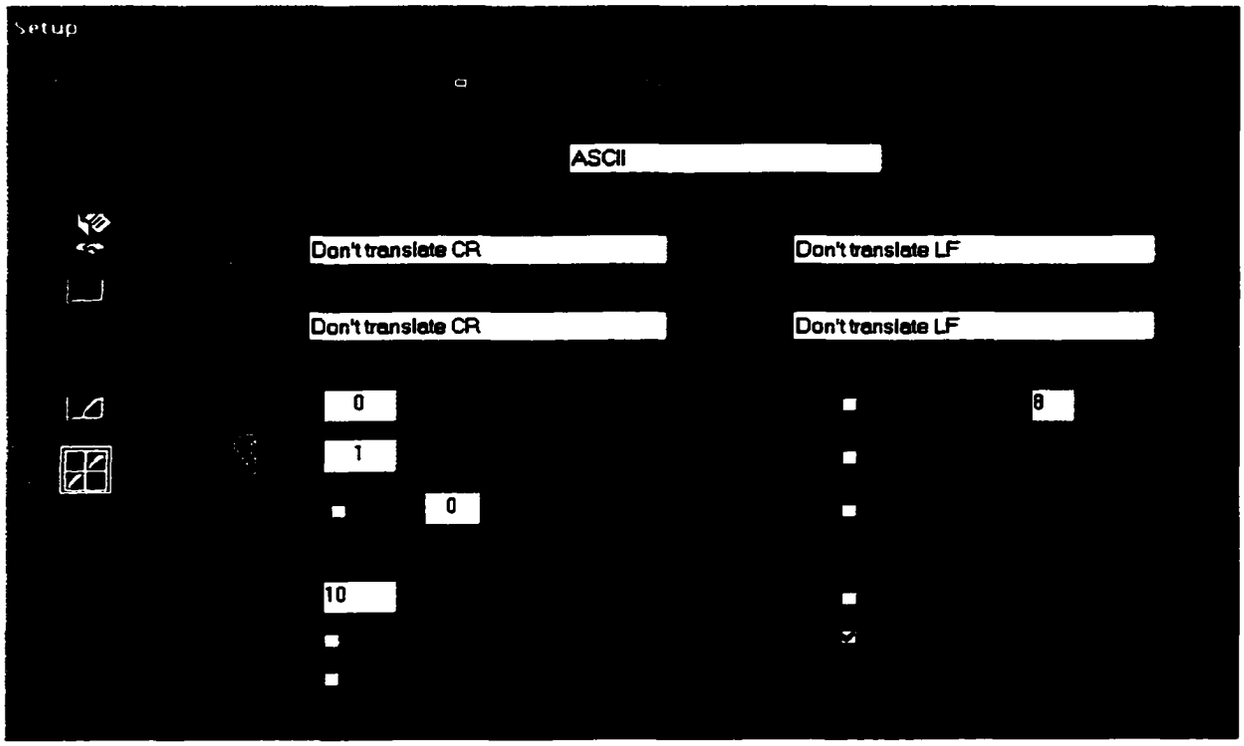


Figure 6.2 Setup Screen

6.3.1 Receiving Data Using Procomm

Recording data sent to Procomm is accomplished using capture files. A capture file is created using the DATA – CAPTURE FILE option from the main bar. When data capture is enabled anything sent to the terminal window or typed on the keyboard will be written to the named file. Selecting the Data Capture option a second time will stop the data capture. A name for the data capture file is specified from the setup menu, Figure 6.3.

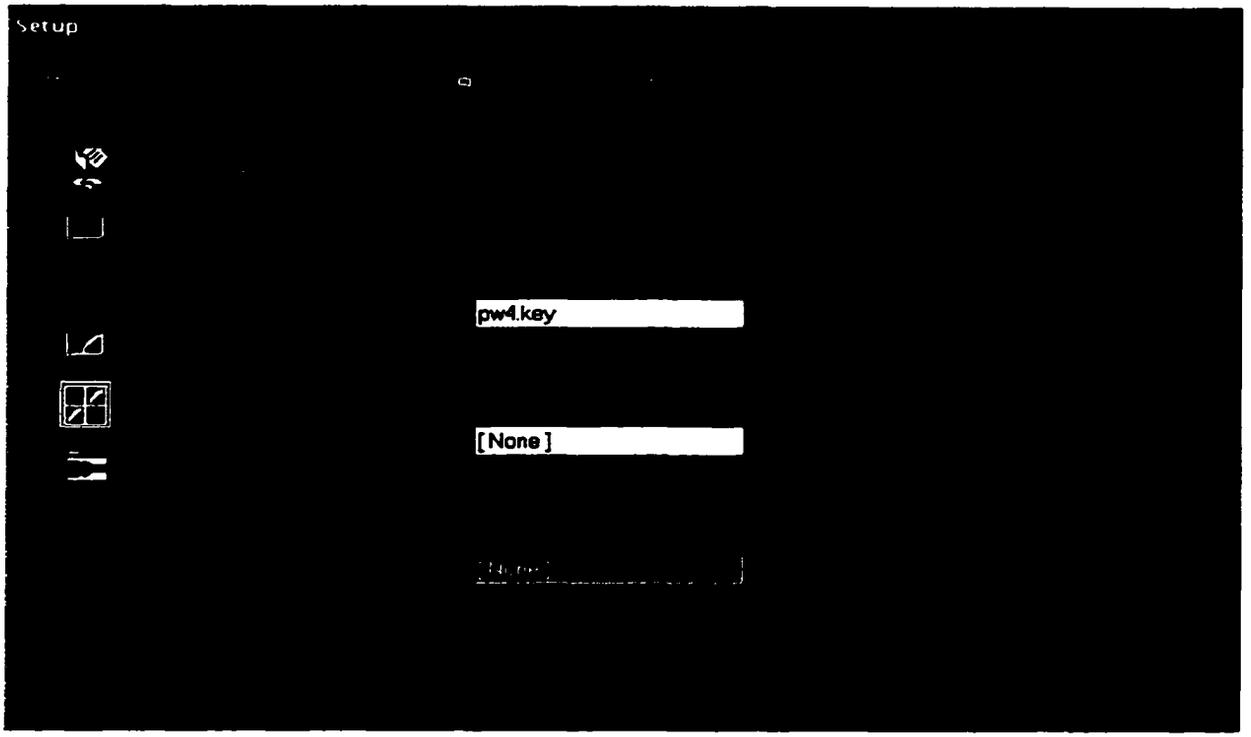


Figure 6.3 Capture File Naming

6.3.2 Downloading Files To The Spectroradiometer Using Procomm

Sending a program to the instrument using Procomm follows the same procedure as Telix. The new program is sent to the instrument by first selecting the download program option from the main spectrometer menu and then the DATA – SEND FILE command can be issued to Procomm. A progress window is displayed during the download. After the download has finished, a software reset is performed to activate the new program.

6.4 Analysis and Report Generation

The Host Computer receives and stores the data taken from the spectroradiometer. The received the data can then be analyzed and displayed. There are a number of

commercial software products available for displaying and manipulating the data. Two particular packages will be discussed; it should not be inferred that these programs are the only ones that can be used, but rather that they are a representative sample of the types of software packages that are available. The two packages available in the lab are EXCEL and Math Cad.

Excel is a spreadsheet program that organizes the data in a matrix of cells. Each pixel data point will be stored in a separate cell. The matrix of cells will be organized having the rows containing the entire data set taken during a particular integration time sample and with the columns representing the different wavelengths.

Once the data is in the spreadsheet matrix it can be graphed. Each row, one complete set of data, could be displayed individually as a scatter diagram or multiple rows could be graphed as a three dimensional surface.

Table 6.1 contains a hypothetical set of atmospheric data and Figure 6.4 is the plot of the data from Excel. This data set has been reduced in size for convenience; an actual data set could have over 800 column entries. The first row contains the wavelength information for successive measurements. The following rows contain the data measured and recorded by the spectroradiometer. This simple example has only one scan of data. An actual measurement could have about 500 columns and 300 rows of data.

Table 6.1 Hypothetical Atmospheric Data

300	400	500	600	700	800	900	1,000	1,100
45	80	95	97	95	85	70	65	50

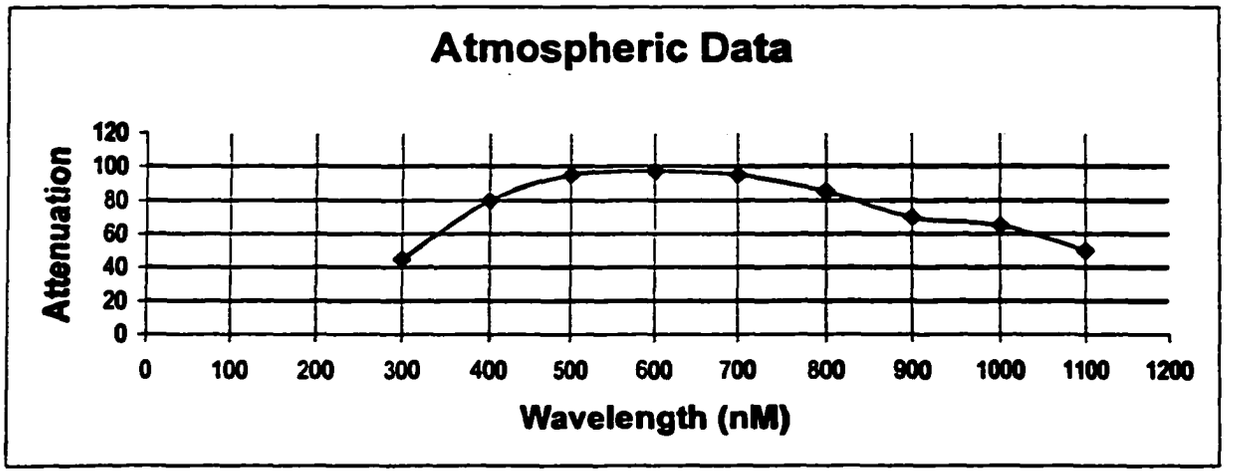


Figure 6.4 Plot Of Hypothetical Atmospheric Data

6.4.1 Math Cad

Math Cad is a tool that enhances our ability to analyze the data from the spectroradiometer. The data from the spectroradiometer can be read into Math Cad, various operations performed on the data, and then the results can be plotted or incorporated into a report.

The data from a hypothetical capture is read into the matrix, Value. The first row contains the wavelength where the measurement was made for all values under the particular column. The remaining five rows contain the atmospheric data, Figure 6.5.

Measured Values from Spectroradiometer

$$\text{Value} := \begin{bmatrix} 300 & 400 & 500 & 600 & 700 & 800 & 900 & 1000 & 1100 \\ 45 & 80 & 95 & 97 & 95 & 85 & 70 & 65 & 50 \\ 44 & 78 & 93 & 99 & 98 & 88 & 75 & 66 & 54 \\ 46 & 82 & 94 & 98 & 99 & 96 & 74 & 67 & 53 \\ 45 & 85 & 96 & 98 & 99 & 98 & 78 & 69 & 55 \\ 48 & 88 & 97 & 98 & 99 & 98 & 79 & 70 & 55 \end{bmatrix}$$

Figure 6.5 Atmospheric Values

The data stored in the Value matrix can be plotted by individual rows, Figure 6.6 or as a surface plot, Figure 6.7. Additional data processing can be performed on the data. This can include subtracting the Dark signal from the data, averaging the data from adjacent columns or averaging the values of several rows.

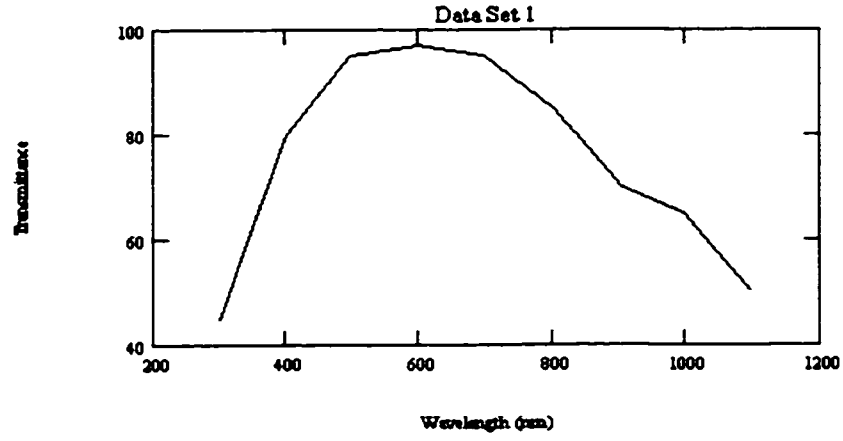


Figure 6.6 Simple Plot

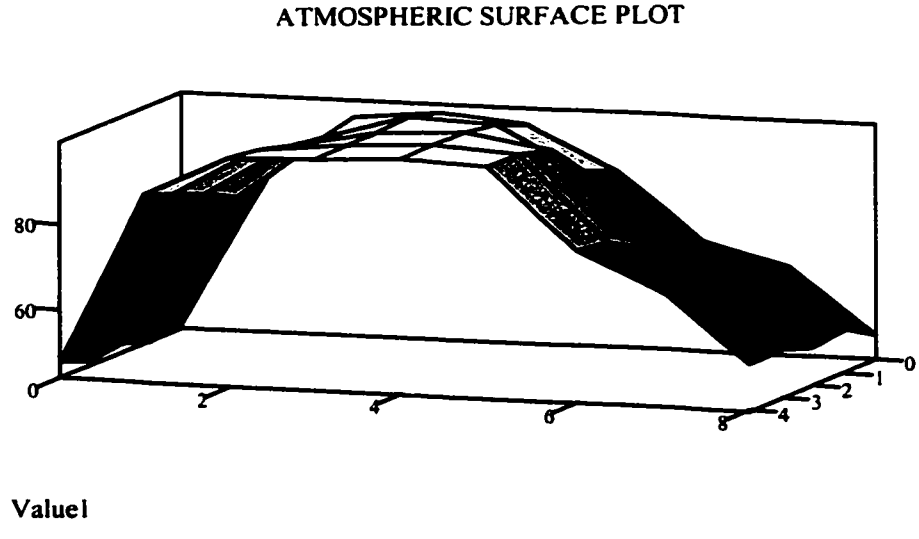


Figure 6.7 Surface Plot

CHAPTER 7

SYSTEM CALIBRATION

The ability to calibrate the instrument was an important consideration in the design of the spectroradiometer. The spectroradiometer calibration is divided into two parts, electrical calibration and optical-mechanical calibration. The optical-mechanical calibration employs both lab bench measurements and actual atmospheric retrievals.

The electrical calibration is straightforward. It verifies the reference voltage and the system clock frequency. The optical calibration is difficult to perform and more involved than the electrical system calibration. The lens must be adjusted to focus the incoming light on the diffuser, the CCD must be correctly placed in the dispersal beam of the spectrograph for pixel alignment with respect to wavelength, the edges of the optical filter must be located, and the overall spectroradiometer transmittance must be measured.

7.1 Electrical Calibration

The electrical calibration begins by verifying the system clock frequency. All of the timing for the instrument is derived from the system clock. Timing calibration is accomplished by measuring the frequency of the CLOCKOUT pin of the processor. The

frequency should be twelve megahertz. The system clock frequency is not a critical parameter but it must be in within 1 percent for the baud rate to be set correctly.

The second step for the electrical calibration is to insure the 5 volt reference is set accurately because all of the unit measurements are made with respect to this reference voltage. Reference voltage calibration is performed by adjusting the two 10-turn potentiometers while measuring the +5 volt reference. One potentiometer adjusts the zero offset and the other adjusts the gain. The voltmeter must have a resolution of better than 50 microvolts to insure 16-bit accuracy.

The ADC does not require manual calibration; it is performed by on chip circuitry. ADC calibration is initiated automatically at power up and under software control during tracker movement intervals. The converter has 10 times the accuracy required for the dynamic range of the CCD. From the ADC forward, the signal is treated in digital form and there is sufficient word size to avoid rounding errors.

There are additional tests that are performed to insure proper operation of the electrical system. These tests require diagnostic software be downloaded and run on the embedded processor. The first set of tests verifies the operation of the processor and integrity of the memory. Three programs are used to test the ADSP2101 processor, the internal memory and external memory; they are named DIAG_PROC, DIAG_INTMEM, and DIAG_EXTMEM, respectively. A pass message will be printed on the terminal if the specific test successfully completes and control will be returned back to the main

spectrometer menu. If a fault is detected the diagnostic program will display a message on the terminal and control will be returned to the main menu, if possible.

The final electrical system test substitutes the CCD with a standard reference voltage. A utility program called TEST_ADC is downloaded into the instrument and executed. A standard cell or other reference source is connected to the ADC input terminals in place of the CCD and the voltage measured by the ADC will be displayed on the host terminal.

The voltage monitoring program, TEST_ADC, will read the ADC and display the results, no signal averaging will take place. The values will be displayed in approximately 0.5 second intervals on the host terminal. When finished viewing the ADC values, remove power from the instrument and disconnect the standard cell. The radiometer will re-boot using the default control program when the power is restored.

7.2 Optical Calibration

The optical calibration is more involved than the electrical calibration. The optical filter stack is first bonded to the CCD and the number of the pixel or pixels where the two pieces of glass meet on the filter stack is recorded. The second step is to register the position of the CCD in the dispersal beam of the diffraction grating. Third, the light from the entrance optics is focused on the diffuser. The final step of the optical calibration is to determine the overall spectrometer transmittance.

7.2.1 CCD/Optical Filter Alignment

The first step in the calibration process is to bond the higher order optical filter to the CCD. The optical filter is comprised of three glass pieces, Figure 7.1. Once the filter is bonded to the CCD, the pixel or pixels where the WG-295 glass filter meets the OG-570 glass filter must be determined. The value read at these pixels will be discarded from actual measurements. This pixel or pixels is located in the middle of the CCD at about pixel number 880 which corresponds to approximately 600 nm.

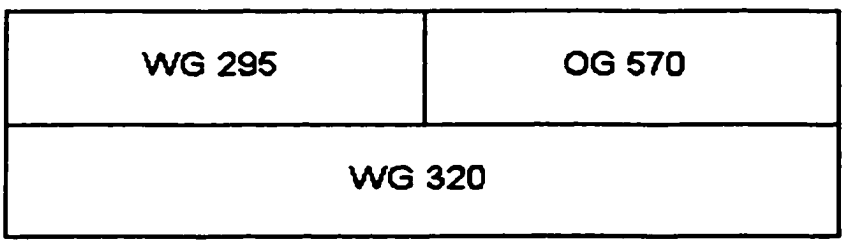


Figure 7.1 Optical Filter

The optical filter calibration procedure begins with the spectrograph cover off and the mirrored grating and entrance lens covered. The CCD, with optical higher-order filter attached, is placed in the CCD mount on the spectrograph. Diffuse sunlight is allowed to reach the CCD and the instrument is operated using simple 2-pixel averaging with the results recorded to a data file. Inspection of the data identifies the pixel or pixels that are under the junction of the two glass pieces of the optical filter. Record the location of

these pixels so they can be removed from future measurements. Uncover the mirrored grating and replace the spectrograph cover.

7.2.2 Lens Focusing

The next step in optical calibration is focusing the incoming beam on the diffuser. The top cover of the spectrograph and the entrance slit are removed. The screw fixing the lens tube is loosened to allow movement of the tube. With the entrance lens pointed at the sun, slide the tube in and out while observing the back of the diffuser. Proper alignment occurs when the spot of light on the diffuser is brightest. Tighten the lens tube screw to secure this position, replace the entrance slit and cover.

7.2.3 CCD Alignment

The pixels from the CCD must be registered with respect to the dispersed light from the mirrored grating. A mercury lamp has sharp spectral lines in the 200 nm to 600 nm wavelength, Figure 7.2.

The position spectrum is shifted across the face of the detector by turning an adjustment screw located on the Spectrograph. Place the 546 nm line from the mercury lamp at pixel number 250 by adjusting the screw and operating the instrument using simple 2-pixel averaging.

Once the 546 line has been positioned, determine the position the 435 nm line. The 435 nm line should be a pixel 135. The separation between these two lines is

adjusted by sliding the assembly holding the entrance slit in or out. Once the two lines are correctly positioned the two screws are locked in place.

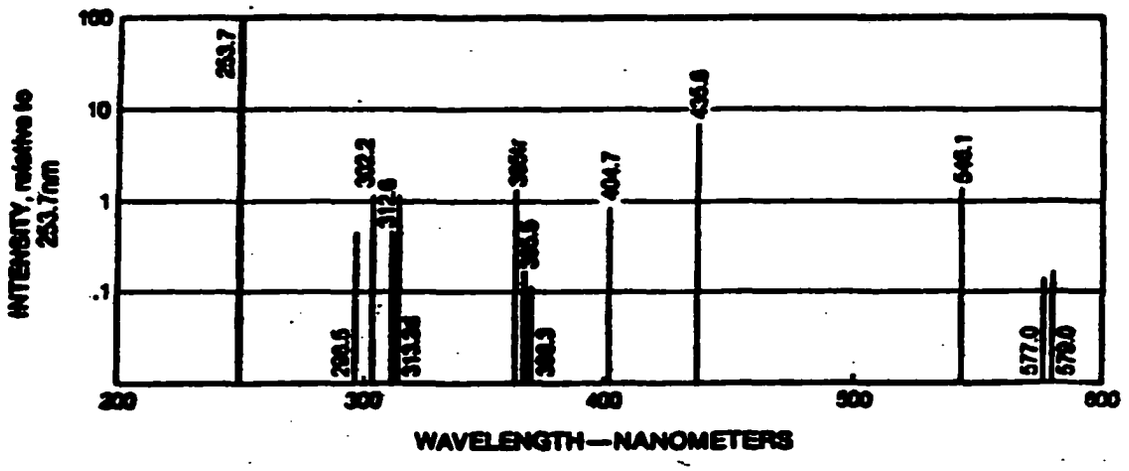


Figure 7.2 Spectral Lines of a Mercury Lamp

The position of the remaining lines of the mercury lamp above 300 nm can be verified and recorded. Other lamp sources, such as xenon or zirconium, can be used to verify the 600 nm to 1000 nm wavelength range.

7.2.4 Overall Spectroradiometer Transmittance

The overall transmittance of the system is last to be computed. One way to measure the transmittance is on the lab bench. The transmittance of the system can be determined by placing a standard lamp source in front of the spectroradiometer; run the instrument and store the converted data to a file. The scaling factor can be computed by

comparing the measured output from the instrument to the output of the source, for a particular wavelength. An interpolation map can be created from the various data points at particular wavelengths.

A second way to determine the systems transmittance would be to use the instrument to make an actual solar measurement. The data would be compared to values taken from other calibrated instruments.

CHAPTER 8

CONCLUSION

The design of this spectroradiometer has evolved three times since its inception. The processor, an ADSP-2101, is the only component that remained throughout the design cycles. The original design had many discrete components and relied on software for some timing sensitive signals. There were two SRAMs for external data memory and a EEPROM for boot memory.

The second design upgrade employed two PLDs, an Altera EPM5032 and a 22V10, to replaced the discrete logic components. This design replaced all software generated critical timing signals. The EPM5032 generated the CCD timing signals and the 22V10 decoded the fast chip select signals. The external data memory and the boot memory were combined using a SIMTEK non-voltile SRAM. The SIMTEK chip is comprised of an SRAM under a Flash memory and at application of power, the Flash is automatically copied into the SRAM.

The present design replaced the two PLDs with a single large, fast CPLD, a Lattice ispLSI 1024. It integrated the logic from the 22V10 and EPM5032 and has room for expansion. The CPLD is in circuit re-programmable using only a simple cable attached to the printer port of a PC. The CPLD was chosen to allow easy integration to new CCD detectors and ADCs.

The CPLD logic was enhanced to simplify the data bit ordering from SPORT0, the CCD charge dump controller. Now each bit of a data word corresponds to one pixel in the CCD. If a new CCD detector is to be incorporated in the spectroradiometer, only the CPLD state machine would need to be re-programmed, the DSP and Host software would remain the same.

The design allows new programs to be downloaded and executed on the instrument using the serial port. These programs could be hardware test programs, calibration programs or improved instrument control programs.

8.1 Next Generation

The design presented is not called the "final" design; it will evolve to incoporate new and improved hardware and software. The next generation instrument could integrate the UART into the CPLD and replace the ADSP-2101 with an ADSP-2181. The 2181 processor has more internal memory which would replace the two SIMTEK memories for data storage and a single byte-wide flash device would be used for boot up.

The current system uses a fixed 10 millisecond integration time interval. An enhancement would be to design an instrument that has a programmable integration timer. New FPGAs from Altera and Xilinx have internal PLLs that can be used to generate programmable clocks. These clock sources can be used to create a programmable integration timer.

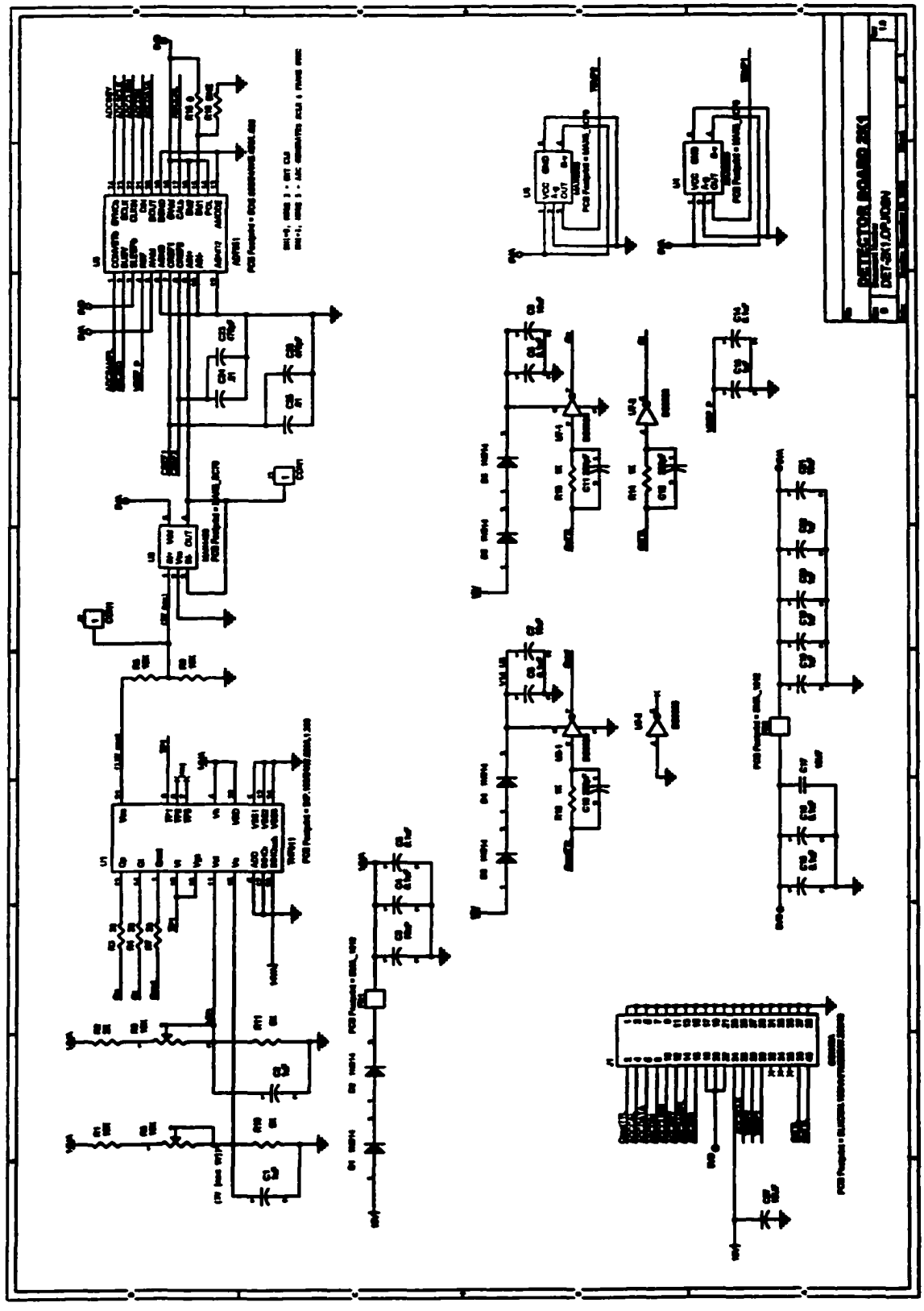
A compact flash, smart media or other memory interface could be added to store data when a host computer is not available. The data could be read out at the end of the

day when all measurements have been taken. The interface with the Host computer could be changed from a hardwired serial interface to a wireless one using a Bluetooth network.

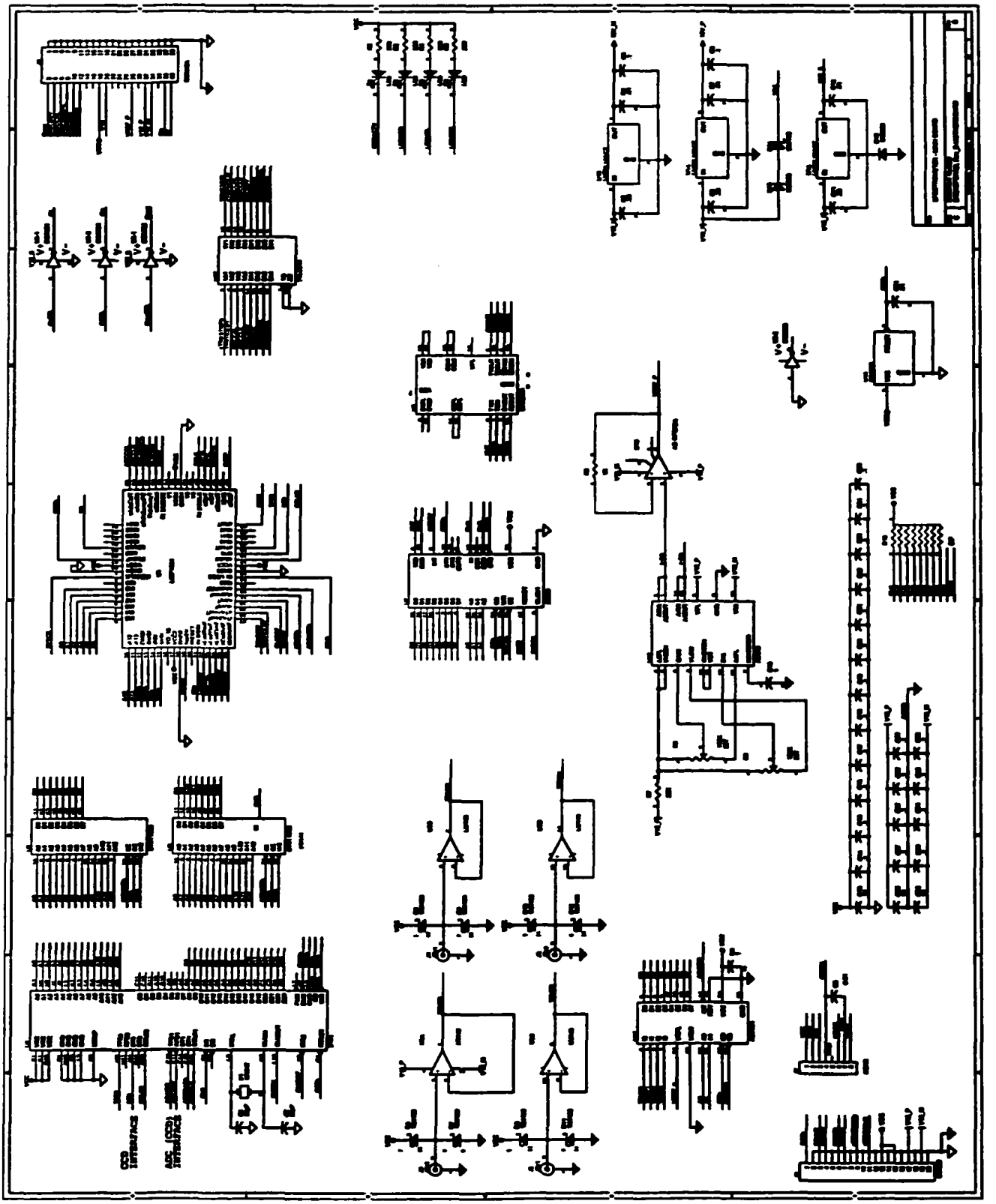
An instrument modification would be to move the spectrograph from the solar tracker and instead use a small, light weight fiber optic cable assembly on the tracker. This would allow a smaller, lower powered tracker to be used, making the instrument more portable.

Two instruments have been introduced that have similar characteristics of the spectroradiometer presented. They are from StellarNet of the United Kingdom [20] and Tristan of Germany [21]. Both units have reduced spectral range, (300 – 800 nm) and have a resolution to 1nm. Light enters the unit through an SMA 905 connector of the StellarNet and through a quatrz fiber on the Tristan unit. Neither units offer the flexibility or programmability of the spectroradiometer presented in this paper.

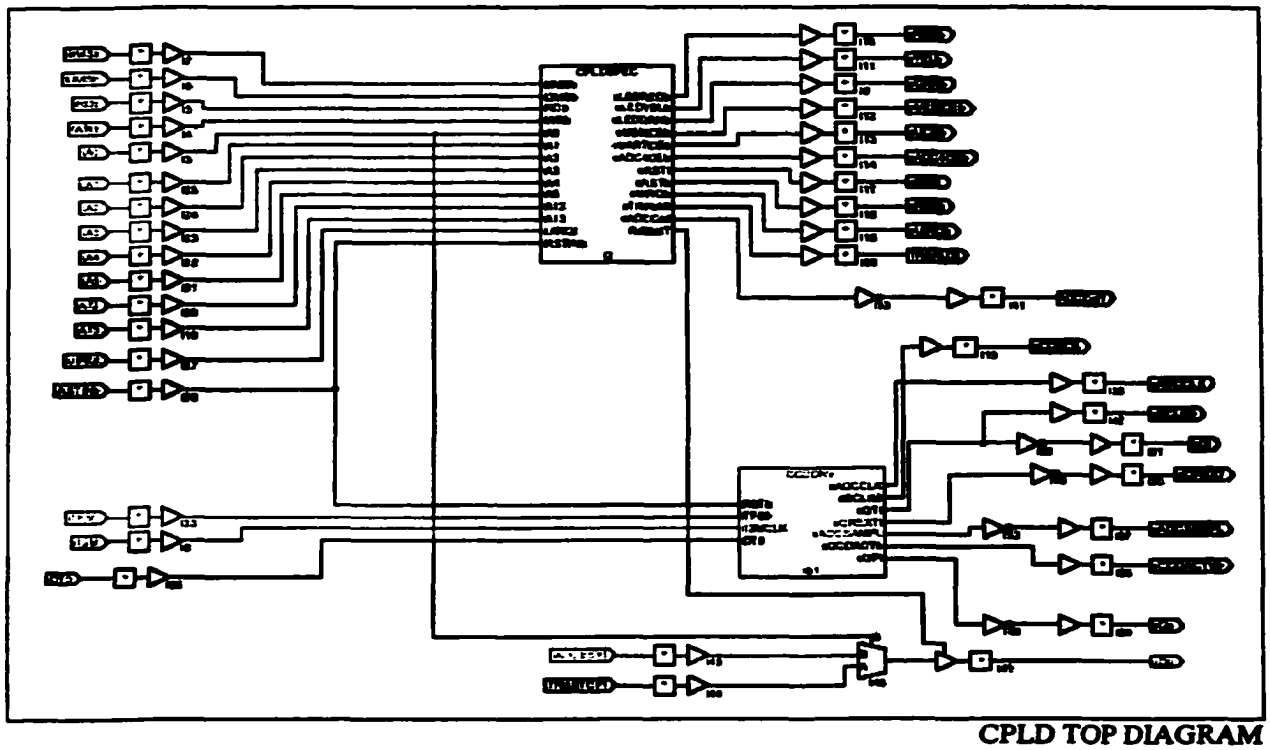
Appendix A



Appendix B



Appendix C



CPLD TOP DIAGRAM

```
MODULE CCDDRV
INTERFACE (i12MCLK,iTFS0,iDT0,iRSTb ->
[oQPt,oQTt,oQREXTt,oSCLK0,oADCCLK,oCCDACTb,oADCSAMPL]);

TITLE 'Generates CCD and ADC signals'
        i12MCLK  PIN;                          "Master 12 MHz clock in
        iTFS0    PIN;                          "SPORT 0 Frame Sync, part of dump charge logic
        iDT0     PIN;                          "SPORT 0 Data, Indicates to dump charge this clock
        iRSTb    PIN;                          " Active low RESET in

        oQPt     PIN istype 'reg,buffer';   "CCD Integrate pulse
        oQTt     PIN istype 'reg,buffer';   "CCD Transport clock, valid data on each edge
        oQREXTt  PIN istype 'reg,buffer'; "CCD reset output buffer

        oSCLK0   PIN;                          "Clock to the 2101 SS port 0
        oADCCLK  PIN istype 'reg_d';           "ADC clock, 2 MHz derrived from 12 MHz clock in
        oCCDACTb PIN istype 'reg,buffer';      "active low LED enable - we're operational
        oADCSAMPL PIN istype 'reg,buffer';     "ADC sample now signal

" Buried Logic - use 'NODE' instead of 'PIN'

" Storage for counter to generate 2 MHz clock from 12MHz clkin
        ADCck2..ADCck0  NODE istype 'reg_d';
        ADCcnt = [ADCck2..ADCck0];


        CCDck5..CCDck0  NODE istype 'reg_d';

        CCDreg state_register;
        CCDcnt = [CCDck5..CCDck0];

"CCD State Values...
CCD_WAIT, CCD_QP, CCD_GO, CCD_DONE     state;

" Equivalence
        X = .X.;

equations
"RESET conditions - put everything in a known state
oCCDACTb.ASET = !iRSTb;

oQPt.ACLR = !iRSTb;
oQTt.ACLR = !iRSTb;
oQREXTt.ACLR = !iRSTb;
oADCSAMPL.ACLR = !iRSTb;
CCDcnt.ACLR = !iRSTb;
ADCcnt.ACLR = !iRSTb;


"Generate a 6 MHz clock from the input 12 MHz clock for the ADC
oADCCLK   = !oADCCLK.fb;
oADCCLK.clk = i12MCLK;


"Generate a 2 MHz clock from the input 12 MHz clock for the CCD
```

```
ADCcnt.clk = i12MCLK;
when ADCcnt < 3 then { oSCLK0 = 0; ADCcnt := ADCcnt +1;}
else when ((ADCcnt >= 3) & (ADCcnt <5)) then { oSCLK0 = 1; ADCcnt := ADCcnt +1;}
else when ADCcnt == 5 then { oSCLK0 = 1; ADCcnt := 0;}


" CCD control section


" Definitions for inter line control
CCDreg.clk = oSCLK0;

[CCDcnt].clk = oSCLK0;
[oCCDACTb, oADCSAMPL].clk = oSCLK0;
[oQPt,oQTt,oQREXTt].clk = oSCLK0;


state_diagram CCDreg;
        State CCD_WAIT: " Wait to start CCD timing
                oADCSAMPL := 0;

                IF ( (iTFS0 == 1) & ( CCDcnt == ^h20) ) THEN CCD_QP WITH
                        {
                        oQPt := 0;
                        oQTt := 0;
                        CCDcnt :=0;
                        oADCSAMPL := 0;
                        }

                ELSE IF (CCDcnt < ^h20 ) THEN CCD_WAIT WITH
                        {
                        oQTt := 0;
                        oCCDACTb := 1;  "Indicate !in-active
                        CCDcnt:= CCDcnt + 1;
                        }

                ELSE IF (CCDcnt >= ^h20) THEN CCD_WAIT WITH
                        {
                        oQTt := 1;
                        CCDcnt:= CCDcnt + 1;
                        oCCDACTb := 1;  "Indicate !in-active
                        }

                ELSE CCD_WAIT WITH
                        {
                        oQPt := 0;
                        oQTt := oQTt.fb;
                        oQREXTt := 0;
                        oCCDACTb := 1;  "Indicate !in-active

                        CCDcnt:= CCDcnt + 1;
                        }

        State CCD_QP: " Start the pattern with QP high for 32 then low for 32
                IF (CCDcnt < ^h20 ) THEN CCD_QP WITH
```

```
                {
                oQTt := 0;
                oQPt := 0;
                CCDcnt:= CCDcnt + 1;
                }
        ELSE IF ((CCDcnt >= ^h20) & (CCDcnt < ^h3f)) THEN CCD_QP WITH
                {
                oQTt := 1;
                oQPt := 1;
                CCDcnt:= (CCDcnt.fb + 1);
                }

        ELSE CCD_GO WITH
                {
                oQTt := 1;
                oQPt := 1;
                oADCSAMPL := 0;
                CCDcnt:= 0;
                }

State CCD_GO: " Start the pattern
        oCCDACTb := 0;

        oQPt := 0;

        when ((CCDcnt >= ^h2)&(CCDcnt <= ^h4)) then { oADCSAMPL := iDT0 }
        else { oADCSAMPL := 0}

        when ((CCDcnt >= ^h7) & (CCDcnt <= ^h9)) then {oQREXTt := iDT0}
        else {oQREXTt := 0}


        IF (CCDcnt < ^h20 ) THEN CCD_GO WITH
                {
                oQTt := 0;
                CCDcnt:= CCDcnt + 1;
                }
        ELSE IF ((CCDcnt >= ^h20) & (iTFS0 == 1)) THEN CCD_GO WITH
                {
                oQTt := 1;
                CCDcnt:= CCDcnt + 1;
                }


        ELSE CCD_DONE WITH
                {
                oQTt := 1;
                CCDcnt:= CCDcnt + 1;
                }

State CCD_DONE: " EXIT
        IF (CCDcnt == 0 ) THEN CCD_WAIT WITH
                {
                oQPt := 0;
                oQTt := 0;
```

```
                    oQREXTt := 0;
                    oCCDACTb := 1;  "Indicate !in-active
                    }
                ELSE CCD_DONE WITH
                    {
                    oQTt := 1;
                    CCDcnt:= CCDcnt + 1;
                    }

async_reset CCD_WAIT: !iRSTb;

END
```

```
MODULE CPLDSPEC
INTERFACE (iA0,iA1,iA2,iA3,iA4,iA5,iA12,iA13,iDMSb,iBMSb,iWRb,iRDb,iRSTINb,iUIRQt ->
        [oLEDREDb,oLEDYELb,oLEDGRNb,oMEMCEb,oUARTCEb,oADC4CEb,oRSTt,oRSTb,Ouir
        Qb,
     oTrkHoldt,oADCCalt,RdStatT]);

TITLE 'SPEC 2K ABLE CPLD'
        iA0     PIN;    "Addresses from ADSP2101
        iA1     PIN;
        iA2     PIN;
        iA3     PIN;
        iA4     PIN;
        iA5     PIN;
        iA12    PIN;
        iA13    PIN;
        iDMSb   PIN;
        iBMSb   PIN;
        iRDb    PIN;
        iWRb    PIN;

        oLEDREDb PIN istype 'reg,invert';
        oLEDYELb PIN istype 'reg,invert';
        oLEDGRNb PIN istype 'reg,invert';

        oMEMCEb         PIN;
        oUARTCEb PIN;
        oADC4CEb PIN;

        iRSTINb         PIN;
        oRSTt   PIN;
        oRSTb   PIN;

        iUIRQt  PIN;
        oUIRQb PIN;
        oTrkHoldt PIN istype 'reg,buffer';
        oADCCalt PIN istype 'reg,buffer';

        RdStatT  PIN;

" Equivalence
        X = .X.;

        q0      NODE istype 'reg,invert';


"CCD Clock generation definitions
        sreg  = [q0];

"State Values...
        A = 0; B = 1;

" Bus Definitions
        Addr  = [iA13,iA12,X,X,X,X,X,X,iA5,iA4,iA3,iA2,iA1,iA0];
        Adr2  = [iA1,iA0];
equations
```

```
" Define the reset states
        oTrkHoldt.ACLR = !iRSTINb;
        oADCCalt.ACLR  = !iRSTINb;

        oLEDREDb.ASET = !iRSTINb;
        oLEDYELb.ASET = !iRSTINb;
        oLEDGRNb.ASET = !iRSTINb;

" Define the clocks for the registers
        oLEDREDb.CLK =  iDMSb # iWRb # !(iA13 & iA12 & !iA5 & iA4 & !iA3 & !iA2);
        oLEDYELb.CLK =  iDMSb # iWRb # !(iA13 & iA12 & !iA5 & iA4 & !iA3 &  iA2);
        oLEDGRNb.CLK =  iDMSb # iWRb # !(iA13 & iA12 & !iA5 & iA4 &  iA3 & !iA2);
        oTrkHoldt.CLK = iDMSb # iWRb # !(iA13 & iA12 & !iA5 & iA4 &  iA3 &  iA2 & !iA1);
        oADCCalt.CLK = iDMSb # iWRb #  !(iA13 & iA12 & !iA5 & iA4 &  iA3 &  iA2 &  iA1);

        oMEMCEb = iBMSb & (iDMSb # !(Addr < ^h2000));
        oUARTCEb = iDMSb # !((Addr >= ^h3000) & (Addr <= ^h3007)) # (iWRb & iRDb);
        oADC4CEb = iDMSb # !((Addr >= ^h3008) & (Addr <= ^h300F)) # (iWRb & iRDb);

" The 'Real-Thing'
        oRSTt = !iRSTINb;
        oRSTb =  iRSTINb;

        oUIRQb = !iUIRQt;

        RdStatT = !iDMSb & !iRDb & iA13 & iA12 & iA5 & !iA4;  "Addr = 0x302X

" Decode the CPLD features
        WHEN (Adr2 == ^h0) THEN oLEDREDb := 0;                  " BASE = 0x3010
        WHEN (Adr2 == ^h1) THEN oLEDREDb := 1;
        WHEN (Adr2 == ^h2) THEN oLEDREDb := !oLEDREDb.FB;
        WHEN (Adr2 == ^h3) THEN oLEDREDb :=  oLEDREDb.FB;

        WHEN (Adr2 == ^h0) THEN oLEDYELb := 0;                  " BASE = 0x3014
        WHEN (Adr2 == ^h1) THEN oLEDYELb := 1;
        WHEN (Adr2 == ^h2) THEN oLEDYELb := !oLEDYELb.FB;
        WHEN (Adr2 == ^h3) THEN oLEDYELb :=  oLEDYELb.FB;

        WHEN (Adr2 == ^h0) THEN oLEDGRNb := 0;                  " BASE = 0x3018
        WHEN (Adr2 == ^h1) THEN oLEDGRNb := 1;
        WHEN (Adr2 == ^h2) THEN oLEDGRNb := !oLEDGRNb.FB;
        WHEN (Adr2 == ^h3) THEN oLEDGRNb :=  oLEDGRNb.FB;

        WHEN (iA0 == ^h0) THEN oTrkHoldt := 0;                  " 0x301C
        WHEN (iA0 == ^h1) THEN oTrkHoldt := 1;                  " 0x301D

        WHEN (iA0 == ^h0) THEN oADCCalt := 0;                   " 0x301E
        WHEN (iA0 == ^h1) THEN oADCCalt := 1;                   " 0x301F


END
```

REFERENCES

[1] Ehsani, Reagan, Erxleben, 1998, Design and Performance of an Automated 10-Channel Solar Radiometer Instrument, *American Meteorological Society.*

[2] Reagan, Thome and Herman, 1995, A Comparison of Columnar Water Vapor Retrievals Obtained with Near-IR Solar Radiometer and Microwave Radiometer Measurements, *Journal of Applied Meterology,* Vol 34, No.6.

[3] Bruegge et. al., 1992, Aerosol optical depth retrievals over the Konza Prairie, *J. Geophys. Res.,* (D17), pp. 743-758.

[4] Teillet et al., 1990, Three methods for the absolute calibration of the NOAA AVHRR sensors in-flight, *Remote Sensing Environ.,* 31, pp. 105-120.

[5] Moore et. al., 1989, Application of the Langlet Plot for Calibration of Sun Sensors for the Halogen Occultation Experiment, *Optical Engineering.*

[6] Reagan et. al., 1987, Extrapolation of Earth-Based Solar Irradiance Measurements to Exoatmospheric Levels for Broad-Band and Selected Absorption-Band Observations, *IEEE Transactions on Geoscience and Remote Sensing,* Vol. GE-25, No. 6.

[7] Shaw G.E., J.A. Reagan and B.M. Herman, 1973, Investigations of Atmospheric Extinction Using Direct Solar Radiation Measurements with a Multiple Wavelength Radiometer, *Journal of Applied Meteorology,* 12, pp.1401-1407.

[8] Kneizys, et.al, 1988, Users Guide to LOWTRAN 7, Air Force Geophysics Laboratory, Report AFGL-TR-88-0177, Hanscom AFB, MA.

[9] Slater, 1980, *Remote Sensing, Optics and Optical Systems,* Addison-Wesley, Massachusetts.

[10] Kasten, F., 1966, New table and approximation formula for the relative optical airmass, *Arch. Meteor.Geophys. Bioklim.,* Vol B14, pp.206-223.

[11] Thomson Composants, 1993, CCD Products, Data Sheet.

[12] Neckel, H. and D. Labs, 1984, The Solar Radiation Between 3300 and 12500 Angstroms, *Solar Physics,* 90, 205-258.

[13] American Holographic Inc., 1990, Model 100S Spectrograph User's Manual, Data Sheet.

[14] Hecht, Zajac, 1979, *Optics*, Addison-Wesley, Massachusetts.

[15] Slater, 1980, *Remote Sensing, Optics and Optical Systems*, Addison-Wesley, Massachusetts.

[16] Smith, 1966, *Modern Optical Engineering*, McGraw-Hill, New York.

[17] RCA, 1974, Electro-Optics Handbook, Technical Series EOH-11.

[18] Analog Devices, 1993, ADSP-2100 Family User's Manual, Data Sheet.

[19] Lattice Semiconductor Corporation, 2001, ispEXPERT System, Data Sheet.

[20] StellarNet UK Limited, 2001, EPP 2000C UV/VIS Fiber Optic Spectroradiometer, Data Sheet.

[21] Photon Technology International, Inc., 2001,Tristan Spectrometer, Data Sheet.