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THE EFFECTS OF COMPENSATION ON LOAD TRANSIENT RESPONSE IN SWITCHED MODE POWER CONVERTERS

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THE EFFECTS OF COMPENSATION ON LOAD TRANSIENT RESPONSE IN SWITCHED MODE POWER CONVERTERS

by

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Date

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ABSTRACT

Using computer simulation, three loop stability compensation techniques are applied to a buck switched mode power converter to determine their effects on load transient response.

A buck converter computer model is developed and the load transient responses of three compensation techniques are simulated. The results are tabulated and evaluated to establish quidelines to aid in the design of switched mode power converters that operate under load transient conditions.

Also included are a discussion of the need for compensation and a description of the two industry used compensation techniques - dominant pole compensation and two real zero cancellation compensation; and a third, new compensation technique - two complex zero cancellation compensation. The design equations for this new compensation technique are given in the appendix and an HP41-C calculator program is listed to aid in the selection of component values for the circuit.

CHAPTER 1

INTRODUCTION

In this day and age, the quest for miniaturized systems has forced power supply design engineers to become inventive in their solutions for providing efficient power from an unrefined source to an often demanding load.

The conventional linear power supply, in which the power regulating transistor operates in a continuous conduction mode, can dissipate large amounts of power at high load currents and large input-output voltage differences. This in turn requires heavier duty power transistors and heat-sinking, both of which increase the size of the power system. Also, a larger power source (battery, for example) is necessary to provide both the necessary power to the load and the power to be dissipated (wasted) by the power supply. Thus, the higher dissipations associated with linear power supplies is detrimental to the cause of miniaturized systems.

In response to the need for smaller, more efficient power systems, the method of switched mode power conversion was developed. This method consists of applying a DC voltage to the collector of a power transistor and varying its ON-OFF duty cycle. The resulting switching waveform is

then put through an LC low pass filter, which removes the higher frequency switching components and allows the "average" or DC value to go to the load. The output voltage is sampled by an error amplifier and compared with a reference voltage. If the output voltage is not within the "error margin" allowed by the loop gain, the ON-OFF duty cycle will be varied until the output voltage falls within the desired limits. Since the power transistor is either turned-on and saturated or is cutoff (except for a brief transition between the two states), the power dissipated within the transistor itself is small. This reduces the size of the power transistor, the size of the associated heatsinking, and possibly the size of the power source. Also, since the basic switching frequency of the power transistor can be controlled, the frequency can be made high such that smaller and more efficient filtering elements can be used. To everyone involved, the solution to more miniaturized power systems seems to have been found.

As with all new discoveries, a multitude of questions follow. What are this new system's shortcomings? How can it be improved? Of the questions that I have heard asked in my several years in the power supply field, the one I have been most intrigued with is the effect of the loop stability compensation of a switched mode power supply on the load transient response. The answer to this question

is invaluable to a power supply design engineer who is given the assignment of designing a power supply with a given closed loop response and with the capability of handling a large step change in load with a very small instantaneous change in output voltage. The constraints of the required closed loop response dictate that loop compensation be used, but the effects of loop compensation on the load transient response have not, as yet, been characterized. The material following is an attempt to answer this question.

CHAPTER 2

COMPUTER MODEL

In my experience, the best way to see how a circuit will work under different operating conditions is to develop a working computer model for it and then make any changes to the model. This alleviates the problem of building the circuit and having it not work due to an incorrect design or a destructive operating condition being applied. Once the different operating conditions have been successfully modelled, the circuit can be built and the different operating conditions can be applied to it. When the testing of the circuit is complete, the original computer results can be compared with the hardware test results and adjustments can be made to the computer model to take into account any "non-ideal" component parameters that will invariably be present in the actual circuit. As a result of this philosophy, this second chapter will be concerned with the development of a computer model for the switched mode power supply topology on which I have concentrated my efforts. The circuit simulation program that will be used is called Simulation Program with Integrated Circuit Emphasis, better known as SPICE (Nagel 1975).

Source-to-Output Circuit Model

Of the three conventional SMPS topologies used throughout the industry, the one I have chosen to look at in depth is the buck power supply (or buck "converter" as they are often called), also referred to as the "chopper" or "step-down" converter. Figure 1 shows the basic source-to-output circuit of the buck converter, with the feedback circuitry not shown. The circuit consists of a power source (V_S), a power transistor (Q_1), a "catch" diode (D_1), an LC output filter and the load (R_L).

Switching States

Figure 2 shows the two switching states of the buck converter, assuming ideal properties of the transistor and diode. The transistor is switched ON and OFF as directed by the control circuitry. Figure 2a shows Q_1 ON and saturated, acting as a short circuit. This allows V_S to be applied to one side of the inductor. The voltage drop across the inductor at this time is

$$V_L = L\frac{dI_L}{dt} = V_S - V_O .$$

Therefore, the slope of the current waveform, I_L, during this time period is

$$\frac{dI_L}{dt} = \frac{V_S - V_O}{L} .$$

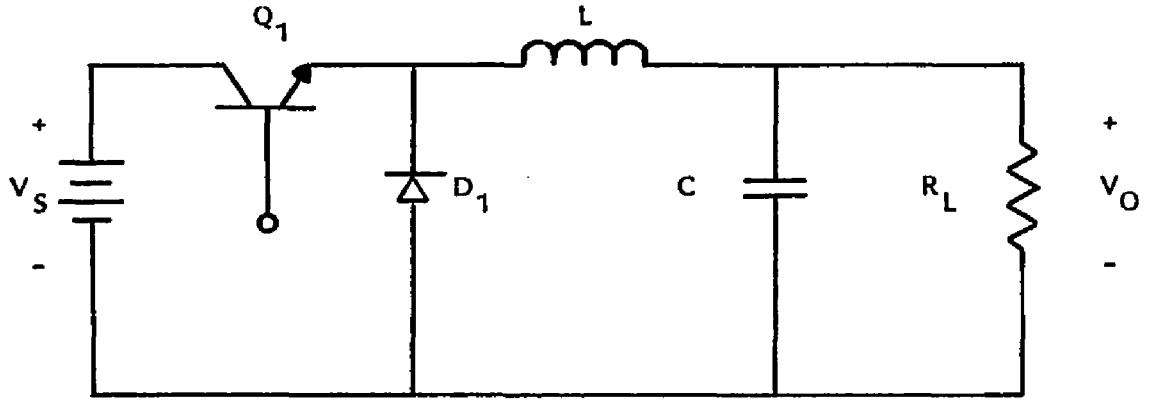
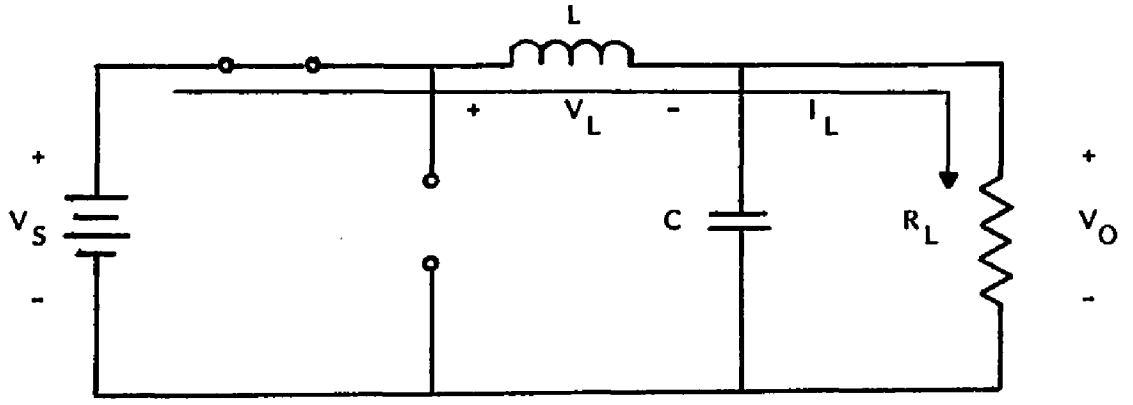
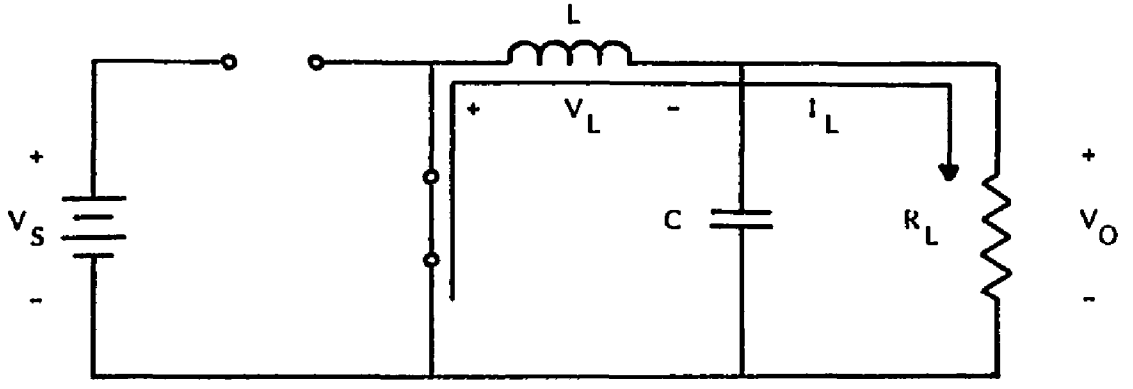


Figure 1. Buck Converter Source-to-Output Circuit



(a) Transistor Saturated



(b) Transistor Cutoff

Figure 2. Two Switching States of the Buck Converter

The time that Q_1 is ON will be denoted by

$$t_S = \frac{t_{ON}}{T_S} T_S = DT_S \ , \qquad (1)$$

where T_S is the period of one cycle of the switching frequency. Therefore, D represents the duty cycle of the converter.

Figure 2b shows Q_1 cutoff, acting as an open circuit. Because the current through the inductor, I_L, cannot change instantaneously, the voltage across the inductor goes negative until D_1 conducts. The voltage across the inductor during this switching state becomes

$$V = L \frac{dI_L}{dt} = - V_O \ .$$

The slope of the current waveform during this state becomes

$$\frac{dI_L}{dt} = - \frac{V_O}{L} \ .$$

The time that Q_1 is OFF will be denoted by

$$\begin{aligned} t_{OFF} &= T_S - t_{ON} \\ &= T_S - DT_S \\ &= (1-D)T_S \ . \end{aligned} \qquad (2)$$

Input-to-Output Switching Relationship

Because the voltage across L changes sign, the instantaneous current flowing through L must be increasing and decreasing about some steady state average value, I_{Lavg}, as shown in Figure 3. For a steady state average current to be present, the initial and final values of instantaneous inductor current must be equal. Therefore

$$I_L(T_S) = I_L(0)$$

or

$$I_L(T_S) - I_L(0) = 0 .$$

This is the integral of dI_L evaluated from t=0 to $t=T_S$

$$I_L(T_S) - I_L(0) = 0 = \int_0^{T_S} dI_L .$$

Using

$$V_L = L\frac{dI_L}{dt}$$

or

$$dI_L = \frac{V_L}{L}\,dt ,$$

therefore

$$0 = \int_0^{T_S} dI_L = \frac{1}{L}\int_0^{T_S} V_L\,dt$$

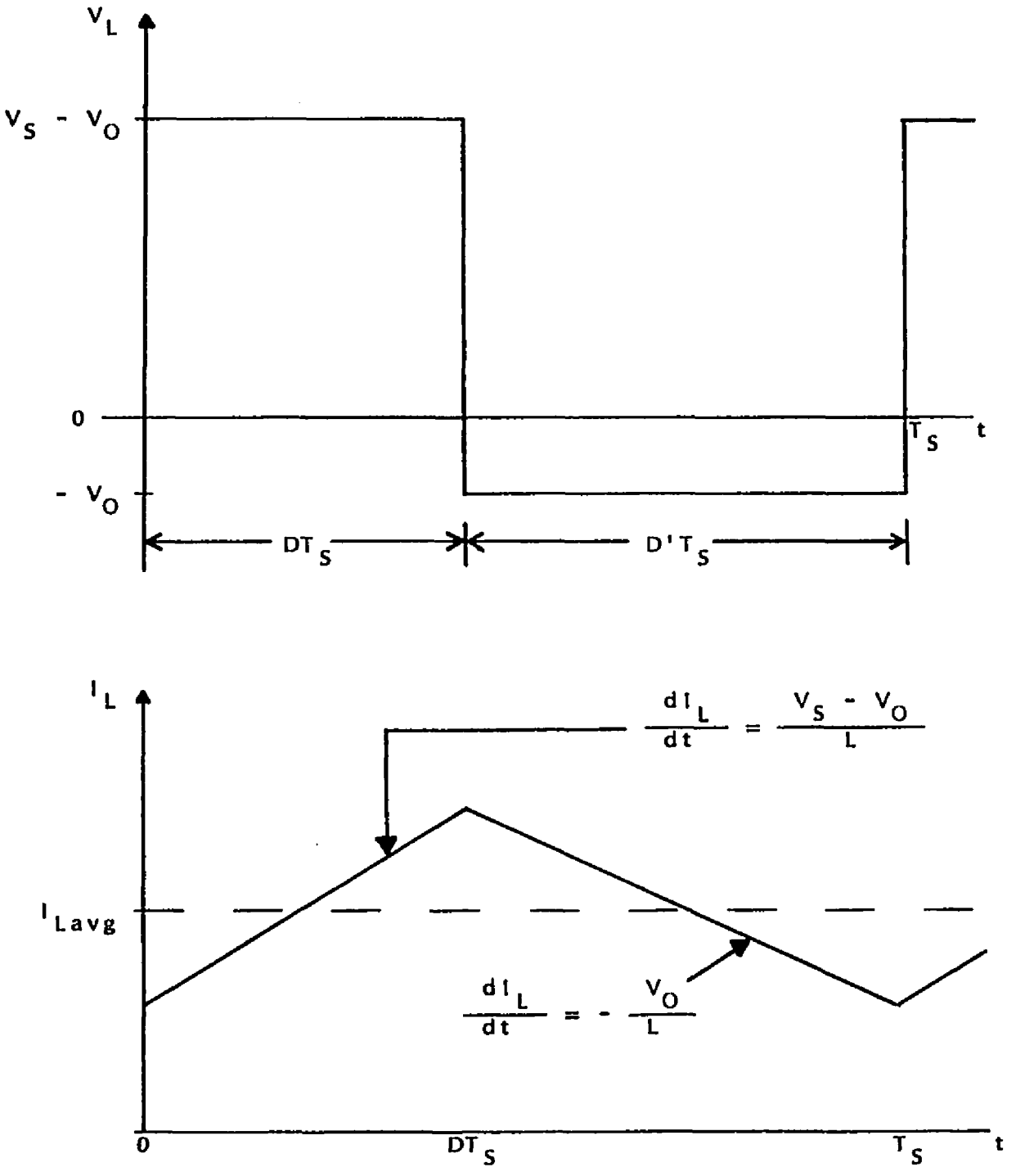


Figure 3. Voltage and Current Waveforms of L

$$= \int_0^{t_{ON}} V_L \, dt + \int_{t_{ON}}^{T_S} V_L \, dt \ .$$

From $t=0$ to $t=t_{ON}$

$$V_L = V_S - V_O$$

and from $t=t_{ON}$ to $t=T_S$

$$V_L = - V_O \ .$$

Therefore

$$0 = \int_0^{t_{ON}} (V_S - V_O) \, dt + \int_{t_{ON}}^{T_S} (-V_O) \, dt$$

$$= (V_S - V_O) t_{ON} - V_O (T_S - t_{ON}) \ .$$

From equations 1 and 2

$$t_{ON} = DT_S$$

and

$$t_{OFF} = T_S - t_{ON}$$

$$= (1-D) T_S \ .$$

Therefore

$$0 = (V_S - V_O)DT_S - V_O(1-D)T_S$$

$$= V_S DT_S - V_O DT_S \ .$$

Finally

$$V_O = DV_S \ . \qquad (3)$$

This shows that the output voltage is the duty cycle times the source voltage. Therefore, the output voltage can be as small as 0 volts ($t_{ON}=0$) or as large as the source voltage ($t_{ON}=T_S$), and any value in between. It can now be seen why the buck converter is also referred to as the "chopper" or "step-down" converter. The output voltage is a "chopped" or "stepped-down" input voltage.

Similarly, it can be shown that the output current is related to the input current by

$$I_S = DI_L \ . \qquad (4)$$

Circuit Model

Equations 3 and 4 represent a dependent voltage and a dependent current generator, respectively. These dependent generators are not only controlled by the input voltage (for the dependent voltage generator) and the load current (for the dependent current source), but they are also controlled by the duty cycle (D). For the purpose of this thesis, the source voltage, V_S, will be considered

purely DC (this model can be used with a small signal source voltage input if the transfer function of the low pass filter is taken into account) This being the case, V_S acts as a gain factor with the duty cycle being the input. Figure 4 shows the circuit model for the source-to-output. As can be seen, the necessity for modelling the transistor and diode has been eliminated with the inclusion of the dependent generators. The low pass output filter and load remain as they were before. This model will be used in subsequent sections to develop an overall circuit model.

Duty Cycle-to-Output Circuit Model

Using Figure 4 as the starting point, the duty cycle-to-output circuit model and transfer function (with V_S constant) will be developed. Pictorially, Figure 5 shows the steps in the process of obtaining the circuit model with Figure 5a a repeat of Figure 4 for ease of reference.

The duty cycle, d, is first perturbated with a small signal change, $\hat{d}$, superimposed upon the DC duty cycle, D. Thus

$$d(t) = D(t) + \hat{d}(t) .$$

This duty cycle perturbation causes a corresponding perturbation in the controlling current for the dependent

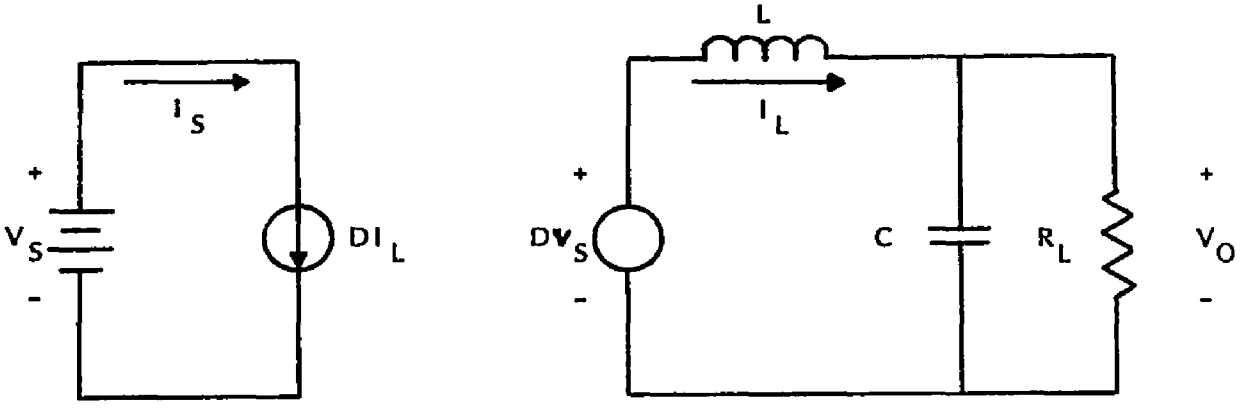
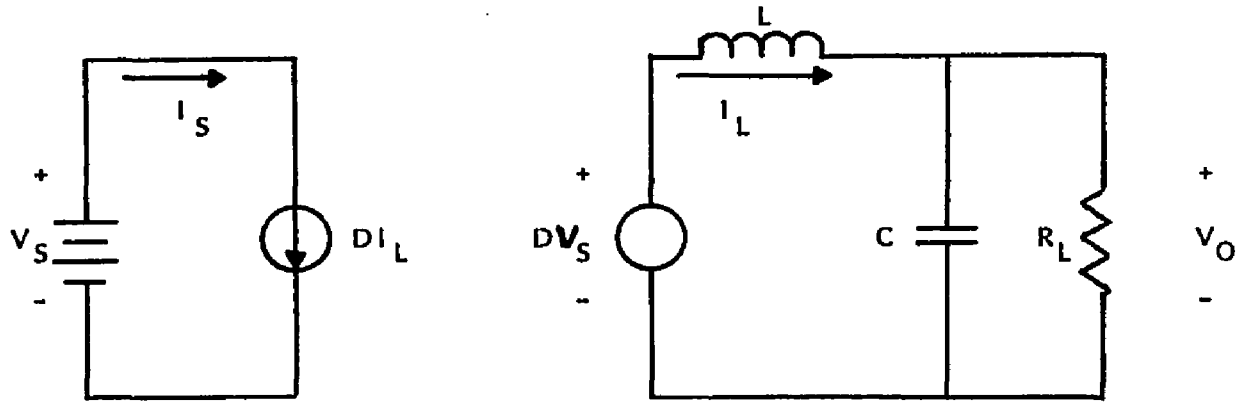
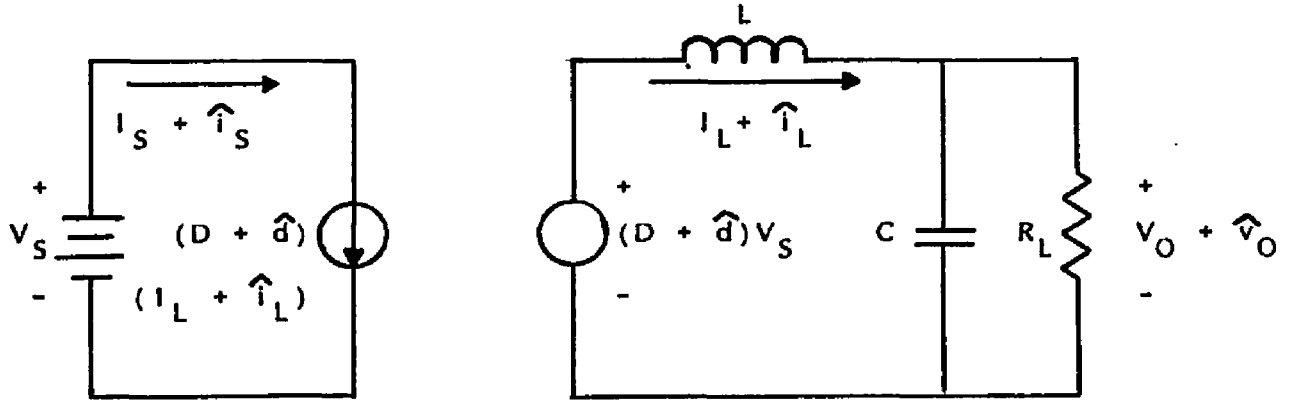


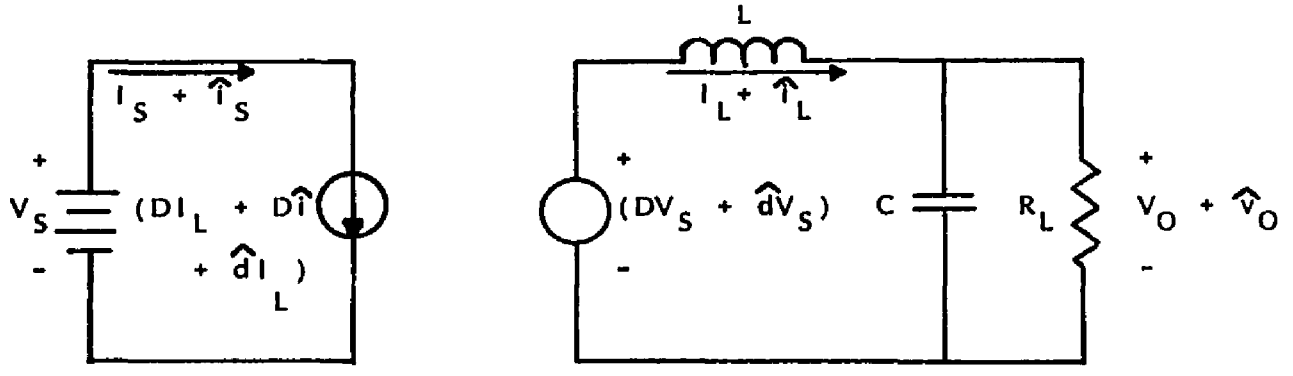
Figure 4. Buck Converter Source-to-Output Circuit Model



(a) Source-to-Output Model

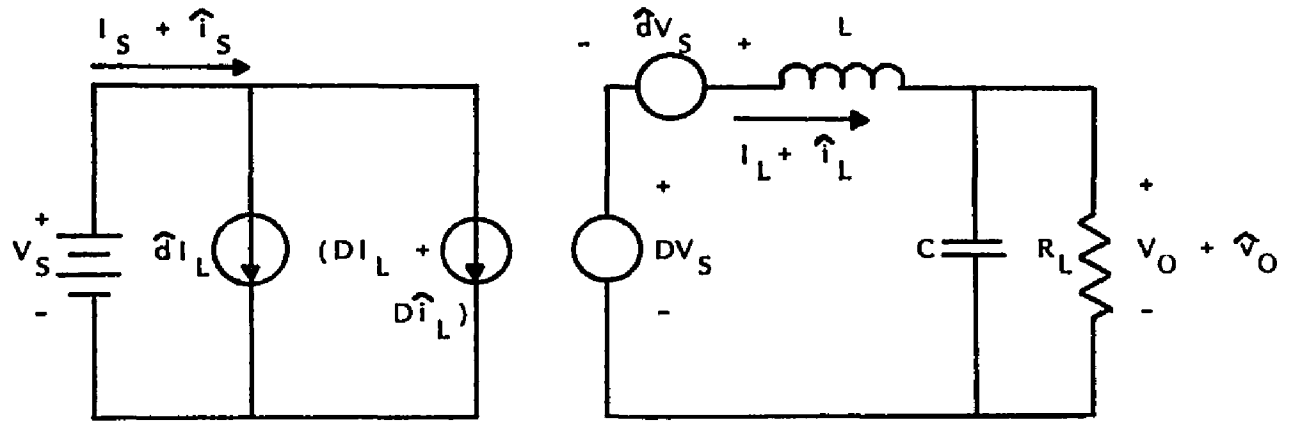


(b) Perturbation of Duty Cycle

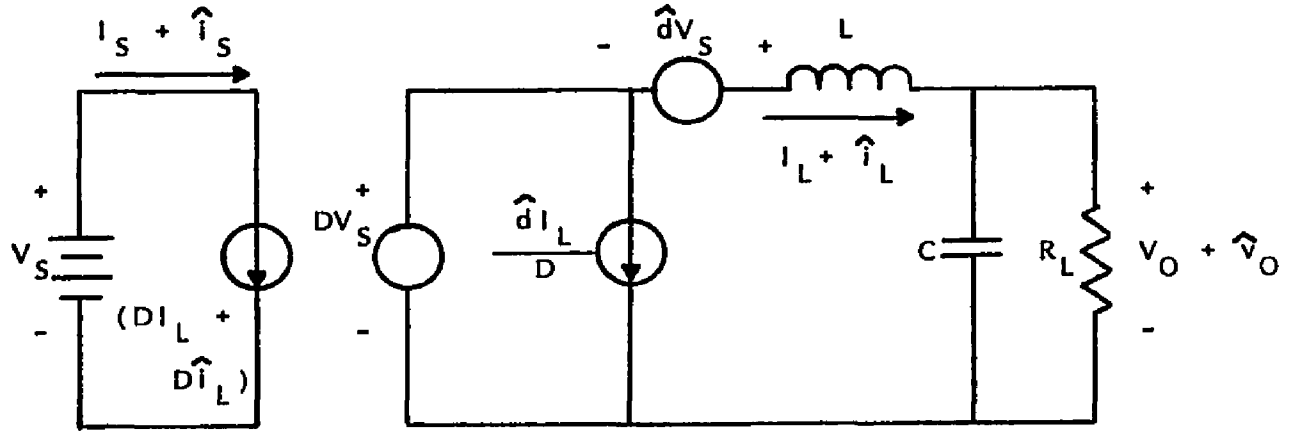


(c) Expansion and Simplification of Terms

Figure 5. Development of Duty Cycle-to-Output Circuit Model



(d) Splitting into AC and DC Generators



(e) Composite AC/DC Duty Cycle-to-Output Circuit Model

Figure 5.--Continued

current source such that

$$i_L(t) = I_L(t) + \hat{i}_L(t) \ .$$

This is shown in Figure 5b. The total perturbation is expanded as follows (with time dependence references removed for clarity)

$$\begin{aligned} di_L &= (D + \hat{d})(I_L + \hat{i}_L) \\ &= DI_L + D\hat{i}_L + \hat{d}I_L + \hat{d}\hat{i}_L \ . \end{aligned} \tag{5a}$$

and

$$\begin{aligned} dV_S &= (D + \hat{d})V_S \\ &= DV_S + \hat{d}V_S \ . \end{aligned} \tag{5b}$$

As shown by the results of the expansion in equation 5a, the duty cycle-to-output function is non-linear. This non-linear equation (and thus, the duty cycle-to-output transfer function) can be linearized by restricting the amplitude of the perturbations of the duty cycle to be small such that the terms di are negligible compared to the rest of the equation. Imposing this restriction

$$\hat{d} << D \ .$$

This forces the induced perturbation on the current to be

$$\hat{i}_L \cong 0 \ .$$

Equation 5 then reduces to

$$di_L = DI_L + \hat{d}I_L + D\hat{i}_L$$

and

$$dV_S = DV_S + \hat{d}V_S \ .$$

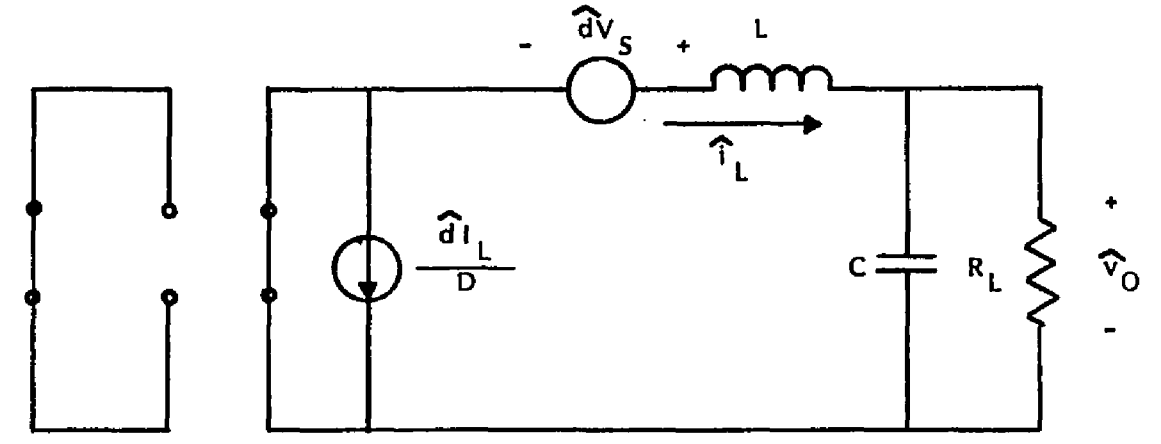
Correspondingly, the circuit shown in Figure 5b is reduced to that shown in Figure 5c.

Each dependent generator (voltage and current) can now be split into two dependent generators, an AC and a DC generator, as shown in Figure 5d. Using standard circuit techniques, the AC dependent current source is reflected to the other side of the DC dependent voltage source, as shown in Figure 5e (the techniques used to do this are the same as one would use to reflect a current source from one winding of a transformer to another, since the DC dependent generators can be thought to be circuit models for an AC/DC transformer). Figure 5e represents the final composite AC and DC duty cycle-to-output computer circuit model that will be used later, with the AC dependent generators being given the circuit symbols IPWM (dependent current generator) and EPWM (dependent voltage generator) for ease of reference.

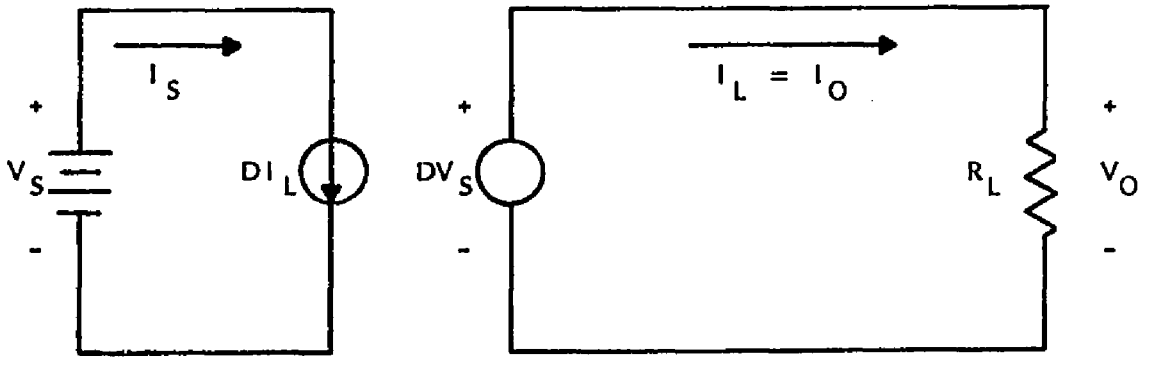
Figure 6 shows the AC and DC models broken apart, with corresponding equations

DC model

$$V_O = DV_S$$



(a) AC Duty Cycle-to-Output Circuit Model



(b) DC Duty Cycle-to-Output Circuit Model

Figure 6. AC and DC Duty Cycle-to-Output Circuit Models shown Separate

$$I_L = I_O = \frac{V_O}{R_L} = \frac{DV_S}{R_L} \quad .$$

AC model

$$\hat{V}_O = H_f \hat{d} V_S \qquad (6a)$$

$$\frac{\hat{d} I_L}{D} = \frac{\hat{d} V_O}{D R_L} = \frac{\hat{d} V_S}{R_L} \quad , \qquad (6b)$$

where H_f is the transfer function of the output filter. In the case of this particular buck converter, IPWM is bypassed by a DC dependent voltage source. This is effectively a short circuit under AC conditions. Therefore, IPWM is not necessary and not included in the duty cycle-to-output transfer function. The time that IPWM becomes critical is when there is an input filter between the DC voltage source, V_S, and the DC dependent source. This input filter can be reflected across the "AC/DC transformer", as was done previously to IPWM. Now, IPWM is no longer looking at a zero impedance DC dependent voltage generator, but has the output impedance of the input filter to contend with. Research (Middlebrook 1978) has shown that IPWM interaction with the input filter output impedance can cause power supply oscillation problems. As far as the model for this thesis is concerned, IPWM will be retained for the sake of completeness.

Control Input-to-Duty Cycle Output Circuit Model

The next step in achieving a useable circuit model is to characterize the circuitry that controls the duty cycle. This circuitry, referred to as a pulse width modulator (PWM), is shown in Figure 7. The PWM is simply a comparator that compares a triangle wave signal against the output from an error amplifier. This comparison results in a "high" or a "low" output from the PWM that turns on and off the transistor switch.

Transfer Function

Figure 8 shows the time and amplitude relationships between the two PWM inputs and its output. V_C is the output signal of the error amplifier which is the amplification of the difference between the converter output voltage, V_O, and the reference voltage, V_{REF}. For a constant V_O and V_{REF}, V_C is constant and is represented by the solid line in Figure 8. When compared with a triangle wave, this constant V_C produces a square wave with a constant duty cycle, D. Now, if V_C has a small signal variation superimposed on it such that

$$v_C(t) = V_C(t) + \hat{v}_C(t) \ ,$$

(where v_C is represented in Figure 8 by the dashed line with gradually increasing slope), then the resulting square

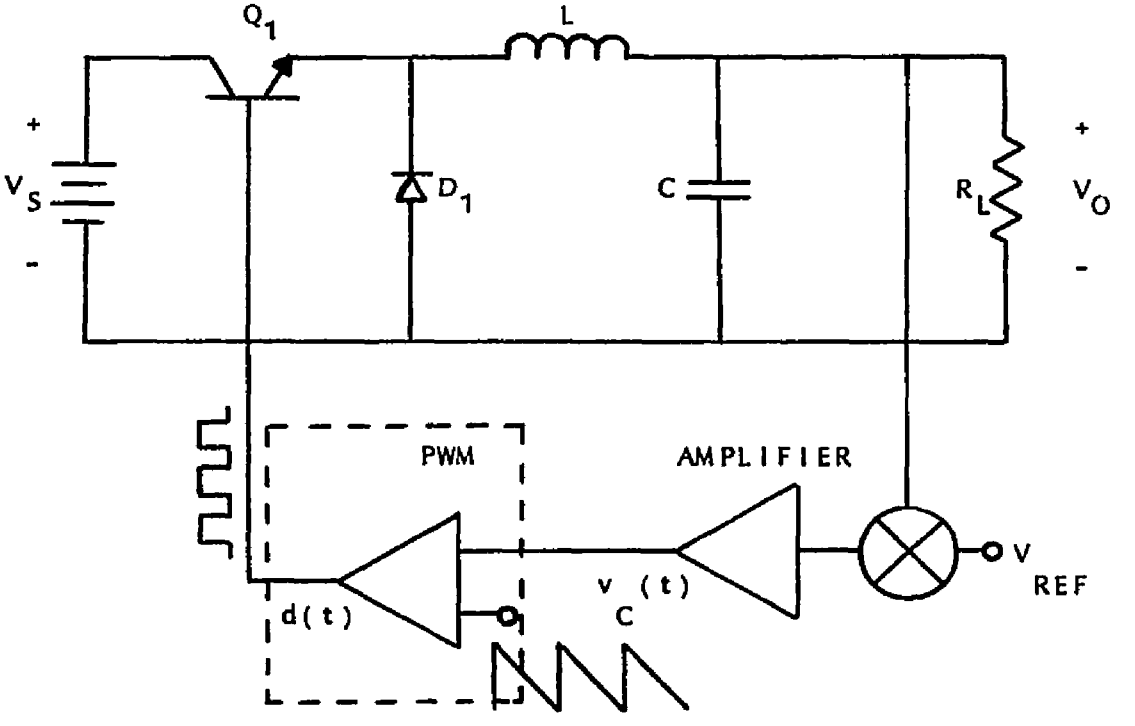


Figure 7. Pulse Width Modulator Circuitry

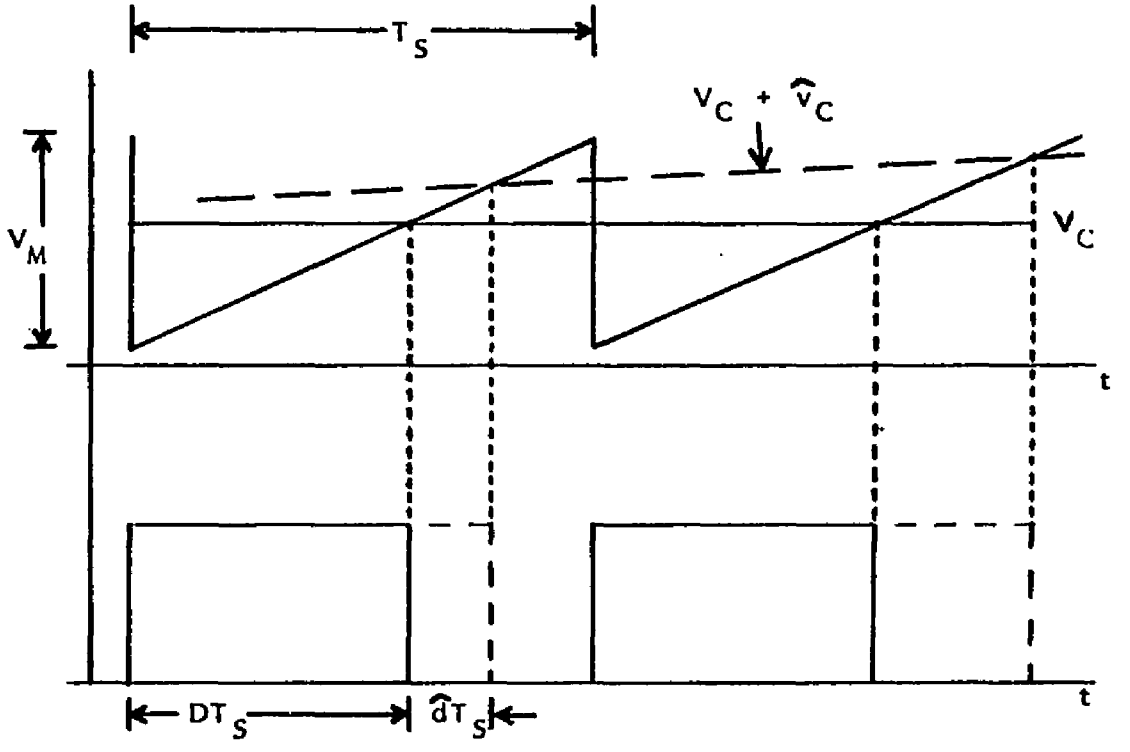


Figure 8. PWM Input/Output Relationship

wave from the comparator will have a duty cycle that varies about the DC duty cycle D such that

$$d(t) = D(t) + \hat{d}(t) .$$

As can be seen in Figure 8, the square wave output of the comparator (and consequently, the duty cycle d) is dependent on the relationship between the instantaneous value of V_C and the peak-to-peak magnitude of the triangle wave signal, V_M. As the instantaneous value of V_C approaches the bottom of the triangle wave, the duty cycle output approaches 0 (no pulse out). Conversely, if the instantaneous value of V_C approaches the top of the triangle wave, the duty cycle approaches 1 (constant DC out). Thus the control signal input-to-duty cycle output transfer function can be written

$$D(t) + d(t) = \frac{V_C(t) + \hat{v}_C(t)}{V_M} .$$

This transfer function is only applicable at frequencies that are small compared to the switching frequency of the converter. As the frequency range of interest approaches the switching frequency, the modulator begins to contribute phase lag (Wester and Middlebrook 1972, Middlebrook and Cuk 1977, and Middlebrook 1978) that must be included in the model. For the purpose of the modelling required

for this thesis, the low frequency transfer function will be adequate.

Circuit Model

Referring back to Figure 5e which shows the final duty cycle-to-output circuit model, and equation 6, the duty cycle dependence can be replaced by control signal dependence such that (with time dependence removed for clarity)

$$V_O = DV_S = \frac{V_S V_C}{V_M} \quad . \tag{7a}$$

$$I_O = \frac{DV_S}{R_L} = \frac{V_S V_C}{V_M R_L} = I_L \quad . \tag{7b}$$

$$I_S = DI_L = \frac{D^2 V_S}{R_L} = \frac{V_S V_C^2}{V_M^2 R_L} \quad . \tag{7c}$$

$$V_{EPWM} = \hat{d}V_S = \frac{V_S \hat{v}_C}{V_M} \quad . \tag{7d}$$

and

$$I_{IPWM} = \frac{\hat{d}V_S}{R_L} = \frac{V_S \hat{v}_C}{V_M R_L} \quad . \tag{7e}$$

Figure 9 shows the results of this change as it affects the dependent generators. The dashed lines show the source of the controlling parameters for all the dependent gener-

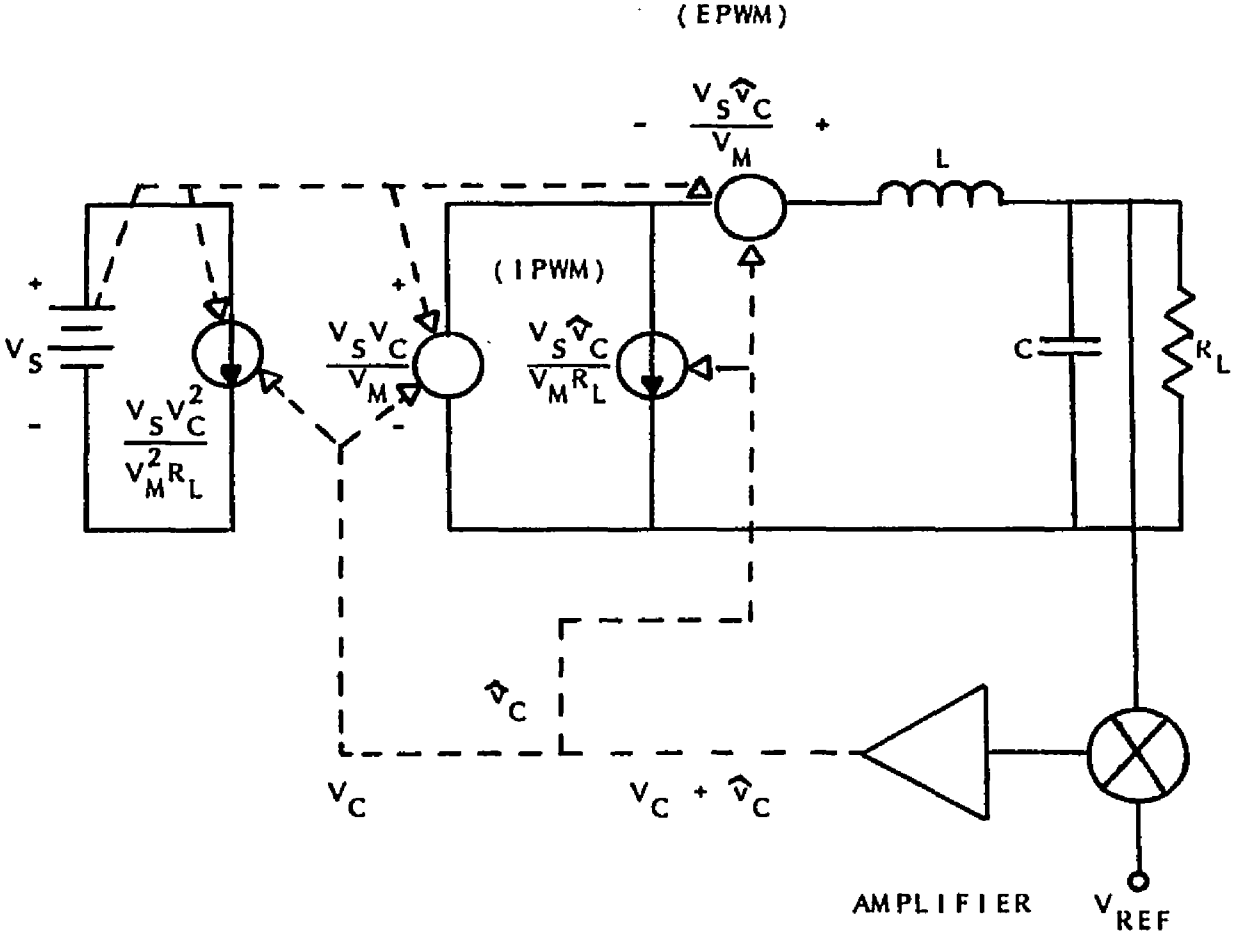


Figure 9. Control Signal-to-Output Circuit Model

ators (including a dashed line from the input source voltage, V_S, to the AC dependent generators since they are dependent on it as well).

Output-to-Control Signal Circuit Model

The final step in the converter modelling process is to model the output-to-control signal circuit.

Transfer Function

The transfer function of the output-to-control signal circuit is essentially the transfer function of the error amplifier, which is

$$V_C(t) + \hat{v}_C(t) = -\frac{R_F}{R_1}\,[V_O(t) + \hat{v}_O(t)] + \left[1 + \frac{R_F}{R_1}\right] V_{REF}(t) \,.$$

This can mathematically be separated into its DC and AC components as follows

$$V_C(t) = -\frac{R_F}{R_1}\,V_O(t) + \left[1 + \frac{R_F}{R_1}\right] V_{REF}(t) \,. \quad (8a)$$

$$\hat{v}_C(t) = -\frac{R_F}{R_1}\,v_O(t) \,. \quad (8b)$$

However, a slight problem presents itself in that the

actual circuit model for the output of the error amplifier also needs to be separated into its DC and AC components in order to control the correct dependent generators. This problem can effectively be solved by making the assumption that the closed loop gain of the error amplifier is much greater than 1

$$\frac{R_F}{R_1} >> 1 ,$$

and V_{REF} equals V_O. This means that from equation 8a

$$V_C(t) = [V_{REF}(t) - V_O(t)] \frac{R_F}{R_1} = 0 ,$$

and the signal from the error amplifier will be purely AC. Now, the AC generators can be controlled directly from the output of the error amplifier. To take care of the dependence of the DC generators, V_C will be made a part of the gain constant of the DC generators. Similarly, the dependence of the AC dependent generators on V_S will be eliminated by including the value of V_S as part of their gain.

Circuit Model

Figure 10 shows the model used for the error amplifier circuit. It is simply the AC model for a simplified

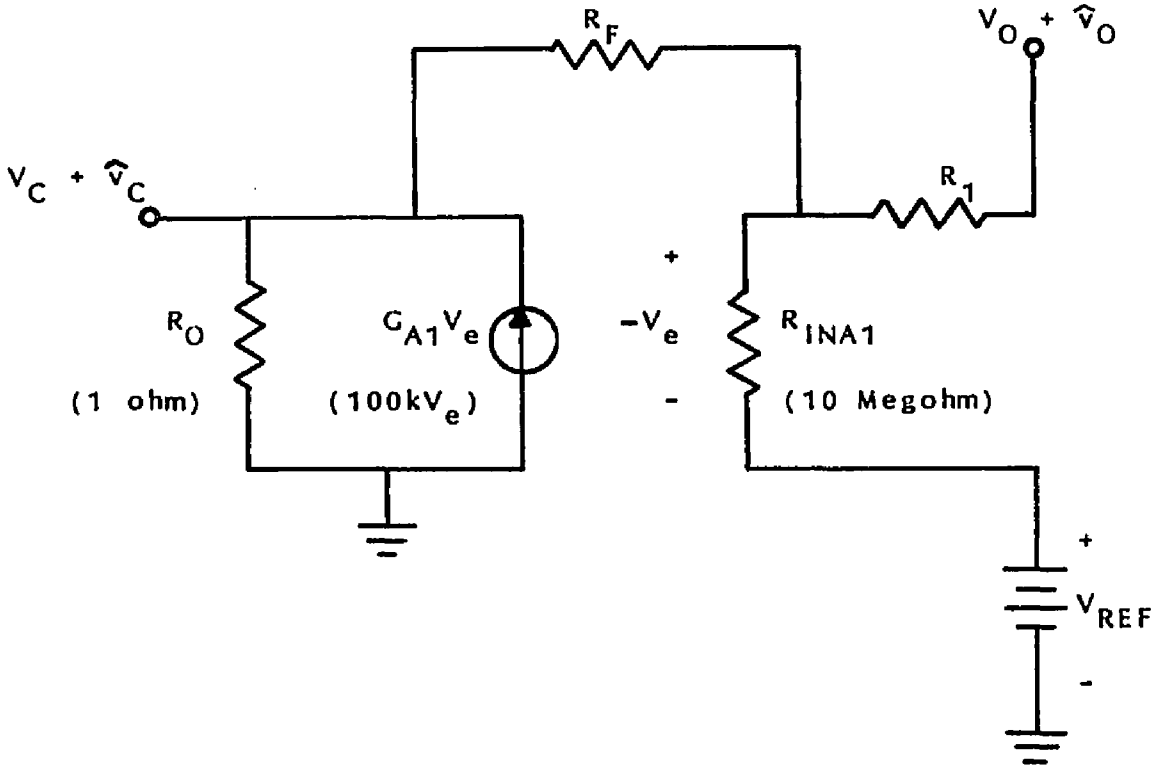


Figure 10. Error Amplifier Circuit Model

operational amplifier (in dashed lines) with associated feedback resistors R_1 and R_F.

Final Converter Circuit Model

The final closed loop circuit model for a buck converter is shown in Figure 11. The extra circuitry in parallel with EPWM is due to the dependence of IPWM on the load resistor, R_L. Equation 7c shows that EPWM has a value of

$$V_{EPWM}(t) = \frac{V_S \hat{v}_C(t)}{V_M} , \qquad (9)$$

and equation 7d shows that I_{IPWM} has a value of

$$I_{IPWM}(t) = \frac{V_S \hat{v}_C(t)}{V_M R_L} . \qquad (10)$$

Substituting equation 9 into equation 10 gives

$$I_{IPWM}(t) = \frac{V_{EPWM}(t)}{R_L} . \qquad (11)$$

Equation 11 is simply the current flowing through R_L with the voltage of V_{EPWM} across it. Thus, the final circuit model shows R_L across EPWM with the current flowing through R_L controlling IPWM. Unfortunately, the only provision that the SPICE circuit analysis program has for controlling a current controlled current source is by using the current

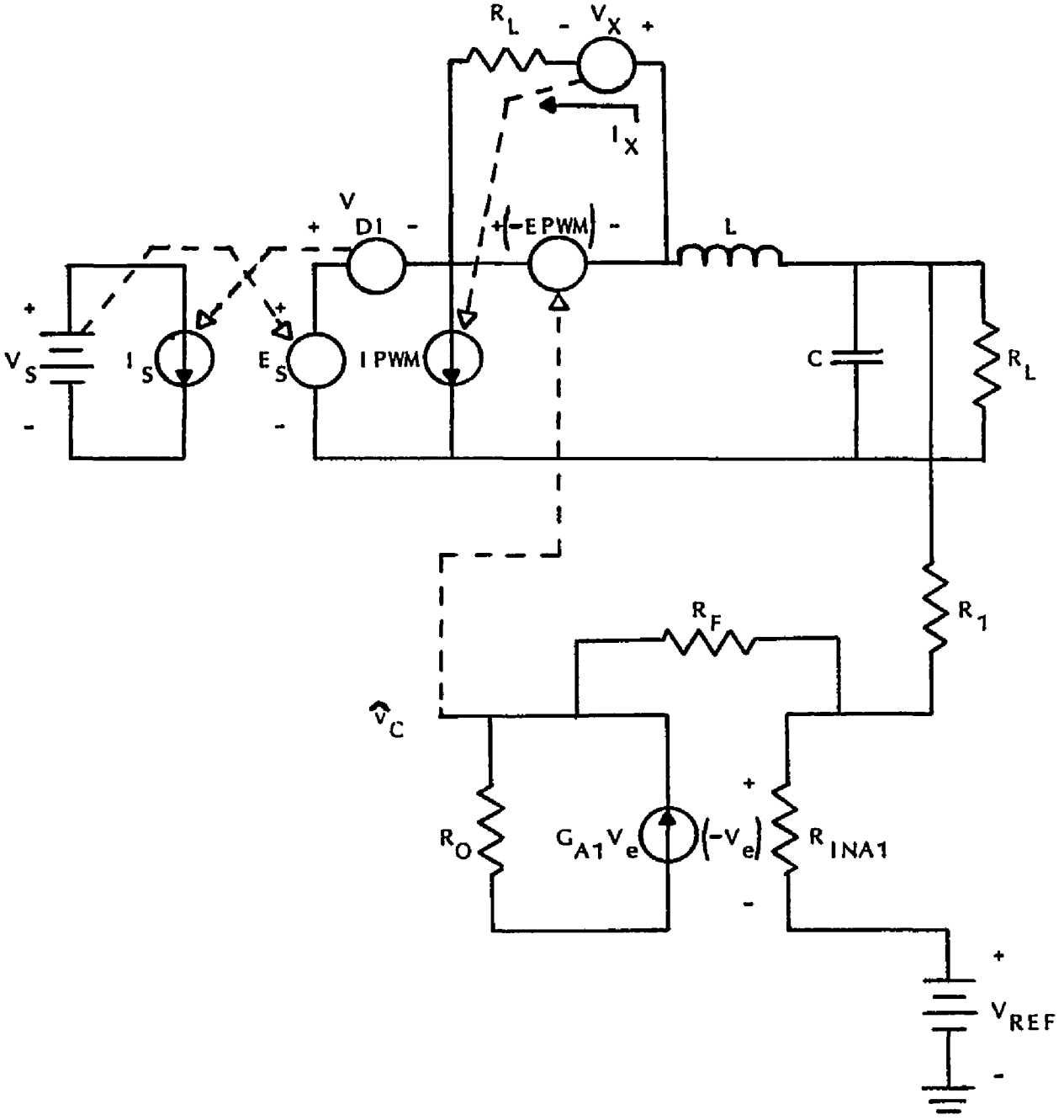


Figure 11. Final Buck Converter Circuit Model

through a voltage source. Therefore, a zero valued voltage source, V_X, is placed in series with R_L to sense the current and ultimately control IPWM. The effects on IPWM of any change in output load resistance can now be modelled by simulating the same step change across EPWM. As mentioned previously, this has no bearing on this thesis since IPWM is bypassed by a zero impedance dependent voltage generator. However, the complete model is presented for future work on this subject.

Similarly, a zero valued voltage source, V_{DI}, is placed in series with the DC dependent voltage generator to allow control of the DC dependent current generator.

The compensation network, not shown in Figure 11, will be placed after the error amplifier when it is needed in the circuit. This subject will be covered in more detail in the following chapters.

CHAPTER 3

DEVELOPMENT OF OPEN AND CLOSED LOOP TRANSFER FUNCTIONS

Now that the buck converter circuit model has been developed, the open and closed loop transfer functions for the circuit will be developed so that hand calculations can be compared with SPICE results to more fully understand the circuit operation. The transfer functions will be developed in two steps - the open loop transfer function first and then, from this, the closed loop transfer function.

Open Loop Transfer Function

The circuit can be separated into four blocks, as shown in Figure 12, where the loop is opened up between the output of the converter and the error amplifier. The product of the transfer functions of each of these blocks will give the overall open loop transfer function.

Figure 13 shows the error amplifier (block 1) that will be used. For the purpose of finding the AC transfer function, V_{REF} appears as an AC short circuit as indicated by the dashed line to ground. The circuit is a simple inverting amplifier (Wait, Huelsman, and Korn 1975)

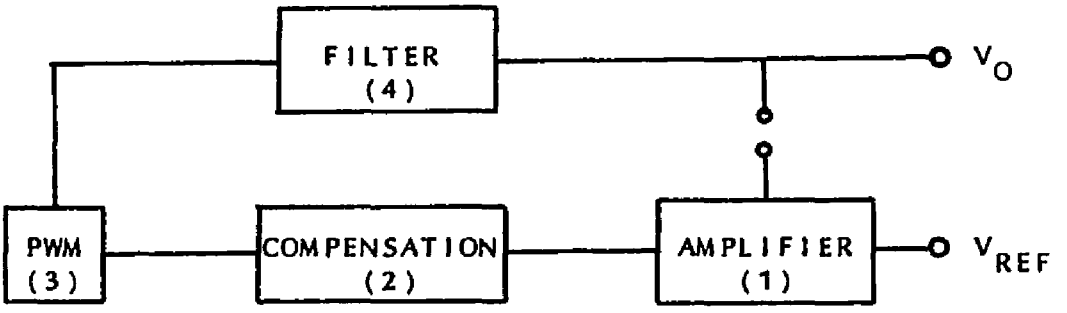


Figure 12. Converter Open Loop Block Diagram

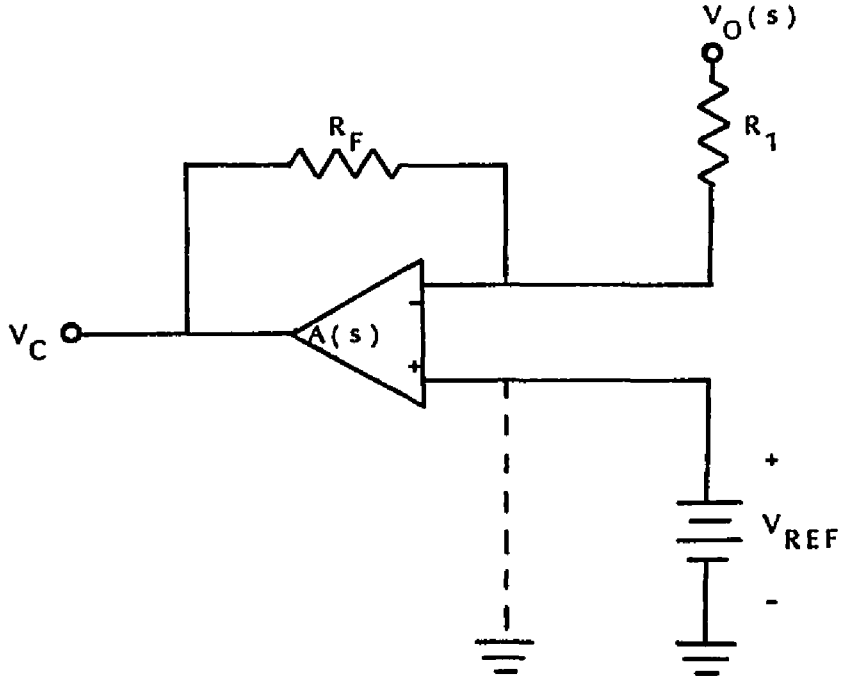


Figure 13. Inverting Amplifier

with the transfer function

$$H_{EA}(s) = \frac{R_F}{R_1} .$$

The compensation network (block 2) will be discussed in more detail in Chapter 4. For the time being, the transfer function of this block will be represented by

$$H_{COMP}(s) = \frac{N(s)}{D(s)} ,$$

where N(s) is the numerator polynomial containing the transfer function zeros and D(s) is the denominator polynomial containing the transfer function poles. As will be seen later, these compensation network poles and zeros will be used to modify the uncompensated open loop gain to obtain a desired converter closed loop transfer function. N(s) and D(s) are such that they will not affect the DC open loop gain. Therefore, they are of the form

$$N(s) = N_1(s) + 1$$

and

$$D(s) = D_1(s) + 1 ,$$

where $N_1(s)$ and $D_1(s)$ consist of s^n terms and their coefficients.

The third block, the PWM transfer function, has already been determined in Chapter 2. Transferring equation

7d to the s domain gives

$$H_{PWM}(s) = \frac{V_{EPWM}(s)}{V_C(s)} = \frac{V_S}{V_M} .$$

By using standard circuit analysis techniques, the filter transfer function (block 4) is found to be

$$H_f(s) = \frac{1}{LCs^2 + \frac{L}{R_L}s + 1} .$$

This transfer function assumes that ideal components are available. In designing actual hardware, two other parameters should be included in the above equation - the wire resistance of the inductor, denoted by R_S, and the equivalent series resistance (ESR)[1] of the capacitor, denoted by R_{ESR}. Appendix A gives this modified transfer function and explains how these parameters affect the open and closed loop transfer functions, and the transient response. The inclusion of R_S and R_{ESR} is beyond the scope of this thesis and will tend to complicate the analysis without contributing pertinent information. Therefore, they will be neglected.

---

1. The ESR of a capacitor is resistance due to four factors - the aluminum oxide thickness, the electrolyte/spacer combination, the length of the capacitor, and the ohmic contacts.

The open loop transfer function is the product of the transfer functions of each of the blocks. The result is

$$H_{OL}(s) = \frac{V_o(s)}{V_i(s)} = \frac{-\frac{R_F V_S N(s)}{R_1 V_M D(s)}}{LCs^2 + \frac{L}{R_L}s + 1} \quad . \qquad (12)$$

Equation 12 determines the stability, closed loop response, transient response, and ultimately, the load transient response of the converter.

Closed Loop Response

The closed loop response with V_{REF} as input and V_O as output can be found by using the equation

$$\frac{V_O(s)}{V_{REF}(s)} = \frac{\text{forward gain}}{1 - \text{open loop gain}} \quad . \qquad (13)$$

The open loop gain is known from the previous section and the forward gain can be found by combining the transfer functions of each of the blocks shown in Figure 14.

Comparing Figure 14 with Figure 12 and Figure 13, the only difference is the configuration of the error amplifier circuit. Looking back at V_O from R_1, the AC impedance is small. Therefore, the connection between R_1 and V_O can be broken and replaced with a ground (shown as a dashed line in Figure 14). This transforms the error

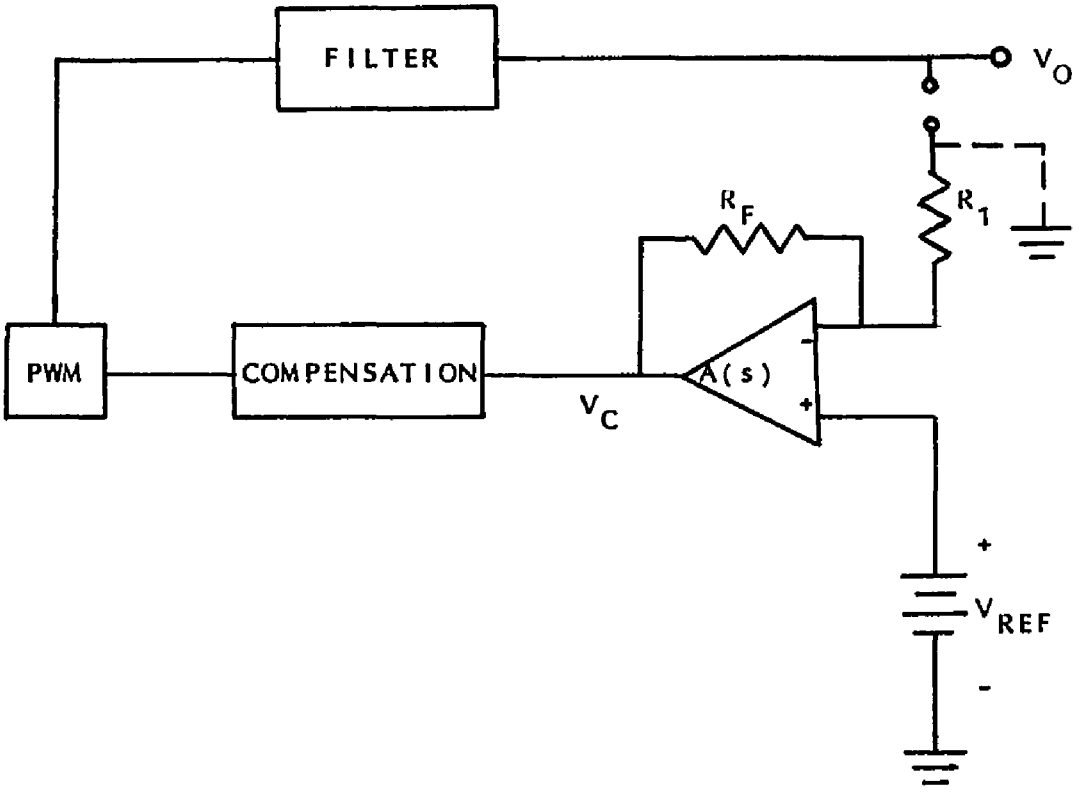


Figure 14. Forward Gain Block Diagram

amplifier to a simple non-inverting amplifier (Wait, Huelsman, and Korn 1975) with the transfer function

$$\frac{V_O(s)}{V_{REF}(s)} = 1 + \frac{R_F}{R_1} .$$

Making the assumption (as done before) that

$$R_1 >> 1 .$$

Therefore,

$$1 + \frac{R_F}{R_1} \cong \frac{R_F}{R_1} .$$

The transfer function of the remaining blocks is the same as before. Therefore, the forward gain is found to be

$$\text{forward gain} = \frac{\frac{R_F V_S N(s)}{R_1 V_M D(s)}}{LCs^2 + \frac{L}{R_L} s + 1} . \qquad (14)$$

Substituting the open loop gain equation (equation 12) from the last section, and the forward gain equation (equation 14) into equation 13 gives the closed loop transfer

function

$$H_{CL}(s) = \frac{V_O(s)}{V_{REF}(s)} = \frac{\dfrac{\dfrac{R_F V_S N(s)}{R_1 V_M D(s)}}{LCs^2 + \dfrac{L}{R_L} s + 1}}{1 + \dfrac{\dfrac{R_F V_S N(s)}{R_1 V_M D(s)}}{LCs^2 + \dfrac{L}{R_L} s + 1}} \quad . \quad (15)$$

Equation 15 is the final closed loop equation that will be used to analyze the results of the open loop equation manipulation to achieve desired closed loop response characteristics.

CHAPTER 4

COMPENSATION

We now have a general model and equations for the buck converter. This chapter will be concerned with the aspects of characterizing the compensation block which presently has the transfer function

$$H_{COMP}(s) = D(s) = D_1(s) + 1 .$$

Before getting into specifics, however, the necessity of compensation will first be discussed.

Reason for Compensation

The reason compensation is necessary can best be seen by looking at Figure 15 which shows a Bode plot of an uncompensated buck converter's open loop gain and phase characteristic. Equating this plot with equation 12 in Chapter 3

$$\frac{V_o(s)}{V_i(s)} = \frac{-\dfrac{R_F V_S N(s)}{R_1 V_M D(s)}}{LCs^2 + \dfrac{L}{R_L} s + 1} ,$$

and letting $\dfrac{N(s)}{D(s)} = 1$ (no compensation),

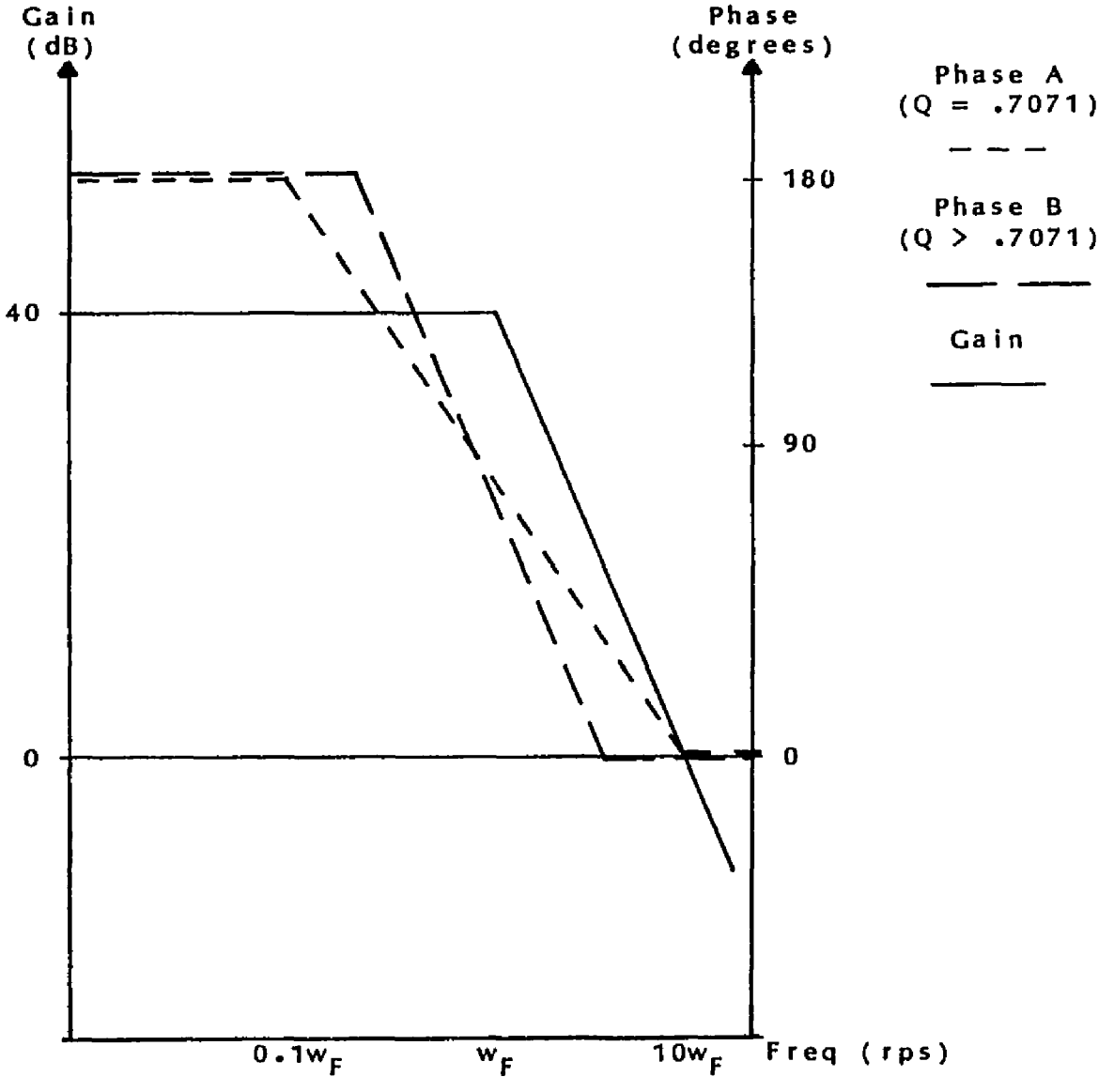


Figure 15. Bode Plot of Uncompensated Buck Converter

the DC gain of 40 dB corresponds to

$$20 \text{ Log } \frac{R_F V_S}{R_1 V_M} = 20 \text{ Log } (100) = 40 \text{ dB} .$$

The 180 degree phase shift at DC corresponds to the negative sign preceding the transfer function. The 40 dB/decade break frequency, w_{nf}, corresponds to the second order LC filter poles such that

$$w_{nf} = \frac{1}{\sqrt{LC}} .$$

The break frequencies of the phase at the 180 degree and 0 degree asymptotes are a function of the quality factor (Q) of the filter, given by

$$Q = \frac{R_L}{\sqrt{\frac{L}{C}}} .$$

The higher the Q, the closer to w_{nf} the break frequencies will occur and the quicker the phase will shift from 180 degrees to 0 degrees. Thus, if the open loop gain and/or the Q of a converter is large enough, the phase shift will approach 180 degrees before the gain has a chance to fall to less than 1. Based on the Nyquist criteria, this creates the potential for oscillation. Depending on the desired performance of the closed loop response of the system, the phase shift of the open loop response

should lie somewhere between 90 degrees and 135 degrees while the gain is greater than 1. Phase shifts in excess of this will result in a closed loop transient response with a damped AC oscillation superimposed on the DC voltage. The larger this phase shift, the larger the amplitude of the oscillation will be and the longer it will take to subside. As can be seen by again referring to Figure 15, for a DC gain of 40 dB and a Q of .7071, the converter has a phase margin of less than 5 degrees. As a result, the closed loop transient response will have a large, and very slowly subsiding oscillation superimposed on its DC output voltage waveform which could induce problems in the load circuitry that the voltage is being supplied to. For a more typical Q (i.e., larger than .7071), the phase shift is smaller and the underdamped oscillation is worse. This creates the need for some form of open loop gain and phase "shaping", more commonly known as compensation, to resolve the problem.

Methods of Compensation

There are basically four methods of compensation techniques used in the industry for compensating a PWM controlled buck converter:

1. dominant pole compensation with damping,
2. dominant pole compensation without damping,
3. two real zero cancellation compensation with damping,

4. two real zero cancellation compensation without damping.

Another compensation technique has recently been developed by Dr. W.J. Kerwin of the University of Arizona. This technique will be referred to as complex zero cancellation compensation, and can be used with and without damping. All of the aforementioned methods of compensation will be discussed in detail in the following sections.

Damping versus No Damping

Damping is the technique of adding resistance to the output filter to reduce its Q. This in itself might be enough to change the phase shift of the open loop gain to a level such that the system will be acceptably stable, as can be seen in Figure 16. The phase shift is originally at an unacceptable 150 degrees. Adding damping changes the phase shift to an acceptable 135 degrees.

Unfortunately, this will only work for systems with sufficiently low gain (only 20 dB in Figure 16) and does not allow enough control of the phase shift to dictate a specific closed loop response. Therefore, this technique is used more as an aid in compensating a system rather than as an actual compensation technique, since lower Q systems are easier to compensate than higher Q systems due to the slower changes in phase shifts that occur in lower Q systems.

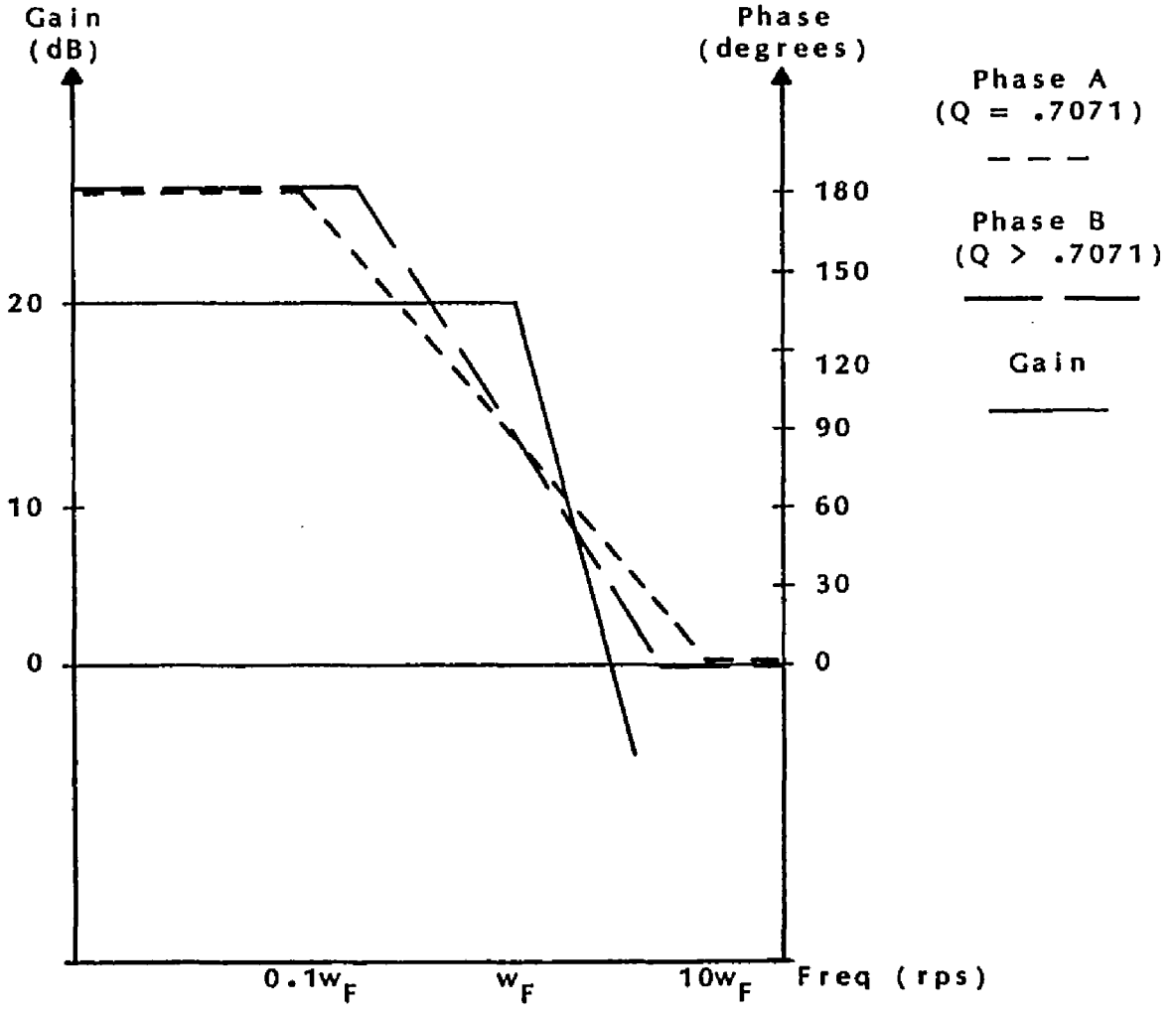


Figure 16. Using Damping as a Compensation Technique

The actual method of adding damping to the filter circuit is shown in Figure 17. L, C, and R_L are the known original filter components with transfer function

$$H_f(s) = \frac{1}{LCs^2 + \frac{L}{R_L} s + 1} .$$

The resulting Q for this circuit is

$$Q = \frac{R_L}{\sqrt{\frac{L}{C}}} .$$

If the Q of the system with just these components is too high, it can be reduced by decreasing R_L. This is accomplished by placing a resistor, R_D, in parallel with R_L to give R_L'. However, this reduction in the value of R_L is only desired at the resonant frequency of the filter and is not desirable at DC since the switching transistor and inductor would have to handle the additional current required by R_L'. Thus, capacitor C_D is added in series with R_D to prevent DC current from flowing. The filter transfer function with damping added becomes

$$H_{fD}(s) = \frac{1}{LCs^2 \quad \frac{L}{R_L} s + 1} .$$

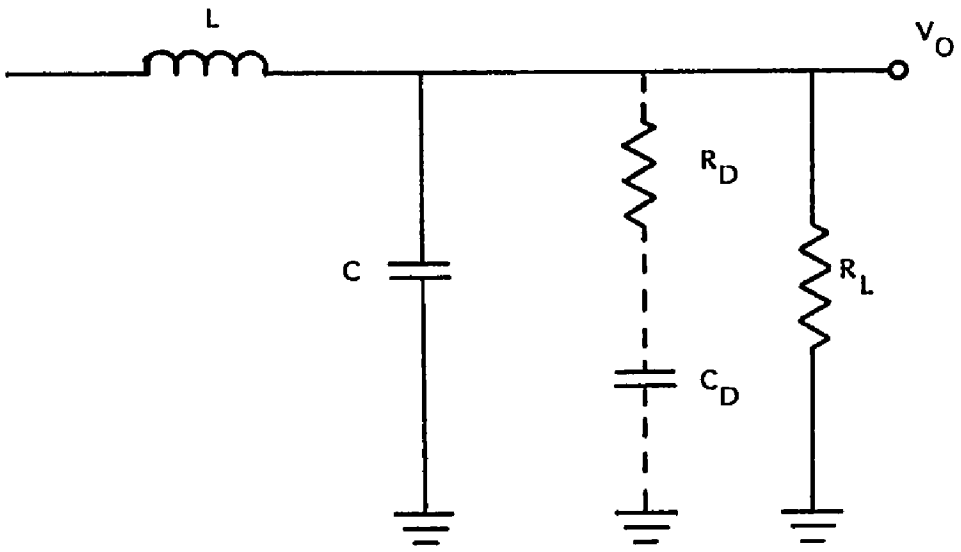


Figure 17. Adding Damping to Filter

with damped Q

$$Q_D = \frac{R_L // R_D}{\sqrt{\frac{L}{C}}} = \frac{R_L'}{\sqrt{\frac{L}{C}}} .$$

The major drawback of adding damping is the fact that C_D must be of sufficient value to appear as a short circuit at the resonant frequency of the filter. This means that it must be larger than the filter capacitor, C. Since C is usually quite large to reduce output ripple, C_D must be extremely large. A general equation for determining the allowable damped Q that a system can have in terms of the ratio of C_D to C (Middlebrook 1978) is given by

$$Q_D = \sqrt{\frac{(1 + n)(2 + n)}{n^2}} ,$$

where

$$n = \frac{C_D}{C} .$$

For a damped Q of .71, C_D must be 100 times larger than C. If C is 1000 microfarads, C_D must be .1 farad. Since this problem is not one of the issues in this thesis, a value of 1 farad will be used for C_D in all computer simulations where damping is used so as not to affect the results.

The design formula for choosing R_D is solved for as follows

$$Q_D = \frac{R_L'}{\sqrt{\frac{L}{C}}}$$

$$\frac{1}{R_L} + \frac{1}{R_D} = \frac{1}{Q_D \sqrt{\frac{L}{C}}}$$

$$R_D = \frac{Q_D \sqrt{\frac{L}{C}}}{1 - Q_D \sqrt{\frac{L}{C}}} \quad . \qquad (16)$$

From the known values of L, C, R_L, and Q_D, the value of R_D can be chosen.

Dominant Pole Compensation

Dominant pole compensation (DPC) is the method of compensating a converter by placing a pole at a low enough frequency that the open loop gain will roll off and pass the 0 dB asymptote before the complex filter pole phase shift causes the open loop phase shift to exceed 180 degrees. Figure 18 shows an example of DPC. The maximum phase shift while the gain is greater than 0 dB should be between 90 and 135 degrees, depending on the closed loop transient response. This means the phase shift of the complex filter poles should begin to take effect at about the frequency that the gain crosses the 0 dB asymptote

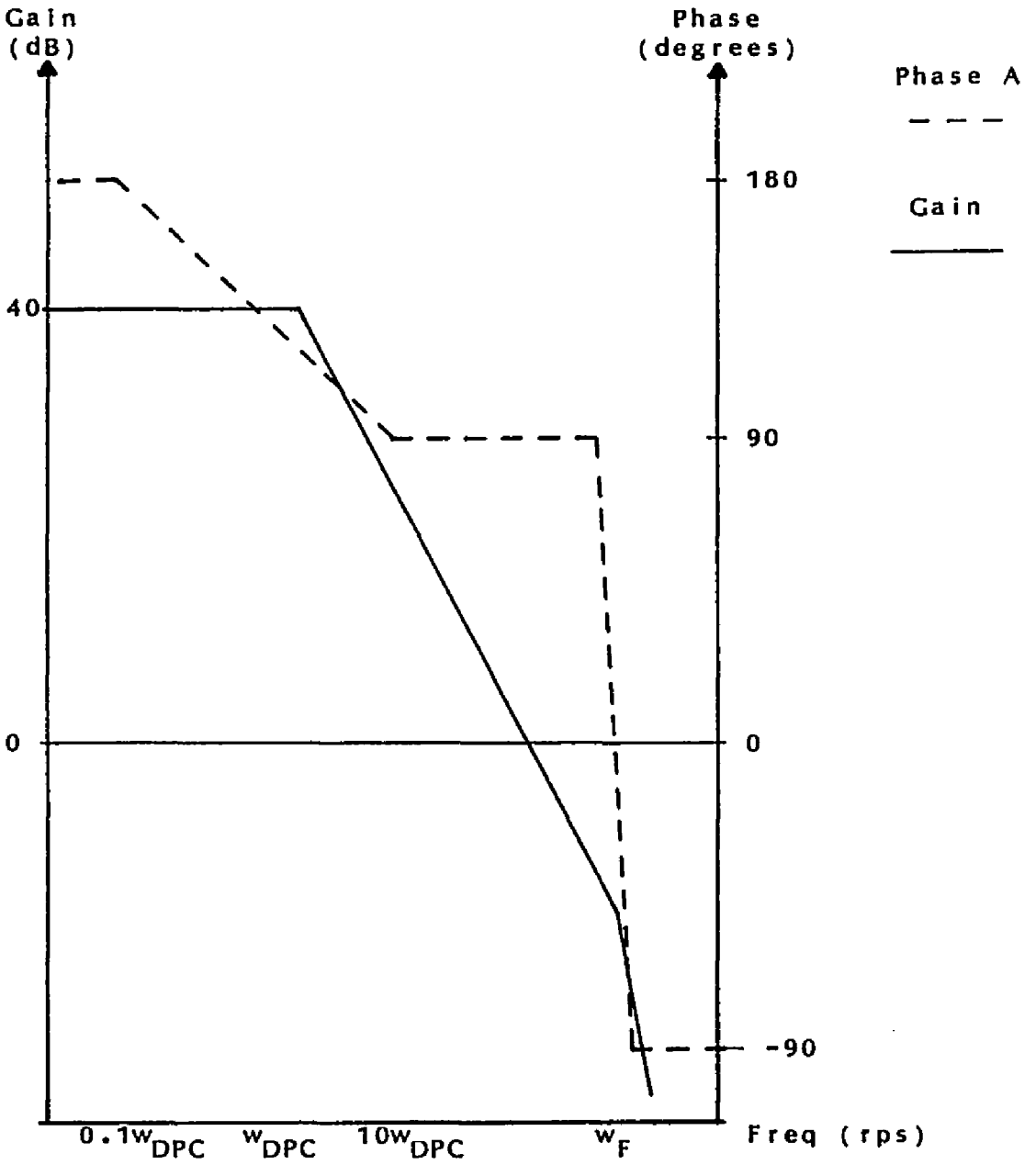


Figure 18. Example of Dominant Pole Compensation

(there is a range of frequencies at which this can occur, depending on the desired phase margin and the Q of the particular filter used).

The major drawback of this type of compensation is the loss in closed loop bandwidth that occurs with such a low frequency pole. This, in turn, causes undesirably long turn-on characteristics in the closed loop transient response.

Another more subtle problem occurs if the open loop gain characteristic forces the resulting third order closed loop system poles to be such that the real pole is small and the Q of the complex poles is large. The closed loop transient response could have some ringing superimposed on it as it rises from zero to its final value (WADC-TR-53-66); or, the overshoot might be the desired value but the settling time might be extremely long. For these cases, adding damping to the filters to modify their Q might aid in forcing the closed loop system to operate in the "good transient response" region.

The circuitry for adding DPC to the converter is an RC low pass filter placed after the error amplifier, as shown in Figure 19. The transfer function for this compensation network is given by

$$H_{DPC}(s) = sR_{DPC}C_{DPC} + 1 \ .$$

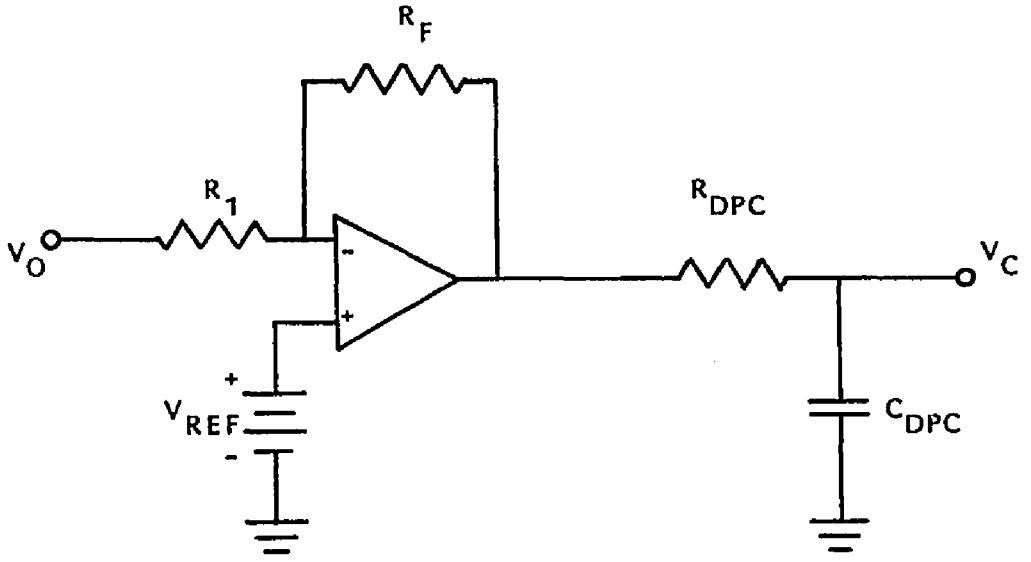


Figure 19. Dominant Pole Compensation Implementation

The open and closed loop converter transfer functions can be found by substituting this transfer function for $\frac{N(s)}{D(s)}$ in equations 12 and 15, giving

$$H_{OL(DPC)}(s) = \frac{-\frac{R_F V_S}{R_1 V_M}}{(sR_{DPC}C_{DPC} + 1)(LCs^2 + \frac{L}{R_L}s + 1)}, \quad (17)$$

$$H_{CL(DPC)}(s) = \frac{\frac{R_F V_S}{R_1 V_M}}{R_{DPC}C_{DPC}LCs^3 + \left[LC + R_{DPC}C_{DPC}\frac{L}{R_L}\right]s^2 + \left[R_{DPC}C_{DPC} + \frac{L}{R_L}\right]s + 1 + \frac{R_F V_S}{R_1 V_M}} \quad (18)$$

These two equations will be used in Chapter 5 to design and evaluate a dominant pole compensated buck converter.

Two Real Zero Cancellation Compensation

Two real zero cancellation compensation (TRZCC) utilizes two zeros, z_1 and z_2, on the real axis of the -jw plane to approximately cancel the effects of the two complex filter poles. Two real poles, p_1 and p_2, are then placed on the real axis, one at low frequencies to roll off the gain and one at high frequencies to cancel the effects of any parasitic zeros that could occur (such as the zero caused by the ESR of the filter capacitor - see Appendix A).

Figure 20 shows an ideal example of TRZCC, where the maximum phase shift at (and below) the gain zero crossing frequency is 90 degrees. Unfortunately, in actual converter applications where the output filter Q is greater than .7071, the phase shift of the two added zeros does not exactly cancel the phase shift of the two complex filter poles. The phase shift of two real zeros begins rolling off at a frequency of $.1w_{z12}$ (where $w_{z1}=w_{z2}=w_{z12}$) with a slope of +90 degrees/decade. The phase shift of a pair of complex poles with a Q greater than .7071 will begin rolling off at frequencies closer to w_{nf} than $.1w_{nf}$ and with a slope greater than -90 degrees/decade. As a result, the overall open loop gain and phase could look like that shown in Figure 21. The phase shift is the same as that shown in Figure 20 until the frequency $.1w_{z12}$ is reached. At this frequency, the phase begins to rise with a slope of +90 degrees/decade due to the two real zeros. Since the Q of the complex filter poles is larger than .7071, its phase shift will not take effect until some frequency k_1w_{nf} (k_1 being a function of Q). At this frequency, the complex filter poles phase shift will begin rolling off with a slope greater than -90 degrees/decade, thereby causing the overall open loop phase shift to fall. This rolloff will continue until some frequency k_2w_{nf} (k_2 is also a function of Q) where the complex poles'

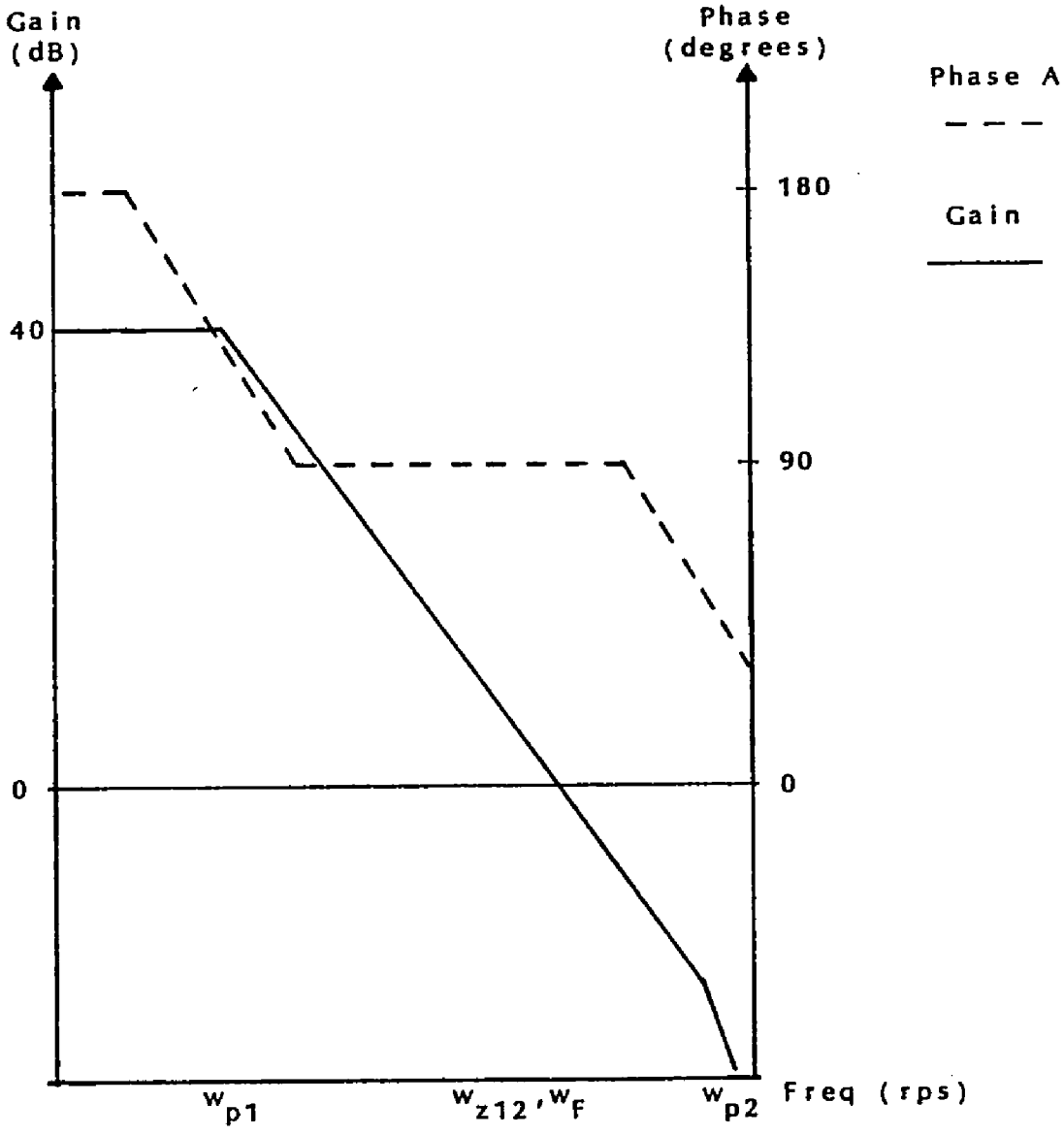


Figure 20. Ideal Example of TRZCC

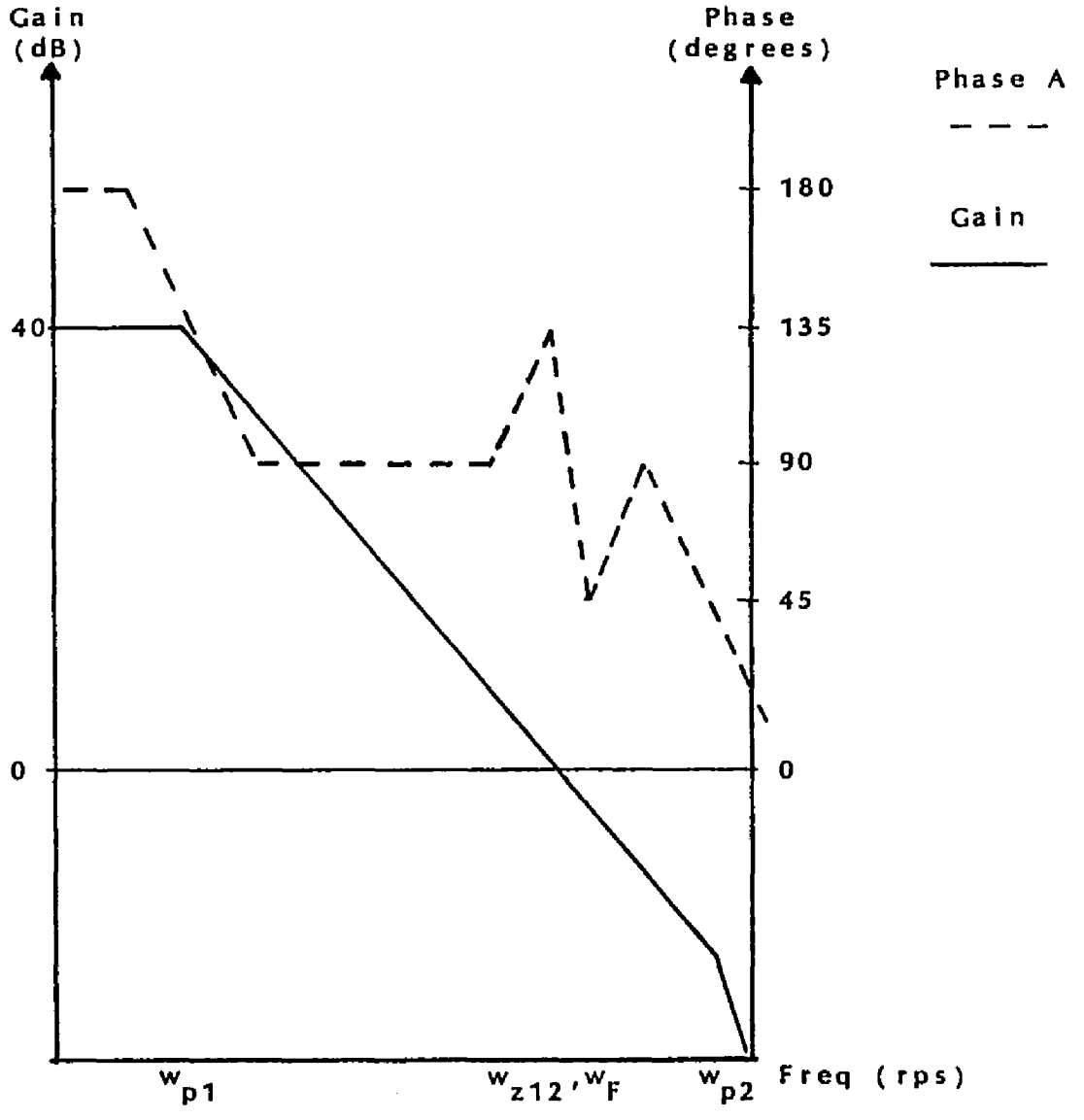


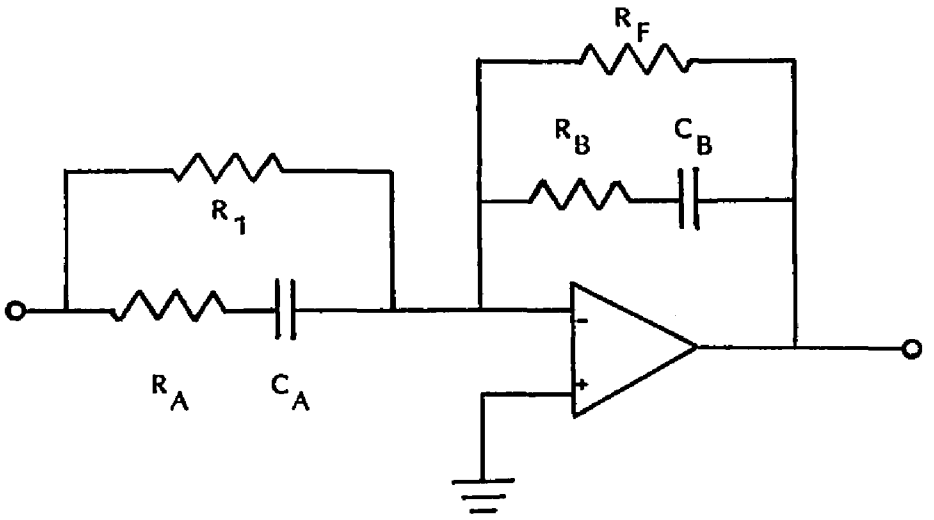
Figure 21. TRZCC with High Q Filter

phase shift will flatten out. At this frequency, the open loop phase will again rise at a rate of +90 degrees/decade until frequency $10w_{z12}$, where the phase shift of the two real zeros flattens out. From this frequency on, the phase shifts are the same as that shown in Figure 20. As a result of these various break points in the open loop phase shift, the maximum phase shift before the gain crosses the 0 dB asymptote is greater than 135 degrees.

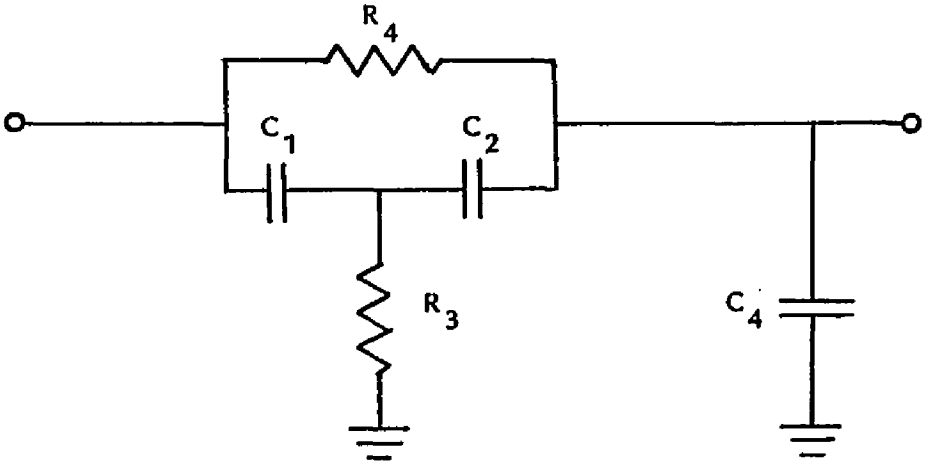
There are two possible solutions to this problem. The first is to add damping to the filter to force its Q to be approximately .7071. A second solution is to adjust the location of the zeros to a frequency less than w_{nf} to allow the effects of their phase shift to take effect at a lower frequency (known as "phase lead"). This will allow the open loop phase shift to increase to a level such that the effects of the complex poles' phase shift will not cause the open loop phase shift to exceed 135 degrees. The location of z_1 and z_2 can be controlled to give any phase shift desired. The actual method for doing this will be covered in more detail in Chapter 5.

TRZCC can be implemented using one of the two circuits shown in Figure 22.

Circuit A, the complex inverting amplifier (CIA), is the one currently being used in industry today (Dixon 1985). Its major drawback is that it requires the use



(a) Complex Inverting Amplifier



(b) Modified Bridged-Tee

Figure 22. TRZCC Circuit Implementation

of two additional inverting amplifier stages, one stage preceding it and one stage following it. The preceding amplifier stage is a buffer, preventing interaction between the output filter and R_1, R_A, and C_A of the CIA stage. As a result of this buffer stage, an inverting amplifier stage must be added following the CIA stage to maintain a negative feedback configuration.

Circuit B, the modified bridged-tee, was recently introduced by Dr. W. J. Kerwin as a part of his complex zero cancellation compensation technique. It was also found to work admirably well for the TRZCC technique. More details on this circuit can be found in the next section where complex zero cancellation compensation is covered, and in Chapter 5.

Both circuits are used in evaluating the TRZCC technique in an effort to determine if the circuitry used has an effect on the load transient response.

The transfer functions for the two circuits shown in Figure 22 are given as follows:

Circuit A

$$H_{CIA}(s) = \frac{R_F[(R_A + R_1)C_A s + 1][R_B C_B s + 1]}{R_1[R_A C_A s + 1][(R_B + R_F)C_B s + 1]} , \quad (19a)$$

where $$\frac{R_F}{R_1} = 1 ,$$

$$\frac{1}{(R_A + R_1)C_A} = \frac{1}{R_B C_B} = w_{z1} = w_{z2} = w_{z12} ,$$

$$\frac{1}{R_A C_A} = w_{p1} ,$$

$$\frac{1}{(R_B + R_F)C_B} = w_{p1} .$$

Circuit B

$$H_{TEE}(s) = \frac{C_1C_2R_3R_4s^2 + R_3(C_1 + C_2)s + 1}{R_3R_4[C_1C_2 + C_4(C_1 + C_2)]s^2} \quad (19b)$$
$$+ [R_3(C_1 + C_2) + R_4(C_2 + C_4)]s + 1$$

where $$\frac{1}{C_1C_2R_3R_4} = w_{z1}w_{z2} = w_{z12} ,$$

$$R_3(C_1 + C_2) = \frac{1}{w_{z1}} + \frac{1}{w_{z2}} = \frac{2}{w_{z12}} ,$$

$$\frac{1}{R_3R_4[C_1C_2 + C_4(C_1 + C_2)]} = w_{p1}w_{p2} ,$$

$$R_3(C_1 + C_2) + R_4(C_2 + C_4) = \frac{1}{w_{p1}} + \frac{1}{w_{p1}} .$$

The open and closed loop transfer functions can be found by substituting the transfer function of either compensation circuit for $\frac{N(s)}{D(s)}$ into equations 12 and 15 and simplifying,

giving

$$H_{OL\ (TRZCC)}(s) = \frac{\frac{R_F V_S}{R_1 V_M}\left(\frac{s}{w_{z12}} + 1\right)^2}{\left(\frac{s^2}{w_{p1}w_{p2}} + \left[\frac{1}{w_{p1}} + \frac{1}{w_{p2}}\right]s + 1\right)}, \qquad (20)$$

$$\times \left(LCs^2 + \frac{L}{R_L}s + 1\right)$$

$$H_{CL\ (TRZCC)}(s) = \frac{\frac{R_F V_S w_{p1} w_{p2}}{R_1 V_M LC w_{z12}^2}\left(\frac{s}{w_{z12}} + 1\right)^2}{s^4 + \left[\frac{1}{R_L C} + w_{p1} + w_{p2}\right]s^3} \qquad (21)$$

$$+ \left[\frac{1}{LC} + \frac{w_{p1} + w_{p2}}{R_L C} + w_{p1}w_{p2} + \frac{R_F V_S w_{p1} w_{p2}}{R_1 V_M w_{z12}^2}\right]s^2$$

$$+ \left[\frac{w_{p1} + w_{p2}}{LC} + \frac{w_{p1}w_{p2}}{R_L C} + \frac{2R_F V_S w_{p1} w_{p2}}{R_1 V_M w_{z12}}\right]s$$

$$+ \left[\frac{R_F V_S}{R_1 V_M} + 1\right]\left[\frac{w_{p1}w_{p2}}{LC}\right].$$

These equations will be used in Chapter 5 to compensate and evaluate a converter using the TRZCC technique.

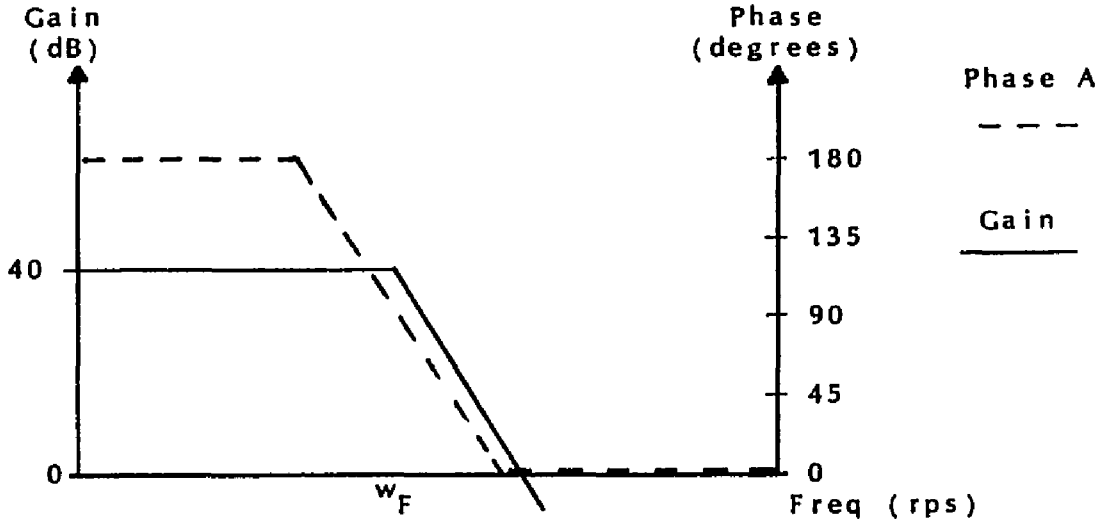
Complex Zero Cancellation Compensation

As mentioned in previous sections, the technique of complex zero cancellation compensation (CZCC) is a relatively new one. What makes it unique is that, until it was developed, the only compensation techniques used

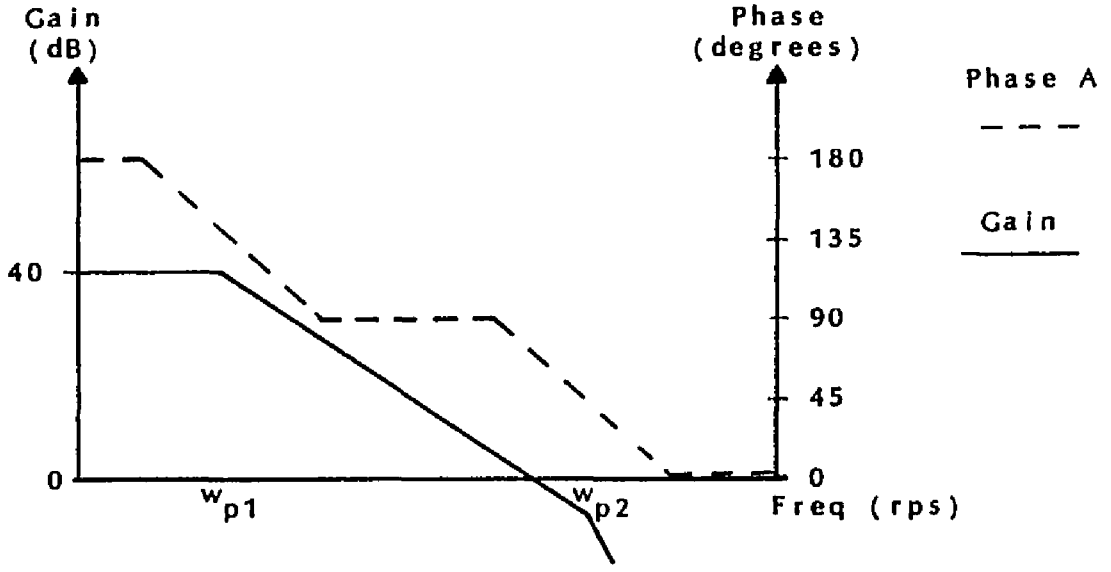
were those that used poles and zeros placed on the real axis of the -jw plane to "shape" the open loop gain and phase (as evidenced by the DPC and TRZCC techniques). CZCC technique actually places a pair of zeros on top of the existing complex filter poles (the zeros are, thus, complex), thereby exactly cancelling the gain and phase effects of the complex poles (this avoids the problems associated with the TRZCC technique). A pair of poles is then placed on the real axis in the -jw plane, forming the open loop response that will give the desired closed loop response. Therefore, the overall open loop system remains a second order system even though there are two zeros and four poles in the transfer function.

Figure 23 illustrates the "before" and "after" open loop response using CZCC technique. Figure 23a shows the response of the converter with no compensation. Figure 23b shows the response when the complex filter poles are cancelled and replaced with two real poles at w_{p1} and w_{p2}, giving an acceptable 45 degree phase margin at, and below, the zero crossing frequency.

The circuit used to obtain this compensation technique is the modified bridged-tee circuit shown in Figure 22b. The transfer function is that of equation 19b from the previous section, where w_{z1} and w_{z2} are complex conjugate zeros, rather than two real and equal zeros. When



(a) Before Compensation



(b) After Compensation

Figure 23. Illustration of CZCC

the compensation circuit transfer function is substituted for $\frac{N(s)}{D(s)}$ in equation 12, the open loop transfer function is

$$H_{OL}(s)_{(CZCC)} = \frac{-\frac{R_F V_S}{R_1 V_M}\left[\frac{s^2}{w_{z1}w_{z2}} + \left(\frac{1}{w_{z1}} + \frac{1}{w_{z2}}\right)s + 1\right]}{\left[\frac{s^2}{w_{p1}w_{p2}} + \left(\frac{1}{w_{p1}} + \frac{1}{w_{p2}}\right)s + 1\right]\left[LCs^2 + \frac{L}{R_L}s + 1\right]}$$

$$= \frac{-\frac{R_F V_S}{R_1 V_M}}{\frac{s^2}{w_{p1}w_{p2}} + \left(\frac{1}{w_{p1}} + \frac{1}{w_{p2}}\right)s + 1} . \qquad (22)$$

This equation can now be substituted into equation 15 to give the closed loop transfer function

$$H_{CL}(s)_{(CZCC)} = \frac{\frac{R_F V_S}{R_1 V_M}}{\frac{s^2}{w_{p1}w_{p2}} + \left(\frac{1}{w_{p1}} + \frac{1}{w_{p2}}\right)s + 1 + \frac{R_F V_S}{R_1 V_M}} . \qquad (23)$$

These transfer functions (along with equation 19b in the previous section) are used to derive equations that will give the actual component values for the modified bridged-tee compensation circuit from the output filter parameters and the desired closed loop response specifications. This will be covered in more detail in Chapter 5.

There appear to be no drawbacks to this compensation technique. However, limitations have been found that need

further exploration. These limitations show up as negative component values when the component values for the bridged-tee compensation circuit are calculated. This implies that certain pole pairs cannot be substituted for the cancelled complex filter poles. A detailed evaluation of this problem, however, is beyond the scope of this thesis.

The next chapter will be concerned with taking each of the compensation techniques outlined in this chapter and applying it to actual converter design.

CHAPTER 5

LOAD TRANSIENT RESPONSE COMPUTER SIMULATION

This chapter is concerned with the design of a buck converter using specifications normally given to power supply designers. This converter will then be simulated using SPICE and the information from Chapter 2. The compensation techniques from Chapter 4 will then be applied and modelled.

Throughout the design and modelling process, four responses will be simulated and tabulated for comparison of compensation techniques. These four responses are: open loop frequency response, closed loop frequency response, reference voltage input transient response, and load transient response. Based on the evaluation of these responses, the effects of compensation technique on load transient response will be more clearly understood.

Buck Converter Design

To begin the comparison of different compensation techniques, a converter circuit is needed. This circuit will be designed using typical design specifications and will initially take the form of the circuit shown in Figure 24. This circuit will then be transformed to the

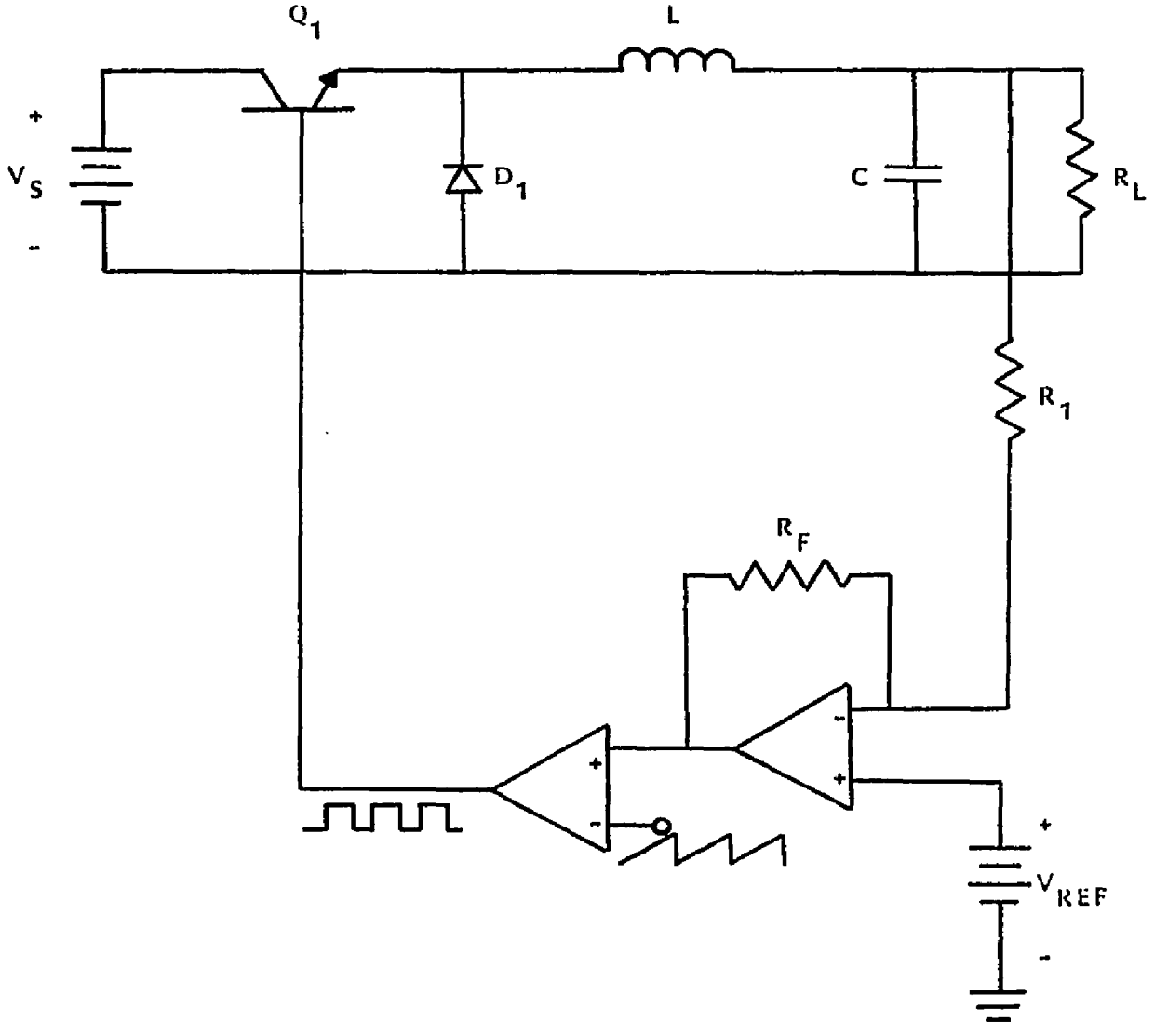


Figure 24. Buck Converter Circuit

final buck converter circuit model, shown in Figure 11, and simulated on SPICE. The results of this design will illustrate the stability problems associated with buck converter design and will show the necessity for having some form of compensation.

Following are the specifications used to design the typical buck converter:

$V_O = 5 \pm 0.1\%$ volts	Output Voltage
$I_O = 5 \begin{smallmatrix} + 5.0 \\ - 0.0 \end{smallmatrix}$ amps	Load Current
$v_{O(R)} = .05\%$	Output Voltage Ripple
$v_{O(LT)} = 2.5\%$	Load Transient Output Voltage Change
$V_S = 25$ volts	Source Voltage
$f_S = 50$ KHz	Switching Frequency

Each of these parameters provides a piece of information that will be used in selecting component values for the converter.

Feedback Circuit Design

The specification parameter of interest in the design of the feedback circuitry is the tolerance on the output voltage, $\pm$ 0.1%. This tolerance establishes the required DC loop gain using

$$\frac{\% \text{ Tolerance}}{100} = \frac{1}{K_{DC}} ,$$

where K_{DC} is the DC loop gain. Solving for K_{DC} gives

$$K_{DC} = \frac{100}{\% \text{ Tolerance}} = \frac{100}{0.1}$$

$$= 1000 .$$

Referring back to equation 12 in Chapter 3, the DC loop gain (neglecting the minus sign) is given as the product of the DC gain of the output filter ($K_{fDC} = 1$), the DC gain of the error amplifier ($K_{eaDC} = \frac{R_F}{R_1}$), and the DC gain of the PWM ($K_{PWMDC} = \frac{V_S}{V_M}$). Therefore

$$K_{DC} = 1000 = \frac{R_F V_S}{R_1 V_M} .$$

In this equation, V_S is the only known quantity. V_M, the peak-to-peak value of the triangle waveform that the error signal is compared to, must be chosen. Most integrated circuit PWMs use values of V_M ranging from 1 volt to 5 volts. The value chosen for this design will be 2.5 volts. This gives a PWM gain of

$$K_{PWMDC} = \frac{V_S}{V_M} = \frac{25}{2.5} \qquad (24)$$

$$= 10 .$$

This is an arbitrary selection of V_M and, in actual hardware design, the design of the triangle wave generator may

play into the decision. The value of 2.5 volts was obviously chosen to make the numbers easier to work with.

Since K_{PWMDC} is equal to 10, the gain of the error amplifier is given by

$$K_{eaDC} = \frac{R_F}{R_1} = \frac{K_{DC}}{K_{PWMDC}} = \frac{1000}{100}$$

$$= 10 .$$

Choosing R_F = 10k ohms, R_1 is found to be

$$R_1 = \frac{R_F}{K_{eaDC}} = \frac{10k}{10}$$

$$= 100 \text{ ohms} .$$

Applying this to the circuit given in Figure 24, R_F and R_1 can be substituted directly in. The PWM gain (equation 24) cannot be readily substituted into Figure 24 since it is inherent in the comparator circuitry. Later, however, it will be incorporated into the final buck converter model in Figure 11.

Reference Voltage Selection

The selection for reference voltage is obvious. Since V_O is 5 volts, and since there is no resistive divider between the output and the error amplifier input, the reference voltage must also be 5 volts.

Load Resistor and Output Filter Design

The selection of the output filter component values is a critical operation in terms of the expected load transient response, as will be seen shortly.

The load resistor is selected based on the output voltage and load current requirements. Using Ohm's law, this gives an R_L of

$$R_L = \frac{V_O}{I_O} = \frac{5}{5}$$

$$= 1 \text{ ohm} .$$

The selection of the inductor, L, is not as straightforward. The equation that will be used is

$$L = \frac{V_O(V_S - V_O)}{f_S V_S I_{LPK}} . \qquad (25)$$

All the parameters of this equation are based on the specifications given except I_{LPK}. This parameter, the peak-to-peak inductor ripple current, is primarily chosen to keep the inductor from operating in the discontinuous conduction mode.[2] Ideally, this parameter should be chosen as small as possible to reduce the peak current requirements

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2. Discontinous conduction occurs when the inductor current falls to zero before the off time of the switching transistor is complete.

of the switching transistor (the peak current seen by Q_1 is given by $I_{PK} = I_{DC} + \frac{1}{2} I_{LPK}$). However, when the load transient response is an important consideration, a secondary concern comes up in that the inductor must be small enough so as not to impede the change in current required of a large change in load. The larger the inductor, the longer it will take to "charge up" or "charge down" to the currents demanded of it. This means the output capacitor must source or sink the extra current until the inductor current can change, causing the output voltage to rise or fall. The capacitor, therefore, must be of sufficient value that this rise or fall in output voltage is controlled. This will be covered in more detail when the capacitor value is selected.

To come up with a reasonable size inductor to meet the load transient requirements, I_{LPK} should be chosen to be between 20% and 40% of the minimum load current requirements (Pressman 1977). This value will provide a large enough inductance to keep discontinous conduction from occurring and still allow the inductor current to change quickly. The range of values for I_{LPK} is

$$0.2 I_{L(MIN)} \leq I_{LPK} \leq 0.4 I_{L(MIN)}$$

$$0.2(5) \leq I_{LPK} \leq 0.4(5)$$

$$1.0 \text{ amp} \leq I_{LPK} \leq 2.0 \text{ amps}$$

Substituting these two values of peak current into equation 25 and solving for L gives a range of inductance values of

$$80\ \mu H \geq L \geq 40\ \mu H$$

A value of 50 microhenries will be chosen, corresponding to about 30% of I_{LPK}.

With the value of inductor chosen, it is now possible to choose the capacitor value. As mentioned previously, to meet the load transient requirements, the capacitor must be of sufficient value that it can handle the excess currents with controlled output voltage change for a period of time while the inductor current builds up or down. It also must be of sufficient value that it can meet the output voltage ripple specifications requirements of $v_{O(R)} = .05\%$.

Capacitor value based on output ripple requirements is given by

$$C = \frac{V_O(V_S - V_O)}{8LV_S f_S^2 v_{O(R)}}$$

$$= \frac{5(25 - 5)}{8(50u)(25)(50k)^2(2.5m)}$$

$$= 1600\ uF\ .$$

Capacitor value to meet the load transient requirements can be calculated using

$$C = \frac{L i_L I_C}{V_{O(LT)} V_L} \quad , \qquad (26)$$

where: $V_{O(LT)}$ is the maximum output voltage change allowed under load transient conditions;

i_L is the additional current that the inductor must build up or down to;

I_C is the maximum excess current that the capacitor is expected to handle;

and V_L is the maximum voltage available across the inductor that causes the inductor current to change.

$V_{O(LT)}$ is either given or selected. In the specifications list, it is given as 2.5% of the output voltage, or .125 volts.

I_C is the difference between the load current at $t = 0_+$ and the inductor current at $t = 0_+$ ($t = 0$ being the time at which the load is switched from 5 amps to 10 amps). Therefore

$$I_C = I_O(t=0_+) - I_L(t=0_+) .$$

Since $$I_L(t=0_+) = I_L(t=0_-) = 5 \text{ amps} ,$$

and $$I_O\,(t=0_+) = 10 \text{ amps},$$

then $$I_C = 10 - 5$$

$$= 5 \text{ amps}.$$

i_L is also the difference between the load current at $t = 0_+$ and the inductor current at $t = 0_+$. Therefore,

$$i_L = I_C = 5 \text{ amps}.$$

V_L is the smaller of the two "maximum" voltages that can be across the inductor during load transient conditions. The extremes for V_L will occur when the transistor is constantly on or constantly off. Under these extremes, V_L can take on the following values

$$V_L = V_S - V_O = 25 - 5$$

$$= 20 \text{ volts} \qquad (Q_1 \text{ on}),$$

and $$V_L = - V_O$$

$$= - 5 \text{ volts} \qquad (Q_1 \text{ off}).$$

For this design, the lower of the two maximum voltage magnitudes is 5 volts.

Substituting these known values into equation 26 gives

$$C = \frac{50u(5)(5)}{(.125)(5)}$$

$$= 2000 \text{ uF}.$$

Therefore, a 2000 microfarad capacitor will be used. As it turns out, a lower value of capacitance could be used if necessary. The reason for this is that equation 26 is based on the assumption that the capacitor would have to handle all of the excess current until the inductor current reached the level of the output current. This is not actually the case. The current flowing through the inductor, as it builds up or down, immediately begins reducing the current the capacitor has to handle. This reduces $v_{O(LT)}$.

The values of L, C, and R_L can now be substituted directly into Figure 24.

Diode and Transistor Selection

The selection of D_1 and Q_1 will not be considered in this thesis since they are averaged out of the computer simulation model. The design of the relevant circuitry of the buck converter is, therefore, complete.

Spice Evaluation

The buck converter design from the previous section will now be fitted to the final buck converter model shown in Figure 11.

Final Buck Converter Model

All the variables are known except for V_C. V_C can be found as follows:

from equation 7a

$$D = \frac{V_C}{V_M} ,$$

therefore, $V_C = V_M D$ volts .

Also, $V_O = DV_S$ volts ,

therefore, $D = V_S = 25 = .02$,

giving $V_C = V_M D = (2.5)(0.2)$

$= 0.5$ volts .

Now all the variables are known and Figure 11 can have actual values substituted in. Working from left to right in Figure 11

$V_S = 25$ volts ,

$I_S = \frac{V_C}{V_M} I_{DI} = \frac{0.5}{2.5} I_{DI} = 0.2 I_{DI}$ amps ,

$V_{DI} = 0$ volts (current sensing source),

$E_S = \frac{V_C}{V_M} V_S = \frac{0.5}{2.5} V_S = 0.2 V_S$ volts ,

$EPWM = \frac{V_S}{V_M} \hat{v}_C = \frac{25}{2.5} \hat{v}_C = 10\hat{v}_C$ volts ,

$IPWM = I_X$ amps (current flowing through V_X) ,

R_L = 1 ohm ,

L = 50 μH ,

C = 2000 μF ,

R_F = 10k ohms ,

R_1 = 100 ohms ,

R_O = 1 ohm , G_{A1} = 100k mhos , R_{IN} = 10M ohms , } (simplified error amplifier model given in Figure 10)

and V_{REF} = 5 volts .

With these values substituted into Figure 11, the SPICE model is complete (the resistor, R_L, in parallel with EPWM has had its variable name changed to R_X; SPICE will only allow one component called R_L).

Simulation Responses

Following is a description of the responses that are simulated on SPICE for the uncompensated and compensated converter:

1. Open loop response - The loop is physically opened between the output of the converter and the feedback resistor, R_1, and a DC voltage of the same potential as the output voltage is connected to R_1. An AC voltage is then superimposed on top of the DC

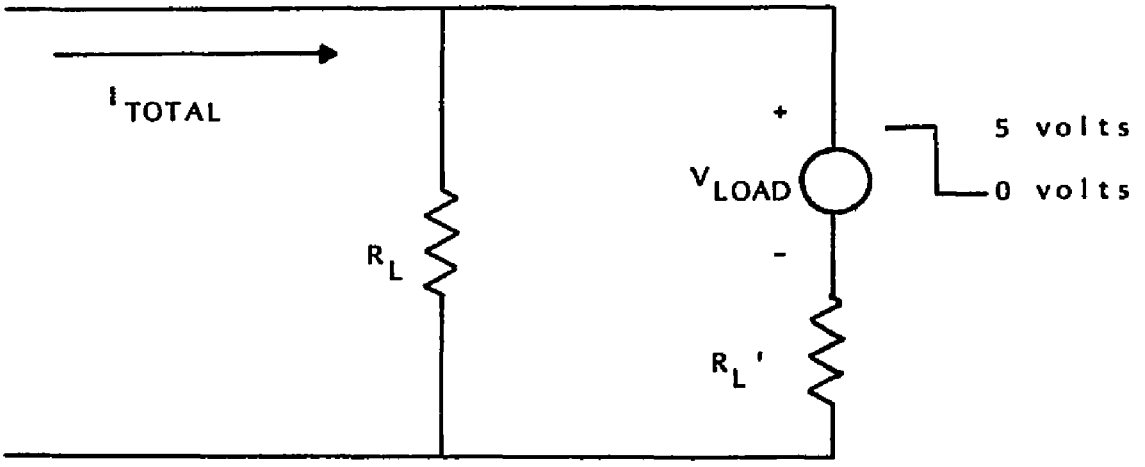
voltage applied to R_1 and a plot of the magnitude and phase of this AC signal across R_L (the output of the converter) is printed out. This information is used to verify that the compensation poles and zeros ended up where they were designed to be, and to look at the maximum phase shift to get a feel for the transient response.

2. Closed Loop Response - An AC signal is superimposed on top of V_{REF} at the input of the closed loop system and the magnitude and phase plot are printed out. This information is used to verify the closed loop bandwidth, which is a parameter that is designed for when the converter is compensated.

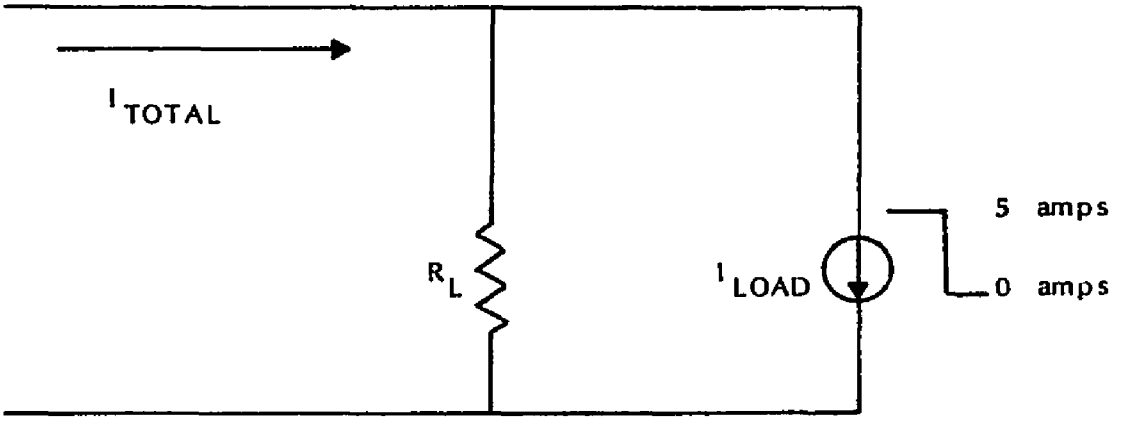
3. Reference Voltage Input Transient Response - V_{REF} is stepped from 0 volts to 5 volts and the output signal waveform is printed out versus time. This response verifies the extent of the compensation (or lack thereof). The amount of transient response overshoot and rise time are parameters that are designed for when the converter is compensated.

4. Load Step Response - The output load resistance is changed from 1 ohm to .5 ohms and then back to 1 ohm. This causes a change of current from

5 amps to 10 amps and back to 5 amps. The circuit used to do this is illustrated in figure 25. To increase the total current (I_{TOTAL}) from 5 amps to 10 amps, a voltage source (V_{LOAD}) in series with a resistor (R_L') is placed in parallel with R_L (R_L' is the same value as R_L). The initial value of V_{LOAD} is set equal to the V_O. When the time comes to increase I_{TOTAL} to 10 amps, V_{LOAD} is stepped to 0 volts. This places R_L' in parallel with R_L and I_{TOTAL} is 10 amps. To decrease the current from 10 amps to 5 amps, R_L is placed in parallel with a current source, I_{LOAD}, that initially has a value of 5 amps. The sum total of the currents flowing through R_L and I_{LOAD} is 10 amps. When I_{TOTAL} is to be decreased from 10 amps to 5 amps, I_{LOAD} is stepped to 0 amps. Now R_L is by itself and only draws 5 amps. Obviously, separate SPICE simulations were run to achieve both load changes. The reason such an involved procedure was used is that the equivalent resistance looking at the load affects the damping of the output variation caused by the load step change. This being the case, the resistance seen by the output filter should be the resistance that is actually drawing the current, not some high



(a) Load Step from 5 Amps to 10 Amps



(b) Load Step from 10 Amps to 5 Amps

Figure 25. Method Used to Simulate Load Current Steps

impedance current source that will have a constant current, whatever the output voltage is. The basic converter model without compensation was simulated to establish a baseline. The results of this, and subsequent simulations, are tabulated in Tables 2 and 3 at the end of this chapter. An evaluation of these results will be given in Chapter 6.

Compensation Criteria

Before compensating the converter, some criteria must be established that will allow a comparison to be made without too many variables being different. Therefore, the following "compensation criteria" will be used:

1. The closed loop -3 dB bandwidth will be designed for 30 krps (4.77 kHz). This corresponds to a transient response rise time (t_R) of 73.3 microseconds.

2. The closed loop transient response will have between a 3% and a 5% overshoot and as short a settling time (t_S) as possible.

3. The compensation techniques will be applied to the uncompensated converter with and without the converter output filter damped to a Q_D of .7071.

As will be seen, not all these conditions will be met with all the compensation techniques.

Damping Resistor Value

The value for the damping resistor, R_D can be found using equation 16, where Q_D is chosen to be .7071

$$R_D = \frac{.7071\sqrt{\frac{50u}{2000u}}}{1 - \frac{.7071\sqrt{\frac{50u}{2000u}}}{1}} .$$

C_D is chosen to be 1 farad, as explained in Chapter 4. When circuit simulations with damping are desired, the series combination of C_D and R_D will be placed in parallel with R_L.

Dominant Pole Compensation Simulation

The DPC technique will be the first one simulated. The location of the dominant pole can be found using the following method:

1. A check must be run to determine if the DPC technique will provide the desired transient response when applied. This can be done by comparing the the Q of the output filter with the Qs given in Table 1 (the Qs in Table 1 are chosen to give a transient response that has less than a 10% overshoot). If the Q of the output filter does not fall within the range specified in Table 1, the

Table 1. Acceptable Q_f s for DPC Design

b	c	Q_f	%OS	t_s
3.3	2.5	.48	5.9	10.8
3.0	2.5	.53	4.2	10.0
2.5	2.5	.63	1.0	0.0
2.0	2.0	.71	8.7	7.0
1.9	2.1	.76	5.1	6.5
2.0	2.5	.79	0.0	8.5
2.0	3.0	.87	0.0	11.3
1.5	2.0	.94	6.7	10.5

output filter will have to be damped to force the Q to the desired value.

2. When the output filter Q is acceptable, the DPC transfer function (equation 17) can be equated to the following equation

$$H_{OL}(s) = \frac{K_{DC}}{\left[\frac{cK_{DC}}{K_f}\, s + 1\right]\left[\frac{1}{cK_f^2}\, s^2 + \frac{b}{cK_f}\, s + 1\right]}, \quad (27)$$

where $$LC = \frac{1}{cK_f^2},$$

$$\frac{L}{R_L'} = \frac{b}{cK_f},$$

and where b and c are the coefficients from Table 1 and K_f is the frequency scaling factor.

3. From equation 27, the frequency scaling factors can be calculated as follows

$$K_f = \sqrt{\frac{1}{(LC)c}},$$

and

$$K_f = \frac{bR_L'}{cL}.$$

4. When K_f is found using the above equations, the DPC circuit component values, R_{DPC} and C_{DPC}, can

be found by using

$$R_{DPC} C_{DPC} = \frac{cK_{DC}}{K_f} .$$

Either R_{DPC} or C_{DPC} can be chosen and the other solved for.

This method was used on the uncompensated buck converter as follows. The Q of the undamped output filter was calculated to be

$$Q = \frac{R_L}{\sqrt{\frac{L}{C}}} = \frac{1}{\sqrt{\frac{50u}{2000u}}}$$

$$= 6.3 .$$

This does not fall within the range specified in Table 1. As it turns out, if the compensation were to continue from this point, a 4% overshoot could be achieved - at the expense of having an extremely long rise and settling time. Needless to say, the DPC technique was not applied to this circuit as it is.

Using damping, the Q of the filter was changed to Q_D = .7071. The desired overshoot is between 3% and 5% with a short settling time. Referring to Table 1, this corresponds to a b and c equal to 1.9 and 2.1, respectively, and a Q of .7600. So as not to create too many differences with the later comparisons, the Q_D of .7071 was retained

rather than designing the damping specifically for a Q_D of .7600. The values of 1.9 and 2.1 were used for b and c. Solving for K_f results in

$$K_{f1} = \sqrt{\frac{1}{(50u)(2000u)(2.1)}}$$

$$= 2182 \text{ rps} ,$$

and

$$K_{f2} = \frac{1.9(1//.126)}{(2.1)(50u)}$$

$$= 2025 \text{ rps} .$$

The reason these values are not the same goes back to the difference between the actual Q used and the Q suggested in Table 1. The average of the two frequency scaling factors was taken and used, giving

$$K_f = \frac{K_{f1} + K_{f2}}{2} = \frac{2182 + 2025}{2}$$

$$= 2100 \text{ rps} .$$

Thus,

$$R_{DPC} C_{DPC} = \frac{cK_{DC}}{K_f} = \frac{(2.1)(1000)}{2100}$$

$$= 1 .$$

Choosing $C_{DPC} = 10$ uF,

$$R_{DPC} = \frac{1.0}{10u}$$

$$= 100k \text{ ohms} .$$

These values were used on SPICE to compensate the buck converter. Unfortunately, the major drawback associated with DPC (loss in closed loop bandwidth) kept the -3 dB closed loop bandwidth requirement from being met. In order to meet the closed loop bandwidth and the transient response requirements, the output filter cutoff frequency would have to be made larger, thereby requiring different values for the output filter capacitor and inductor. Again, trying to limit the differences in circuitry to be compared, the results with smaller closed loop bandwidth were retained. These results are tabulated in Tables 2 and 3 at the end of the chapter.

Two Real Zero Cancellation Compensation Simulation

The method to obtain the pole and zero locations for the TRZCC technique is not as straightforward as for the DPC technique. The steps taken are listed as follows:

1. Make an initial selection for the pole and zero locations. A rule of thumb for placing the zeros is to locate them at one-half the output filter cutoff frequency if the output filter Q is greater than or equal to 1

$$w_{z12} = (0.5)w_{nf} \qquad \text{for } Q \geq 1 .$$

If the output filter Q is less than 1, place the

zeros at the output filter cutoff frequency

$$w_{z12} = w_{nf} \qquad \text{for } Q < 1 .$$

The higher frequency pole, p_2, should be placed at the frequency of any known zeros in the loop. If there are none, p_2 should be placed at a frequency that is at least 10 times that of the desired -3 dB closed loop bandwidth

$$w_{p2} \geq 10 w_{-3dB(CL)} .$$

This is so as not to cause interaction that might degrade the compensation effects of the two real zeros. The lower frequency pole, p_1, should be placed at a frequency that will allow the open loop gain to roll off with a slope of -20 dB/decade from w_{p1}, through the 0 dB asymptote at a frequency equal to the closed loop -3 dB bandwidth (this assumes the real zeros cancel most of the effects of the complex poles). This can be done by placing p_1 at a frequency that is $\frac{1}{K_{DC}}$ of the closed loop -3 dB bandwidth

$$w_{p1} = \frac{1}{K_{DC}} w_{-3dB(CL)} .$$

2. With the initial selection of these pole and zero

locations, the closed loop transfer function coefficients must be found using equation 21. From this equation, the magnitude at DC and at the -3 dB bandwidth frequency must be solved for to see if the selected pole and zero locations actually give a magnitude that is down -3 dB at the desired -3 dB bandwidth frequency

$$20 \text{ Log} \left[\frac{\left| H_{CL}(w = w_{-3dB}) \right|}{\left| H_{CL}(w = 0) \right|} \right] \stackrel{?}{=} -3 \text{ dB} .$$

3. If the calculated gain magnitude from step 2 is significantly greater than -3 dB (i.e., closer to 0 dB), then p_1 must be shifted to a lower frequency. Likewise, if the gain magnitude is significantly less than -3 dB, p_1 must be shifted to a higher frequency. Select another location for w_{p1} and repeat step 2 until the gain magnitude at the -3 dB bandwidth frequency is 3 dB down from the gain at DC.

4. When the the pole and zero locations have been selected to give the correct -3 dB bandwidth, the next step is to see if these same pole and zero locations will provide the correct transient response. This can be accomplished by whatever method is available. The overall converter with

the selected pole and zero locations can be modelled on SPICE to see if the resulting transient response is correct; or, the transient response can be solved for by hand by finding the roots of the closed loop transfer function, applying an s-domain step function ($\frac{1}{s}$), and taking the inverse laplace transform to find the time domain step response. Values of time can then be substituted into this time domain equation and the transient response characteristic can be found. When this characteristic is known, if the overshoot is significantly larger than desired, the two real zeros must be shifted to a lower frequency (to provide more phase lead before the complex poles begin to affect the loop phase shift). Similarly, if the overshoot is smaller than desired, the zero locations must be shifted to a larger frequency.

5. Steps 2 through 4 must be repeated until the final compensation pole and zero locations give the desired closed loop bandwidth and transient response. When the final locations have been determined, the pole and zero frequencies can be equated with equations 19a and 19b and the component values can be found using the following equations

Circuit A

Choose $$R_F = R_1 = R \ . \qquad (28a)$$

Solving for R_A:

$$\frac{\frac{1}{C_A(R_A + R_1)}}{\frac{1}{R_A C_A}} = \frac{w_{z12}}{w_{p2}}$$

$$\frac{R_A}{R_A + R_1} = \frac{w_{z12}}{w_{p2}}$$

$$R_A = \frac{R_1}{\frac{w_{p2}}{w_{z12}} - 1} \ . \qquad (28b)$$

Solving for R_B:

$$\frac{\frac{1}{C_B(R_B + R_F)}}{\frac{1}{R_B C_B}} = \frac{w_{p1}}{w_{z12}}$$

$$\frac{R_B}{R_B + R_F} = \frac{w_{p1}}{w_{z12}}$$

$$R_B = \frac{R_F}{\frac{w_{z12}}{w_{p1}} - 1} \ . \qquad (28c)$$

Solving for C_A:

$$\frac{1}{R_A C_A} = w_{p2}$$

$$C_A = \frac{1}{w_{p2} R_A} . \qquad (28d)$$

Solving for C_B:

$$\frac{1}{R_B C_B} = w_{z12}$$

$$C_B = \frac{1}{w_{z12} R_B} . \qquad (28d)$$

Circuit B (the derivation of these equations is given in Appendix B)

Let

$$a = \frac{1}{w_{z12}^2} ,$$

$$b = \frac{2}{w_{z12}} ,$$

$$c = \frac{1}{w_{p1} w_{p2}} ,$$

$$d = \frac{1}{w_{p1}} + \frac{1}{w_{p2}} .$$

Choose

$$C_4 = C_4 . \tag{29a}$$

$$R_4 = \frac{c - a}{bC_4} , \tag{29b}$$

$$C_2 = \frac{C_4(b^2 - db + c - a)}{a - c} , \tag{29c}$$

$$R_3 = \frac{1}{C_2}\left[b - \frac{a}{C_2 R_4}\right], \tag{29d}$$

$$C_1 = \frac{a}{C_2 R_3 R_4} . \tag{29e}$$

The methods described above were implemented on the undamped buck converter (Q = 6.32) with the following results for TRZCC zero and pole locations

$$w_{z1} = w_{z2} = w_{z12} = 1700 \text{ rps} ,$$

$$w_{p1} = 7 \text{ rps} ,$$

$$w_{p2} = 300k \text{ rps} .$$

Substituting these values into equations 28 and 29 gives

Circuit A $R_F = R_1 = 10k \text{ ohms} ,$

$R_A = 57 \text{ ohms} ,$

$R_B = 41.3 \text{ ohms} ,$

$C_A = 58.5$ nF ,

$C_B = 14.2$ μF .

Circuit B $C_4 = 1$ nF ,

$R_4 = 110.6$k ohms ,

$C_2 = 1.3$ μF ,

$R_3 = 917.5$ ohms ,

$C_1 = 2.66$ nF .

These two circuits were used to compensate the undamped buck converter, with the results tabulated in Tables 2 and 3 at the end of this chapter.

The TRZCC technique was also applied to the damped buck converter ($Q_D = .7071$). The pole and zero locations for this are given as follows

$w_{z1} = w_{z2} = w_{z12} = 3.16$k rps ,

$w_{p1} = 25$ rps ,

$w_{p2} = 300$k rps .

Substituting these values into equations 28 and 29 gives

Circuit A $R_F = R_1 = 10$k ,

$R_A = 106$ ohms ,

$R_B = 80$ ohms ,

$C_A = 31.5$ nF ,

$C_B = 3.96$ μF .

Circuit B $C_4 = 1$ nF ,

$R_4 = 52.7$k ohms ,

$C_2 = .746$ μF ,

$R_3 = 844$ ohms ,

$C_1 = 3$ nF .

Applying these two circuits to the damped buck converter gives the results that are tabulated in Tables 2 and 3 at the end of the chapter.

Complex Zero Cancellation Compensation Simulation

The CZCC technique is, by far, the easiest to implement. The method used to obtain CZCC component values is outlined as follows:

1. Solve for the denominator of the output filter transfer function

$$D_f(s) = LCs^2 + \frac{L}{R_L} s + 1 .$$

2. Equate this equation with the numerator of equation 19b (this step places the compensation zeros on

top of the filter poles)

$$C_1C_2R_3R_4s^2 + R_3(C_1 + C_2)s + 1 = LCs^2 + \frac{L}{R_L}s + 1 ,$$

where

$$LC = C_1C_2R_3R_4 = a ,$$

$$\frac{L}{R} = R_3(C_1 + C_2) = b .$$

3. From the closed loop specifications, solve for the closed loop denominator using

$$D_{CL}(s) = \left[\frac{1}{w_{-3dB}^2}\right]s^2 + \left[\frac{1}{w_{-3dB}Q_{CL}}\right]s + 1 .$$

4. Equate this equation with a slightly modified form of equation 23

$$\left[\frac{1}{w_{-3db}^2}\right]s^2 + \left[\frac{1}{w_{-3dB}Q_{CL}}\right]s + 1 =$$

$$\left[\frac{1}{w_{p1}w_{p2}\left(1 + \frac{R_FV_S}{R_1V_M}\right)}\right]s^2 + \left[\frac{\frac{1}{w_{p1}} + \frac{1}{w_{p2}}}{1 + \frac{R_FV_S}{R_1V_M}}\right]s + 1$$

where

$$\frac{1}{w_{-3dB}} = \frac{1}{w_{p1}w_{p2}\left[1 + \frac{R_FV_S}{R_1V_M}\right]} ,$$

or

$$\frac{1}{w_{p1}w_{p2}} = \frac{1 + \frac{R_F V_S}{R_1 V_M}}{w_{-3dB}} = c \ , \qquad (30a)$$

and

$$\frac{1}{w_{-3dB}Q_{CL}} = \frac{\frac{1}{w_{p1}} + \frac{1}{w_{p2}}}{1 + \frac{R_F V_S}{R_1 V_M}}$$

$$\frac{1}{w_{p1}} + \frac{1}{w_{p2}} = \frac{1 + \frac{R_F V_S}{R_1 V_M}}{w_{-3dB}Q_{CL}} = d \ . \qquad (30b)$$

5. Since the overall objective is to solve for the component values, equations 30a and 30b can be equated with equation 19b to give

$$c = \frac{1}{w_{p1}w_{p2}} = R_3R_4[C_1C_2 + C_4(C_1 + C_2)]$$

$$d = \frac{1}{w_{p1}} + \frac{1}{w_{p2}} = R_3(C_1 + C_2) + R_4(C_2 + C_4)$$

6. The equations for giving the component values using a, b, c, and d can be found in the previous section (equation 29).

These six steps were programmed into an HP-41C calculator with the listing for the program given in Appendix B, along with the derivation of the equations for the component values (portions of the program can also be used to solve for the TRZCC, circuit B component values).

The calculator program (called TEE) was used to solve for the modified bridged tee component values to compensate the undamped and damped buck converter. The component values chosen are given as follows

Undamped

$C_4 = .1\ \mu F$,

$R_4 = 202k$ ohms ,

$C_2 = .132\ \mu F$,

$R_3 = 348$ ohms ,

$C_1 = .011\ \mu F$.

Damped

$C_4 = .01\ \mu F$,

$R_4 = 226.5k$ ohms ,

$C_2 = .196\ \mu F$,

$R_3 = 2.26k$ ohms ,

$C_1 = 993\ pF$.

The results of using this compensation technique are tabulated in Tables 2 and 3 in the following section.

Tabulation of Results

The following two tables give the results of all the SPICE runs completed for the buck converter designed at the beginning of this chapter. Table 2 gives the results of the AC open and closed loop responses to verify the location of the compensation poles and/or zeros. Table 3 gives the results of the input transient and load transient responses. These tables will be evaluated in the following chapter.

Table 2. Open and Closed Loop AC Response Results

Compensation Technique	w_{nf}	w_{p1}	w_{p2}	w_{z1}	w_{z2}	ϕ_M	w_{-3dB}
None	3150	--	--	--	--	.256	99.6k
Damping	3150	--	--	--	--	2.4	99.6k
CZCC	--	20.1	42k	--	--	65	29k
CZCC w/ Damping	--	20.1	42k	--	--	65	29k
DPC	--	--	--	--	--	--	--
DPC w/ Damping	3100	.942	--	--	--	63	2k
TRZCC (Ckt. A)	3149	7.0	276k	1772	1772	79	30.1k
TRZCC (Ckt. A) w/ Damping	3149	25	283k	3020	3020	79	31.5k
TRZCC (Ckt. B)	3147	7.1	280k	1771	1771	78	30.1k
TRZCC (Ckt. B) w/ Damping	3140	25	289k	3140	3140	80	30.2k

Table 3. Input and Step Transient Response Results

Compensation Technique	t_R(μs)	%OS	(1%) t_S(mS)	% V_{UP}	(0.1%) t_S(mS)	% V_{DN}	(0.1%) t_S(mS)
None	13	92	--	-.481	1.4	.459	1.4
Damping	12	92	--	-.979	--	.991	--
CZCC	75	4.1	.240	-1.72	10	1.76	10
CZCC w/ Damping	75	3.9	.220	-1.85	1.5	1.87	1.5
DPC	--	--	--	--	--	--	--
DPC w/ Damping	1200	4.2	3.2	-6.5	4.6	6.86	4.2
TRZCC (Ckt A)	71	5.0	3.1	-1.62	2.4	1.62	2.4
TRZCC (Ckt A) w/ Damping	76	3.0	.890	-1.27	1.3	1.24	1.3
TRZCC (Ckt B)	71	5.0	3.1	-1.77	2.47	1.62	2.45
TRZCC (Ckt B) w/ Damping	72	4.4	.860	-1.44	1.36	1.47	1.36

CHAPTER 6

LOAD TRANSIENT RESPONSE EVALUATION

This chapter will be used to evaluate the results of the SPICE simulation that are documented in Tables 2 and 3 at the end of Chapter 5. This evaluation will then be used to present guidelines that can be used in selecting the compensation for a buck converter that will used under varying load conditions.

Observations

For the most part, the open and closed loop circuit simulation responses were pretty close to the design objectives (except, of course, for the expected loss in closed loop bandwidth for the DPC simulation). Most of the apparent errors in determining the open and closed loop pole and zero locations can be explained by the fact that their determination was based on looking at the phase and gain plots and printout, and making a best guess as to where the given poles and zeros were located. This was a difficult task in the regions where the phase and/or gain characteristics of the poles and zeros overlapped.

Another interesting observation is the fact that the maximum phase shift (while the open loop gain was

greater than 0 dB) of all but two of the simulations with compensation used was around 120 degrees. This indicates that for an input transient response with a 4% overshoot, the most the open loop phase should be allowed to shift while the open loop gain is greater than 0 dB is 120 degrees.

There are three general observations that can be made about the load transient response results given in Table 3.

The first observation is that the load transient results for the DPC technique are the worst of the simulation runs, with the output voltage varying in excess of 6.5% (.325 volts) with a settling time greater than 4 mS. This, coupled with the fact that the -3 dB closed loop bandwidth requirement could not be achieved (meaning the rise time is longer for this circuit than when the other compensation techniques are used), makes the DPC technique the least desirable one to use.

The second observation deals with the comparison of the results of the TRZCC compensation technique with the results of the CZCC technique. It appears that the TRZCC technique is, by far, the better of the two when no damping is used (10 mS settling time for CZCC compared to only 2.47 mS for TRZCC). When damping is used, the

TRZCC still comes out as being slightly better than CZCC ($\pm$ 1.27% change in output voltage with 1.3 mS settling time for TRZCC versus $\pm$ 1.85% change in output voltage with 1.5 mS settling time for CZCC).

The third observation is that there appears to be a slight difference in the results when using circuit A as opposed to using circuit B. Circuit A appears to have a slightly better response under both damped and undamped conditions

Circuit A (damped)	$V_O = \pm$ 1.62%	t_S = 2.40 mS
Circuit B (damped)	$V_O = {}^{+\ 1.79\%}_{-\ 1.77\%}$	$t_S = {}^{2.45\ \text{mS}}_{2.47\ \text{mS}}$
Circuit A (undamped)	$V_O = \pm$ 1.27%	t_S = 1.30 mS
Circuit B (undamped)	$V_O = {}^{+\ 1.47\%}_{-\ 1.44\%}$	t_S = 1.36 mS

Part of this difference may be due the convergence criteria of the SPICE simulation program and the complexity of circuit B as compared to circuit A. Circuit B has three reactive components whereas circuit A only has two. Also, circuit B is in a split tee configuration. Both of these circuit topology characteristics might force SPICE to converge to a slightly different "correct" value.

Mathematical Characterization of Load Transient Response

This section will be used to derive a mathematical representation of the load transient response in order to have something to compare the results of the simulations with.

The first step in this procedure is to define a simplified circuit model that will establish the output characteristics of the converter before and after the load transient occurs. This is easily done as shown in Figure 26, which shows a buck converter with its gain stages and compensation stage. The parameters that dictate the output characteristics before the load transient occurs are the initial conditions that are present in the actual circuit, with the voltage across the capacitor being the same as the output voltage of the converter

$$V_C(t=0_-) = V_O(t=0_-)$$

and the current flowing through the inductor being the same as the output load current

$$I_L(t=0_-) = I_O(t=0_-)$$

The step input of V_{REF} is used to establish the final (steady state) output characteristics that will be present after the load transient has occurred and the initial

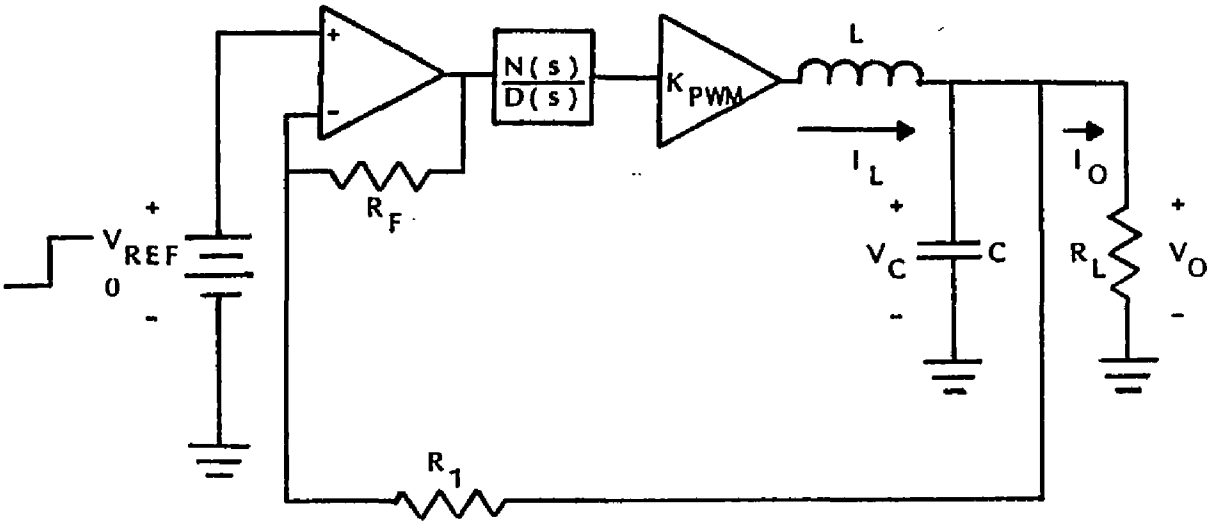


Figure 26. Circuit Model for Mathematical Characterization of Load Step Response

conditions have died out. Thus, the load transient has been modelled by a set of initial conditions and an input step in reference voltage.

The transfer function of the circuit model in Figure 26 was found with the help of the circuit shown in Figure 27. The initial conditions have been modelled by impulse voltage and current generators (Huelsman 1972). Applying standard circuit analysis techniques to this circuit, V_O can be found in terms of V_B (the input of the output filter), given as follows

$$V_O(s) = \frac{V_B + K_L K_{IR} + K_C K_{IR} Ls}{LCs^2 + \frac{L}{R_L} s + 1} , \qquad (31)$$

where $K_L = I_L(0_-)L$

$K_C = V_C(0_-)C$

and K_{IR} = Impulse Response Input

solving for V_B in terms of V_O and V_{REF} gives

$$V_B(s) = \left[1 + \frac{R_F}{R_1}\right] V_{REF} - \left[\frac{R_F}{R_1}\right] V_O \left[\frac{N(s)}{D(s)}\right] K_{PWM}$$

$$\cong \frac{R_F}{R_1} V_{REF} - \frac{R_F}{R_1} V_O \frac{N(s)}{D(s)} K_{PWM} , \qquad (32)$$

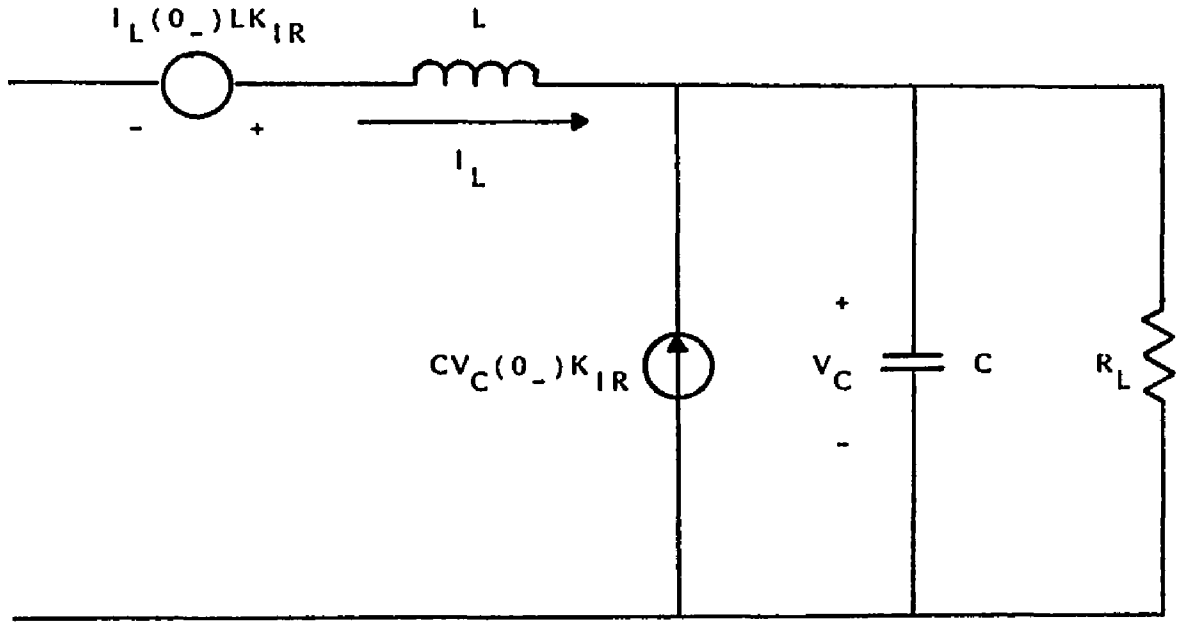


Figure 27. Circuit Model using Impulse Generators to Control Initial Conditions

Substituting equation 32 into 33 and solving for V_O yields

$$V_O(s) = \frac{\frac{R_F N(s) K_{PWM}}{R_1 D(s)} V_{REF}}{LCs^2 + \frac{L}{R_L} s + 1 + \frac{R_F N(s) K_{PWM}}{R_1 D(s)}} \qquad (33)$$

$$+ \frac{K_{IR} K_L + K_{IR} K_C L s}{LCs^2 + \frac{L}{R_L} s + 1 + \frac{R_F N(s) K_{PWM}}{R_1 D(s)}} .$$

To generate a steady state final output voltage of $V_O(0_-)$, V_{REF} should be a step function of magnitude $V_O(0_-)$

$$V_{REF}(s) = \frac{V(0_-)}{s}$$

Applying this step function to equation 33, assuming for the moment that $\frac{N(s)}{D(s)}$ is 1, and taking the inverse laplace transform of the resulting equation gives the following results

$$v_O(t) = K_1 \left[\frac{1}{a^2 + b^2} + \frac{1}{b\, a^2 + b^2} e^{-at} \sin(bt - \phi_1) \right] \qquad (34)$$

$$+ K_2 \left[\frac{1}{b} e^{-at} \sin(bt) \right] + K_3 \left[\frac{a^2 + b^2}{b} e^{-at} \sin(bt + \phi_1) \right],$$

where $$\phi_1 = \tan^{-1} \frac{b}{-a} ,$$

$$a = \frac{1}{2R_L(0_+)C} ,$$

$$b = \frac{\frac{R_F K_{PWM}}{R_1}}{LC} - a^2 ,$$

$$K_1 = \frac{\left[\frac{R_F K_{PWM}}{R_1}\right] V_O(0_-)}{LC} ,$$

$$K_2 = \frac{V_O(0_-)}{R_L(0_-)C} ,$$

and

$$K_3 = V_O(0_-) .$$

Applying this equation to the uncompensated, undamped buck converter, the hand calculated results were compared with the SPICE simulation results and tabulated in Table 4. The correlation between the hand calculations and the computer simulations is very good. The calculated peak change in output voltage is within .04% of the simulated value. The settling time calculated results (1.4 mS) are exactly the same as the simulation results. The largest difference occurs at 700 uS with a 0.4% discrepancy. Based on this comparison, equation 33 appears to be the governing equation for load transient response.

Application of Governing Equation

The intent of this section is to apply equation 33 to each of the compensation techniques in an effort to find out what causes the differences in the load tran-

TABLE 4. Load Transient Response Comparison of SPICE Simulation and Equation 34

Time(uS)	(SPICE) V_O (volts)	(EQ. 34) V_O (volts)
0	5.050	5.050
5	5.042	5.038
10	5.032	5.032
20	5.026	5.026
40	5.063	5.065
45	5.070	5.073
50	5.072	5.074 *
55	5.070	5.070
60	5.065	5.061
70	5.042	5.037
80	5.028	5.026
100	5.051	5.060
150	5.031	5.033
200	5.046	5.030
400	5.042	5.035
700	5.057	5.035
1000	5.041	5.053
1380	5.046	5.047
1400	5.042	5.042

* Peak Output Voltage Change

sient response tabulated in Table 3. The evaluation will be done in general terms.

Applying the general compensation network transfer function

$$\frac{N(s)}{D(s)} = \frac{as^2 + bs + 1}{c^2 + ds + 1}$$

to equation 33 and simplifying gives

$$V_O(s) = \frac{K_L K_{IR}\left(1 + \frac{K_C L}{K_L} s\right)(as^2 + bs + 1)}{\left(LCs^2 + \frac{L}{R_L} s + 1\right)(cs^2 + ds + 1) + K_{DC}(as^2 + bs + 1)} + \frac{K_L K_{IR}\left(1 + \frac{K_C L}{K_L} s\right)(cs^2 + ds + 1)}{\left(LCs^2 + \frac{L}{R_L} s + 1\right)(cs^2 + ds + 1) + K_{DC}(as^2 + bs + 1)} \quad (35)$$

where $K_L = I_L(0_-)$,

$$\frac{K_C L}{K_L} = R_L(0_-)C ,$$

and $$K_{DC} = \frac{R_F K_{PWM}}{K_L} .$$

Applying equation 35 to each compensation technique (in general terms) yields the following equations

DPC: (a = b = c = d)

$$V_O(s) = \frac{K_{DC}K_{REF}}{(LCs^2 + \frac{L}{R_L}s + 1)(ds + 1) + K_{DC}}, \quad (36)$$

$$+ \frac{K_L K_{IR}(1 + \frac{K_C L}{K_L}s)(ds + 1)}{(LCs^2 + \frac{L}{R_L}s + 1)(ds + 1) + K_{DC}}$$

CZCC: $(a = LC,\ b = \frac{L}{R_L})$

$$V_O(s) = \frac{K_{DC}V_{REF}}{(cs^2 + ds + 1 + K_{DC})} \quad (37)$$

$$+ \frac{K_L K_{IR}(1 + \frac{K_C L}{K_L}s)(cs^2 + ds + 1)}{(cs^2 + ds + 1)(as^2 + bs + 1) + K_{DC}(as^2 + bs + 1)}$$

TRZCC: (Refer to equation 35)

Based on the above equations, the reason that a small inductor value is desired in the circuit design for improved load transient response is that it reduces the impulse response term (IR) of each of the equations above. This would have the effect of reducing the overall output voltage change due to load transients.

Pole-zero diagrams for each of the equations (35, 36, and 37) were drawn to see if they revealed any further

information. This is shown in Figure 28. The pole and zero locations of the IR term appear to be a modified combination of the compensation network pole-zero locations and closed loop pole-zero locations. The compensation network poles and zeros are transformed to zeros and poles, respectively, in the IR term. The closed loop poles remain as they are for the IR term. The closed loop zeros are the same as the compensation network zeros, which are already included in the IR term. These transformations, as well as the additional zero which is a function of the initial conditions, dictate the differences seen in the transient responses given in Table 3 (this is based on the assumption that the step responses of each of the compensated converters is approximately equal, which it should be based on the compensation criteria established in Chapter 5).

Following are the observations made about the different compensation techniques based on the pole-zero diagrams and equations 35, 36, and 37:

1. One of the reasons that the DPC technique causes a larger change in output voltage under load transient conditions is that there are two dominant zeros in the IR term (this statement neglects

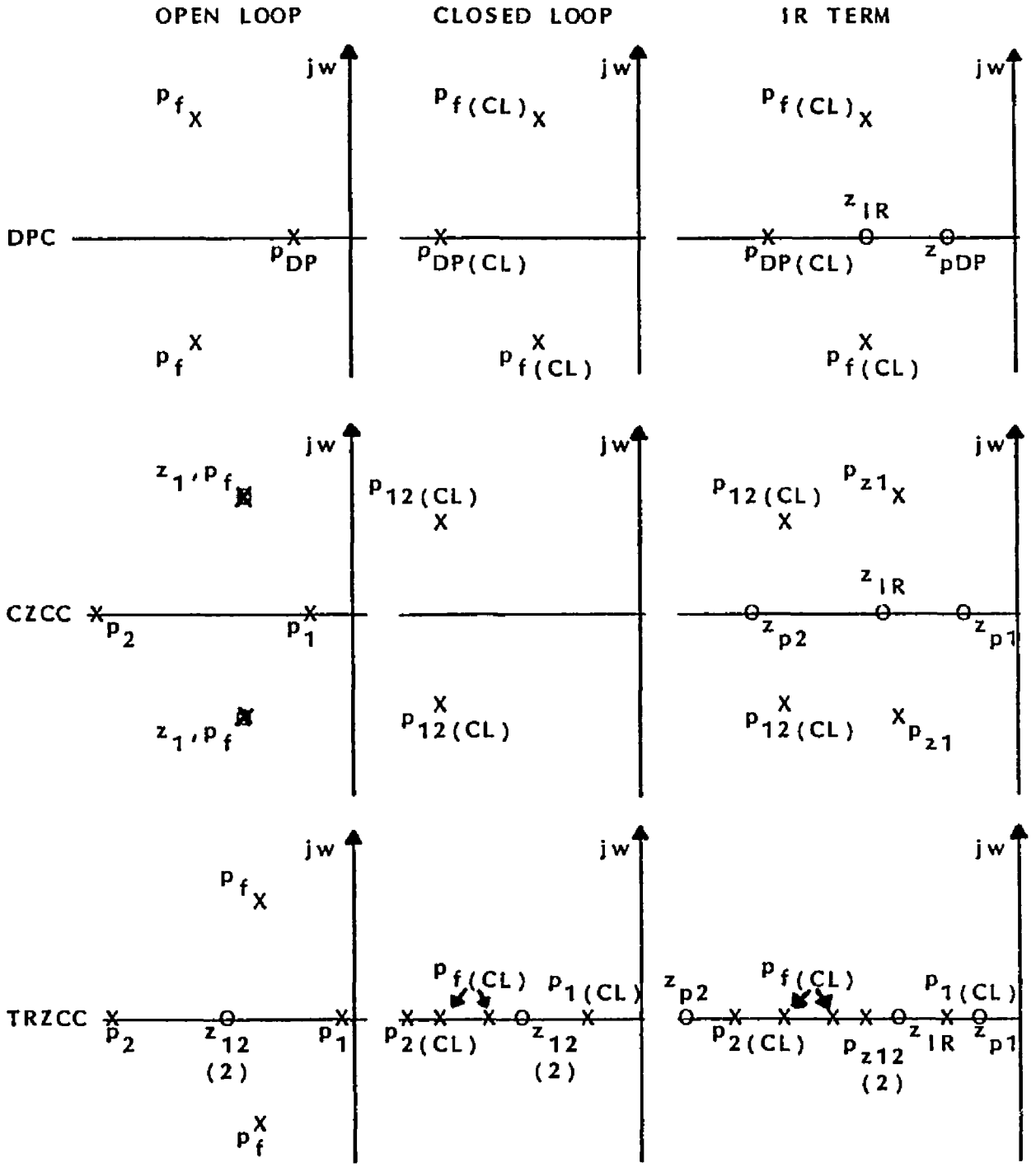


Figure 28. Pole-Zero Diagrams of Open Loop, Closed Loop, and IR Term Functions

the differences in step response that are obviously there due to the differences in -3 dB bandwith). These two zeros will have the tendency to increase the magnitude of the time response of the IR term which, in turn, increases the change in output voltage.

2. The reason that the TRZCC technique is better than the CZCC technique is due to the real poles and zeros evident in the IR term of the TRZCC transient response equation. As a result, the time magnitude of the TRZCC's IR term will be less, as will be its settling time. The CZCC IR term, on the other hand, contains four complex poles. Two of these poles are the transformed "cancelling zeros" from the compensation network. If the open loop response had high Q output filter poles, the cancelling zeros which were designed to cancel these poles are also high Q. This now causes two high Q poles to be created in the IR term. Now it can be seen why the settling time of the undamped CZCC filter is so long (10 mS). The high Q "transformed" poles prolonged the transient response. When damping was applied, this shifted the output filter poles away from the jw axis

and allowed the "cancelling" zeros to have a lower Q. This was transformed to the IR term as two lower Q poles, which did not as adversly affect the load transient response. The settling time was appreciably better (1.5 mS).

3. There is nothing that is evident in the equations or in the pole-zero diagrams that would explain why the circuit A implementation of the TRZCC technique should be any better than the circuit B implementation. This further lends to the theory that it was a convergence difference within SPICE that created the discrepancies, not the configuration of the circuits.

The fact that the TRZCC closed loop response and the IR term had all real zeros and poles is a curious phenomena. Apparently, the output filter complex pole pair moves to the real axis and splits. While one of the two poles heads for one of the two compensating zeros located at a lower frequency, the other pole heads towards the high frequency compensation pole. When these two poles meet, they break away from the real axis and head for the zeros located at infinity. Further investigation of this phenomena is beyond the scope of this thesis. It

would be beneficial, however, to find out how to purposely achieve it, as can be seen by the simulation results.

Compensation Guidelines

Based on the information from the last section, several guidelines can be suggested for the compensation of buck converters that will be used under load transient conditions.

1. First of all, in the original design of the converter, make the inductor as low in value as reasonably possible in order to reduce the IR term in the transient response equation.

2. If the CZCC technique is going to be used (it is the easiest to implement), the Q of the output filter complex poles must be damped so as not to create a high Q, "transformed" pole in the IR term of the load transient response equation.

3. The DPC technique should be avoided if possible. Not only does the dominant pole in the open loop response convert to a dominant zero in the IR term, thereby causing a larger change in output voltage when the load changes, but the loss in bandwidth associated with the use of this technique creates

a very slow loop response. This reduces the capability of the loop to respond quickly to variations in input or output voltage. As a result, the output voltage regulation is degraded.

4. If a compensation technique other than those covered in this thesis is used, the open loop poles and zeros should be selected such that the closed loop poles and zeros are located on the real axis (similar to the TRZCC technique) and the location of the compensation network zeros should be carefully selected so as not to cause high Q poles in the IR term.

Implementing these four suggestions should result in a buck converter design that will work acceptably well under load transient conditions.

CHAPTER 7

SUMMARY AND CONCLUSIONS

In concluding this thesis, the effects of compensation on load transient response have been explored and characterized. Guidelines have been developed that will aid the circuit designer in designing a buck converter that will operate with reasonable success in a load transient environment.

These goals were achieved by first developing a circuit model that could simulate a buck converter's open loop, closed loop, input transient, and load transient responses. Chapter 2 took care of this aspect of the thesis. From this circuit model, the open and closed loop response equations were developed in Chapter 3 to aid in the analysis and evaluation of the transient response comparisons for the buck converter.

Chapter 4 was then used to give insight into the need for compensation and presented an overview of the different forms of compensation used in industry. Also presented in Chapter 4 was an introduction to a new form of compensation that used complex zeros to cancel the effects of the output filter complex poles, rather than real zeros or poles.

Chapter 5 was used to describe the process an engineer goes through in designing a buck converter from specifications given to him. This process was then used to design a sample converter in order to model it on SPICE. This was successfully done with the results of the SPICE simulation tabulated in Tables 2 and 3. Chapter 6 then evaluated this tabulated data with emphasis placed on looking at the load transient response data from Table 3. To aid in determining why the different compensation techniques changed the transient response characteristics, a general mathematical model was generated which put the load transient response in equation form. This equation was then evaluated in terms of its poles and zeros and certain load transient response characteristics could be seen to be affected by the form of the equation. From this evaluation of the equation, guidelines were developed that would aid a designer in developing a converter that would not be as susceptible to load changes.

Appendix A

EFFECTS OF PARASITIC RESISTANCES ON CONVERTER RESPONSE

In actual hardware, the output filter contains additional damping in the form of the wire resistance in the inductor (R_S) and the ESR of the capacitor (R_{ESR}). These parasitic resistances will reduce the effective Q of the output filter, thereby reducing the closed loop system Q and improving the closed loop input transient response. Unfortunately, the ESR of the capacitor also creates a mid-to-high frequency zero that increases the complexity of the open loop response and makes it more difficult to compensate the converter. The output filter transfer function with the parasitic resistances included is

$$H_f(s) = \frac{CR_{ESR}s + 1}{\left[\frac{LC(R_L + R_{ESR})}{R_S + R_L}\right]s^2 + \left[\frac{C(R_L R_S + R_{ESR}R_S + R_{ESR}R_L) + L}{R_S + R_L}\right]s + 1},$$

where $$w_{nf} = \sqrt{\frac{R_S + R_L}{LC(R_L + R_{ESR})}},$$

and $$Q_f = \frac{1}{w_{nf}\left[\frac{C(R_L R_S + R_{ESR}R_S + R_{ESR}R_L) + L}{R_S + R_L}\right]} .$$

$$w_z = \frac{1}{CR_{ESR}}$$

The denominator can be simplified by assuming

$$R_L >> R_S$$

and

$$R_L >> R_{ESR}$$

This is usually a good assumption to make unless high output current levels (low values of R_L) are being used. With these assumptions made

$$w_{nf} = \sqrt{\frac{1}{LC}} ,$$

$$Q_f = \frac{1}{w_{nf}C(R_S + R_{ESR}) + \frac{L}{R_L}}$$

$$= \frac{1}{\frac{1}{Q_C} + \frac{1}{Q_F}} ,$$

where Q_C is the unloaded Q of the filter (Demaw 1978), defined by the equation

$$Q_C = \frac{|Z_C(w = w_{nf})|}{|R_{eq(unloaded)}|}$$

$$= \frac{\frac{1}{w_{nf}C}}{R_L + R_{ESR}}$$

$$= \frac{1}{w_{nf}[C(R_S + R_{ESR})]} ,$$

and where Q_L is the loaded Q of the filter, defined by the equation

$$Q_L = \frac{|R_{eq(loaded)}|}{|Z_L(w = w_{nf})|}$$

$$= \frac{R_S + R_L}{w_{nf}L}$$

$$= \frac{R_L}{w_{nf}L} .$$

The zero at $\frac{1}{R_{ESR}C}$ will cause the gain stage slope to change from -40 dB/decade to -20 dB/decade and the phase eventually to begin increasing with a slope of +45 degrees/decade. If the zero is low enough in frequency, it can actually help the uncompensated closed loop system response by keeping the phase shift from reaching 180 degrees before the gain crosses the 0 dB asymptote, as shown in Figure 29. In this figure, the phase shift of the zero reduces the slope of the complex pole phase shift enough to keep the overall open loop phase shift from exceeding 135 degrees (shown with the dark lines in

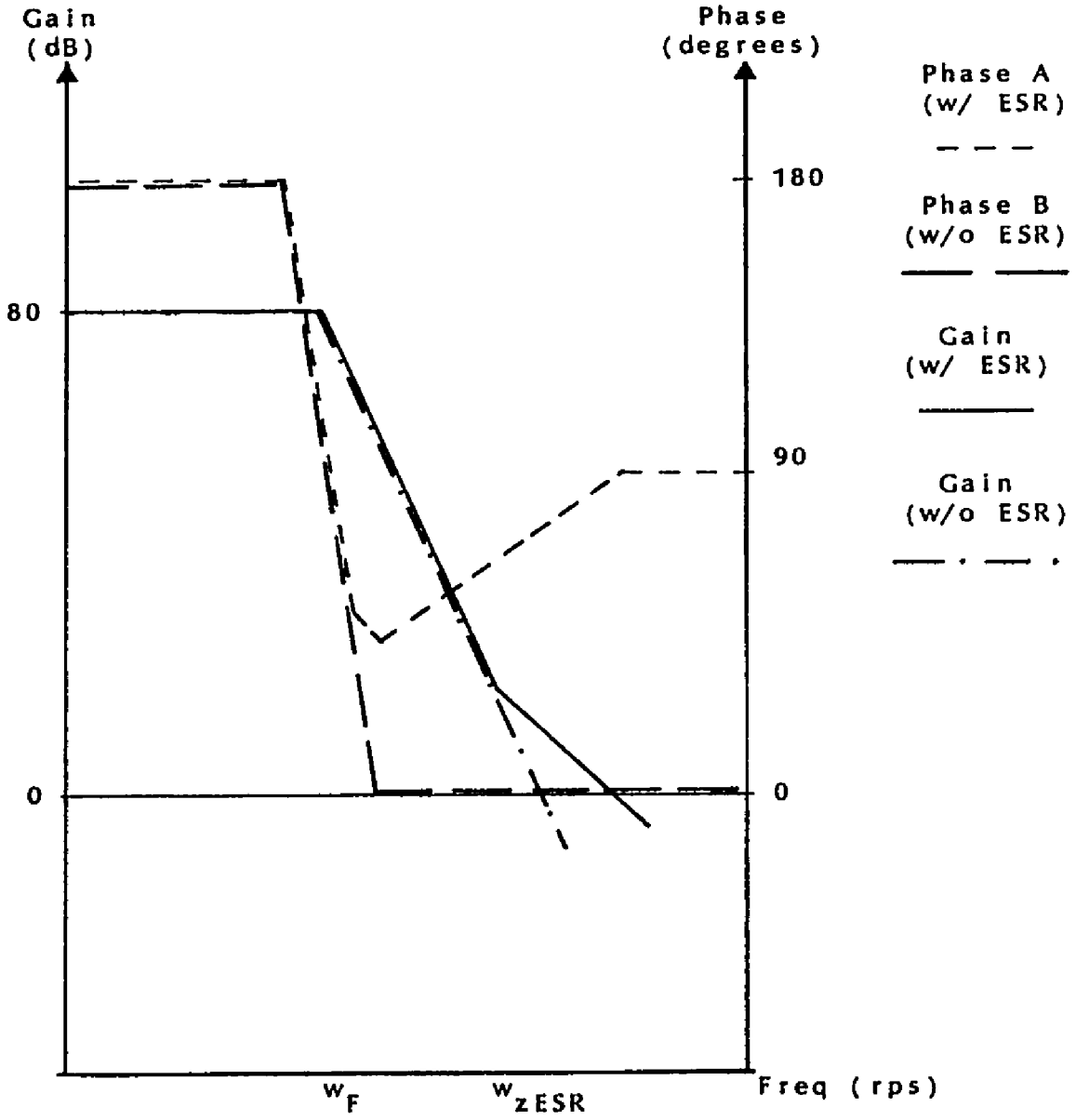


Figure 29. Compensation Effects of Zero Caused by R_{ESR}

Figure 29). Otherwise, the open loop phase shift would have continued down at a rate of -90 degrees/decade and would have reached the 180 degree asymptote before the gain is anywhere near 0 dB (shown with the dashed lines in Figure 29).

Unfortunately, the ESR of the capacitor is not always that predictable and should not be depended on to provide adequate compensation from converter to converter (especially if the converters are to be built for mass production). Therefore, some other form of compensation is usually required. When this is the case, the additional ESR created zero makes it more difficult to determine the location of the compensation poles and zeros (especially in the case where the compensation must be determined by iteratation such as the TRZCC technique). In most cases, the power supply designer will cancel the zero, thereby simplifying the compensation process.

The standard method used to cancel the zero is to place a capacitor, C_F, in parallel with R_F in the error amplifier circuit. This creates a pole in the open loop response that can be adjusted to exactly cancel the ESR zero by choosing C_F such that

$$C_F = \frac{R_{ESR}C}{R_F}$$

If the TRZCC technique is being used, there is already a higher frequency pole, p_2, in the transfer function that can be used to cancel the ESR zero. Either method will work.

Appendix B

MODIFIED BRIDGED-TEE CIRCUIT

Figure 22b in Chapter 4 illustrates the modified bridged-tee circuit that can be used to implement the TRZCC and CZCC techniques. The transfer function of this circuit is given by equation 19b, repeated here for ease of reference

$$H_{TEE}(s) = \frac{C_1C_2R_3R_4s^2 + R_3(C_1 + C_2)s + 1}{R_3R_4[C_1C_2 + C_4(C_1 + C_2)]s^2 + [R_3(C_1 + C_2) + R_4(C_2 + C_4)]s + 1} \quad . \quad (38)$$

When the coefficients of the desired modified bridged-tee transfer function are known

$$H_{COEFF}(s) = \frac{as^2 + bs + 1}{cs^2 + ds + 1} \quad , \quad (39)$$

the component values in terms of these known coefficients can be found in the following manner.

Equating equation 38 with equation 39 gives

$$a = C_1C_2R_3R_4 \quad , \quad (40)$$

$$b = R_3(C_1 + C_2) \quad , \quad (41)$$

$$c = R_3 R_4 [C_1 C_2 + C_4 (C_1 + C_2)$$

$$= C_1C_2R_3R_4 + R_4C_4[R_3(C_1 + C_2) , \qquad (42)$$

$$d = R_3(C_1 + C_2) + R_4(C_2 + C_4)$$

$$= R_3(C_1 + C_2) + R_4C_2 + R_4C_4 . \qquad (43)$$

Substituting equations 40 and 41 into equations 42 and 43 results in

$$c = a + R_4C_4b , \qquad (44)$$

$$d = b + R_4 C_2 + R_4 C_4 . \qquad (45)$$

Solving for R_4C_4 using equation 44 yields

$$R_4 C_4 = \frac{c - a}{b} , \qquad (46)$$

and substituting this equation into equation 45 gives

$$d = b + R_4 C_2 + \frac{c - a}{b} . \qquad (47)$$

Now, solving for R_4C_2 in equation 47 gives

$$R_4 C_2 = d - b - \frac{c - a}{b} . \qquad (48)$$

Letting C_4 be some arbitrary chosen value

$$C_4 = C_4 \qquad (49)$$

and solving equation 46 for R_4 yields

$$R_4 = \frac{c - a}{C_4 b} \quad . \tag{50}$$

Solving equation 48 for C_2 results in

$$C_2 = \frac{d - b - \frac{c - a}{b}}{R_4}$$

$$= \frac{bd - b^2 - c + a}{bR_4}$$

$$= \frac{b^2 - bd + a - c}{-(bR_4)} \quad .$$

Substituting equation 50 into this equation gives

$$C_2 = \frac{b^2 - bd + a - c}{-b\left(\frac{c - a}{C_4 b}\right)}$$

$$C_2 = \frac{C_4(b^2 - bd + c - a)}{a - c} \quad . \tag{51}$$

Solving for $R_3 C_1$ from equation 40 gives

$$R_3 C_1 = \frac{a}{R_4 C_2} \quad . \tag{52}$$

Substituting this equation into equation 41 and solving

for R_3 yields

$$b = R_3C_1 + R_3C_2$$

$$= \frac{a}{R_4C_2} + R_3C_2 \quad .$$

Therefore,

$$R_3C_2 = b - \frac{a}{R_4C_2}$$

and

$$R_3 = \frac{1}{C_2}\left[b - \frac{a}{R_4C_2}\right] \quad . \qquad (53)$$

Finally, solving equation 52 for C_1 gives

$$C_1 = \frac{a}{C_2R_3R_4} \quad . \qquad (54)$$

Now all the component values can be found in a progressive manner from the known coefficients of the modified bridged-tee transfer function.

In order to apply these equations specifically to the CZCC technique, five additional equations are needed to solve for the "known" coefficients a, b, c, and d, based on the output filter characteristics (Q_f and w_{nf}) and the desired closed loop characteristics (Q_{CL}, w_{nCL}, and K_{DC}). These five equations are

$$a = \frac{1}{w_{nf}^2} = LC \, , \qquad (55)$$

$$b = \frac{1}{Q_f w_{nf}} = \frac{L}{R_L} , \qquad (56)$$

$$c = \frac{1 + K_{DC}}{w_{nCL}^2} , \qquad (57)$$

$$d = \frac{1 + K_{DC}}{Q_{CL} w_{nCL}} , \qquad (58)$$

$$K_{DC} = \frac{R_F V_S}{R_1 V_M} . \qquad (59)$$

Since the filter has already been designed by the time the compensation network is added, the values of a and b have already been determined. As for determining c and d, K_{DC} is also already known and w_{nCL} can be found by selecting the desired rise time (t_R) of the closed loop transient response and solving

$$w_{nCL} = \frac{2.2}{t_R} . \qquad (60)$$

All that is left is to specify Q_{CL}. This would probably be specified based on the desired input transient response overshoot (%OS). The equation used to solve for Q_{CL} based on %OS is given by

$$Q_{CL} = -\sqrt{\frac{\pi^2 + \left(\text{Ln}\,\frac{\%OS}{100}\right)^2}{2\left[\text{Ln}\,\frac{\%OS}{100}\right]}}$$

Now, c and d can be calculated.

To facilitate the design of a modified bridged-tee circuit to be used for CZCC, equations 49 through 51 and equations 53 through 60 were used to generate an HP-41C calculator program. This program, called TEE, is reproduced at the end of this appendix. The input parameters for the program are:

L	-	output filter inductor value
C	-	output filter capacitor value
R_L	-	load resistor value
R_{ESR}	-	capacitor ESR value (if used)
R_S	-	inductor winding resistance (if used)
$\frac{V_S}{V_M}$	-	PWM gain
R_F	-	error amplifier feedback resistor value
R_1	-	error amplifier input resistor value
t_R	-	closed loop transient response rise time
Q_{CL}	-	closed loop transfer function Q

The program will then calculate and display the "known" coefficients a, b, c and d. The program will then request a value to use for C_4. Using this value and the "known" coefficients, the component values R_4, C_2, R_3, and C_1 are then solved for and displayed. If the values are not

reasonable for the value of C_4 chosen, pressing the R/S key will allow another value of C_4 to be selected.

Program TEE Listing

```
01  LBL 'TEE'
02  ENG 6
03  'CALC. COMP.'
04  'L?'
05  PROMPT
06  STO 00
07  'C?'
08  PROMPT
09  STO 01
10  'RL?'
11  PROMPT
12  STP 02
13  'RESR?'
14  PROMPT
15  STO 03
16  'RS?'
17  PROMPT
18  STO 04
19  'VS/VM?'
20  PROMPT
21  STO 05
22  'RF?'
23  PROMPT
24  STO 06
25  'R1?'
26  PROMPT
27  STO 07
28  LBL b
29  'TR?'
30  PROMPT
31  STO 08
32  'Q?'
33  PROMPT
34  STO 15
35  'CALC. a'
36  PROMPT
37  RCL 02
38  RCL 03
39  +
40  RCL 01
41  *
42  RCL 00
43  *
44  RCL 04
45  ENTER
46  RCL 02
47  +
48  /
49  STO 10
50  'a='
51  ARCL 10
52  PROMPT
53  'CALC b'
54  PROMPT
55  RCL 02
56  RCL 04
57  *
58  RCL 03
59  RCL 04
60  *
61  +
62  RCL 02
63  RCL 03
64  *
65  +
66  RCL 01
67  *
68  RCL 00
69  +
70  RCL 02
71  RCL 04
72  +
73  /
74  STO 11
75  'b='
76  ARCL 11
77  PROMPT
78  'CALC. ALPHA'
79  PROMPT
80  2.2
81  RCL 08
82  /
83  STO 09
84  RCL 02
85  RCL 04
86  +
87  RCL 07
88  *
89  1/X
90  RCL 02
91  *
92  RCL 06
93  *
94  RCL 05
95  *
96  1
```

```
97  +
98  STO 14
99  RCL 09
100 X**2
101 /
102 STO 12
102 "ALPHA="
103 ARCL 12
105 PROMPT
106 "CALC. BETA"
107 PROMPT
108 RCL 14
109 RCL 15
110 /
111 RCL 09
112 /
113 STO 13
114 "BETA="
115 ARCL 13
116 PROMPT
117 LBL a
118 "C4?"
119 PROMPT
120 STO 16
121 "CALC. R4"
122 PROMPT
123 RCL 12
124 RCL 10
125 -
126 RCL 11
127 /
128 RCL 16
129 /
130 STO 17
131 "R4="
132 ARCL 17
133 PROMPT
134 "CALC. C2"
135 PROMPT
136 RCL 13
137 RCL 11
138 *
139 CHS
140 RCL 11
141 X**2
142 +
143 RCL 12
144 +
145 RCL 10
146 -
147 RCL 16
148 *
149 RCL 10
150 RCL 12
151 -
152 /
153 STO 18
154 "C2="
155 ARCL 18
156 PROMPT
157 "CALC. R3"
158 PROMPT
159 RCL 10
160 RCL 17
161 /
162 RCL 18
163 /
164 CHS
165 RCL 11
166 +
167 RCL 18
168 /
169 STO 19
170 "R3="
171 ARCL 19
172 PROMPT
173 "CALC. C1"
174 PROMPT
175 RCL 10
176 RCL 18
177 /
178 RCL 19
179 /
180 RCL 17
181 /
182 STO 20
183 "C1="
184 ARCL 20
185 PROMPT
186 GTO a
187 END
```

REFERENCES

DeMaw, Doug, ed. Radio Amateur's Handbook. Newington, CN.: American Radio League, 1977.

Dixon, Lloyd H., Jr. "Closing the Feedback Loop", in Unitrode Power Supply Design Seminar. Lexington, MA: Unitrode Corporation, 1985, n. pag.

Huelsman, Lawrence P. Basic Circuit Theory with Digital Computations. Englewood Cliffs, NJ: Prentice-Hall, 1972.

Middlebrook, R. D. "Design Techniques for Preventing Input-Filter Oscillations in Switched-Mode Power Regulators." Proceedings of Powercon 5, the 5th National Solid-State Power Conversion Conference. 4-6 May 1978. San Francisco, CA, 1978.

Middlebrook, R.D. and Slobodan Cuk. "Modelling and Analysis Methods for DC-to-DC Switching Converters". Proceedings of the IEEE International Semiconductor Power Converter Conference, 1977 Record, pp. 90-111. 28-31 March 1977. Lake Buena Vista, FL, 1977.

Nagel, Laurence W. SPICE2: A Computer Program to Simulate Semiconductor Circuits. Memorandum No. ERL-M 520 Electronics Research Laboratory, University of California, Berkeley, 1975.

Pressman, Abraham I. Switching and Linear Power Supply, Power Converter Design. Rochelle Park, NJ: Hayden Book Co., 1977.

WADC-TR-53-66. Wright Air Development Center, OH: WADC, 1953.

Wait, John V., Lawrence P. Huelsman and Granino A. Korn. Introduction to Operational Amplifier Theory and Applications. New York: Mcgraw-Hill, 1975.