DESIGN AND ANALYSIS OF INTEGRATED ELECTROTHERMAL FILTERS

by

Manoon Aramrattana

A Dissertation Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL ENGINEERING

In Partial Fulfillment of the Requirements
For the Degree of

DOCTOR OF PHILOSOPHY

In the Graduate College

THE UNIVERSITY OF ARIZONA

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THE UNIVERSITY OF ARIZONA
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I hereby recommend that this dissertation prepared under my direction

by Manoon Aramrattana

entitled Design and Analysis of Integrated Electrothermal Filters

be accepted as fulfilling the dissertation requirement for the Degree

of Doctor of Philosophy.

Douglas J. Hamilton — 18 Dec 1978
Dissertation Director — Date

As members of the Final Examination Committee, we certify that we have read this dissertation and agree that it may be presented for final defense.

William J. Kerwin — 19 Dec 1978
Date

2 Jan 1979
Date

David L. Hetrick — 2 Jan 1979
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SIGNED: Manoon Aramrattana

DEDICATED TO

My mother, Mrs. Suihiang Aramrattana,

and my father, the late Mr. Pairote Aramrattana.

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ABSTRACT

Electrothermal circuits (ETC) are integrated circuits which use to advantage the interaction between electrical and thermal properties of silicon. The electrothermal filter is a unique low frequency filter system in which no electrical energy storage elements are employed. A state-variable synthesis technique is used in the electrothermal filter designs where ETC's are employed as active integrator elements.

The main objective of this dissertation is to achieve two independent ETC integrators on one chip, from which a second-order state-variable ETC filter can be obtained. Two ETC configurations are analyzed and designed: namely, a chip with two geometrically orthogonal channels each with a single-heater and differential-sensor, and a chip with two thermally isolated channels each comprising differential heaters and sensors. A band-pass filter is used to verify the feasibility of the designs.

The single-heater differential-sensor configuration was designed based on the analogy to the RC uniformly-distributed structure and fabricated on a 60x60x10 mil silicon chip. The measured isolation between the two geometrically orthogonal channels was approximately 20 dB; this is insufficient for designs requiring two ETC integrators on one chip. Two ETC chips are thus used to implement second-order ETC band-pass filters at center frequencies of 10, 50, and 100 Hz

with Q of 10. The measured values of the center frequencies and the Q are within 1% and 2%, respectively, of the calculated values.

Finally, the chip with two thermally-isolated ETC channels is fully analyzed, and the design criteria are given for band-pass filter designs. The heater and sensor locations are so arranged that an approximately single-pole ETC system is obtained in each channel. The ETC chip was fabricated with each channel being 20x60x2 mils, and with 10 mils separation between the channels. The measured isolation is approximately 55 dB. Using this chip, second-order ETC band-pass filters are designed at the center frequency of 60 Hz with Q's of 5 and 10. The experimental results agree within 3% of theoretical predictions.

CHAPTER 1

INTRODUCTION

In modern technology, integrated circuits (IC) have been a very important part of research and development of electronic systems. Many electronic subsystems are available in integrated circuit form for both digital and linear applications; for example, analog-to-digital and digital-to-analog converters, microprocessors, and various kinds of operational amplifiers. Operational amplifiers have been widely used in active Resistance Capacitance (RC) filter applications [Huelsman, 1968]. Active RC filter design is a first step toward filter system integration where both R and C can be fabricated along with transistors. Only small values of R and C can be fabricated in order to minimize the physical size of the IC chip. Consequently, only high frequency (1 kilohertz and up) applications are possible [Allstot, Broderson, and Gray, 1978]. This fabrication limit of R and C is a major obstacle to active filter integration for low frequency applications (below 1 kilohertz).

To alleviate this problem, several approaches have been suggested. The simplest way is to use integrated operational amplifiers as gain blocks and add discrete R's and C's externally. Unfortunately, this approach is costly. Resistance and capacitance multiplication techniques were suggested by Lin, Davis, and Sun [1966], but these are rather complex and impractical.

Another approach is to use electrical-thermal interactions in semiconductor material; these interactions produce attractive low frequency characteristics. Such an approach is the main subject of this dissertation.

Integrated circuits which take advantage of interaction between electrical and thermal properties of devices are called electrothermal circuits (ETC). Historically, ETC's were first reported in 1964 [Matzen and Meadows, 1964; Matzen, Meadows, Merryman and Emmons, 1964] where the low frequency characteristic of an ETC was demonstrated experimentally. Later, in 1969, two-dimensional analysis of ETC was done by Paul R. Gray using both lumped and distributed models. Thermal transfer functions were also calculated. Furthermore, it was shown that various ETC transfer functions can be obtained by placing heaters and sensors at different locations [Gray and Hamilton, 1971]; and Temperature-Stabilized Substrate (TSS) can be conveniently designed [Gray, Hamilton, and Lieux, 1974]. By using state-variable synthesis techniques, or KHN techniques, for active RC filters [Kerwin, Huelsman, and Newcomb, 1967], ETC filters were designed to have 100 Hz low pass and high pass characteristics; a 90 Hz band pass filter and 60 Hz notch filter were also fabricated [Louw, Hamilton and Kerwin, 1977]. In this particular technique, ETC integrators were obtained by pole-zero cancellations of higher pole locations while preserving the lowest frequency pole. The pole-zero cancellations are possible by selectively arranging heater and sensor locations [Louw, 1975]. Use of the ETC long time constant property was also made in designing ETC pulse generators [McCormick, 1975]. Pulse durations of one second to ninety seconds have been obtained. Other applications of ETC include a high-Q band-pass filter with center frequency of 20 kHz [Friedman, 1969]; TSS design using two-port ETC parameters [Fletcher, 1970]; RMS measurement techniques [Ott, 1974]; and a four-quadrant multiplier [Szekely, 1976]. Furthermore, a general three-dimensional analysis of ETC systems was performed by Mir T. Ali [1975], and the results were compared to those of Gray [1969]. From the comparison, it was concluded that the two-dimensional analysis gives satisfactory results in most ETC filter designs.

Use of the state-variable synthesis techniques [Louw, Hamilton, and Kerwin, 1977] is probably the most attractive approach leading to the integration of active ETC filters for low frequency applications. The main active element of this technique is the active integrator. Only second-order ETC filters were considered; these require two ETC integrators. Unfortunately, the second-order ETC filters obtained by Louw et al. [1977] used four ETC chips. The next step toward integration is to use two ETC chips and, ultimately, one ETC chip to obtain the same results.

In order to fabricate a second-order ETC filter on one chip, two ETC integrators on the chip must be implemented. This is the broad objective of this dissertation. The specific objectives are as follows:

1. Design and fabricate an ETC analog to uniformly RC distributed structures.

2. Design an active ETC integrator by means of positive electrical feedback.
3. Design a band-pass filter with the active ETC integrators using state-variable synthesis techniques.
4. Design and fabricate two independent ETC integrators on one chip.
5. Design a band-pass ETC filter with two independent ETC integrators on one chip.

All of these objectives were achieved. In general, the results were obtained from two principal ETC designs, the first using two-chip ETC filter systems, and the second using one-chip systems.

Band-pass filters at center frequencies of 10, 50, and 100 Hz with Q of 10 were obtained from the two-chip ETC filter system. A one-heater differential-sensor ETC configuration was used to implement each integrator.

In the one-chip ETC filter system, a differential heater and sensor ETC configuration was used for the integrator. Two independent ETC integrators were obtained by etching grooves through the silicon chip to thermally isolate the two integrator channels. For 20x60x2 mil channels with 10 mils separation, the measured isolation was about 55 dB. For the purpose of feasibility demonstration of the ETC chip, band-pass filters at a center frequency of 60 Hz with Q's of 5 and 10 were achieved. Furthermore, the filters can operate in the frequency range of 10 Hz to about 500 Hz depending on design sensitivity requirements. Substantial discussion of designs and analyses as well as results for ETC filters and their electronic circuits are given in later chapters.

A brief outline of this dissertation proceeds as follows. In Chapter 2, the general ETC thermal system is discussed and the two-dimensional analysis model and its transfer function, presented by Gray [1969], are introduced. ETC filter system analysis is also introduced in general form for later use in Chapter 4 and 5.

Various heater and sensor circuits are discussed and illustrated in Chapter 3. These circuits are those incorporated into ETC filter systems presented in this dissertation. New heater and sensor circuits are also introduced and analyzed.

Chapter 4 is concerned with ETC active integrator designs based on a uniformly distributed RC structure analogy. Band-pass filters are designed using those integrators. Experimental results are discussed and illustrated.

The design of two ETC integrators on one chip is fully investigated in Chapter 5. It is shown that with appropriately chosen heater and sensor locations, a rectangular chip can be made to have effectively one-dimensional heat flow. Parallel channel ETC configurations are described and implementation of the ETC configurations by using chemical etching is introduced. Then, an ETC filter design using this chip is discussed and experimental results are given.

Finally, ETC filter designs and experimental results are summarized in Chapter 6, and recommendations for further work are given.

CHAPTER 2

GENERAL ETC SYSTEM AND ACTIVE ETC FILTER SYNTHESIS

Introduction

In this chapter, the ETC thermal system is discussed briefly and a two-dimensional thermal transfer function is given. Relevant approximations are also discussed. Second-order state-variable synthesis is considered next. Then, two kinds of ETC active integrators are introduced, those with distributed poles and those with only a single pole. Finally, complete ETC filter systems are analyzed and discussed.

General ETC Thermal System

An ETC system consists of heat sources and temperature sensor devices arbitrarily located on a semiconductor chip which is mounted on an insulator. For all the work presented here, transistors are used as heater and sensor devices, silicon is used as the semiconductor chip, and DuPont Kapton [Bulleton H-2, n.d.] H-film is used for the insulator.

In the two-dimensional analysis presented by Gray [1969], the general thermal system consisted of an ETC chip mounted on an insulator which was attached to an isothermal surface, as shown in Fig. 2.1. The analysis imposed the following boundary conditions:

1. There is no temperature gradient at the perimeter of the chip.
2. There is no temperature gradient along the silicon-insulator interface.

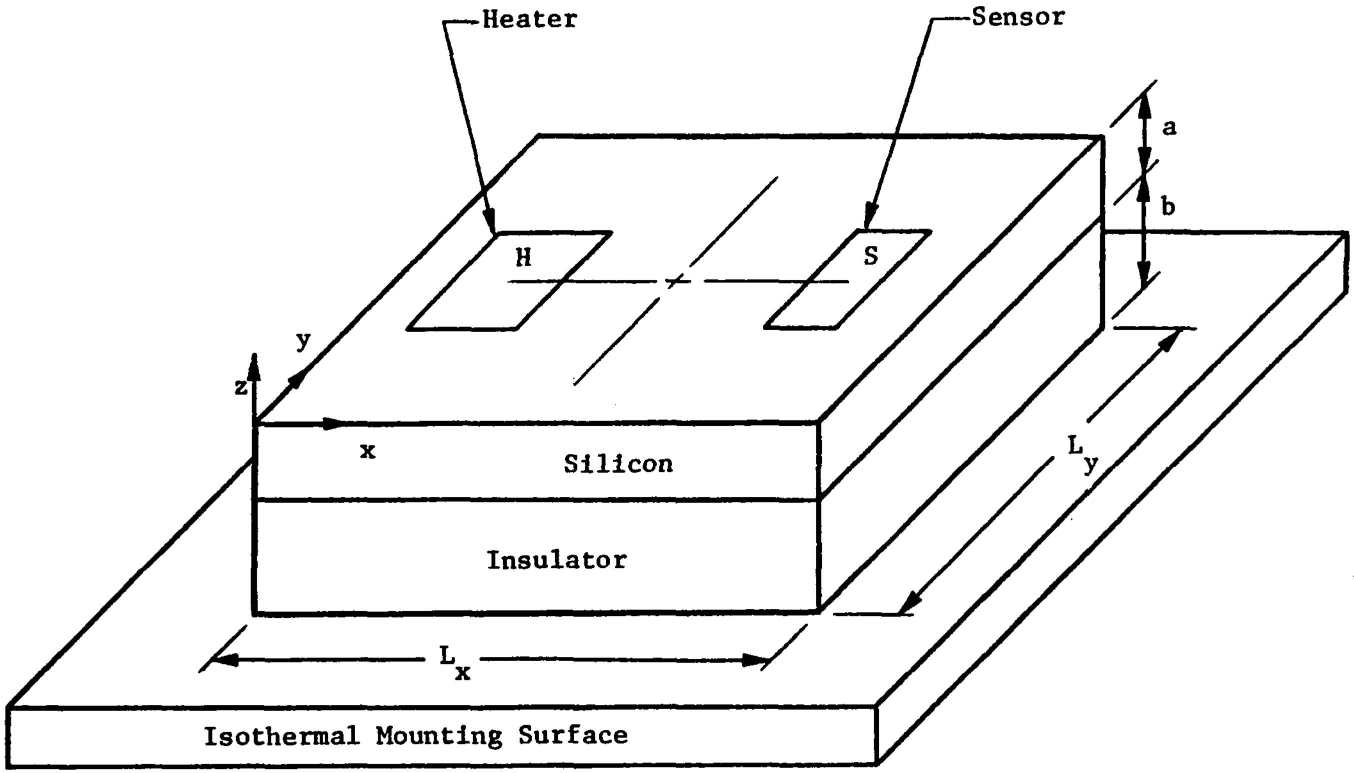


Fig. 2.1 Thermal System

3. Heat flows only in x- and y-directions in the silicon chip.
4. Heat flows only in z-direction in the insulator.

The thermal transfer function can be generally defined as:

$$T(p) = \frac{\text{Average temperature over the sensor area}}{\text{Average input power over the heater area}} \tag{2.1}$$

where p is the complex frequency parameter, i.e., $p = j\omega$.

By using finite cosine series expansions and the above boundary conditions, a steady state thermal transfer function was obtained as defined by Eq. (2.1). The thermal transfer function is [Gray, 1969]:

$$F(p) = \frac{4\sqrt{\omega_x \omega_y}}{ak_s A_S A_H} \sum_{n=o} \sum_{m=o} \frac{H_{nm} S_{nm}}{[\delta(n) + 1][\delta(m) + 1][p + A\,\omega_x]} \tag{2.2}$$

where

$$A = (n\pi)^2 + (m\pi)^2 \frac{\omega_y}{\omega_x} + \frac{\omega_i}{\omega_x}\sqrt{\frac{p}{\omega_z}} \coth\sqrt{\frac{p}{\omega_z}}$$

H_{nm} and S_{nm} are the finite Fourier cosine transforms of heater and sensor areas, respectively. They are defined as:

$$H_{nm} = \iint_{\text{Chip Area}} W_H(x,y) \cos\frac{n\pi x}{L_x} \cos\frac{m\pi y}{L_y}\, dxdy \tag{2.3}$$

and

$$S_{nm} = \iint_{\text{Chip Area}} W_S(x,y) \cos\frac{n\pi x}{L_x} \cos\frac{m\pi y}{L_y}\, dxdy \tag{2.4}$$

$W_H(x,y)$ and $W_S(x,y)$ are dimensionless weighting functions of heater and sensor areas, respectively. Their values are unity in their respective areas and zero elsewhere. $\delta(n)$ and $\delta(m)$ are defined as:

$$\delta(n),\ \delta(m) = \begin{cases} 1 & n = m = o \\ 0 & n \neq o,\ m \neq o \end{cases} \tag{2.5}$$

Other parameters are defined as follows:

$$\omega_x = \frac{k_s}{\rho_s c_s L_x^2} \tag{2.6}$$

$$\omega_y = \frac{k_s}{\rho_s c_s L_y^2} \tag{2.7}$$

$$\omega_i = \frac{k_s}{\rho_i c_i ab} \tag{2.8}$$

$$\omega_z = \frac{k_i}{\rho_i c_i b^2} \tag{2.9}$$

The thermal parameters of silicon and H-film are given in Table 2.1 [Louw, 1975].

Table 2.1 Thermal Parameters of Silicon and H-Film

Parameters	Values
k_s	2.23 mW/°C mil
$\rho_s c_s$	27.7×10^{-6} mW-sec/°C mil^3
k_i	0.004 mW/°C mil
$\rho_i c_i$	25.4×10^{-6} mW-sec/°C mil^3

The transfer function given in Eq. (2.2) is not very convenient to use because the term $\sqrt{p/\omega_z}$ coth $\sqrt{p/\omega_z}$ is a complex function. Certain approximations must be made for Eq. (2.2) to be more practical. In most cases of practical importance,

$$\sqrt{p/\omega_z} \coth \sqrt{p/\omega_z} \approx 1 \tag{2.10}$$

is a good approximation. It has been shown that with this approximation the maximum relative error in the transfer function of a 10-mil thick silicon chip mounted on H-film 5 mils thick is 16% [Louw, 1975]. By using the approximations in Eq. (2.6) through Eq. (2.10), Eq. (2.2) becomes

$$F(p) = \frac{4\omega_x}{ak_s A_S A_H}\left(\frac{L_x}{L_y}\right) \sum_{n=o} \sum_{m=o} \frac{H_{nm}\, S_{nm}}{[\delta(n) + 1][\delta(m) + 1][p + A\,\omega_x]}$$

where

$$A = n\pi^2 + m\pi^2 \left(\frac{L_x}{L_y}\right)^2 + \frac{k_i}{k_s} \cdot \frac{L_x^2}{ab} \tag{2.11}$$

Equation (2.11) is the thermal transfer function having multiple poles distributed along the real axis in the complex plane. This property of Eq. (2.11) will be used in Chapter 4. Further, it will also be used in Chapter 5 for designing an approximately single-pole ETC using pole-zero cancellation techniques.

In addition, a computer program, in FORTRAN IV, has been developed to make frequency response calculations of Eq. (2.2) [Gray, 1969]. The program computes the first 30x30 terms of Equations (2.2), (2.3), and (2.4); it is used in designing ETC systems in both Chapters 4 and 5.

Active Filters

In general, resistors, capacitors, and operational amplifiers are used in synthesizing active filters. Resistors and capacitors can be either discrete [Huelsman, 1968] or distributed [Burns and Kerwin, 1975; Ghausi and Kelly, 1968], and operational amplifiers are in integrated form. Attempts have been made to avoid using any external capacitors by taking advantage of the built-in capacitor in operational amplifiers [Acar and Ghausi, 1978].

There are several approaches for designing active filters. Among them, a few well-known active filter structures are the Sallen and Key structures [Sallen and Key, 1955], Twin-T structures [Bachmann, 1959], distributed structures [Ghausi and Kelly, 1968; Kerwin, 1967], and state-variable techniques [Kerwin, Huelsman, and Newcomb, 1967]. However, state-variable synthesis will receive more attention here because it is the main synthesis technique used for active ETC filter designs in later chapters.

The basic idea of state-variable synthesis is the use of analog computer integrator active elements to implement any order of active filter by means of positive and negative electrical feedback and feedforward. The features of this technique are low sensitivity to component changes and relatively straightforward implementation. For example, second-order filters using this technique with transfer functions at various outputs are shown in Fig. 2.2; 1/p is the positive gain integrator element in frequency domain.

As one can see, integrators are the important part of the design. Therefore, the implementation of active ETC integrators is a salient objective of this dissertation.

Active ETC Filter Implementations

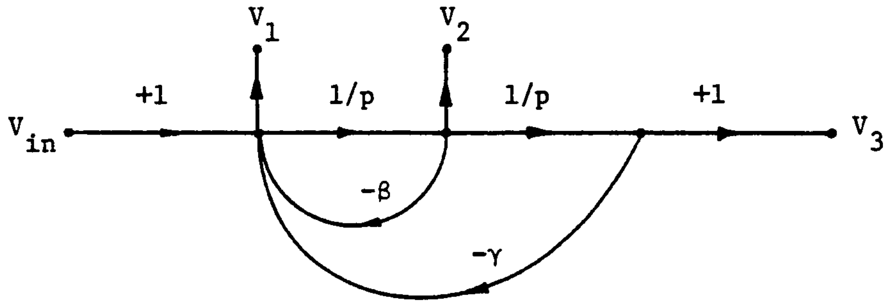
To obtain active ETC filters, active ETC integrators must be incorporated in the flow graph in Fig. 2.2. Active ETC integrators are implemented by using two types of ETC's. One has multiple poles distributed along the negative real axis in the complex plane, and the other has approximately a single negative real pole. RC analogs of both ETC's are first discussed; then active ETC integrators are analyzed.

A multiple-pole system is obtained by using a uniform RC distributed structure analog (URC) as shown in Fig. 2.3(a). The voltage transfer function of terminals 1 and 2 is given by [Ghausi and Kelly, 1968]

$$T_{12}(p) = \frac{1}{\cosh\sqrt{RCp}} \tag{2.12}$$

By using an infinite power series expansion, $\cosh\sqrt{RCp}$ can be expanded to be

$$\cosh\sqrt{RCp} = 1 + \frac{RCp}{2!} + \frac{(RCp)^2}{4!} + \frac{(RCp)^3}{6!} + \ldots. \tag{2.13}$$

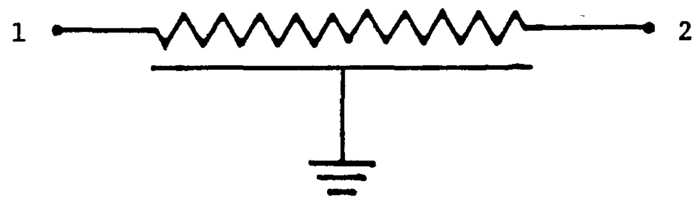


$$T_1(p) = \frac{V_1}{V_{in}} = \frac{p^2}{p^2 + \beta p + \gamma}$$

$$T_2(p) = \frac{V_2}{V_{in}} = \frac{p}{p^2 + \beta p + \gamma}$$

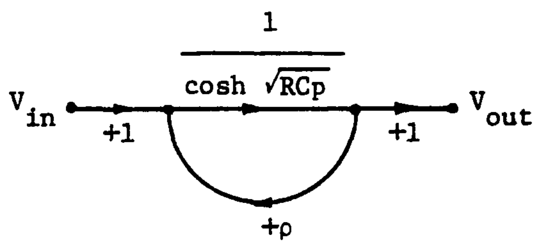
$$T_3(p) = \frac{V_3}{V_{in}} = \frac{1}{p^2 + \beta p + \gamma}$$

Fig. 2.2 Signal Flow Graph of Second-Order Filter Systems



$$T_{12}(p) = \frac{V_2}{V_1} = \frac{1}{\cosh\sqrt{RCp}}$$

(a) Uniformly RC Distributed Structure



$$\frac{V_{out}}{V_{in}} \approx \frac{1}{RCp} \qquad \text{when} \quad \rho = 1.000$$

(b) Flow Graph of an Active URC Integrator System

Fig. 2.3 Distributed Poles System

When positive feedback is applied to the transfer function in Eq. (2.12) as shown in Fig. 2.3(b), the closed loop transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{1}{\cosh \sqrt{RCp} - \rho} \tag{2.14}$$

where ρ is the feedback coefficient. When ρ is unity and Eq. (2.13) is used, Eq. (2.14) can be approximated as

$$\frac{V_{out}}{V_{in}} \approx \frac{2}{RCp} \tag{2.15}$$

where $RCp << 1$.

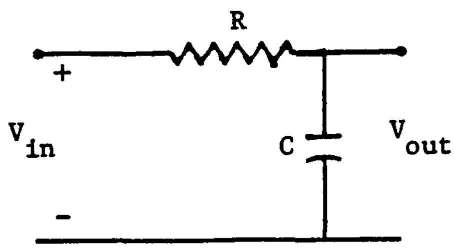
Similarly, Fig. 2.4(a) is the RC analog of approximately single-pole ETC's, and Fig. 2.4(b) is its feedback system. The transfer function of Fig. 2.4(b) is

$$\frac{V_{out}}{V_{in}} = \frac{1/RC}{p + 1/RC\ (1 - \rho)} \tag{2.16}$$

where ρ is the feedback coefficient, When ρ is unity, Eq. (2.16) becomes

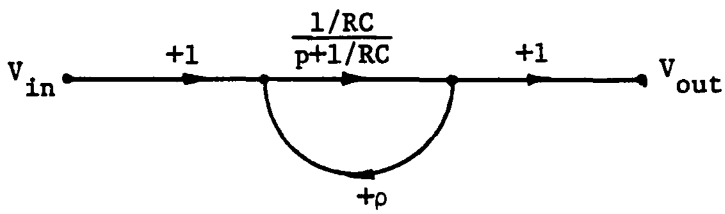
$$\frac{V_{out}}{V_{in}} = \frac{1}{RCp} \tag{2.17}$$

ETC integrators similar to those of Fig. 2.3(b) and Fig. 2.4(b) are presented in Fig. 2.5 where γ is a real pole. Subsequently, Equations (2.15) and (2.17) become



$$\frac{V_{out}}{V_{in}} = \frac{1/RC}{p + 1/RC}$$

(a) Simple RC Low Pass Network

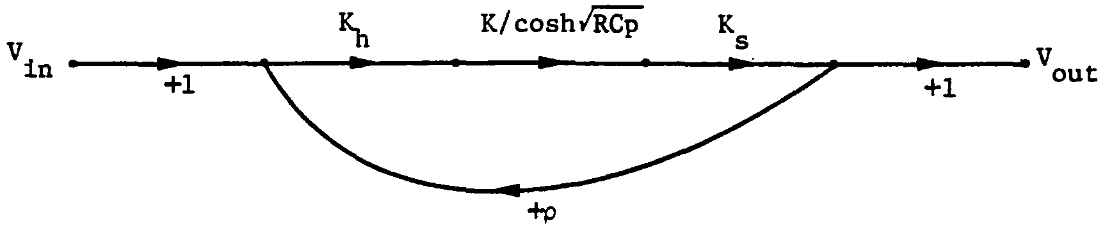


$$\frac{V_{out}}{V_{in}} = \frac{1/RC}{p + \frac{1}{RC}(1 - \rho)}$$

$$= \frac{1}{RCp} \qquad \text{when} \qquad \rho = 1$$

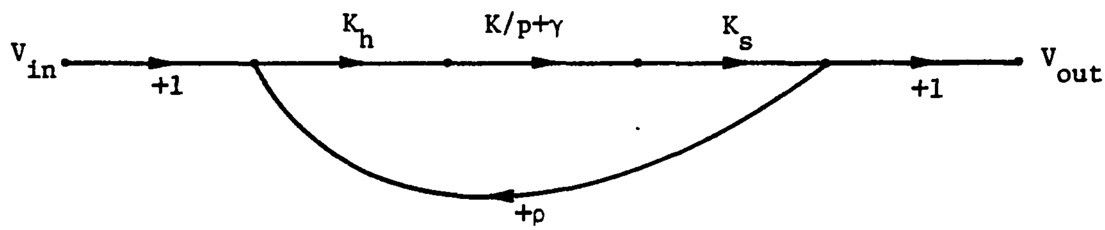
(b) Flow Graph of an Active RC Integrator

Fig. 2.4 Single-Pole System



$$\frac{V_{out}}{V_{in}} = \frac{K'}{RCp} \qquad \text{when} \quad \rho = 1/K'.$$

(a) An Active ETC Integrator Using a Distributed-Pole ETC



$$\frac{V_{out}}{V_{in}} = \frac{K'}{p} \qquad \text{when} \quad \rho = \gamma/K'.$$

(b) An Active ETC Integrator Using Approximately Single Pole ETC

Fig. 2.5 Signal Flow Graph of Active ETC Integrators

$$\frac{V_{out}}{V_{in}} \approx \frac{K'}{RCp} \quad , \tag{2.18}$$

and

$$\frac{V_{out}}{V_{in}} = \frac{K'}{p} \quad , \tag{2.19}$$

respectively; where $K' = K_h \cdot K \cdot K_s$, and K_h and K_s are heater and sensor conversion constants.

The ETC integrators of Fig. 2.5 can be used in the second-order filter of Fig. 2.2; the result is shown in Fig. 2.6, where T(p) is either a multiple-pole ETC or an approximately single-pole ETC. Figure 2.6 can be reduced to a simpler flow graph as shown in Fig. 2.7. The functions $F_1(p)$ and $F_2(p)$ are summarized in Table 2.2. The filter transfer functions are summarized in Table 2.3.

The filter transfer functions derived above are generalized so that one can have a better understanding of which parameters are in what part of the transfer functions. More detailed discussions and implementations of the system in Fig. 2.7 are presented in Chapters 4 and 5.

One more important element of active ETC filter systems is the electronic circuitry implementing heaters and sensors to provide appropriate gains, K_h and K_s, respectively, as well as output voltage and current levels. Before the complete design of ETC filters is presented, heater and sensor circuits are discussed.

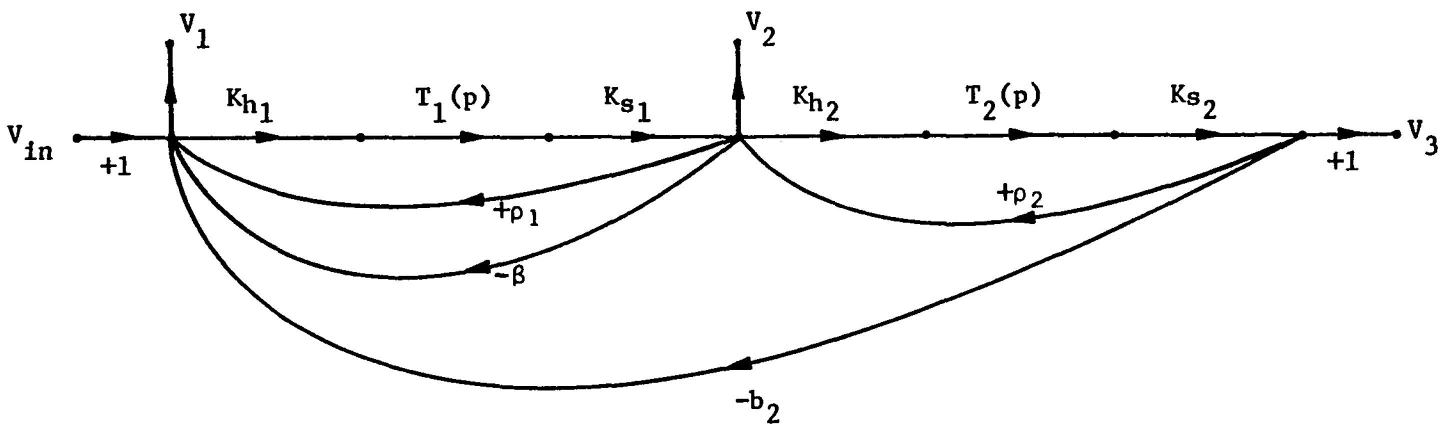


Fig. 2.6 Signal Flow Graph of a Second Order Active ETC Filter

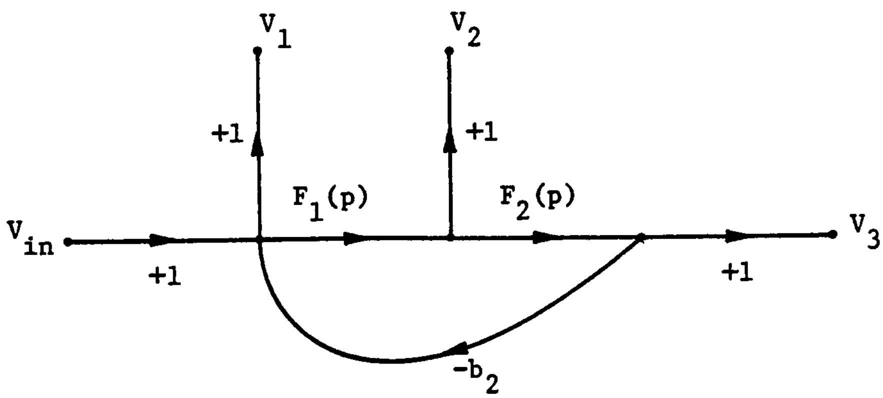


Fig. 2.7 Simplified Flow Graph of Fig. 2.6

Table 2.2 Transfer Functions of $F_1(p)$ and $F_2(p)$ Shown in Figure 2.7

$T(p)^*$	$F_1(p)$	$F_2(p)$
$\dfrac{K}{\cosh \sqrt{RCp}}$	$\dfrac{K_1'}{\cosh \sqrt{RCp} - b_1 K_1'}$	$\dfrac{K_2'}{\cosh \sqrt{RCp} - \rho_2 K_2'}$
$\dfrac{K}{p + \gamma}$	$\dfrac{K_1'}{p + \alpha_1}$	$\dfrac{K_2'}{p + \alpha_2}$

where $b_1 = \rho_1 - \beta$

$\alpha_1 = \gamma - b_1 K_1'$

$\alpha_2 = \gamma - \rho_2 K_2'$

$K' = K_h \cdot K \cdot K_s$

*From Fig. 2.6

Table 2.3 Generalized Active ETC Filter Transfer Functions

(a) $T(p) = \dfrac{K'}{\cosh\sqrt{RCp}}$

Filters	Transfer Functions
Low Pass	$\dfrac{K_1'\ K_2'}{\cosh^2\sqrt{RCp} - (b_1K_1' + \rho_2K_2')\cosh\sqrt{RCp} + b_1K_1'\rho_2K_2' + b_2K_1'K_2'}$
Band Pass	$\dfrac{K_1'\ (\cosh\sqrt{RCp} - \rho_2K_2')}{\cosh^2\sqrt{RCp} - (b_1K_1' + \rho_2K_2')\cosh\sqrt{RCp} + b_1K_1'\rho_2K_2' + b_2K_1'K_2'}$
High Pass	$\dfrac{\cosh^2\sqrt{RCp} - (b_1K_1' + \rho_2K_2')\cosh\sqrt{RCp} + b_1K_1'\rho_2K_2'}{\cosh^2\sqrt{RCp} - (b_1K' + \rho_2K_2')\cosh\sqrt{RCp} + b_1K_1'\rho_2K_2' - b_2K_1'K_2'}$

(b) $T(p) = \dfrac{K'}{p + \gamma}$

Filters	Transfer Functions
Low Pass	$\dfrac{K_1'\ K_2'}{p^2 + (\alpha_1 + \alpha_2)\ p + (\alpha_1\alpha_2 + b_2K_1'K_2')}$
Band Pass	$\dfrac{K_1'\ (p + \alpha_2)}{p^2 + (\alpha_1 + \alpha_2)\ p + (\alpha_1\alpha_2 + b_2K_1'K_2')}$
High Pass	$\dfrac{p^2 + (\alpha_1 + \alpha_2)\ p + \alpha_1\alpha_2}{p^2 + (\alpha_1 + \alpha_2)\ p + (\alpha_1\alpha_2 + b_2K_1'K_2')}$

CHAPTER 3

ELECTRONIC CIRCUITS FOR ETC SYSTEMS

Introduction

One can see from the system analyses in Chapter 2 that several electronic circuits must be incorporated to implement the ETC filter systems. These electronic circuits can be categorized as heater circuits, sensor circuits, coefficient-setting circuits and current-summing circuits. Illustrations and brief descriptions of these circuits are given in this chapter. A single heater circuit is first discussed, followed by the discussion of differential heaters. Then the basic sensor circuit and modifications for low-noise performance are described. The description of a common-collector version of the basic sensor circuit is also given. Finally, the coefficient setting circuit is discussed, and its current-summing circuit is also described.

Heater Circuits

Single Heater Circuit

A heater circuit for an ETC system where only one heater is needed to implement a desired ETC transfer characteristic is shown in Fig. 3.1. In this circuit, the heater transistor Q_1 operates as in a class A amplifier. In order to have sufficient ETC power excursion, adequate variation of the collector current of Q_1 is required. The operational amplifier, R_1, R_2 and transistor Q_3 are connected as a voltage-to-current converter where the negative input of the operational

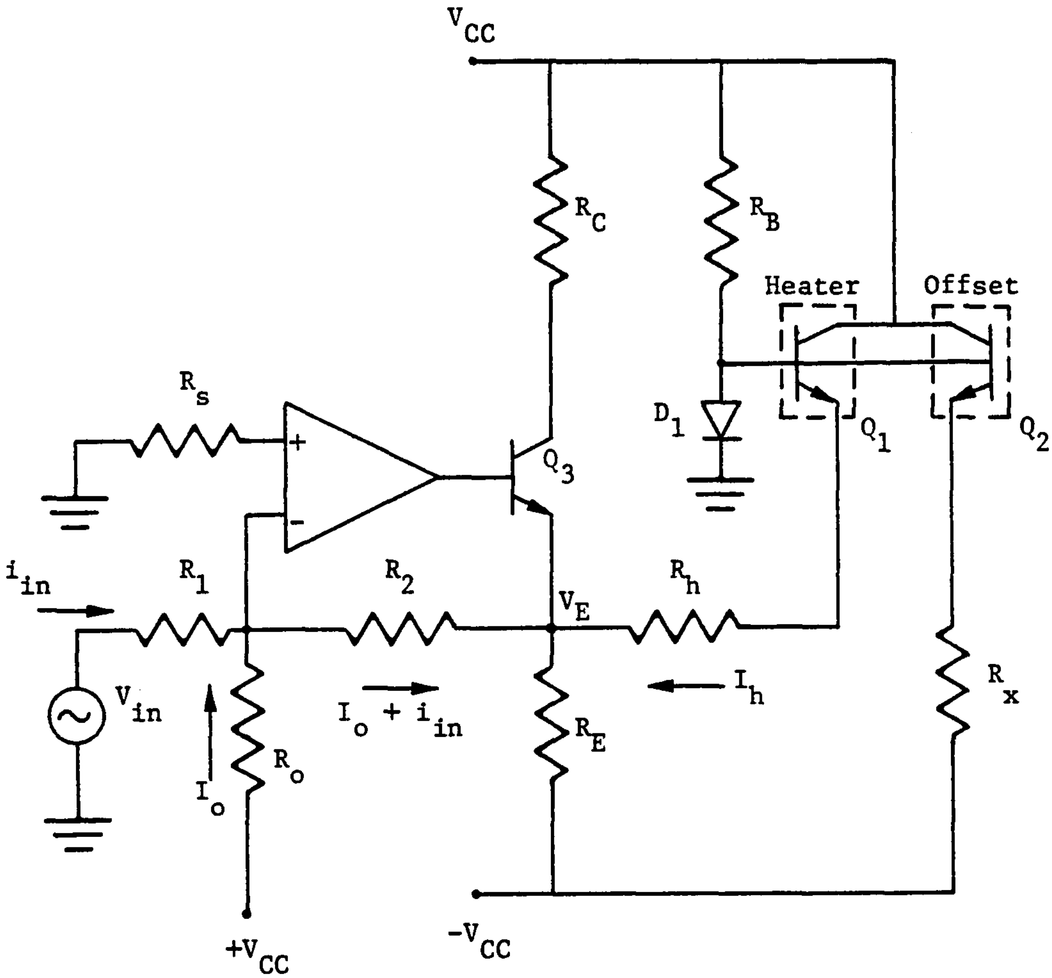


Fig. 3.1 New Heater Circuit

amplifier serves as the current-summing node. In addition, the transistor Q_3 is added to ensure that enough current is supplied to the heater Q_1.

Since the negative input of the operational amplifier and the emitter of Q_1 are at virtual ground voltage, the heater current, I_h, is given by

$$I_h = \frac{R_2}{R_h} (I_o \pm i_{in}) \tag{3.1}$$

where I_o is the operating current. To ensure maximum current swing, V_E must be chosen so that it also has the maximum swing. Unfortunately, V_E must always be negative, and $V_E = 0$ is the maximum voltage. This voltage is given by

$$V_E = - \frac{R_2}{R_0} V_{CC} \pm \frac{R_2}{R_1} i_{in} \tag{3.2}$$

From Eqns. (3.1) and (3.2), the small signal heater conversion factor (mW/mA) can be determined by

$$k_h = V_{CB} \frac{R_2}{R_h} \tag{3.3}$$

When a single heater transistor is used, it always causes an offset voltage at the output of the sensor circuit if the heater transistor is not at the center of the chip. This offset voltage, caused by the temperature gradient on the chip, can be nulled by applying a constant current source to a second heater transistor Q_2 that gives exactly the opposite effect on the sensor transistors. This adjustment technique will be pointed out in Chapter 4.

This kind of heater circuit will be utilized in Chapter 4 where the distributed-pole ETC requires the use of a single heater transistor and differential sensor transistors.

Differential Heater Circuit

Both voltage-driven and current-driven differential heater circuits have been designed by Louw [1975]. For integration purposes the current-driven circuit was chosen. A brief discussion of its performance is presented, and the circuit is shown in Fig. 3.2.

By taking the loop voltage around transistors Q_1, Q_2, Q_3 and Q_4 to be zero, one can find the total currents

$$I_1 = \frac{I_a}{2} + \frac{I_a}{I_b} i_s \tag{3.4}$$

and

$$I_2 = \frac{I_a}{2} - \frac{I_a}{I_b} i_s \tag{3.5}$$

where i_s is the small-signal input current. Subsequently, the small-signal input power can be determined by

$$P_i = \pm V_{CB} \cdot \frac{I_a}{I_b} \cdot i_s \tag{3.6}$$

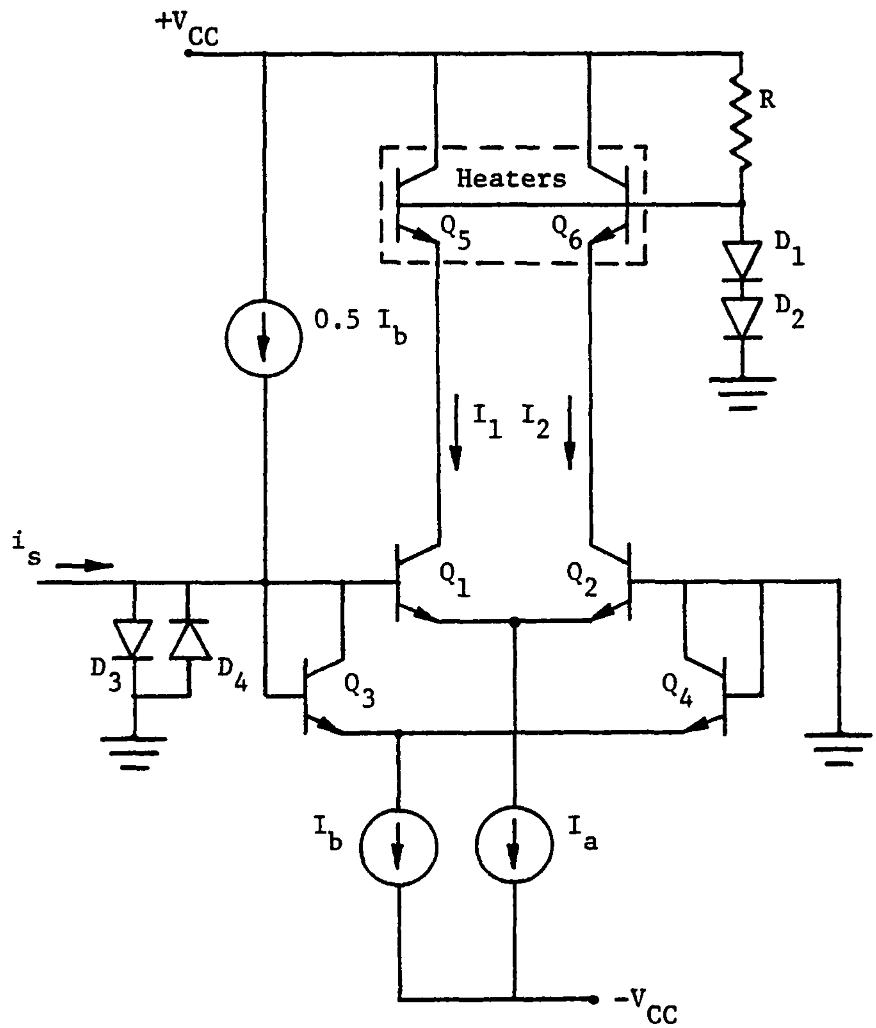


Fig. 3.2 Current-Driven Differential Heater Circuit

where V_{CB} is the constant collector-base voltage. Therefore, the heater conversion factor (mW/mA), from input current to heater output power, is

$$k_h = V_{CB} \frac{I_a}{I_b} \qquad (3.7)$$

The maximum power swing is limited by the bias currents I_a and I_b, and the maximum power dissipation of the heater transistors. Under ideal conditions where the transistor pairs Q_1-Q_2, Q_3-Q_4, and Q_5-Q_6 are matched pairs, the input current, i_s, is limited by either I_a or I_b, whichever is smaller. In practice, I_a is normally larger than I_b. However, the ratio I_a to I_b must be kept low enough that I_1, $I_2 \geq 0$. In addition, the current I_a must also be set such that

$$\left| V_{CB} \frac{I_a}{I_b} i_{s_{max}} \right| \leq P_{d(max)} \qquad (3.8)$$

where $P_{d(max)}$ is the maximum power dissipation of heater transistors Q_5 and Q_6.

However, in practice, these transistor pairs are likely to be mismatched. Therefore, the maximum power swing is reduced by the power difference at the bias condition. That is, the dynamic range of the heater transistors is reduced. The diodes D_3 and D_4 are added to the input node of the heater circuit for over-voltage protection. This heater circuit will be used in Chapter 5.

Sensor Circuits

Basic ETC Sensor Circuit

To interface the ETC systems to the rest of the electronic systems, the temperature difference of the sensor areas must be converted into either voltage or current. The conversion factor of a sensor circuit must also be linear with the temperature difference. Transistors are used as the sensing elements because of the temperature dependence of the emitter-base voltage. An ingenious way of implementing a sensor circuit, was reported by Louw [1975]. This sensor circuit is shown in Fig. 3.3. A brief discussion of the circuit follows.

When the transistors Q_1 and Q_2 are at different temperatures, the operational amplifier will force the V_{BE} difference V to appear at the base of the transistor Q_2; that is

$$V = V_{BE2} - V_{BE1} \tag{3.9}$$

Let η be the conversion constant (V/°C) of the sensor output voltage; then

$$V = \eta(T_2 - T_1) \tag{3.10}$$

where $(T_2 - T_1)$ is the temperature difference of the sensor areas. For negligible base current of the transistor Q_2,

$$V_{out} = \frac{(R_2 + R_1)}{R_2} \cdot \eta(T_2 - T_1) \quad . \tag{3.11}$$

Consequently, the sensor output voltage conversion factor (V/°C) is

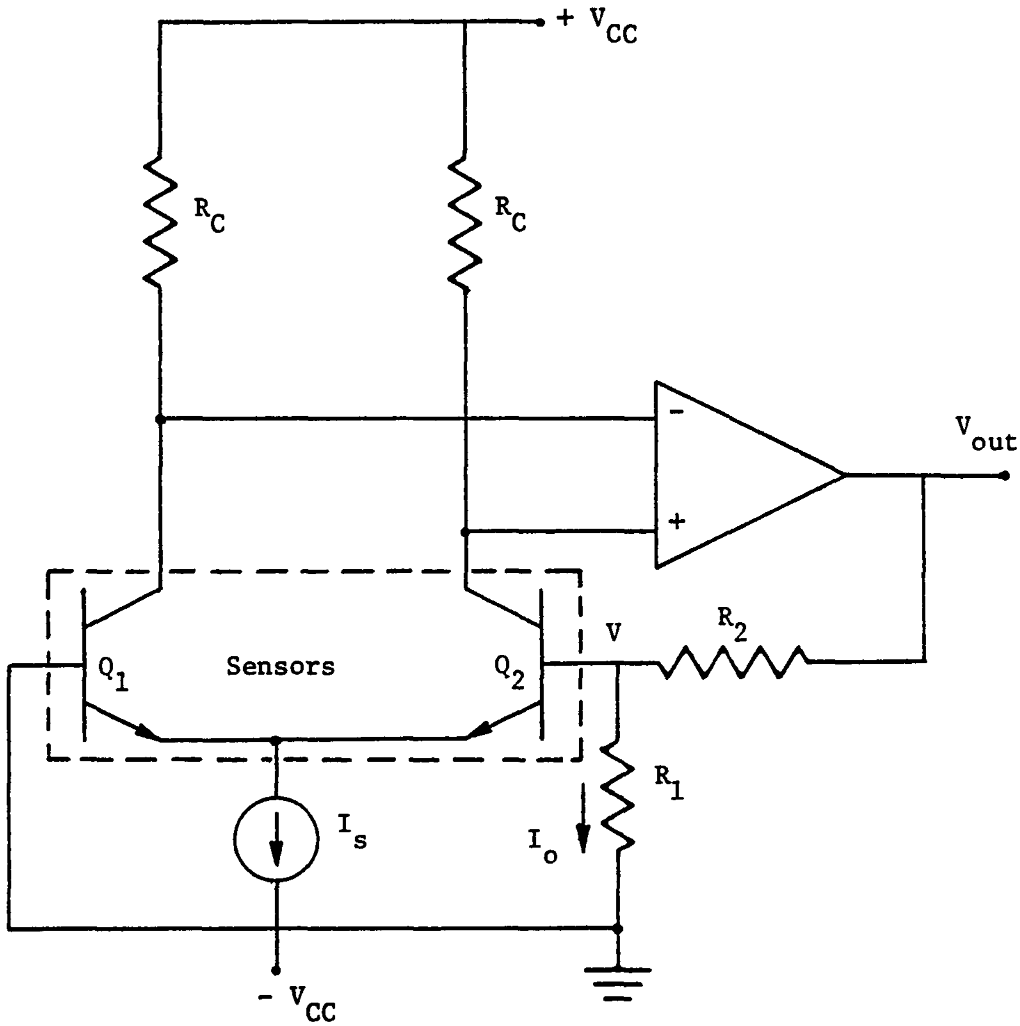


Fig. 3.3 Basic ETC Differential Sensor Circuit

$$k_{VS} = \frac{(R_2 + R_1)}{R_1} \cdot \eta \quad ; \tag{3.12}$$

and the output current conversion factor (A/°C) is

$$k_{is} = \frac{\eta}{R_1} \quad . \tag{3.13}$$

To find the conversion factor η, the emitter-base voltage and emitter current of the transistors must be considered. From the four-layer model equations, a transistor emitter current, I_E, at the forward-active region operation is given by [Hamilton and Howard, 1975]

$$I_E \approx I_{s2} \left[\frac{I_{s1}}{\alpha_I \, I_{s2}} \exp(V_{BE}/V_T) + 1 \right] \tag{3.14}$$

where I_s, α_I, and V_T are saturation currents, inverse current gain, and mKT/q, respectively. When one relates I_{s1}, I_{s2} and α_I to physical parameters, $I_{s1}/(\alpha_I I_{s2})$ is always greater than unity. Then, when $V_{BE} >> V_T$, Eq. (3.14) can be approximated to be

$$I_E \approx I_s \, e^{V_{BE}/V_T} \tag{3.15}$$

where I_s is a saturation current depending on the diffusion coefficient, impurity lifetime, impurity doping level, intrinsic property, base width and emitter area of a transistor. By taking the temperature dependence of all the physical parameters into account, the temperature dependence of I_s can be approximated as

$$I_s \approx A\ D\ T^{2.4}\ \exp[-E_g/kT] \quad ; \tag{3.16}$$

where A is the emitter area, D is a constant and E_g is the semiconductor band-gap in eV. Then Eq. (3.15) becomes

$$I_E = A\ D\ T^{2.4}\ \exp[(V_{BE} - E_g/q)/V_T] \tag{3.17}$$

By solving for V_{BE} in Eq. (3.17) and substituting in Eq. (3.9), one obtains

$$V = \frac{mk}{q} \left[(T_2 - T_1)\ \ell n \frac{I_E}{AD} - 2.4\ (T_2\ \ell n\ T_2 - T_1\ \ell n\ T_1) \right] \tag{3.18}$$

where T_1 and T_2 are the average temperatures of the sensor areas in °K. In a typical ETC, the sensor temperatures differ by less than 1°K; thus $T_1 \approx T_2 \approx T_o$ where T_o is the ambient temperature in °K. Consequently, Eq. (3.18) becomes

$$V = \frac{mk}{q} \left[\ell n \frac{I_E}{AD} - 2.4\ \ell n\ T_o \right] (T_2 - T_1) \tag{3.19}$$

By equating Eqns. (3.10) and (3.19)

$$\eta = \frac{mk}{q} \left[\ell n \frac{I_E}{AD} - 2.4\ \ell n\ T_o \right] \tag{3.20}$$

The term I_E/AD is a constant, but its actual value depends on the bias current, I_E, the emitter area, A, and the numerical values of physical parameters, D, of the sensor transistors. Hence, it can only be obtained accurately by experiment. Note that m = 1 and T_o = 300°K are normally used.

Low-Noise Sensor Circuit

From the system analysis in Chapter 2, positive feedback is employed to implement ETC filter systems. When positive feedback is applied to implement an integrator, the system becomes sensitive to any noise introduced in the feedback loop. Unfortunately, the sensor circuit in Fig. 3.3 has a signal-to-noise ratio of about 43 dB and is too noisy to be used for a positive feedback ETC system. Hence, modifications need to be made.

Sensor noise problems are caused principally by shot noise and 1/f noise. It has been reported that for the common-emitter transistor configuration, shot noise increases with increasing base current [Van Der Ziel, 1976]. The 1/f noise is also directly proportional to base current [Plumb and Chenette, 1963]. Furthermore, it has been reported that 1/f noise exhibits a strong dependence on collector voltage, and that the collector leakage mechanism is the cause of this noise [Plumb and Chenette, 1963].

The circuit of Fig. 3.3 was therefore modified accordingly. By reducing the emitter current to 60 μA and the collector-base voltage to less than 1 v, the signal-to-noise ratio was increased to 52 dB, an improvement of almost 10 dB. The modified sensor circuit is shown in Fig. 3.4.

This circuit is used in Chapter 4 to implement ETC band-pass filters.

Common-Collector Sensor Circuit

It will be noted that the geometrical locations of heater and sensor transistors are dictated by the requirements of the particular ETC transfer function being realized. In some cases the heaters and sensors must be so close together that there is insufficient space for an isolation diffusion. When this occurs, electrical isolation of heater and sensor transistors is not possible. This means that all transistor collectors are electrically connected, and heater and sensor circuit design must take this into account. For such a situation the sensor circuit in Fig. 3.4 is no longer applicable, and a common-collector sensor circuit must be developed. The modified version of the sensor circuit in Fig. 3.3 is shown in Fig. 3.5; here the sensor transistors are shown within the broken line. The analysis of the circuit remains the same as previously described. For this circuit the noise performance was improved by means of low emitter currents only. This sensor circuit is used in Chapter 5.

Coefficient-Setting Circuit

In ETC filter systems, both positive and negative feedback are employed to obtain the desired filter response. To have complete integration of the filter system, feedback-coefficient-setting procedures

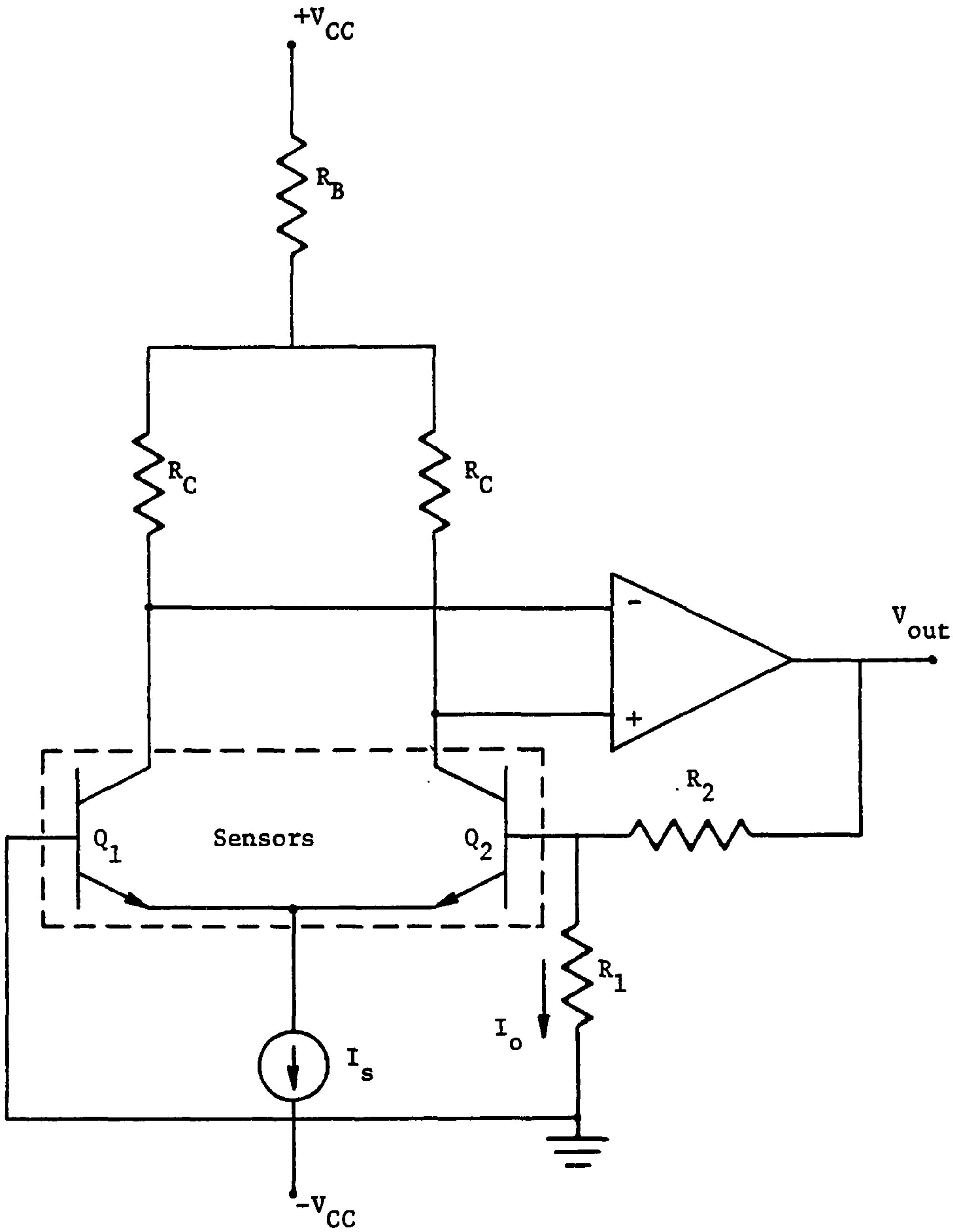


Fig. 3.4 Low Noise Sensor Circuit

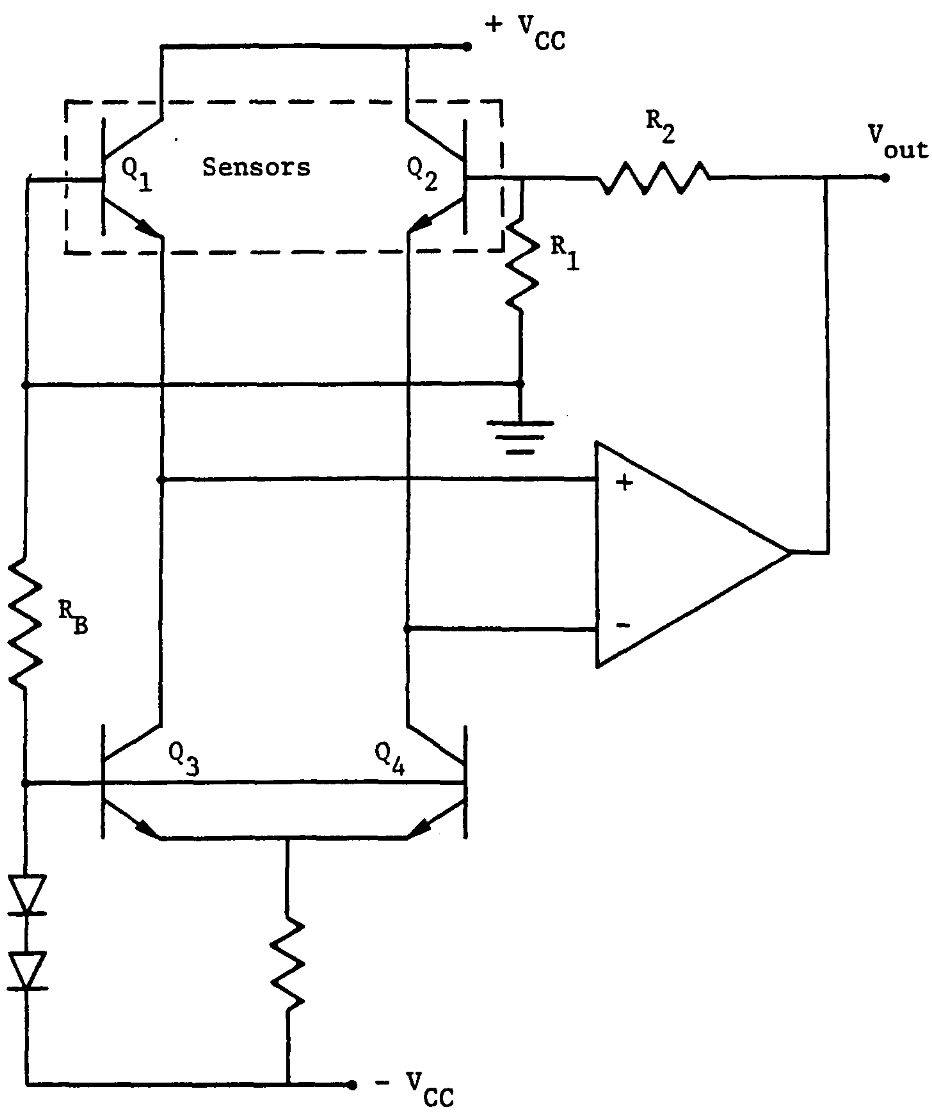


Fig. 3.5 Common-Collector ETC Differential Sensor Circuit

must be such that minimum area on the silicon chip is used. Rather than using resistor ratios where large resistor values are sometimes essential, current ratios are used so that circuits consisting mostly of transistors rather than resistors can be employed. Feedback coefficients which are determined by current ratios can be obtained by using the circuit of Fig. 3.6.

In Fig. 3.6, under ideal conditions where all the transistor pairs are matched, collector currents of transistors Q_1 and Q_2, and Q_3 and Q_4 are equal. The collector currents are then mirrored by the identical p-n-p Wilson current mirror circuits [Wilson, 1968]. Transistors Q_{13}-Q_{14}-Q_{15} and Q_{17}-Q_{16}-Q_{18} mirror the collector currents of Q_3 and Q_4, respectively. Consequently, the collector currents of Q_{15} and Q_{18} are the same as those of Q_3 and Q_4. Similarly, the collector currents of Q_9 and Q_{12} are the same as those of Q_1 and Q_2.

Let i_1 and i_2 be the signal currents of the transistor Q_1-Q_2 and Q_3-Q_4 pairs. When a signal input current, i_s, is applied, the magnitude of i_1 and i_2 can be calculated in the same way as was done for the differential heater in Fig. 3.2. That is

$$|i_1| = \frac{I_1}{I_b} \cdot i_s \quad , \tag{3.21a}$$

and

$$|i_2| = \frac{I_2}{I_b} \cdot i_s \quad . \tag{3.21b}$$

Therefore, the total output currents at the collectors of Q_9-Q_{12} and Q_{15}-Q_{18} are, respectively,

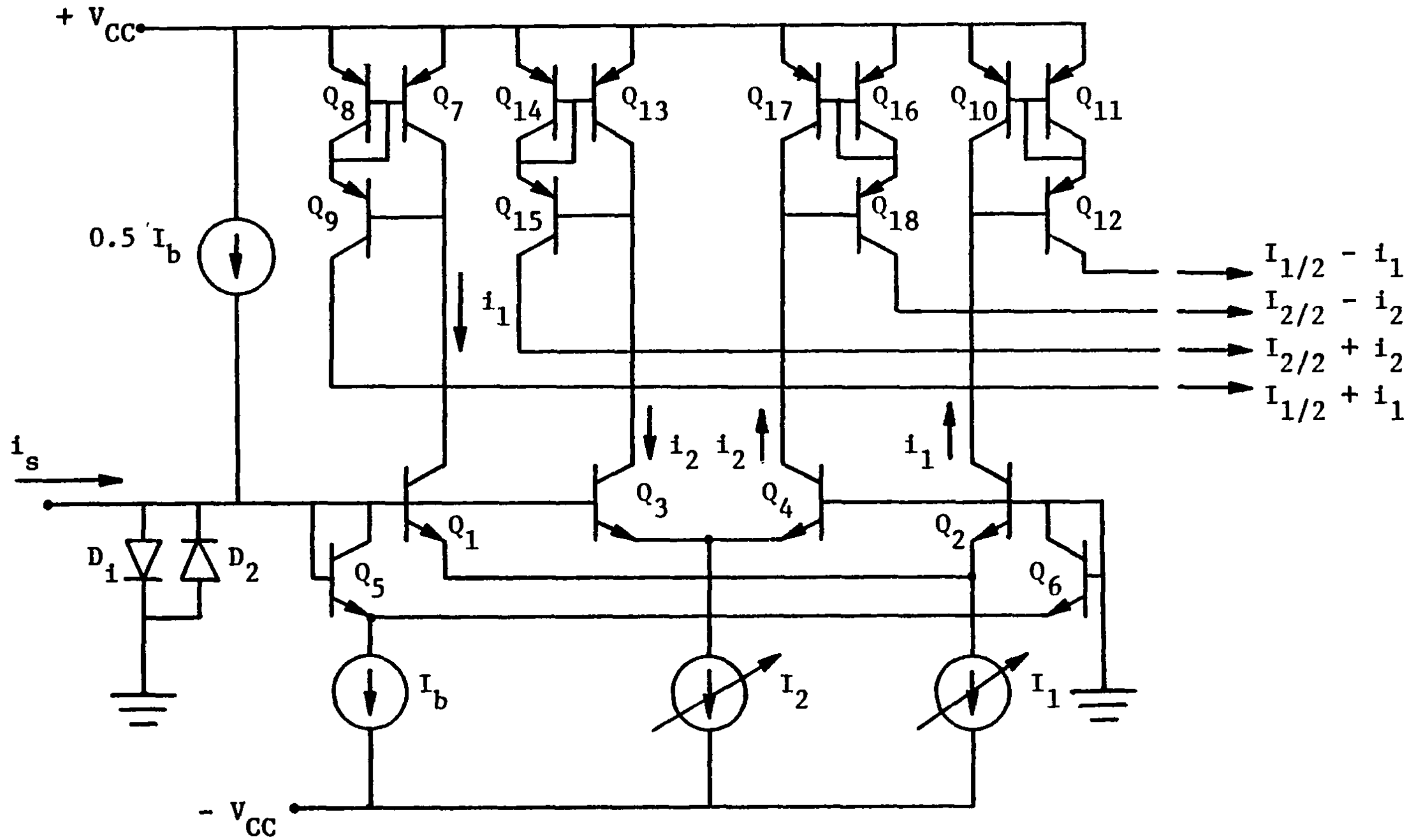


Fig. 3.6 Composite Coefficient-Setting Circuit

$$I_{o1} = \frac{I_1}{2} \pm \frac{I_1}{I_b} \cdot i_s \tag{3.22a}$$

and

$$I_{o2} = \frac{I_2}{2} \pm \frac{I_2}{I_b} \cdot i_s \tag{3.22b}$$

Note that this is a large signal analysis. Consequently, the circuit is linear through a large dynamic range of the input current i_s; in fact, i_s can have an absolute magnitude close to the bias current 0.5 I_b [Gilbert, 1968]. In addition, to be practical, the output currents are fed into a current-summing circuit, described in the next section, where a single-ended output current is obtained, and DC components are eliminated.

From Eq. (3.21), one can set the output signal currents at any positive or negative multiple of i_s by adjusting current sources I_1, I_2 and I_b. However, in practice, I_b is usually fixed, and I_1 and I_2 are varied. This is because the 0.5 I_b-current source has to be readjusted each time I_b is changed. Note that Eq. (3.21) also applies to the non-ideal case where the transistor pairs are not matched. The mismatch of the transistors causes offset currents in the circuit, and thus the dynamic ranges of the input and output currents are reduced.

The signal limitations of the circuit are the same as those of Fig. 3.2. Here again, the diodes D_1 and D_2 serve as overvoltage protection.

Current-Summing Circuit

The total output currents of Fig. 3.6 cannot be used to set feedback coefficients as yet. The DC components of the output currents must be removed so that only the signal output currents are available for feedback and feedforward purposes. This can be done by using a current summing circuit as shown in Fig. 3.7.

The basic function of this circuit configuration is similar to that of the active load circuit of the input stage of modern monolithic operational amplifiers. In fact, it is the n-p-n Wilson current mirror circuit [Wilson, 1968]. The collectors of transistors Q_1 and Q_3 are connected to the collectors of Q_{12} and Q_{15}, and Q_9 and Q_{18} of Fig. 3.6, respectively. When transistors Q_1 and Q_2 are matched and if $i_s = 0$ and $\beta = \infty$, collector current Q_3 will mirror the collector current of Q_1 exactly. In fact, this is true at all times even when there is a signal input current, i_s. Therefore, the sum of the currents at point A must be such that the collector currents of Q_1 and Q_3 are equal. Consequently,

$$i_o = 2(i_1 - i_2) \qquad (3.23)$$

where i_1 and i_2 are positive and negative feedback currents given in Eq. (3.21).

Under non-ideal conditions where the transistors are not matched, the offset currents from the circuits of Fig. 3.6 and Fig. 3.7 will appear in the output current i_o. Then, one obtains

$$i_o = I_{offset} + 2(i_1 - i_2) \quad . \qquad (3.24)$$

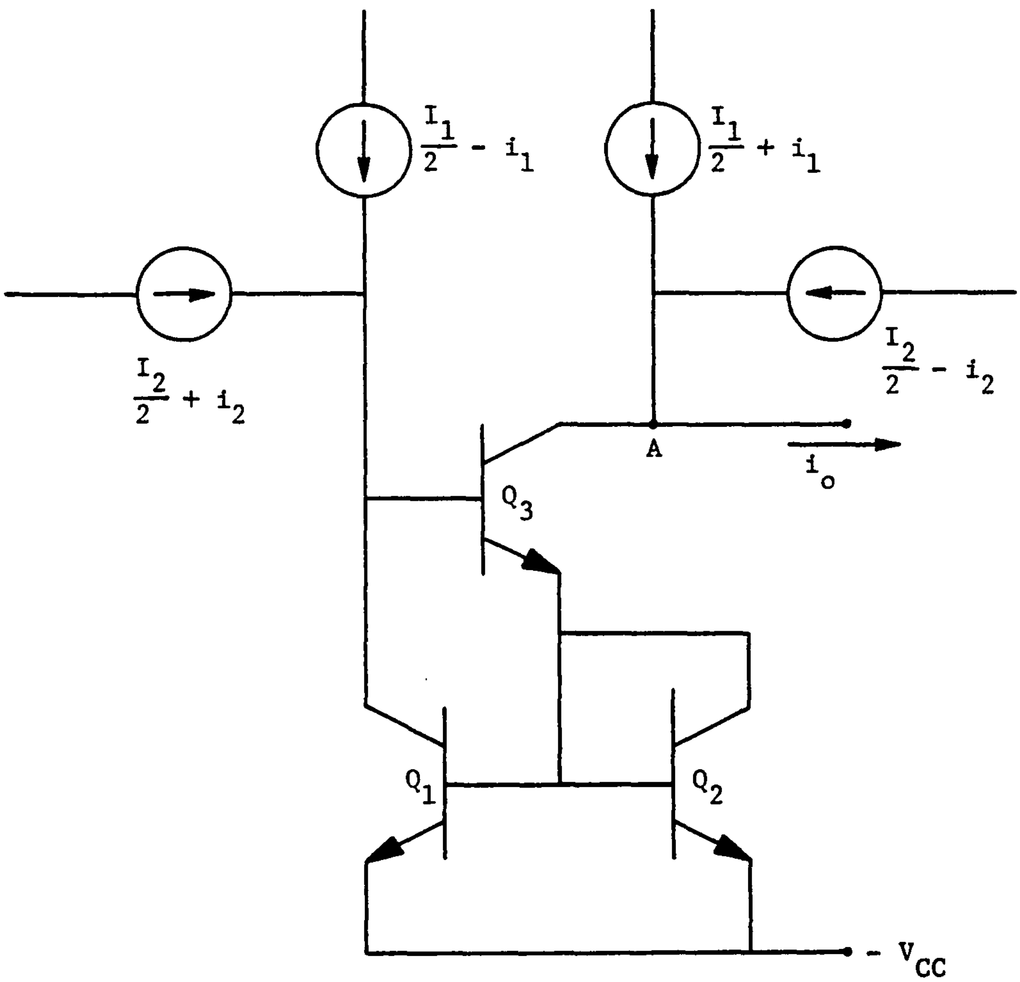


Fig. 3.7 Current-Summing Circuit

However, this offset current can be nulled out by the input stage of the differential heater circuit in Fig. 3.2.

Note that the output resistance at point A is rather high, hundreds of kilohms. In fact, it is equal to the parallel collector resistance of Q_3 in Fig. 3.7, and Q_9 and Q_{18} in Fig. 3.6. Therefore, point A simulates a current source i_o which is suitable to feed into the low impedance input of Fig. 3.2.

The circuits in Fig. 3.6 and Fig. 3.7 are incorporated to form coefficient setting networks for required feedback coefficients, positive and negative, in Chapter 5.

CHAPTER 4

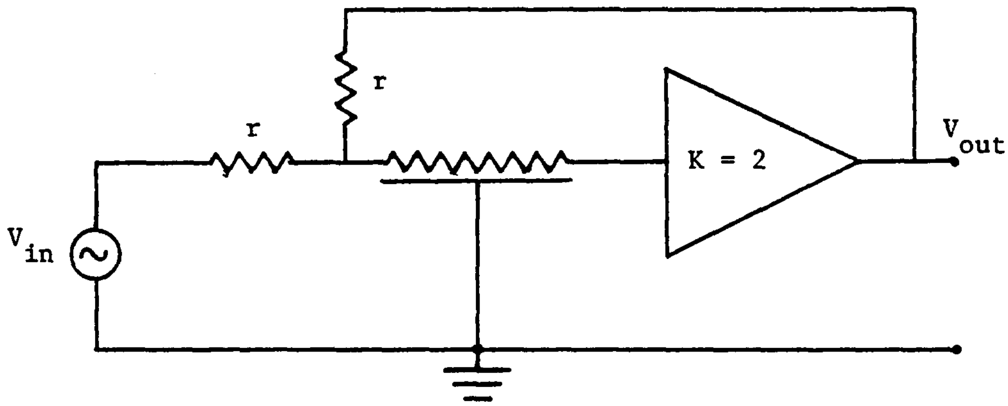
MULTIPLE-POLE ACTIVE ETC INTEGRATOR AND ITS BAND-PASS FILTERS

Introduction

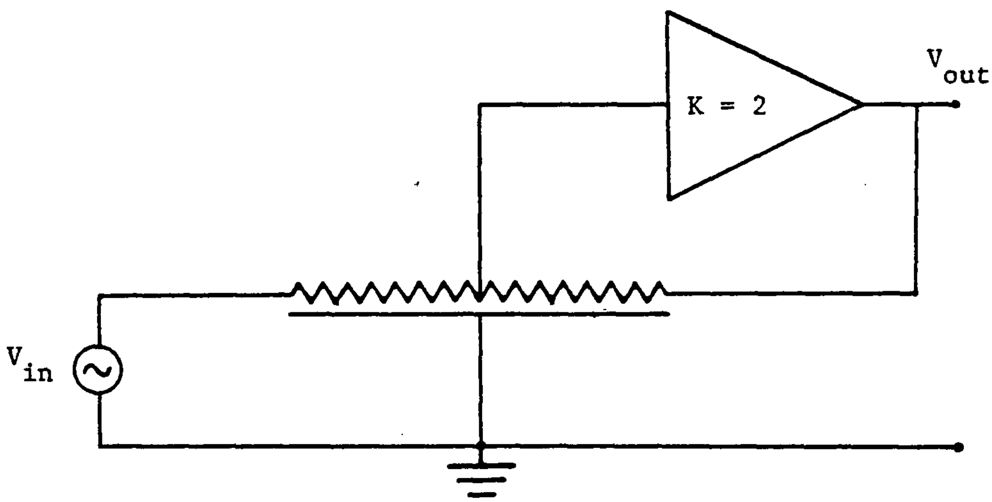
In this chapter the active URC integrator system shown in Fig. 2.3(b) is implemented by using a lumped RC line as an approximate URC structure. Then, an ETC equivalent to a URC structure is analyzed and discussed. The flow graph in Fig. 2.5(a) is used in implementing an active ETC integrator. Active ETC band-pass filters are implemented according to the flow graph analysis of Fig. 2.7 and the equation in Table 2.3(a). Finally, a discussion is presented of the results and the possibility of having two independent active ETC integrators on one chip by using this particular ETC layout.

Active URC Integrator

Before analyzing an active ETC integrator, the analogy of the multiple-pole ETC, made in Chapter 2, must be investigated in order to verify the assumptions. The active URC integrator of Fig. 2.3(a) can be implemented two ways as illustrated in Fig. 4.1. Figure 4.1(a) is a straightforward implementation from Fig. 2.3(a) where $K = 2\rho$. In contrast, Fig. 4.1(b) is a modified version of Fig. 4.1(a) where $K = 2\rho$. Note that the active URC integrator can be obtained when $\rho = 1$.



(a)



(b)

Fig. 4.1 The Active URC Integrator

In the experiment, a lumped 20 RC-section line was used as an approximation of a URC structure with R = 562Ω and C = 0.0015 μf, matched within 1%. The active integrator frequency response from both circuits was measured and the results are plotted in Fig. 4.2. Although both results have essentially the same magnitude response, the integrator of Fig. 4.1(a) is a more practical circuit. Therefore, this integrator circuit will be used in designing band-pass filters.

Band-pass filters at center frequencies ranging from 100 to 500 Hz were obtained with Q's from 10 to 40. This demonstrates the feasibility of using the URC structure in designing active band-pass filters. Next, one must find an ETC which has a transfer function similar to that of the URC structure. Active ETC filters can then be implemented.

Active ETC Integrator

The major difference between the ETC and the URC is in the nature of their inputs and outputs. While the URC system has no input-output restrictions, the input and output of the ETC are strictly limited, for all practical purposes, to thermal power and temperature, respectively. That is, the thermal transfer function of the ETC is analogous to the transimpedance function of the URC. The electrical analogy is the ratio of the open-circuit output voltage to the input current. By nature, the transimpedance function is not the same as the open-circuit voltage transfer function of the URC. With this analogy, ETC heater and sensor configurations must be obtained such that the thermal transfer function is similar to that of the open-circuit voltage transfer function of the URC. That is

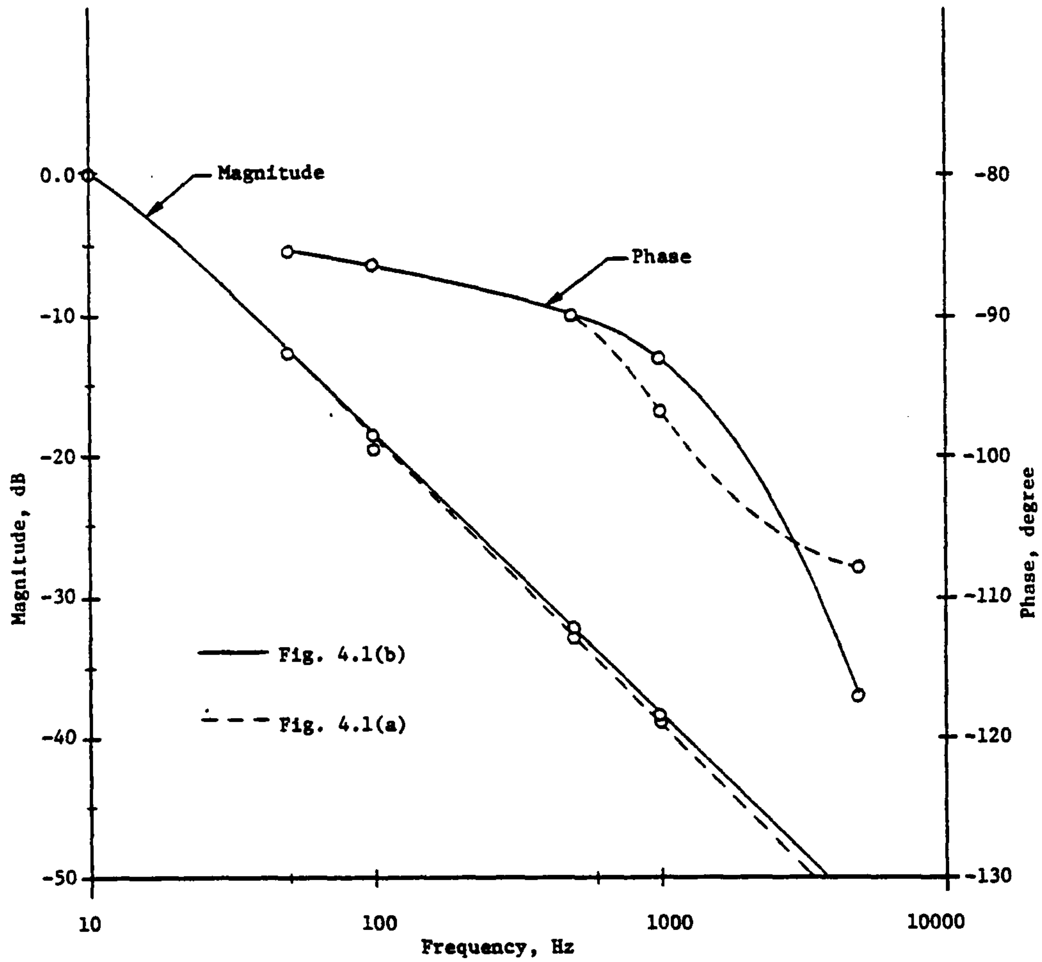


Fig. 4.2 Measured Frequency Response of Fig. 4.1(a)

$$\frac{\text{output temperature}}{\text{input heat power}}(p) = \frac{1}{\cosh\sqrt{\tau p}} \tag{4.1}$$

where τ is the thermal time constant.

Computer analysis shows that the ETC transfer function in Eq. (4.1) can be obtained by having a single heater and differential sensors as shown in Fig. 4.3, where heater and sensors are placed along the diagonal line of the ETC chip. It was also found that the same arrangement along either orthogonal center line of the ETC chip also yielded similar transfer functions. However, these have about 3 dB lower DC gains. Further, in Fig. 4.3, only one heater is necessary. When one heater is used at the corner of the chip as shown, a second device can be added for offset adjustment as will be discussed later.

The frequency response of an ETC chip 60x60x10 mils with H-film insulator 60x60x5 mils was analyzed. The results are plotted and compared with the frequency response of a URC as shown in Fig. 4.4. For the ETC, the heater areas are 6x6 mils, and those of the sensors are 2x2 mils. As one can see, the ETC frequency response is closely matched with that of the URC at low frequencies. The thermal time constant, τ, is 0.012 sec.

A photomicrograph of the chip is shown in Fig. 4.5. The measured open-loop frequency response of the ETC is plotted and compared with the computer analysis and that of Eq. (4.1) in Fig. 4.4. Measurements were made by using heater and sensor circuits of Fig. 4.6 ($R_f = \infty$) with heater and sensor conversion constants K_h = 71.96 mW/mA and K_s = 5.09 V/°C,

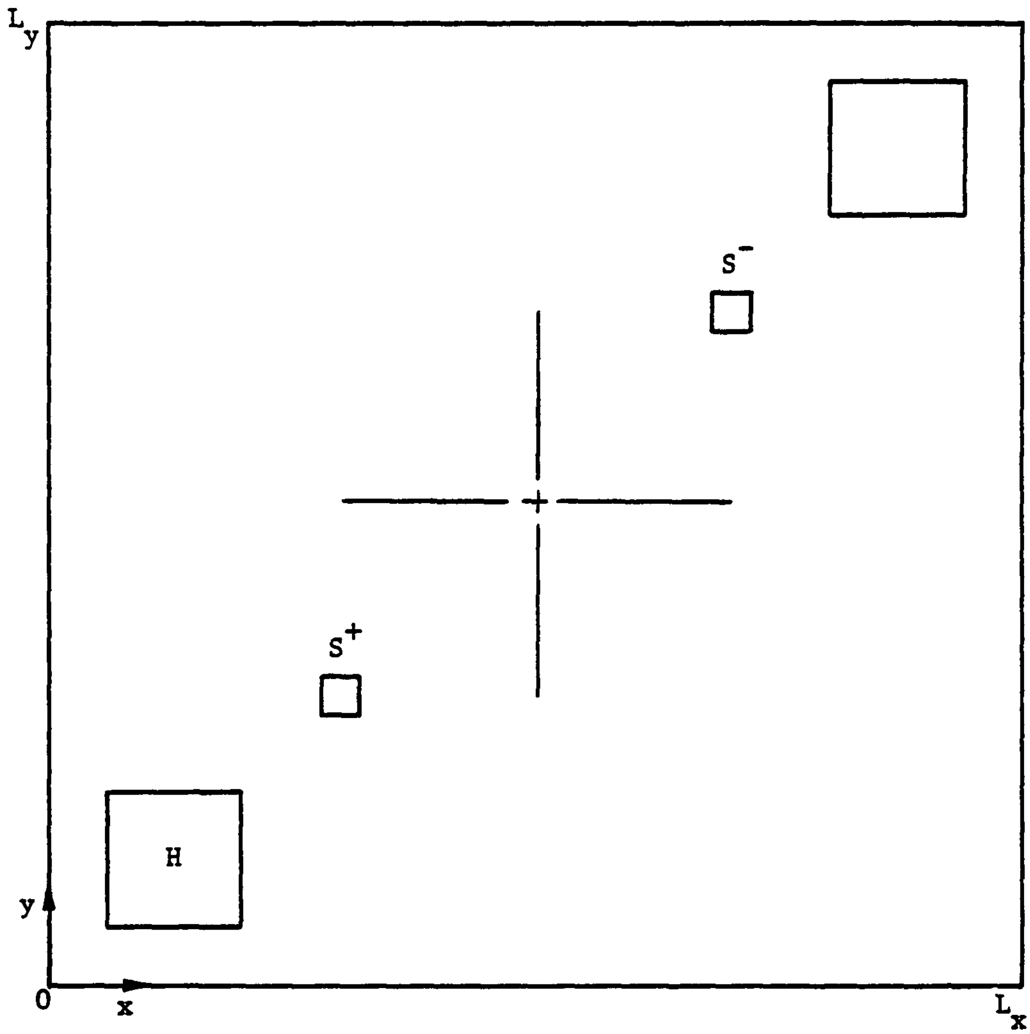


Fig. 4.3 Multiple-Pole ETC Layout

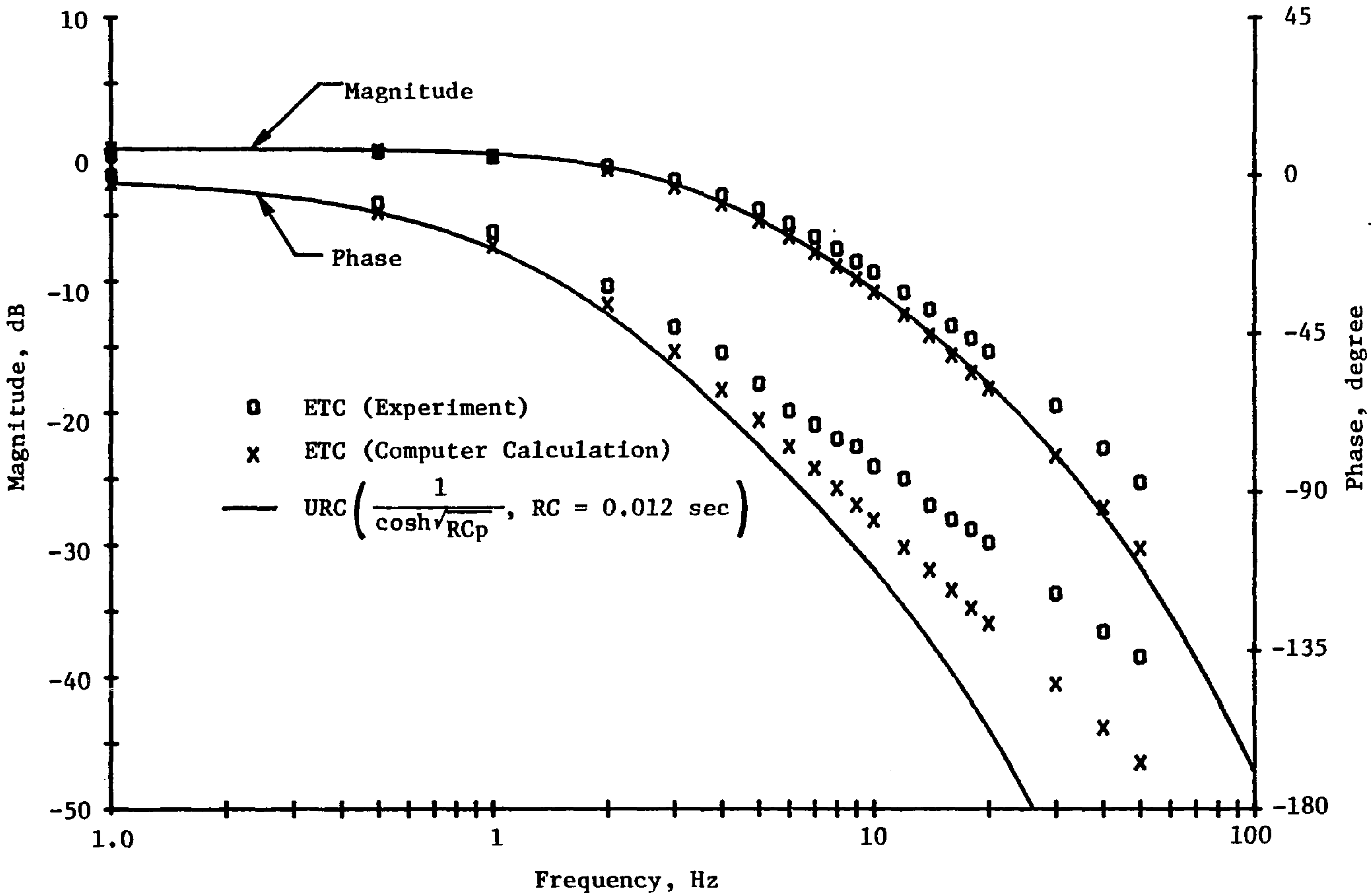


Fig. 4.4 Comparison of URC and ETC Frequency Response, Both from Computer Calculation and Experiment Results

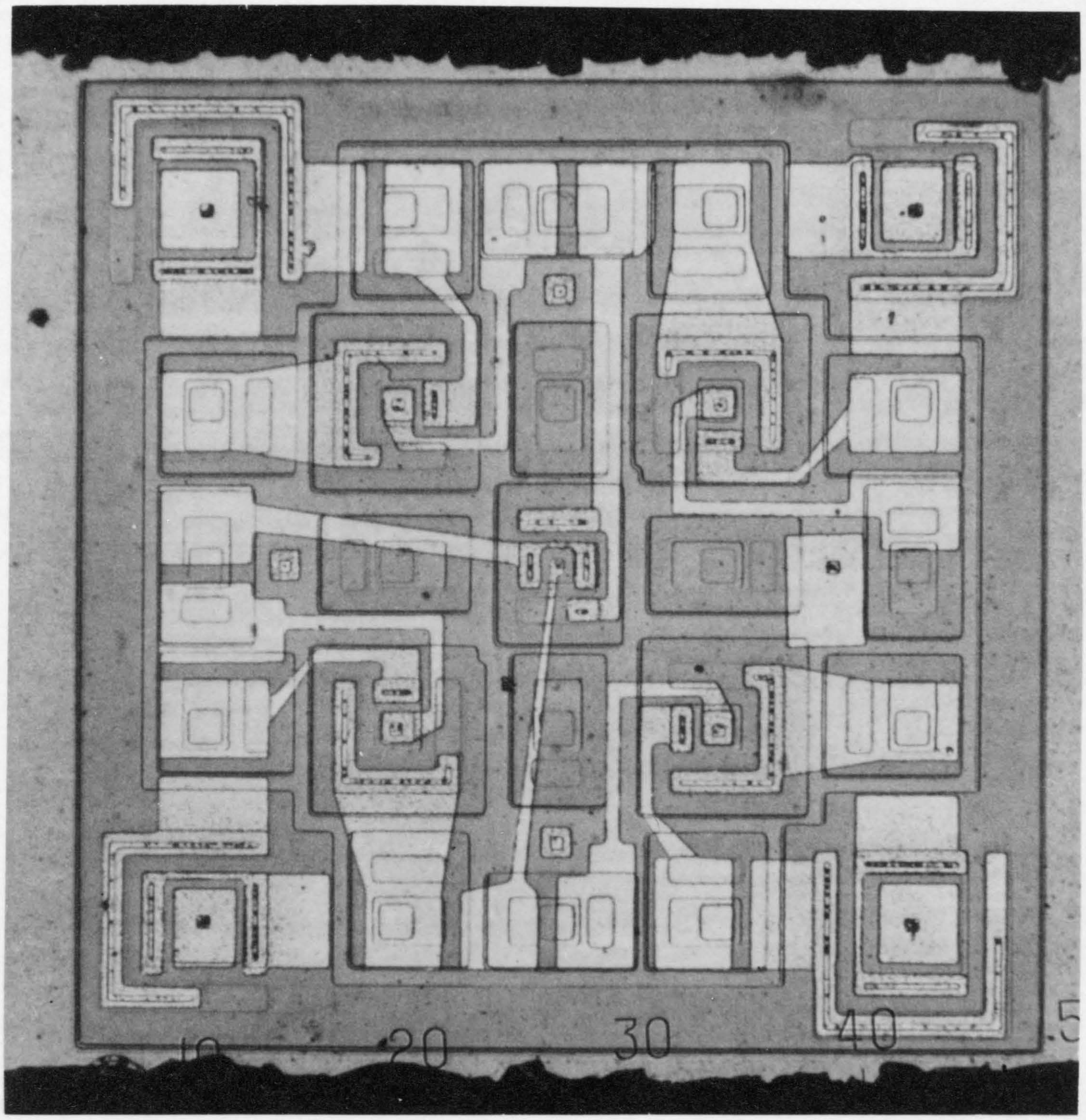


Fig. 4.5 Photomicrograph of the ETC Chip (X84 magnification)

respectively. It is clear that the ETC can be made closely analogous to the URC structure shown in Fig. 2.3(a).

For the active ETC integrator, from the flow graph in Fig. 2.5(a), the transfer function is

$$\frac{V_{out}}{V_{in}}(p) = \frac{K_h K_s F(p)}{1 - \rho\, K_h K_s F(p)} \tag{4.2}$$

To obtain an active ETC integrator, the feedback coefficient, ρ, must be

$$\rho = \frac{1}{K_h K_s F(0)} \tag{4.3}$$

where F(0) is the DC gain of the ETC transfer function.

Figure 2.5(a) is implemented by using heater and sensor circuits presented in Fig. 3.1 and Fig. 3.2. The active ETC integrator is shown in Fig. 4.6. For this realization, Equations (4.2) and (4.3) become

$$\frac{V_{out}}{V_{in}}(p) = \frac{K_h K_s F(p)}{R_1\left[1 - \frac{K_h K_s F(p)}{R_f}\right]} \tag{4.4}$$

and

$$\rho = \frac{1}{R_f}\ , \tag{4.5}$$

respectively. Hence, from Eq. (4.3)

$$R_f = K_h K_s F(0)\ . \tag{4.6}$$

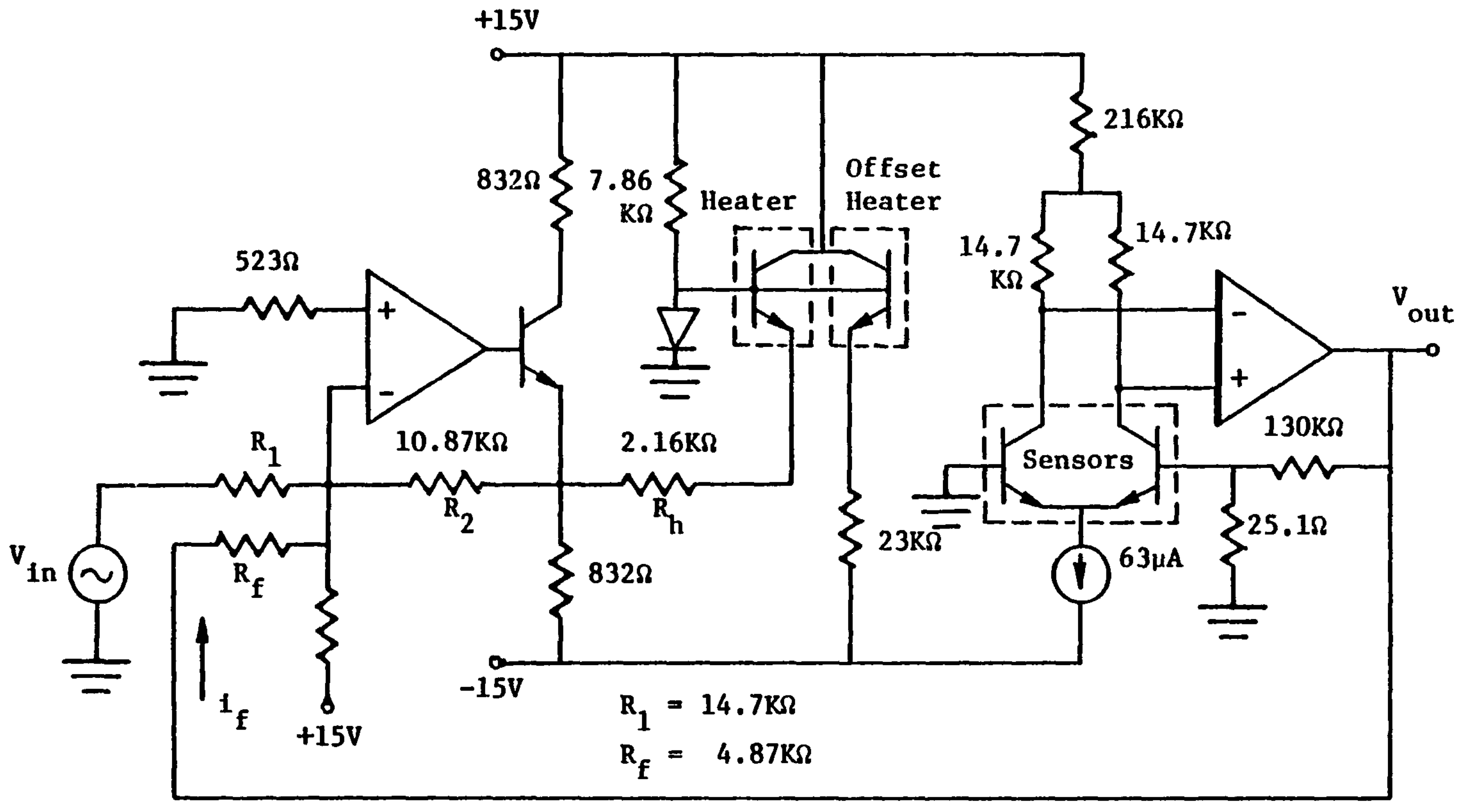


Fig. 4.6 Active ETC Integrator Circuit

By using Equations (4.1) and (4.6), Eq. (4.4) becomes

$$\frac{V_{out}}{V_{in}}(p) \approx \frac{2K'}{R_1 \tau p} \tag{4.7}$$

where $K' = K_h \cdot K \cdot K_s$ as defined in Chapter 2. Equation (4.7) can be rewritten as

$$\frac{V_{out}}{V_{in}}(p) \approx \frac{H}{p} \tag{4.8}$$

where $H = 2K'/R_1\tau$.

From the numerical values given previously and those in Fig. 4.6, R_f = 4.87K and H = 53.99 rps. The measured closed-loop frequency response is plotted and compared with the computer analysis results in Fig. 4.7. Although the measured values of magnitude are less than expected, the slopes of the magnitude response are essentially the same, i.e., 20 dB per decade. Figure 4.7 also indicates that the active ETC integrator can be used in the frequency range of 5 to 100 Hz.

The active ETC discussed above is a positive feedback system. Any offset voltage existing at the sensor output will always be fed back to the heater input which will cause voltage saturations of heater and sensor circuits. To nullify the sensor offset voltage, the second heater transistor was used as indicated in Fig. 4.6. The offset power supplied to the transistor reduces the temperature difference of the sensor transistors when the input power is at its operating power, i.e.,

$$P_o = V_{CB} \frac{R_2}{R_h} \cdot I_o$$

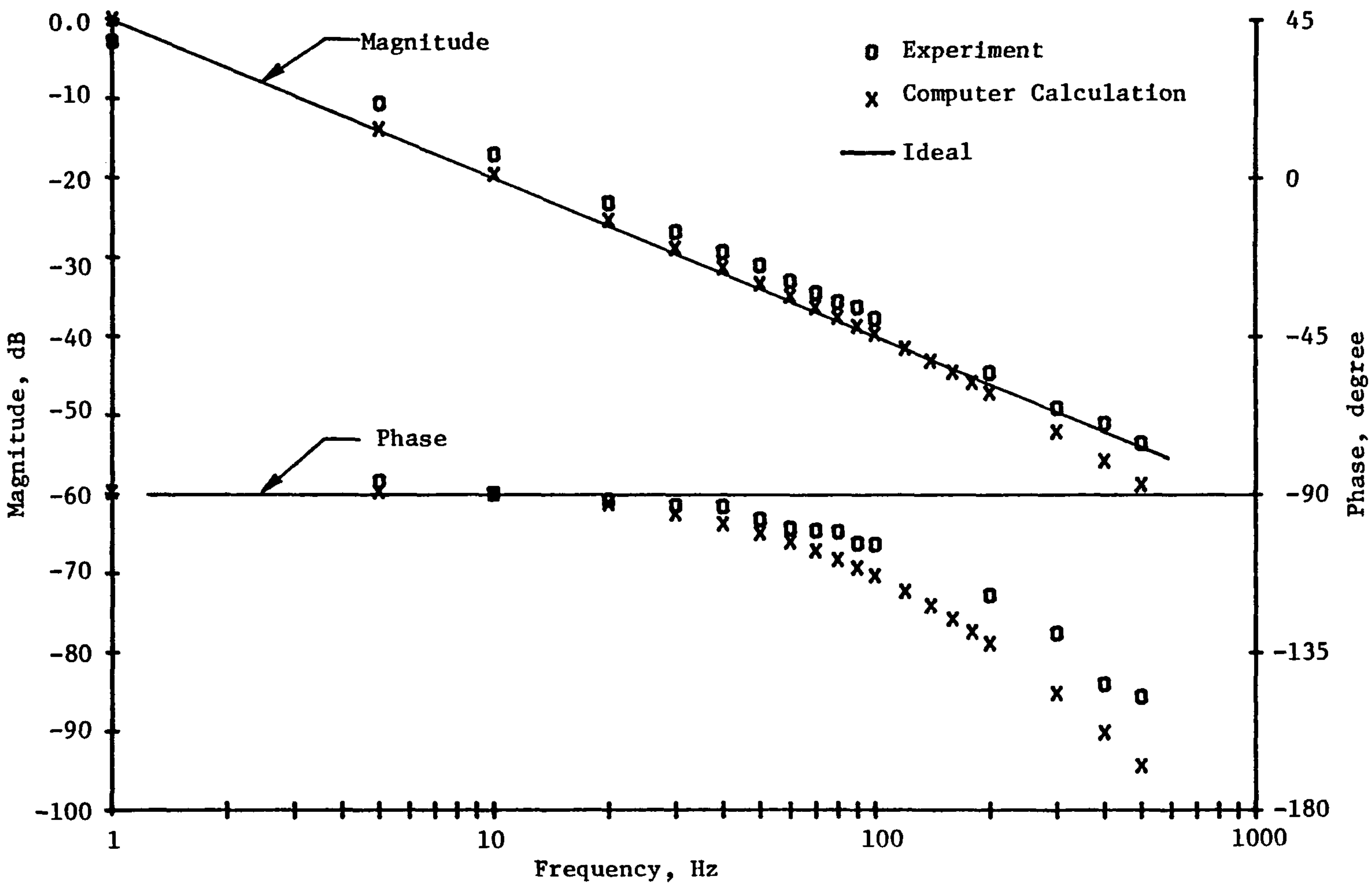


Fig. 4.7 Measured and Computer Analysis Frequency Response of the Active ETC Integrator

Active ETC Band-Pass Filter Designs and Experiments

By using the previously discussed active ETC integrators and a summing amplifier, a second-order state-variable band-pass filter system is implemented as shown in Fig. 4.8. Each square block represents an active ETC integrator of the type shown in Fig. 4.6. With the summing amplifier added, Equations (2.13), (4.1), and (4.7) yield the band-pass function

$$\frac{V_{out}}{V_{in}}(p) = \frac{R_1/R_{in}\ Hp}{p^2 + \frac{R_7}{R_3}Hp + \frac{R_7}{R_4}H^2} \tag{4.9}$$

where

$$|T(j\omega_o)| = \frac{R_3R_1}{R_7R_{in}}$$

$$\omega_o = H\sqrt{R_7/R_4}$$

$$Q = \frac{R_3}{\sqrt{R_7R_4}}$$

By adjusting values of R_3, R_4, and R_7, one can readily design band-pass filters at various center frequencies and Q's. With Q = 10, band-pass filters having center frequencies at 10, 50 and 100 Hz were designed and constructed. The measured frequency response of the filters is shown in Figs. 4.9, 4.10. and 4.11. Measured and calculated

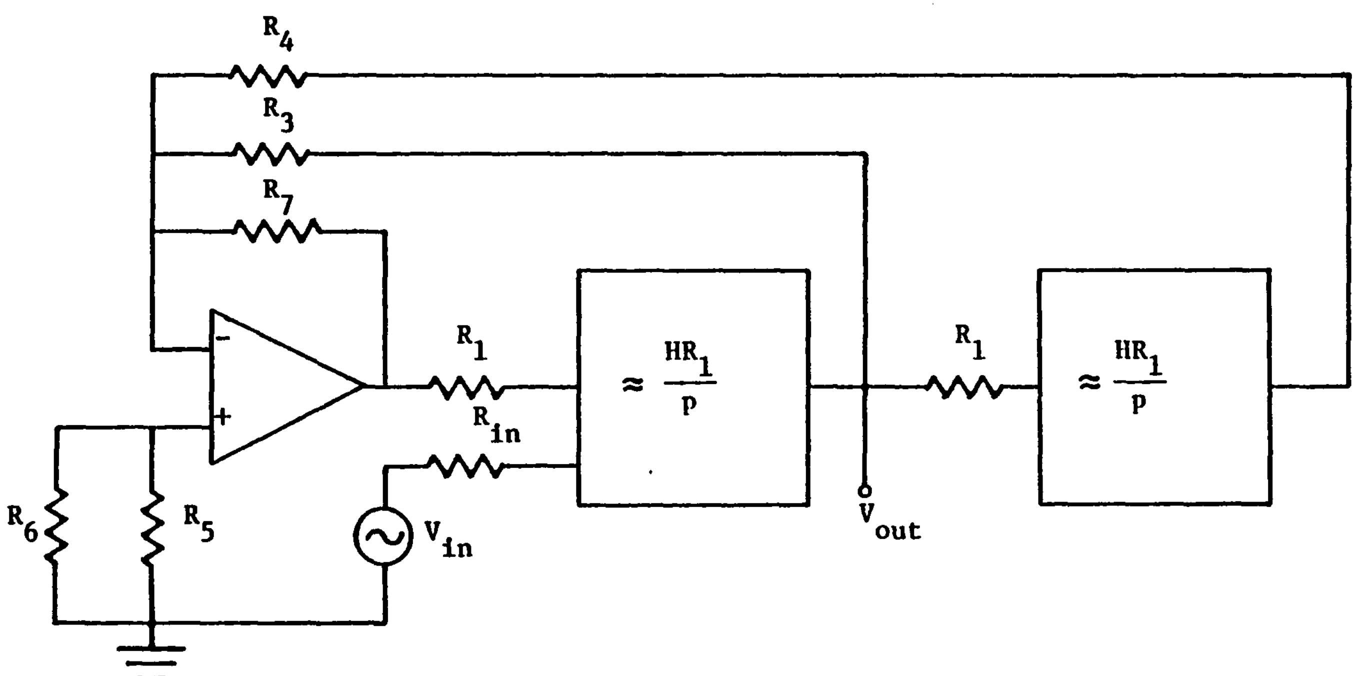


Fig. 4.8 Second-Order State-Variable Active ETC Filter Schematic

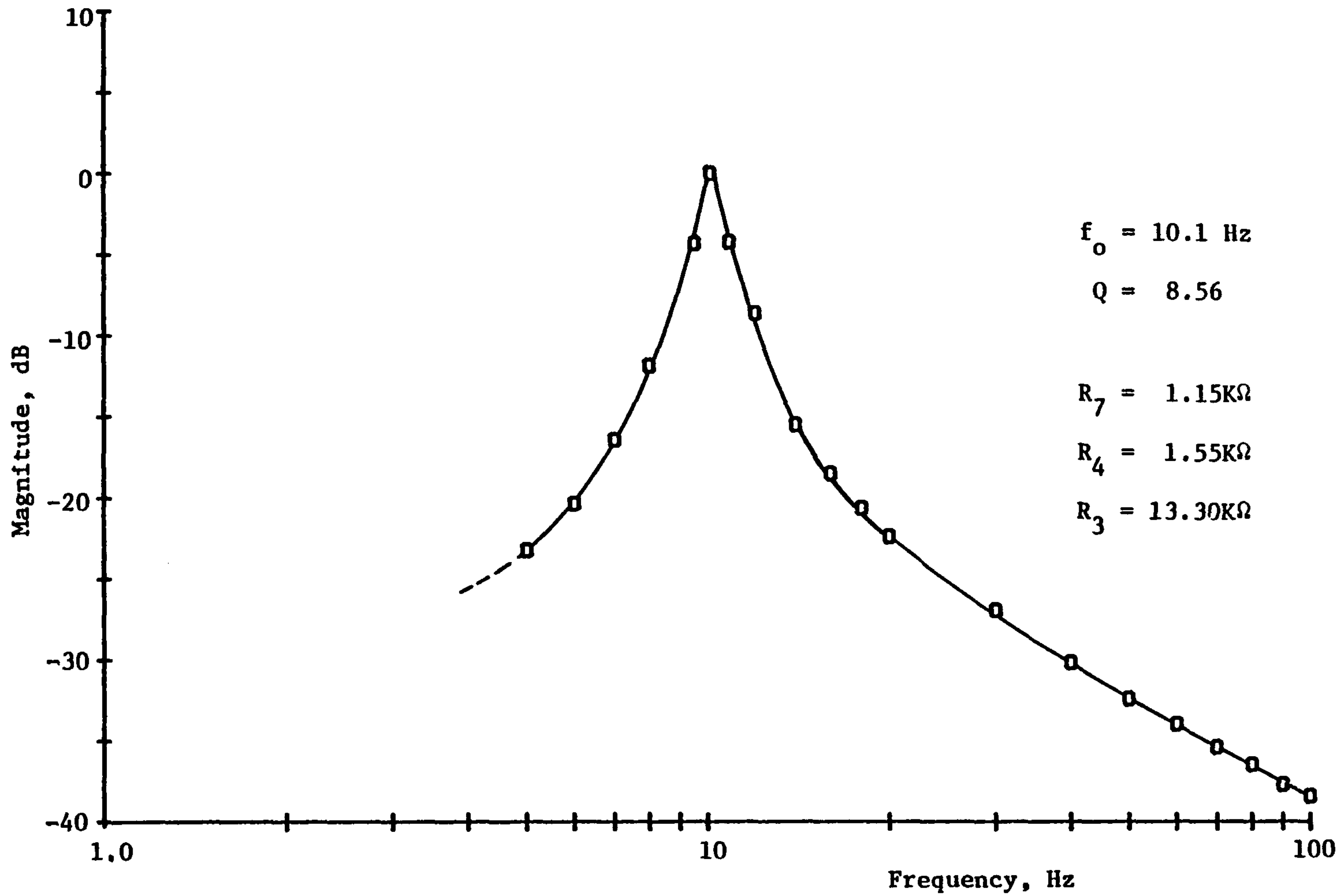


Fig. 4.9 Measured Magnitude Response of the Active ETC Band-Pass Filter (f_o = 10.1 Hz, Q = 8.56)

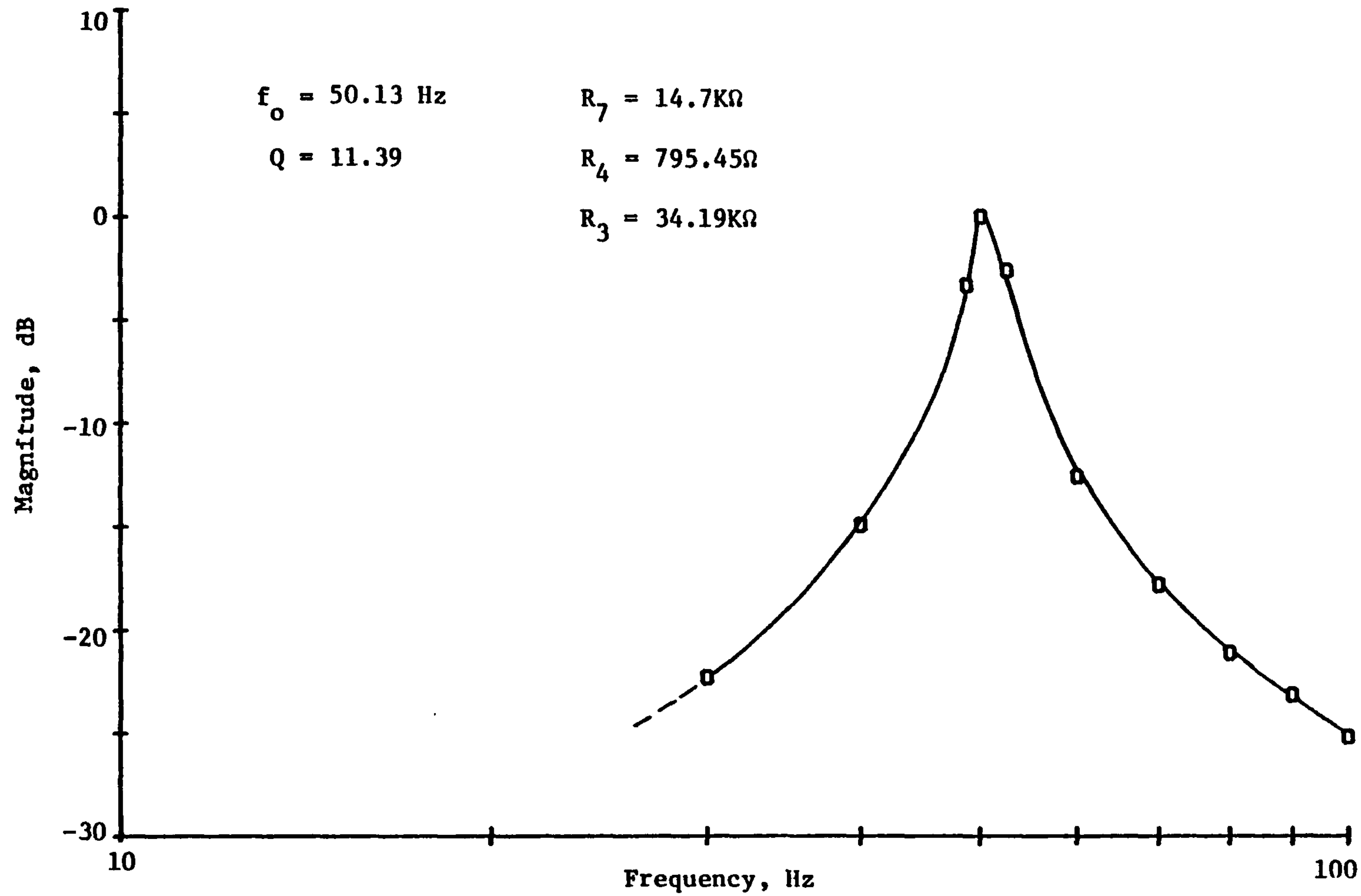


Fig. 4.10 Measured Magnitude Response of the Active ETC Band-Pass Filter (f_o = 50.13 Hz, Q = 11.39)

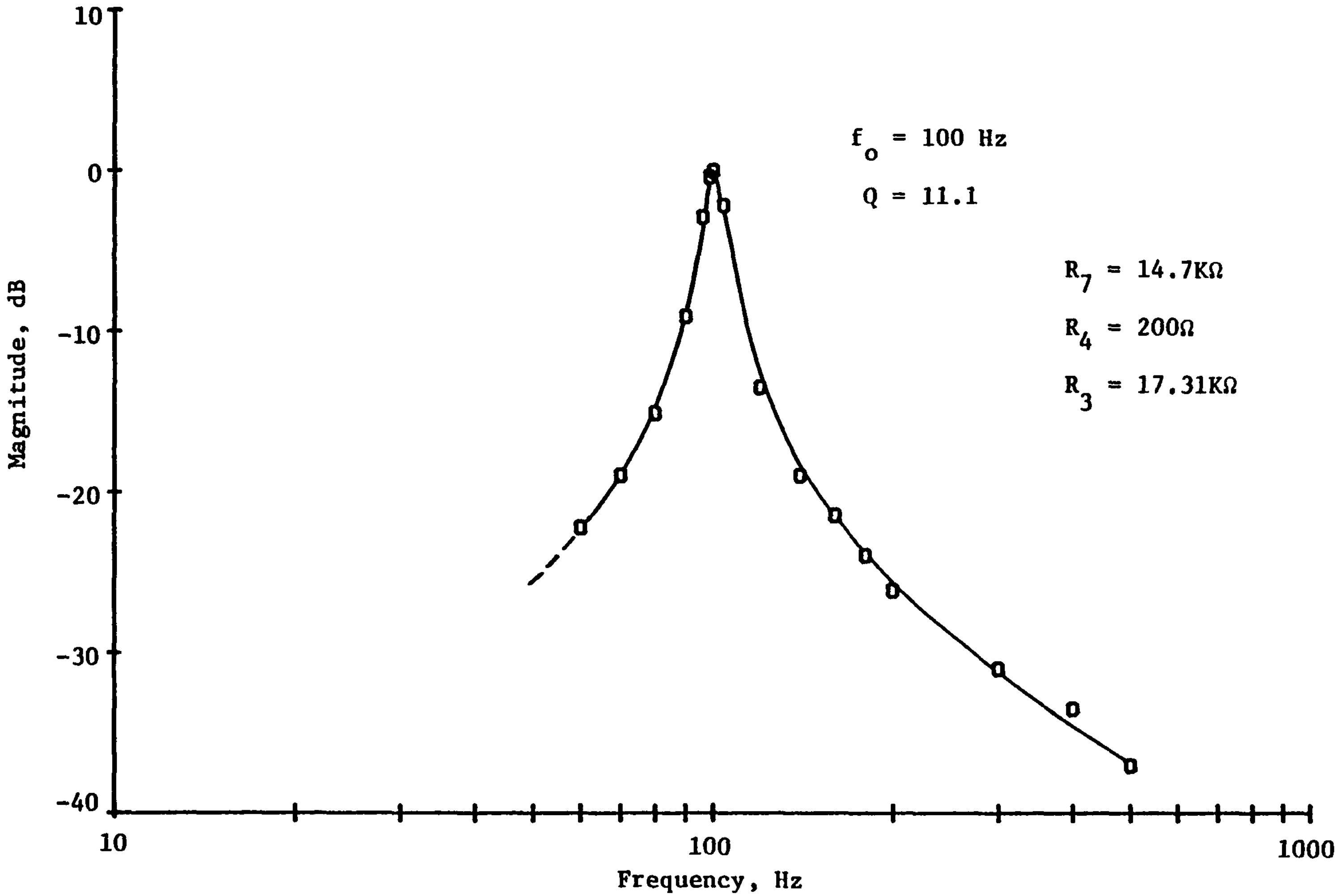


Fig. 4.11 Measured Magnitude Response of the Active ETC Band-Pass Filter (f_o = 100 Hz, Q = 11.1)

results are compared in Table 4.1. The reason for different center frequency gains is that different values of the ratio R_3/R_7 were used.

Note that the H value in this case must be found experimentally rather than from Eq. (4.8), since in the experiment R_f cannot be set to the exact value given in Eq. (4.6). From Eq. (4.9), it is clear that H is the center frequency of the band-pass filter when R_7/R_4 is set to unity. Hence, from the experiment, H = 73.07 rps.

Discussion and Conclusions

All the experimental results presented in the preceding sections proved that multiple-pole active ETC filters can be obtained by incorporating positive electrical feedback and state-variable filter design technique. The major problem of this type of filter is that the single heater ETC inherently produces sensor offset voltages. A fairly stable offset adjustment system is required since the feedback coefficient of the integrator depends directly on the sensor output voltage. Any changes of the feedback coefficient may cause oscillations. In addition, the temperature dependence of thermal conductivity and capacity of both silicon and insulator must be compensated.

In spite of the above problems, it has been demonstrated that second-order state-variable active ETC filters can be obtained with two ETC chips instead of four [Louw, 1975]. Other filters rather than band-pass can be obtained in similar fashion.

If one examines Fig. 4.3 closely, another set of heaters and sensors can be placed along the other diagonal line. This is shown in

Table 4.1 Calculated and Measured Values of the Active ETC Band-Pass Filter Parameters and Their Percent Errors

Parameters	Calculated	Measured	Error (%)
f_o:			
Fig. 4.9	10.02	10.10	+0.80
Fig. 4.10	50.39	50.13	-0.52
Fig. 4.11	99.71	100.00	+0.29
Q:			
Fig. 4.9	7.48	8.56	+14.44
Fig. 4.10	10.13	11.39	+12.44
Fig. 4.11	10.10	11.10	+9.90
$\|T(j\omega_o)\|$:			
Fig. 4.9	9.96	10.00	+0.40
Fig. 4.10	2.34	2.50	+6.84
Fig. 4.11	1.18	1.42	+20.34

Fig. 4.12. In principle, since the two sets are arranged orthogonal to each other, there should be two independent multiple-pole ETC transfer functions on one chip. However, this must require very accurate determination of chip dimensions as well as closely matched transistor areas and locations.

In the experiments, the definition of the ETC chip was not quite perfect due to difficulties in diamond saw cutting of the chip. There were both DC and AC signal interactions between channels. The interaction was measured to be about -20 dB, open-loop, which was large enough that the closed-loop transfer function of both channels could not be accurately obtained. The feedback coefficients could not be properly set. Therefore, other types of ETC configurations must be investigated which will be suitable for designs requiring two active ETC integrators on one chip.

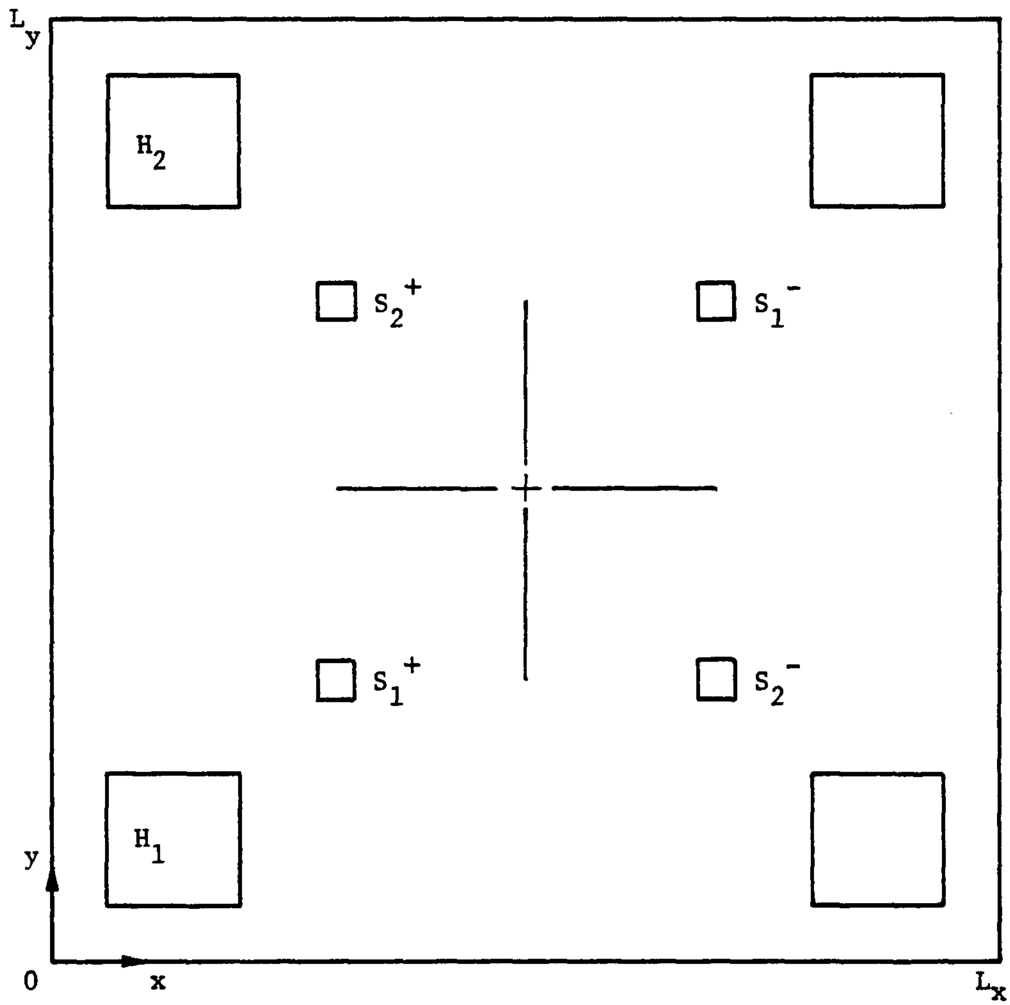


Fig. 4.12 Orthogonal Configuration of Fig. 4.3

CHAPTER 5

TWO INDEPENDENT ETC INTEGRATORS ON ONE CHIP

Background and ETC Configurations

Background [Louw, 1975]

An ETC configuration suitable for use as a two-channel ETC chip was first investigated by Louw [1975]. The configuration consists of two differentially driven heaters and two differential sensors with heater and sensor locations so arranged, as shown in Fig. 5.1, that the ETC thermal transfer function has approximately single pole behavior. Thus

$$F(p) = \frac{K}{p + \pi^2 \omega_x} \tag{5.1}$$

where K is a constant and ω_x is as defined in Chapter 2. All the heater and sensor locations are important but the y-coordinate of the center of the sensor areas; these can have any y-coordinates as long as the length of the heater area is equal to L_y. These specific heater and sensor locations were obtained from differential ETC solutions of Eq. (2.2).

To obtain a two-channel ETC, two of the ETC configurations in Fig. 5.1 are superimposed orthogonally so that the interaction between

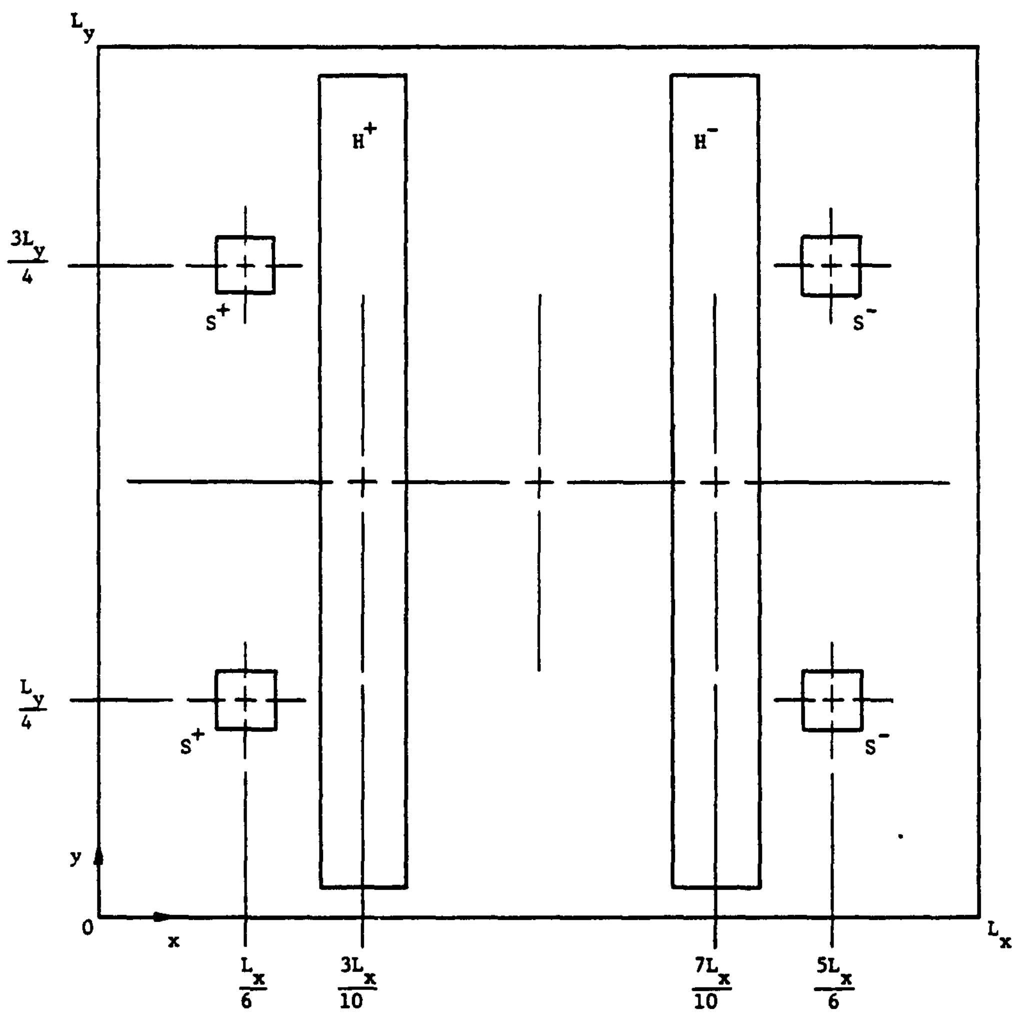


Fig. 5.1 Differential Heater and Sensor Geometry of Approximately Single Pole Thermal Transfer Function

the two channels is minimum. Figure 5.2 shows such an arrangement [Louw, Hamilton and Kerwin, 1977].

The configuration in Fig. 5.2 was fabricated with chip dimensions 60x60x10 mils, and the ETC chip was mounted on an H-film insulator with dimensions 60x60x5 mils. From the given dimensions, Eq. (2.6) and Table 2.1, the cutoff frequency of Eq. (5.1) was approximately 35 Hz, and the DC gain was approximately 8×10^{-3} °C/mW.

For the experimental chip, it was found that the DC gain was too low; and that the offset voltages forced the bias power to an unacceptable level. To alleviate the problem, the DC gain of the ETC transfer function must be increased by reducing the chip thickness. Similarly, for a better single-pole approximation an insulator of lower specific thermal capacitance (of the order of 10^{-6} $\frac{\text{mW-sec}}{\text{mil}^3\text{-°C}}$) was recommended.

In addition to Louw's recommendation, there are other problems that must also be considered. The fabrication of the ETC chips in Figures 5.1 and 5.2 is not trivial; some approximations must be made in the layout since two different heaters cannot occupy the same space. New heater and sensor locations must be found, if possible, to produce a transfer function whose characteristics are at least as good as those of Eq. (5.1). Another problem is the thermal interaction between the two channels in Fig. 5.2. This problem is evident in the experiments of multiple-pole ETC's presented in Chapter 4. Hence, the interaction problem and chip thickness reduction problem are major obstacles to the design of a two-channel ETC on one chip. Since the approximation of a

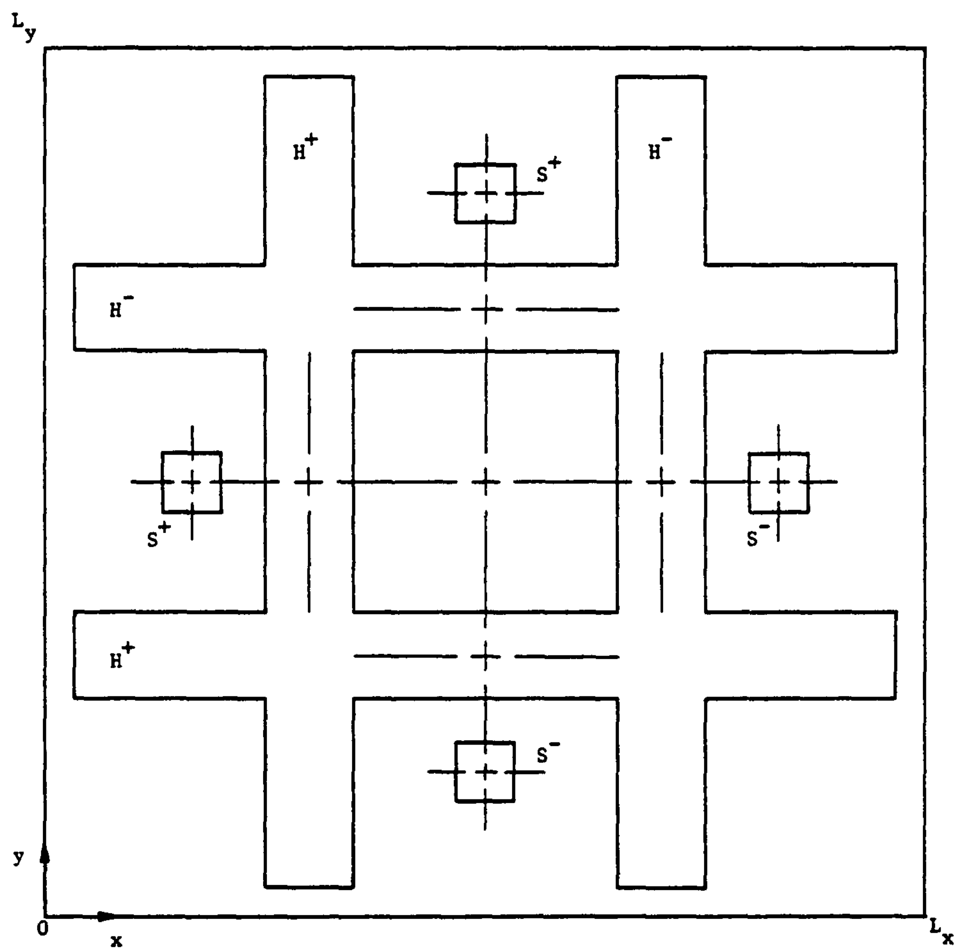


Fig. 5.2 Two Independent ETC Thermal Transfer Functions on One Chip

single-pole ETC is presently satisfied, the insulator problem is considered minor.

In summary, there are three problem areas to be investigated. First, new heater and sensor locations and sizes are needed so that they are more practical to fabricate. Secondly, ETC chip dimensions for higher DC gain must be investigated. Finally, the two-channel ETC on one chip must be designed such that the interaction between channels is minimum. The first two problems are investigated and discussed in this section, and the last problem is investigated in a later section.

ETC Configurations

Analysis shows that one can derive alternate heater and sensor locations which produce thermal transfer functions identical to that of Eq. (5.1). The analysis, similar to that done by Louw [1975], starts with the writing of Eq. (2.11) in terms of differential heaters and sensors. Then the heater and sensor locations are chosen so that the residues of undesired poles vanish. The analysis is presented in Appendix A.

Figures 5.3 and 5.4 are the new heater and sensor locations; optional locations are also included. The optional sensor and heater locations are represented by the dotted lines in Figures 5.3 and 5.4, respectively. These optional locations also produce approximately the same single pole thermal transfer function as that of Eq. (5.1), but with less DC gain. [See Appendix A, Eq. (A.9)]. Note that by applying the reciprocity theorem, one can obtain the configuration of Fig. 5.4 from Fig. 5.3, and vice versa. In practice, it is not necessary

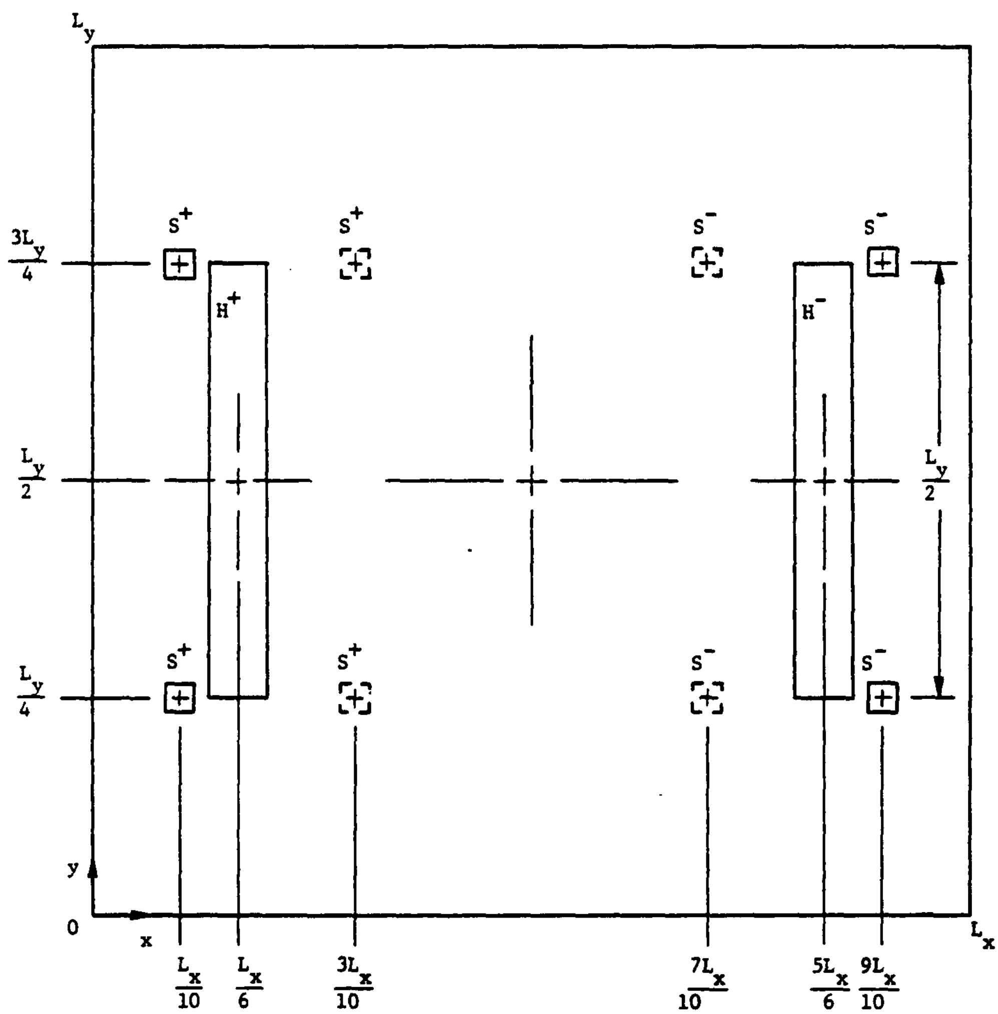


Fig. 5.3 The New ETC Configuration ($c_x = L_x/6$)

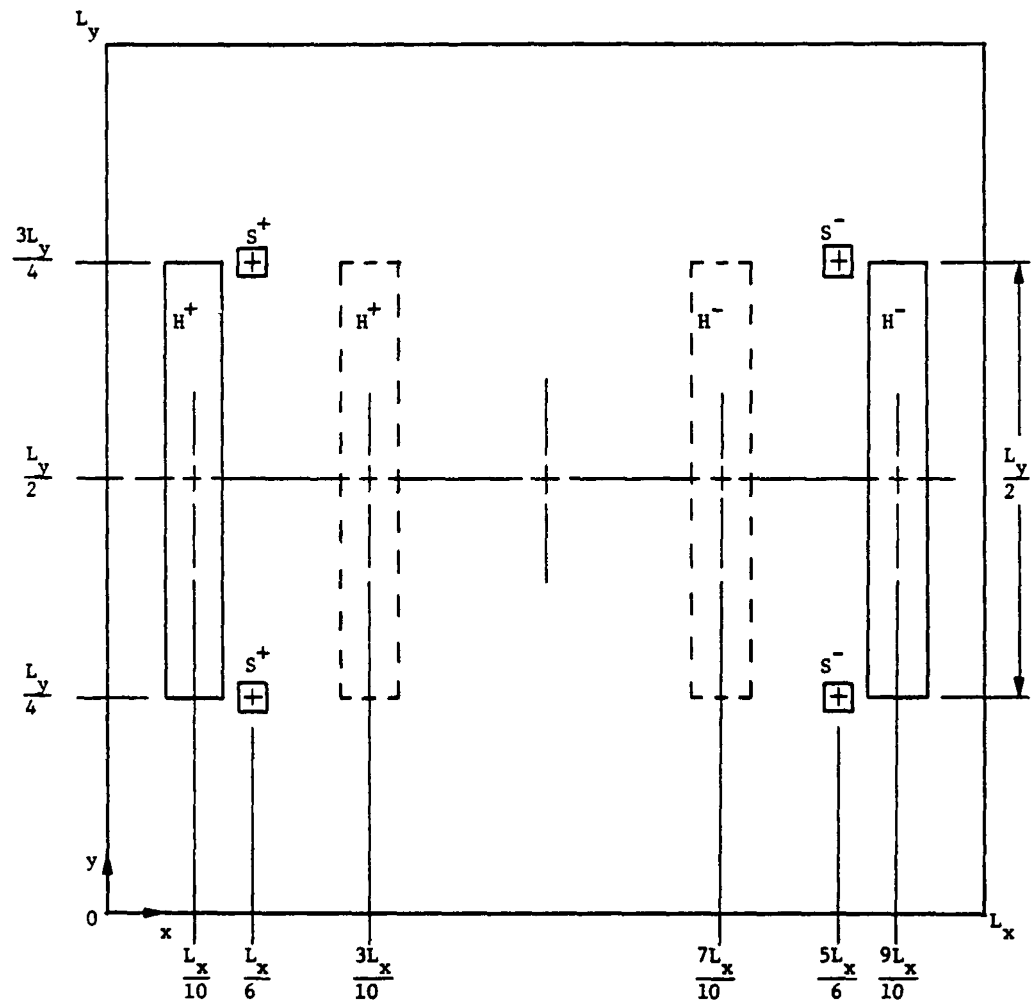


Fig. 5.4 The New ETC Configuration ($d_x = L_x/6$)

to have the optional sensors and heaters; either set of heater and sensor locations may be chosen to satisfy the design requirements, and processing constraints.

To obtain higher DC gain and satisfy the processing constraints, the configuration in Fig. 5.3 is chosen for a prototype ETC structure.

With suitable approximations, the thermal transfer function can be rewritten as

$$F(p) = \frac{K}{p + \gamma} \tag{5.2}$$

where

$$K = \frac{8\omega_x}{ak_s} \cdot \frac{L_x}{L_y} \cdot \cos\frac{\pi}{6} \cdot \cos\frac{\pi}{10}$$

$$\gamma = \pi^2 \omega_x$$

Consequently, the thermal DC gain is

$$\frac{K}{\gamma} = \frac{8 \cdot \cos \pi/6 \cdot \cos \pi/10}{k_s \; \pi^2} \left(\frac{L_x}{aL_y}\right) \tag{5.3}$$

The analysis has evidently shown that the layout problem of Fig. 5.1 has been solved. Similarly, Eq. (5.3) provides greater perception of what is involved to increase the thermal DC gain. Reducing the chip thickness is clearly a solution as recommended. On the other hand, the DC gain can also be increased by having L_x/L_y greater than unity. Therefore, in addition to heater and sensor locations given in

Fig. 5.3, the DC gain can be increased by having a thin rectangular chip as shown in Fig. 5.5. For example, for L_x = 60 mils and L_y = 20 mils, the DC gain in Fig. 5.5 is three times greater than that of Fig. 5.3 with the same chip thickness.

The implementation of a thin rectangular ETC chip requires the addition of processing steps to the standard integrated circuit fabrication; these are discussed in a later section.

ETC Band-Pass Filter Analysis and Design

From the ETC thermal analysis in the previous section, the heater and sensor locations are so chosen that an approximately single pole ETC system is obtained. Two such ETC systems of the type shown in Fig. 5.5 must be used to design a second-order state-variable filter system. A band-pass filter design is used here to demonstrate the innovation made in the previous section. Once this is obtained, low-pass, high-pass, and band-elimination filters can be obtained in similar fashion.

Analysis

The general analysis of a second-order state-variable ETC band-pass filter has already been given in Fig. 2.7, and the results are tabulated in Table 2.3(b). However, for more practical results, the analysis is modified slightly as shown in Fig. 5.6. Then, the transfer function becomes

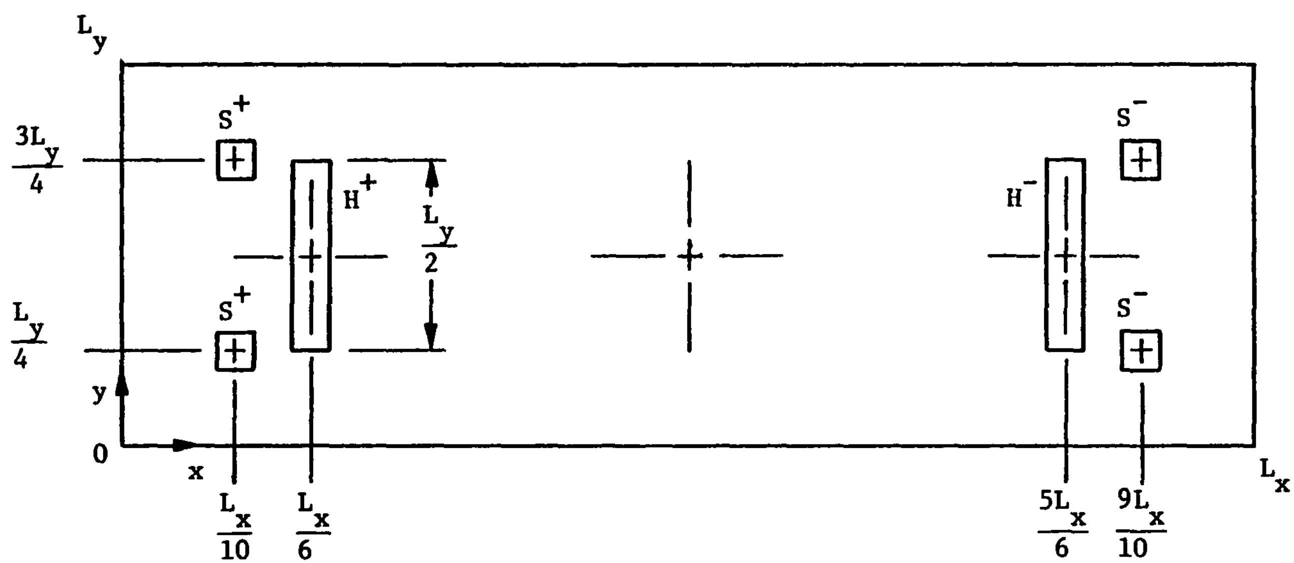


Fig. 5.5 Rectangular ETC Structure of Fig. 5.3

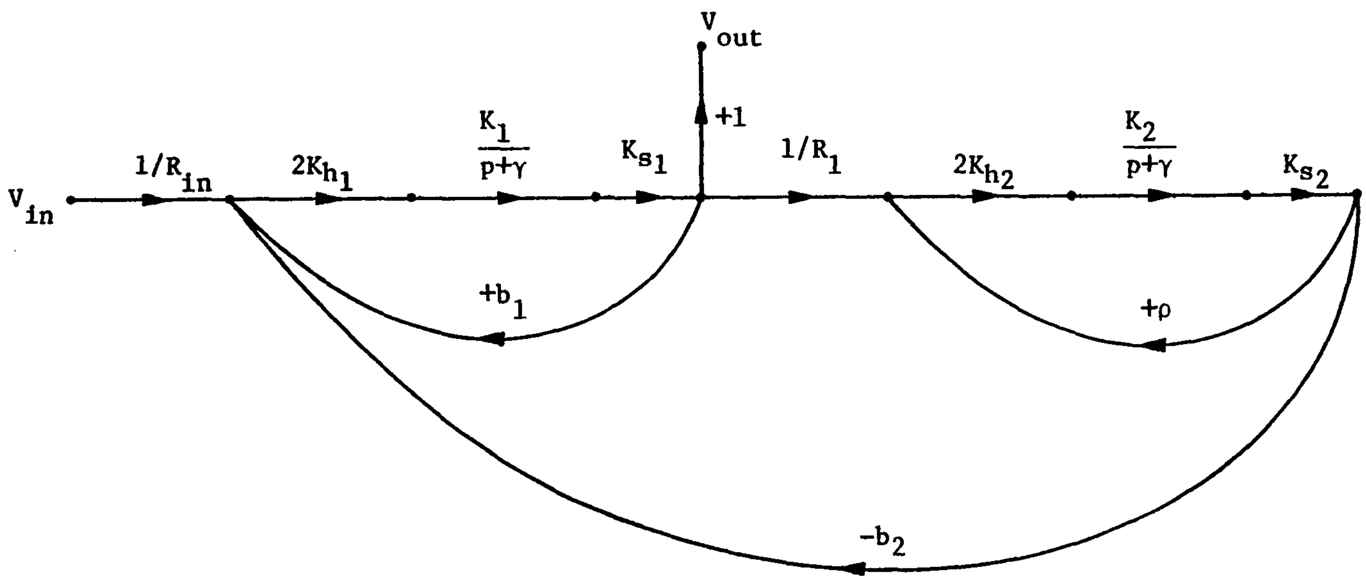


Fig. 5.6 Flow Graph Analysis of Second-Order State-Variable Band-Pass Filter

$$T(p) = \frac{(2K_1'/R_{in})(p + \alpha_2)}{p^2 + (\alpha_1 + \alpha_2)p + \left(\alpha_1\alpha_2 + \dfrac{4\ b_2\ K_1'K_2'}{R_1}\right)} \qquad (5.4)$$

where

$$\alpha_1 = \gamma - 2b_1\ K_1'$$

$$\alpha_2 = \gamma - 2\rho\ K_2'$$

$$K' = K_h \cdot K \cdot K_s$$

Furthermore, by relating Eq. (5.4) to band-pass filter parameters, one obtains

$$\omega_o = \sqrt{\alpha_1\alpha_2 + \frac{4b_2\ K_1'\ K_2'}{R_1}} \qquad (5.5)$$

$$Q = \frac{\sqrt{\alpha_1\alpha_2 + \dfrac{4b_1K_1'K_2'}{R_1}}}{\alpha_1 + \alpha_2} \qquad (5.6)$$

$$|T(j\omega_o)| = \frac{2K_1'\ \sqrt{\omega_o^2 + \alpha_2^2}}{R_{in}\ (\alpha_1 + \alpha_2)\ \omega_o} \qquad (5.7)$$

For a true band-pass filter, α_2 must be zero. Then, Equations (5.4) through (5.7) are reduced to

$$T(p) = \frac{(2K_1'/R_{in})p}{p^2 + \alpha_1 \, p + \frac{4b_2 \, K_1'K_2'}{R_1}} \quad ; \tag{5.8}$$

$$\omega_o = \sqrt{(4b_2K_1'K_2')/R_1} \quad , \tag{5.9}$$

$$Q = \frac{\sqrt{(4b_2K_1'K_2')/R_1}}{\alpha_1} \quad , \tag{5.10}$$

$$|T(j\omega_o)| = \frac{2K_1'}{\alpha_1 \, R_{in}} \quad . \tag{5.11}$$

When $\alpha_2 = 0$,

$$\rho = \frac{\gamma}{2K_2'} \quad . \tag{5.12}$$

In practice, the condition in Eq. (5.12) is not possible because when α_2 is close to zero, the system approaches instability and becomes extremely sensitive to noise. However, for first-order approximations, the condition is assumed. In addition, a sensitivity analysis is performed for use in design. The design criteria, which are described later, are based on an arbitrarily prescribed sensitivity of band-pass filter parameters with respect to the feedback coefficients.

The sensitivity analysis was performed based on the definition

$$S_K^T = \frac{K}{T}\frac{\partial T}{\partial K} \tag{5.13}$$

where T is the filter parameter and K is the varying filter element. For $\alpha_2 = 0$, the sensitivity of ω_o and Q with respect to feedback coefficients are summarized in Table 5.1.

Design Criteria

The objective of defining design criteria is to relate the band-pass filter parameters to the physical size of the ETC chip. That is, with prescribed sensitivity requirements, one can choose an ETC chip size so that the desired ETC band-pass filter performance is obtained.

From Table 5.1, $S_{b_1}^{Q}$ is the only sensitivity term that relates physical size of the ETC to the band-pass filter parameters ω_o and Q. Let

$$S_{b_1}^{Q} = q\ Q \tag{5.14}$$

where q is a prescribed sensitivity factor. For low sensitivity q is a number less than unity. Substituting Eq. (5.14) in $S_{b_1}^{Q}$ in Table 5.1, one obtains

$$\gamma = \omega_o(q + 1/Q) \tag{5.15}$$

From Equations (5.2) and (2.6), Eq. (5.15) becomes

$$L_x = \sqrt{\frac{\pi^2\ k_s}{\rho_s C_s\ (q + \frac{1}{Q})\ \omega_o}} \tag{5.16}$$

Hence, for a given q, ω_o and Q, L_x can be calculated. Plots of L_x as a function of ω_o for a Q of 10 are shown in Fig. 5.7 with q as a

Table 5.1 Sensitivity of the Band-Pass Filter Parameters with Respect to Feedback Coefficients ($\alpha_2 = 0$)

$$S_{\rho}^{\omega_o} = 0$$

$$S_{b_1}^{\omega_o} = 0$$

$$S_{b_2}^{\omega_o} = 1/2$$

$$S_{\rho}^{Q} = 0$$

$$S_{b_1}^{Q} = (\gamma Q/\omega_o - 1)$$

$$S_{b_2}^{Q} = 1/2$$

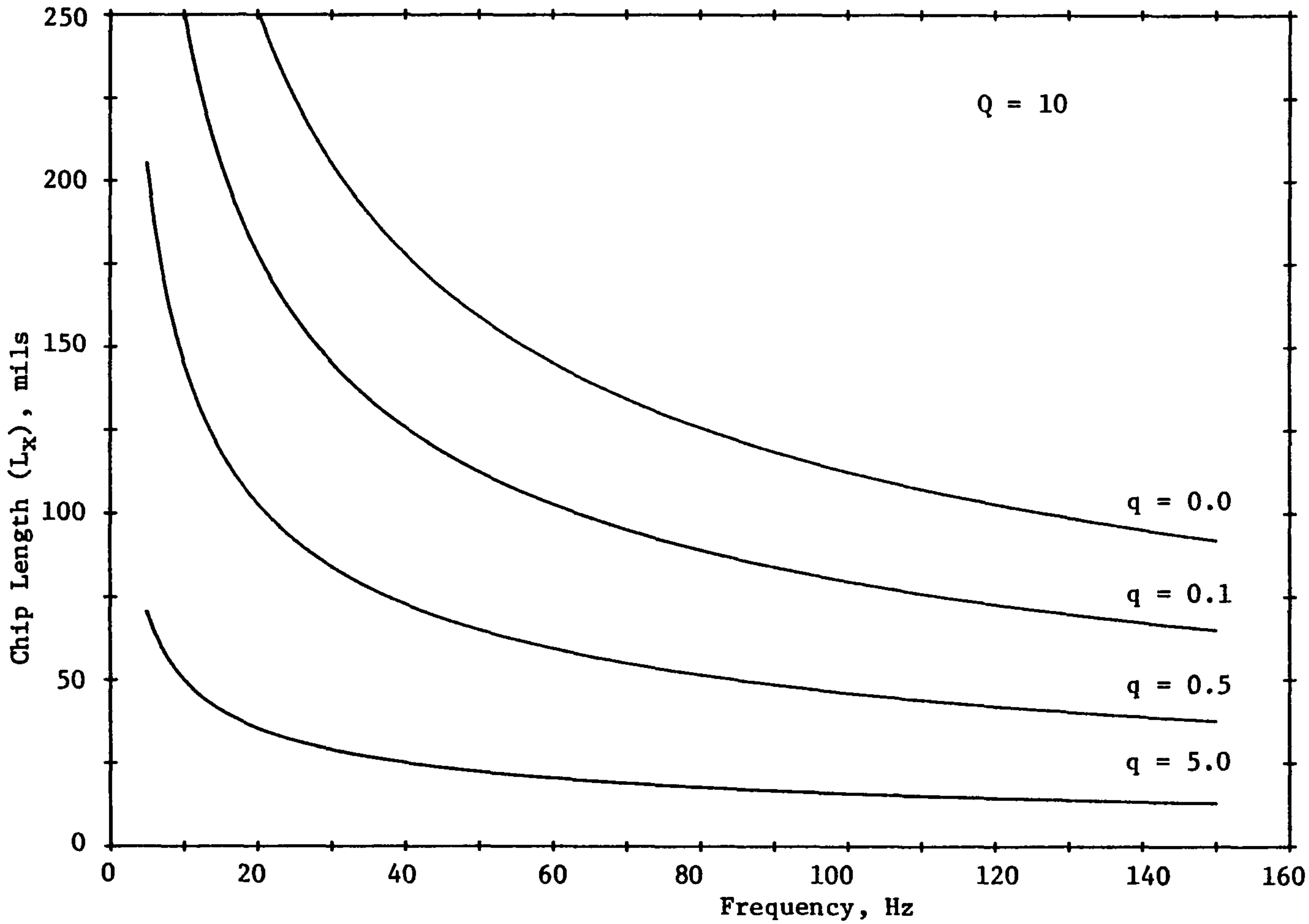


Fig. 5.7 The Relations Between the Chip Length and the Desired Center Frequencies at Q of 10

parameter. If the chip is made longer than the L_x obtained from Fig. 5.7, the sensitivity will be improved, except for the case $q = 0$. Contrarily, when the chip length is shorter than L_x, the sensitivity performance of the filter will be worse. For example, for $q = 0.5$, $Q = 10$, $\omega_o = 2\pi$ (60) rps, recommended L_x is 59.27 mils. Then, it is reasonable to choose the chip size to have L_x equal to 60 mils. For a prototype chip, $L_x = 60$ mils and $L_y = 20$ mils are used for an ETC band-pass filter at $\omega_o = 120\pi$ rps, with Q of 10 having $S_{b_1}^{Q} = 5$.

Two Independent ETC Structures on One Chip, and Its Fabrication

ETC Structure

Only one ETC channel (Fig. 5.5) has been discussed in previous sections. To obtain a complete monolithic ETC band-pass filter system, two independent ETC channels on one chip is the most important requirement. The previous attempts to accomplish this goal were unsuccessful as stated in Chapter 4. However, the results have indicated that the orthogonal arrangement alone will not be enough to isolate the two channels. This indicates that means must be found to thermally isolate the two channels. The most fundamental way of doing that is to physically cut the thermal path between the two channels. To implement this idea, one must modify the IC fabrication process.

For the present, let us assume that no matter what must be done to thermally isolate the ETC channels, it can be accomplished. By keeping the orthogonal structure, the previously proposed ETC structures are as shown in Appendix B. It is later demonstrated that the orthogonal configuration is not necessary when the channels are physically isolated. To have two ETC channels on one chip, a bridge between the channels is necessary.

From the above discussion, two ETC structures are proposed, the parallel ETC structures 1 and 2, as shown in Figures 5.8 and 5.9. Note that both structures have two parallel channels. Actually, the channels can have any orientation as long as they are constructed to have minimum thermal interactions. Because of the differential heater arrangement, the bridge at the middle of the channels has very small temperature variations for steady state operation. It also serves as a mechanical support.

These ETC structures impose a minor problem; that is the thermal cross-coupling between the channels. The cross-coupling magnitude depends on the operating frequencies and distance "S" separating the channels. From an analytic calculation [Louw, 1975, Chapter 6], for channel spacing of 10 mils at steady-state frequency of 24 Hz, the thermal cross-coupling is less than -60 dB. For frequencies higher than 24 Hz, the cross-coupling is substantially less than -60 dB. However, the cross-coupling is about -30 dB for a frequency of 1.6 Hz.

The above discussions have established necessary conditions and dimensions for an ETC structure layout. We now turn to the fabrication of the device.

The Device Fabrication

The fabrication of the device was designed so that the finished ETC chip would have two independent thin rectangular channels. To

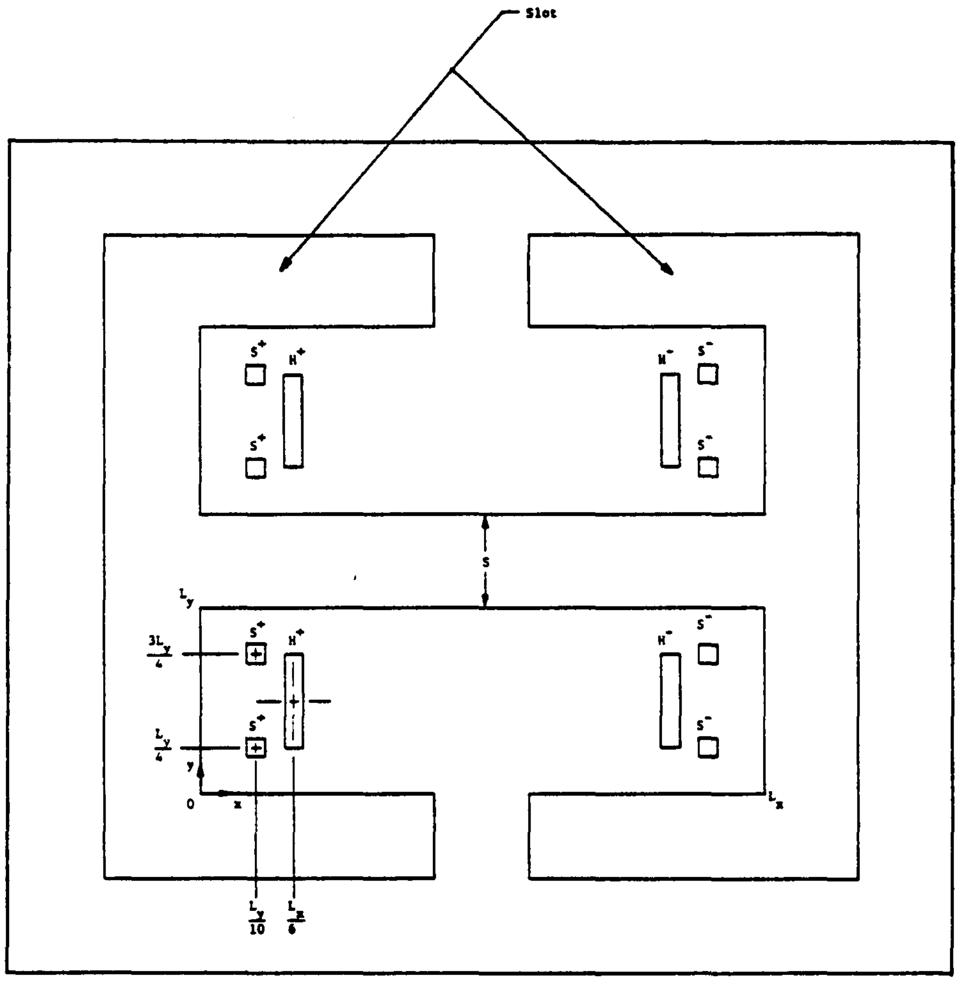


Fig. 5.8 Parallel ETC Structure 1

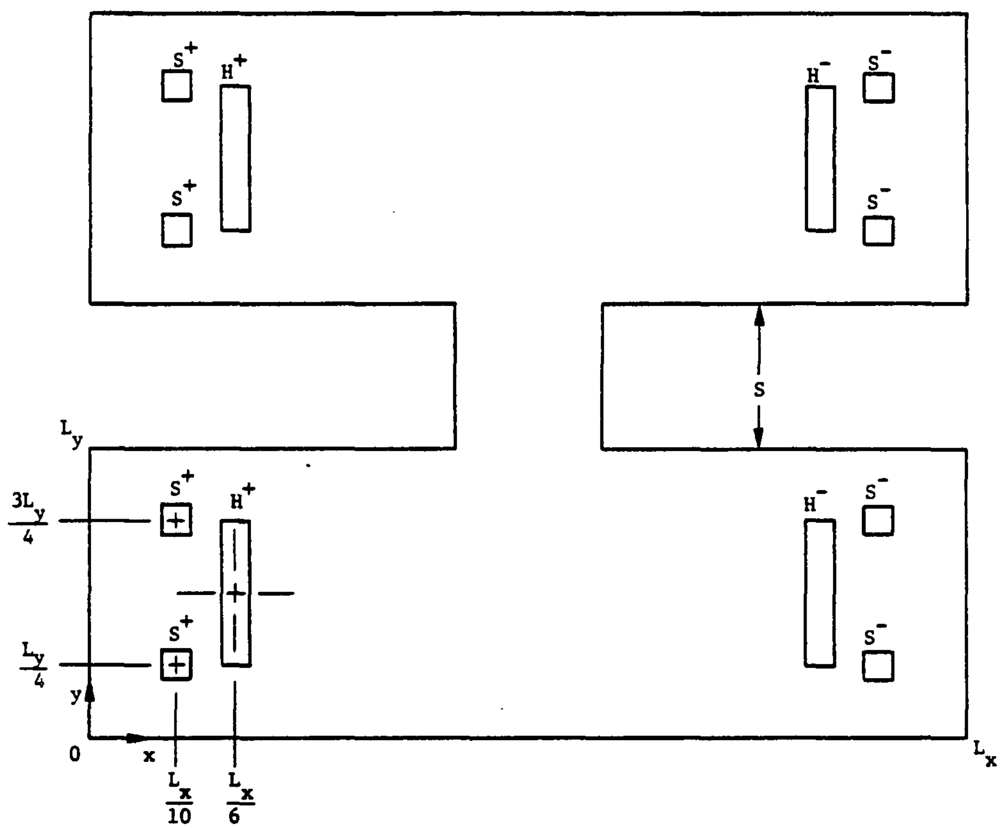


Fig. 5.9 Parallel ETC Structure 2

fabricate the ETC structures shown in Figures 5.8 and 5.9, one has to groove cut the chip. Furthermore, the starting silicon wafers are normally of the order of 10 mils thick. To obtain a thinner chip, one must thin the wafer; this must be done as the last step of the process so that the wafer does not break during processing.

The groove etch and thin etch are incorporated with the standard IC processing. There is also a groove mask added to the processing masks. The entire fabrication process employed standard diffusion processes, ion implantation, Chemical Vapor Deposition (CVD), and chemical etching. The major processing steps are outlined as follows:

1. Isolation diffusion (if applicable)
2. Base diffusion
3. Emitter diffusion
4. Open contact windows
5. Groove etch
6. Metalization
7. Thin etch

Figure 5.10 depicts the cross-section A-A' of the ETC chip at Steps 4, 5, 6 and 7. The processing details are described in Appendix C. Note that the dimensions in Fig. 5.10 are not scaled, and the transistor locations are for demonstration purposes only.

Because of photolithography limitations in the Solid State Engineering Laboratory, chips larger than 80 x 80 mils are not easily fabricated. Therefore, the structure of Fig. 5.9 was chosen, in which the dimensions are L_x = 60 mils, L_y = 20 mils, and channel spacing is

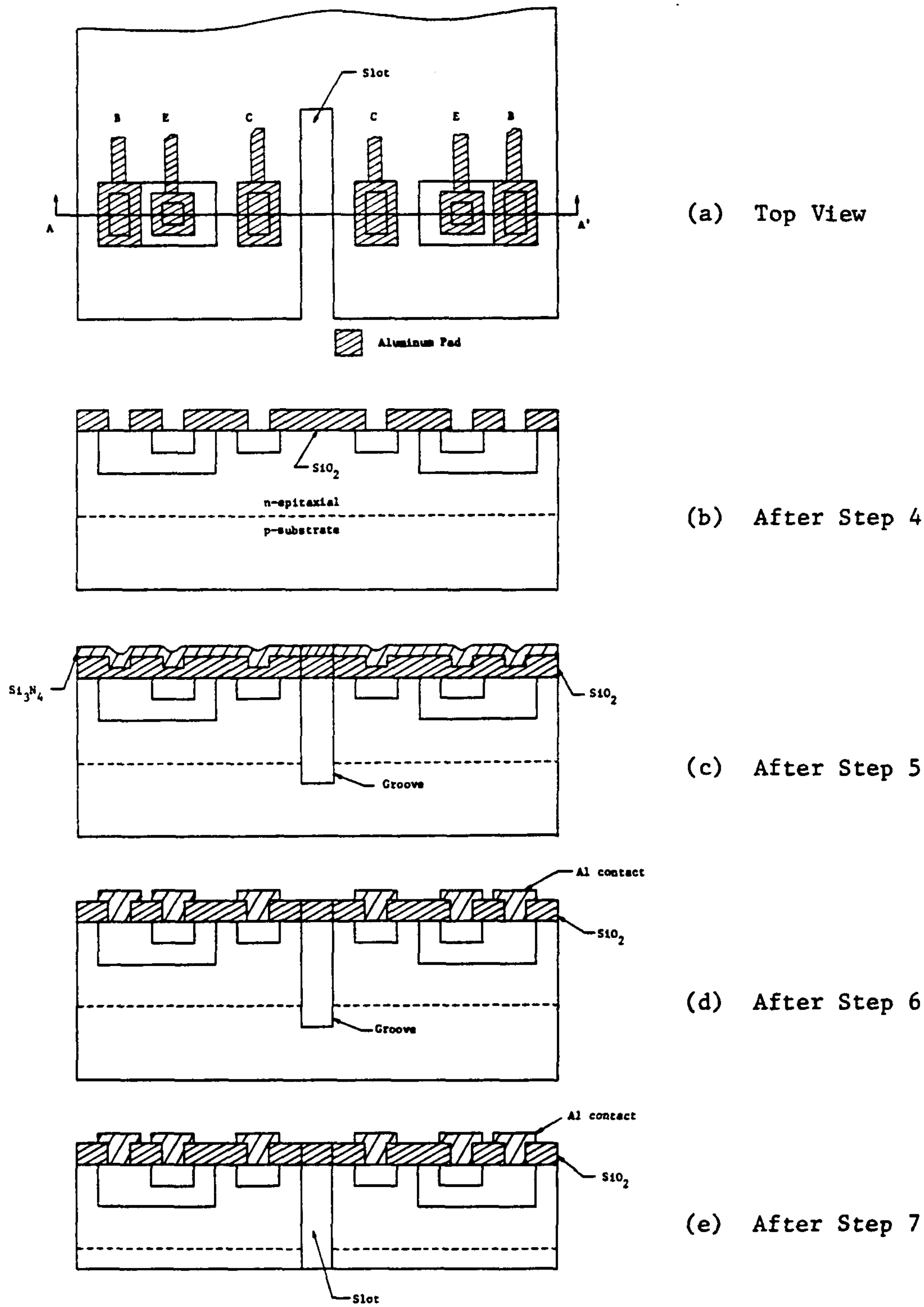


Fig. 5.10 Cross-Section A-A' of Each Processing Step from Step 4 through Step 7

10 mils. The chip thickness (groove depth) is designed to be between 2 to 2.5 mils. The fabricated ETC chip is shown in Fig. 5.11. The measured average chip thickness is approximately 2 mils and each channel of the chip is 60x20 mils. The chip is mounted on 100x100x10 mils Dupont Kapton H-film insulator. Commercially known, 5-minute epoxy is used as the adhesive between the chip and the insulator, and between the insulator to the isothermal mounting surface.

Experimental Results of the Two-Channel ETC and Its Band-Pass Filter

The ETC chip in Fig. 5.11 was tested; open-loop and closed-loop frequency response, and the thermal interaction of the channel were measured. In the experiment, heater and sensor circuits, and coefficient setting circuit of Figures 3.2, 3.5, 3.6 and 3.7, respectively, were used.

From the experiment, the isolation between the channels is approximately 55 dB. This is about two orders of magnitude better than that obtained in Chapter 4. The measured open-loop frequency response is shown in Fig. 5.12 together with the results of the computer analysis. The cutoff frequency is about 25 Hz, and 0 dB is equivalent to 0.434 °C/mW.

For the closed-loop frequency response (ETC integrator) measurements, the feedback coefficient was calculated from Eq. (5.12), and the schematic in Fig. 5.13 was used. However, due to the instability of the system with positive feedback; it was necessary to reduce the feedback coefficient to 90 percent of its calculated value. That is, in the experiment, ρ = 0.0293 mA/V which is equivalent to 1.89 mW/°C.

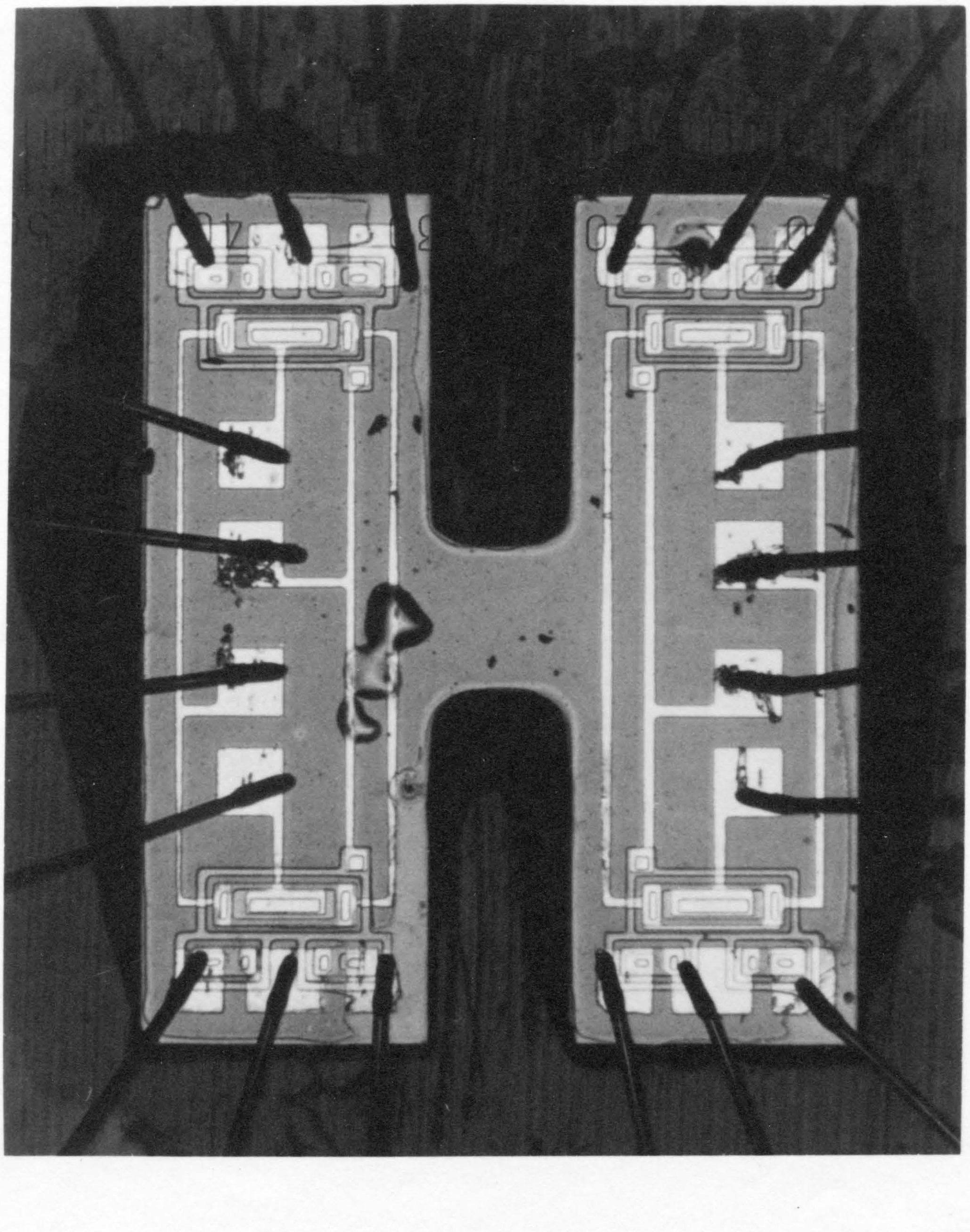


Fig. 5.11 Photomicrograph of Parallel ETC Structure 2
(X80 magnification)

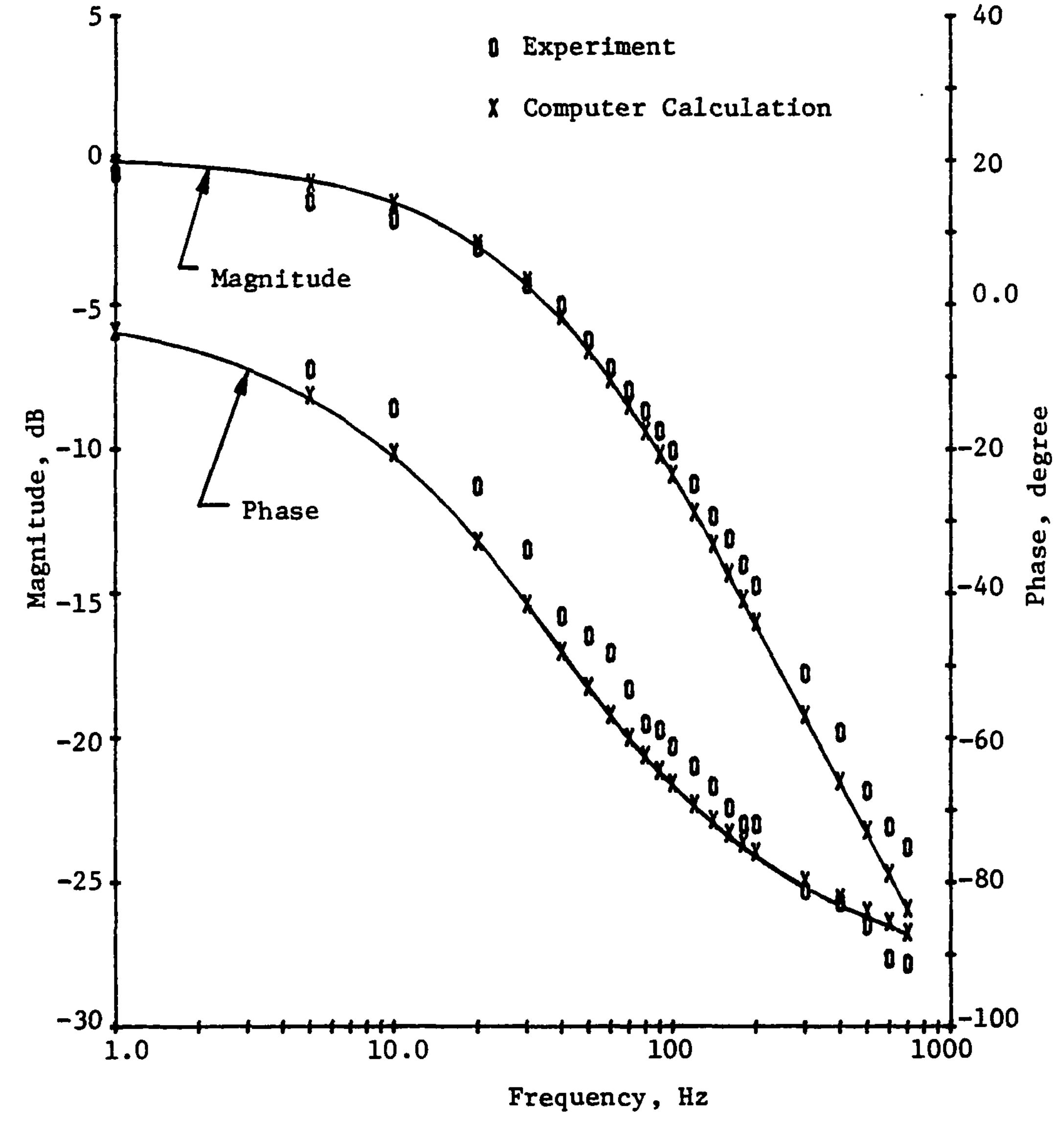


Fig. 5.12 Measured and Calculated Open-Loop Frequency Response of Two-Channel ETC

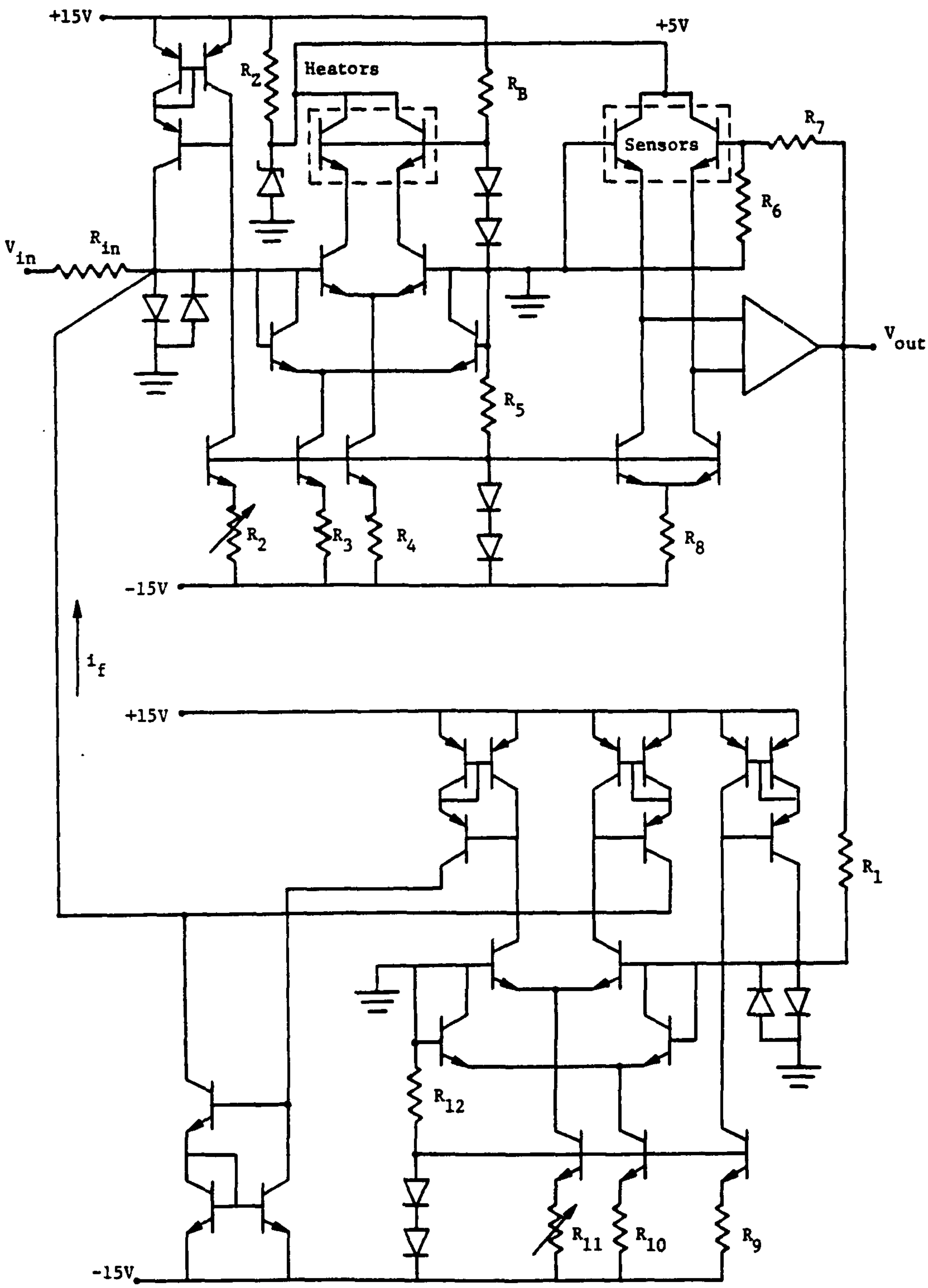


Fig. 5.13 The ETC Integrator Circuit

The measured closed-loop response is shown in Fig. 5.14; 0 dB is 2.417 °C/mW. Note that the element values of Fig. 5.13 are given in Appendix D.

In feedback coefficient calculations, there is some difficulty in determining the correct values of thermal conductivity and capacity. These are functions of temperature and doping level. It is necessary to have accurate values of thermal conductivity and capacity because they determine K and γ. From Equations (5.9) and (5.10), one obtains

$$b_2 = \frac{\omega_o^2 R_1}{4K_1' K_2'} \tag{5.17}$$

$$b_1 = \frac{(\gamma - \omega_o/Q)}{2K_1'} \quad . \tag{5.18}$$

Therefore, the accuracies of b_1, b_2 and ρ depend on the correct values of K_1, K_2 and γ.

Because of unavailable data of thermal conductivity and capacity for low resistivity material, the published data for higher resistivity materials are used. This is a good first-order approximation because both thermal conductivity and capacity are insensitive to doping level at temperatures in the vicinity of 300°K and higher [Sze, 1969]. From experimental data reported by Morris and Hurst [1961], and Shanks, Maycock, Sidles and Danielson [1963], the temperature dependence of thermal conductivity and capacity can be approximated as

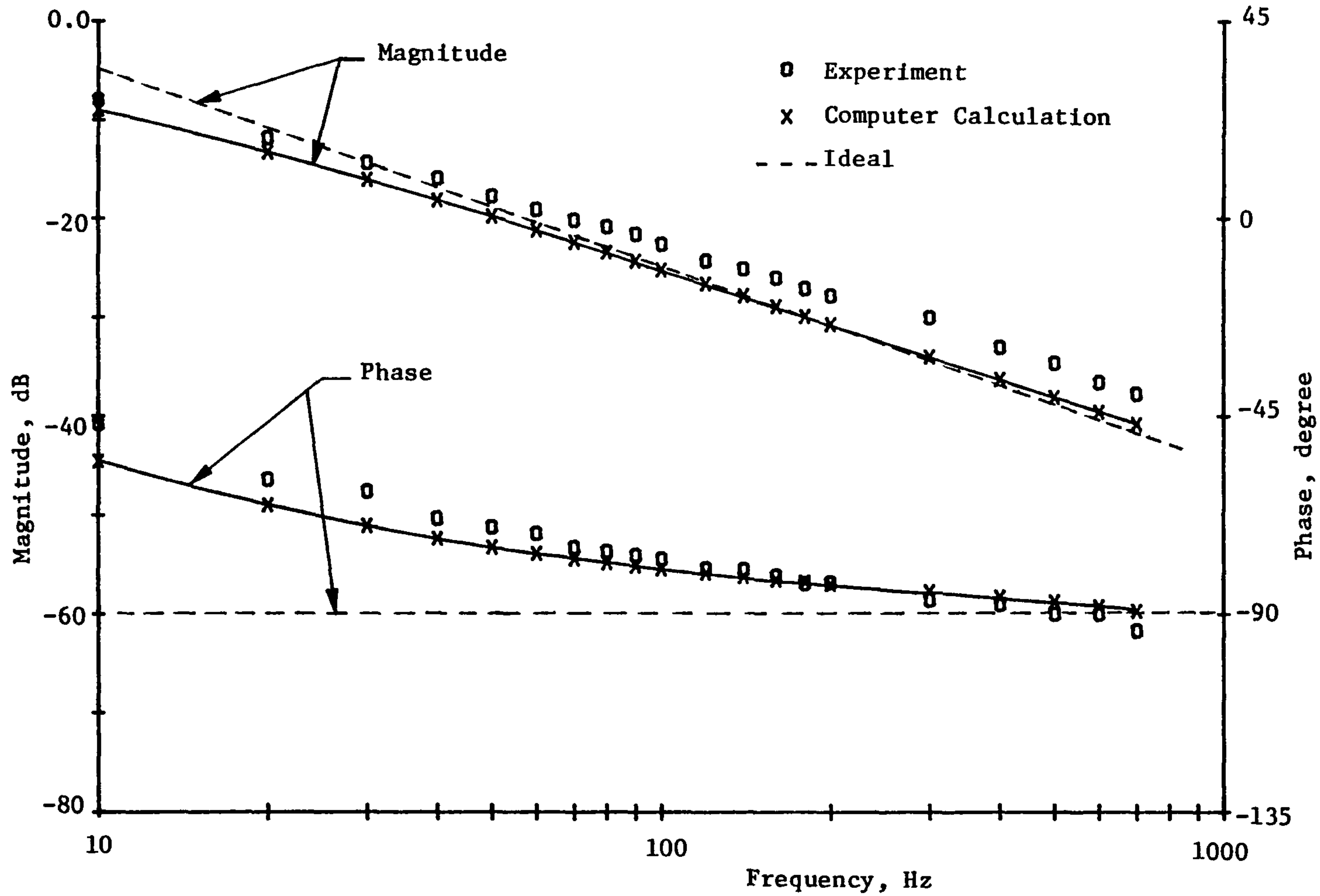


Fig. 5.14 Measured and Calculated Integrator Frequency Response of ETC

$$k_s = \frac{1087}{T} - 0.39 \qquad mW/mil - {}^\circ C \tag{5.19}$$

and

$$\rho_s c_s = (2.076 \times 10^{-8})T + 2.164 \times 10^{-5} \ \frac{mW - sec}{mil^3 - {}^\circ C} \tag{5.20}$$

where T is in degrees Kelvin. The Equations (5.19) and (5.20) are the results of the interpolation of published data at temperatures from 273°K to 500°K.

From Equations (5.2), (5.4), (5.12), (5.17) and (5.18), and Chapter 3, the calculated and measured conversion constants and feedback coefficients are summarized in Table 5.2. The detailed calculations are given in Appendix D. By using the circuits in Chapter 3 and setting the feedback coefficients at values given in Table 5.2, the experimental results of band-pass filters at center frequency of 60 Hz with Q's of 5 and 10 are obtained; these are shown in Figures 5.15 and 5.16. Note each heater had a bias power of 10 mW and the chip temperature was estimated to be approximately 45°C. The full schematic of the ETC band-pass filter is given in Appendix D.

Discussion and Conclusions

New geometrical configurations for heater and sensor locations have been derived which produce an ETC transfer function having approximately single-pole behavior. A thin rectangular chip was found to have higher DC gain than that obtained by Louw [1975]. A prototype chip

Table 5.2 Measured Value of Conversion Factors and Feedback Coefficients of the Second-Order Band-Pass Filters*

	Values	Unit
Conversion Factors:		
K_1	88.38	°C/mW-sec
K_2	81.08	°C/mW-sec
K_{h_1}	27.14	mW/mA
K_{h_2}	27.69	mW/mA
K_{s_1}	1.12	V/°C
K_{s_2}	1.10	V/°C
Feedback Coefficients:		
b_1 (Q = 5)	0.041	mA/V
b_1 (Q = 10)	0.048	mA/V
b_2	0.154	mA/V
ρ	0.073	mA/V

*See Appendix D.

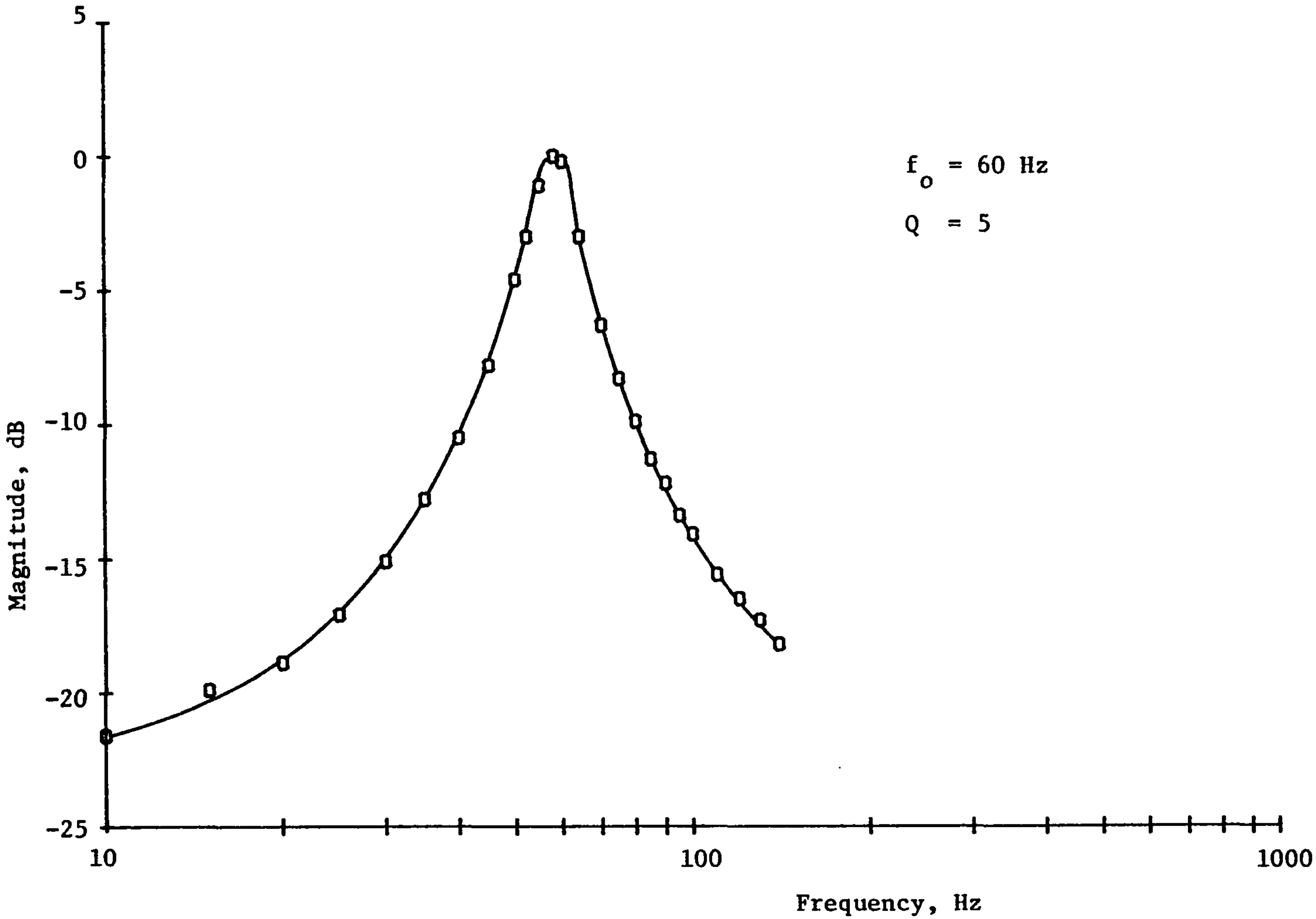


Fig. 5.15 Measured ETC Band-Pass Filter (f_o = 60 Hz, Q = 5)

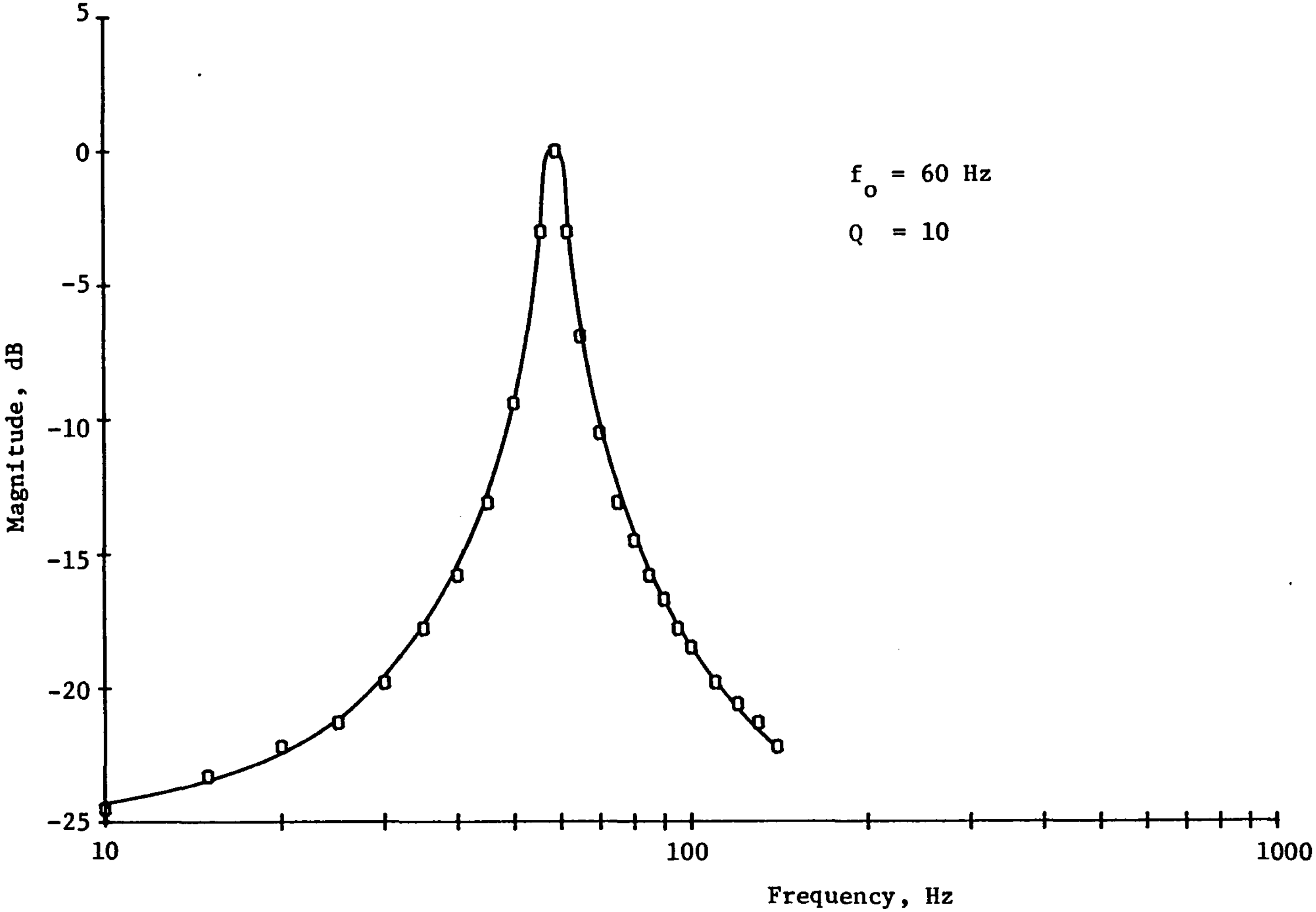


Fig. 5.16 Measured ETC Band-Pass Filter (f_o = 60 Hz, Q = 10)

having two thin independent rectangular ETC channels was fabricated with average chip dimensions of 60 x 20 x 2 mils per channel. The measured open-loop and closed-loop transfer functions agreed closely with the calculations. The isolation between the channels was measured to be approximately 55 dB. Finally, second-order state-variable band-pass filters were implemented using the ETC chip. The experimental results also agreed closely with the calculations; that is for center frequency of 60 Hz at Q's of 5 and 10, the measured center frequency and Q's agreed within 3 percent of the calculations.

One problem needs further investigation; that is the temperature dependence of thermal conductivity and capacity of silicon. If the filter is in an uncontrolled-temperature environment, means of temperature compensation must be provided in order to minimize changes of the filter performance with ambient temperature. The temperature compensation can be provided in several external circuits such as the heater, sensor, or coefficient-setting circuits or combinations thereof.

The experimental results obtained in this chapter have successfully demonstrated the feasibility of the design and analysis of two independent ETC integrators on one chip. They have also indicated successful applications of the circuits given in Chapter 3. From Fig. D.1, one can see that the necessary external circuits used in implementing the second-order band-pass filter are suitable for integration by a standard bipolar linear process. Therefore, the results obtained in this chapter represent a major step toward the realization of a fully integrated ETC filter on one chip.

CHAPTER 6

CONCLUSIONS

Summary

The objectives of this dissertation stated in Chapter 1 were achieved. First, ETC systems were designed using the two-dimensional analysis and thermal transfer functions of Gray [1969], and by pole-zero cancellation techniques [Louw, 1975]. Then, ETC integrators were designed by means of positive electrical feedback using the ETC systems. Electronic heater and sensor circuits were developed to be incorporated into the required ETC filter systems in such a way that they can be integrated. State-variable synthesis techniques were used to design two ETC filter systems: a two-chip ETC filter, and one-chip ETC filter systems. ETC chips were then fabricated and tested which yielded the following results.

Band-pass filters having center frequencies at 10, 50, and 100 Hz with $Q \approx 10$ were obtained from two-chip ETC filter systems. Because of ambient temperature sensitivity, these filters were not stable in a varying ambient temperature environment. Although two orthogonal ETC channels can be obtained from this particular configuration, two ETC integrators on one chip cannot be obtained because of interactions between the two channels. The amount of interaction between the two channels was measured and found to be approximately -20 dB; with this level of interaction, adequate isolation between the two channels cannot be obtained.

One-chip ETC systems were used in designing band-pass filters. At a center frequency of 60 Hz, band-pass filters with Q's of 5 and 10 were obtained. The experimental results agree within 3 percent of the theoretical predictions. The ETC chip, with each channel 20x60x2 mils, can also be designed for different frequencies, ranging from 10 Hz to 500 Hz. However, the sensitivity $S_{b_1}^{Q}$ will also vary, being higher at lower frequencies. Differences between experimental and calculated results are caused by two major factors. The first factor results from nonuniformity of the chip thickness, and from problems with the uniformity, the properties of the insulator, and the adhesive between the chip and the insulator. Second, the temperature dependences of thermal conductivity and specific heat of silicon cause variations of the amount of positive and negative feedback of the filter systems as the ambient temperature changes.

The results obtained in this dissertation demonstrate that it is possible to reduce to one the number of chips required for a second-order filter. It remains only to integrate on this same chip all of the auxiliary electronic circuits. This is possible by modifying the structure in Fig. 5.9 as proposed in Fig. 6.1. The two channels are the same as before, but the channels are farther separated. Then not only all of the auxiliary electronic circuits can be fabricated in the middle area, the structure also enhances the isolation of the channels. With

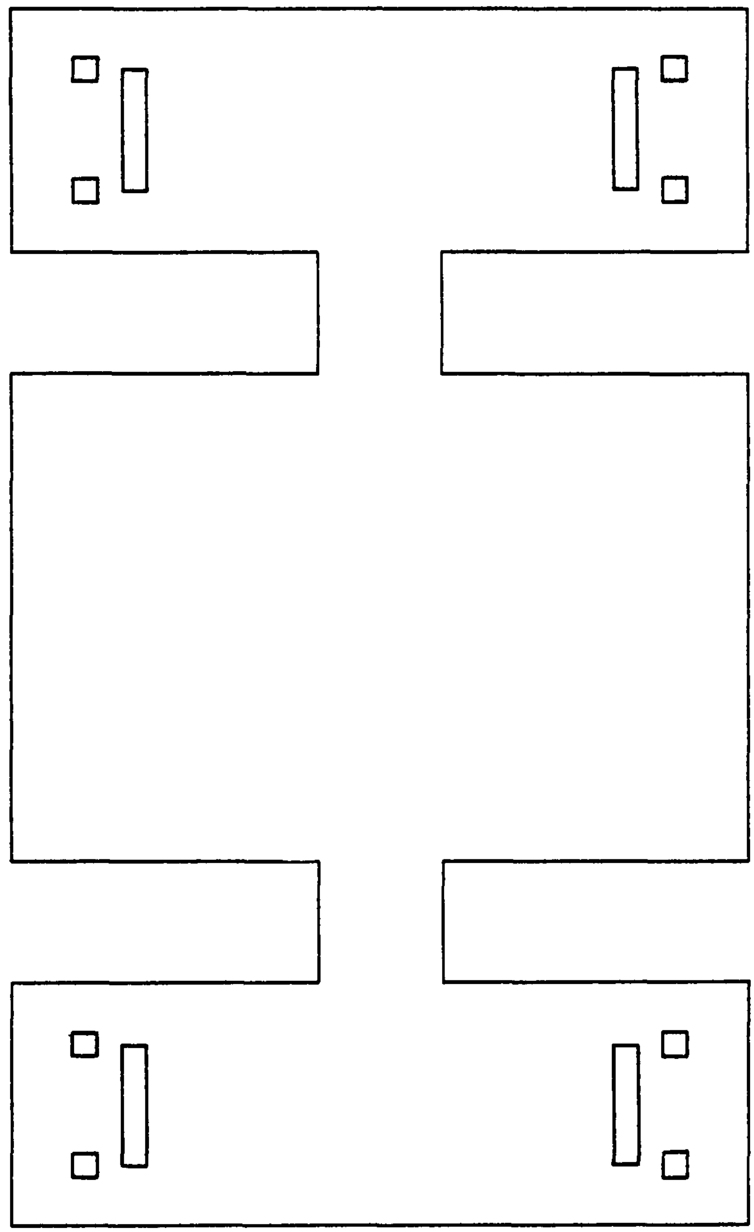


Fig. 6.1 The Proposed Structure

this proposed structure, it should be possible to fabricate a monolithic ETC second-order filter with no external components. In addition, if the structure in Fig. 6.1 is modified by adding two more parallel channels to the left and right sides of the middle area, it should also be possible to fabricate a monolithic ETC fourth-order filter provided the middle area does not exceed the fabrication limits to accommodate all of the auxiliary electronic circuits.

Original Contributions of the Dissertation

The original contributions of this dissertation can be summarized as follows:

1. A new heater circuit was developed for single heater ETC use.
2. The differential sensor circuit was modified to have low noise performance.
3. A new differential sensor circuit was developed to accommodate common collector sensor transitors.
4. A new coefficient-setting circuit and technique were developed suitable for integration.
5. An active URC integrator was obtained by means of positive electrical feedback.
6. An ETC structure analogous to the URC structure with capacitor grounded was designed and fabricated.
7. An active ETC integrator was obtained by means of positive electrical feedback.

8. A new and more practical ETC configuration for an approximately single-pole system was developed. This configuration permits a reduction of the heater size required.
9. Orthogonal and parallel thermally isolated ETC structures were developed for two independent ETC integrators on one chip. One of the parallel structures was fabricated.
10. ETC filter design criteria were presented for prescribed sensitivity requirements.
11. Finally, modified etching techniques for grooving and separating silicon chips were developed. The techniques were used in order to improve the DC gain and to thermally isolate the two channels.

Recommendations for Future Work

Of the design approaches presented here, that of using two independent ETC channels is the most promising. Several improvements of the design and fabrication of two independent ETC channels on one chip are recommended for future work:

1. The proposed structure in Fig. 6.1 should be fabricated with all of the auxiliary electronic circuits included.
2. Since ETC channels can be in any configuration, the channels can be arranged so that more area on the chip can be used for ancillary circuits.
3. Should undercutting by the etch prove to be a problem, other means of groove etch can be used, such as V-groove etching in MOS technology, in which the groove depth is also better controlled.

4. As facilities at the Solid State Engineering Laboratory permit, smaller transistor geometries should be fabricated. This would permit narrower ETC channels to be obtained. Consequently, higher DC gain can be accomplished.
5. MOS versions of ETC's should be investigated.
6. Temperature compensation schemes must be incorporated to nullify the temperature dependence of the thermal parameters of silicon chips.

APPENDIX A

DIFFERENTIAL ETC ANALYSIS

This is the differential ETC analysis for finding proper heater and sensor locations for approximately single pole ETC configuration, as discussed in Chapter 5. For differential heaters and sensors, and from Eq. (2.11), one can write

$$F(p) = \frac{4}{ak_s A_S A_H}\left(\frac{L_x}{L_y}\right) \omega_x \sum_{n=o}^{\infty} \sum_{m=o}^{\infty} \frac{(H_{1nm} - H_{2nm})(S_{1nm} - S_{2nm})}{[\delta(n)+1][\delta(m) + 1][p + A_{\omega_x}]} \tag{A.1}$$

where

$$A = (n\pi)^2 + \left(m\pi \cdot \frac{L_x}{L_y}\right)^2 + \frac{k_i\ L_x^2}{k_s\ a\ b} \quad .$$

The analysis begins by using Equations (2.3) and (2.4), and defining the heater and sensor locations relative to the co-ordinates of the center of the areas and the size of the areas, with a symmetrical arrangement as shown in Fig. A.1. This leads to heater and sensor weighting factors

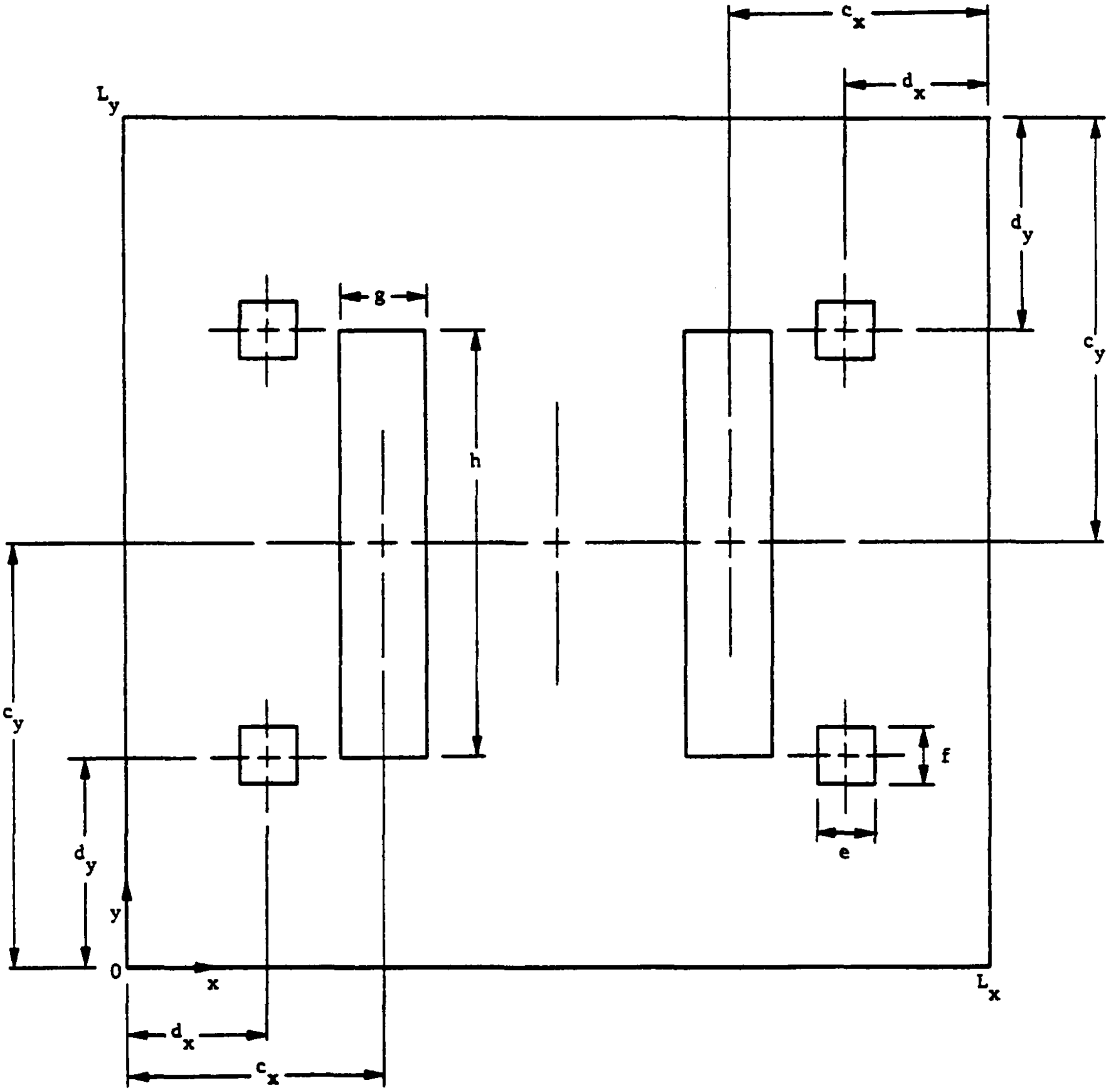


Fig. A.1 The ETC Configuration and Heater and Sensor Locations Used in the Analysis

$$
(H_{1nm}-H_{2nm}) = \begin{cases}
0 & n+m = \text{even} \\[2ex]
4h\left(\dfrac{L_x}{\pi}\right) \cos\left(\dfrac{n\pi}{L_x} c_x\right) \cdot \sin\left(\dfrac{n\pi}{2L_x} g\right) & , m = 0,\ n = \text{odd} \\[2ex]
4g\left(\dfrac{L_x}{m\pi}\right) \cos\left(\dfrac{m\pi}{L_y} c_y\right) \cdot \sin\left(\dfrac{m\pi}{2L_y} h\right) & , m = \text{odd},\ n = 0 \\[2ex]
8\, \dfrac{L_x L_y}{nm\pi^2} \cos\left(\dfrac{n\pi}{L_x} c_x\right) \cdot \sin\left(\dfrac{n\pi}{2L_x} g\right) \cdot \cos\left(\dfrac{m\pi}{L_y} c_y\right) \cdot \sin\left(\dfrac{m\pi}{2L_y} h\right) , & \\
 & n+m = \text{odd}
\end{cases}
\tag{A.2a}
$$

and

$$
(S_{1nm}-S_{2nm}) = \begin{cases}
0 & n+m = \text{even} \\[2ex]
4f\, \dfrac{L_x}{n\pi} \cos\left(\dfrac{n\pi}{L_x} d_x\right) \cdot \sin\left(\dfrac{n\pi}{2L_x} e\right), & m = 0,\ n = \text{odd} \\[2ex]
4e\, \dfrac{L_y}{m\pi} \cos\left(\dfrac{m\pi}{L_y} d_y\right) \cdot \sin\left(\dfrac{m}{2L_y} f\right), & m = \text{odd},\ n = 0 \\[2ex]
8\, \dfrac{L_x L_y}{nm\pi^2} \cos\left(\dfrac{n\pi}{L_x} d_x\right) \cdot \sin\left(\dfrac{n\pi}{2L_x} e\right) \cdot \cos\left(\dfrac{m\pi}{L_y} d_y\right) \cdot \sin\left(\dfrac{m\pi}{2L_y}\right) f , & \\
 & n+m = \text{odd}
\end{cases}
\tag{A.2b}
$$

where

d_x = center of sensor area from y-axis

d_y = center of sensor area from x-axis

c_x = center of heater area from y-axis

c_y = center of heater area from x-axis

$e \cdot f$ = sensor area (A_S)

$g \cdot h$ = heater area (A_H)

When one lets $c_y = L_y/2$, $d_y = L_y/4$, or, $3L_y/4$, and $h = L_y/2$, Eq. (A.1) becomes one-dimensional; that is

$$F(p) = \frac{4}{ak_s A_S A_H} \left(\frac{L_x}{L_y} \right) \omega_x \sum_{n=o}^{\infty} \frac{(H_{1n0}-H_{2n0})(S_{1n0}-S_{2n0})}{2(p + A\ \omega_x)} \qquad n = \text{odd},\ m = 0 \tag{A.3}$$

where

$$A = (n\pi)^2 + \frac{L_i L_x^2}{k_s ab}$$

For convenience, let

$$(H_{1n0} - H_{2n0})(S_{1n0} - S_{2n0}) = U_{n0} \tag{A.4}$$

Then the remaining residues are

$$\ldots \quad U_{10} \quad U_{30} \quad U_{50} \quad U_{70} \quad U_{90} \quad \ldots$$

For an approximately single-pole ETC, U_{10} must be preserved, while as many higher indexed ones as possible must be eliminated. By setting $c_x(d_x)$ at $L_x/10$, or, $3L_x/10$, and $d_x(c_x)$ at $L_x/6$, the residues at indices $n = 5, 15, 25, \ldots$, and $n = 3, 9, 15, \ldots$, are eliminated. Hence, the remaining residues are

$$\ldots \quad U_{10} \quad \ldots \quad U_{70} \quad \ldots \quad U_{11} \quad \ldots$$

The poles of these residues are $-\pi^2\omega_x$, $-49\pi^2\omega_x$, and $-121\pi^2\omega_x$, respectively. These poles are sufficiently well separated that $-\pi^2\omega_x$ is considered the dominant pole.

Therefore, when

$$c_y = h = L_y/2 \quad ,$$

$$d_y = L_y/4 \quad ,$$

$$c_x(d_x) = L_x/10, \text{ or, } 3L_x/10$$

and

$$d_x(c_x) = L_x/6 \quad ,$$

then Eq. (A.3) is approximately

$$F(p) \approx \frac{2\omega_x}{ak_s A_S A_H} \left(\frac{L_x}{L_y}\right) \frac{U_{10}}{p + \left(\pi^2 + \frac{k_i}{k_s} \cdot \frac{L_x^2}{ab}\right)\omega_x} \tag{A.5}$$

The heater and sensor locations are shown in Figures 5.3 and 5.4.

As discussed in Chapter 5, $d_x = L_x/10$, or, $3L_x/10$, and $c_x = L_x/6$ are chosen for a prototype. If Equations (A.2a) and (A.2b) and c_x are substituted in Eq. (A.4), U_{10} becomes (d_x is not substituted)

$$U_{10} = 16hf\left(\frac{L_x}{\pi}\right)^2 \cdot \cos\left(\frac{\pi}{6}\right) \cdot \cos\left(\frac{\pi}{L_x} d_x\right) \cdot \sin\left(\frac{\pi}{2L_x} g\right) \cdot \sin\left(\frac{\pi}{2L_x} e\right) \tag{A.6}$$

In most cases, g, e << L_x. Therefore,

$$U_{10} \approx 4\ A_H A_S \cdot \cos\left(\frac{\pi}{6}\right) \cdot \cos\left(\frac{\pi}{L_x} d_x\right) \tag{A.7}$$

Substituting U_{10} in Eq. (A.5), one obtains

$$F(p) \approx \frac{8\ \omega_x}{a\ k_s}\left(\frac{L_x}{L_y}\right) \frac{\cos\left(\frac{\pi}{6}\right) \cdot \cos\left(\frac{\pi}{L_x} d_x\right)}{p + \left(\pi^2 + \frac{k_i}{k_s}\frac{L_x^2}{ab}\right)\omega_x} \tag{A.8}$$

For a reasonable approximation, let $\frac{k_i}{k_s} \cdot \frac{L_x^2}{ab} << \pi^2$. Then Eq. (A.8) can be rewritten as (d_x is substituted)

$$F(p) \approx \frac{K}{p + \gamma} \tag{A.9}$$

where

$$K = \frac{8\omega_x}{k_s}\left(\frac{L_x}{aL_y}\right)\cos\frac{\pi}{6} \cdot \cos\frac{\pi}{10} \qquad \text{(for } d_x = L_x/10\text{)},$$

or,

$$\frac{8\omega_x}{k_s}\left(\frac{L_x}{aL_y}\right)\cos\frac{\pi}{6}\cdot\cos\frac{3\pi}{10} \qquad (\text{for } d_x = 3L_x/10),$$

$$\gamma = \pi^2\omega_x \quad .$$

For $d_x = L_x/10$,

$$\frac{K}{\gamma} = \frac{8\cdot\cos\frac{\pi}{6}\cdot\cos\frac{\pi}{10}}{k_s\ \pi^2}\left(\frac{L_x}{aL_y}\right) \quad . \tag{A.10}$$

APPENDIX B

EVOLUTION OF THE ORTHOGONAL ETC STRUCTURES

For the completeness of presentation of the ETC structures, the thermally isolated orthogonal ETC structures are shown in Figures B.1, B.2, and B.3. However, analytical solutions for these structures are not available; such analytical solutions were not developed because the structures of Figures 5.8 and 5.9 appear to be more practical. For the purpose of illustration, each channel has the same heater and sensor locations as shown in Fig. 5.5.

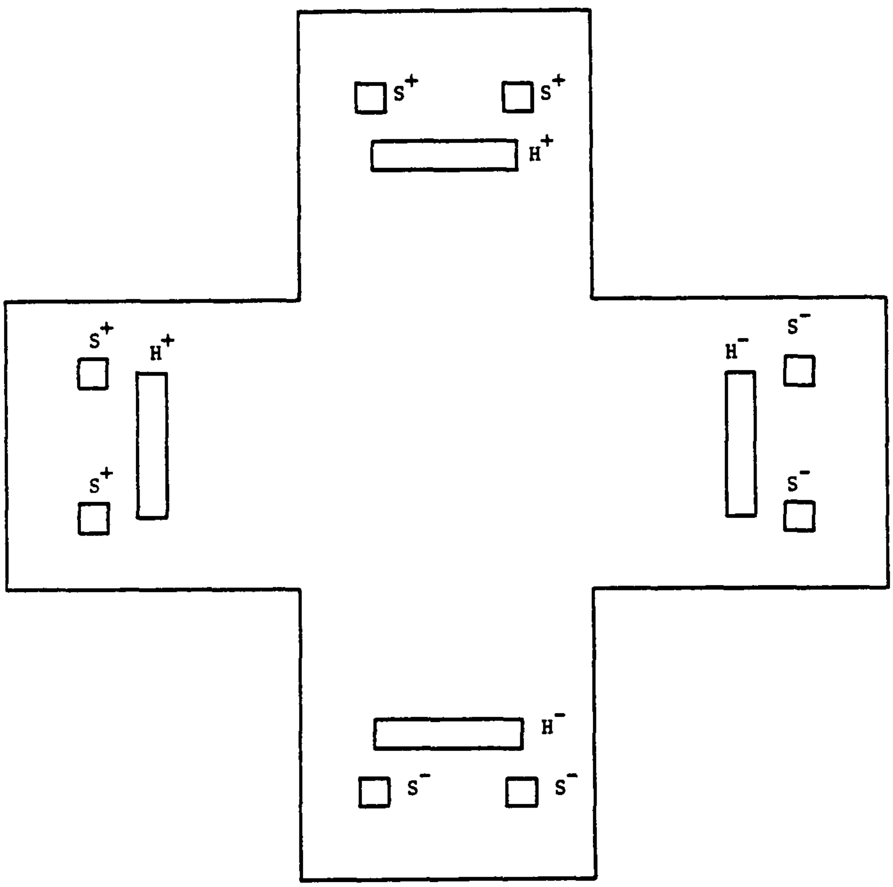


Fig. B.1 ETC Orthogonal Structure 1

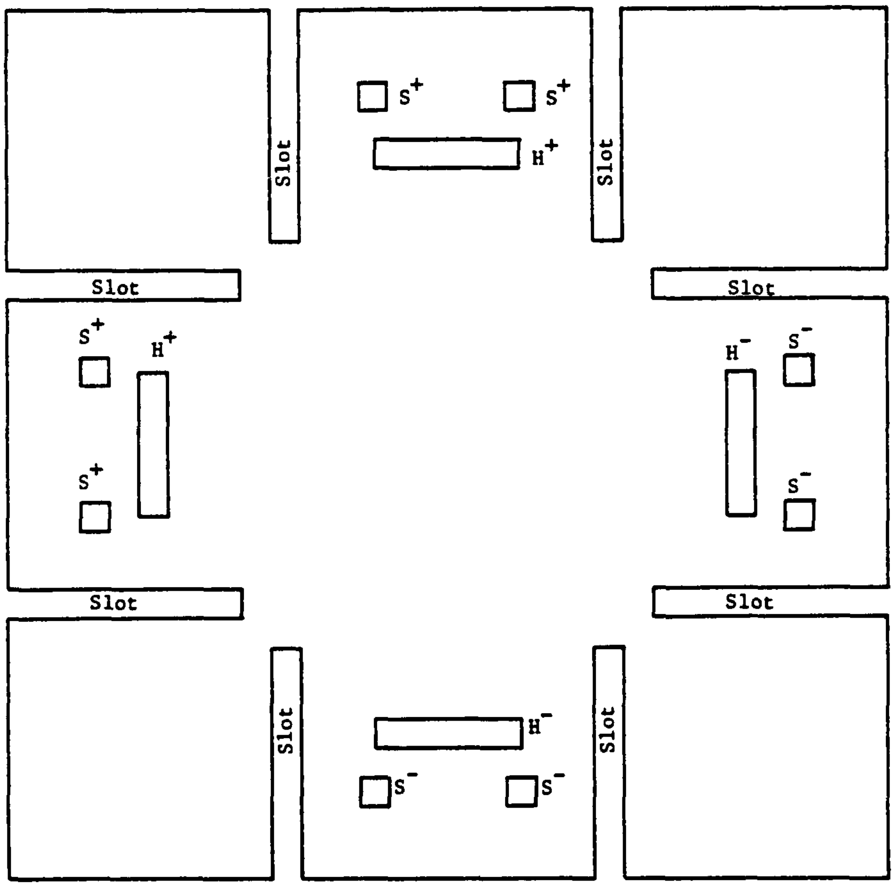


Fig. B.2 ETC Orthogonal Structure 2

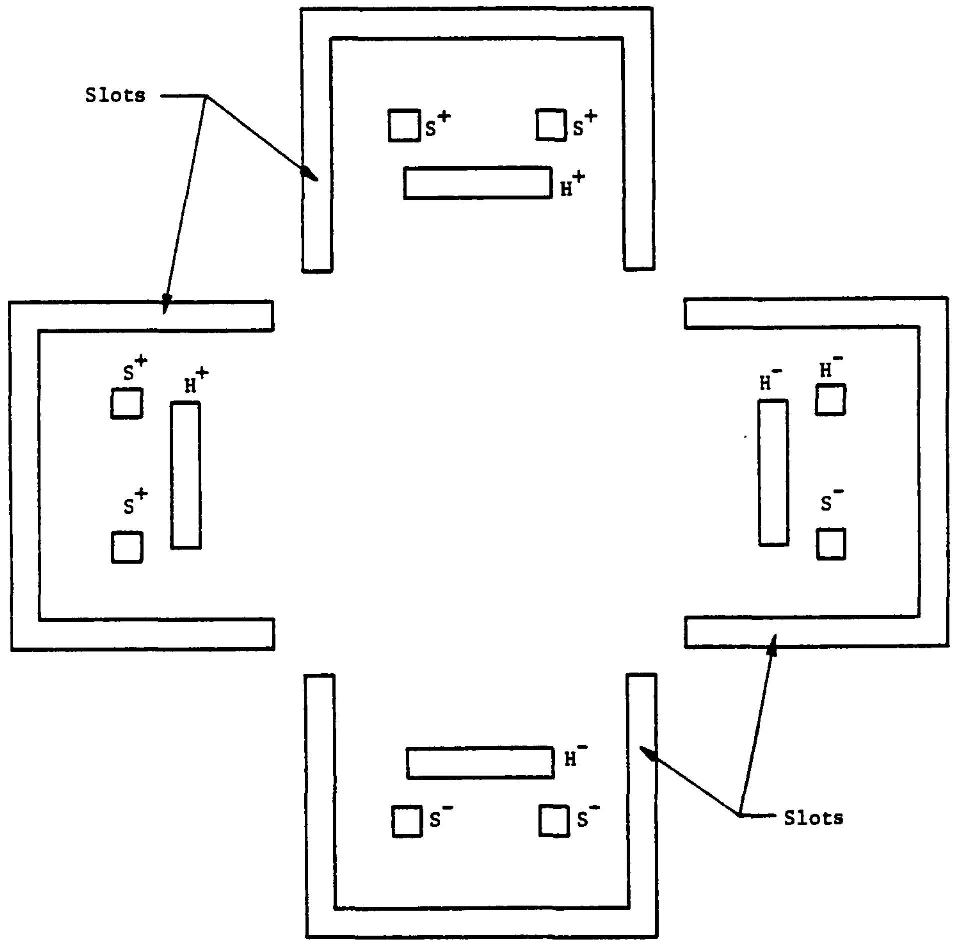


Fig. B.3 ETC Orthogonal Structure 3

APPENDIX C

TWO-CHANNEL ETC FABRICATION PROCEDURES

The transistors were fabricated by using n-type epitaxial layer with resistivity of 0.1 ohm-cm. The wafer had a crystal orientation of $\langle 111 \rangle$, and was about 15 mils thick. The fabrication of the two-channel ETC was mainly divided into seven steps as follows:

I. Isolation Diffusion
II. Base Diffusion
III. Emitter Diffusion
IV. Open Contact Window
V. Groove Etch
VI. Metalization
VII. Thin Etch

I. Isolation

See Integrated Circuit Engineering Institute Manual (ICEIM), 1976.

II. Base Diffusion

1. Clean the wafers.
2. Grow SiO_2 for 5000A on wafers (steam).
3. Open base region windows (photoresist).
4. Regrow SiO_2 for 2000A on the wafers (dry O_2).
5. Ion implant the wafers with dose level at 812.5 micro-coulombs.

6. Base Drive-In:

   Temperature = 1160°C

   Time = 50 min; N_2 at 50

   Time = 25 min; O_2 at 50

   Sheet Resistance $\approx$ 227 $\Omega/\square$

The wafers are now ready for opening emitter windows (photoresist).

III. Emitter Diffusion

1. Predeposition:

   Temperature = 1050°C

   Time = 5 min; O_2 at 40

   Time = 1 min; O_2 at 40; N_2 at 70 through $POCl_3$

2. Drive-in:

   Temperature = 1050°C

   Time = 4 min; O_2 at 40; N_2 at 70

   $\beta \approx 5$

3. Oxidation:

   Temperature = 900°C

   Time = 5 min; O_2 at 50

   Time = 25 min; Dry O_2 at 50; O_2 through steam at 30

   $\beta \approx 10$

IV. Open Contact Windows

See ICEIM, 1976.

V. Groove Etch

1. Regrow wet SiO_2 for 2000A.

2. Clean the wafers.

3. Deposit Si_3N_4 and W by CVD [Raymond and Nelson, 1978].

   Temperature = 750°C

   Time = 20 min; He pressure at 5 Torr; SiH_4 at 3 cc/min; and NH_3 at 133

   Time = 5 min; WF_6 at 3 cc/min

   Si_3N_4 = 3000A - 4000A

   W = 1 μm

4. Groove pattern:

   (a) Open groove window (photoresist)

   (b) W etch

   (c) Si_3N_4 etch in hot H_3PO_4

   (d) SiO_2 etch

5. Groove etch:

   (a) Mix the etchant ($HF:HNO_3$ = 1:25 by volume)

   (b) Mount the wafer on an etch header

   (c) Si etch in ultrasonic bath for 10 minutes

VI. Metalization

1. Aluminum deposition.

   See ICEIM, 1976.

VI. Metalization (Continued)

2. Apply photoresist (PR):

   (a) Mix PR and xylene with xylene:PR = 20:8 by drops.

   (b) Apply the mixture on the wafer and spin shortly. Repeat the process once.

   (c) Let the mixture dry on the spinner chuck.

3. Pre-bake for 10 minutes.

4. Post-bake for 30 minutes.

5. Delineate Al.

VII. Thin Etch [Stoller, Speers, and Opresko, 1970; and Wise, 1977]

1. Mix the etchant (HNO_3:HF:Acetic = 720:76:4 by volume).

2. Add 11.6 gm of sodium chlorite, slowly.

3. Mount the wafer on an etch header.

4. Si etch in a bubbling bath with CO_2 gas.

5. Remove the chips when the groove pattern appears.

APPENDIX D

SAMPLE CALCULATIONS AND THE ETC FILTER SCHEMATIC

From Eq. (5.2), and $L_x = 60$ mils, $L_y = 20$ mils and $a = 2.2$ mils

$$K = \frac{2.495 \times 10^{-3}}{\rho_s c_s} \quad \frac{\text{mW-sec}^{-1}}{°\text{C}} \tag{D.1}$$

$$\gamma = 2.742 \times 10^{-3} \frac{k_s}{\rho_s c_s} \quad \text{rps} \tag{D.2}$$

From Equations (5.19) and (5.20), at T = 318°K (45°C),

$$k_s = 3.03 \quad \frac{\text{mW}}{\text{mil - °C}}$$

$$\rho_s c_s = 28.24 \times 10^{-6} \quad \frac{\text{mW-sec}}{\text{mil}^3 \text{ - °C}}$$

Substituting k_s and $\rho_s c_s$ in Equations (D.1) and (D.2), one obtains

$$K = 88.38 \quad \frac{\text{mW-sec}^{-1}}{°\text{C}}$$

$$\gamma = 294 \quad \text{rps} \tag{D.3}$$

Each heater in Fig. D.1 has bias power of about 10 mW, and the chip temperature is estimated to be about 45°C (318°K). At T = 318°K, from Equations (5.19) and (5.20), one obtains

$$k_s = 3.03 \qquad \frac{\text{mW}}{\text{mil - °C}}$$

$$\rho_s c_s = 28.24 \times 10^{-6} \qquad \frac{\text{mW-sec}}{\text{mil}^3 \text{ - °C}}$$

From the experiment, it was found that

$$\frac{K_1}{K_2} = 1.09$$

For a = 2.2 mils, L_x = 60 mils, and L_y = 20 mils, from Eq. (5.2)

$$K_1 = 88.38 \qquad \frac{\text{°C}}{\text{mW-sec}}$$

$$K_2 = 81.08 \qquad \frac{\text{°C}}{\text{mW-sec}}$$

From measurements of heater currents and sensor gains, and η = 0.6924 mV/°C

$$K_{s_1} = (1.614)(0.6924) = 1.12 \text{ V/°C}$$

$$K_{s_2} = (1.586)(0.6924) = 1.10 \text{ V/°C}$$

$$Kh_1 = 27.14 \text{ mW/mA}$$

$$Kh_2 = 27.69 \text{ mW/mA}$$

Substituting Eq. (D.3) and $\omega_o = 2\pi$ (60) rps in Equations (5.17) and (5.18), one obtains

$$b_2 = 0.154 \quad \text{mA/V}$$

$$\rho = 0.060 \quad \text{mA/V}$$

$$Q = 5 \qquad b_1 = 0.041 \quad \text{mA/V}$$

$$Q = 10 \qquad b_1 = 0.048 \quad \text{mA/V}$$

Note that in the experiments all the feedback coefficients were set at the calculated values, except ρ. The measured value of ρ was 0.073 mA/V. The 20 percent error was due to combination of unknown values of exact k_s and $\rho_s c_s$, and experimental error.

The feedback coefficients calculated above were applied to their appropriate feedback loops given in Fig. 5.6. The full ETC band-pass filter schematic is shown in Fig. D.1. The element values of resistors are given in Table D.1. Note that Rb_1, $R\rho$ and Rb_2 in the schematic indicate the variable resistors used for adjusting the feedback coefficients. Other variable resistors are for offset adjustments.

Table D.2 shows element values for the ETC integrator circuit given in Fig. 5.13.

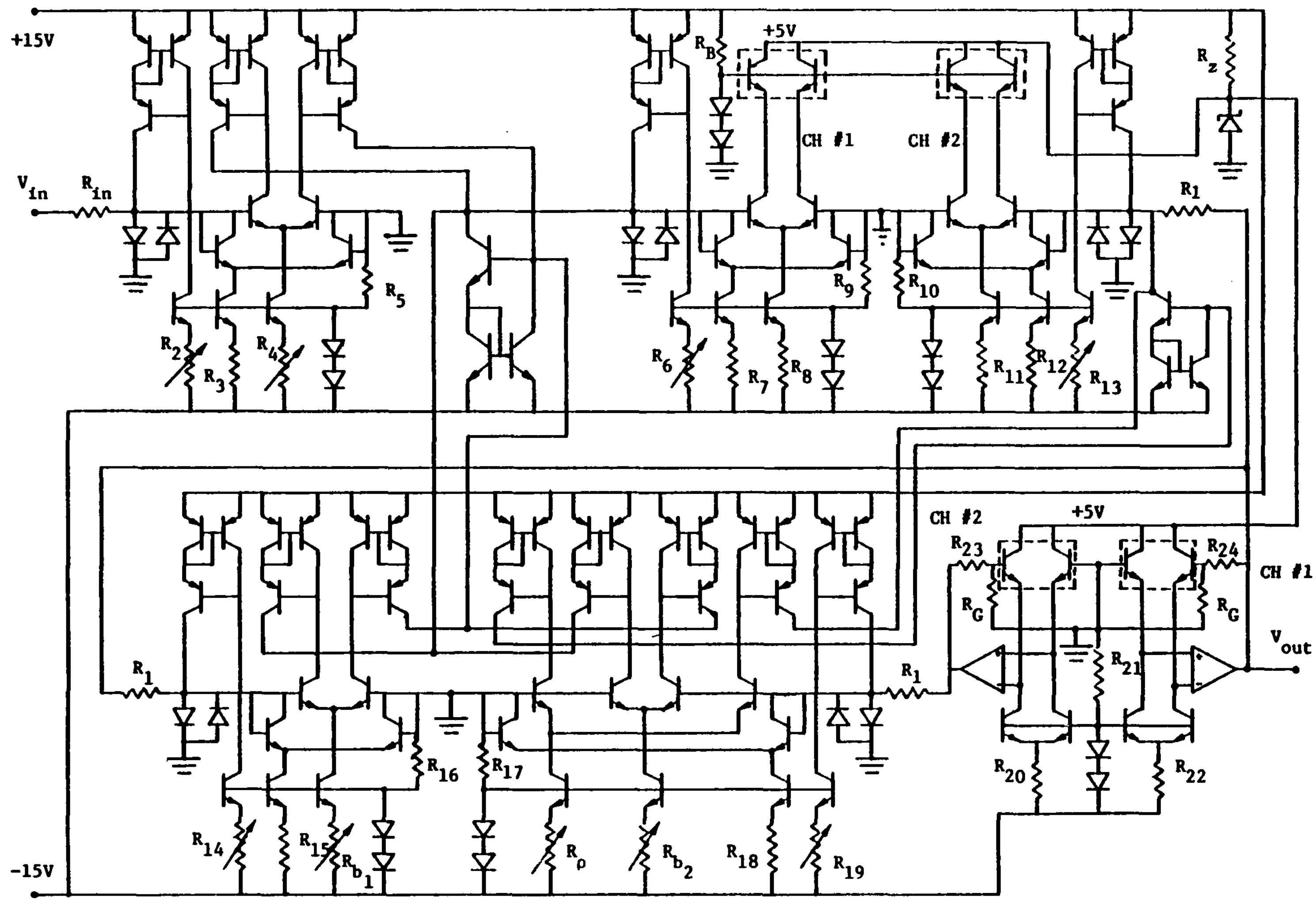


Fig. D.1 Schematic of the ETC Band-Pass Filter

Table D.1 Resistor Values of the ETC Band-Pass Filter Schematic in Fig. D.1

Resistors	Values (ohms)	Resistors	Values (ohms)
R_{in}, R_1	28.7K	R_2	300 + 10K pot.
R_B	6.8K	R_4	476 + 10K pot.
R_6	52.2	R_6, R_{13}	10K pot.
R_2	680.0	R_{14}, R_{19}	10K pot.
R_3	150.7	R_{b_1}	1.5K // 20K pot.
R_5	5K	R_ρ	390 // 20K pot.
R_7	788.0	R_{b_2}	1.41K // 10K pot.
R_8	100.0		
R_9, R_{10}	10K		
R_{11}	101.0		
R_{12}	791.0		
R_{15}, R_{18}	768.0		
R_{16}, R_{17}	10K		
R_{20}	10.39K		
R_{21}	1.5K		
R_{22}	9.56K		
R_{23}	82.75K		
R_{24}	84.2K		

Table D.2 Resistor Values of the ETC Integrator Circuit in Fig. 5.13

Resistors	Values (ohms)
R_{in}, R_1	28.7K
R_z	680
R_B	6.8K
R_3	788
R_4	100
R_5, R_{12}	10K
R_6	52.2
R_7	84.2K
R_8	9.56K
R_9	1.5K
R_{10}	768
R_2	10K pot.
R_{11}	1.5K//20K pot.

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