IMPROVED RELIABILITY IN THRESHOLD LOGIC CIRCUITS THROUGH REDUNDANCY

by

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TABLE OF CONTENTS

LIST OF TABLES

ILLUSTRATIONS

ABSTRACT

This paper investigates the use of redundancy in threshold logic circuits to improve the system reliability. Three basic theories for implementing redundancy into threshold logic are presented. The developments of each method modify a gate to incorporate error correction on redundant information while maintaining its functional nature. The error correction is provided by these logical decisions in conjunction with the proper gate interconnections.

Each method is indicated to have specific advantages and disadvantages in light of certain types of errors. The first method can efficiently correct errors resulting from component tolerance variations. The third method is most attractive when errors resulting from catastrophic component failures are to be corrected. Although the second method is not as efficient as the other two in correcting specific errors, it is advantageous in that it effectively corrects both types of errors.

The relative advantages of the three methods are compared by indicating their relative reliability improvements. Also the modification procedures for each development are indicated by some example applications.

CHAPTER ONE

A digital computer designed to accurately process information requires a measure of confidence that the system will behave as planned. Since the computer uses individual components with a limited reliability, the system reliability is bounded. Any desire to insure a system with a greater reliability must use some form of redundancy. The subject of this paper is to present theories for implementing redundancy in threshold logic circuits.

From a view on its logical power a threshold logic element is superior to the conventional (OR, AND, NAND, and NOR) logical elements. The functions generated by conventional elements are special cases in the class of functions realizable by a single threshold gate. Since threshold gates can realize a variety of functions, a threshold circuit realization of a boolean function will generally require fewer gates than a realization using conventional elements. In a program designed to study the feasibility of using threshold gates to build a computer, Coates and Lewis (1963) determined that with the exception of memory the number of threshold gates required is about one-fourth the number of NOR gates that would be needed. The hardware reduction makes threshold gates seem more attractive than conventional elements for building digital computers. (This assumes the amount of hardware needed in a threshold gate is comparable to that required by a conventional gate, as is the case for resistor-transistor gate realizations.)

The main limitation of a physical threshold device is the constraint placed on the tolerances of the components. As the function to be generated becomes more and more complex the actual component values become more critical. Thus the properties of threshold gates which can be practically realized depend on component fluctuations.

Methods are developed which correct errors due to varying component values and errors stemming from catastrophic component failures characteristic of both threshold and conventional devices. Techniques developed by other authors for conventional circuitry are applied to threshold circuits, and new techniques specifically applicable to threshold elements are introduced. To the author's knowledge no literature has appeared specifically applying error correction to threshold circuits, with the exception of a development by Pierce (1964) for simple threshold devices.

One error correcting technique receiving considerable attention involves generating a set of redundant signals and using a majority gate as a restoring organ to determine the correct output. Threshold logic can be modified to perform a similar decision and still maintain its functional nature. This development is presented as the third method in chapter four.

Another technique developed by Tryon (1962) and extended by Pierce (1964) uses alternating layers of correction. Errors not corrected in one level are transmitted to the next level and corrected there. This application to threshold circuits is presented in the third chapter.

The two previous methods involve correction on a set of redundant outputs by gates that follow. The technique presented in the second chapter is basically different in that each non-redundant element is replaced by an interconnection of redundant elements which provide a single more reliable output. Once the output is generated it is assumed correct. In this case the reliability improvment is dependent on the significance of the probability of permanent gate failure. This is characteristic for any development of this nature, since the reliability of the redundant circuit can be no greater than the probability of a permanent failure not occuring in the output gate. This points to a difference in the value of the two types of developments. The second and third methods correct errors on outputs, hence it is immaterial why these errors occur. The first method can only correct for tolerance errors but does so more efficiently than the other two. Proofs are included in the presentations which state that for the first and third methods the effects of certain types of errors can be arbitrarily minimized. These proofs are not intended to assert that arbitrary reliability can actually be achieved but are merely intended to indicate which developments are best suited to correct a certain type of failure.

Several devices have been proposed with characteristics which lend themsleves useful as a threshold logic element. Five of these are mentioned by Minnick as:

1. Magnetic core circuits
2. Resistor-transistor circuits
3. Parametron circuits

4. Resistor-tunnel diode circuits

5. Multiple coil relay circuits

The developments of this paper are applicable to threshold gates in general, but are primarily designed for use with resistor-transistor circuits. An example of a simple resistor-transistor gate realization is presented in figure 1.

LINEARLY SEPARABLE FUNCTIONS

The class of functions which can be realized by a single threshold gate are called linearly separable functions as now defined.

A function f of the boolean variables in the set $\{X\} = \{x_1, x_2, \cdots x_n\}$ is linearly separable if and only if there exists a set of weights $\{N\} = \{N_1, N_2, \cdots N_n\}$ and a value for $N_t > 0$ such that:

$$\sum_{i=1}^{n} N_i x_i < N_t \Big|_{f=0} \quad [1] \tag{1}$$

$$\sum_{i=1}^{n} N_i x_i > N_t \Big|_{f=1} \tag{2}$$

In a circuit realization of the above function component values are selected to give each input x_i its corresponding weight N_i. Also a designed threshold T_d is established near enough to N_t to provide proper functioning. The resistor-transistor gate in figure 1 has been designed to realize $\bar{f} = x_1 + x_2x_3$, where $N_1 = 2$, $N_2 = 1$, $N_3 = 1$, and $N_t = 3/2$.

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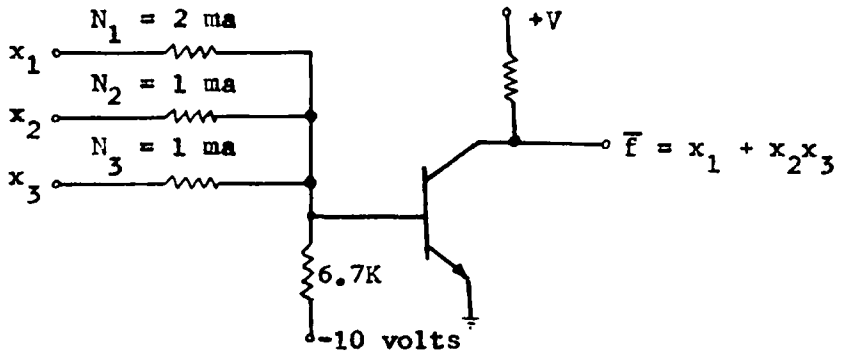
1. The vertical line followed by an equation is used to designate: "the relation holds under the condition stated in the equation."



A resistor-transistor threshold gate realizing the function $x_1 + x_2x_3$

Figure 1

RELIABILITY

A threshold device realizing f will have a tolerance range t for its threshold T. The example of figure 1 has a designed threshold T_d = 1.5 ma with a tolerance range between 1 and 2 ma. The tolerance range can be determined from the properties of f as follows:

M is defined as the maximum of $\sum_{i=1}^{n} N_i x_i \Big|_{f=0}$ (3)

m is defined as the minimum of $\sum_{i=1}^{n} N_i x_i \Big|_{f=1}$ (4)

$$t = m - M \tag{5}$$

It is assumed in a gate realization that the weights have their designed values and their actual fluctuations only contribute to a narrowing of t. For a discussion on the effects of threshold and weight sensitivities, see Lewis and Coates (1963). If the actual threshold T is outside the specified tolerance range, the device will be in a state

capable of making one of two errors. These errors are designated by e_1 and e_2 as now defined.

$$e_1 \text{ occurs when } \sum_{i=1}^{n} N_i x_i > T \Big|_{f=0} \tag{6}$$

$$e_2 \text{ occurs when } \sum_{i=1}^{n} N_i x_i < T \Big|_{f=1} \tag{7}$$

Associated with the T of each device is some probability distribution P(T) dependent on the distributions of the components themselves. From the distribution certain probabilities are defined as:

$$p_1 = P(T<M) \qquad \text{probability of } e_1 \tag{8}$$

$$p_2 = P(T>m) \qquad \text{probability of } e_2 \tag{9}$$

The probability that the device is in an error producing state is:

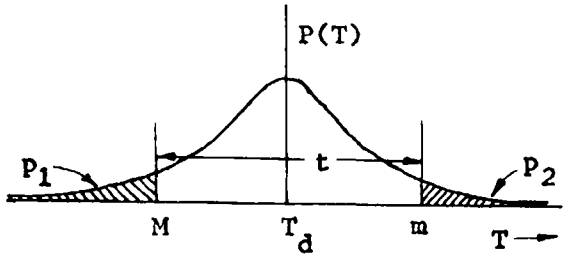
$$p_e = p_1 + p_2 \tag{10}$$

It is assumed in general that p_e can be minimized by placing T_d in the middle of t.

The reliability, or probability that the gate functions as designed, is designated by:

$$p_f = 1 - p_e \qquad P(T \subset t) \tag{11}$$

These probabilities are illustrated in figure 2.



Probability distribution of T

Figure 2

The reliability measure used in analyzing the circuits is a functional reliability established by Amarel and Brzozowski (1962) as " a measure of confidence that the circuit will perform exactly as intended by its logical designer." It is not general enough to state that a circuit is in error since this depends on the input.

An analysis of the reliability of the redundant cirduits involves consideration of two types of errors. The first type of error is one that results because component values are such that the actual threshold is non-zero and finite but outside the specified tolerance range. In a resistor-transistor gate this type of error can result from noise and deviations in resistive values, switching characteristics of the transistor, and power supply values. Since the switching characteristics of the transistors are temperature dependent, thermal conditions can also be significant factors. This type of error is referred to as a tolerance error.

The second type of error is one that results because the logical element is in a state that gives an output independent of any input. In a resistor-transistor gate this error can result from complete failures of any of the components (i.e. the components become open or short circuits) or faulty connections within and between gates. This type of error is referred to as permanent. The probabilities of the two permanent errors are denoted by:

$$p_s = P(T=0) \qquad \text{i.e. the output is always "1"} \quad (12)$$

$$p_o = P(T=\infty) \qquad \text{i.e. the output is always "0"} \quad (13)$$

When the reliability of a redundant network is determined, the following assumptions are made:

1. Errors occuring in separate gates are assumed independent. If power supply fluctuations contribute significantly to the probability of error, this assumption requires each in a set of redundant gates to be supplied separately. Another consequence of this assumption is that a failure of a gate does not corrupt its inputs, since inputs may lead to other gates as well.

2. Sets of higher order errors will be considered negligible. That is, in a set of redundant gates a certain subset of E + 1 gates and another subset of E + 2 gates can both cause a failure. The probability of the latter occuring is assumed insignificant to that of the former. This is valid as long as p_e is sufficiently small.

3. In order to compare the reliability of redundant realizations to those of non-redundant realizations, redundant and non-redundant gates are assumed to have similar reliabilities. This is true to a greater or lesser degree depending on how the redundancy modifications change the tolerance range.

REDUNDANT CIRCUITS

A non-redundant circuit is one that has a system failure if any element fails. Applying redundancy by the methods presented allows any E gates in a set of R redundant gates to fail but insures that the overall system functions properly. The value of E is designated as the order of error correction, and R is the redundancy applied to achieve this correction.

The notation used in a redundant circuit will designate redundant functions and signals by superscripts. In this manner a gate realizing the function f will be replcaced by a set of R gates realizing the functions f^1, f^2, ... f^R. A variable x_i will be replaced by a set of variables $\{x_i\}^R = \{x_i^1, x_i^2, \ldots x_i^R\}$ all designed to represent the same information.

The error correction is accomplished by modifying a non-redundant gate or circuit to form what we shall hereafter call a decision on the redundant information. The decisions are so chosen that a gate realizing a function f is redundancy modified to realize a function f'. f' represents the same information as f, but incorporates in addition to its logical function, a decision on the redundant information. When a gate is modified to realize f', it is generally necessary to change the non-redundant threshold T_d to a new threshold T_d' and certain weights N_i to new weights N_i'. The method by which these modifications are made constitute a redundancy modified logic theory. The decisions and the methods of interconnection are the distinguishing features of the three developments.

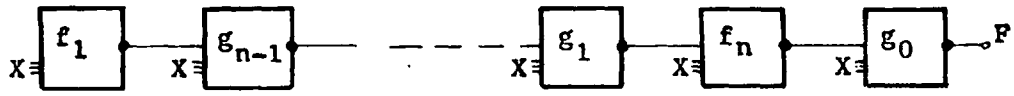
FUNCTION REALIZATIONS

Although a general boolean function F can be realized in a variety of ways with threshold gates, two specific methods have a property which admits easy adaptation to error correction. This property is that all gates in the realization receive only one input from another gate. Thus if the input variables to the circuit are assumed reliable,

a gate need only provide error correction on one input. This manner of realization does not necessarily provide a minimal solution as will be shown for the seven bit parity checker in chapter six.

Both methods of realization under consideration involve breaking F up into a set of linearly separable functions and realizing the sub-functions by alternation of generating and impeding functions. The need to alternate generating and impeding levels follows from the use of resistor-transistor gates which invert their outputs.

Method I The first method is one in which the output of each gate is "OR"ed with the function of the next gate. This can be accomplished for any function by merely weighting the previous gate's output greater than the threshold. Figure 3 indicates the method of realization where $\{X\}$ represents the set of input variables to the circuit. A dot is used on the gate output to denote an inverting device.



$$F = \overline{g_0} f_n + \overline{g_1} f_{n-1} + \overline{g_2} f_{n-2} + \cdots \overline{g_{n-1}} f_1$$

Type I function realization

Figure 3

$$F = \overline{g_0 + \left(f_n + \left(g_1 + \left(f_{n-1} + \cdots \overline{(g_{n-1} + \overline{f_1})}\right)\right)\right)}$$

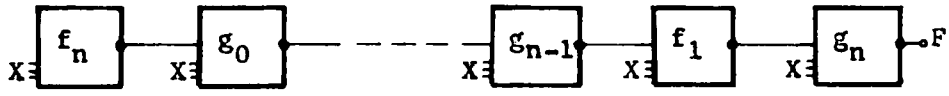
$$= \overline{g_0}\left[f_n + \left(g_1 + \left(\overline{f_{n-1} + \cdots (g_{n-1} + \overline{f_1})}\right)\right)\right]$$

$$= \overline{g_0} f_n + \overline{g}_0 \overline{g}_1 f_{n-1} + \overline{g}_0 \overline{g}_1 \overline{g}_2 f_{n-2} + \cdots \overline{g}_0 \overline{g}_1 \cdots \overline{g}_{n-1} f_1$$

If $g_{n-1} \supseteq g_{n-2} \supseteq \cdots g_1 \supseteq g_0$,

$$F = \overline{g_0} f_n + \overline{g_1} f_{n-1} + \overline{g_2} f_{n-2} + \cdots \overline{g_{n-1}} f_1 \tag{14}$$

Method II The second method "ANDS" the output of each gate with the function of the next gate. This can always be accomplished by sufficiently increasing a gate's threshold to insure it won't be exceeded unless the output of the previous gate is "1". The output of the previous gate is then weighted with a value equal to the increase. Figure 4 demonstrates this method of realization.



$$F = \overline{g_n} + f_1\overline{g_{n-1}} + f_2\overline{g_{n-2}} + \cdots f_n\overline{g_0}$$

Type II function realization

Figure 4

$$F = \overline{g_n\left(f_1\left(g_{n-1}\left(f_2\left(\cdots \overline{g_0 f_n}\right)\right)\right)\right)}$$

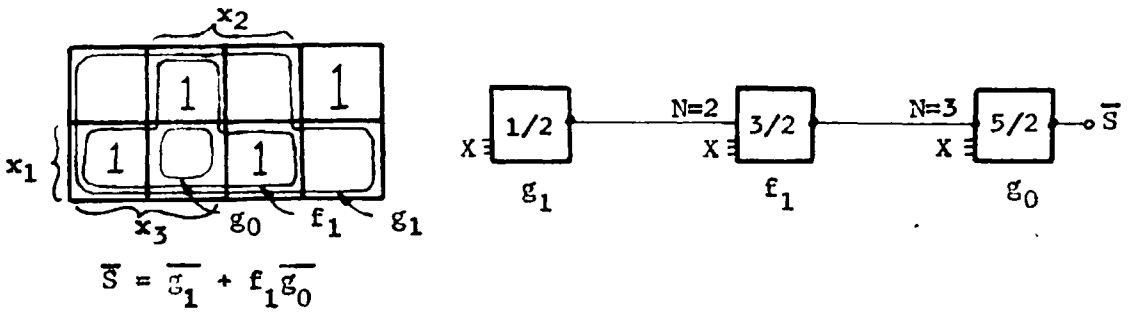
$$= \overline{g_n} + f_1\overline{g_{n-1}} + f_1 f_2\overline{g_{n-2}} + \cdots f_1 f_2 f_3 \cdots f_n\overline{g_0}$$

If $f_1 \supseteq f_2 \supseteq f_3 \supseteq \cdots f_n$,

$$F = \overline{g_n} + f_1\overline{g_{n-1}} + f_2\overline{g_{n-2}} + \cdots f_n\overline{g_0} \tag{15}$$

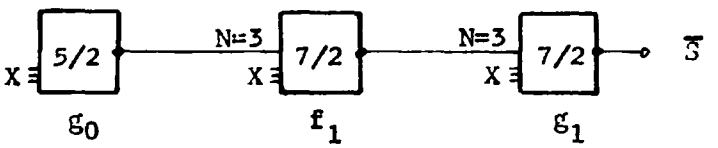
It is indicated in both developments that any function F can be realized by breaking it into a set of subfunctions. Each subfunction is expressed as the boolean product of a linearly separable generating

function and a linearly separable impeding function. An example realization for a full adder is provided for both methods in figures 5 and 6.



Type I adder realization

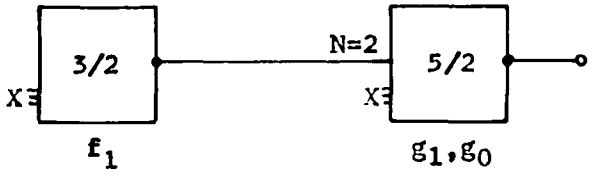
Figure 5



Type II adder realization

Figure 6

For certain functions methods I and II can be combined to yield a more nearly minimal solution. The full adder is one of these functions. The combination involves "AND"ing the previous output with one function f_1 of a gate and "OR"ing the result with another function f_2 of the same gate. A necessary condition is that f_1 strictly contains f_2. Realizations of this type are particularly applicable to symmetric functions which are considered at length in Kautz (1961) and Sheng (1964). The adder realized in this way is shown in figure 7.



Modified adder realization

(where $g_1 \supset g_0$ and are both realized by one gate)

Figure 7

CHAPTER TWO

A method is presented in this chapter which replaces a non-redundant gate by an interconnection of gates producing a single output, that is more reliable as long as permanent errors are negligible. The development is systematic in that higher degrees of redundancy are extensions of lower degrees. Since the redundancy can be applied to a gate realizing any linearly separable function, the method is applicable to any form of realization.

A circuit with $R = (E+1)^2$ redundant gates generates the information of f R times. This produces the set of functions $\{f\}^R = \{f^1, \cdots f^R\}$. The circuit interconnections and modified gates systematically operate on $\{f\}^R$ to produce a single output which is correct as long as no more than E gates are in error.

Each gate (except those on the first level) receives, in addition to the $\{X\}$ inputs, two inputs from other gates also generating the information of f. One of the additional inputs is "AND"ed with the function f and the other is "OR"ed with the result. If these two inputs are y_1 and y_2 respectively, the redundancy modification becomes one of generating the function $f' = fy_1 + y_2$. Since y_1 and y_2 represent the same information as f, f' also represents the information of f. That any gate realizing a linearly separable function can be so modified is established in theorem 1.

Define W as $\sum_{i=1}^{n} N_i$. (16)

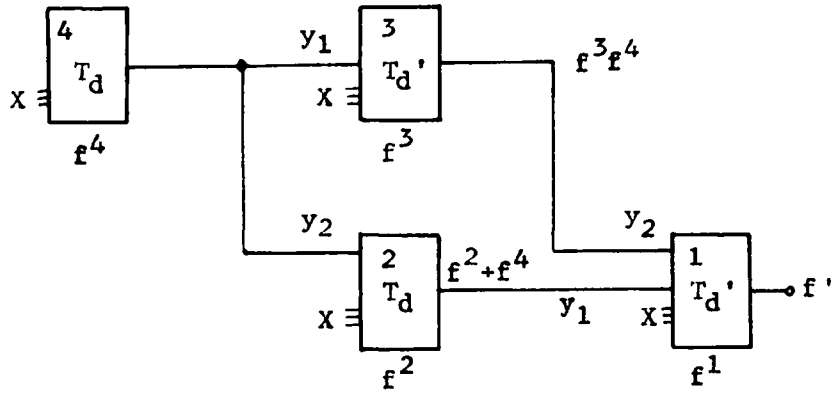
Theorem 1 If N_t is the value separating a non-redundant f(X), $N_t' = W + N_{y1}$ separates the function fy_1 where y_1 is an additional variable with weight N_{y1}. If another variable y_2 is weighted with N_{y2} greater than N_t', N_t' separates the function $f' = fy_1 + y_2$.

Proof: It is merely necessary to note that:

$$f' = 1\Big|_{y_2=1} \qquad \text{and} \qquad f' = f\Big|_{y_1=1,y_2=0}$$

A threshold gate could in theory realize f' for any N_{y1}. However, N_{y1} must not be too large for tolerance reasons. If N_{y1} is quite large compared to the values in N, a small fluctuation on its part could be a major fluctuation affecting the tolerance range of f. If N_{y1} is highly accurate and y_2 has a perfect zero, the tolerance range t is unchanged. Thus, the redundancy modified gate has a functional reliability similar to that of the non-redundant gate dependent only on N_{y1} and the zero of y_2. N_{y2} should be as large as is practical to insure that $f' = 1$ when $y_2 = 1$. Notice that if both y_1 and y_2 are accurate, the gate can fail only if $T < W$ or $T > N_{y2}$. If P(T) is assumed to have a small standard deviation with respect to t (not unreasonable if the gate is fairly reliable), $P(T<W)$ is essentially p_s and $P(T>N_{y2})$ is essentially p_o. It can now be seen that if y_1 and y_2 are made more and more reliable with increasing redundancy the reliability of f' is bounded above only by $1 - (p_o+p_s)$.

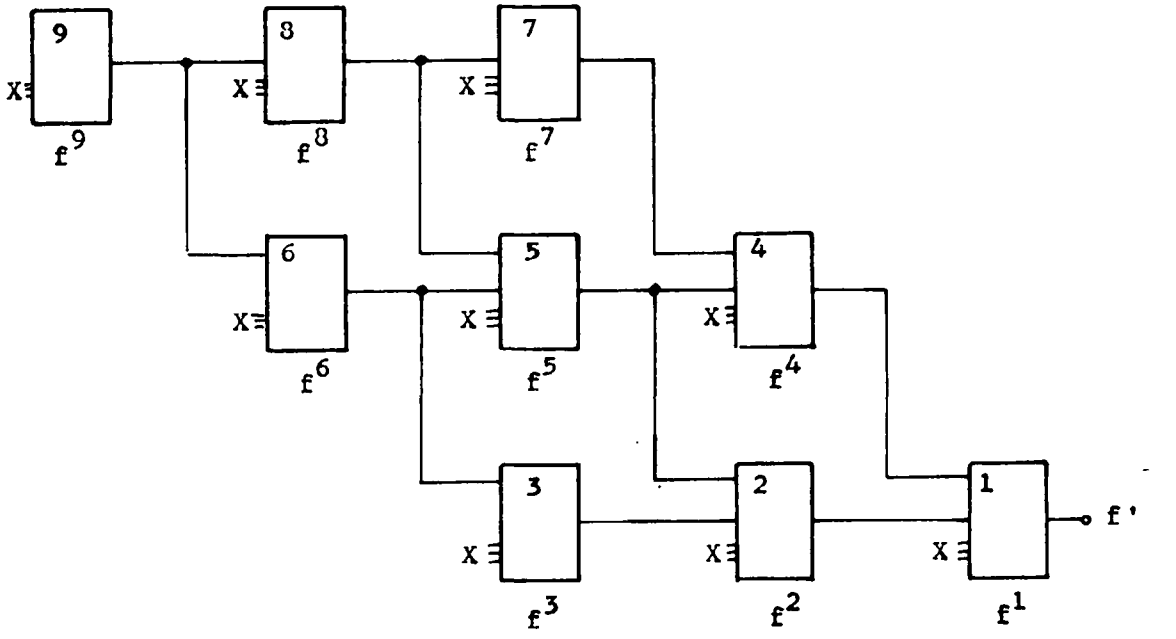
Since the modifications for a gate realizing the redundancy modified function f' have been given, only the interconnections between gates need be established. The circuits in figures 8 and 9 indicate the connections to be made for E = 1 and 2. The y_1 for each gate (#j) is



$$f' = f^1(f^2+f^4) + f^3f^4$$

Circuit for 1st order error correction

Figure 8



$$f' = f^1\left[f^2(f^3+f^6+f^9) + f^5(f^6+f^9) + f^8f^9\right] + f^4\left[f^5(f^6+f^9) + f^8f^9\right] + f^7f^8f^9$$

Circuit for 2nd order error correction

Figure 9

the output of the gate (#j+1) immediately to its left and y_2 is the output of the gate (#j+E+1) to the left and above. T_d' is the designed threshold of a gate realizing f'.

Greater error correction is achieved by extending the circuit form of figure 9. The development directly follows that used to proceed from the circuit for E = 1 to that for E = 2. A circuit correcting all sets of three errors requires sixteen gates.

An analysis of the reliability of the above circuits must consider the effect of permanent error states on the circuit's error correcting ability. The circuit will be in a state of permanent error if gate 1 is permanently in error or if gate E + 2 is always in a "one" state. The probability of this occuring is $2p_s + p_o$.[2] Thus the development is actually more unreliable in terms of permanent error correction.

If permanent errors are considered negligible, the circuits produce the outputs indicated. A reliability analysis in terms of p_1 and p_2 for individual gates is now developed.

A circuit of error correction E will have a probability of error:

$$p_e(E) = p_1(E) + p_2(E) \tag{17}$$

$$\text{where } p_1(E) = C_1(E)p_1^{E+1} \quad \text{and } p_2(E) = C_2(E)p_2^{E+1} \tag{18}$$

$C_1(E)$ is the number of combinations of gates in error state one that produce a circuit "one" when "zero" is correct (type one error). $C_2(E)$ is the number of combinations of gates producing type two errors

---

2. The probability is actually $p_s + p_o + p_s(1-p_s-p_o)$, but this involves higher order effects which are negligible under the assumption that p_s and p_o are small.

that give the circuit a type two error state. In the development shown equal error dependence has been placed on p_1 and p_2 so that $C_1(E) = C_2(E)$. $C_1(E)$ can be determined by examining the output equations for the number of minterms in the expanded form. This is easily seen to be three for the circuit in figure 8. $C_1(E)$ can be determined for the general case by noting that separate terms are generated in the same fashion as Pascal's triangle for binomial coefficients. Equating the two produces the result:

$$C_1(E) = \binom{2E+1}{E} \tag{19}$$

The following table uses the above results to show the reliability for various orders of error correction when permanent errors are neglected.

Table 1

Error probabilities and necessary redundancy (for different orders of error correction)

Order of error correction	Necessary redundancy	$p_1(E)$	$p_2(E)$
0	1	p_1	p_2
1	4	$3p_1^2$	$3p_2^2$
2	9	$10p_1^3$	$10p_2^3$
3	16	$35p_1^4$	$35p_2^4$
4	25	$126p_1^5$	$126p_1^5$
E	$(E+1)^2$	$C_1(E)p_1^{E+1}$	$C_2(E)p_2^{E+1}$

Table 1 indicates that the reliability of a circuit for E = 1 is better than that of a non-redundant gate, if both p_1 and p_2 are less than 1/3. If a circuit for E = 2 is to be more reliable than one for

E = 1, it is sufficient that p_1 and p_2 be less than 3/10. In general a circuit with an order of error correction E + 1 will be more reliable than one with error correction E if p_1 and p_2 are both less than 1/4. This result is indicated in the following theorem.

Theorem 2 A systematic expansion of these circuits to higher orders of error correction produces arbitrary reliability if the probability of permanent errors is negligible and both p_1 and p_2 are less than 1/4.[3]

Proof: The error probabilities for successive orders of error correction can be considered a sequence of terms in an infinite series. The E^{th} term of the series is $C_1(E)p_1^{E+1} + C_2(E)p_2^{E+1}$. Since $C_1(E) = C_2(E)$, only the series for $p_1(E)$ will be considered and the same results will hold for $p_2(E)$. The ratio test will be used to show the series converges.

$$r = \frac{p_1(E+1)}{p_1(E)} = \frac{\binom{2E+3}{E+1}p_1^{E+1}}{\binom{2E+1}{E}p_1^{E}}$$

$$= \frac{(2E+3)!E!(E+1)!}{(2E+1)(E+1)!(E+2)!}p_1$$

$$= \frac{(2E+3)(2E+2)}{(E+2)(E+1)}p_1$$

$$= \frac{4(E+3/2)}{(E+2)}p_1$$

$$< 4p_1$$

$$< 1 \qquad \text{if } p_1 < 1/4$$

---

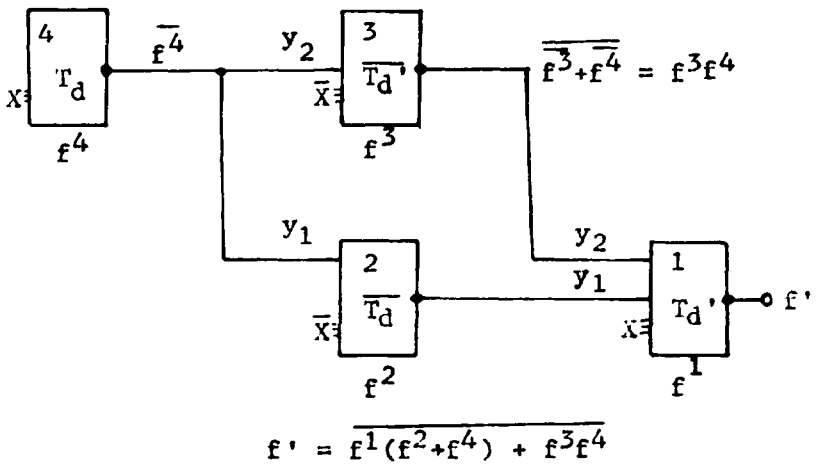
3. The expressions for error probability assume p_1 and p_2 are much smaller than 1/4, but since the expressions are greater than the actual probability, the theorem holds for an exact analysis by comparison.

The development has so far assumed non-inverting gates. Since resistor-transistor gates are the principal concern of this investigation, the effect of inverting elements is now considered. Inverting gates will cause the inputs y_1 and y_2 to represent the function $\bar{f}$ instead of f. An inverting gate can be modified to behave as a non-inverting gate if negative weights are allowed. If N_t separates a function of the variables $\{X\} = \{x_1, \cdots x_i, \cdots x_n\}$ with weights $\{N\} = \{N_1, \cdots N_i, \cdots N_n\}$, then $N_t' = N_t - N_i$ separates the same function where the variables are $\{X'\} = \{x_1, \cdots \bar{x}_i, \cdots x_n\}$ with weights $\{N'\} = \{N_1, \cdots -N_i, \cdots N_n\}$. Thus, to modify a gate realizing f' which receives complemented variables for y_1 and y_2, change T_d' to $T_d'' = T_d' - N_{y1} - N_{y2}$ and change the sign of their respective weights.

An alternative approach eliminates the need for negative weights. If the gates generating y_1 and y_2 are modified to generate $\bar{f}$, double negation occurs so y_1 and y_2 represent f. This requires the set of inputs to the circuit to include both the natural and negated forms. If N_t separates the function f of the variables $\{X\} = \{x_1, \cdots x_n\}$ with weights $\{N\}$, $\bar{N}_t = W - N_t$ separates the function $\bar{f}$ where the variables are $\{\bar{X}\} = \{\bar{x}_1, \cdots \bar{x}_n\}$ with weights $\{N\}$. The desired error correction can now be realized if levels alternate in realizing f and $\bar{f}$. The development for E = 1 is shown in the following figure. Notice that y_1 and y_2 have been interchanged on alternating levels because of the inversion.

If one circuit drives another circuit of the same development, it must provide both f and $\bar{f}$. This can be accomplished by adding an inverter or using an output from gate 2 or gate E + 2. These outputs are less

reliable from a tolerance standpoint, but using the gate 2 output reduces the effect of permanent errors slightly. Either of the above methods provide the side advantage of not requiring a single gate to drive all gates in another redundant circuit.



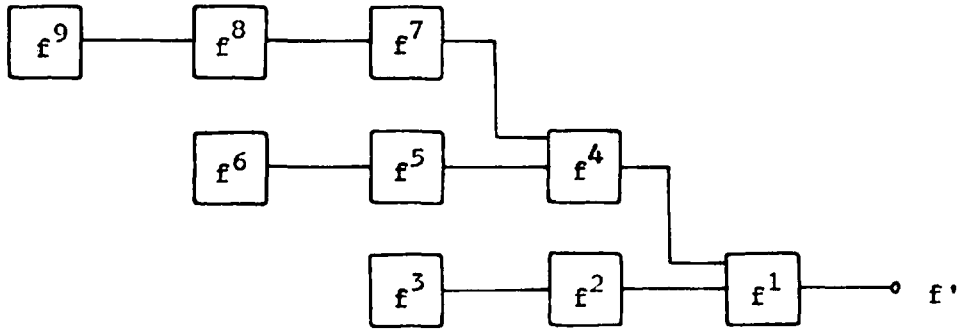
Circuit for error correction of order 1
(where inverting gates are used)

Figure 10

ALTERNATE CIRCUITS

1. The previous development was made with the intention of keeping the reliability dependence on p_1 and p_2 equal. By eliminating y_2 connections, the reliability is less dependent on p_1 but more dependent on p_2. For the extreme case where the maximum number of y_2 connections are eliminated, a circuit for E = 2 is shown in figure 11. A list of the corresponding error probabilities is given in table 2 for circuits with various orders of error correction, when the maximum number of

y_2 connections are removed. Notice that the sum of the coefficients on p_1^{E+1} and p_2^{E+1} is greater than when all conections are made, so that unless p_2 is smaller than p_1 the initial configuration is best.



$$f' = f^1f^2f^3 + f^4f^5f^6 + f^7f^8f^9$$

Circuit for order 2 error correction
(with maximum number of y_2 inputs removed)

Figure 11

Table 2

Error probabilities for circuits with minimum number of y_2 connections

Order of error correction	$p_1(E)$	$p_2(E)$
1	$2p_1^2$	$4p_2^2$
2	$3p_1^3$	$27p_2^3$
3	$4p_1^4$	$256p_2^4$
E	$(E+1)p_1^{E+1}$	$(E+1)^{E+1}p_2^{E+1}$

Table 2 shows that no reliability increase can be obtained when $(E+1)p_2$ approaches one.

2. A dual development is possible where a gate's function is "OR"ed with y_1, and the result is "AND"ed with y_2 so that $f' = (f+y_1)y_2$. This produces the same reliabilities as the previous development for a complete circuit. If y_2 connections are eliminated from this development, the reliability becomes more dependent on p_1 and less dependent on p_2. Thus a method is produced which best corrects errors if p_1 is dominant.

CHAPTER THREE

Following the work of Tryon (1962) and Pierce (1964) for conventional circuits, another technique for error correction in threshold circuits is developed. In this method a non-redundant gate is replaced by a set of gates which constitute a redundancy level. The outputs of each gate in a level drive gates in the next level. Error correction is accomplished by modifying the gates of succeeding levels to compare the redundant outputs of the previous level.

When a redundancy modified gate compares a set of redundant inputs, it forms a decision. The decisions used by this method are either "AND" decisions or "OR" decisions. If the "AND" decision is used, the modified gate operates on the redundant inputs as "1" only if all of them are "1". Thus a gate modified to make an "AND" decision on the set of signals $\{x_j\}^r = \{x_j^1, \cdots x_j^r\}$ operates on $x_j^1 x_j^2 \cdots x_j^r$ as x_j is operated on by a non-redundant gate.[4] The use of an "OR" decision modifies a gate to operate on the redundant inputs as "0" only if all of them are "0". In this way an "OR" decision on the inputs $\{x_k\}^r = \{x_k^1, \cdots x_k^r\}$ requires a modified gate to function on $x_k^1 + x_k^2 + \cdots x_k^r$ as a non-redundant gate functions on x_k.

If any input upon which an "AND" decision is made erroneously becomes a "0", an error will be made. Similarly any input erroneously becoming a "1" causes an "OR" decision to be in error. A critical error

---

4. A small r is used to denote input redundancy because it is less than the gate redundancy R.

is one that causes a decision to be in error. An error that does not cause the decision to be in error is said to be subcritical. A "0" to "1" error (e_1) and a "1" to "0" error (e_2) are subcritical for "AND" and "OR" decisions respectively.

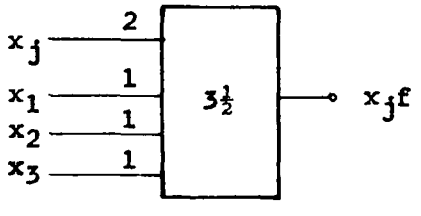
The method of error correction is one of building alternating layers of correction. The decisions are so chosen that a critical error in one level is subcritical in the next. This implies that an "OR" decision must be followed by an "AND" and vice versa (unless inverting gates are used). When the proper interconnections are made, errors becoming subcritical by passing through one level of gating are compared with correct signals in the next level. In this way a critical error must not corrupt two gates which are compared with each other in the next level.

For this development the use of inverting gates turns out to be an advantage. If all levels use the "OR" decision exclusively or the "AND" decision exclusively, a critical error in one level automatically becomes subcritical in the next. Thus all gates can be modified to perform the same decision and proper interconnections provide the error correction.

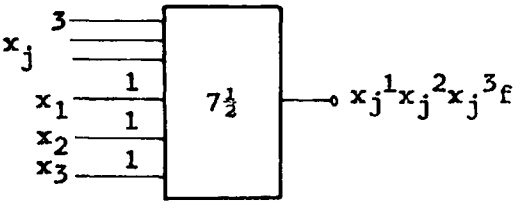
The principal limitation in using this method is that some gates realizing linearly separable functions can not be modified to perform the desired decision. As a simple example for r = 2, a gate realizing the following function can not be modified to perform the "AND" decision: $f = x_j + x_1x_2$. This follows because the function: $f' = x_j^1x_j^2 + x_1x_2$ is not linearly separable. Similarly a gate realizing $f = x_k(x_1 + x_2)$ can

not be modified to realize $f' = (x_k^1 + x_k^2)(x_1 + x_2)$ because this also is not linearly separable. The error correction of this method is not completely inapplicable to these functions, however, and some alternatives are presented later in the chapter which modify the development to these cases.

A realization in either of the two forms presented in the introduction can easily be modified to perform the decisions. In the type I realization an input x_k with weight N_k is "OR"ed with the function of the gate. If x_k is replaced by $\{x_k\}^r$ where each x_k^i has a weight N_k, the gate will function on $x_k^1 + x_k^2 + \cdots x_k^r$ in the same manner as on x_k. Thus the gate is only modified by adding additional inputs. In the type II realization the input x_j with weight N_j is "AND"ed with the function of the gate. If x_j is replaced by $\{x_j\}^r$ where each x_j^i has a weight N_j and $T_d' = T_d + N_j(r-1)$, the gate will operate on $x_j^1 x_j^2 . x_j^r$ as the non-redundant gate does on x_j. As an example for the type II realization, figure 12 shows a non-redundant gate realizing $x_j f$ and the redundancy modified gate realizing $x_j^1 x_j^2 x_j^3 f$ where $f = x_1x_2 + x_1x_3 + x_2x_3$.



Non-redundant gate

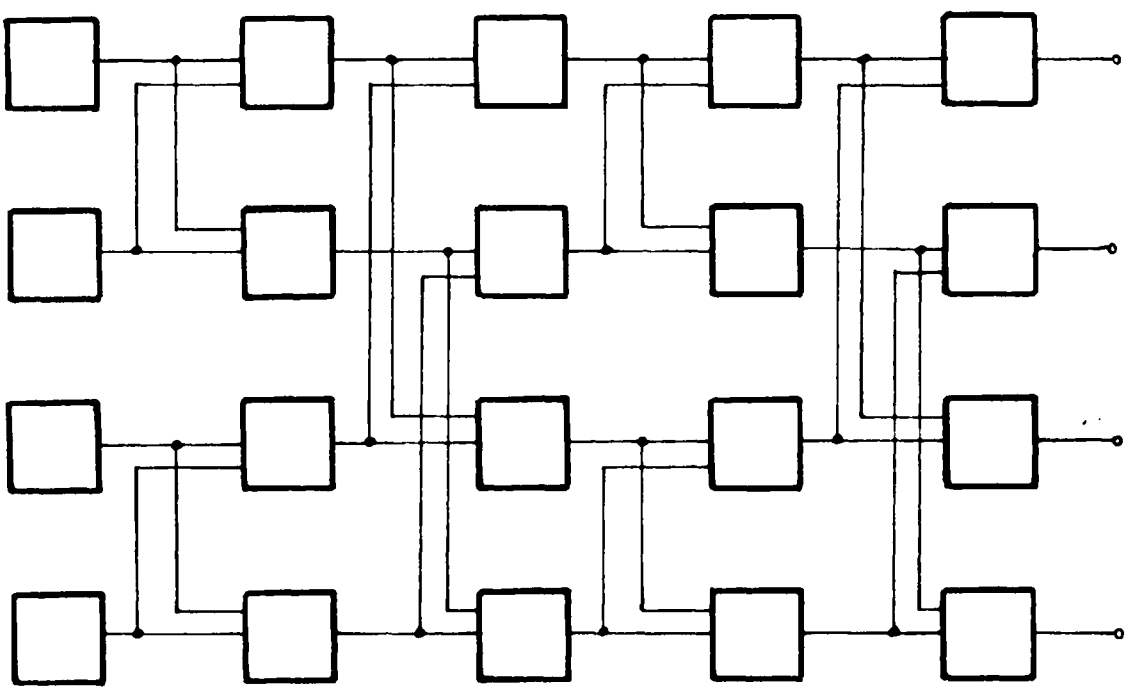


Redundancy modified gate

Non-redundant and redundant realization of $x_j f$

Figure 12

Now that the modifications have been established for the two types of realization, the remaining requirement is to provide the proper interconnections. Figure 13 shows a means of interconnecting four gates where r = 2 to have order of error correction E = 1. Although a critical error in one level corrupts two gates in the next level, the errors of these gates are subcritical in the following level due to inversion. Both subcritical errors are corrected by comparison with correct signals from other gates. Table 3 lists a possible set of interconnections for various orders of error correction where r = E + 1.



Gate interconnections for E = 1

Figure 13

Table 3

Possible grouping for E = 1, 2, and 3

Order of error correction	Redundancy	First layer	Second layer
1	4	$(1,2)(2,1)$ $(3,4)(4,3)$	$(1,3)(3,1)$ $(2,4)(4,2)$
2	9	$(1,2,3)_3^3$ $(4,5,6)_3^3$ $(7,8,9)^3$	$(1,4,7)_3^3$ $(2,5,8)_3^3$ $(3,6,9)^3$
3	16	$(1,2,3,4)_4^4$ $(5,6,7,8)_4^4$ $(9,10,11,12)_4^4$ $(13,14,15,16)^4$	$(1,5,9,13)_4^4$ $(2,6,10,14)_4^4$ $(3,7,11,15)_4^4$ $(4,8,12,16)^4$

The reliability of these circuits depends on the number of gates (E+1) that must be in error and the number of combinations of these errors that produce a circuit error. Any set of errors which causes an entire circuit to be in error is designated as uncorrectable. A set of uncorrectable errors can be generated all in one level or as a combination of critical errors in one level with subcritical errors in the next. An uncorrectable error is generated in one level by a critical error occuring in each grouping of by all gates of one grouping producing subcritical errors. A critical error in one level accompanied by subcritical errors in the next level generates a circuit error if the subcritical errors occur in the remaining gates of a grouping partially corrupted by the critical error.

The probability of a circuit error can be determined from the probabilities of the above errors occuring. The probability of a set of critical errors in one level generating a circuit error is designated

by $p_c(E)$ while that for subcritical errors in one level is denoted by $p_{sc}(E)$. The probability that a circuit error is generated by errors in two adjoining levels is designated as p2(E). These probabilities are listed in table 4 when the groupings are as listed in table 3. The probability of a critical error occuring is denoted by p_c while that of a subcritical error is denoted by p_{sc}. When the "AND" decision is used, $p_c = p_2$ and $p_{sc} = p_1$. If the "OR" decision is used, $p_c = p_1$ and $p_{sc} = p_2$. The probability of circuit error can be obtained from table 4 as:

$$p_e(E) = p_c(E) + p_{sc}(E) + p2(E) \qquad (20)$$

Table 4

Error probabilities for two layer error correction

Order of error correction	$p_c(E)$	$p_{sc}(E)$	p2(E)
1	$4p_c^2$	$2p_{sc}^2$	$8p_cp_{sc}$
2	$27p_c^3$	$3p_{sc}^3$	$81p_cp_{sc}^2 + 81p_c^2p_{sc}$
3	$256p_c^4$	$4p_{sc}^4$	$1024p_cp_{sc}^3 + 1536p_c^2p_{sc}^2 + 1024p_c^3p_{sc}$
E	$(E+1)^{E+1}p_c^{E+1}$	$(E+1)p_{sc}^{E+1}$	$(E+1)^{E+1}\left[\binom{E+1}{1}p_cp_{sc}^E + \cdots \binom{E+1}{E}p_c^Ep_{sc}\right]$

Since the coefficients (number of combinations) in table 4 increase rapidly with the greater error correction, it is obvious that this method of error correction is only useful for comparatively low redundancies. In fact when $(E+1)p_c$ approaches one, the greater redundancy only increases the chances of a circuit error.

The feature that makes this development most attractive is that tolerance and permanent errors are corrected equally well. The tolerance range for the functional nature of the modified gate is only moderately changed by the modifications. The change for a realization of the first type is dependent only on the zeros of $\{x_k\}^r$. The tolerance changes for a realization of the second type is dependent on fluctuations in the weights of $\{x_j\}^r$.

ALTERNATE CIRCUITS

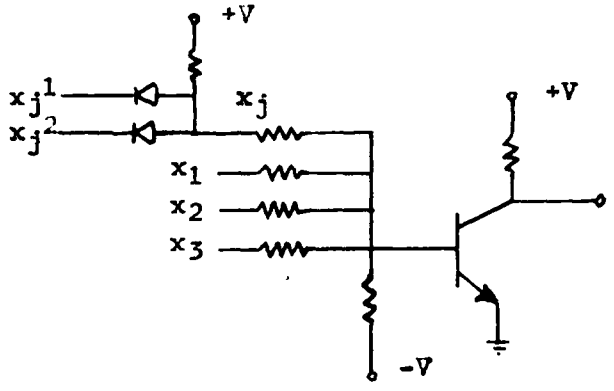
1. Interconnecting the gates in different manners can lower the reliability dependence on p_{sc} but increase the dependence on p_c. Since the dependence on p_c is already larger, this would not be desirable unless p_c is much smaller than p_{sc}. A set of groupings: (1,2)(2,3)(3,4)(4,1) for E = 1 eliminates the probability of two gates with subcritical errors generating a circuit error in one level. If no errors occur in the next level, three gates must have subcritical errors to cause a circuit error. Thus the circuit has an E = 2 for subcritical errors, but an E = 1 with more uncorrectable combinations for critical errors.

2. A given order of error correction can be achieved with less redundancy if more levels are used to correct errors (Pierce 1964). These methods have not been analyzed extensively, but the use of several levels to correct errors greatly increases the uncorrectable combinations. In this case the reliability for a given E would be smaller with less redundancy. However, if the probability of error is sufficiently small, this development could give a better reliability for a comparable redundancy.

3. As mentioned previously, the principal limitation in applying this method is that it can not be applied as developed to a general threshold circuit. It can be applied to a general circuit by making one of the two following modifications.

The first modification merely eliminates corrections where they can not be made. If a gate can not be modified to perform the desired decision, errors in the previous level are propagated through with no interconnections and corrected in a gate that can be properly modified. This is disadvantageous since the combinations of uncorrectable errors increases greatly with the number of levels between generation and correction of errors.

The second modification uses diode logic to perform the decisions while the threshold gate is unmodified. This is particularly attractive since decisions can be made on any number of the inputs. Thus any threshold circuit can be modified to correct errors on all inputs. Figure 14 shows a threshold gate where diode logic performs an "AND" decision on a set of two redundant inputs.



Threshold gate with diode logic performing "AND" decision

Figure 14

CHAPTER FOUR

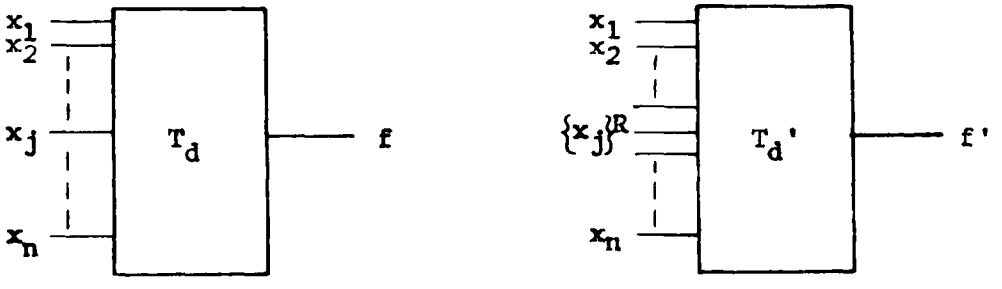
The method of error correction considered most in the literature involves generating a set of redundant signals and using a majority organ to determine the correct signal (Brown et al 1962, Knox-Seith 1964, Suran 1962, Pierce 1964). Although a properly functioning majority organ corrects all sets of E errors with a redundancy of 2E+1, they are special cases of threshold gates and therefore insert additional sources of error into the redundant circuit. A threshold gate can be modified to correct all sets of E errors on a set of R redundant inputs and maintain its functional nature. Even though R is generally greater than 2E + 1, this method of error correction is particularly applicable to threshold circuits since gates used solely for error correction are unnecessary.

This method corrects errors on a set of redundant inputs much the same as in the last development, except that all sets of E errors are corrected in one level. To eliminate the existence of critical errors, the decision uses a pseudo majority function. A gate modified to perform a decision on R redundant inputs considers the inputs to represent a "1" only if R - E or more of the inputs are "1". Similarly the modified gate considers the redundant inputs to represent a "0" only if R - E or more of the inputs are "0".

Although any gate realizing a linearly separable function can in theory be modified to incorporate the decision, the development is limited

in that the necessary R to correct E errors depends on the non-redundant function. If the function to be modified is quite complex, R may be prohibitively large.

An input x_j with a weight N_j is to be replaced by a set of inputs $\{x_j\}^R$ with weights N_j'. The modified function f' is to operate on R - E or more of the $\{x_j\}^R$ in the same manner as f operates on x_j. To do this a T_d' must separate f' as T_d separates f. Figure 15 indicates the nature of the error correction. The function f' represents the same information as f, but uses R - E of the $\{x_j\}^R$ to obtain it.



Non-redundant gate Redundant gate

Non-redundant and redundancy modified gate
Figure 15

The proof of theorem 3 requires the use of the following parameters of f:

Define M_1 as the maximum of $\sum_{i=1,i\neq j}^{n} N_i x_i \Big|_{f=0,x_j=1}$,

Define M_0 as the maximum of $\sum_{i=1,i\neq j}^{n} N_i x_i \Big|_{f=0,x_j=0}$

Define m_1 as the minimum of $\sum_{i=1,i\neq j}^{n} N_i x_i \Big|_{f=1,x_j=1}$

Define m_0 as the minimum of $\sum_{i\neq j,\, i=1}^{n} N_i x_i \Big|_{f=1, x_j=0}$

Notice that M_1 does not exist if N_j is greater than N_t and m_0 does not exist if $W - N_j$ is less than N_t. Otherwise it can be seen from the definitions that $M_0 = N_j + M_1$ and $m_0 = N_j + m_1$.

In the development it is assumed that the members of $\{N\}$ are integers the smallest of which is 1. This leads to the relations that $M_1 + 1 = m_1$ and $M_0 + 1 = m_0$.

Theorem 3 Any linearly separable function of the variables $\{X\} = \{x_1, \cdots x_j, \cdots x_n\}$ with weights $\{N\}$ can be modified to correct all sets of E errors in R versions of the variable x_j if and only if

$$R > E(N_j+1) \tag{21}$$

Proof: It will be shown that as long as R satisfies (21), an N_t' and an N_j' exist such that N_t' separates f' as desired.

From the four definitions the following relations must hold if f' is to be realized for all sets of E or less errors:

$$RN_j' + M_1 < N_t' \tag{22}$$

$$EN_j' + M_0 < N_t' \tag{23}$$

$$(R-E)N_j' + m_1 > N_t' \tag{24}$$

$$m_0 < N_t' \tag{25}$$

The first two conditions represent the maximum input when f' = "0". The second two conditions represent the minimum input when f' = "1".

Examining the second condition shows that $EN_j' < 1$ since $M_0 + 1 > N_t'$. Comparing the second and third inequalities establishes the necessary condition on R.

$$(R-E)N_j' + m_1 > M_0 + EN_j'$$

$$RN_j' > M_0 - m_1 + 2EN_j'$$

$$R > E(M_0-m_1+2) \qquad \text{because } 1/N_j' > E$$

$$> E(N_j+1)$$

Once a value for R satisfying (21) has been determined, some leeway is allowed in choosing values for N_j' and N_t'. The range of values for N_j' can be determined from:

$$(N_j-1)/(R-2E) < N_j' < N_j/(R-E) \tag{26}$$

To show that an N_j' satisfying (26) exists, the upper bound is established as being strictly greater than the lower bound.

From (21) $R > E(N_j+1)$

$$R - 2E > E(N_j-1)$$

$$R - 2E + (R-2E)(N_j-1) > E(N_j-1) + (R-2E)(N_j-1)$$

$$(R-2E)N_j > (R-E)(N_j-1)$$

$$N_j/(R-E) > (N_j-1)/(R-2E)$$

The range of values from which N_t' can be selected is given by (23) and (24) as:

$$EN_j' + M_0 < N_t' < (R-E)N_j' + m_1 \tag{27}$$

N_t' exists since the lower bound of N_j' in (26) establishes the upper bound of N_t' to be strictly greater than the lower bound of N_t'.

The conditions of (23) and (24) have been satisfied by establishing (27). Establishing (27) and the upper bound of (26) has satisfied the conditions of (22) and (25). Thus the necessary requirements of f' have been satisfied and the theorem is proved.

The permissible range of values for N_t' given by (27) shows that the choice of a T_d' is more restricted than a choice of T_d. When minimal redundancy is used, T_d' is in general greater than T_d (assuming the latter to be in the middle of its tolerance range). Thus the redundancy modification has changed the error distribution.

A second development is now presented which is desirable in that it allows the designed threshold to remain unchanged through the application of the redundancy modifications. Although more redundancy is needed, this development allows a gate to maintain the non-redundant tolerance range when all gates in the previous level are correct. The necessary condition is:

$$EN_j' + M_0 < N_t \tag{28}$$

When $N_t = M_0 + 1/2$, this requires $EN_j' < 1/2$.

The necessary condition of R now becomes:

$$R > 2EN_j \tag{29}$$

When R satisfies (29), the weights of $\{x_j\}^R$ can be chosen as:

$$N_j' = N_j/R \tag{30}$$

Under the conditions of (29) and (30) if each x_j^i represents the correct signal, the input to the modified gate is the same as that to a non-redundant gate. When a number of errors less than E + 1 are present, the tolerance range of $T_d' = T_d$ is smaller than that for a non-redundant gate. This smaller range is referred to as the correction tolerance range.

Establishing the four conditions (22),(23),(24), and (25) to be satisfied indicates the tolerance range for correction in relation to that for functioning on no errors.

$$RN_j' + M_1 < EN_j' + M_0 < T_d < (R-E)N_j' + m_1 < m_0 \qquad (31)$$

$RN_j' + M_1 < EN_j' + M_0$ because $RN_j' + M_1 = M_0$

$EN_j' + M_0 < T_d < (R-E)N_j' + m_1$ satisfied by (29)

$(R-E)N_j' + m_1 < m_0$ because $RN_j' + m_1 = m_0$

The relations in (31) show the tolerance range for correction is the non-redundant functional tolerance range reduced by $2EN_j'$. Since N_j' can be made smaller by increasing R, the correction tolerance range can be increased. Although the greater redundancy increases the reliability of making the correction, the errors are more likely to occur. Thus increasing R to larger and larger values gives diminishing returns in reliability.

Whether or not these developments are useful depends on the particular function modified and the significance of x_j in the function. When N_j is necessarily large, (21) and (29) indicate a large redundancy is required to achieve a relatively small order of error correction. Since the greater redundancy also allows more gates to be in error, the reliability decreases when N_j increases. Table 5 lists the minimum redundancy for various orders of error correction. The redundancies are listed in terms of a parameter Q equal to $N_j + 1$ in the first development and $2N_j$ in the second development. The odd columns do not apply to the second development since N_j is an integral value.

Table 5

Minimum redundancy for
correction of E errors

	Q					
E	2	3	4	5	6	7
1	3	4	5	6	7	8
2	5	7	9	11	13	15
3	7	10	13	16	19	22
4	9	13	17	21	25	29
5	11	16	21	26	31	36

If a set of E + 1 errors occur, a properly functioning gate modified to correct all sets of E errors will produce an erroneous output (assuming certain input conditions are present). A set of E + 1 errors is therefore designated as uncorrectable. The probability of a set of E + 1 errors occuring is the individual error probability raised to the E + 1 power. Since the number of ways these errors can occur is $C(E) = \binom{R}{E+1}$, the probability of uncorrectable errors occuring is:

$$p_e(E) = C(E)p_1^{E+1} + C(E)p_2^{E+1} \tag{32}$$

Table 6 lists the number of combinations C(E) for the orders of error correction and values of Q listed in table 5. The redundancies used to determine C(E) are the minimal values listed in table 5.

Examination of table 6 shows the reliability improvment for increasing E is also quite dependent on Q. Theorem 4 establishes the bounds on p_e if a circuit for order of error correction E + 1 is to be more reliable than one for E.

Table 6

Combinations of critical errors
for minimum redundancy

E	2	3	4	5	6	7
1	3	6	10	15	21	28
2	10	35	84	165	286	455
3	35	210	715	1820	3876	7315
4	126	1287	6188	20349	53130	
5	462	8008				

Theorem 4 If p_1 and p_2 are sufficiently small, the probability of uncorrectable errors occuring in one level can be made arbitrarily small by modifying the gates in the next level to correct for a large enough number of errors.

Proof: The proof will follow the one given for theorem 2 by showing that $p_e(E+1)$ is less than $p_e(E)$ for large E and sufficiently small p_1 and p_2. Since the error probabilities are symmetric, the proof considers only p_1 and the same results apply to p_2.

The minimum redundancy for order of error correction E is EQ + 1. $Q = N_j + 1$ for the first development and $2N_j$ for the second.

$$\frac{p_1(E+1)}{p_1(E)} = \frac{C(E+1){p_1}^{E+1}}{C(E){p_1}^{E}}$$

$$= \frac{\binom{EQ+Q+1}{E+2}}{\binom{EQ+1}{E+1}} p_1$$

$$= \frac{(EQ+Q+1)!(EQ-E)!(E+1)!}{(EQ+1)!(EQ+Q-E-1)!(E+2)!}$$

$$= \frac{(EQ+Q+1)(EQ+Q) \cdots (EQ+2)}{[E(Q-1)+Q-1] \cdots [E(Q-1)+1]\ (E+2)} p_1$$

$$= \frac{(EQ)^Q + a_1 E^{Q-1} + \cdots a_Q}{E[E(Q-1)]^{Q-1} + b_1 E^{Q-1} + \cdots b_Q} p_1$$

$$\lim_{E\to\infty} \frac{p_1(E+1)}{p_1(E)} = \frac{Q^Q}{(Q-1)^{Q-1}} p_1$$

$$< 1 \qquad \text{if } p_1 < \frac{(Q-1)^{Q-1}}{Q^Q} \tag{33}$$

Thus the theorem is proved for p_1 and p_2 satisfying (33). The upper bound on p_1 and p_2 is an ever decreasing function of Q. Therefore given a minimum p_1 and p_2, only certain functions can be modified to arbitrarily correct errors in the previous level (so far it has been assumed that this correction can be accomplished with sufficient reliability).

The previous section has considered the probability of a redundant level generating a set of errors that can not be corrected by an arbitrarily reliable gate. A reliability analysis of these circuits must also consider the probability that a correctable set of errors will in fact be corrected. The next section considers the probability of correctable errors not being corrected when the second development is used.

The modifications of the second development have been designed to maintain the non-redundant tolerance range t if no errors are made. If a number of errors v less than E occur, the tolerance range t_v for correction is $t - 2vN_j'$. That is, whenever $T < M_0 + vN_j'$ or $T > m_1 - vN_j'$, the gate is in a functional state capable of producing an error.

The probability $p_1(E)'$ of a gate producing a type one error when a correction should be made can now be expressed as the sum of probabilities:

$$p_1(E)' = p(1\ e_1)P(M_0<T<M_0+N_j') + p(2\ e_1)P(M_0<T<M_0+2N_j') + \cdots$$
$$p(E\ e_1)P(M_0<T<M_0+EN_j') \qquad (34)$$

Similarly the probability of a type two error occuring when a correction should be made can be expressed by:

$$p_2(E)' = p(1\ e_2)P(m_1-N_j'<T<m_1) + p(2\ e_2)P(m_1-2N_j'<T<m_1) + \cdots$$
$$p(E\ e_2)P(m_1-EN_j'<T<m_1) \qquad (35)$$

From (32), (34), and (35) the total error probability of the modified gates can be expressed as:

$$p_e(E)' = p_e(E) + p_1(E)' + p_2(E)' \qquad (36)$$

An analysis of $p_e(E)'$ from equations (34) and (35) is quite involved and requires a knowledge of P(T). If $P(T\subset t_0) = P(T\subset t_1) = \cdots P(T\subset t_E)$, $p_e(E)'$ reduces to $p_e(E)$. Since this assumption is valid when only permanent errors are significant (i.e. $p_1 = p_s$ and $p_2 = p_o$), theorem 4 indicates that the effects of permanent errors can be arbitrarily minimized.

If $P(T\subset t_v)$ for v greater than 0 is much smaller than $P(T\subset t_0)$, equations (34) and (35) indicate that the redundant circuit reliability can be less than that of a non-redundant circuit. If a normal distribution is assumed for P(T), numerical comparisons can be made between redundant and non-redundant circuit reliabilities. As a simple example for $E = 1$ and $N_j = 3$, a modified gate uses $R = 7$ and $N_j' = 3/7$.

If $P(T<1) = .93$, $P(T<1/7) = .26$ and the reliability is .95. Thus the redundant circuit is less reliable than the non-redundant one. This indicates that this method is not useful for strictly tolerance error correction, since the correction is strongly dependent on tolerances.

In general t_E is inversely dependent on E causing the probability of correction to become smaller with increasing E. If $R = 2EN_j'$, however, $N_j'E = N_j/(2N_j'+1)$ and is invariant under E. Although this requires more than minimal redundancy, it shows that any order of error correction can be achieved with a specified tolerance range.

The developments have shown that these methods of error correction can be applied to one input of any threshold gate. It is quite simple to extend the last development to any number of inputs by applying it to each input separately while assuming the other inputs to be correct. Since a correct set of redundant inputs has the same weight as the non-redundant input it replaced, the order of application is immaterial. If the gate is designed to correct E errors on more than one set of redundant inputs, it can only correct for E errors on one set at a time. It will, however, correct all sets of E errors distributed throughout the sets of redundant inputs as shown in the following theorem.

Theorem 5 A threshold function with variables $\{X\}$ having weights $\{N\}$ can be modified to correct any set of E errors among the sets of redundant variables $\{x_1\}^{R1} \cdots \{x_i\}^{Ri} \cdots \{x_n\}^{Rn}$ where each R_i is sufficient to allow correction of E errors in the set $\{x_i\}^{Ri}$ (R_i must satisfy (29)).

Proof: A function modified to correct E errors on a variable $\{x_i\}$ is designed to overlook fluctuations of a magnitude equal to EN_i'. Of all the sets of redundant variables $\{x_i\}^{Ri}$, there is at least one $\{x_j\}^{Rj}$ such that $N_j' \geq N_i'$ for all i. The function has therefore been modified to overlook fluctuations equal to EN_j'. Since among the sets of redundant variables, any other combination of E weights can at most equal EN_j', and the theorem is proved.

CHAPTER FIVE

The reliability analyses have indicated that each method has some relative advantages and disadvantages. Certain assumptions were made when the reliability of each method was determined, which must be kept in mind when any two methods are compared.

Since the error correcting ability of the last method is more strongly dependent on tolerance variations, a comparison between its reliability and that of the first two is difficult. The second and third methods can be compared for strong permanent error effects, if the latter is designed so as not to affect the functional tolerance range. This is justified under the assumption that the effect of a redundancy modification in the second method is comparable to the probability that correctable errors in the third method aren't corrected. Without knowing the effect of tolerance variations on the error correcting ability of the third method, it can't be compared to the first since the latter only corrects tolerance variations.

The first and second methods are easily compared for tolerance error correction since they have similar modifications and the same redundancy for a given E.

When two methods are compared, the significant factors are the reliability and the redundancy used to obtain the reliability. To make a comparison on this basis a figure of merit is established as the product of the error probability and the redundancy. The figures of merit for various E can be determined from the error probabilities and the

necessary redundancies given in the developments. If the error probabilities p_1 and p_2 equal $p_e/2$, the figure of merit for a given E has the form: $C_M p_e^{E+1}$. Assuming the p_e for each development to be the same makes the coefficient C_M the significant factor in determining the relative merits of each method. Table 7 lists the values of C_M for each development and various orders of error correction. The third method lists the values of C_M for the second development, that doesn't alter the functional tolerance range.

Table 7

Relative merits of each method as expressed by the coefficient C_M

E	1st Method	2nd Method	3rd Method		
			N_j = 1	2	3
1	6	14	4.5	25	73.5
2	22.5	216	12.5	189	930
3	70	3844	30.6	1160	9170
4	197	75600	70.9	6570	83000

Table 7 indicates the first method corrects tolerance variations more efficiently than the other two. Even in the third method where $N_j = 1$, this is probably true since the effect of tolerance variations on error correction has not been considered. It is necessary to remember that the first method's reliability is determined assuming a negligible effect from permanent errors.

If permanent errors are sufficiently significant, either of the last two methods must be used. Table 7 indicates the third method is

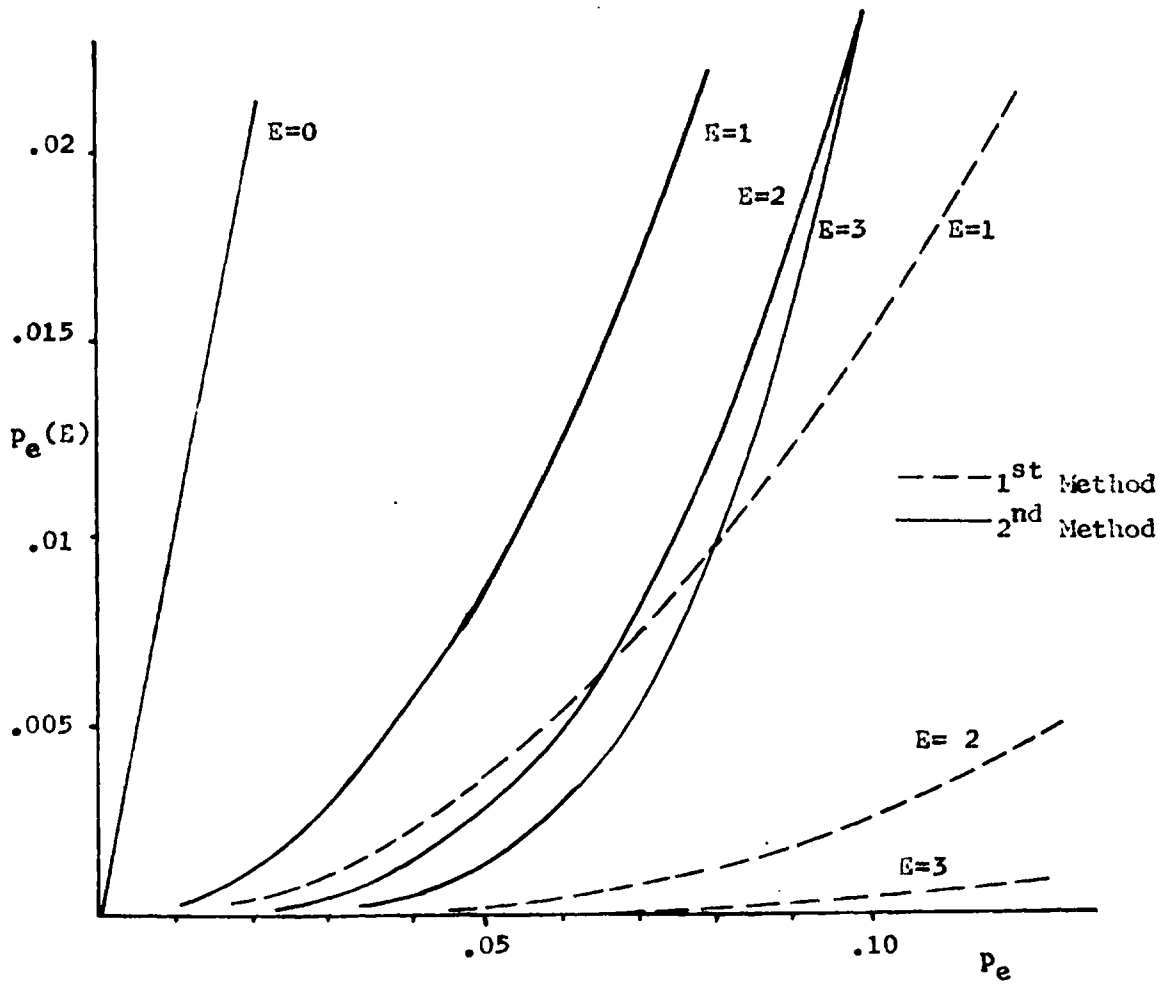
best for small values of N_j, but its attraction decreases rapidly with larger values of N_j. It should also be remembered that the second method must either be limited to certain functions or use diode logic to make the corrections. Table 7 indicates that the third method is eventually better than the second for ever increasing orders of error correction regardless of N_j.

If only permanent errors are significant, the third method can achieve the same order of error correction with much less redundancy. This, as is shown in theorem 4, indicates the third method is generally best for strictly permanent error correction.

As another comparison the error probabilities given in the developments are plotted (assuming $p_1 = p_2 = p_e/2$) in figures 16 and 17 for various orders of error correction. This enables one to determine the E and therefore the necessary redundancy for each development when a certain error probability is desired. Again only the first and second, and the second and third methods are compared with each other.

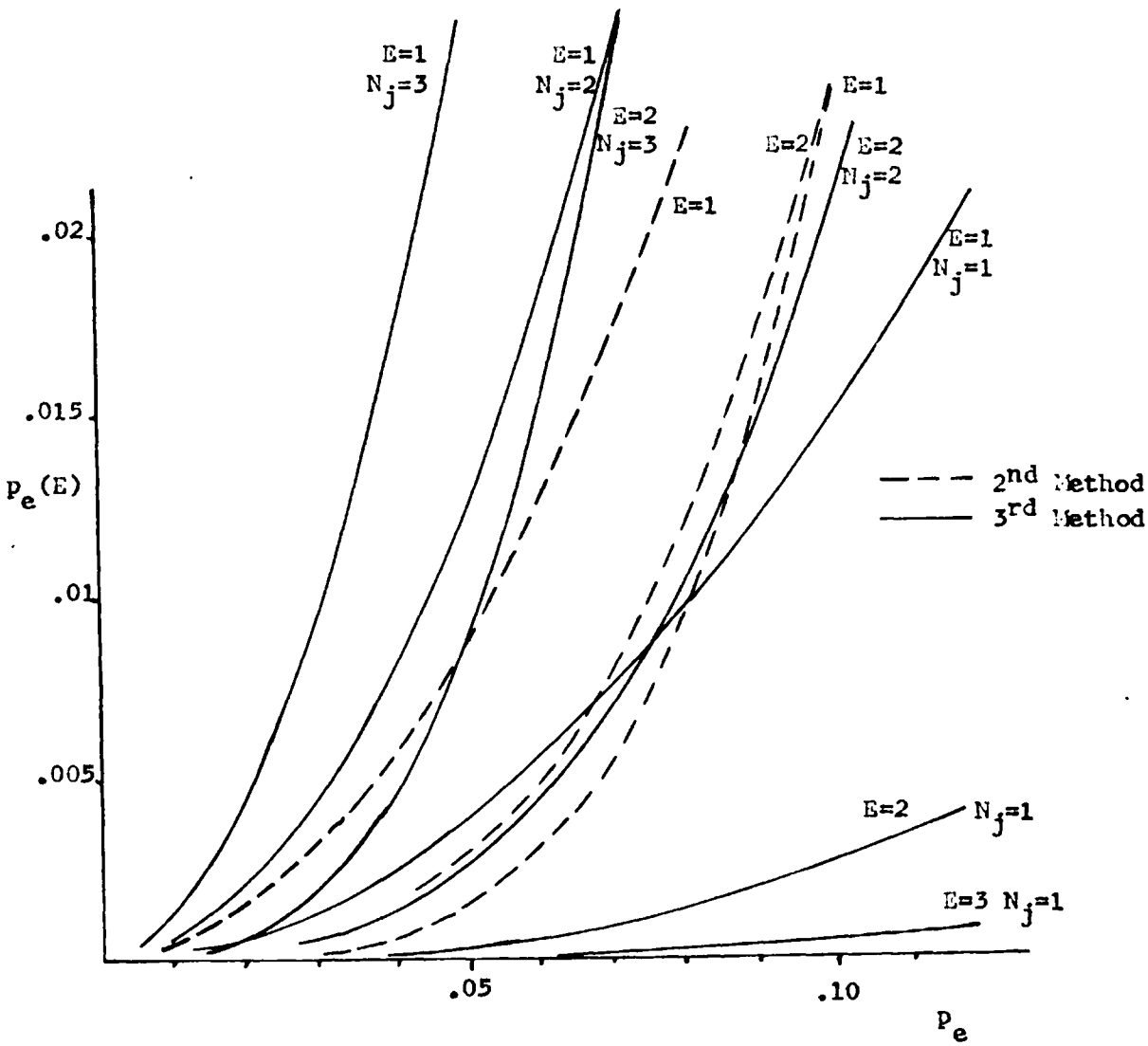
In a computer using redundant circuits it may be desirable to examine the particular elements and eliminate bad ones. In an application such as this it is advantageous to eliminate gates without having to modify the remaining gates. An important factor in determining which method should be used is the effect the degree of redundancy has on the modifications. If the redundancy modifications are independent of R, a circuit with a high order of error correction can be easily modified to a circuit with a lower order of error correction. The first method has just this property. A bad gate can be bypassed without making

modifications on the other gates. The second method may require only small gate modifications, particularly in a type I realization, but needs different interconnections for different values of E. The third method requires major modifications and therefore would not be too useful in such an application.



Error probabilities for the first and second methods

Figure 16



Error probabilities for the second and third methods

Figure 17

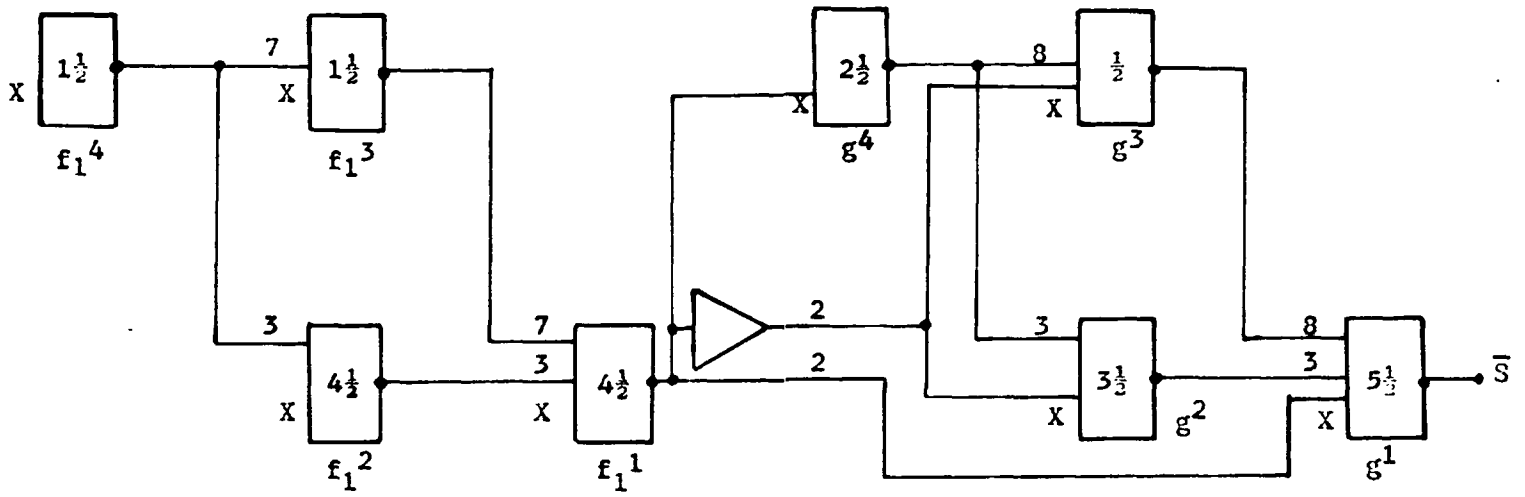
CHAPTER SIX

The first example application will be to apply single error correction to the adder realization presented in the first chapter. The first and third methods apply error correction to the third realization in figure 7. The second method could have been applied to the circuit if diode logic performed the error correction. However, it was concluded that the type II realization in figure 6 represented a more typical application.

The gate generating f_1 of figure 7 has a designed threshold $T_d = 1\frac{1}{2}$ and a $W = 3$. To apply the first method the values for N_{y1} and N_{y2} are nominally set at 3 and 7 respectively. This requires $T_d' = 1\frac{1}{2} + 3 = 4\frac{1}{2}$. The gate generating g_1 and g_0 has a designed threshold $T_d = 2\frac{1}{2}$ and a $W = 3$. In this case the values for N_{y1} and N_{y2} are set at 3 and 8 respectively to give the modified gates the same tolerance range for both functions. Thus $T_d' = 2\frac{1}{2} + 3 = 5\frac{1}{2}$.

Since inverting gates are used, the even level gates must generate their negated functions. For f_1 this requires a $\overline{T}_d = 3 - 1\frac{1}{2} = 1\frac{1}{2}$ and a $\overline{T}_d' = 3 + 1\frac{1}{2} = 4\frac{1}{2}$. For g_1 and g_0 $\overline{T}_d = 3 - 2\frac{1}{2} = \frac{1}{2}$ and $\overline{T}_d' = 3 + \frac{1}{2} = 3\frac{1}{2}$.

The redundant circuit realized by the above modifications is given in figure 18. If permanent errors are negligible, the error probability of the redundant adder is: $2(3)(p_1^2+p_2^2) = 3p_e^2$ when $p_1 = p_2$. This should be compared to $2p_e$ for the non-redundant adder.



$g = g_1, g_0$

Application of first method to
adder of figure 7

figure 18

The application of the third method involves duplicating the gates of the first level enough times to allow single error correction by gates in the second level. The gate generating g_1 and g_0 has $N_j = 2$, $M_1 = 0$, $M_0 = 2$, $m_1 = 1$, and $m_0 = 3$. When minimum redundancy is desired in the first level, R can be determined from (21) as 4. The range of values for N_j' can be determined from (26) as: $1/2 < N_j' < 2/3$. If N_j' is chosen as 5/8, the range of values for N_t' can be determined from (27) as: $2+5/8 < N_t' < 2+7/8$. If the designed threshold of a modified gate is placed in the middle of the correction tolerance range, $T_d' = 2+3/4$.

The redundancy of the output gate depends on the function it drives. If it drives an inverter to obtain S, it must be duplicated 3 times. The circuit in figure 19 shows this case where the redundancy modified inverter uses $R = 3$, $N_j' = 1/3$, and $T_d' = T_d = 1/2$.

The probability of uncorrectable errors occuring in the first level is $6(p_1^2+p_2^2) = 3p_e^2$ if $p_1 = p_2$. If the gates of the first level are correct, the probability of error occuring in the second level is: $3\,P(T<2+1/4)^2 + 3\,P(T>3)^2$. Thus the functional tolerance range has been narrowed by a factor of 3/4 through the redundancy modification. When the distribution P(T) is unknown, the redundant circuit reliability can not be related to the non-redundant circuit reliability.

If the second development of chapter four is used to apply redundancy to this circuit, the designed threshold and the functional tolerance range are unaltered. The necessary redundancy from (29) is 5, N_j' from (30) is 2/5, and $T_d' = T_d = 2+1/2$. The circuit realized

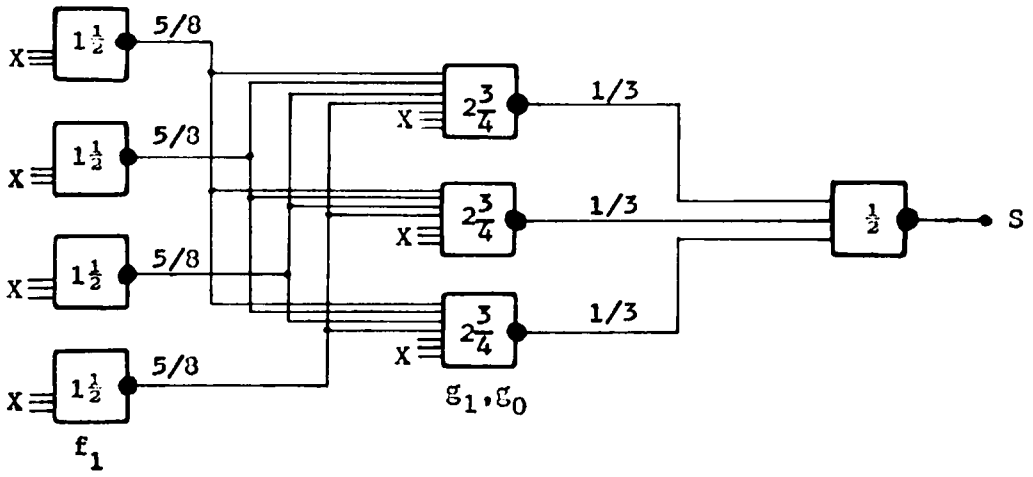
with these modifications is shown in figure 20.

In this case the probability of uncorrectable errors occurring in the first level is: $10(p_1^2+p_2^2) = 5p_e^2$ if $p_1 = p_2$. If no errors occur in the first level, the probability of uncorrectable errors occurring in the second level is $3(p_1^2+p_2^2) = 3/2p_e^2$.

The application of the redundancy modifications to the inverter have indicated that the liberal use of inverters in the non-redundant design greatly facilitate error correction. Since they require only a majority of correct inputs to produce a correct output and the functional tolerance range is unchanged, they provide the most efficient corrections. A non-redundant inverter can be considered to produce errors only of a permanent nature. The assumption that correctable errors are corrected by a redundancy modified inverter is then justified for low values of E. This indicates the third method is generally best for all types of error correction when the inverter is used as a restoring organ.

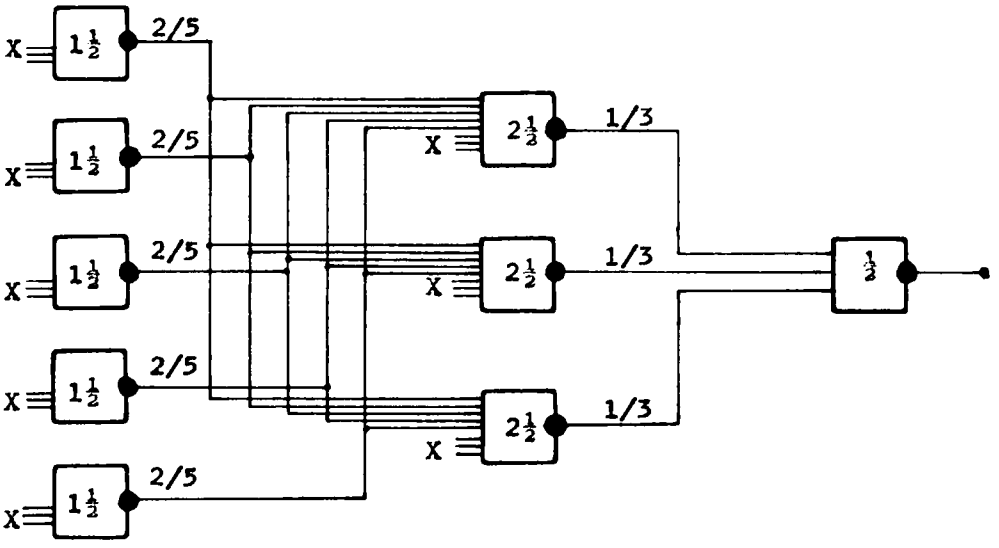
The second method is used to correct errors in the circuit of figure 6. The modifications consist only of making $T_d' = T_d + N_o$. The level generating g_1 has gates with modified threshold $T_d' = 7/2 + 3 = 6+1/2$. The gates in the second level have a $T_d' = 7/2 + 2 = 5+1/2$. Figure 21 shows the circuit for single error correction.

If the output gates are assumed to drive other similar error correcting gates, the reliability for each level as determined from table 4 is: $4p_2^2 + 2p_1^2 + 8p_1p_2 = 7p_e^2$ if $p_1 = p_2$.



Application of third method to
adder of figure 7

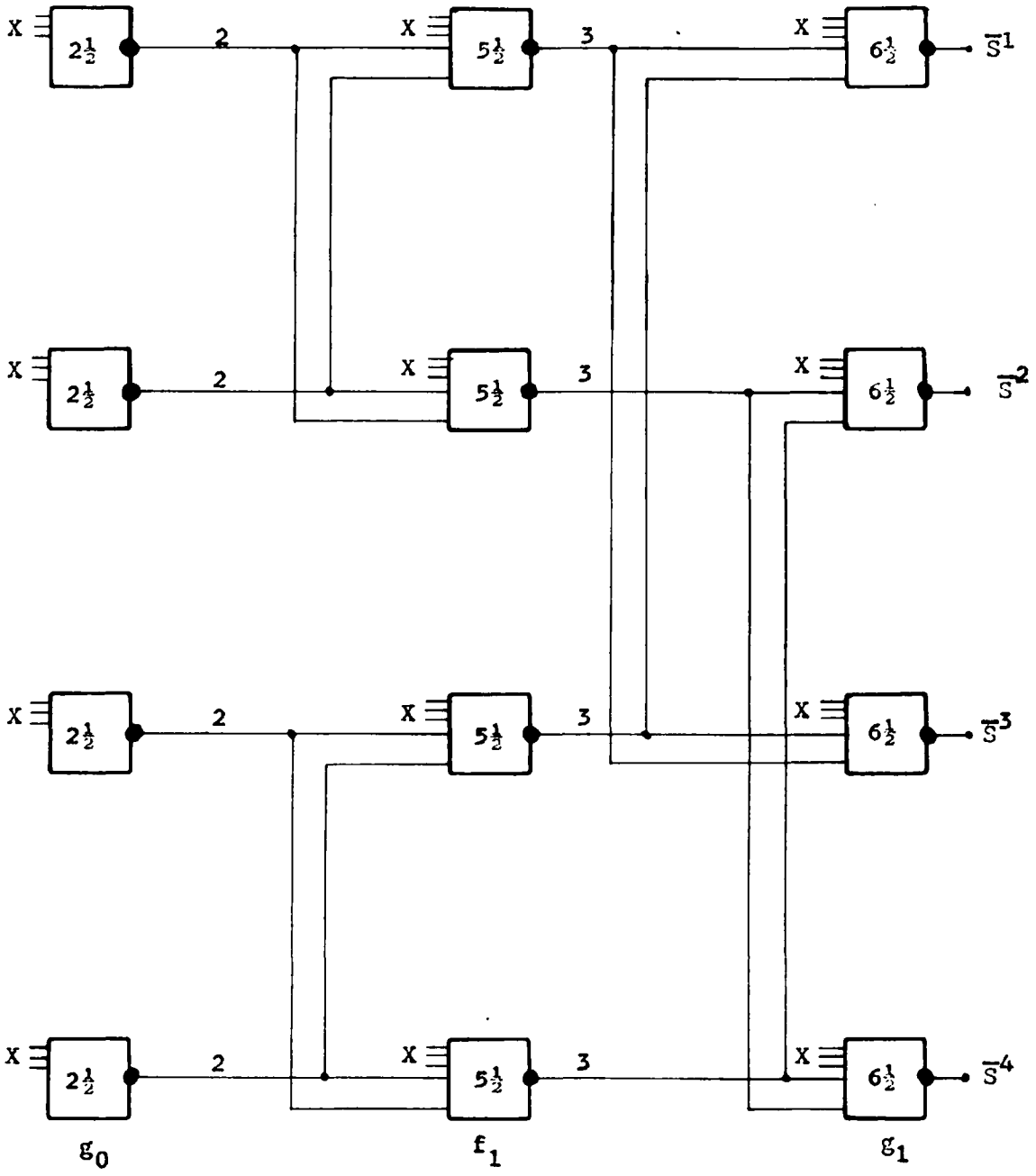
Figure 19



Application of third method to
adder of figure 7

(second development)

Figure 20



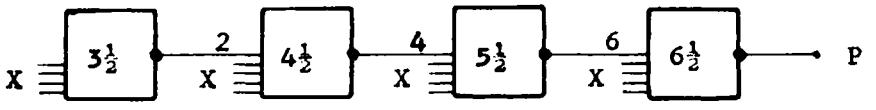
Application of second method
to adder of figure 6

Figure 21

As another example, redundancy is applied to a seven bit parity checker. A realization using the combined type I and II methods mentioned in the first chapter is given in figure 22. Although this realization is not minimal, it has the desirable property that each gate need only correct errors on a single input.[5]

The redundant circuit of figure 23 uses a hybrid application of the second and third methods. The third method is used to correct errors in the first level since a redundancy of only four is needed. Examinations of the functions in the third and fourth levels reveal that redundancies of six and eight are needed in the second and third levels respectively. Since the second method appears better in these cases it is used. This method must, however, use diode logic to make the corrections. A strictly type I or type II realization requires seven nonredundant gates and therefore would not be advantageous in allowing gate correction instead of diode correction.

In the second level $N_j = 2$, $M_1 = 2$, $M_0 = 4$, $m_1 = 3$, and $m_0 = 5$. The modifications are now determined as: $R = 4$, $N_j' = 5/8$, and $T_d' = 4+3/4$.



Seven bit parity checker

Figure 22

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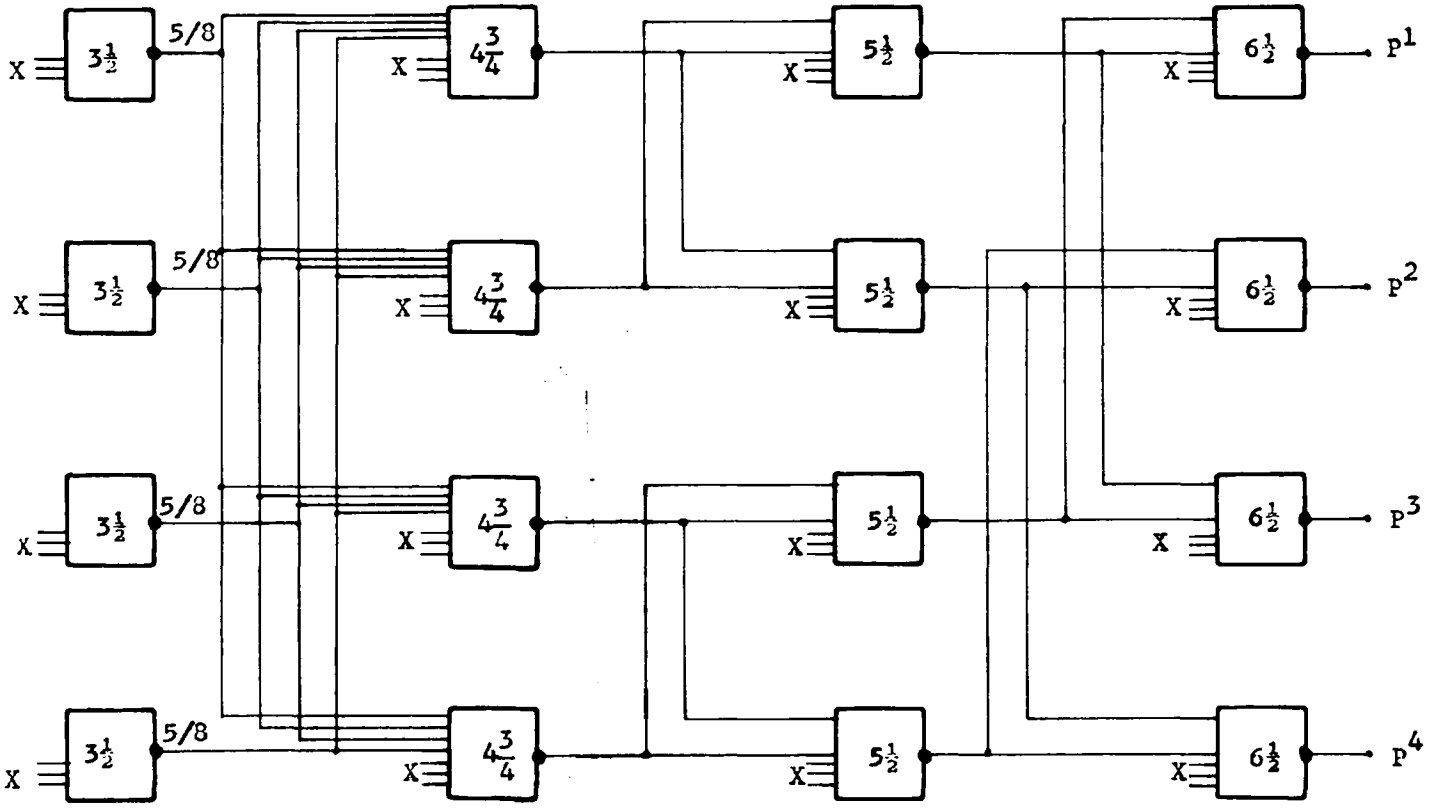
5. A minimal 7 bit parity checker requires only 3 gates (Kautz 1961).



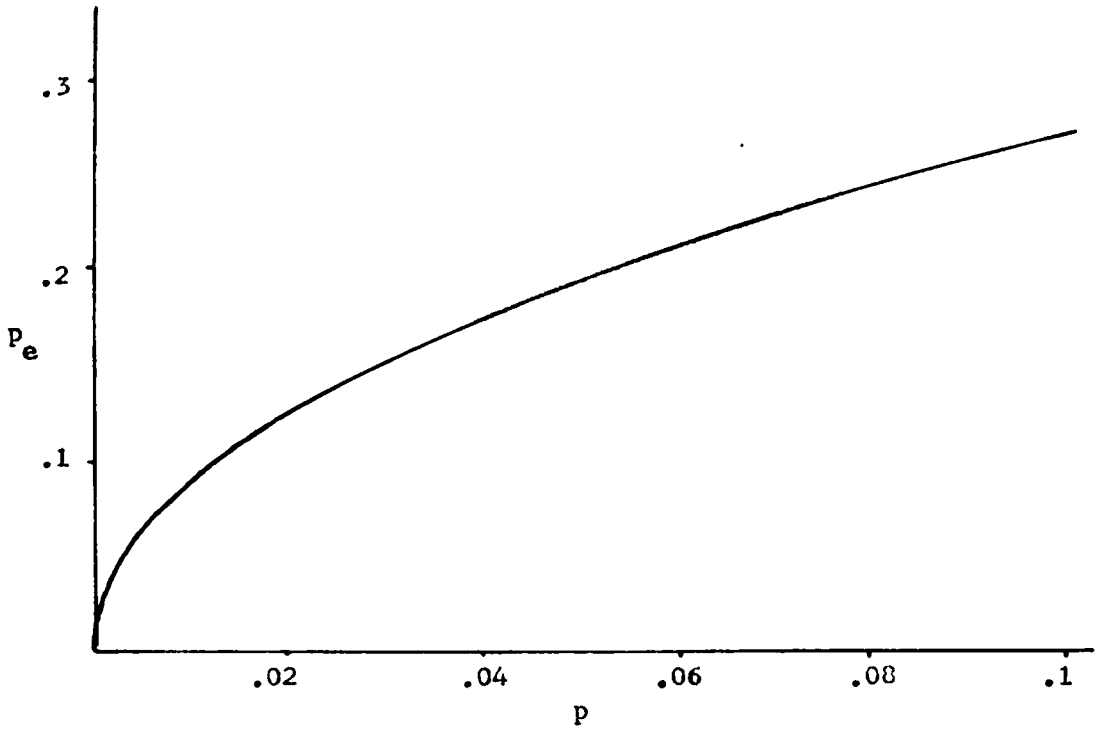
Hybrid application of
redundancy to parity checker

Figure 23

The error probabilities of each level as listed in the developments are: $3p_e^2$ in the first level (assuming correctable errors are corrected) and $7p_e^2$ in each of the remaining levels. If p_e is small, the probability of a circuit error can now be expressed as $24p_e^2$.

A non-redundant parity checker using six exclusive "OR" blocks with three gates in each requires 18 gates. Thus a conventional element realization requires even more gates than the redundant threshold gate realization. If the probability of a conventional gate error is p, the circuit error probability is $1 - (1-p)^{18}$ which is essentially 18p for small p. Comparing this to the circuit error probability of the redundant threshold realization indicates that the latter is smaller if p_e is less than $(3/4)^{\frac{1}{2}}$. Figure 24 is a plot of the maximum p_e for which the redundant threshold circuit is more reliable than the conventional realization. The curve indicates that p_e need not be very small to make the threshold circuit substantially more reliable.

If the parity checker is modified for error correction by the first method the probability of a circuit error is $12p_e^2$. Thus if tolerance errors are dominant, the parity checker can be made even more reliable. Although in this case the reliability would not compare as favorably to conventional circuitry, since tolerance variations are primarily characteristic of threshold devices.



Maximum p_e of threshold gates vs: error probability p of conventional gates

Figure 24

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