PLANAR UNIJUNCTION TRANSISTORS FOR A NEURISTOR REALIZATION

by

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A Thesis Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL ENGINEERING

In Partial Fulfillment of the Requirements
For the Degree of

MASTER OF SCIENCE

In the Graduate College

THE UNIVERSITY OF ARIZONA

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STATEMENT OF AUTHOR

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ACKNOWLEDGMENTS

The author wishes to thank his advisor, Dr. Roy H. Mattson, for his continued guidance, encouragement, and time while this thesis was being prepared.

The author also wishes to express his appreciation to Dr. Victor W. Bolie for his suggestions and encouragement during the preliminary work on the thesis topic; to all those associated with the Solid State Engineering Laboratory at The University of Arizona for help and guidance with the fabrication processes; and to Mrs. Freida H. Long for typing and proofreading the manuscript.

Finally, the author wishes to express his gratitude to his wife, Gayla, for typing the preliminary copies of the thesis and for her continued assistance and understanding during the entire time of the preparation of the thesis.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS--Continued

LIST OF TABLES

ABSTRACT

This work explains the design and fabrication of a unijunction transistor for the realization of a neuristor line in integrated circuit form. The unijunction transistor is designed and constructed in a manner that permits the realization of the neuristor line in a simple and practical manner.

An existing theoretical model of the unijunction transistor is adapted to the design geometry used in this work, and this model is implemented as an engineering design aid. It is also used to predict the characteristics of a particular unijunction transistor design.

This study emphasizes the fabrication techniques that were used for the physical construction of the unijunction transistor.

Chapter 1

INTRODUCTION

The Neuristor

A device called a neuristor has been defined by H. D. Crane (1960) as "a device having the form of a one-dimensional channel along which signals may flow, the signals taking the form of propagating discharges having the following properties:

1. Threshold stimulability
2. Uniform velocity of propagation
3. Attenuationless propagation
4. Refractory period following the passage of a discharge, after which the neuristor can again support a discharge."

The action of a neuristor can be compared to the burning of a chemical fuze. It is threshold stimulable (it must be ignited), it has a uniform velocity of propagation (it burns at a uniform rate), and it has attenuationless propagation (it continues burning with the same intensity for the entire length of the fuze). However, a fuze cannot again support combustion, as the neuristor must again support a discharge. In a sense, a fuze has an infinite refractory period, while the neuristor must have a finite refractory period.

Crane explains that by various interconnections of neuristors, Boolean logic functions and memory functions can be realized. Thus, it is possible to build entire electronic digital computers using only neuristors.

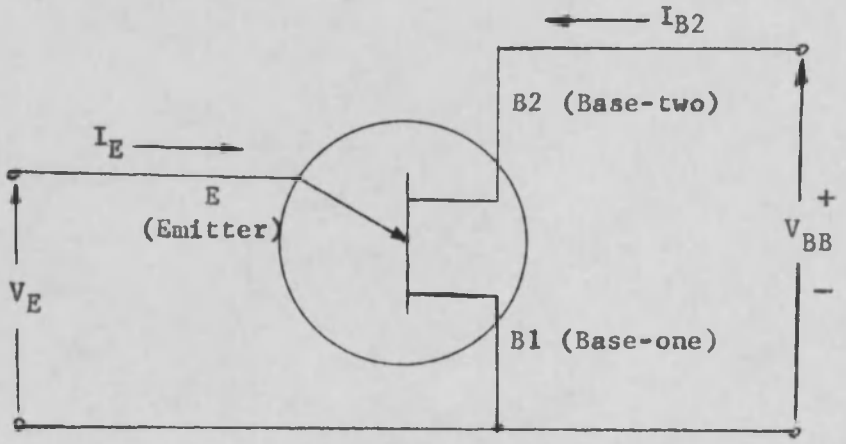
R. H. Mattson (1964) and A. Ambroziak (1964) have demonstrated the feasibility of fabricating neuristors from the unijunction transistor (UJT). The purpose of this thesis is to explain the realization of a unijunction transistor that has been optimized for a neuristor application. The optimized UJT is compatible with integrated circuit technology so that the entire neuristor circuit could be fabricated in integrated circuit form.

The Role of the Unijunction Transistor in the Construction of a Neuristor

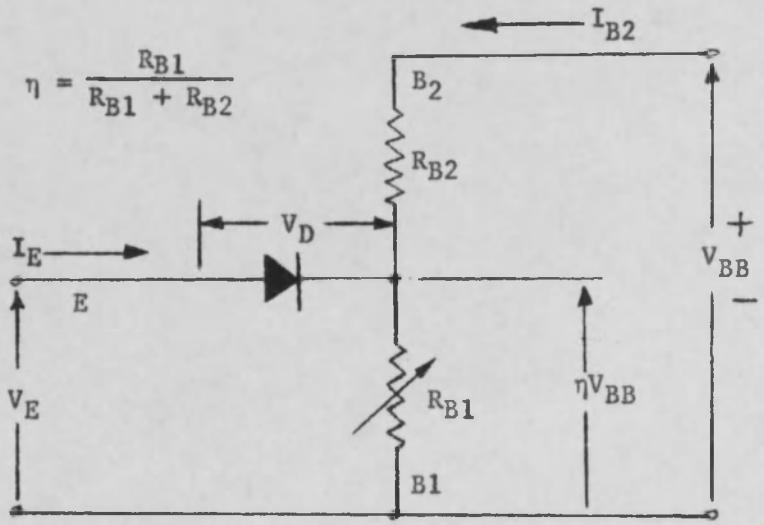
The unijunction transistor symbol and a simplified model of the UJT are shown in Fig. 1.1.

The static emitter characteristics of the UJT are given in Fig. 1.2. Notice that the emitter current I_E is small until the p-n junction diode becomes forward biased, which occurs when the emitter voltage V_E is equal to ηV_{BB} where η is the stand-off ratio $\frac{R_{B1}}{R_{B1} + R_{B2}}$. As the p-n junction diode becomes forward biased, holes are injected into the n-type substrate and are swept toward base-one by the field, thus increasing the conductance (reducing the resistance) of R_{B1}. This conductivity modulation accounts for the negative resistance region of the input characteristic curves.

A monostable unijunction transistor circuit and the path of operation on its input characteristic are shown in Fig. 1.3. The circuit is triggered when a positive pulse E_s of sufficient magnitude is applied to the circuit to cause the load line to be raised above the peak voltage V_p, where $V_p = \eta V_{BB} + V_D$ and V_D is the threshold voltage of the p-n junction diode (Millman and Taub, 1965). The circuit can



(a) Unijunction transistor symbol with identification of important voltages and symbols.



(b) Simplified equivalent circuit of the UJT.

Figure 1.1 Unijunction transistor symbol and a circuit model (Cleary, 1964).

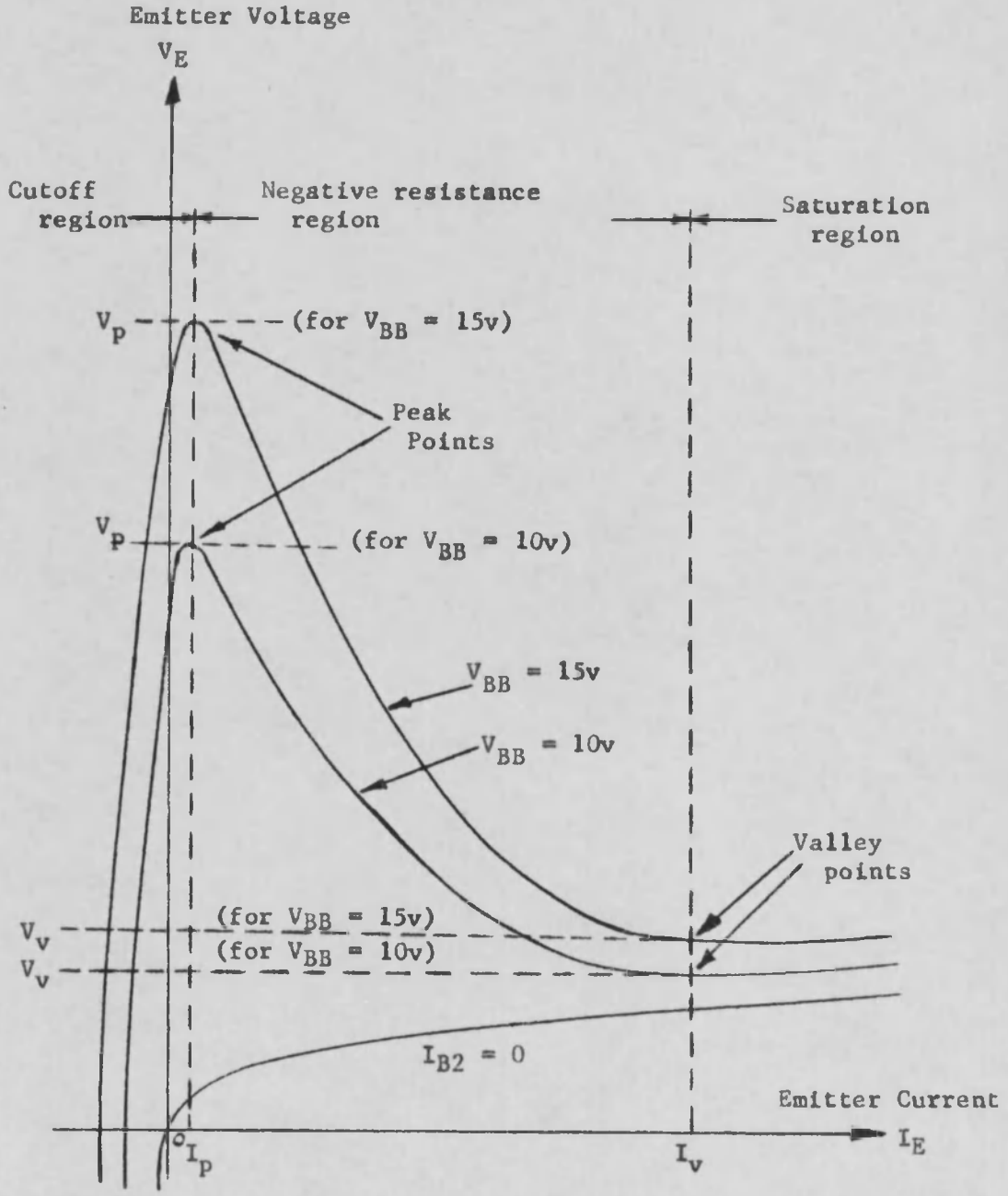
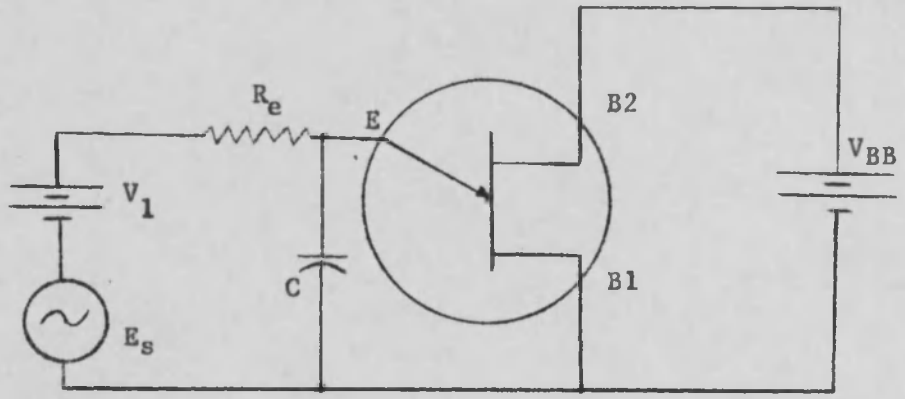
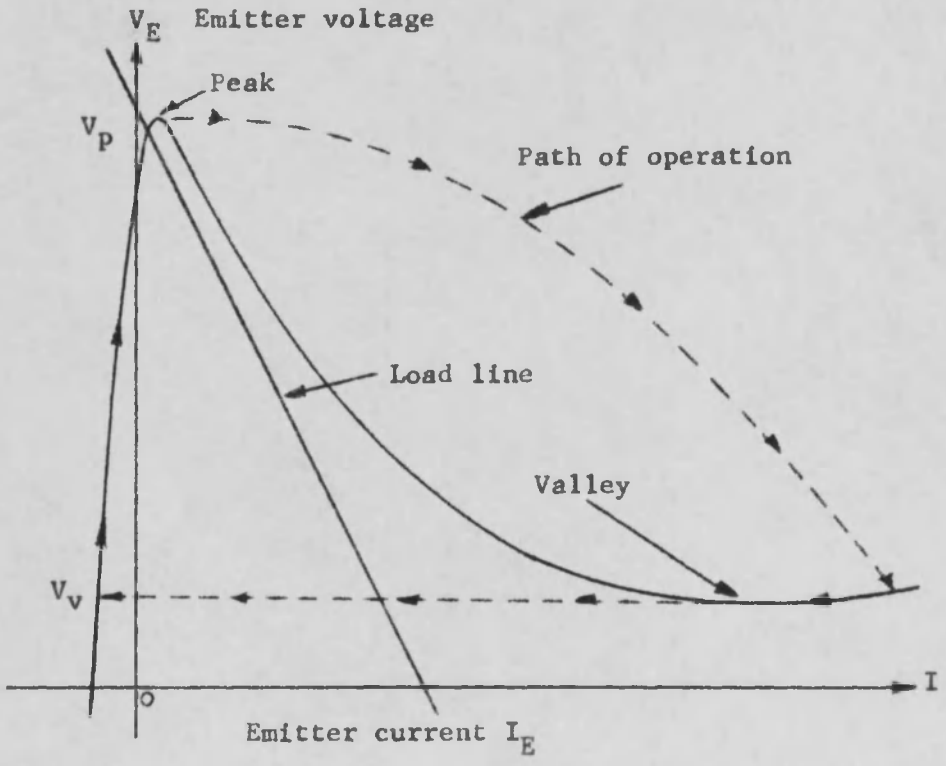


Figure 1.2 Static emitter characteristics of the unijunction transistor.



(a) Monostable UJT circuit.



(b) Input characteristic curve of UJT showing the path of operation.

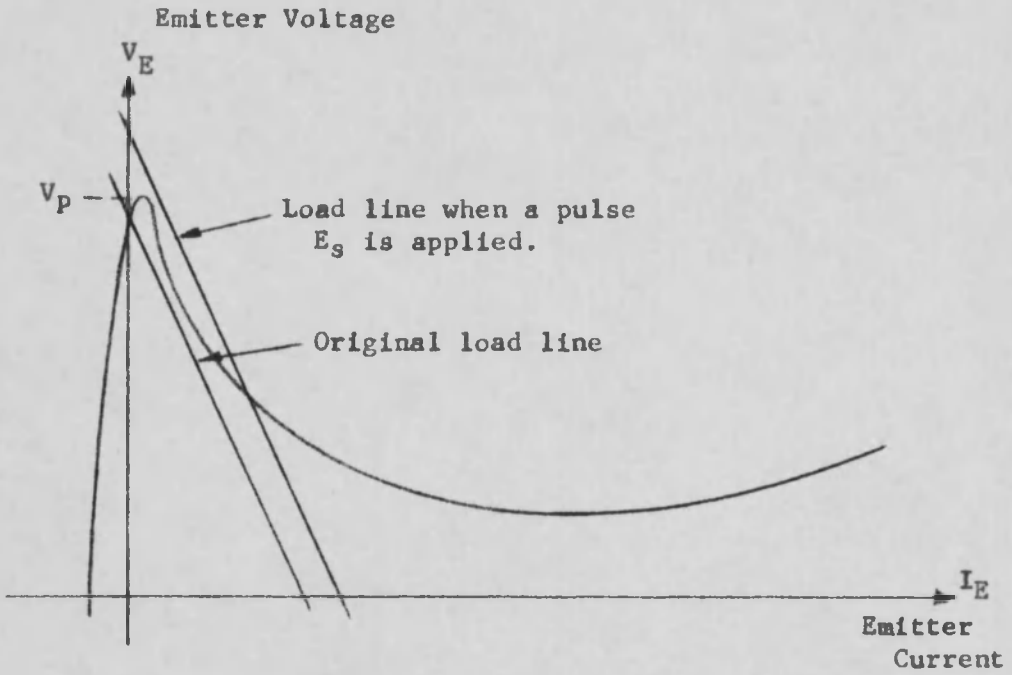
Figure 1.3 Monostable unijunction circuit and its path of operation.

also be triggered by causing the voltage V_p on the input characteristic curve to fall below the load line, which is accomplished by lowering the entire input characteristic curve. These two methods of triggering are illustrated in Fig. 1.4(a) and Fig. 1.4(b), respectively.

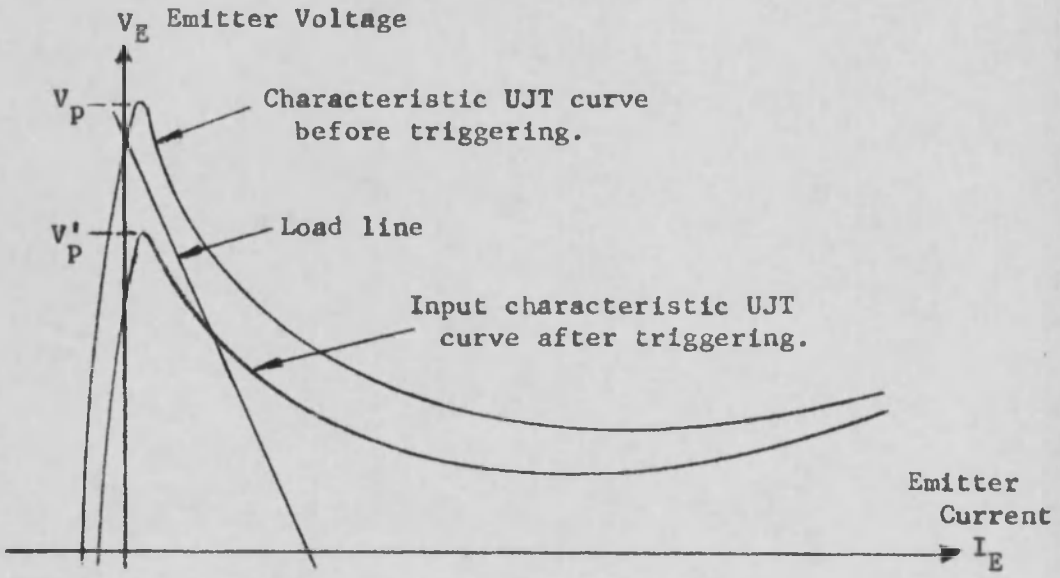
The geometry of the UJT investigated in this thesis is shown in Fig. 1.5. The planar unijunction structure is fabricated on a high resistivity n-type substrate. A low resistivity p-type emitter ring is formed near the surface of the substrate by means of the high temperature diffusion of p-type impurities. Ohmic contacts for the base-one, base-two, and emitter regions are formed of aluminum. In order to assure an ohmic contact between the lightly doped base regions and the aluminum, the base regions are heavily doped with n-type impurities (indicated by n+) prior to the deposition of the aluminum.

Several UJTs can be fabricated on the same substrate with a common base-two as shown in Fig. 1.6(a). The neuristor is formed from this configuration or "line" of UJTs by biasing each UJT as a monostable circuit. The simplified circuit model of the neuristor line is shown in Fig. 1.6(b).

Neuristor line operation is initiated when a positive pulse E_s triggers the first UJT into monostable operation. This causes the resistance R_{B1_1} in Fig. 1.6(b) to be greatly reduced due to conductivity modulation. This in turn causes the voltage in the region "a_1" in the n-type substrate to be reduced below the valley voltage V_v. Since the valley voltage is usually only 1 or 2 volts, the n-type substrate in the region "a_1" is close to ground potential. Region "a_1", in the

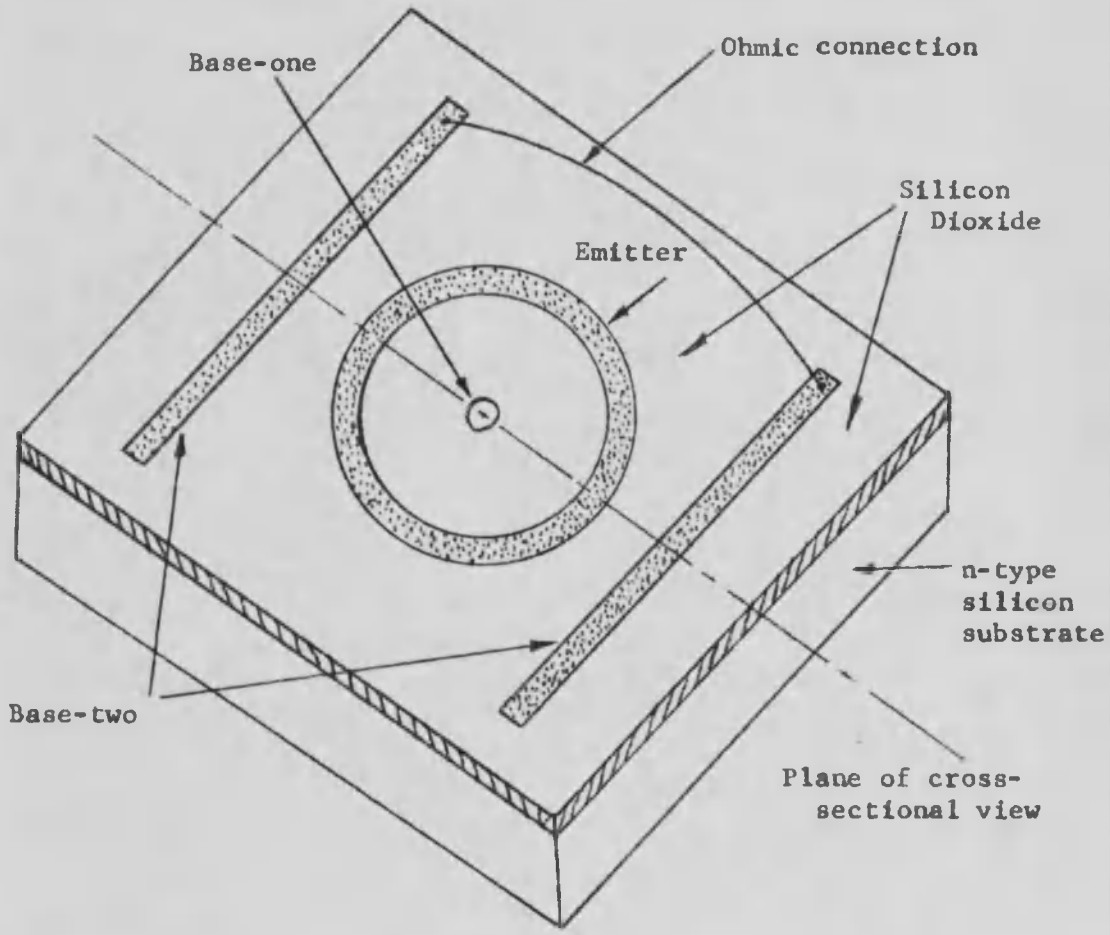


(a) Triggering caused by a shift in the load line.

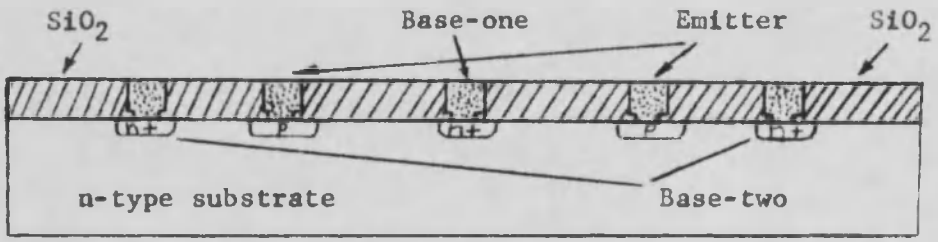


(b) Triggering caused by a shift in the characteristic UJT curve.

Figure 1.4 Two methods of triggering the monostable circuit of Fig. 1.3.

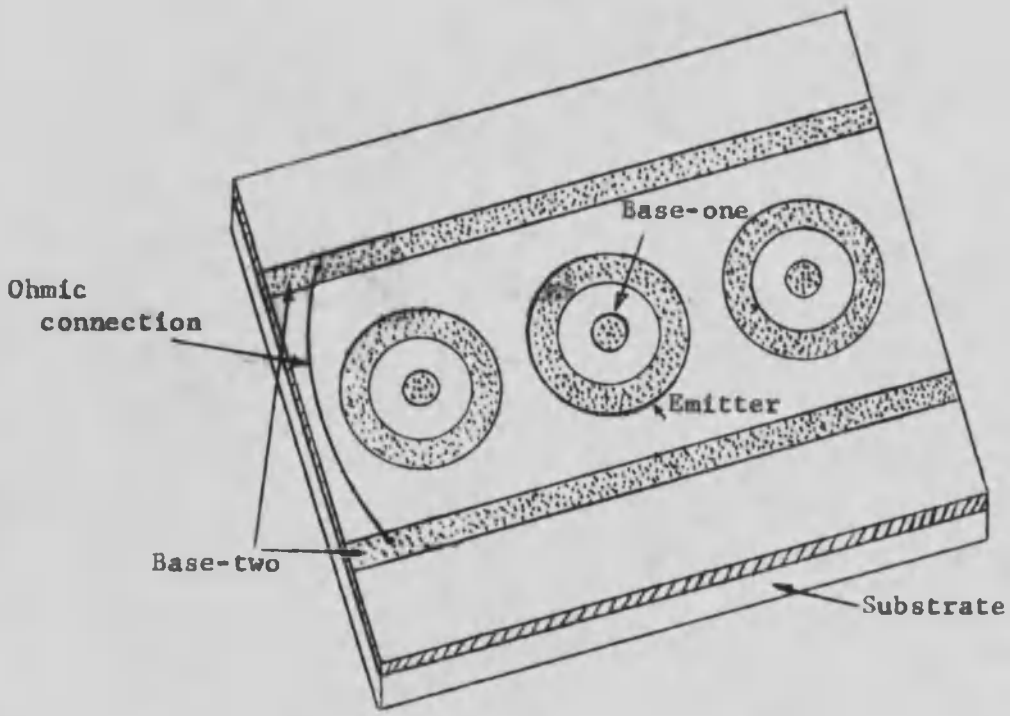


(a) Top view.

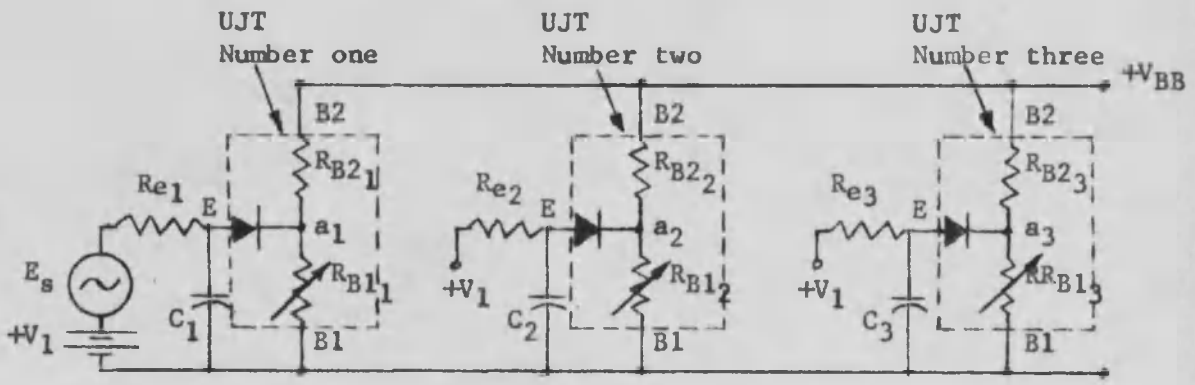


(b) Cross-sectional view.

Figure 1.5 Geometry of the planar unijunction transistor.



(a) Three unijunction transistors form a neuristor line.



(b) Simplified circuit model of the neuristor line, using the three unijunction transistor configuration shown in (a).

Figure 1.6 A neuristor line realization using unijunction transistors.

geometry of Fig. 1.6(a), is the n side of the p-n junction diode and is located below the emitter ring.

Now if the region "a_2", which is located below the emitter ring of the second UJT, is physically close to the very low potential of region "a_1", then the potential in region "a_2" will be decreased. A sufficient decrease in the potential in region "a_2" will cause the second UJT to self-trigger. This is the self-triggering method shown and discussed in conjunction with Fig. 1.4(b).

The self-triggering action between adjacent UJTs will continue until all UJTs in a line have been triggered and thus the signal will propagate down the line.

After a time period determined by R_e and C, each unijunction transistor will return to its initial stable point, usually in the same order as their triggering sequence, and the neuristor will then be capable of propagating another pulse. As each UJT returns to its initial stable point, it cannot be retriggered by the UJT to the right of it (which <u>is</u> still triggered), because the UJT to its right will have reached the region of its input characteristic curve where conductivity modulation and carrier injection no longer exist (namely, the region of the curve where the p-n junction diode is reverse biased).

Chapter 2

DESIGN OF THE UNIJUNCTION TRANSISTOR FOR A NEURISTOR CIRCUIT

Characteristics Required for the Unijunction Transistor

The geometry of the UJT, as shown in Fig. 1.6(a), was chosen for several reasons. First, the entire fabrication process is readily adaptable to integrated circuit techniques. Also, lines of UJTs are easily fabricated on the same substrate, and the amount of interaction between adjacent UJTs, which is necessary for self-triggering, is large.

Another feature of the geometry of Fig. 1.6(a) is that with a voltage V_{BB} applied between base-two and base-one, most of the potential drop is close to the base-one because of its small size (Warner, 1965). This is utilized to obtain high values of η and interbase resistance in a relatively small total area.

The area in the substrate from the base-one to the emitter has a large electric field because of the large potential drop near base-one. This is desirable because every excess carrier is injected directly into the region of highest electric field, and thus these injected carriers are swept with a higher velocity with less time for recombination.

As the area of the base-one contact is made smaller, high values of interbase resistance and η are realized, and the recombination of injected carriers is reduced due to the high electric field between the emitter and base-one. The total area of the device can also be reduced. Since all these characteristics are desirable, the base-one contact is made as small as practical.

A high standoff ratio η allows a high peak voltage to valley voltage ratio and also permits the operation of the UJT at lower values of V_{BB}. Lower values of V_{BB} reduce the power dissipated in the device.

The high peak voltage to valley voltage ratio greatly increases the ability of one UJT to trigger an adjacent UJT, because as the first UJT fires, there is a large change of the voltage beneath the emitter of the adjacent UJT (assuming a close spacing between emitters). This will cause the adjacent UJT to be triggered over a large range of initial bias conditions. Thus all UJTs in a row can be biased substantially below the value of V_p so that noise and temperature variations will not cause unwanted triggering, yet the UJTs will still perform as desired. This will also allow for some variation in V_p from one unit to another.

Design Theory

This design of the UJT attempts to optimize the peak to valley voltage ratio on the input characteristic curve. The physical constants of the device are chosen to give this result. An equation that relates emitter voltage V_E to emitter current I_E in terms of V_{BB} and the physical constants of the device has been developed by R. H. Schmidt (1965). The equation was developed for the UJT design in Fig. 2.1 and is

$$I_E = \frac{4\pi w \sigma_{mod} V_E}{\ln \frac{r_2 r_3}{r_1^2} + \frac{\sigma_{mod}}{2\sigma_{bulk}}} - \frac{(V_{BB} - V_E)\sigma_{bulk}}{K} \qquad (2.1)$$

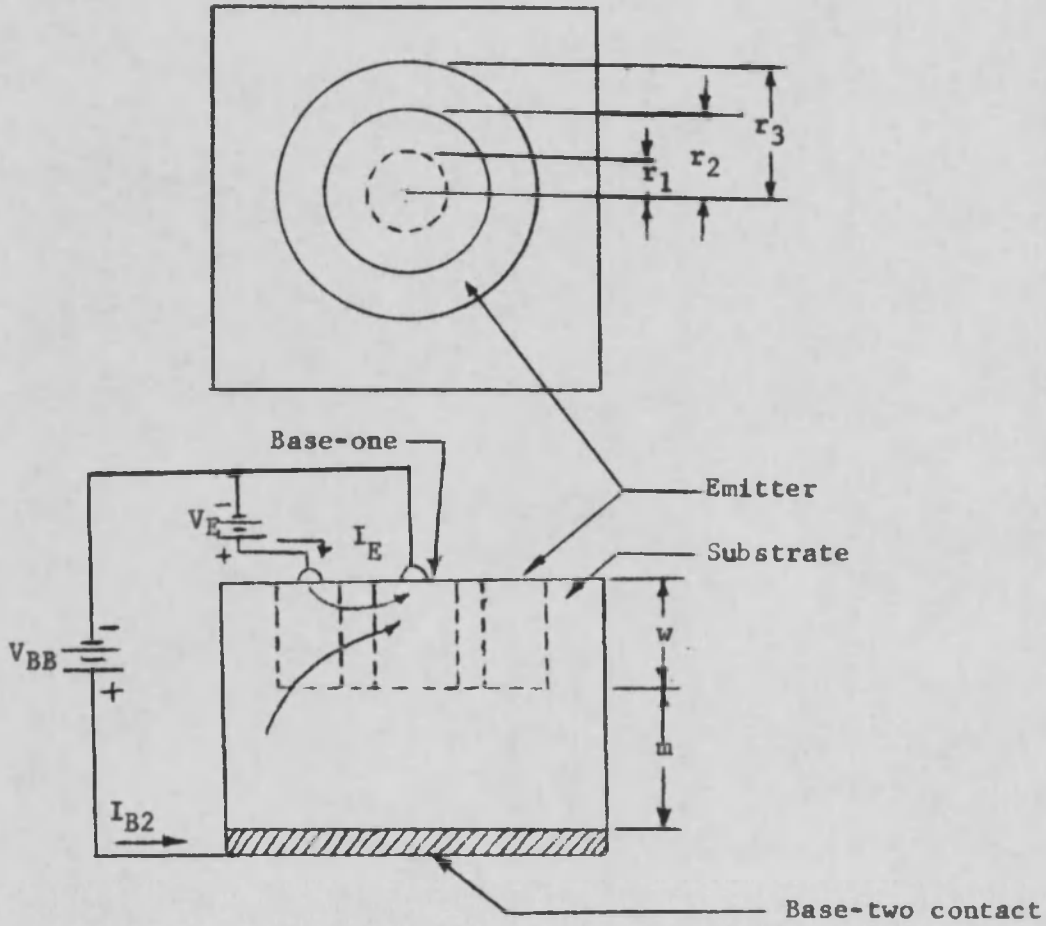


Figure 2.1 Unijunction transistor geometry used in deriving Eq. (2.1).

where

$$\sigma_{bulk} = q\,\mu_n\,N_d \tag{2.2}$$

$$\sigma_{mod} = q[\mu_n(N_d + p(0)) + \mu_p p(0)] \tag{2.3}$$

and

$$p(0) = \frac{I_E}{Aq}\left(\frac{t_{pn}}{D_p}\right)^{\frac{1}{2}} \tag{2.4}$$

This equation is valid when the p-n junction diode is forward biased. The value w in Eq. (2.1) is the effective depth of the n-type substrate that is conductivity modulated. The value r_1 is the radius of the base-one region, and r_2 and r_3 are the inside and outside radii of the emitter. σ_{bulk} is the unmodulated conductivity of the n-type substrate, while σ_{mod} is the modulated conductivity of the n-type substrate. K is a constant of the geometry.

Schmidt plotted V_E versus I_E as a function of the several parameters in Eq. (2.1) to find which conditions gave a maximum of negative resistance and a maximum peak voltage. He found that high resistivity material, a high V_{BB}, high values for w, and a low value of $\ln \frac{r_2\, r_3}{r_1^2}$ all cause the value of the negative resistance to be higher. He also found that a high V_{BB}, a low value for w, and a high value of $\ln \frac{r_2\, r_3}{r_1^2}$ cause the peak voltage to be higher. All of these predictions were experimentally verified by Schmidt (1965).

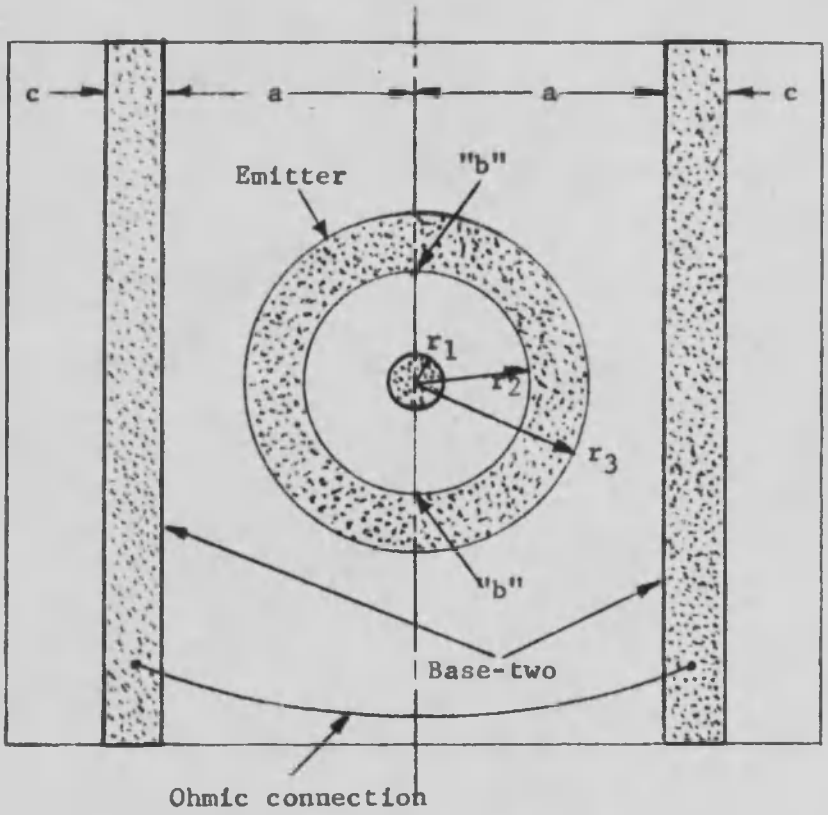
Since both a high negative resistance and a high peak voltage are desired, the following qualities are necessary for the UJT: a high resistivity material, a moderate value for w, a moderate value for $\ln \frac{r_2}{r_1} \frac{r_3}{2}$, and a high voltage V_{BB}.

Physical Design

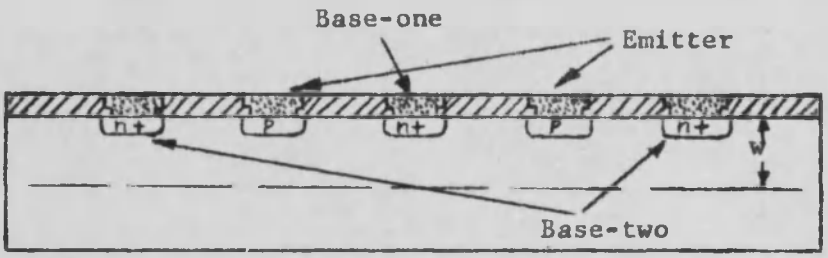
The above facts provide a basis for the design of the UJT whose geometry and dimensions are shown in Fig. 2.2. This geometry is used for the reasons mentioned previously, which include ease of fabrication through planar diffusion techniques, ability to attain high values of η in a relatively small area, the ability to have a large amount of interaction between two adjacent UJTs, and the absence of high field regions.

The first step in the design of the UJT is the determination of the most suitable resistivity for the n-type substrate. It has been shown that for a resistivity less than 10 Ω-cm, the extrinsic majority carrier concentration is too high to permit effective conductivity modulation (Hachtel and Haines, 1964). A resistivity of 150 Ω-cm was chosen because of its availability in the laboratory.

The interbase resistance R_{BB} is chosen to be approximately 5 kΩ. This value, which is used in commercial UJTs, limits the interbase current to a reasonable value when the device is conducting heavily. This is not a critical parameter, however, and it can be changed if other design considerations so indicate.



(a) Top view.



(b) Cross-sectional view taken through the center of the device.

Figure 2.2 Geometry of the unijunction transistor showing important dimensions.

The radius r_1 is chosen as small as practical so that the overall device size will be as small as possible. A small device size also implies a small distance from the emitter to base-one. This limits injected carrier recombination in the emitter to base-one region, because there is less distance in which recombination can occur. Thus, conductivity modulation in the region is increased. The smallest circle that could be drawn on the original artwork had a radius of 45 mils, so after a 30 to 1 reduction, the minimum practical value of r_1 was 1.5 mils.

The effective thickness w of the substrate material should neither be too thick nor too thin for the geometry of Fig. 2.1. For the geometry of Fig. 2.2, however, the value of w is not as critical because the UJT is in one plane. An effective thickness of 5 mils was thus chosen, because 5 to 7 mil wafers are easily diced, and the effective thickness is always less than the actual thickness of the wafer.

The parameters R_{BB}, the resistivity ρ_o , the effective thickness w of the substrate material, and the radius r_1 determine the value of the distance "a" in Fig. 2.2. The distance "a" in this particular configuration is rather difficult to calculate. However, as a rough approximation, the base-two ohmic contact can be assumed to be circular and then the distance "a" becomes a radius "a" and is quite easily calculated. The equation for the determination of radius "a" (assuming a circular base-two contact) is

$$\log \frac{a}{r_1} = \frac{2\pi R_{BB} w}{2.3 \rho_o} \qquad (2.5)$$

or

$$a = r_1 \, 10^{\frac{2\pi R_{BB} w}{2.3\rho_o}} \qquad (2.6)$$

This equation is derived in Appendix A. From this equation, letting R_{BB} = 5 kΩ, ρ_o = 150 Ω-cm, w(effective) = 5 mils, and r_1 = 1.5 mils, radius "a" was found to be 18 mils.

By having two parallel bars for base-two instead of the above assumption of a circular base-two, the value of R_{BB} increases. Thus in order to maintain R_{BB} constant, the distance "a" must be less than the radius "a". The distance "a" was thus estimated to be 13 mils.

The radius r_2 determines the value of the standoff ratio η, and a value of 0.6 to 0.7 is the desired range of values for η. Before r_2 is calculated, the exact location of the area where the p-n junction first becomes forward biased must be known. This area can be located by knowing the potential that exists throughout the n-type substrate when the p-n junction diode is reverse biased. A sketch of the electric field and the equipotential lines throughout the substrate for this geometry is given in Fig. 2.3.

From Fig. 2.3 it can be seen that several different equipotential lines pass under the inside edge (r_2) of the emitter. The lowest potential at the inside edge of the emitter exists at points "b". Thus, it is at points "b" that the p-n junction first becomes forward biased, because these are the points that are least reverse biased.

Again it is difficult to calculate the exact radius r_2 to points "b", but a rough approximation can be found by assuming that the base-two contact is circular. The equation for the determination of r_2, in

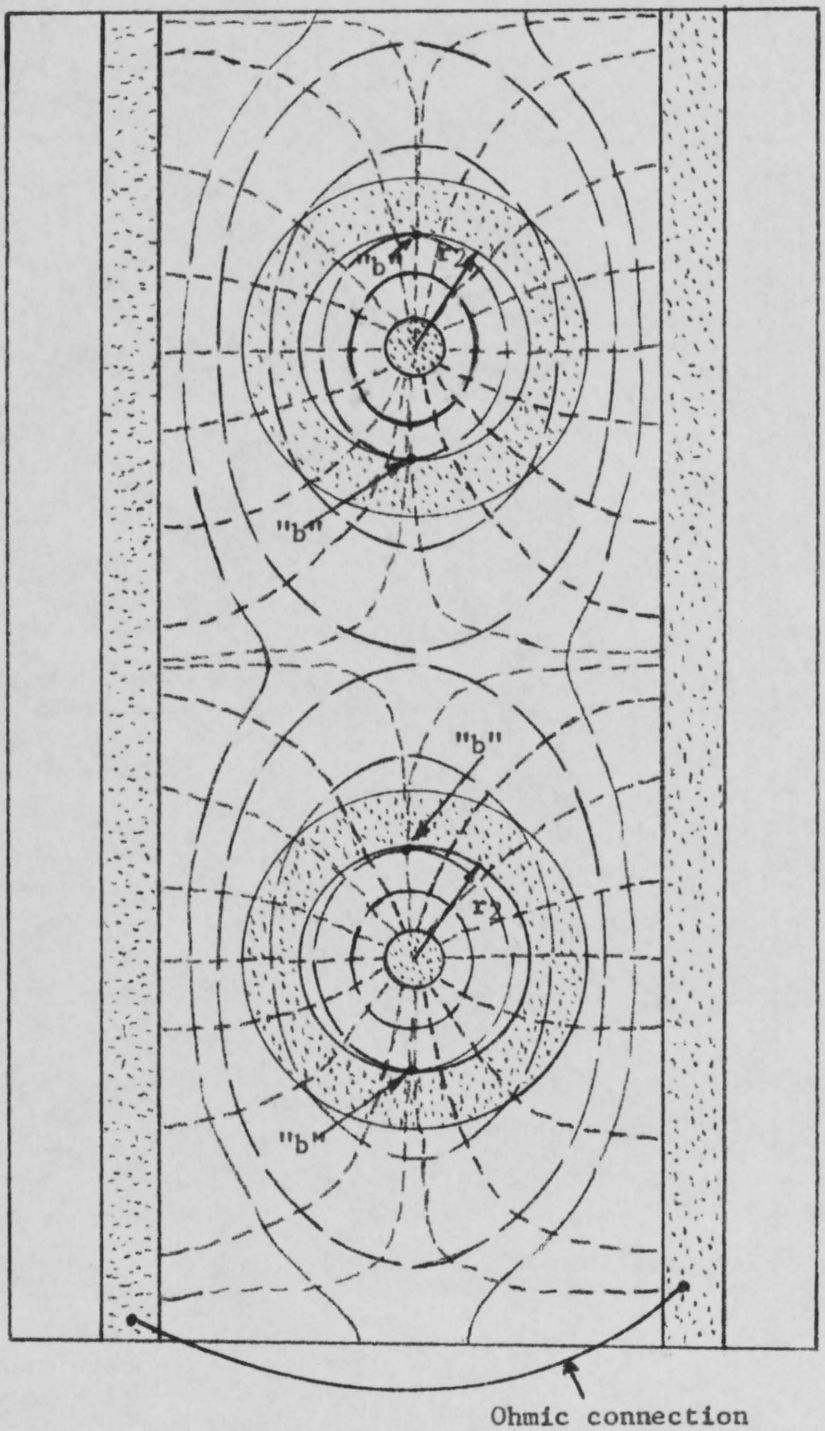


Figure 2.3 Two unijunction transistors showing the electric field and potential lines between base-two and base-one, with the emitter p-n junction being reverse biased.

terms of r_1, η, ρ_o, w, and R_{BB} is

$$\log \frac{r_2}{r_1} = \frac{2\pi \eta R_{BB} w}{2.3 \rho_o} \tag{2.7}$$

or

$$r_2 = r_1 \, 10^{\frac{2\pi \eta R_{BB} w}{2.3 \rho_o}} \tag{2.8}$$

This equation is derived in Appendix B. From this equation, letting R_{BB} = 5 kΩ, η = .6 w(effective) = 5 mils, r_1 = 1.5 mils, and ρ_o = 150 Ω-cm, the approximate radius r_2 was found to be 6 mils.

The minimum radius r_3 is determined by the accuracy of the artwork, and the precision with which one mask can be aligned on another. The minimum value for r_3 was chosen to be 9 mils, which made the emitter 3 mils wide. A 1.0 mil wide emitter contact window was cut at the center of the emitter to provide an ohmic contact to the emitter. This allowed a mask and alignment error of 1.0 mil which proved satisfactory with the equipment available in the laboratory. In fact, some devices were successfully fabricated using an emitter width of 2 mils and a total alignment tolerance of 0.5 mil.

Since r_1 = 1.5 mils, r_2 = 6 mils, and r_3 = 9 mils, the value of $\ln \frac{r_2 r_3}{r_1^2}$ is 3.2. This is a moderate value, according to results of Schmidt (1965) and should give a relatively high peak voltage and a relatively large amount of negative resistance.

The width of the base-two contact, designated by the letter "c" in Fig. 2.2 is not a critical dimension so it was made 3 mils wide to

allow sufficient area for probing and bonding of the wire leads. The final design of the UJT is shown in Fig. 2.4.

Equation (2.9) was used to predict the V-I characteristics using the geometry in Fig. 2.4. Given below is the equation used for prediction purposes.

$$I_E = \frac{4\pi w \sigma_{mod} V_E}{\ln \frac{r_2 r_3}{r_1^2} + \frac{\sigma_{mod}}{2\sigma_{bulk}}} - \frac{2\pi w \sigma_{bulk} (V_{BB} - V_E)}{\ln \frac{r_4}{r_3}} \tag{2.9}$$

where

$$\sigma_{bulk} = q \mu_n N_d \tag{2.10}$$

$$\sigma_{mod} = q[\mu_n(N_d + p(0)) + \mu_p p(0)] \tag{2.11}$$

$$p(0) = \frac{I_E}{Aq} \left(\frac{t_{pn}}{D_p}\right)^{\frac{1}{2}} \tag{2.12}$$

From these equations and the parameter values given in Table 2.1, the input characteristics of the UJT design of Fig. 2.4 were plotted. These calculated input characteristics are shown in Fig. 2.5 for several values of V_{BB}.

Table 2.1

VALUES OF THE PHYSICAL AND GEOMETRIC CONSTANTS APPEARING IN EQUATIONS (2.9) to (2.12)

Symbol	Value
r_1	1.5 mils
r_2	6.0 mils
r_3	9.0 mils

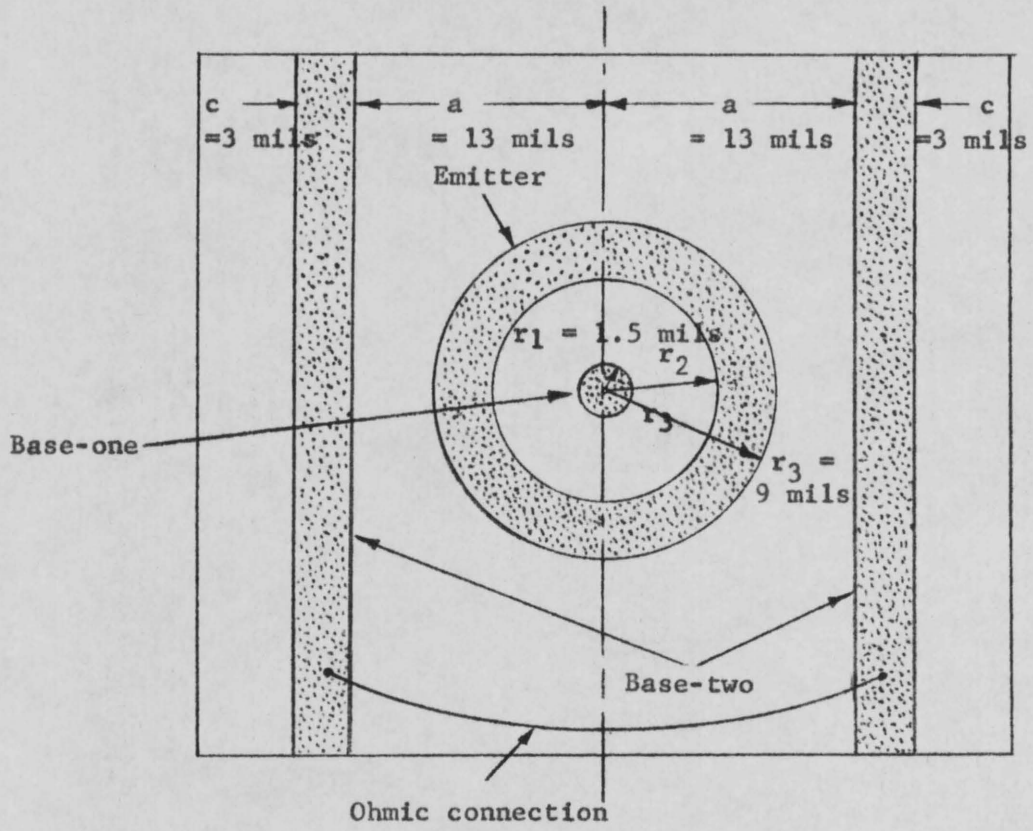


Figure 2.4 Final design of the unijunction transistor.

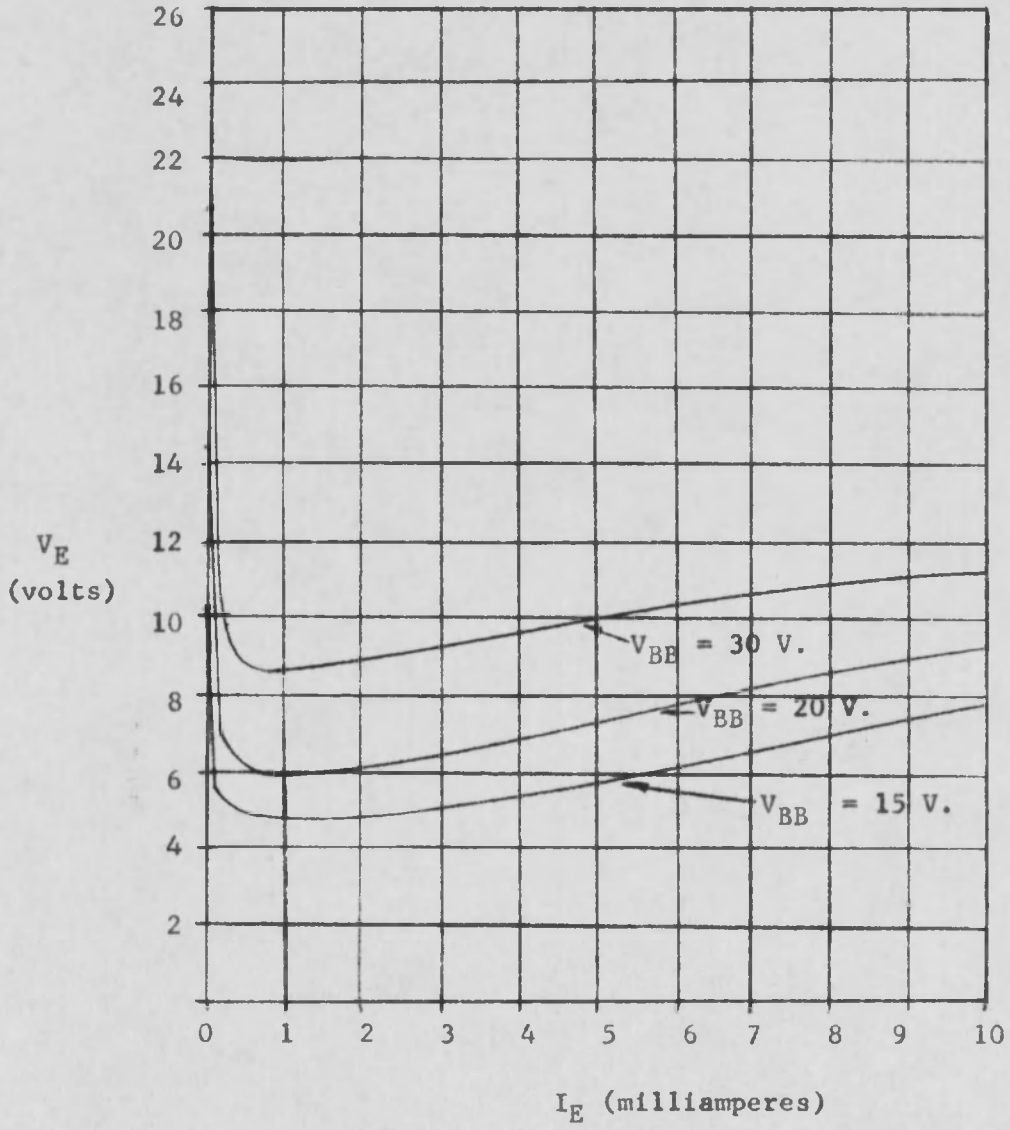


Figure 2.5 Calculated input characteristics of the design shown in Figure 2.4.

Table 2.1 (Continued)

Symbol	Value
r_4	13.0 mils
w	3.0 mils
μ_n	1350 cm^2/volt sec.
μ_p	480 cm^2/volt sec.
t_{pn}	10^{-6} sec.
D_p	3.2 cm^2/sec.

Variations to the Design of the UJT

Several other UJT geometries were investigated and fabricated for neuristor line evaluation. These geometries are shown in Fig. 2.6 and Fig. 2.7. These variations in geometry are evaluated in the next chapter.

Figure 2.6(a) shows a configuration with a slightly larger r_2 value of 8 mils, which should increase the value of the standoff ratio. The emitter width is still 3 mils. Figure 2.6(b) shows the same basic design with an r_2 value of 5 mils which is smaller than the original design, so the standoff ratio should be smaller.

Figures 2.6(c) and 2.6(d) illustrate the design of a UJT with a base-two to center spacing of 8.5 mils. The emitter spacings are different between Fig. 2.6(c) and Fig. 2.6(d), as are the emitter widths. Figure 2.6(c) has an emitter width of 2 mils, which allows an emitter contact window of 1 mil in the center of the emitter and a 0.5 mil alignment tolerance on each side.

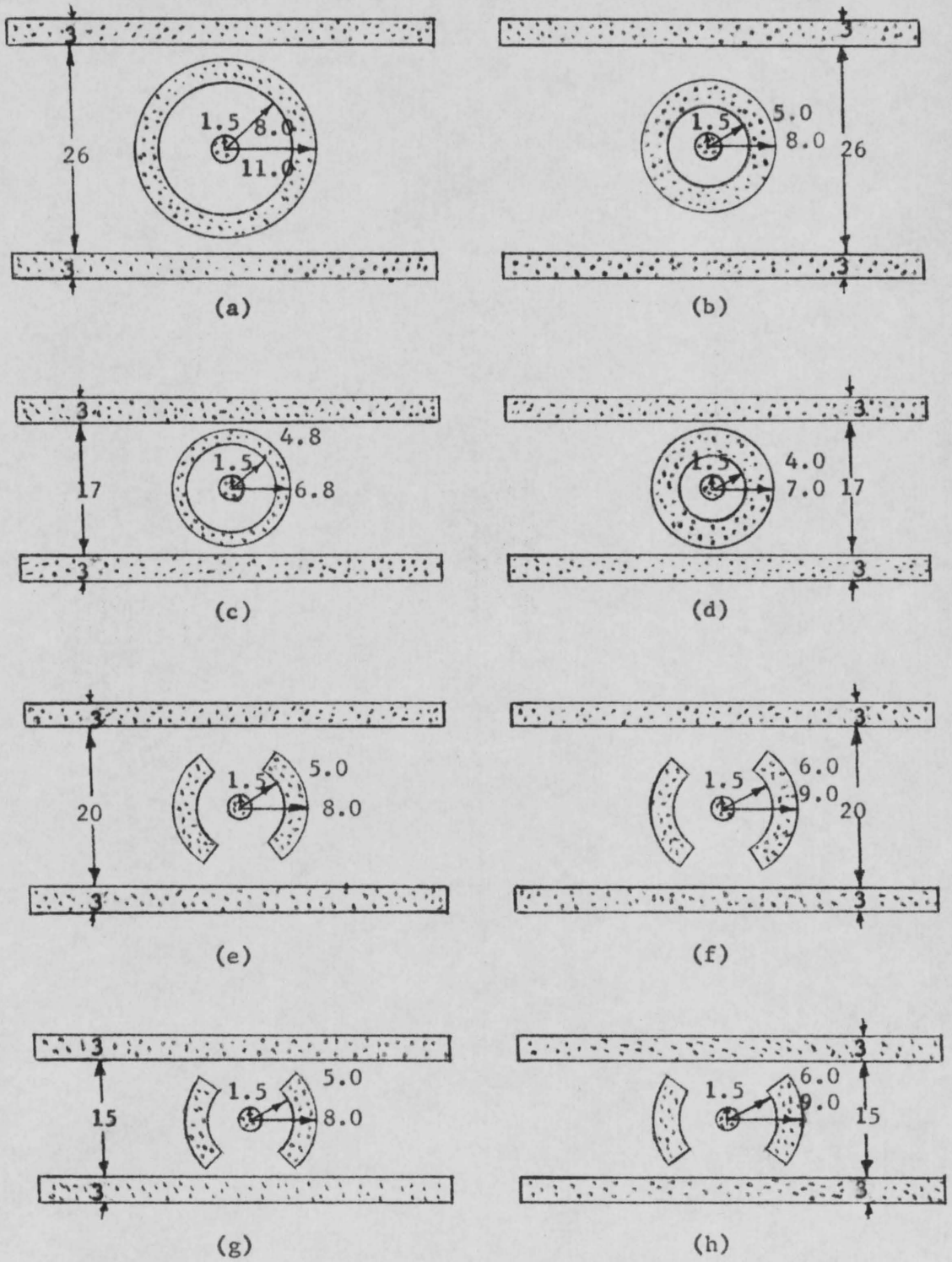


Figure 2.6 Alterations of the original design of the unijunction transistor.

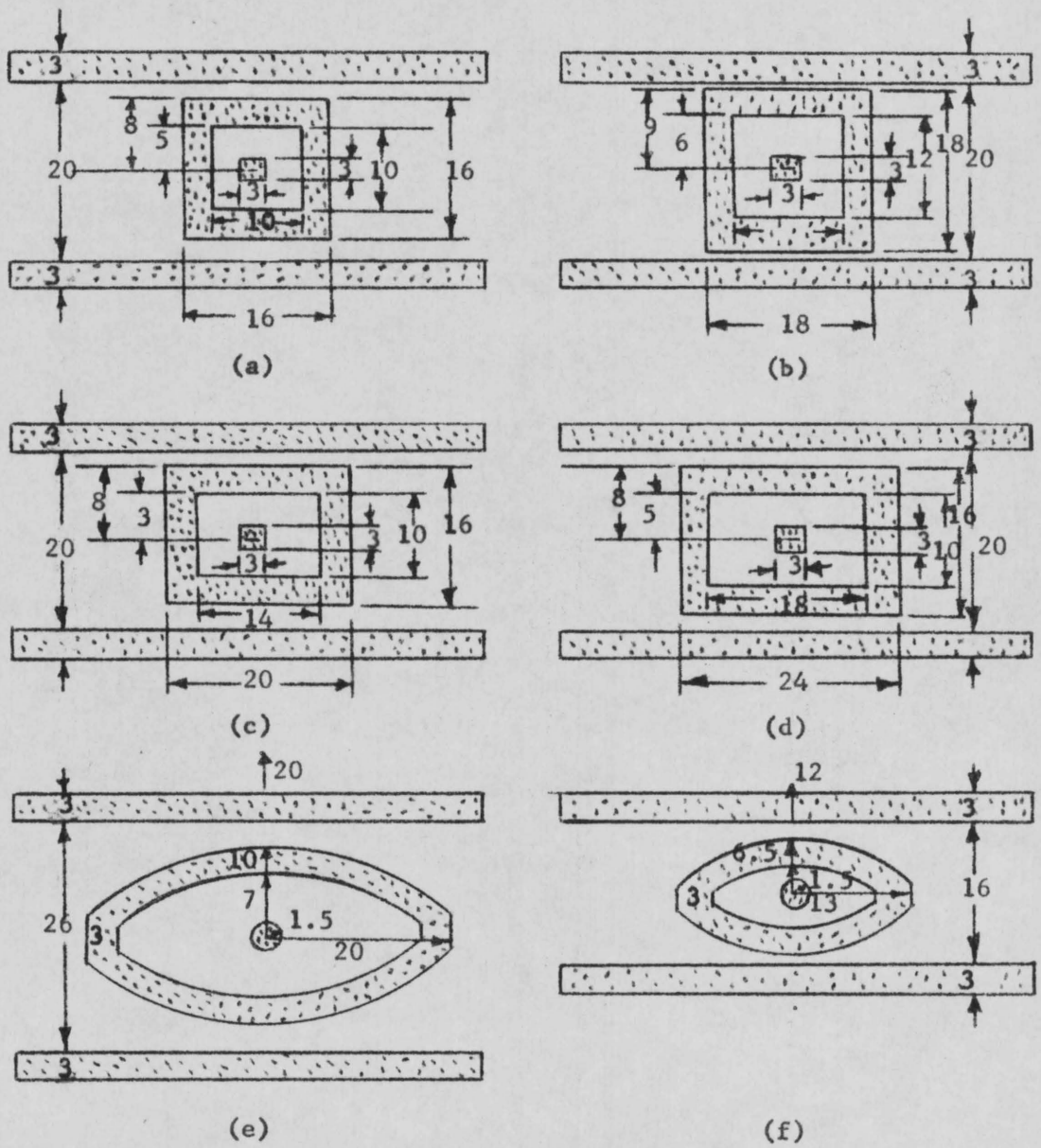


Figure 2.7 Variations of the original design of the unijunction transistor. (All dimensions in mils).

A type of split emitter is shown in Fig. 2.6(e), 2.6(f), 2.6(g) and 2.6(h). The base-two to center spacings and the emitter spacings were varied among the four designs. This type of design permits the value of r_2 to be almost as large as the base-two to center distance, as can be seen in Fig. 2.6(h). Also, the function of the part of the emitter that was omitted can be determined, and thus it can be found if the upper and lower areas of the emitter are necessary. As was explained earlier in this paper, the area of the emitter that first becomes forward biased is indicated by point "b" in Fig. 2.3.

The designs illustrated in Figs. 2.7(a) and 2.7(b) have a square-shaped emitter and base-one contacts. These designs were tried because they are much more accurately produced than the circular designs.

The designs shown in Figs. 2.7(c) and 2.7(d) have rectangular-shaped emitters, which should give a larger value for the standoff ratio η. These two designs are similar to the design in Fig. 2.7(a) except that the emitter patterns have been altered to form rectangles.

Figures 2.7(e) and 2.7(f) show designs attempting emitter construction in the general shape of the equipotential lines that exist in the substrate material when the p-n junction is reverse biased. If this could be attained, then the entire inside edge of the emitter would become forward biased at the same time.

The operating characteristics of all of these designs are given in a later section.

Chapter 3

FABRICATION OF THE UNIJUNCTION TRANSISTOR

Basic Procedure

The basic procedure for the fabrication of the UJT is given in the flow chart of Fig. 3.1. These steps are discussed and explained in the following paragraphs.

Mask Preparation and Photo-Reduction Process

In order to prepare the masks for the photo-etch processes, the desired layout of the UJT was drawn on a sheet of "Studnite" film, which consists of a red strippable coating on a mylar film base. The red coating was cut and areas were removed to form the desired geometries. The straight lines were cut with a Coradograph coordinatograph capable of cutting lines accurate to $\pm$ 1 mil, and the circles were cut with a compass. A photograph of the four original pieces of artwork is given in Fig. 3.2.

The lines on the mask had to be placed within an accuracy of 0.25 mil, which meant that the original artwork had to be accurate within 30 x 0.25 mil, or 7.5 mils, since the original artwork was 30 times larger than the final mask. This was accomplished by cutting the artwork with a coordinatograph and using the coordinatograph to lay out the radii for the circles. The original artwork was reduced 30 times using a Robertson Minitor camera with a Micro-Nikkor 70 mm lens.

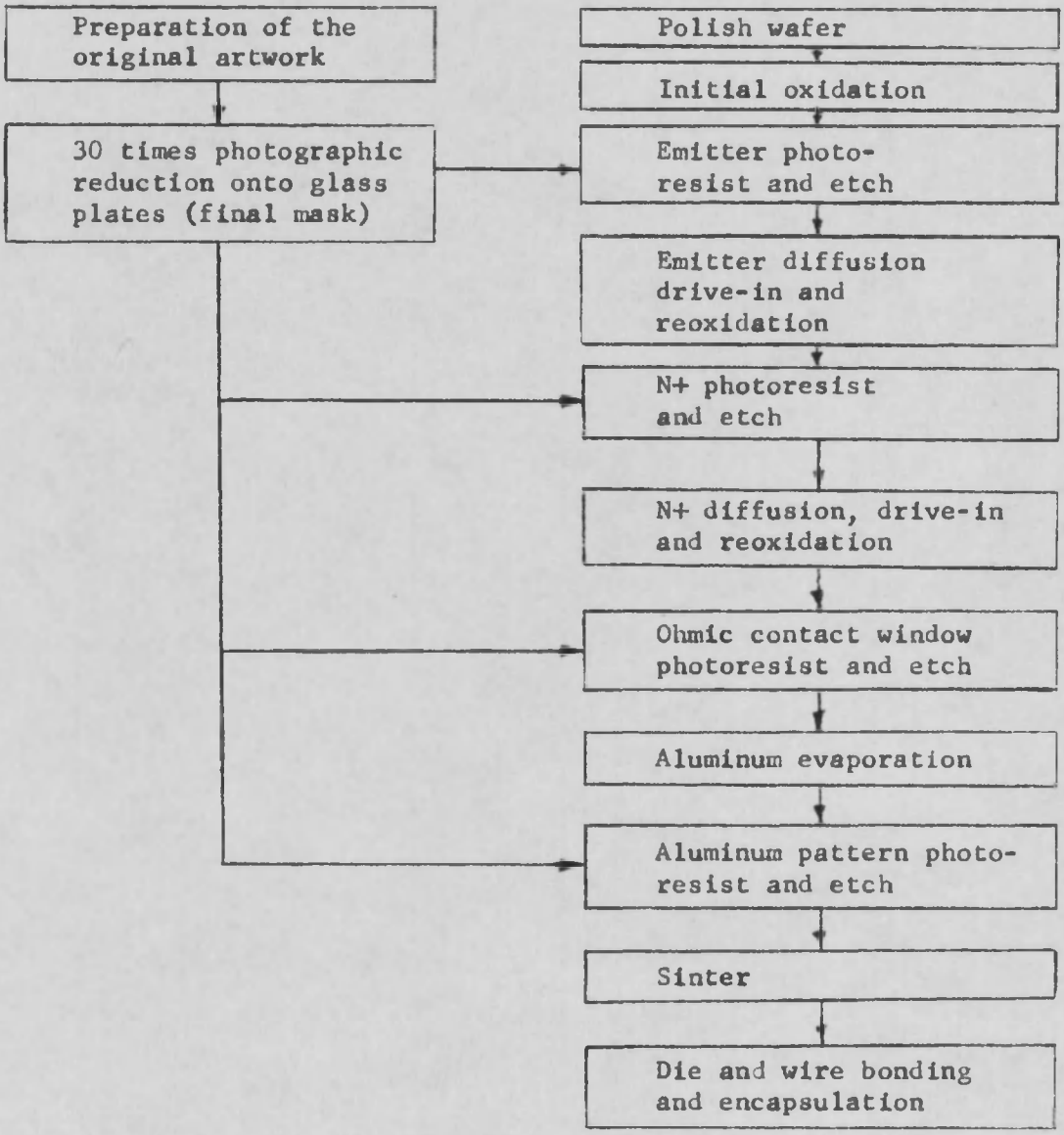
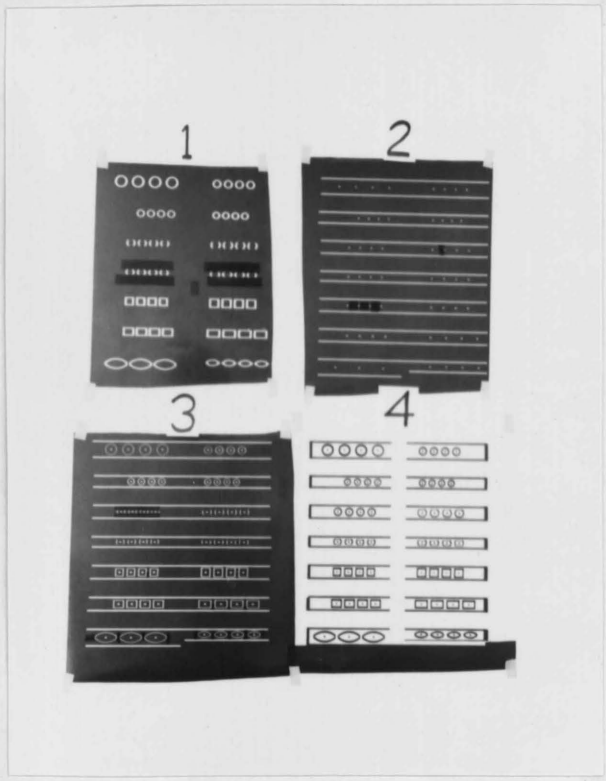


Figure 3.1 Flow chart for the fabrication of the UJT.



No. 1 is the p-type diffusion mask, No. 2 is the n-type diffusion mask, No. 3 is cut-before-metallization mask, and No. 4 is the metallization mask.

Figure 3.2 The original artwork used in the fabrication of the UJTs.

Each piece of artwork was directly reduced onto a 2 inch x 2 inch Kodak High Resolution Glass Plate. The Kodak High Resolution Glass Plate was exposed for 3.5 minutes using a Robertson backlight which has a high intensity monochromatic light source of 5460 Å.

The plate was developed for two minutes in Kodak D-8 developer which had been diluted with water in the ratio of two developer to one water. The plate was then rinsed in Kodak Stop Bath SB-1a for 15 seconds and fixed in Kodak Rapid Fixer for 60 seconds. Then the plate was rinsed in water for 30 seconds, bathed in Kodak Hypo Clearing Agent for one minute, and washed in water for two minutes. After a 15 second rinse in diluted Kodak Photo-Flo Solution to minimize drying marks, the plate was blown dry with nitrogen and allowed to air-dry for 30 minutes (Eastman Kodak Co., 1967). All the above chemicals were maintained at a temperature of 20°C. This final mask, the glass plate, was then inspected under a microscope for possible defects.

Polishing of Wafers

The next step in the processing schedule is the preparation of the wafer surface. The wafers that were used had already been lapped so only polishing was required.

The chemical polishing method was used with relative success. The chemical polish or etch was accomplished by immersing the wafers in a bath of nitric acid, hydrofluoric acid, and sodium dichromate (ratios 30:20:1) for one minute. The etch was stirred by a rotating magnetic bar. Every five seconds the wafers were exposed to air for one second and then immediately re-immersed in the etch solution.

Immediately after the etch the wafers were rinsed in deionized water, given a 10 second bath in 1:10 ($HF-H_2O$) dilute hydrofluoric acid, rinsed again in deionized water, rinsed in isopropyl alcohol, and then blown dry with nitrogen. The wafers were then either immediately prepared for the initial oxidation or stored in isopropyl alcohol until they were needed.

Initial Oxidation

The following step was the initial oxidation of the wafers. First the wafers were cleaned again by placing them in a 1:1 solution of concentrated ammonia and hydrogen peroxide. The solution was boiled for 10 minutes before the wafers were removed. After 10 minutes in hot ($90^{\circ}C.$) nitric acid and a thorough rinse in deionized water, trichloroethylene, and isopropyl alcohol, the wafers were blown dry with nitrogen and loaded in the oxidation boat.

The cleaned wafers were oxidized for 1.5 hours at $1100^{\circ}C.$ in an atmosphere composed from the following sources: 500 cc per minute of O_2 and 500 cc per minute of O_2 bubbled through $92^{\circ}C.$ water. The inside diameter of the oxidation furnace barrel through which these gases flowed is 40 mm. This procedure resulted in a silicon dioxide thickness of approximately 0.6 micron, thus providing an adequate mask for future diffusions (Research Triangle Institute, 1965).

Photoresist and Etch Process

After oxidation, the wafers were immediately coated with the photoresist, Kodak Metal Etch Resist (KMER). Prior to its application,

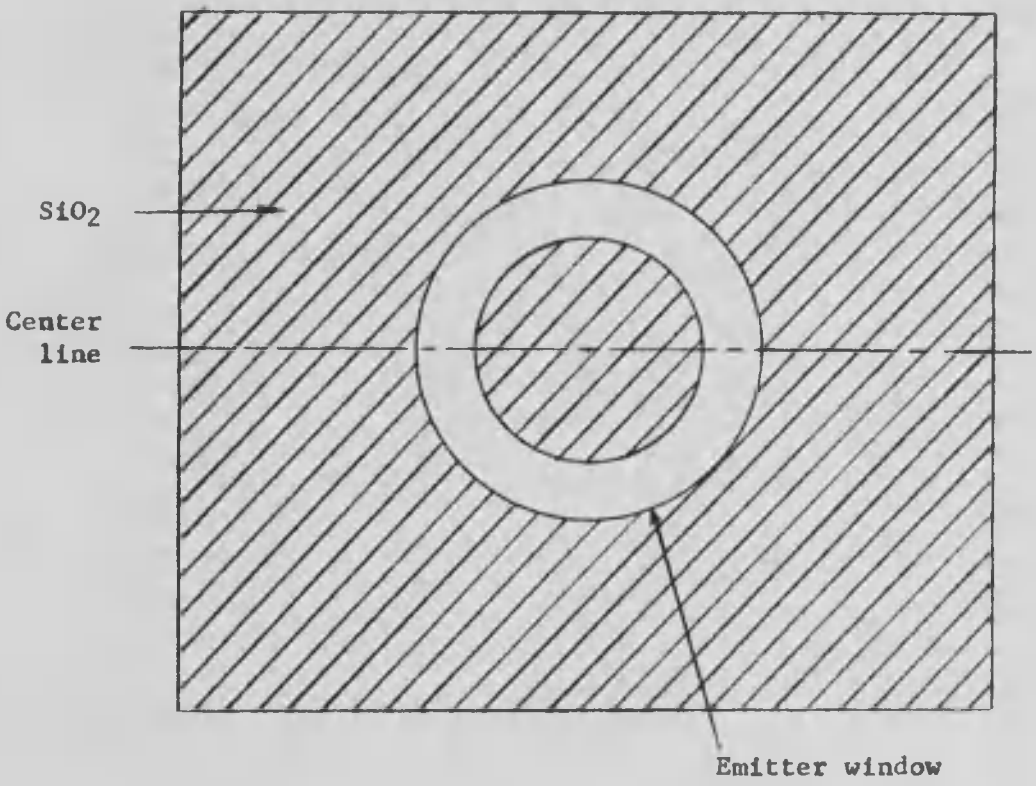
it was centrifuged at 15,000 rpm for 3 hours to purify it. The photoresist was not filtered or thinned.

The photoresist was applied with a eye dropper to the wafer, and then the wafer was spun at 6000 rpm for 10 seconds to produce a thin photoresist coating of approximately 2.0 microns in depth. The wafer was then baked for 10 minutes at 95°C. to dry the resist (Research Triangle Institute, 1964a).

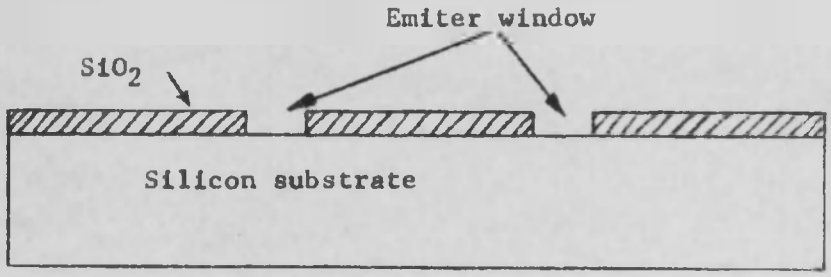
With the mask properly aligned over the wafer, the photoresist was exposed to ultraviolet light for 30 seconds and developed for 25 seconds with a spray of KMER developer. After rinsing with isopropyl alcohol and blowing dry, the wafer was baked for 20 minutes at 140°C.

The wafer was then immersed in an etching solution of 200 ml. of 40 percent NH_4F and 50 ml. of 48 percent HF to etch away the areas of silicon dioxide that were not protected by photoresist. The rate of etch was 0.15 micron of silicon dioxide per minute. The wafers were then inspected under a microscope to insure the complete removal of the silicon dioxide from the unprotected areas.

The photoresist was removed from the wafers by immersing them in hot (90°C.) sulphuric acid for 10 minutes and then scrubbing them in a bath of trichloroethylene. After a rinse with isopropyl alcohol, the wafers were dried or stored in isopropyl alcohol until just prior to the emitter diffusion. Figure 3.3 shows two views of the wafer with the etched emitter window.



(a) Top view.



(b) Cross-sectional view taken through the center of the device.

Figure 3.3 Two views of the UJT showing the etched emitter window.

P-type Emitter Diffusion, Drive-in, and Reoxidation

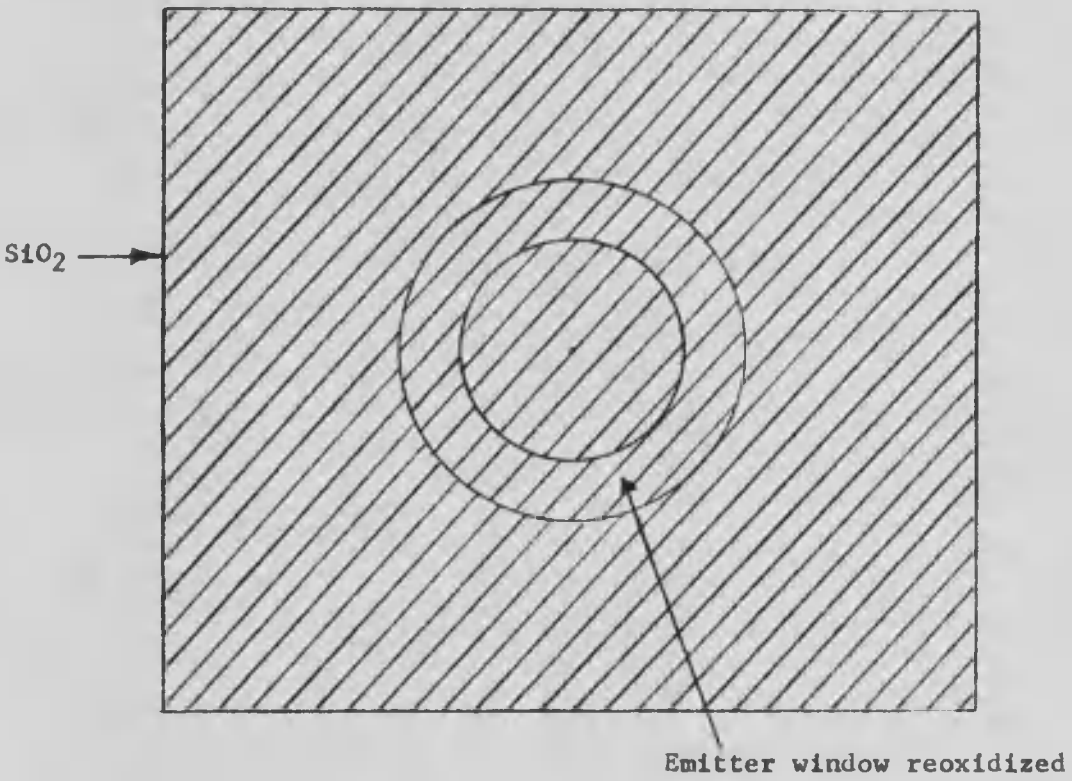
The emitter diffusion (p-type) was performed in an oven heated to 1051°C. with the flat zone held within 0.5 degree of 1051°C. Diborane gas was used as the doping source. During the diffusion the flow rates of the various gases through the 60 mm barrel of the furnace were as follows: 500 cc per minute of 1000 parts per million diborane in argon, 15 cc per minute of oxygen, and 500 cc per minute of nitrogen. The diffusion time was 22 minutes.

The wafers were then placed in the 1098° ± 0.5 °C oven for the impurity distribution and regrowth of the silicon dioxide layer. The wafers remained in this oven for 1.0 hour with the following flow rates through the 60 mm barrel: 500 cc per minute of oxygen and 500 cc per minute of oxygen bubbled through 92°C. water. The regrowth of silicon dioxide on the exposed silicon surface was 0.4 micron thick, which was sufficient protection against future diffusions (Keonjian, 1963).

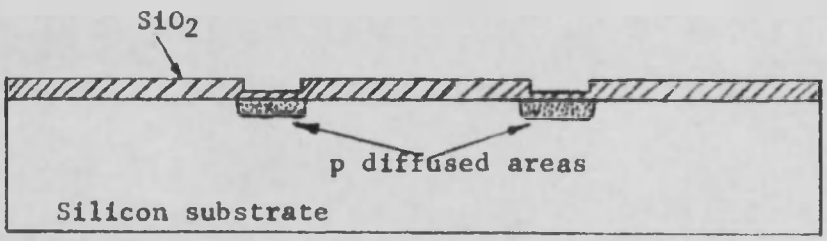
Since an oxide layer was regrown immediately after diffusion, most of the impurity atoms were trapped in the silicon and could not out-diffuse during the 1.0 hour of distribution time. The junction depth after the distribution time was measured to be 2.3 microns, and the sheet resistance was measured to be 175 Ω/square. Figure 3.4 shows two views of the wafer after the p-type diffusion.

N-type Diffusion, Drive-in, and Reoxidation

After the p-type emitter diffusion and distribution was completed, the wafers were recoated with photoresist and the entire process repeated, except that this time the n-type mask was used to etch



(a) Top view.



(b) Cross-sectional view taken through the center of the device.

Figure 3.4 Two views of the UJT showing the p-type diffusion and regrown layer of silicon dioxide.

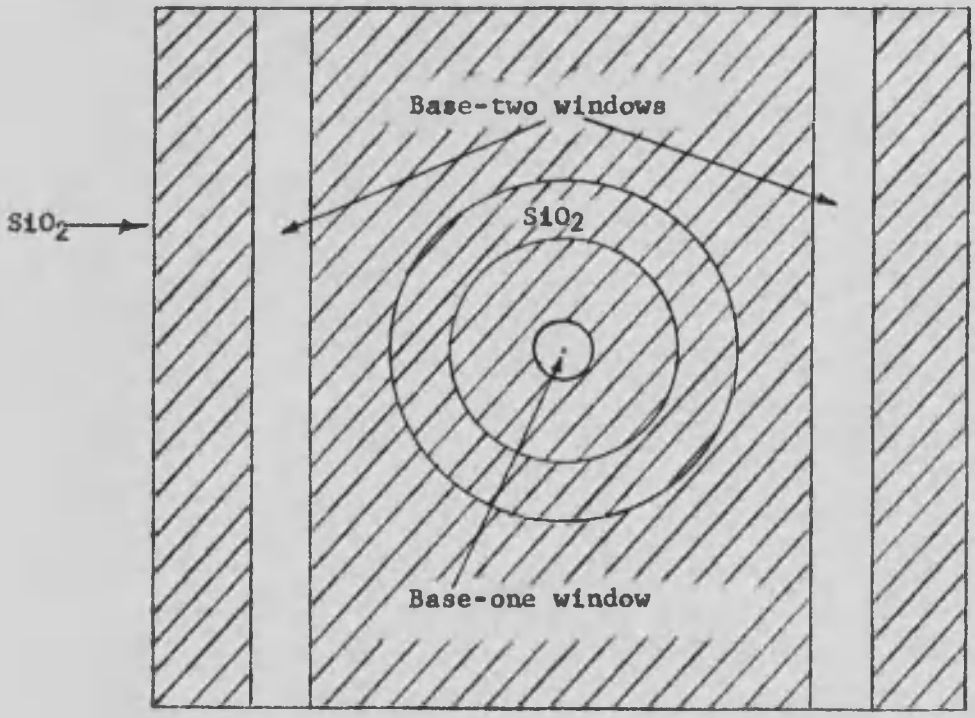
the silicon dioxide layer. The n-type mask was necessary to permit the formation of ohmic contacts on the surface of the lightly doped n-type wafer. Figure 3.5 illustrates the two views of the wafer after the windows were cut for the n-type diffusion.

The n-type diffusion was performed in an oven heated to 1051°C. with the flat zone of the oven held within 0.5 degrees of 1051°C. Phosphine gas was used as the impurity source. During the diffusion the flow rates of the various gases through the 60 mm barrel of the furnace were as follows: 500 cc per minute of 1000 ppm phosphine in argon, 15 cc per minute of oxygen, and 500 cc per minute of nitrogen. The diffusion time was 15 minutes and the resulting sheet resistance was 7 ohms per square.

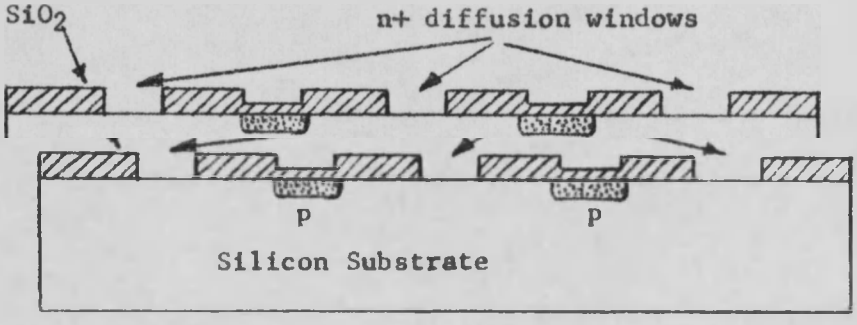
The wafers were then oxidized in the 1102° $\pm$ 0.5°C. oven for 15 minutes. The gas flow during this time was composed of 500 cc per minute of oxygen and 500 cc per minute of oxygen bubbled through 92°C. water. The two views of the wafer in Fig. 3.6 show the n+ diffusion and the subsequent regrowth of silicon dioxide.

The purpose of this 15 minute distribution and oxidation was not only for distribution of the impurities, but was also for the oxide regrowth. The oxide layer forms a surface to which the photoresist can adhere, while photoresist adheres poorly to an n+ wafer surface due to the presence of phosphorus glass on the surface.

As the oxide grows on the silicon, the n-type impurities (phosphorus) tend to pile up on the surface of the silicon because the phosphorus atoms have little relative affinity for silicon dioxide in

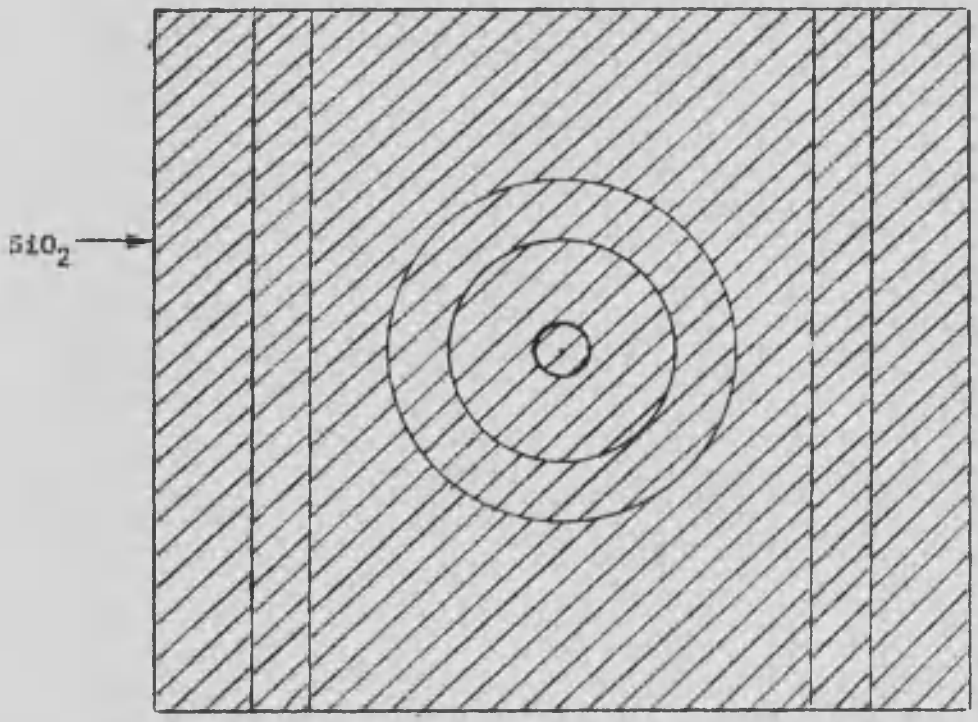


(a) Top view.

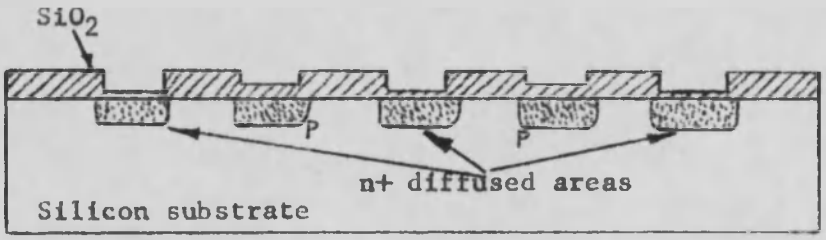


(b) Cross-sectional view taken through the center of the device.

Figure 3.5 Two views of the UJT showing the addition of windows cut for the n-type diffusion.



(a) Top view.



(b) Cross-sectional view taken through the center of the device.

Figure 3.6 Two views of the UJT showing the n+ diffusion and the subsequent regrowth of silicon dioxide.

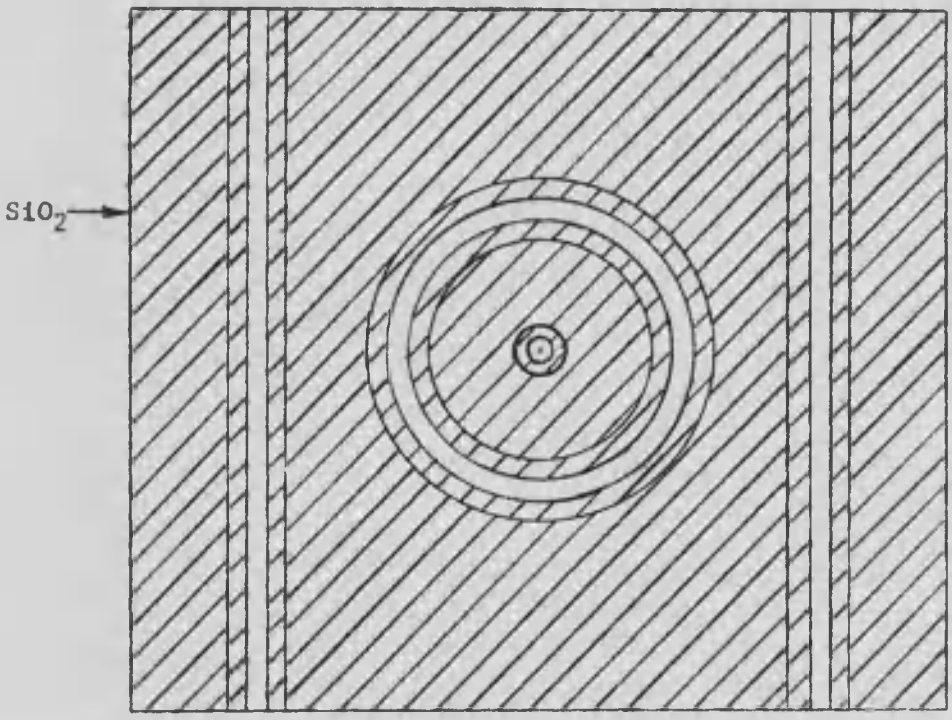
comparison with the silicon. This is called the snowplow effect and tends to increase the surface impurity concentration (Research Triangle Institute, 1964b). This is a desirable effect since a high surface concentration of n-type impurities is necessary for a good ohmic contact. Thus the 15 minute oxide growth after the n+ diffusion not only provides a more desirable impurity distribution due to the snowplow effect, but it also provides a surface to which photoresist adheres more readily.

Again, the wafers were recoated with photoresist and the entire photoresist process duplicated using the cut-before-metallization mask. This mask provided windows through the silicon dioxide to the silicon so that the electrical contact could be made. This is illustrated in Fig. 3.7.

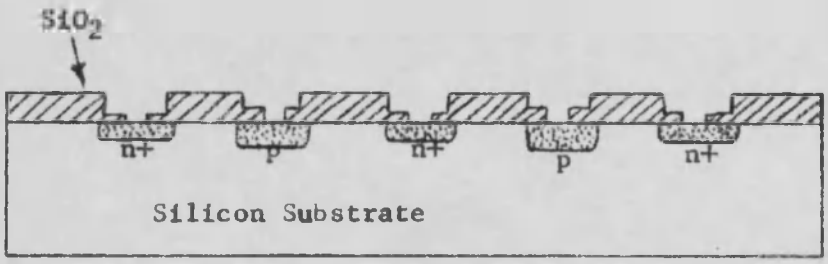
The wafers were then stored in isopropyl alcohol to prevent any reoxidation from forming over the recently cut windows, since small amounts of silicon dioxide form even at room temperature in air.

Metallization Process

The metallization step which followed consisted of placing the wafers in a high vacuum bell jar and depositing a thin layer of aluminum over the entire surface. The aluminum was heated and evaporated and, due to the high vacuum, the mean-free path of the aluminum atoms was much greater than the distance from the aluminum source to the wafers. Thus, the aluminum atoms radiated in all directions and struck and coated the wafers. The thickness of the aluminum depostion was 2500 Å and the deposition took place in a vacuum of 5×10^{-5} torr. The wafer was heated during the deposition process to a temperature of 200°C. by



(a) Top view.



(b) Cross-sectional view taken through the center of the device.

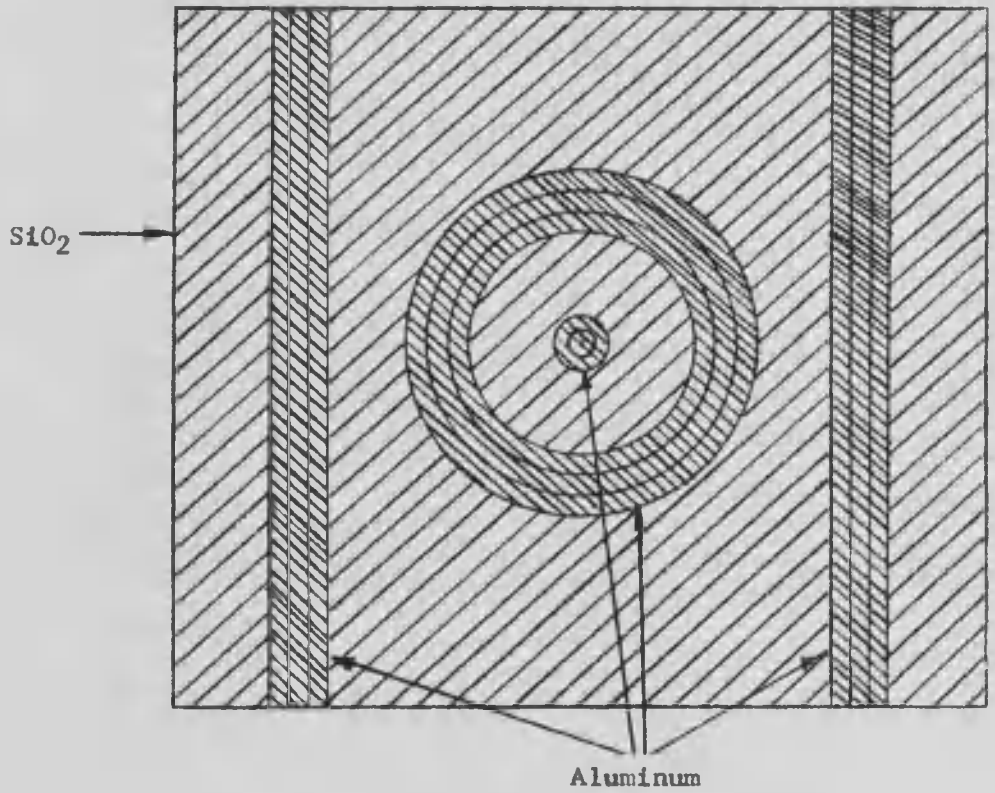
Figure 3.7 Two views of the UJT showing the etch through the silicon dioxide prior to the metallization step.

means of a substrate heater. This increased the adhesion of the aluminum to the wafer.

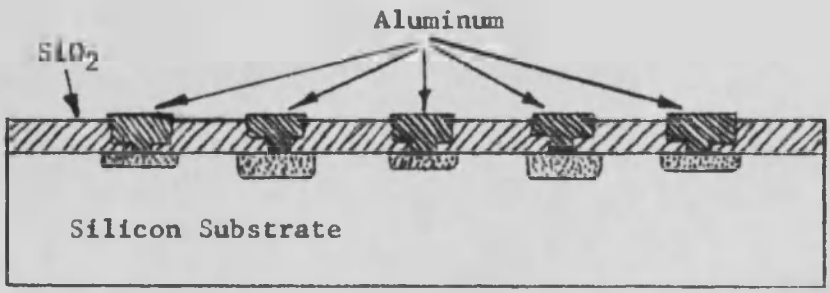
Since the aluminum now covered the entire surface, the aluminum had to be etched to isolate the various electrical contacts, and this is the function of the fourth and final mask, the metallization mask. As before the wafers were coated with photoresist and the entire photoresist process was repeated using the metallization mask. However, this time the wafers were etched in an aluminum etch instead of the silicon dioxide etch. The aluminum etch was composed of 4 ml of HNO_3, 18 ml of H_2O, and 80 ml of H_3PO_4. The areas of aluminum that were protected by the photoresist and thus not etched away formed ohmic contacts with the various regions in the wafer. At this point the UJTs were electrically operable and could be tested, although most of the testing was performed after the sintering process. The appearance of the wafer at this point is shown in Fig. 3.8.

The Sintering Process

The sintering process was accomplished by heating the wafer to a temperature of 500°C. in an atmosphere of forming gas (10% hydrogen, 90% nitrogen) for 5 minutes. The sintering process helps form an even better ohmic contact to the silicon surface and it also increases the adhesion of the aluminum. In the sintering step, aluminum diffuses through any thin layer of silicon dioxide that may have formed between the silicon and aluminum.



(a) Top view.



(b) Cross-sectional view taken through the center of the device.

Figure 3.8 Two views of the UJT after the deposition and etch of the aluminum layer.

Encapsulation

The wafers were now easily probed and tested, and the results of the testing is given in the next chapter. When a row of UJTs proved to be satisfactory, the wafer was diced, and the good dies were cemented to a 10-pin header. Sairset fire brick cement, which is an electrical insulator, was used for this purpose. One mil diameter wire leads were thermocompression ball bonded from the die to the package leads, and the entire device was encapsulated in a TO-5 package. The ball bonding process required the header and die to be heated to a temperature of 320°C. to 340°C. The row of UJTs were now ready to be utilized as a neuristor.

Chapter 4

UNIJUNCTION TRANSISTOR PERFORMANCE

Experimental Results

The UJTs that were fabricated in the laboratory performed with the desired characteristics prior to the sintering process, and although the characteristics were altered by sintering, the characteristics were still favorable with some units. Many units were bonded and encapsulated without being sintered, and a high percentage of these devices met all the desired characteristics. During the wire bonding process these devices were "sintered" at 330°C. instead of 500°C.

The input characteristics of a typical UJT fabricated in the laboratory is shown in Fig. 4.1. These curves were recorded from a device before it was sintered. From this figure the standoff ratio was measured to be about 0.7, although there were slight variations as a function of the interbase voltage V_{BB}. There is a large peak voltage to valley voltage ratio, making this device a suitable one for a neuristor circuit.

There were some problems encountered because the reverse breakdown voltages of the p-n junction diodes were 5 to 10 volts, instead of the several hundreds of volts that was expected due to the high resistivity n-type material. It was first thought that the low breakdown voltages were due to defects in the wafer surface, such as scratches and other forms of mechanical damage, but later it was found

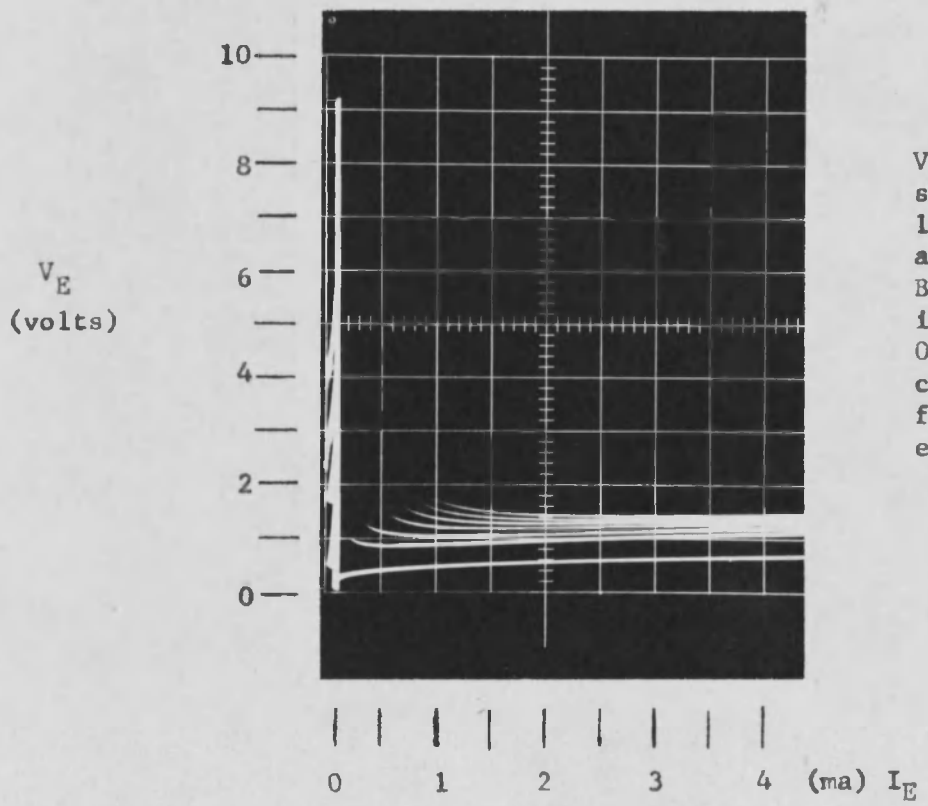


Figure 4.1 Measured input characteristics of the UJT.

that the low breakdowns were due to contamination of the wafer. Improved cleaning procedures eliminated this problem.

Performance as a Function of the Shape and Size of the UJT

Table 4.1 summarizes the operating characteristics of the design shown in Fig. 2.4, as well as the other designs shown in Figs. 2.6 and 2.7. This table shows that the designs in Figs. 2.4, 2.6(a), 2.6(b), 2.6(f), 2.6(g), 2.6(h), 2.7(b), 2.7(c), 2.7(d), and 2.7(e) all have standoff ratios of 0.6 or greater. Figures 2.6(f), 2.6(g), 2.6(h), 2.7(b), 2.7(c), and 2.7(d) are all smaller than the other designs and thus are more suitable. Since the design in Fig. 2.7(b) has accurate and easily drawn artwork, along with a high standoff ratio and small size, this design seems to be well-suited for the neuristor realization.

The experimental device characteristics (Fig. 4.1 and Table 4.1) and the calculated characteristics (Fig. 2.5) are similar in some ways and quite different in other ways. The experimental results are superior, in most respects, to the predicted results. This indicates that the mathematical model used for derivation of Eq. (2.9) may not be as complete as desired.

The experimentally measured standoff ratio of most of the designs is very close to the calculated value of 0.6. The low values of η for the designs of Figs. 2.6(c), 2.6(d), and 2.7(f) are due to the particular device geometry, and the low values were expected.

The valley voltage for all devices was measured to be lower than the predicted values in Fig. 2.5. This may be due to the incomplete model, or it may be due to an unusually large minority carrier lifetime

Table 4.1

SUMMARY OF THE OPERATING CHARACTERISTICS OF VARIOUS UJT DESIGNS

Description of the UJT	η	V_{BB}*	V_p	V_v	V_{BB} = 10 v.	
					V_p	V_v
Figure 2.4	0.6	15	8.8	3.7	6.0	3.0
Figure 2.6(a)	0.7	29	20	6.0	7.3	4.4
Figure 2.6(b)	0.6	30	19	3.0	6.0	2.4
Figure 2.6(c)	0.55	30	16	2.5	5.6	1.9
Figure 2.6(d)	0.45	30	13	3.0	4.7	1.8
Figure 2.6(e)	0.6	30	17	3.0	5.8	1.8
Figure 2.6(f)	0.75	30	23	4.0	7.3	2.5
Figure 2.6(g)	0.6	30	18	3.5	5.7	2.3
Figure 2.6(h)	0.75	30	23	4.0	7.7	3.4
Figure 2.7(a)	0.55	15	7.5	2.3	5.1	1.9
Figure 2.7(b)	0.7	30	22	4.0	7.0	2.1
Figure 2.7(c)	0.6	16	9.5	2.3	6.0	1.9
Figure 2.7(d)	0.6	30	18	3.0	6.0	1.7
Figure 2.7(e)	0.8	18	14	5.0	8.2	3.7
Figure 2.7(f)	0.4	23	8.5	2.0	4.0	1.6

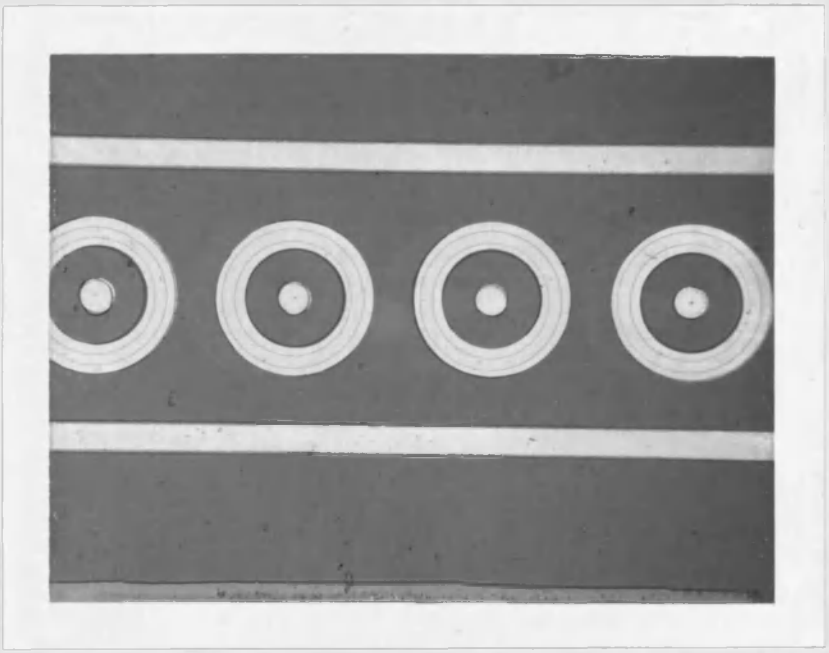
*This value of V_{BB} is either the largest value at which reverse breakdown does not occur, or 30 volts, whichever occurs first.

in the substrate. The effect of minority carrier lifetime is taken into account in Eq. (2.12).

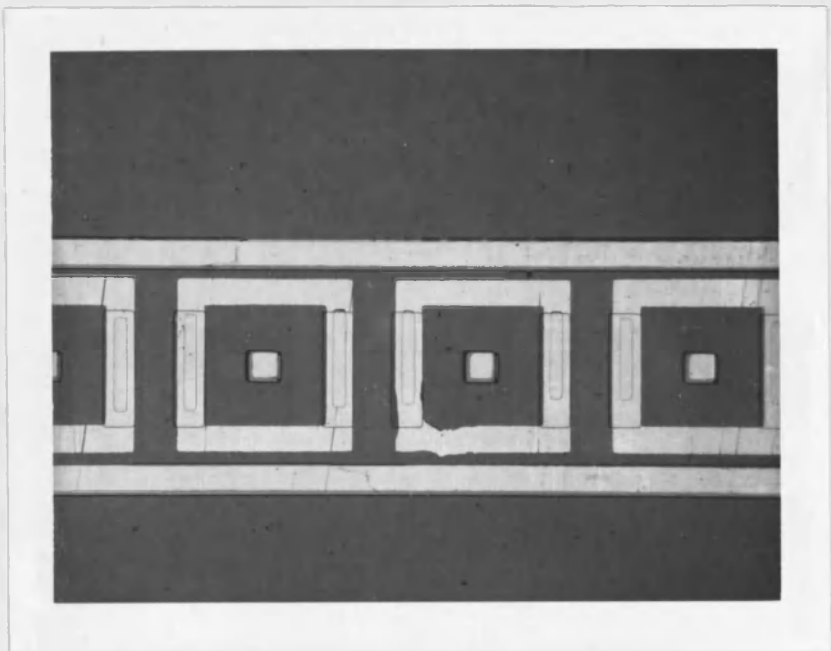
The interbase resistance was measured to be between 3kΩ and 5kΩ for all devices. This is reasonably close to the predicted value of 5kΩ.

A peak voltage to valley voltage ratio of up to 6:1 was realized. This large ratio permits simple biasing of the neuristor circuit, and was a much larger value than predicted.

Shown in Fig. 4.2(a) is a photograph of four UJTs of the design shown in Fig. 2.4. The most suitable design, Fig. 2.7(b), is shown in Fig. 4.2(b). The criteria for this decision were a large standoff ratio and a large peak to valley voltage ratio.



(a) Design 2.4



(b) Design 2.7(b)

Figure 4.2 Pictures of processed wafers showing the designs from Figs. 2.4 and 2.7(b).

Chapter 5

CONCLUSION

Evidently the design of Fig. 2.7(b) is the most suitable design for a UJT for the realization of the neuristor, although many of the designs were acceptable.

The process used in fabricating the UJTs was acceptable, although certain difficulties were encountered, such as the inability to obtain satisfactory devices after the sinter process. In spite of these problems, good devices were fabricated. Future work should strive to eliminate these deficiencies so that more reliable devices can be produced with higher yields.

Investigation can also be carried on concerning the reduction of the size of the device. This will be practical as soon as there is a two-step photographic reduction process available in the laboratory. The two-step photographic reduction process is necessary to get larger total reductions. The reduction ratio at the present time is limited to 35 to 1.

Preliminary tests indicate that the neuristor can be successfully realized using the lines of UJTs that were described in this thesis (Lillis, 1967). The fabrication of lines containing eight or ten unijunction transistors should permit that realization.

Appendix A

CALCULATION OF THE SPACING BETWEEN BASE-ONE AND BASE-TWO

The resistance R_{BB} is the resistance between base-two and base-one of the unijunction transistor shown in Fig. A-1. The distance r_1 is assumed and the distance r_4 is calculated so that R_{BB} is the resistance between r_1 and r_4.

Basic equations:

$$J = \sigma E \tag{1}$$

$$I = JA \tag{2}$$

$$V = -\int_{r_1}^{r_2} E\,dr \tag{3}$$

The current passing under r_4 is equal to the current passing under r_1. Current is assumed to flow in only one plane. Thus, the emitter region and base regions are assumed to extend to a depth of w.

$$I = JA = J_{r_4}(\text{area under } r_4) = J_{r_1}(\text{area under } r_1) \tag{4}$$

$$I = J_{r_4} \times 2\pi\, r_4\, w = J_{r_1} \times 2\pi\, r_1\, w \tag{5}$$

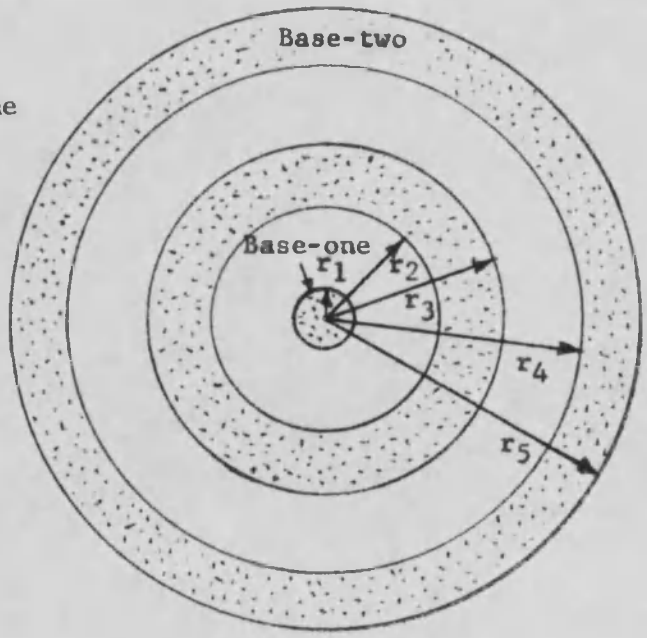
$$J_r\, r_4 = J_{r_1} r_1 \tag{6}$$

Thus

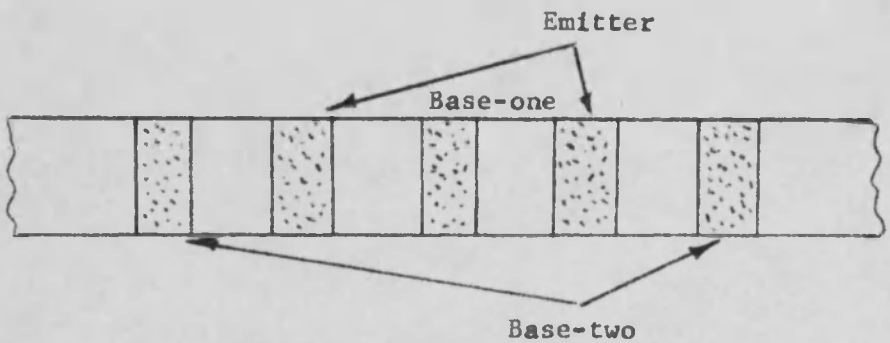
$$J_{r_4} = J_{r_1} \frac{r_1}{r_4} \tag{7}$$

Since $$E = \frac{J}{\sigma} \tag{8}$$

w = depth (into paper) of the UJT.



(a) Top view.



(b) Cross-sectional view.

A-1 UJT with dimensions for the calculation of R_{BB}.

Then by substitution

$$E_{r_4} = \frac{J_{r_5}}{\sigma} = \frac{J_{r_1}\, r_1}{\sigma\, r_4} \tag{9}$$

For any r such that $r_4 > r > r_1$

$$E_r = \frac{J_{r_1}\, r_1}{\sigma\, r} \quad . \tag{10}$$

Since

$$V = -\int_{r_1}^{r_2} E\, dr \tag{11}$$

and

$$V_{(r_1 \text{ to } r_4)} = -\int_{r_1}^{r_4} \frac{J_{r_1}\, r_1}{\sigma}\, dr = -\frac{J_{r_1}\, r_1}{\sigma} \int \frac{dr}{r} \tag{12}$$

then by integration

$$V_{(r_1 \text{ to } r_4)} = -\frac{J_{r_1}\, r_1}{\sigma} [\ln r_4 \quad \ln r_1] = -\frac{J_{r_1}\, r_1}{\sigma} \ln \frac{r_4}{r_1} \tag{13}$$

Substituting for J_{r_1}

$$V = -\frac{I\, r_1}{2\pi\, r_1\, w\, \sigma} \ln \frac{r_5}{r_1} = -\frac{I \ln \frac{r_4}{r_1}}{2\pi\, w\, \sigma} \tag{14}$$

$$R = \frac{V}{I} = \frac{\ln \frac{r_4}{r_1}}{2\pi\, w\sigma} = \frac{\rho \ln \frac{r_4}{r_1}}{2\pi\, w} \tag{15}$$

Let

$R = 5\ k\Omega$

$r_1 = 1.5$ mils

$\rho = 150\Omega$-cm

$$w_{(effective)} = 5 \text{ mils} = 1.20 \times 10^{-2} \text{ cm}$$

Then

$$\ln \frac{r_4}{r_1} = \frac{2\pi w R}{\rho} = \frac{2\pi \times 1.20 \times 10^{-2} \times 5000}{150} = 2.51 \tag{16}$$

$$r = 18.5 \text{ mils}$$

Now, if base-two is made into two parallel bars, such as in Fig. 2.2, the value of R_{BB} is increased. Thus, the value of r_4 must be reduced to maintain a constant value for R_{BB}.

Let r_4 be approximately equal to 10 to 13 mils.

Appendix B

CALCULATION OF THE VALUE OF r_2 IN FIGURE A-1

From Appendix A:

$$\underset{\substack{\text{(resistance}\\ \text{from } r_1 \text{ to } r_4)}}{R} = \frac{\rho \ln \frac{r_4}{r_1}}{2\pi w} \tag{17}$$

so

$$\underset{\substack{\text{(resistance}\\ \text{from } r_1 \text{ to } r_2)}}{R_{B1}} = \frac{\rho \ln \frac{r_2}{r_1}}{2\pi w} \tag{18}$$

Since $\eta \approx \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{R_{BB}}$ (19)

$$R_{B1} = \eta R_{BB} = 0.6 \times 5k = 3k\Omega$$

by substitution

$$R_{B1} = 3.0\ k\Omega = \frac{150 \ln \frac{r_2}{r_1}}{2\pi \times 1.2 \times 10^{-2}} \tag{20}$$

$$\frac{r_2}{1.5 \text{ mils}} = 4.53$$

then

$$r_2 \approx 7 \text{ mils}$$

This is assuming that the base-two is circular. If base-two is made into two parallel bars, such as in Fig. 2.2, the value of η is decreased. In order to keep the standoff ratio constant, r_2 must be increased. Let the value of r_2 be approximately 9 mils.

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