NEURISTOR REALIZATION

by

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Roy H. Mattson — Jan. 9, 1968

Roy H. Mattson
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Date

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ABSTRACT

This work deals with the design and successful fabrication of neuristor lines in limited form. The neuristors are realized in semi-distributed form based on unijunction transistor monostable oscillator circuits.

The so-called "cylindrical geometry" for unijunction transistors is modified, and resistance paper analogs are used as a design aid to optimize certain characteristics. The optimum geometry determined from the analog, is then scaled down and fabricated in single crystal silicon slices by planar techniques.

The test data for several variations on the geometry and the conclusions drawn from these data are presented. Finally, the characteristics of these neuristor lines are determined.

Chapter 1

INTRODUCTION

As electronic systems became more miniaturized, often a large loss in electrical power occurred in the small diameter wires used for component and system interconnections. This was true in both component and hybrid integrated systems and to a lesser degree in large scale integration (LSI) of monolithic circuits. While searching for a means to circumvent these increased transmission losses, H. D. Crane [1960] considered the use of active transmission paths, similar in nature to nerve axons. From this work a new class of device called neuristor was defined.

To understand neuristors, a description of axon nerve action is necessary. The axon part of a neuron is a long fiber or cord capable of transmitting electrical nerve impulses. While the axon is in its quiescent state, there exists an electrical potential difference across the semi-permeable membrane which makes up the wall of the neuron. The stored energy associated with this potential difference can be discharged by the application of a trigger pulse, usually chemical in nature but sometimes electrical, if triggered artificially. To trigger the nerve axon, the applied potential must exceed a threshold. After the threshold is exceeded and the axon is triggered, the discharge propagates along the neuron in both directions from the trigger point. The propagation of the discharge is lossless as the potential difference

supplies the energy which maintains it. The velocity of propagation depends on the size of the neuron. After being triggered, the neuron cannot immediately support another propagating pulse, since its stored energy has been depleted, for a fixed time. This time, called the refractory period, is the time it takes for the nerve fiber to recharge. Thus a dead-zone follows the leading edge of the discharge wave along the neuron. An interesting result of this phenomenon is the annihilation of two pulses during a head-on collision. The discharge wavefront of each pulse runs into the dead-zone of the other and disappears. Analogous to the nerve axon, the characteristics of the neuristor class of devices as proposed by Crane are:

1) Threshold stimulability
2) Attenuationless propagation
3) Uniform propagation velocity
4) Refractory period following the passage of a discharge.

Another characteristic of the neuron is its distributed nature.

Working with this postulated class of devices, Crane showed analytically that they could be used not only as mere connectors of logic elements but that they could also perform logic functions. Thus the neuristor is a truly "active wire" capable of performing new logic functions.

Neuristors can be connected in two basic types of junction, the T and S junctions. The T, or trigger junction, illustrated in Fig. 1.1, is a junction of m + 1 branches, such that when a discharge pulse

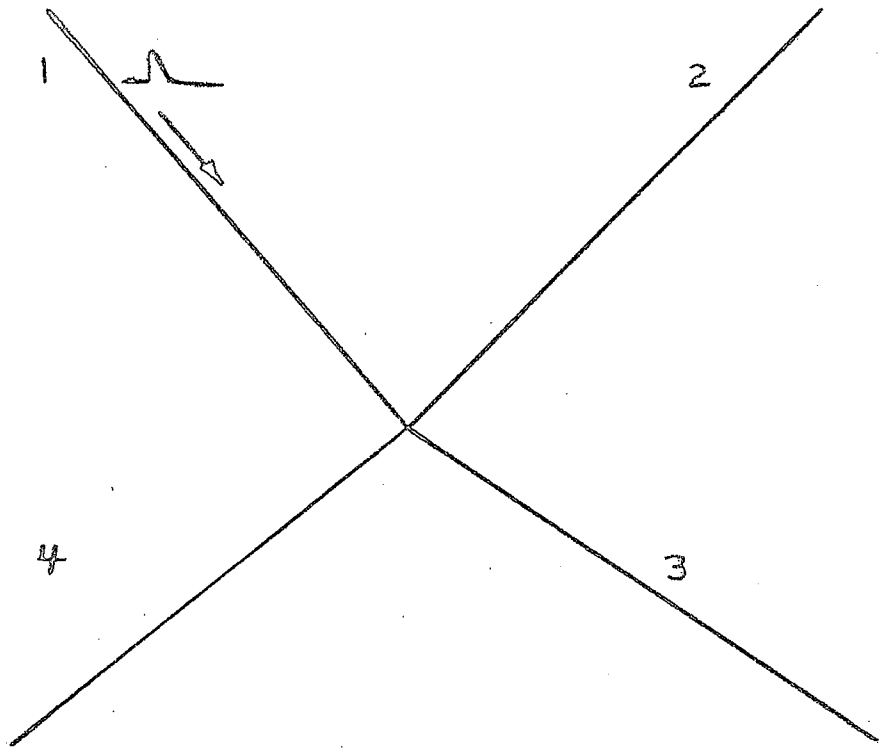


Fig. 1.1 Four Branch Neuristor T Junction

arrives at the junction on any one branch it actuates discharge pulses on the other m branches of the junction. This junction makes use of the stimulability characteristic, assuming one pulse to be sufficient to simultaneously exceed the m thresholds, and thus trigger the m lines. The S, or storage junction, illustrated in Fig. 1.2, relies for its operation on the refractory period characteristic. If m + 1 lines are joined such that they share a common energy storage facility at the junction, then, as a discharge pulse passes through the junction on any one of the m + 1 lines, it depletes the stored energy of the other m lines. The result is that transmission on any of the other m lines is inhibited for the duration of the refractory period.

Utilizing both T and S junctions, many logic operations including Boolean type gates, and the storage function may be constructed. Crane[9]'s work consists mainly of the consideration of such systems of logic. However, he notes that there is considerable importance in "the ability to develop simple techniques of physical realization".

Unfortunately, neurons themselves require rather elaborate support systems. Turning his attention to a purely electronic realization, Crane postulated a distributed thermistor-capacitor realization. He analyzed a semi-distributed lumped model of the proposed thermistor structure, and saw in its monostable mode of operation the possibility of neuristor action.

Several implementations of the neuristor have been attempted using relays, distributed tunnel diode structures, superconductive lines, four layer switches, and other approaches. The discrete component

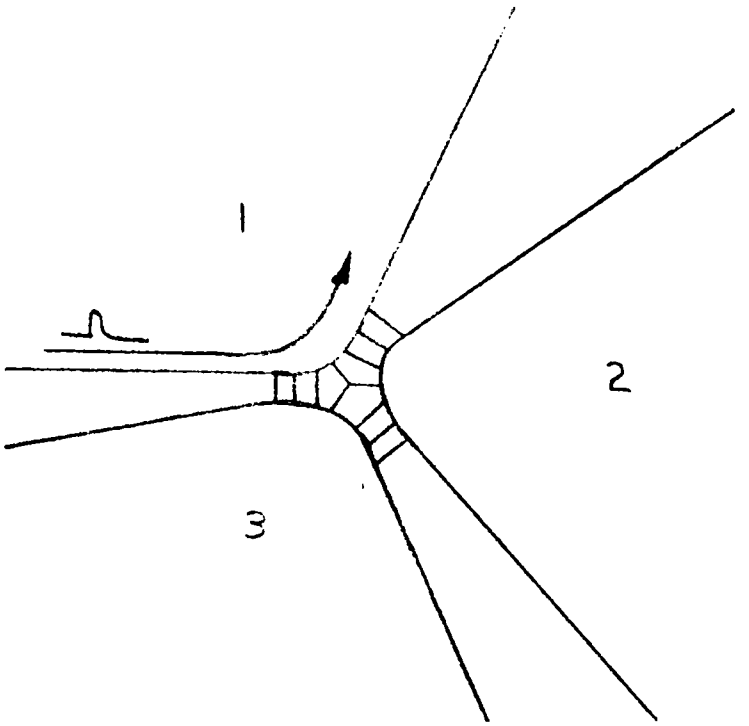


Fig. 1.2 Three Branch Neuristor S Junction

realizations, while successful in producing neuristor action were not very interesting since vast numbers of discrete components would be required to synthesize a line. While the distributed realizations incorporating negative resistance phenomena were successful in many respects, they often raised more questions than they answered. They also lacked repeatable characteristics and "simple techniques of physical realization". One conclusion drawn by A. J. Cote, Jr. [1965] from his work with a long distributed tunnel diode realization is of note. "Neuristor propagation has been measured in these long tunnel diode structures. But the propagation probably jumps between the discrete points at which bias is applied . . . ." This indicated that a semi-distributed structure might furnish a useful neuristor-like realization.

In early 1964, R. H. Mattson reported the successful operation of a semi-distributed neuristor line using unijunction transistors. A unijunction transistor, when biased as in Fig. 1.3 has the voltage-current characteristic shown in Fig. 1.4. The negative resistance phenomenon may be explained by the well-known fact that over a certain range, the conductivity of a semiconductor increases as the number of carriers increases. Under suitable conditions, the decrease in resistance caused by carriers, injected from the emitter into the base region can yield the negative resistance section of the V-I characteristic. The unijunction transistor monostable multivibrator circuit and the location of the quiescent load line on the characteristic curve are shown in Fig. 1.5 and Fig. 1.6 respectively. The bias voltage, V_B , is chosen such that

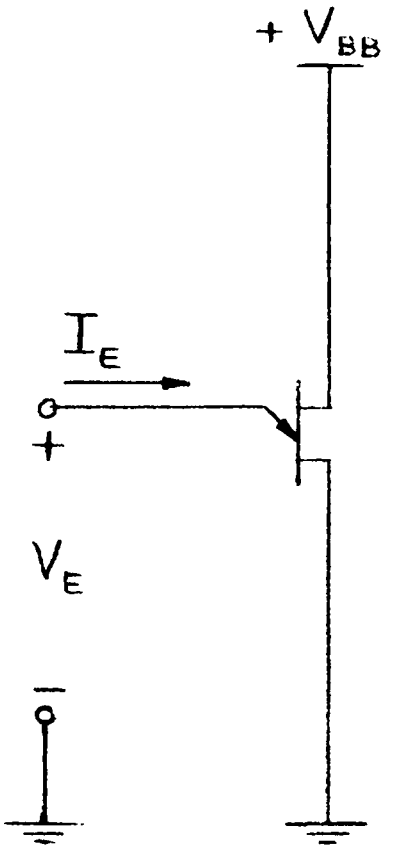


Fig. 1.3 Unijunction Transistor Circuit Arrangement

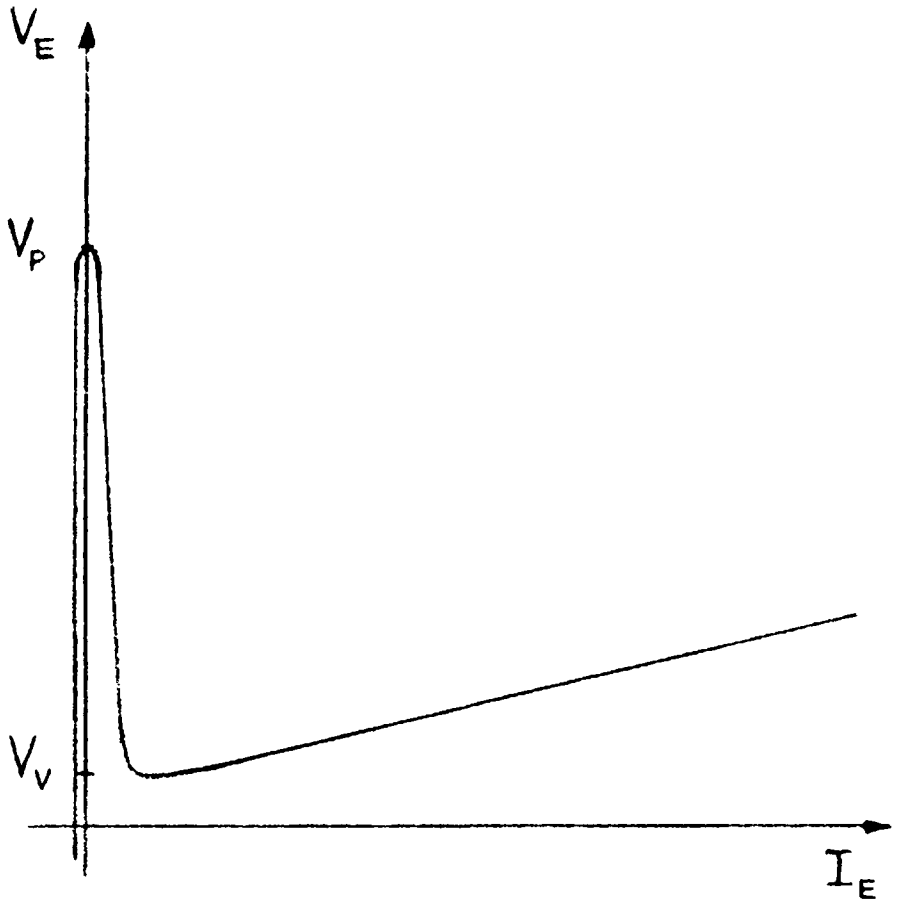


Fig. 1.4 Unijunction Transistor Emitter Characteristics

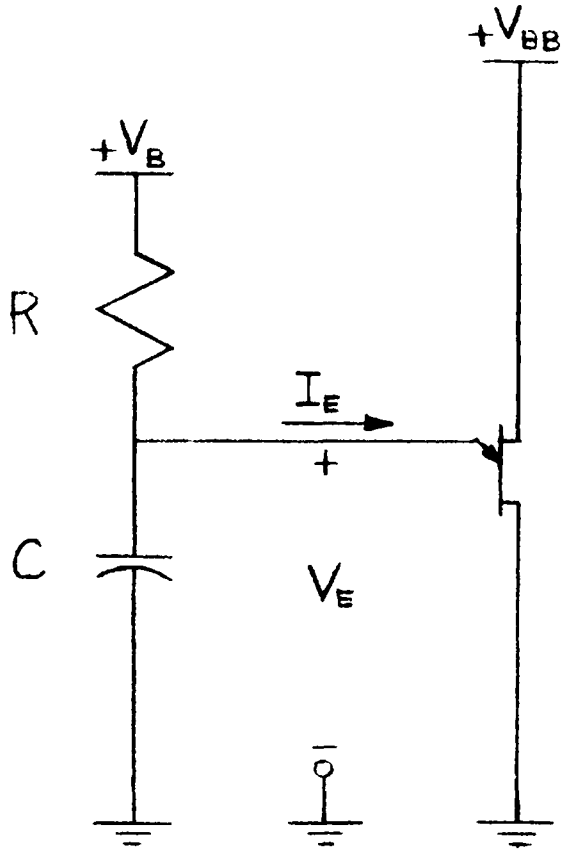


Fig. 1.5 Unijunction Transistor Monostable Oscillator Circuit

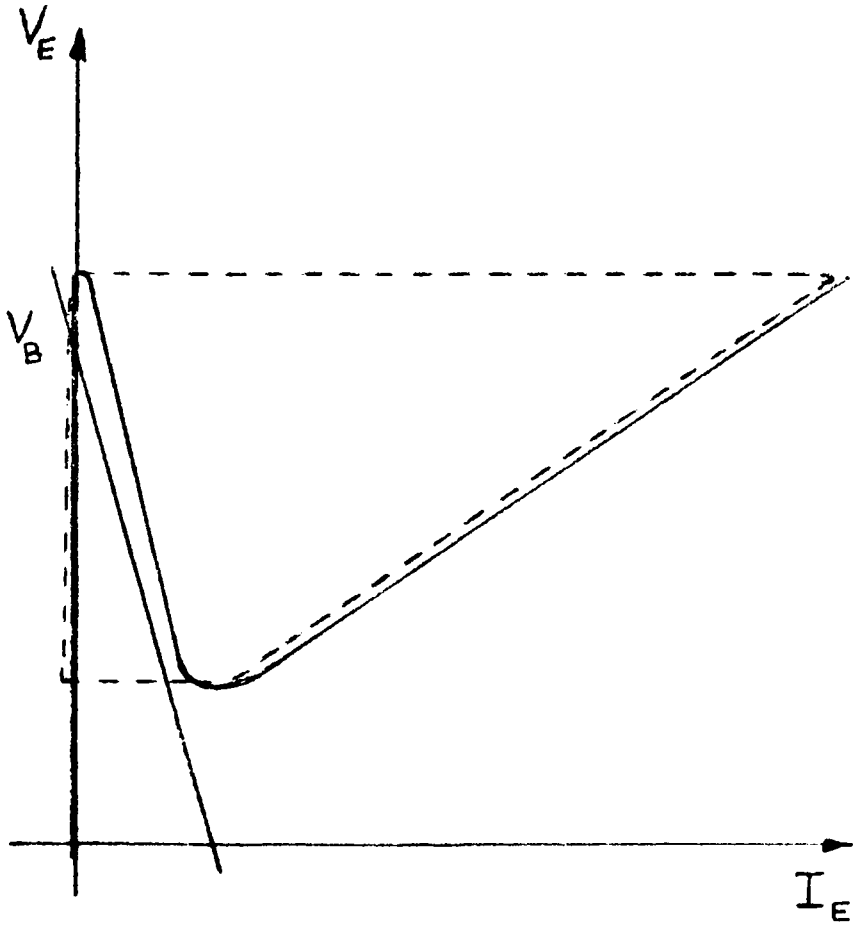


Fig. 1.6 Unijunction Transistor Monostable Oscillator Characteristic Including Load Line and Operating Path

it is slightly less than the peak voltage, V_p. When the unijunction transistor is triggered, the operating point follows the dotted line giving rise to a pulse in the time domain. The various times associated with the pulse are determined by the capacitor and the applicable resistances.

The neuristor realization achieved by Mattson took the semi-distributed form of Fig. 1.7. The emitters were biased as shown in the figure such that their operating points were just below the peak points of their respective characteristics. When unit one was triggered, its operating point followed the dotted line of Fig. 1.6. The emitter characteristic of the nearest neighbor is shown in Fig. 1.8. Curve A results when unit one is at its quiescent point. Curve B results when unit one is at its valley voltage, V_V. The reduction of the peak voltage results from the reduction of the effective supply voltage. In this case a similar cause can be found if we consider the lowered potential of the neighboring (triggered) unit as another bias source acting in conjunction with V_{BB} to provide the total supply for the region around the emitter of unit two. Since the biasing is as shown by the load line, the triggering of unit two results from its peak voltage being reduced, which is caused by unit one being fired. This process is repeated in time along the line and the result is a pulse propagating with no attenuation. The time required for the capacitor to fully discharge and then recharge to the bias point is the refractory time. The velocity of propagation is controlled by the R-C time constant associated with the discharge of the capacitor through the emitter, and by the physical spacing of the units.

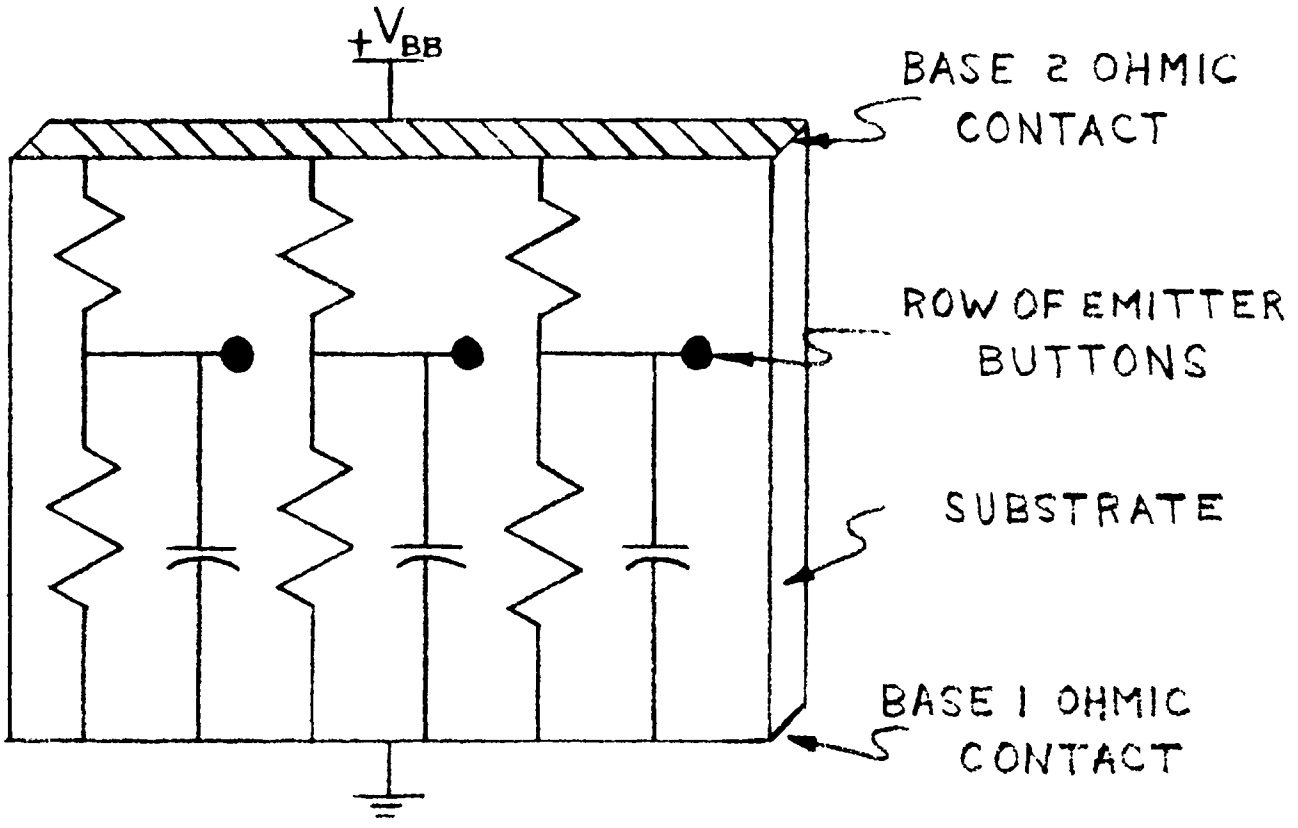


Fig. 1.7 Complete Neuristor Line Including External Lumped Circuitry

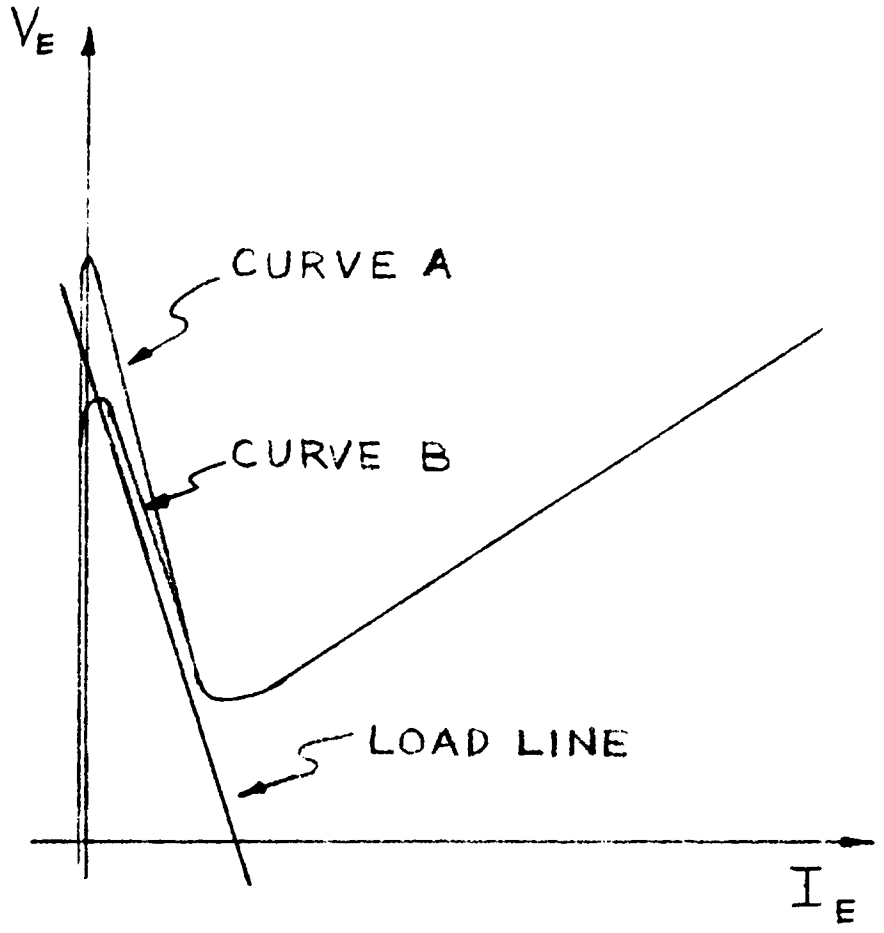


Fig. 1.8 Emitter Characteristics of Nearest Neighbor Unit

The first units to be fabricated by Mattson were realized with germanium alloy junction devices. Successful propagation was achieved, as were annihilation of pulses by head-on collision and T and S junction action. It was realized that germanium technology was not conducive to fabricating reliable, high quality neuristors by simple procedures. The advantage of employing silicon and utilizing the sophisticated techniques of monolithic circuit fabrication was apparent. A successful realization in silicon was made. It was also recognized that a modification of the geometry was necessary to avoid the problem of very high fields associated with T junctions as shown in Fig. 1.9. Another problem encountered was that of not only triggering the nearest neighbor when one unit fired, but also triggering the next-nearest neighbor. This led to some ambiguity in propagation velocity and junction operation. This thesis deals mainly with these two problems.

To overcome the high field region in T junctions, the "cylindrical" geometry used to fabricate individual unijunction transistors, as shown in Fig. 1.10, is modified [Wise, 1968]. The problem of multiple triggering is investigated by experimenting with various spacings between units and various channel widths.

In Chapter 2, the results of a resistance paper analog, employed to investigate these problems, are presented. Chapter 3 deals with the first order realization of the proposed unijunction transistors in silicon by monolithic integrated circuit techniques. The various experimental results for different geometric configurations are presented and analyzed. The operation of the lines as neuristors is treated in Chapter 4. The conclusions are presented in Chapter 5.

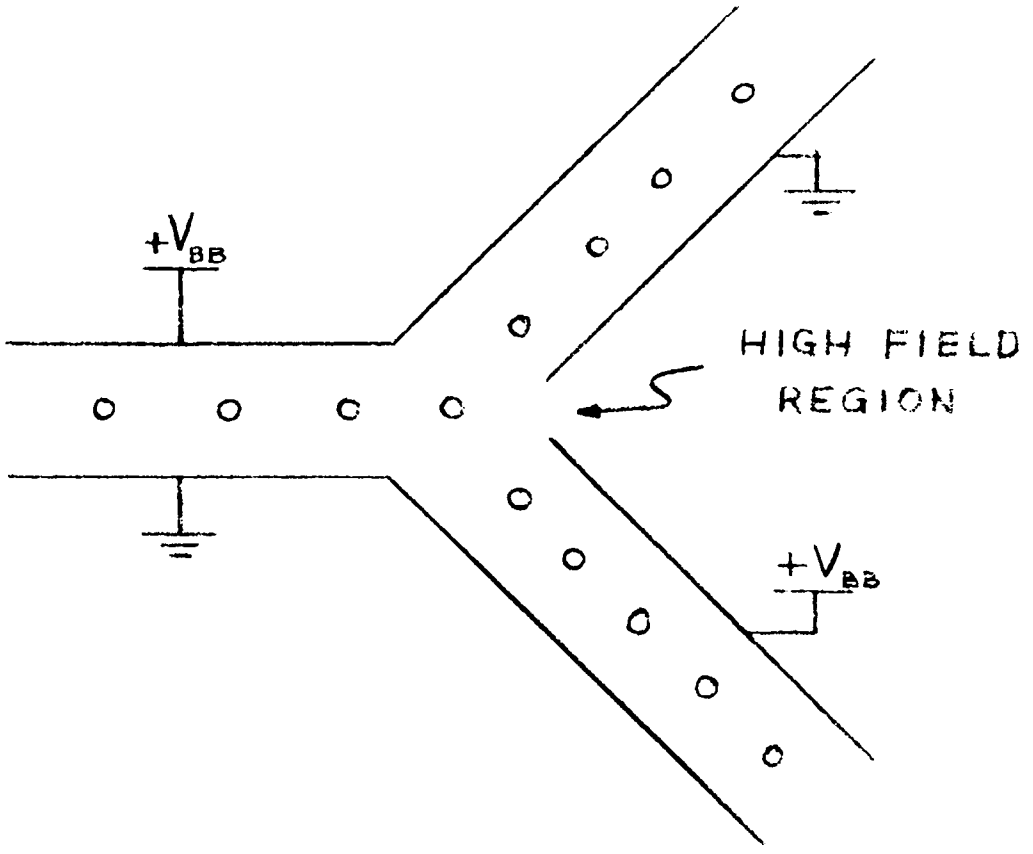


Fig. 1.9 Problem of High Field Region at T Junction in Adaptation of Bar Geometry

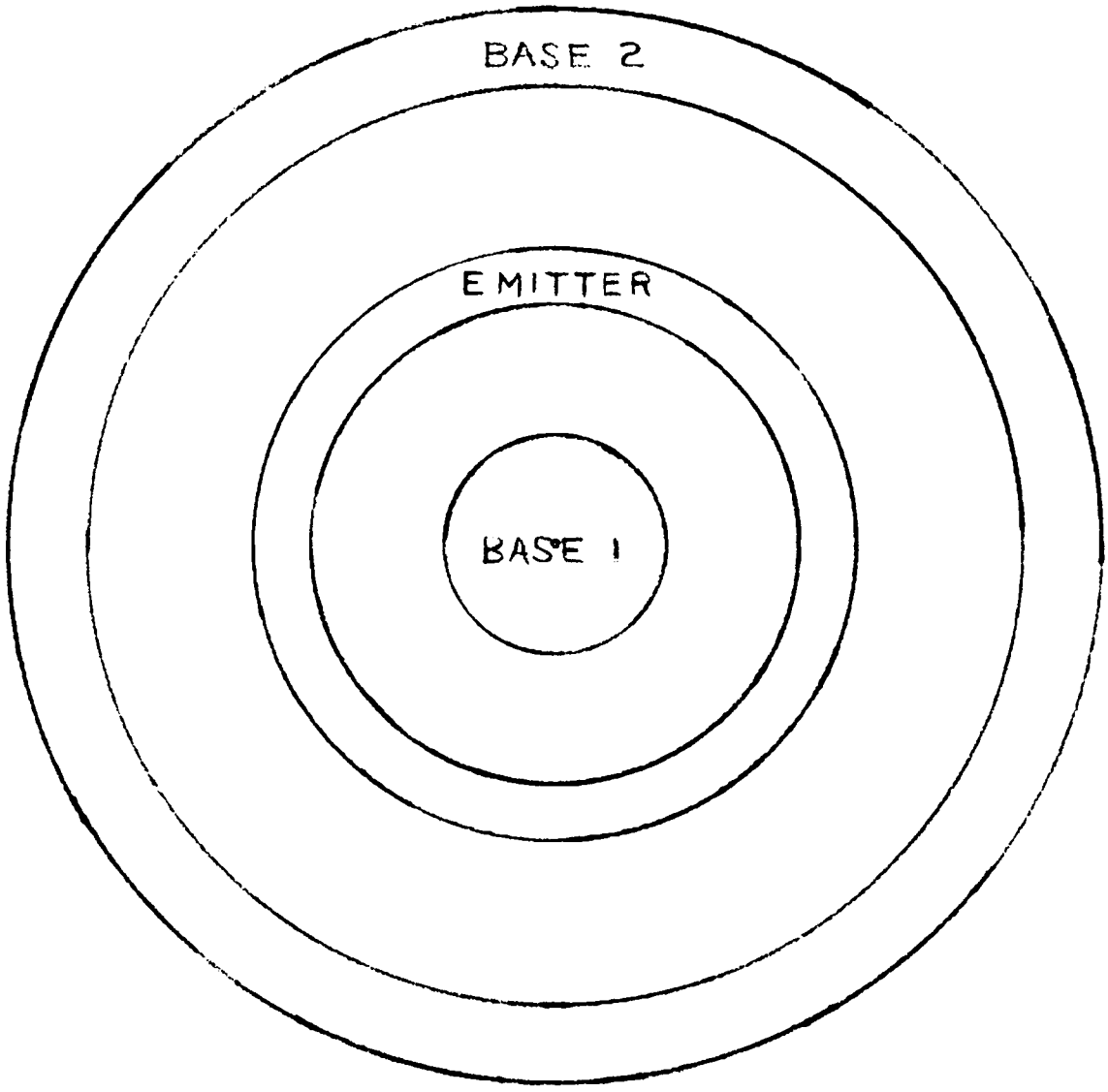


Fig. 1.10 Cylindrical Geometry Configuration of Unijunction Transistor

A limitation in the work presented here is the use of discrete, rather than integrated, components in conjunction with the unijunction transistor lines.

Chapter 2

GEOMETRY INVESTIGATION UTILIZING RESISTANCE PAPER ANALOG

Previous work indicated that ohmic coupling was the predominant mode of coupling between the elements in a semidistributed neuristor line realized using unijunction transistors. As one unit fired and entered its quasi-stable region of operation, the potential on its emitter dropped sharply and slowly recovered to its quiescent value. This reduced potential caused a redistribution of the electric field which resulted in a reduced potential in regions near the emitter of the fired element. If the emitter of the nearest neighbor was near enough, it would be triggered by this reduced potential. It was therefore advantageous to study the potential distributions in the proposed geometries.

For the most part, the geometries involved in the proposed realization were too complex for even the most elementary analysis of the static field conditions. As a result, analogs of these geometries were constructed employing resistance paper.

Resistance paper is paper impregnated with a substance that results in the sheet resistance of the paper being uniform over a very large region. The sheet resistance of the paper used was approximately 16,000 ohms per square.

The investigation was limited to the static field distributions, under certain conditions of bias. In constructing the analog, the

electrodes representing base-one, base-two, and the fired emitter were simulated on the paper by areas of constant potential realized with highly conductive paint. Using the equipment in Fig. 2.1, a null type method was employed in measuring the potentials at the points of interest. Using this method of measurement, the effect of the measuring instrument was minimized.

As a check on the linearity of both the paper analog and the measurement technique, the geometry of Fig. 2.2 was constructed and investigated. The analytical solution was obtained by solving Poisson's equation for the region between a and b.

$$\Phi = \frac{V}{\ell n\ (b/a)}\ \ell n\ (r/a) \qquad (2.1)$$

For convenience, values of a = 1 and b = 7.4 were chosen, with the result that

$$\Phi = \frac{V}{2}\ \ell n\ r \qquad (2.2)$$

The potential was measured at five points, corresponding to five values of r. These five points, and Eq. 2.2 were plotted as shown in Fig. 2.3. The close agreement between theory and experiment was evident.

This data indicated that both the paper and measuring technique introduced negligible error. Therefore, in the absence of a theoretical check, it was assumed the resistance paper model would yield good first order information on the potential distribution in the proposed neuristor line. It was realized that the results would be of limited value since the model was two dimensional and the device would be three dimensional.

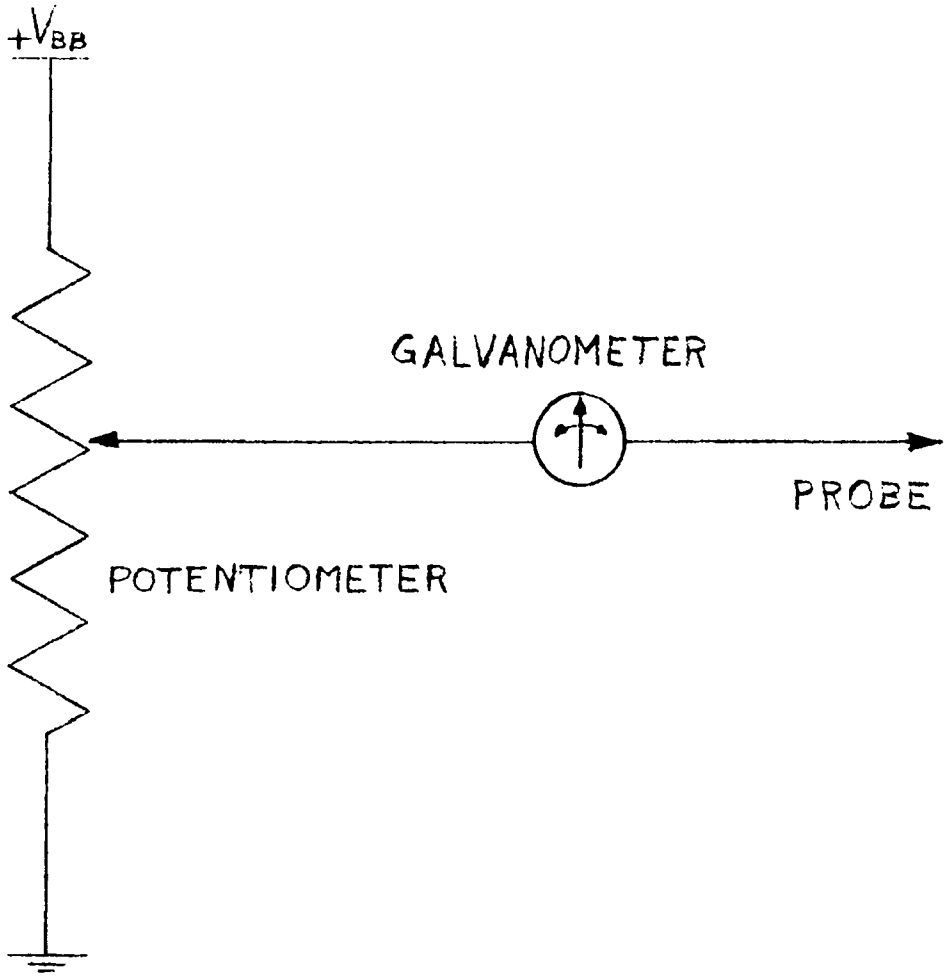


Fig. 2.1 Potential Measuring Equipment

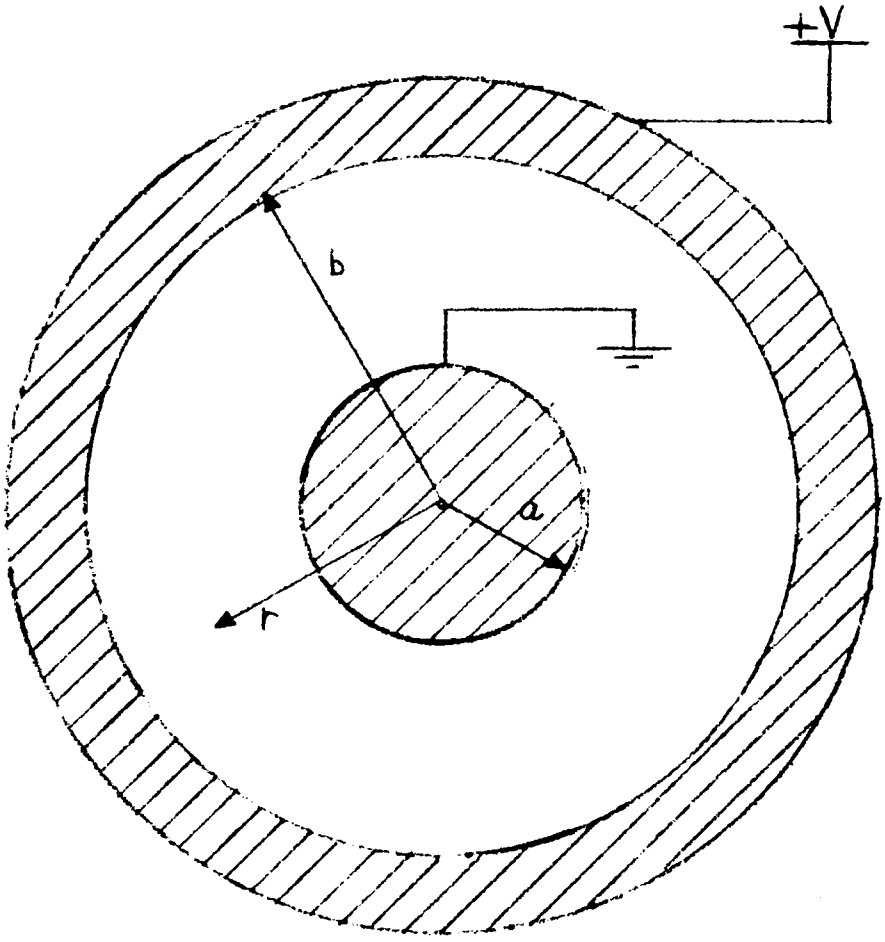


Fig. 2.2 Test Geometry for Resistance Paper

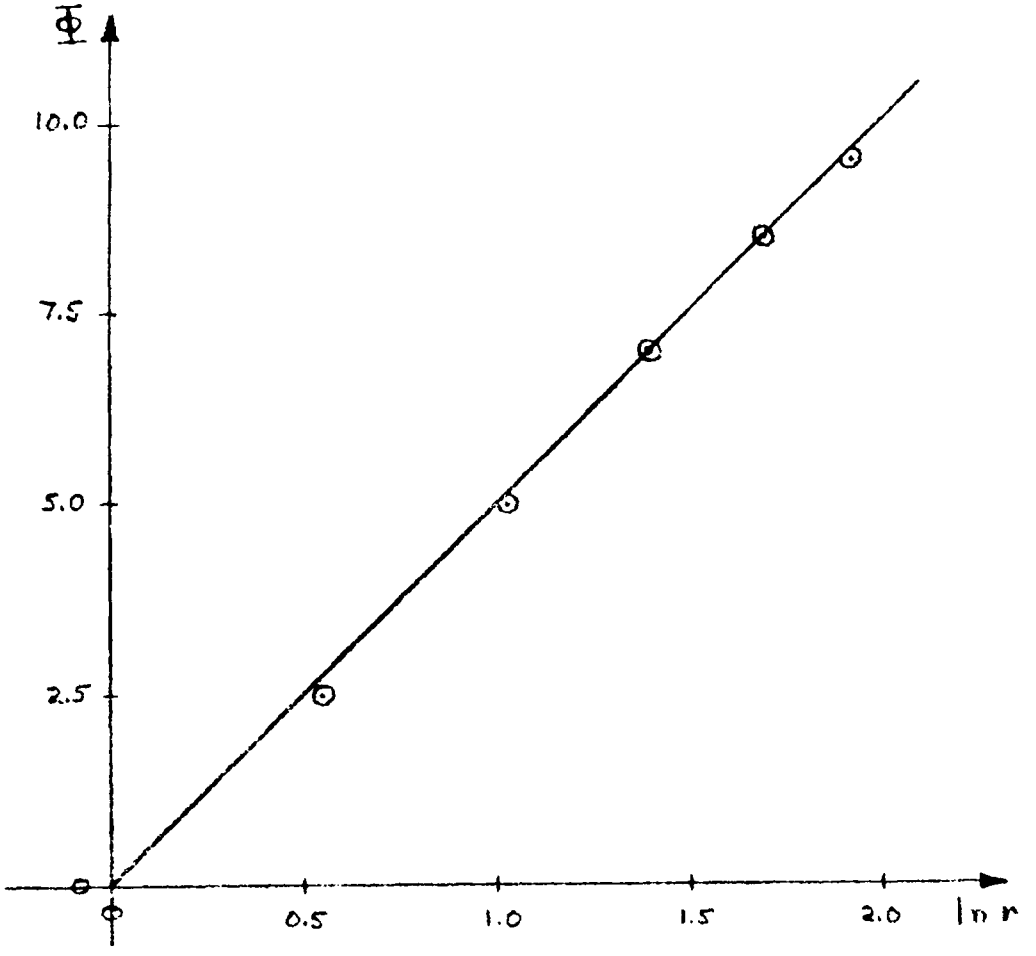


Fig. 2.3 Potential vs. Radius for Geometry of Fig. 2.2

The first two geometries investigated were slight perturbations of the closed cylindrical geometry of Fig. 1.10. The base-two contact region was opened on either end to permit coupling between units as is shown in Fig. 2.4. The position of the emitter ring was determined from a consideration of the intrinsic stand-off ratio of the unijunction transistor on which the model was based. The intrinsic standoff ratio is the ratio between the resistance from the emitter to base-one, with no emitter current flowing, and the resistance from base-two to base-one, again with no emitter current flowing. A standoff ratio of 0.68 was chosen as a typical value, and the inner and outer radii of the emitter ring were determined from the following equations for the closed cylindrical geometry.

$$R_1 = R_{e_1} - a = \frac{1}{2\pi\sigma} \ell n \ \frac{e_1}{a} \tag{2.3}$$

$$R_2 = R_{e_2} - b = \frac{1}{2\pi\sigma} \ell n \ \frac{b}{e_2} \tag{2.4}$$

$$\eta = \frac{R_1}{R_1 + R_2} = \frac{\ell n \ (e_1/a)}{\ell n \ (\frac{b}{a} \frac{e1}{e_2})} \tag{2.5}$$

$$\left(\frac{e_1 b}{e_2 a}\right)^{\eta} = \frac{e_1}{a} \tag{2.6}$$

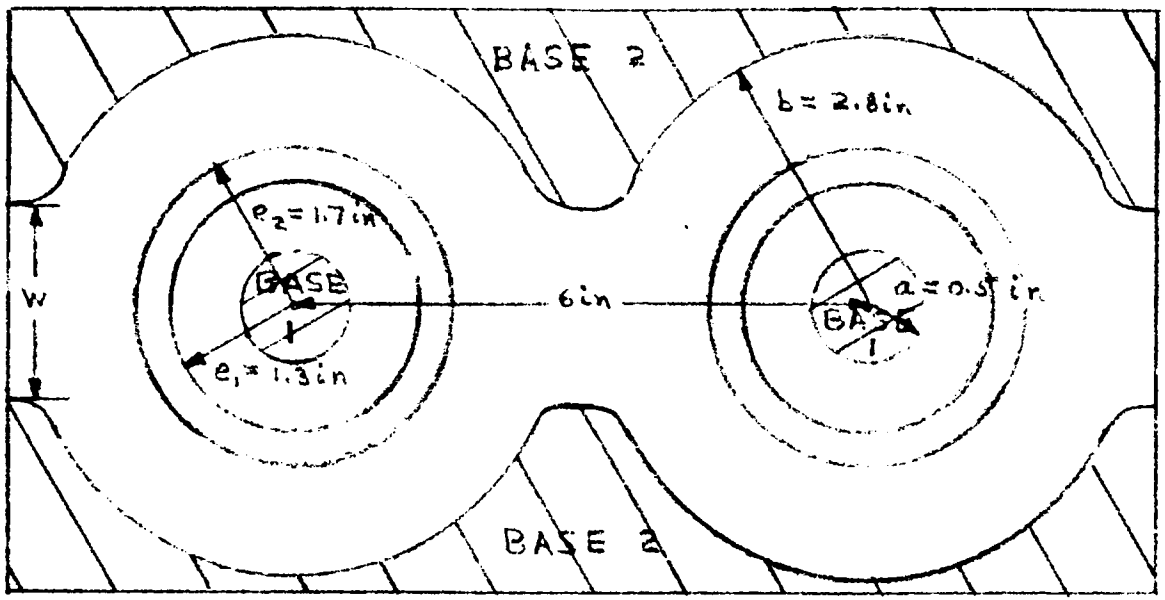
Where:

η = standoff ratio

a = base one radius

b = base two radius

e_1 = inner emitter radius



Geometry A W = 1 in.
Geometry B W = 2 in.

Fig. 2.4 Neuristor Test Geometries A and B

e_2 = outer emitter radius

The following values were chosen,

$e_2 = 1.2\ e_1$

$a = 1$ in.

$b = 2.8$ in.

The result was:

$e_1 = 1.8$ in.

$e_2 = 2.1$ in.

The purpose of the investigation was to observe the effect of a triggered unit on its nearest neighbor, and to maximize this coupling. The emitter of the fired unit was therefore painted to provide an equipotential and a potential corresponding to the valley voltage was applied to it. The potential was measured in the region of the emitter of the nearest neighboring unit to determine the influence of the fired unit on its nearest neighbor. In this manner it was determined that for geometry A, regardless of the potential on the fired emitter, the potential at the emitter of the nearest neighbor was unchanged. It remained at approximately 6.5 v for an interbase voltage of 10 v. It was seen from this that the configuration of geometry A, with a channel width of 1 in., did not permit coupling from one unit to the next. Also the value of intrinsic standoff ratio was very close to that predicted by considering a completely closed base-two.

In geometry B the channel width, w , connecting the units was opened from one inch to two inches. For three conditions of the emitter of one unit, corresponding to the quiescent state and two possible

values of valley voltage, the potential at the emitter of the nearest neighbor was recorded. This was done for both the inner and outer emitter radii, e_1 and e_2 respectively, at the point nearest the open channel where the coupling was most pronounced. It was felt that not painting in the emitter of the element under investigation would most correctly simulate the condition of a unit before firing: a uniformly resistive substrate separated from the emitter contact by a reverse-biased junction.

The results of investigating geometry B are presented in Table 2.1. The recorded data indicated that some weak coupling was present. However, it was felt that the magnitude of the coupling was insufficient to cause the nearest neighbor to be reliably triggered. At the somewhat optimistic valley voltage of 1 v, the extent of the influence on the nearest neighbor was a reduction of potential in the emitter region of only 0.2 v. Furthermore, this occurred at the nearest point on the emitter. There was very little influence at any other point on the emitter. At this time it was decided to open the channel completely, i.e., to replace the base-two contact regions by two parallel bars.

The geometry of Fig. 2.5 was constructed. It was recognized that this configuration would lead to smaller values of intrinsic standoff ratio, but this disadvantage was accepted. With a value of 10 v interbase voltage, the highest value of potential observed on a line, through the centers of the base-one circles, parallel to the base-two bars was 6.00 v. Inner and outer emitter radii of 1.6 in. and 1.9 in. respectively yielded an intrinsic standoff ratio of approximately

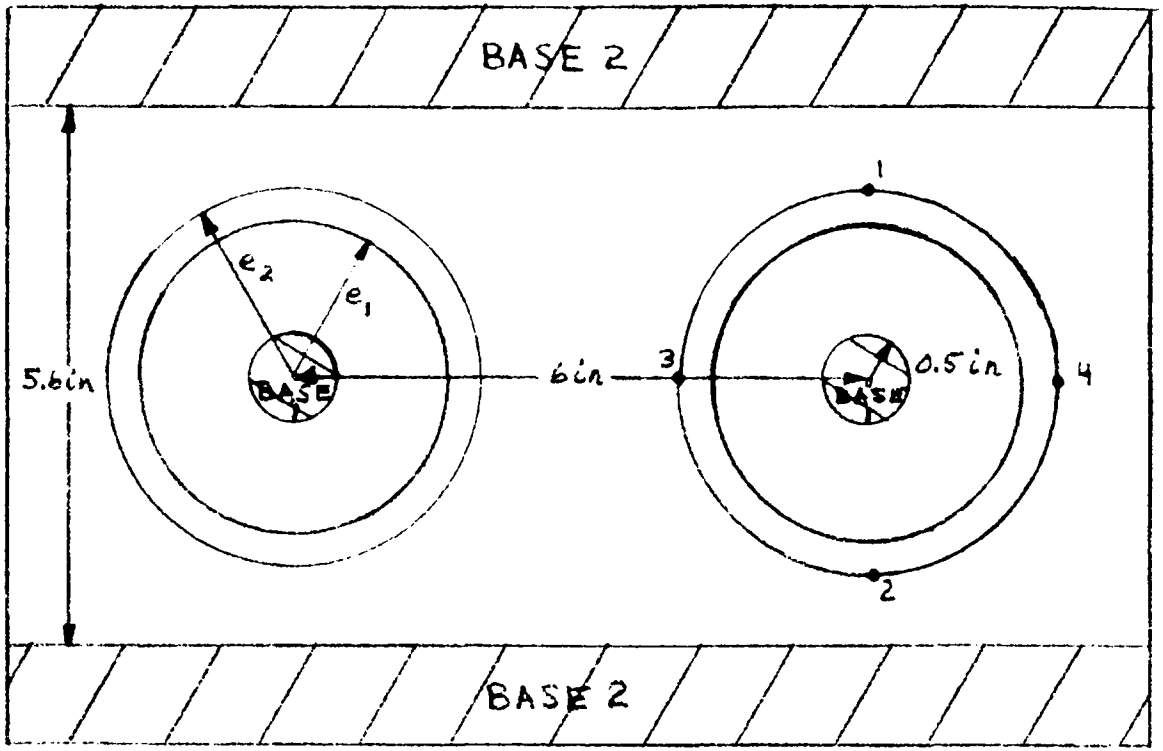


Fig. 2.5 Open Channel Neuristor Geometry

0.58. Referring to Fig. 2.5, the numbers one through four around the emitter ring determine the four measurement points which were used in evaluating this geometry. As before various values of potential were applied to the emitter of one unit to simulate its having fired and measurements were made at these four points on both the inner and outer emitter radii of the unit to the right.

Table 2.1

Nearest Neighbor Potential for Geometry #2

Triggered Emitter Condition	V_{e_1}	V_{e_2}
Open	5.00v	6.34v
3.30v	4.88v	6.22v
1.00v	4.79v	6.05v

Based on V_{BB} = 10v

The results of these measurements are given in Table 2.2, based on an interbase voltage of 10v. As can be seen from this table, there is a marked influence on the nearest point of the neighboring emitter, position 3. The magnitude of this coupling is illustrated in Fig. 2.6, which is a plot of the potential measured at point 3 of the emitter of the nearest neighbor vs. the potential on the fired emitter. Also of interest is the fact that none of the other measuring points showed any effect of the fired emitter.

Table 2.2

Nearest Neighbor Potentials for Open Channel Geometry

Condition on Fired Emitter	Position Number	V_{e_1} (v)	V_{e_2} (v)
Open Ckt.	1	6.1	7.2
	2	6.1	7.2
	3	4.8	5.3
	4	4.7	5.3
5v	1	6.1	7.2
	2	6.1	7.2
	3	4.6	5.1
	4	4.7	5.3
4v	1	6.1	7.2
	2	6.1	7.2
	3	4.4	4.8
	4	4.7	5.3
3v	1	6.1	7.2
	2	6.1	7.2
	3	4.2	4.6
	4	4.7	5.3
1v	1	6.1	7.2
	2	6.1	7.2
	3	3.8	4.1
	4	4.7	5.3

Based on V_{BB} = 10v

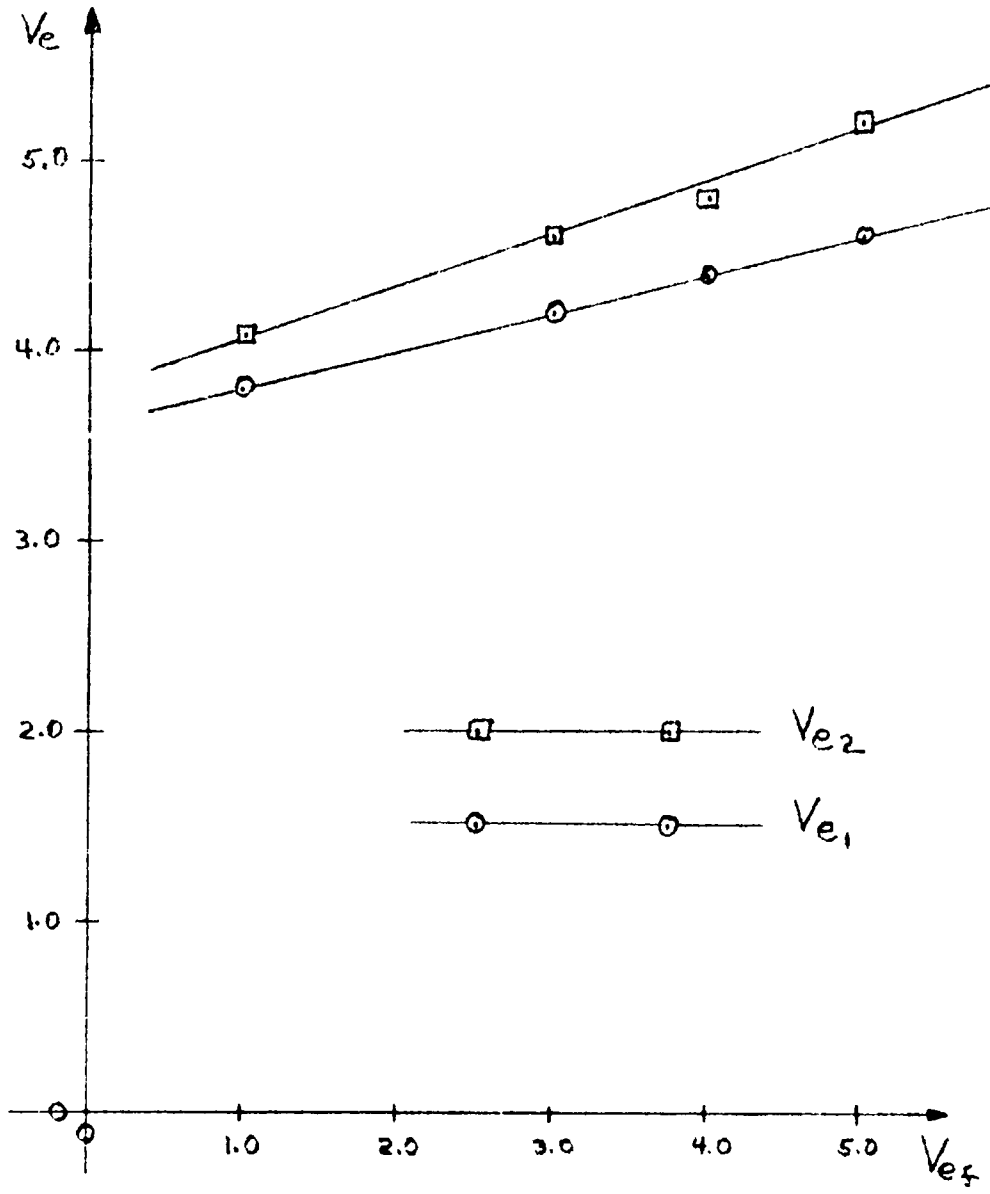


Fig. 2.6 Nearest Neighbor Emitter Potential vs. Fired Emitter Potential for Open Channel Geometry

It was felt that closer coupling would be needed for a successful neuristor line. Therefore, four new measurement points were introduced corresponding to position #3 for four new radii, 1.2 in., 2.2 in., 2.5 in., and 2.8 in. The potential at these points was measured for several values of potential on the emitter ring of the unit to the left. These measurements resulted in the data presented in Table 2.3. Not unexpectedly, as the distance between the fired emitter and the point of measurement was decreased, the influence of the fired emitter on the potential was increased.

This is illustrated in Fig. 2.7 where the measured potential vs. fired emitter potential is plotted for both the largest and smallest distance between measurement point and fired emitter. From Fig. 2.7 it is seen that the increased influence of the fired emitter potential on the measured potential is reflected in the slope of the lines, $\frac{\partial V}{\partial V_{e_f}}$. The slope vs. radius value is plotted in Fig. 2.8.

It was decided to choose a geometry which would yield a change in potential, due to the firing of another unit, of one half the peak voltage to valley voltage difference. From Fig. 2.8 it was seen that an emitter to emitter distance of 1.2 in. would be required. Rather than achieve this by merely expanding the emitter ring radius, the center to center distance of the units was decreased from six inches to five inches. Thus the emitter radii of 1.6 in. and 1.9 in. were retained. This geometry is shown in Fig. 2.9. The smaller center to center distance of the elements resulted in a reduced standoff ratio, but it was decided to sacrifice standoff ratio for the benefit of greater coupling.

Table 2.3

Potential Values at Six Different Radii
on Open Channel Geometry

Radius at Which Voltage Was Measured	Condition of Fired Emitter	V_1 (v)	V_2 (v)	V_3 (v)	V_4 (v)	V_5 (v)	V_6 (v)
V_1 (r = 1.2 in)	6v	3.7	4.8	5.4	5.8	6.1	6.2
V_2 (r = 1.6 in)	5v	3.6	4.6	5.1	5.5	5.7	5.8
V_3 (r = 1.9 in)	4v	3.5	4.4	4.8	5.2	5.3	5.3
V_4 (r = 2.2 in)	3v	3.4	4.2	4.6	4.8	4.8	4.8
V_5 (r = 2.5 in)	2v	3.3	4.0	4.4	4.5	4.5	4.4
V_6 (r = 2.8 in)	1v	3.1	3.8	4.1	4.2	4.1	3.9
	0v	3.0	3.6	3.8	3.9	3.7	3.4

Based on V_{BB} = 10v

At this time the geometry of Fig. 2.9 was considered the optimum in terms of standoff ratio and coupling.

This configuration was tested in the manner described above. The data was recorded in Table 2.4. From that data it was seen that the coupling was pronounced at the nearest point to the fired emitter, and yet at the farthest point, position #4, there was little effect. The conclusion was drawn that the next-nearest neighbor coupling did not exist for this geometry, at least in the resistance paper simulation.

It was then decided to construct a neuristor line in silicon, along the lines of the optimum geometry. This phase of the neuristor development is considered in the next chapter.

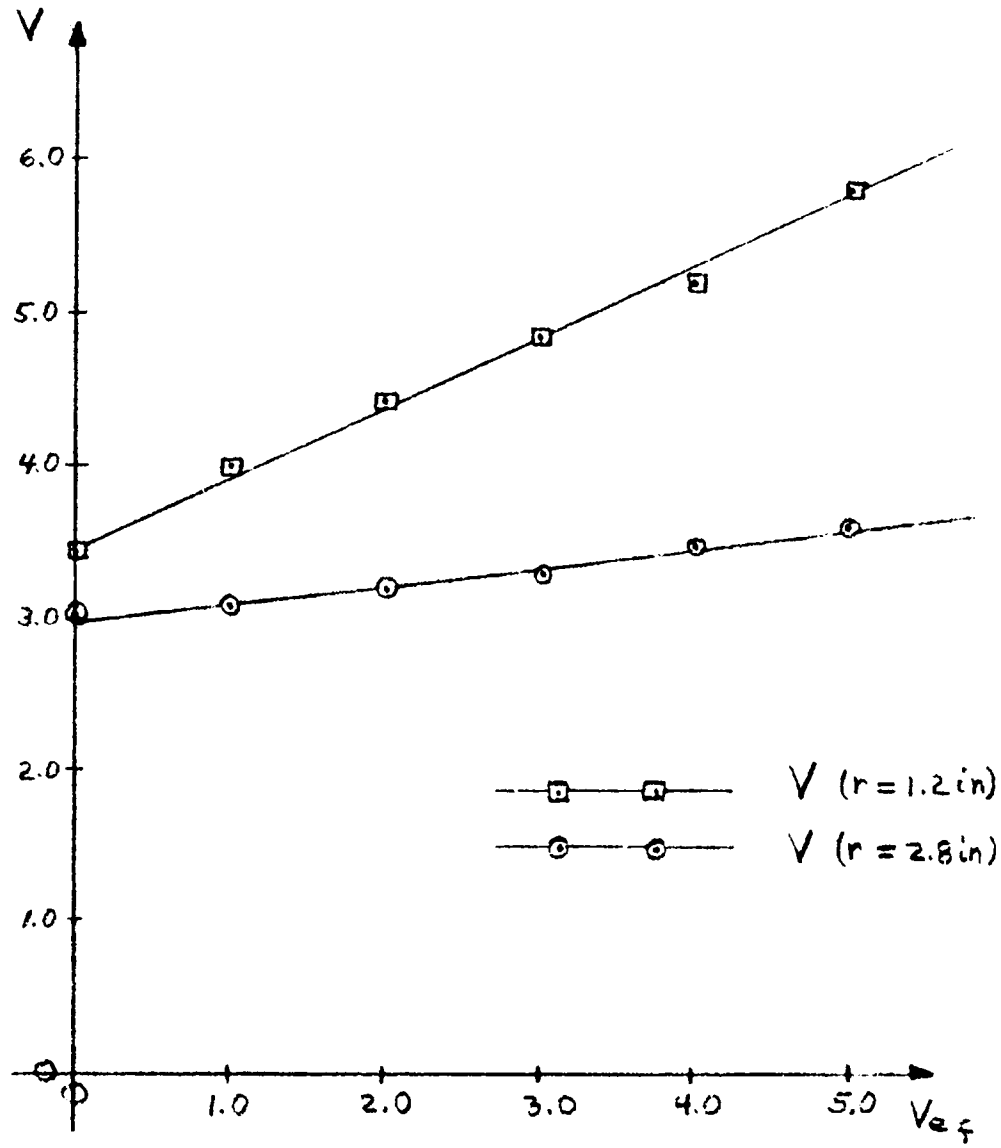


Fig. 2.7 Potential at Two Radii vs. Fired Emitter Potential for Open Channel Geometry

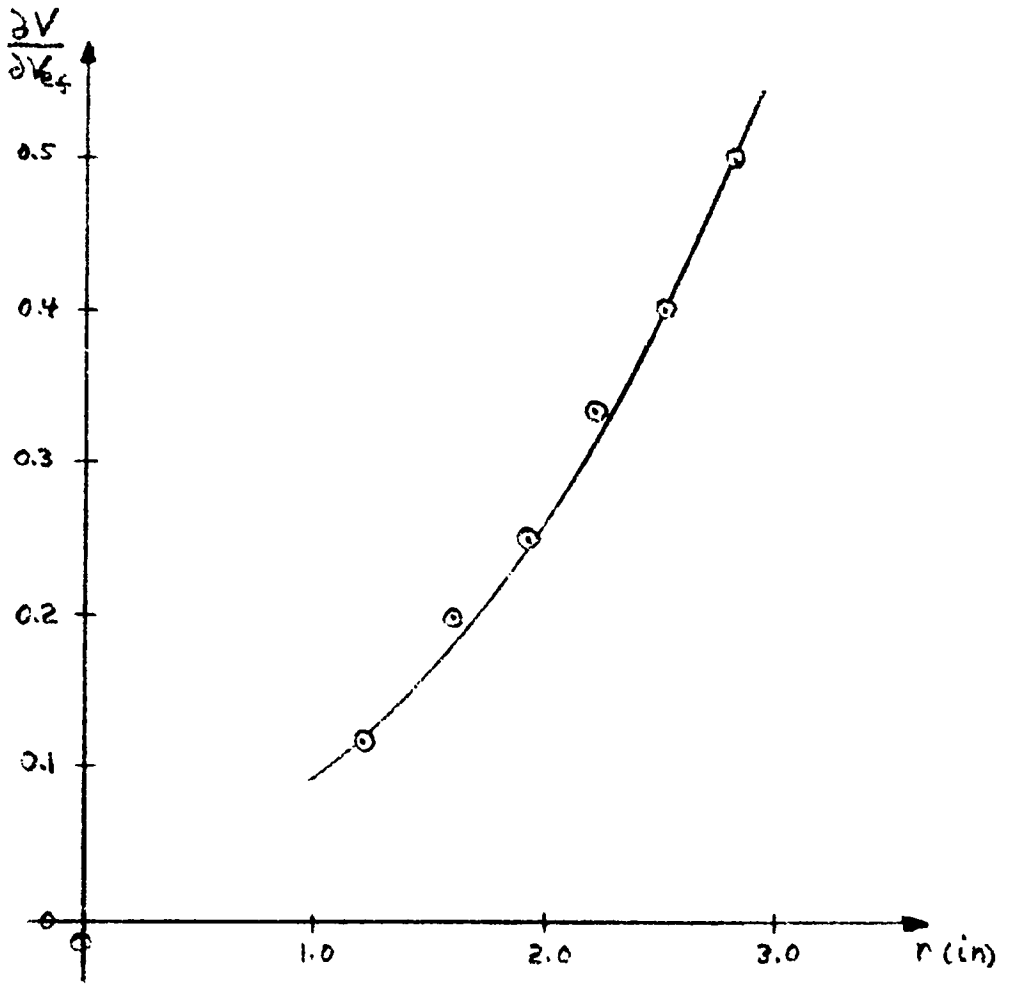


Fig. 2.8 $\frac{\partial V}{\partial V_{ef}}$ vs. Measuring Point Radius

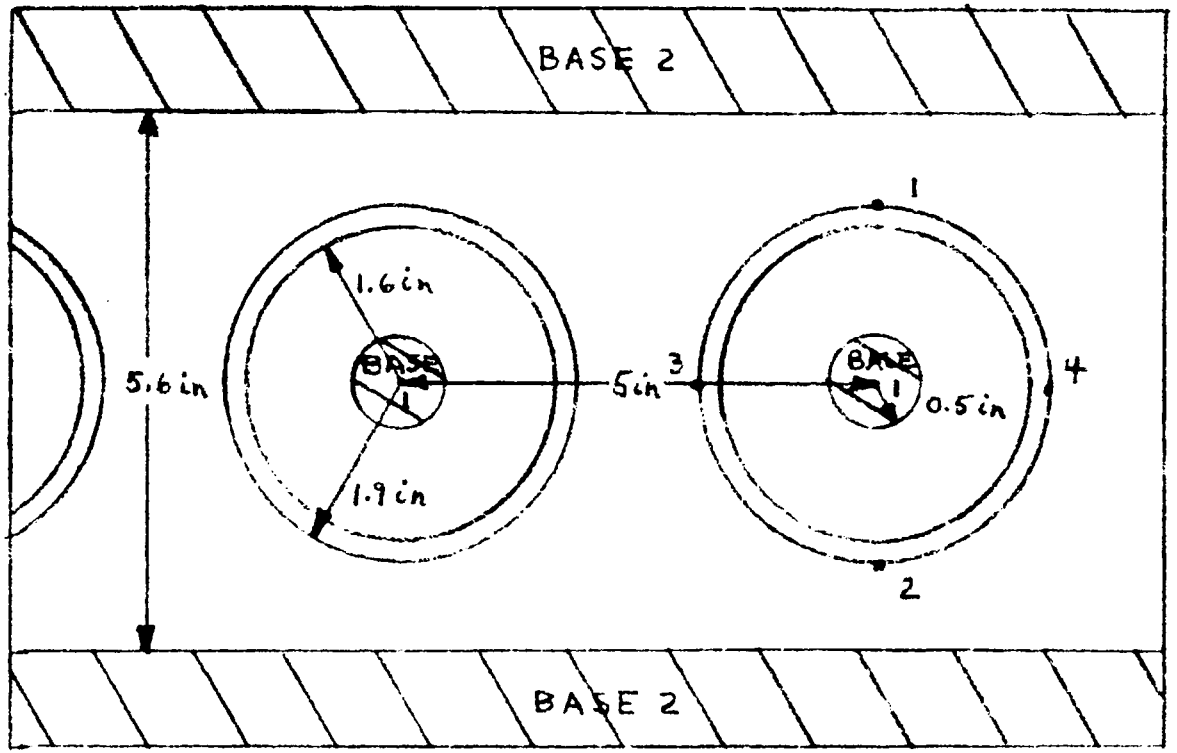


Fig. 2.9 Best Neuristor Simulation Geometry

Table 2.4

Potential Measurements of Optimum Geometry

Condition of Fired Emitter	Position Number	V_{e_1} (v)	V_{e_2} (v)
Open Ckt.	1	6.2	7.1
	2	6.1	7.1
	3	4.2	4.6
	4	4.3	4.7
5v	1	6.2	7.1
	2	6.1	7.1
	3	4.2	4.6
	4	4.3	4.7
3v	1	6.0	7.0
	2	6.0	7.0
	3	3.4	3.6
	4	4.3	4.7
2v	1	6.0	6.9
	2	6.0	7.0
	3	3.1	3.2
	4	4.3	4.7
1v	1	6.0	6.9
	2	6.0	6.9
	3	2.7	2.7
	4	4.3	4.7

Based on V_{BB} = 10v

Chapter 3

UNIJUNCTION LINE IMPLEMENTATION IN SILICON SUBSTRATE

The transfer of the neuristor line design from the resistance paper analog to single crystal silicon wafers was recognized as a venture into an unknown area for two reasons. The first was the general lack of faith in the resistance paper as a valid simulation of the resistivity properties of silicon. The paper was constructed specifically to have uniform and constant resistivity. It was evident that silicon, particularly near-intrinsic silicon, had anything but constant resistivity. The second was that the basis for the operation of this neuristor realization, the switching characteristics of the unijunction transistor, could not be simulated using resistance paper. For these reasons a separate study of unijunction transistors, particularly those of approximately the geometry thought useful for neuristor realization, was undertaken [Wise, 1968].

A representative geometry is shown in Fig. 3.1. A brief description of the fabrication follows; for more details, see Wise [1968]. To enhance the peak voltage, V_p , to valley voltage, V_v , difference, high resistivity (100-150 Ω-cm) homogeneous n type single crystal silicon wafers were chosen for substrate (base) material. The p type emitter was formed by solid state diffusion of boron, the source for this being diborane gas. The resulting junction depth and sheet resistance of the emitter were 2.3 microns and 175 ohms per square respectively.

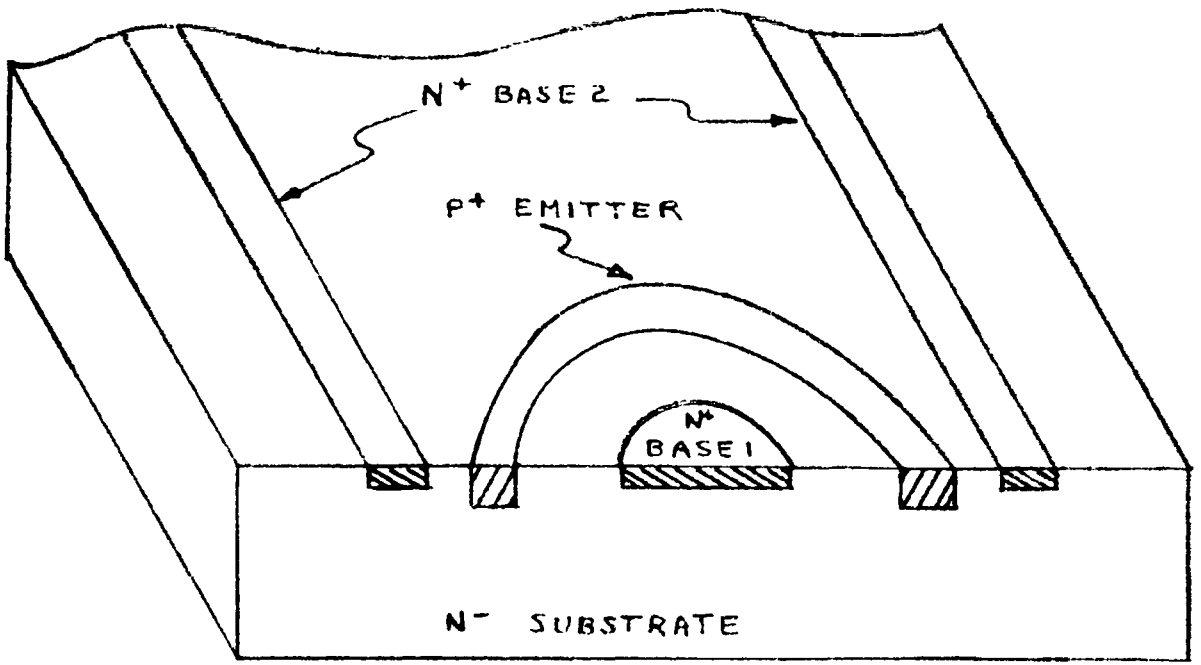


Fig. 3.1 Adapted Cylindrical Unijunction Transistor Geometry

Since the base region was of high resistivity, heavily doped n type regions, n^+, had to be formed in the areas of the base-one and base-two contacts to insure ohmic contacts. These n^+ regions were formed by solid state diffusion of phosphorous, the source for this being phosphine gas. The contact metallization was formed by evaporation of aluminum. In this manner several device geometries were fabricated by means of masking and photolithographic techniques standard in the monolithic integrated circuits industry.

The principle problem involved in the fabrication was caused by the high resistivity material employed for the substrate. The surface of a semiconductor can assume rather peculiar electrical properties if it is not extremely defect-free material and is not kept immaculately clean. When the material is moderately doped, the "background" carrier concentration can swamp out the anomalies caused by surface conditions. Unfortunately, the high resistivity material used had a very low "background" concentration, and so the results of surface conditions appeared unmitigated by the substrate doping. As a result, if surface conditions were not to dominate device performance, extreme care had to be exercised throughout the fabrication process. The care exercised was not completely successful in minimizing surface effects. The fact that the base current followed almost exclusively parallel to the surface enhanced the effect of surface conditions on device performance.

Another problem in fabrication was caused by the lack of electrical isolation between the header and the die containing the neuristor line by conventional die mounting techniques. The manner in which

the dice are mounted to the headers is as follows. The headers are heated to 390°C, and a gold-silicon alloy is melted in the region where the die is to be placed on the header. Then the silicon die is placed on this melt, and the header is allowed to cool. The molten gold silicon alloy forms a silicon-rich alloy at the wafer, and a gold-rich alloy at the gold plated header. This affords very good mechanical, thermal and electrical contact between die and header.

The excellent electrical contact is the problem situation. The die is typically six to eight mils thick, and the n type region which forms the base is connected to the header. As a result, an equipotential surface is created on the bottom of the die which is about the same distance from any emitter as a neighboring emitter.

This auxiliary potential source acts to reduce the effect of the change in potential of the fired emitter on its nearest neighbors in the following manner. When the line is in the quiescent state, the potential at any point is determined by the interaction of the base-one, base-two, and bottom equipotentials. When one emitter fires, and the potential in its region is reduced, it acts in conjunction with the other sources of potential to redetermine the potential in the region of the neighboring emitter. If there is an equipotential approximately as near as the fired emitter to an unfired emitter, and this potential doesn't change when one emitter is fired, the effect of the fired emitter is reduced, and coupling is inhibited.

To overcome this problem, some means of mounting the die with an insulating substance had to be devised. In the absence of more

refined bonding materials, "Starset" fire-brick cement was employed with some success.

It was decided that, for the initial fabrication runs, the amount of circuitry on each die be limited to the line of unijunction transistors. Also, to facilitate complete testing, the base-one contact for each individual unijunction transistor was to be bonded to a pin so that separate units could be connected to and disconnected from the line easily. In this manner units could be tested individually, in pairs, etc. This imposed a restriction on the geometries that could be employed, since contact size had to be large enough so that the "nail head" ball bonder could be used. The minimum size bonding pad to which contact could be made was 2 to 3 mils. Other processing problems precluded the use of large pads on the oxide connected to small areas in the material so the minimum base-one radius was determined to be 3 mils.

The separate connection to the base-one contact for each unit imposed a restriction on the number of units which could be mounted in one package. The only available package, at that time, was the 10 pin version of the standard TO-5 header. Because there was a maximum of 10 connections to the package and each unit required two, one for the emitter contact and one for the base-one contact, the maximum line size was fixed at four units.

The fabrication problems were met with varying degrees of success and several successful neuristor lines were produced. Five of the most successful geometries are shown in Fig. 3.2 through Fig. 3.6. The geometry of Fig. 3.2 is an adaptation of the geometries found to be most successful in the resistance paper analog.

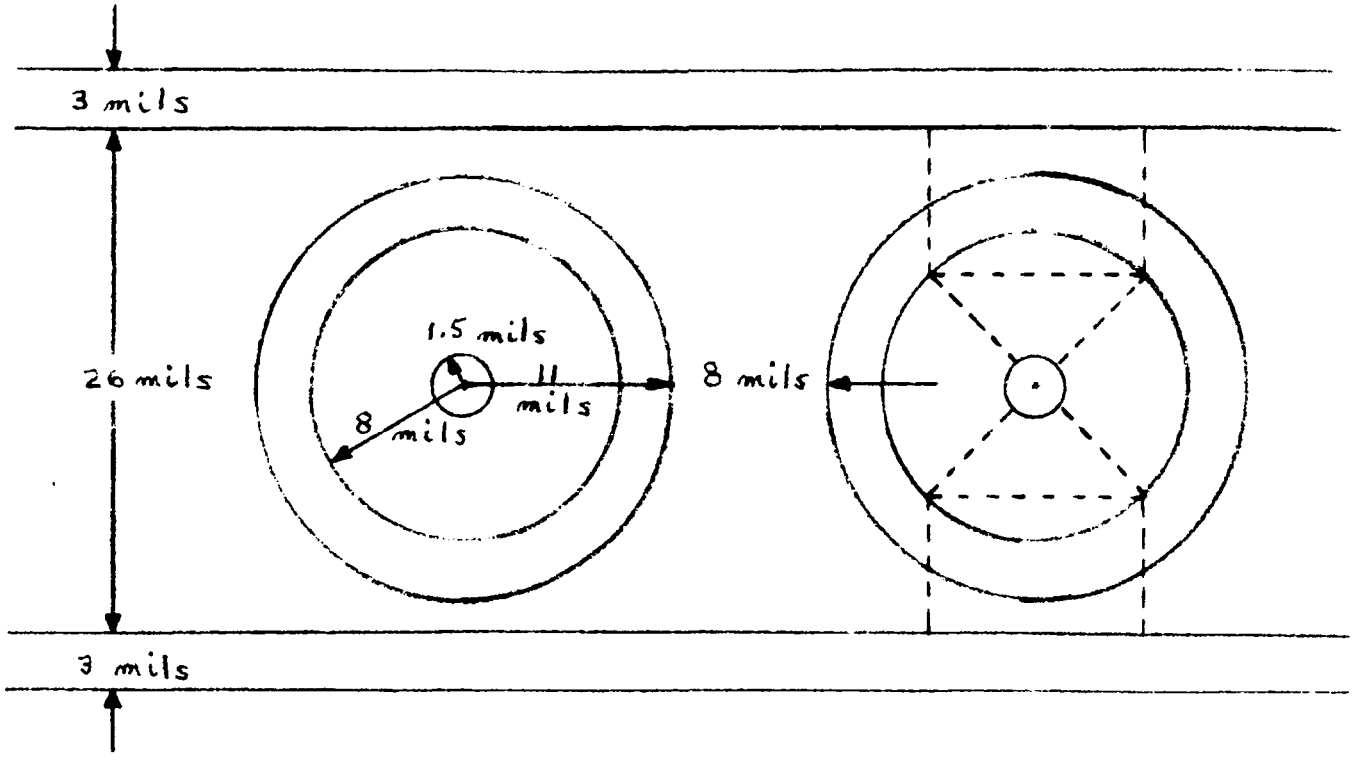


Fig. 3.2 Neuristor Geometry No. 1

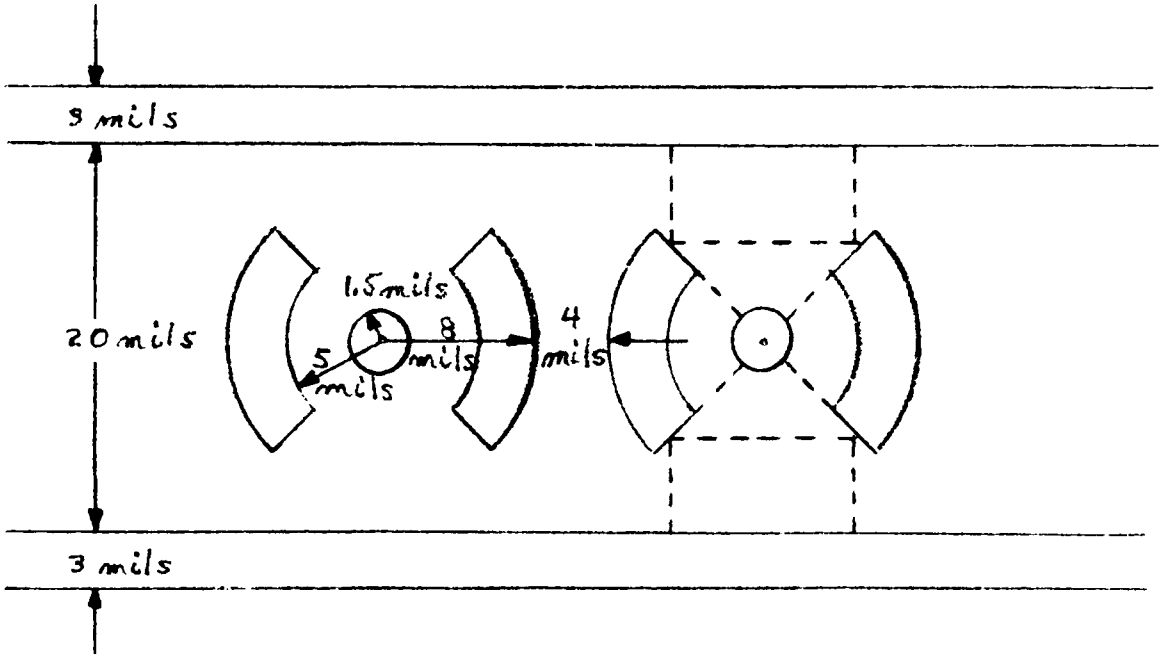


Fig. 3.3 Neuristor Geometry No. 2

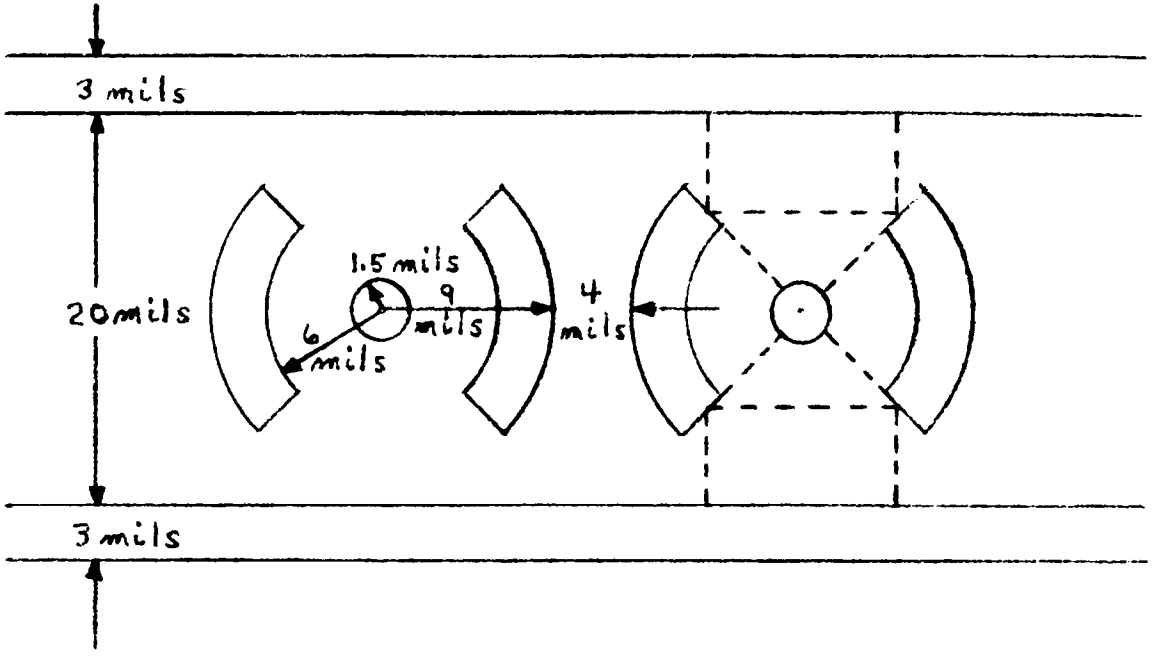


Fig. 3.4 Neuristor Geometry No. 3

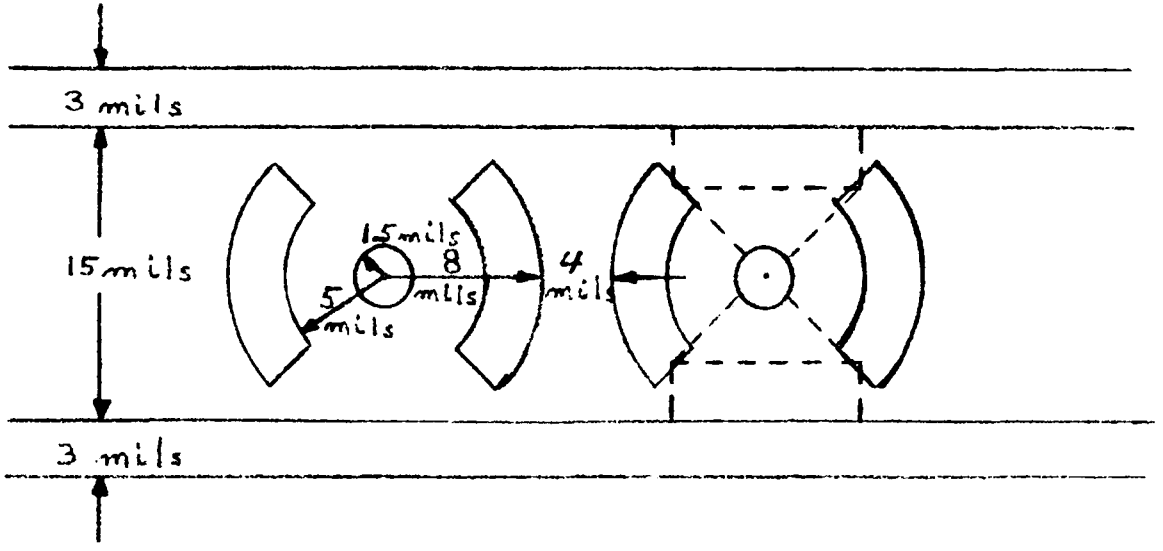


Fig. 3.5 Neuristor Geometry No. 4

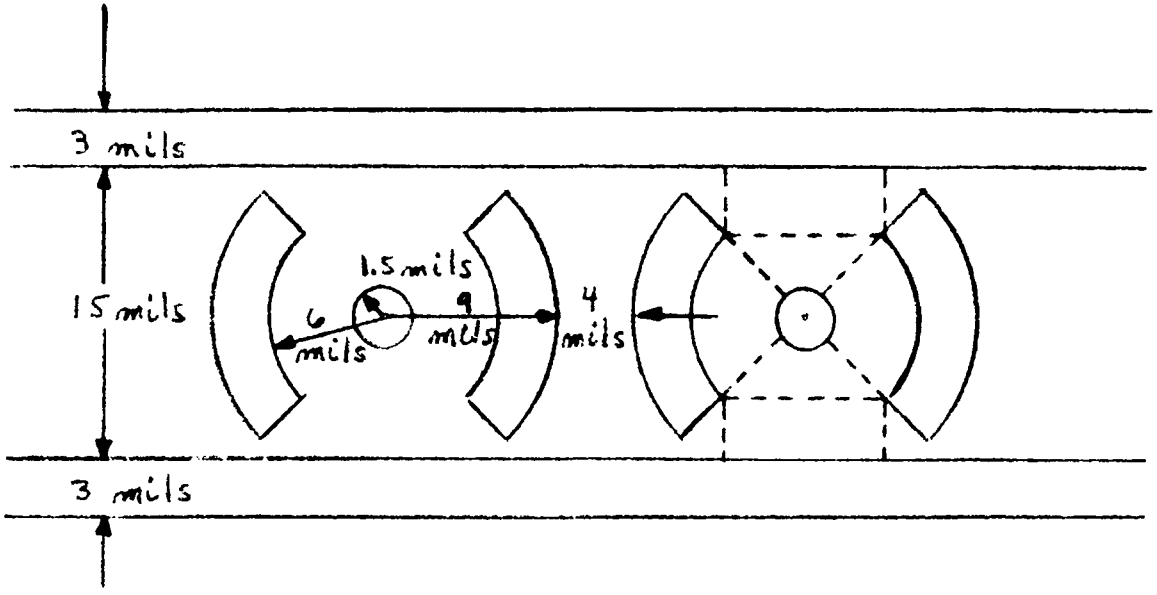


Fig. 3.6 Neuristor Geometry No. 5

The geometries of Fig. 3.3 through 3.6 differed from that of Fig. 3.2 in that the emitter ring was "split". It was determined that the split ring emitter geometry was desirable since it made possible two things. First, it was realized that the two construction restrictions of circular emitters and parallel line base-two contacts made the achievement of high intrinsic standoff ratio impossible. The potential measurements of Chapter 2 showed that the minimum potential the emitter experiences is in that region of the emitter in the center of the channel. To increase this minimum value, the emitter ring radius must be increased. However, soon the emitter ring approaches the base-two contacts. This sets a maximum emitter ring radius so long as the ring is kept closed.

By splitting the emitter ring, relatively large values of emitter radii were possible without the problem of overlapping the base-two contacts. This increased emitter radius made possible higher intrinsic standoff ratios. Also, since the neighboring units also had larger emitter radii, the emitters were closer, and hence the coupling between the elements in a line was also enhanced.

It was felt, that due to the large variation of potential under the emitter ring, only that portion of the ring near the center of the channel would become forward biased when the intrinsic standoff ratio was exceeded. As a result not much, if any, active emitter area would be lost by employing the "split-ring" geometry. More importantly, however, it was feared that only one side of the split emitter would be forward biased, and the other would remain reverse biased. In this way transmission would come to an unfortunate end.

To check on this several geometries were fabricated, each successive one getting more to the extreme split-ring geometry. These are the geometries #2 through #5. It can be seen (Fig. 3.2 through Fig. 3.6) that geometry #2 is similar to geometry #1 with the emitter ring split and all dimensions slightly reduced. Geometry #3 is a slightly more extreme splitting than geometry #2, etc. It was found that by limiting the emitter diffusion to the areas indicated in the "split-ring" geometries, and then connecting the two halves of the emitter in the metallization process, no loss of performance would result. Evidently, as one side of the emitter became forward biased due to the effect of one of its nearest-neighbors being fired, the conductivity modulation was sufficient to influence the region between the base-one contact and the other half of the emitter.

In this manner, the other half is also fired. As a result, transmission proceeds as before aided by the increased intrinsic standoff ratio and closer emitter coupling. A more detailed consideration of the results obtained for these geometries appears below.

The five geometries were first tested so that the characteristics of the five different unijunction transistor geometries would be evident. Particular attention was paid to the "split-ring" geometries to determine the effects of the discontinuous emitter ring. The characteristics of interest in the preliminary study were peak voltage, V_p, and valley voltage, V_v, for a typical value of interbase voltage, V_{BB} and hence intrinsic standoff ratio, η . These were important because the peak to valley voltage difference was the source of the potential difference which triggered the nearest neighbor.

Another critical parameter was the value of the interbase resistance, R_{BB}. Because long neuristor lines would consist of many of these unijunction transistors connected in "parallel", the power dissipated by the line would be excessive unless the interbase resistance was kept high. Also with a high value for η, relatively small values of interbase voltage would yield high values of peak voltage. To summarize, for both efficient operation and low power dissipation a high value of η was desirable. Also for both enhanced conductivity modulation and low power dissipation high resistivity substrate "bases" were desirable.

The first characteristic is dependent on geometry while the second is dependent on material. Typical values of peak and valley voltage, interbase resistance and standoff ratio measured on the five geometries are presented in Table 3.1. The highest value of intrinsic standoff ratio and interbase resistance was observed on geometry 1. Also, this geometry lends itself most easily to the calculation of the effective depth of the base.

Table 3.1

Typical Parameter Values for Five Neuristor Geometries

Geometry	V_p (v)	V_v (v)	R_{BB} kΩ	η	$\Delta V_E = V_p - V_v$
1	6.2	2.0	6.0	.62	4.2
2	3.3	1.2	4.0	.33	2.1
3	4.5	1.3	3.4	.45	3.2
4	3.6	1.2	3.6	.36	2.4
5	4.8	1.3	3.0	.48	3.5

Based on V_{BB} = 10v

As a zero order approximation, consider the interbase resistance as composed of two parts. The first is between the base-one radius and the inner emitter radius. As a more accurate approximation only about 2/3 of this circle is effective. The second part is the resistance of the region between the base-two contacts and the inner emitter radius. The current is assumed to flow only parallel to the surface. These regions are indicated on Fig. 3.2 by the dashed lines. The resistance between two cylinders of depth D is given from (2.3) as

$$R_1 = \frac{1}{D} \frac{\rho}{2\pi} \ell n \left(\frac{r_2}{r_1}\right) \tag{3.1}$$

For ρ = 100 Ω-cm, r_2 = 8 mil, r_1 = 1.5 mil:

$$R_1 \approx \frac{1}{D} 7.2 \text{ k}\Omega \tag{3.2}$$

where D is given in mils.

The second part of the resistance is approximated by rectangular regions of length, ℓ, width, w , and depth, D, located between the base-two contacts and the cylindrical segments mentioned above.

$$R_2 = \frac{\rho \ell}{w D} \tag{3.3}$$

For ρ = 100 Ω-cm, ℓ = 8 mils, w = 12 mils:

$$R_2 \approx \frac{26\text{k}\Omega}{D} \tag{3.4}$$

The total resistance given in Table 3.1 is:

$$R_T = \frac{3}{2} R_1 + \frac{1}{2} R_2 \tag{3.5}$$

$$6k\Omega = \frac{23.8k\Omega}{D} \tag{3.6}$$

$$D \approx 4 \text{ mils} \tag{3.7}$$

This value for the "thickness" of the base region was only a gross approximation. However, it was useful as an order of magnitude indication of the thickness. One conclusion from this was that, if an n-type epitaxial layer on a p-type substrate had been used for the base region, higher values of interbase resistance would have resulted, (provided, of course, that the layer was less than 4 mils thick). This conclusion follows because the cross-sectional area through which the base current flowed would have been reduced. An order of magnitude increase in interbase resistance could be expected if a 10μ "epi" layer was employed for the base material.

An attempt was then made to predict the interbase resistance of the split ring geometries. The results agreed within 20% with the measured values if the outer radius of the cylindrical resistor was chosen to be between 60% and 70% of half the channel width, and the length and width of the rectangular segments were chosen so that the width was one half of the center to center spacing and the length yielded an overlap between 1 and 3 mils. These regions are illustrated by dotted lines in Fig. 3.3 through 3.6.

As was expected, this analysis showed that less than one half of the total interbase resistance was contained in the circular regions. This agreed with the values of intrinsic standoff ratio measured. The

agreement served to support the assumption that effectively, only two thirds of the circular regions carried appreciable current.

Considering geometries 3.2 through 3.5, two trends are worth noting. When the channel width was reduced from 20 mil to 15 mil but all other dimensions were held constant, the interbase resistance decreased by 400 ohms in both cases. When the center to center distance was increased by two mils, but all other dimensions were held constant the interbase resistance decreased by 600 ohms in both cases. There were too few data points to make concrete statements but the trends were obvious.

The approximate nature of this analysis is seen in that it assumes no current flow where the emitter potential is lowest, i.e., where injection begins. However, it is worth noting that the analysis indicates that in the quiescent state relatively little current flows in the region in which injection first occurs.

Table 3.1 indicates that the valley voltages of all the "split-ring" geometries are approximately 0.8v below that of geometry 1. This can be attributed to the 8 mil inner emitter radius of the first geometry geometry vs. the 5 to 6 mil inner emitter radii of the split-rings emitters. As can be seen from Fig. 3.3 through 3.6, the basic difference between geometries 2 and 4, and 3 and 5 is the channel width. As the width was reduced the value of intrinsic standoff ratio increased. The basic difference between geometries 2 and 3, and 4 and 5 is the emitter radius. Here, the intrinsic standoff ratio was increased by increasing the radius of the emitter ring.

The forward resistance of the emitter base-one (base-two open) and emitter to base-two (base-one open) diodes is given in Table 3.2. From the data, it can be seen that a drastic reduction in the resistance of the material takes place when the junction is forward biased. The emitter-base-one resistance of geometry 1 is seen to be considerably larger than that of any of the "split-ring" geometries which explains the high value of valley voltage for this geometry.

Table 3.2

Forward Diode Resistance

Geometry	R_{E-B_1} (B_2 Open)	R_{E-B_2} (B_1 Open)
1	45Ω	16Ω
2	16Ω	16Ω
3	16Ω	16Ω
4	16Ω	18Ω
5	16Ω	18Ω

The lines were then tested to determine the extent of the coupling between successive units. All the base-one contacts were connected together, then 10v was applied between the common base-two and common base-one connections. A voltage was applied to the emitter of the first unit in the line and increased until the peak-voltage was exceeded. Because of a current limiter in the input circuit, the emitter voltage settled at the valley voltage. Then the other units in the line were tested to determine their new peak voltages. After this had been accomplished, the procedure was repeated for the remaining three units.

In this manner measurements of the extent of peak voltage lowering (self-triggering) were recorded for each of the five geometries.

The results of these tests are shown in Table 3.3. The values recorded there are typical values, for each geometry, but all the observed values were within $\pm$ 0.1 v of those in the table. In each case the peak voltage of the next-nearest neighbor is unchanged by a unit's having fired. This agrees with the data obtained from the resistance paper analog. The column on the far right, $\Delta V_p/\Delta V_E$, lists the change in peak voltage caused by the firing of the nearest neighbor, per volt change in the fired unit's emitter potential. This is a measure of the coupling efficiency, ζ . Evidently, geometry 1 has a very poor coupling efficiency, which is understandable since the spacing between adjacent emitters is 8 mils. The other geometries all have 4 mil spacing between emitters, and this is reflected in their high coupling efficiency. The efficiencies of geometries 2 and 3 is higher than those of 4 and 5 because the channel is wider, and so the effect of one emitter on the other is not reduced as much by the base-two potential since it is farther away. Similarly, the efficiencies of geometries 3 and 5 is greater than those of 2 and 4 because the emitter rings in geometries 3 and 5 are farther away from the base-one potential.

One advantage of fabricating all the elements of a line at the same time is the close match in parameters which results. The tests on the various geometries confirmed this in that the parameter values of the units in a line were all within $\pm$ 5% of each other. Most were considerably better than this. This matching is critical when the line

Table 3.3

Extent of Coupling

Geometry	V_p (nearest)	V_p (next nearest)	$\zeta = \Delta V_p/\Delta V_E$ (nearest)
1	4.8	6.2	.33
2	1.6	3.3	.81
3	1.5	4.5	.94
4	1.9	3.6	.71
5	1.7	4.8	.89

Based on V_{BB} = 10v

is employed in junction connections and when bilateral properties are important.

At this point a list may be made of the two geometrical variables and their consequences.

1. Decrease channel width:
   a) lower R_{BB}
   b) higher η
   c) lower coupling efficiency, ζ .
2. Increase center to center distance, while holding emitter to emitter spacing constant:
   a) higher η
   b) higher coupling efficiency, ζ .

For size considerations, the channel width should be decreased; however, there are two disadvantages in this. These are listed above. To some extent the decreased coupling efficiency can be compensated for by increasing the center to center distance and holding the emitter to

emitter distance constant. The two geometries with the most desirable parameter values (high η, high R_{BB}, high ζ) are geometries 3 and 5. Of these geometry 3 has a slight advantage since its interbase resistance is higher, even though its η is smaller. The 10% difference in η and ζ is negligible but, because of the power dissipation problem mentioned above, any improvement in R_{BB} makes a large difference.

Additional circuitry was then connected to each line and those characteristics ascribable to complete lines rather than to unijunction transistors or combinations of unijunction transistors were observed. The discussion of these observations is presented in Chapter 4.

Chapter 4

NEURISTOR LINE OPERATION

The previous chapter described the fabrication of five different neuristor lines, and the characteristics of each ascribable to unijunction transistor performance. The lines were then connected to external elements to determine their propagation characteristics.

Each line (composed of four unijunction transistors) was connected such that all the base-one contact pins of the 10 pin header were connected to ground, 0v. A base bias, V_{BB} , of +10v was applied to the common base-two contact pin. A capacitor, C , was connected between the emitter contact pin of each unit and ground. A resistor, R, was connected between the emitter contact pin of each unit and an emitter bias, V_E. This configuration is shown in Fig. 4.1. The emitter bias was selected such that its value was 0.5v below the unlowered (self-triggered) peak voltage of the elements. This value was selected as a good compromise in satisfying the conflicting requirements of noise immunity and ease of triggering. A lower value would have made triggering unnecessarily difficult, while a higher value would have made false triggering a distinct possibility.

It is now evident why the consistent values of peak voltage within a line mentioned in Chapter 3 are so important. If the above method of emitter biasing (a common voltage value) is utilized, any deviation from the standard peak voltage value leads to reduced noise

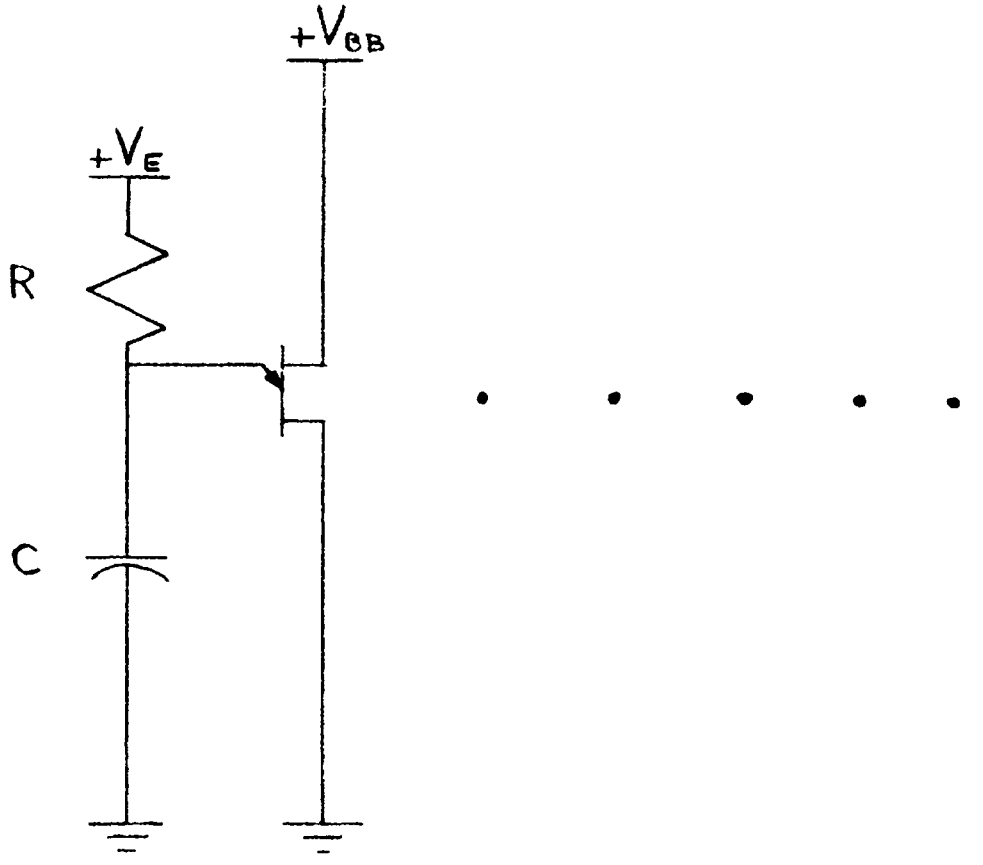


Fig. 4.1 Neuristor Line Circuit Connections

immunity or increased triggering requirements. For the above value of emitter bias, a variation of 0.5v, (approximately 10%) would be disastrous since some elements would be in the fired condition when the line is in the quiescent state. When the pulse reaches the fired element, it would disappear. This is the basis for pulse annihilation through head-on collision. Fortunately, the fabrication technique precludes such problems to a large extent.

After the line had been connected to the external elements and bias supplies, the first element in the line was triggered by the introduction of a 10 μsec wide positive going pulse with a 1.5 msec repetition period. For values of R = 24k and C = 0.047 μf, the shape of the propagating pulse for geometry 5 was as shown in Fig. 4.2. The upper trace shows the emitter voltage of element two and the lower trace shows the emitter voltage of element four. The wave shape was unchanged, indicating that one of the properties of the neuristor, attenuationless propagation, is present in the lines under study. It is also interesting to note that the shape of the propagating wave is dominated over most of the period by the externally connected capacitor and resistor. This is defined in Chapter 1. Tests on the other geometries yielded the same waveforms, with the exception of the peak and valley voltage values which varied from geometry to geometry.

The time scale was then expanded to better illustrate the shape of the transition from V_p to V_v. The upper trace of Fig. 4.3 shows the emitter voltage of element two of geometry five and the lower trace shows the emitter voltage of element four of geometry five. The fall

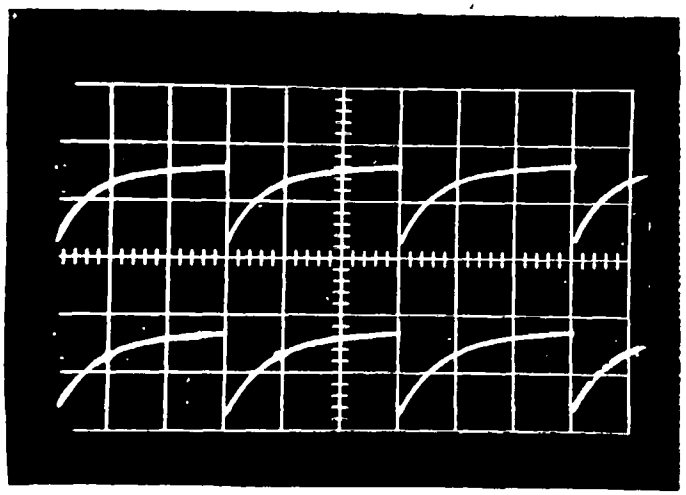


Fig. 4.2 Pulse Propagation on Neuristor Line
(Vert: 2v/cm; Hor: 0.5 msec/cm)

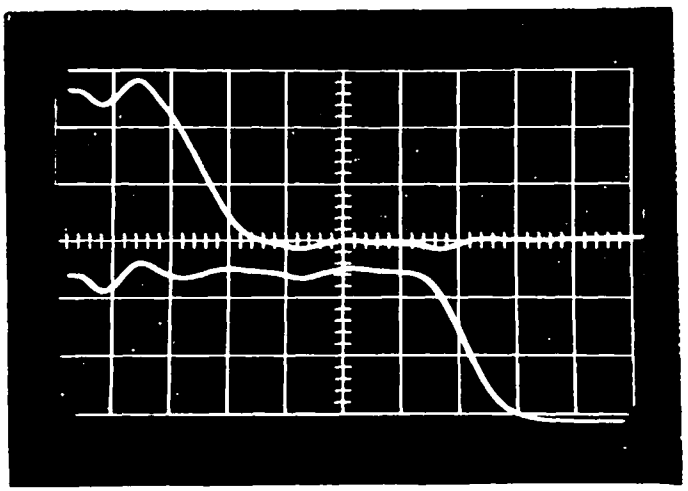


Fig. 4.3 Pulse Fall Time on Neuristor Line
(Vert: 1 v/cm; Hor: 2 μsec/cm)

time of each element is 2 μsec. This is in agreement with the empirically arrived at Eq. 13-21 for fall time given on page 502 of Millman and Taub [1965].

$$T = (2 + 5C)\ V_E \tag{4.1}$$

where T is the fall time in μsec. C is the emitter capacitance in μf, and V_E is approximately the valley voltage. For the element values used, $2 \gg 5C$, hence the fall time is independent of external circuitry.

The velocity of pulse propagation may also be measured from Fig. 4.3. The time lapse between the midpoint of the voltage drop of element two and of element four is approximately 9 μsec. Since this represents the time taken by the pulse to pass through two elements, the propagation time is about 4.5 μsec/unit. Since the elements are on 22 mil centers, this represents a propagation velocity of:

$$v_p \approx 5000 \text{ in/sec} \tag{4.2}$$

or

$$v_p \approx 125 \text{ meters/sec} \tag{4.3}$$

Similar tests on the other geometries yielded propagation times between 3 and 5 μsec per unit. The indication was that the propagation velocity was independent of the external elements, and the spacing between the emitter. When one unit's triggering was sufficient to trigger the nearest-neighbor, it did so 3 to 5 μsec. later. However, a very slight dependence of propagation velocity on emitter bias voltage was observed. This dependence was really very small, varying the emitter bias voltage increased and decreased the propagation velocity

by no more than 1 μsec. It appears that the only way to drastically reduce the propagation time per unit is to reduce the size of the units.

Figure 4.3 also illustrates the degree of noise immunity necessary for the successful operation of the line. The vertical scale is 1v per cm., and the lower trace illustrates the magnitude of the spurious signals which are present in the emitter potential previous to its being fired. These signals are almost exclusively due to the firing of other elements "up-stream". The upper trace also shows evidence of the firing of other units. It is interesting to note the indication of units three and four firing in the trace of unit two (upper trace). Both traces show evidence of the positive pulse firing unit one. This characteristic wave shape is present in the emitter potentials of all units which are the nearest-neighbors of the one fired by a positive pulse.

The bilateral transmission characteristics of the line are illustrated in Fig. 4.4. In this case, the positive pulse was applied to the emitter of unit three of geometry number five, and the upper and lower traces show the transitions of the emitter potentials of elements four and two respectively. The similarity of the two traces again indicates the uniformity of parameters achieved by the fabrication process.

As a test on the refractory period characteristic of the line, the 0.047 μf capacitor connected to the emitter of unit four of geometry five was replaced by one of slightly higher value, 0.054 μf. This had the effect of slightly increasing the recovery time through increasing the R-C time constant of the equivalent circuit proper to the recovery part of the cycle. The repetition rate of the positive pulse was decreased to 1.7 msec to facilitate the test.

The result, shown in Fig. 4.5, was the inability of every pulse arriving at the emitter of unit four to cause unit four to trigger. This was a consequence of unit four's not being recovered, i.e., still in its refractory period, due to the transmission of a previous pulse. In this case, by the time every second pulse arrived, the unit had completely recovered. The effect is that of frequency division. Division by numbers other than two was also possible. By adding an element whose capacitance value is the same as that of the elements before the long refractory period element, the original pulse shape is restored. In this manner multiple stage frequency division is possible with no distortion of the pulse waveform.

As defined in Chapter 1, the S type junction is constructed from individual lines by connecting a portion of each line to a common energy storage element. The emitter capacitors are the energy storage elements in the neuristor realization described here. When two lines were connected such that one unit of each shared a common emitter capacitor, S type junction operation was observed. Pulse propagation on either precluded the possibility of pulse propagation on the other until after a time, equivalent to the refractory time, had passed.

It was considered desirable to make the operation of the lines as fast as possible. This implied reducing the recovery time of the individual unijunction transistor circuits of which the lines were composed. The obvious procedure was to reduce the values of both R and C to a minimum. The minimum value of R was found to be 1.5 kΩ. If the emitter resistor was reduced below this value, the unijunction transistor

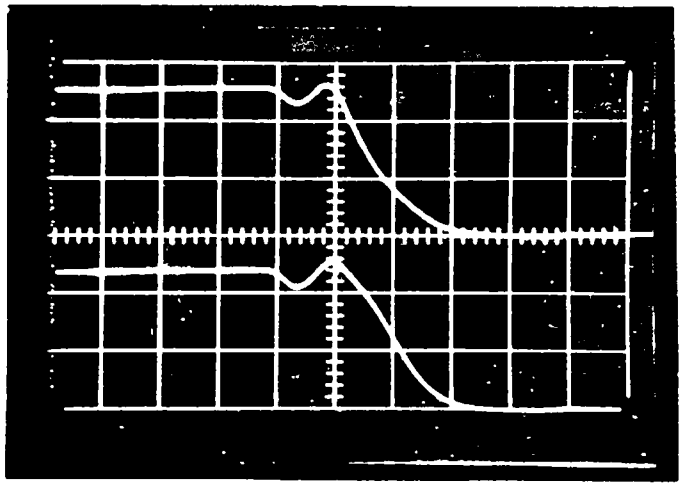


Fig. 4.4 Bilateral Properties
(Vert = 1 v/cm; Hor = 2 μsec/cm)

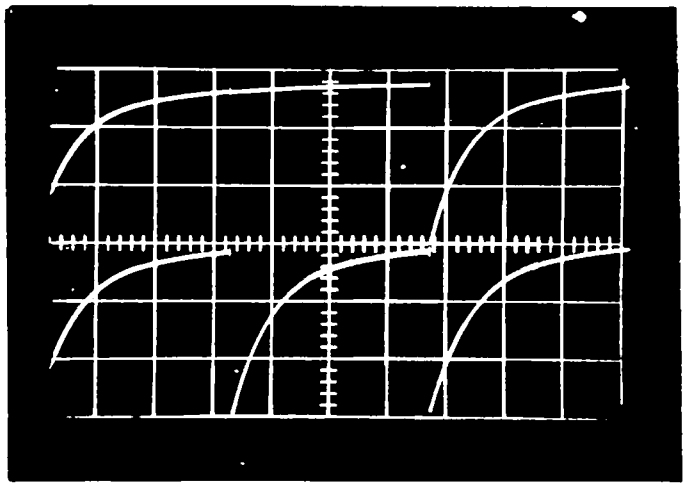


Fig. 4.5 Loss of Pulse Propagation During Refractory Period
(Vert = 1 v/cm; Hor = 0.5 msec/cm)

circuit operated as a bistable multivibrator. This mode of operation can be seen from Fig. 1.6. As the resistance value is decreased, the slope of the load line becomes less steep and it intersects the unijunction transistor characteristic curve a second time, on the positive resistance portion beyond the valley voltage.

The value of the emitter capacitance was then reduced. A minimum value was found to be approximately 0.007 μf for geometry five. The smallest workable capacitor for geometry one was about twice as large. A smaller capacitance resulted in the loss of propagation in the following manner. The first unit, which was triggered by the positive pulse, was observed to fire. The emitter potential of the second unit was also observed to undergo the transition from bias value to valley voltage and then recover. However, no change in the emitter potential of the third unit was apparent. This was observed both for the split emitter and continuous emitter structures.

An explanation of this observation is as follows. Both sides of the emitter of the first unit were triggered by the positive pulse. The energy of the pulse was sufficient to cause the nearest side of the second unit to fire. But there was not enough charge stored in the capacitor to effectively modulate the conductivity of a sufficient region of the base in the neighborhood of the base one contact to cause the other side of the second unit to fire. The result was that unit three was unfired. In effect the p-n junction on the far side of unit two remained reverse biased. The fall in potential was caused by only one side being fired. That these same effects were observed on geometry one was

an indication that those portions of the emitter ring near the base two contacts remain inactive and so serve no useful purpose.

With the minimum values of R and C, the recovery time was reduced to approximately 25 μsec. The total refractory period in this case being approximately 30 μsec. The fastest repetition period observed was 90 μsec, but this limit was imposed by the positive pulse generator.

In summary, all the properties of neuristor lines as well as S junction operation were observed in one form or another in the lines under test.

Chapter 5

CONCLUSIONS

The primary conclusion drawn is that neuristors can be successfully realized using the modified cylindrical geometry unijunction transistors. The absence of next-nearest neighbor triggering can be attributed to the relatively large spacing between an emitter and its next-nearest neighbor which is a consequence of the cylindrical geometry. Also, the location of the base-one potential between an emitter and its next-nearest neighbor aids in isolating one emitter from all but its nearest neighbors.

The success in using the split emitter ring configuration makes possible relatively higher intrinsic standoff ratios and closes emitter to emitter spacing. One can conclude from its operation that only that part of the emitter near the center of the channel becomes an injecting region when the unit is triggered.

The study also indicates that the parts of the interbase region which carry most of the quiescent base current are those parts between the base-one and base-two contacts. The center of the channel makes a negligible contribution to the interbase resistance.

One of the reasons for going to monolithic integrated circuit fabrication techniques is the uniformity of parameters achieved by these methods. This work indicates that this uniformity is a prerequisite for success.

It is recognized that this study is at most a successful first step toward a satisfying realization of neuristor lines. From a consideration of the results of this work, the next step appears to be a further reduction in the size of the geometries used. This smaller size would make possible the use of a smaller capacitance value for the emitter circuit and hence faster operation. Also, the value of capacitance must be reduced for it to be integrated. An equally important result of a reduction in size of the individual units is the ability to put many on one die and hence, in one header. In this manner both T and S junctions can be produced in one package.

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