A SOLID STATE CIRCUIT FOR GENERATING ULTRA-WIDE PULSES

by

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STATEMENT BY AUTHOR

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ABSTRACT

An ultra-wide pulse generator capable of high-duty cycle with a stable pulse duration and low standby power is developed. Novel means are employed to reduce standby power and recovery time. Characteristics of the generator are: (1) pulse duration variable from 3 milliseconds to 16.72 seconds, (2) stability of 0.03 per cent, (3) recovery time of 270 microseconds, and (4) a standby power of 10.8 milliwatts.

A very low-frequency astable square-wave generator is also discussed.

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Chapter 1

INTRODUCTION

A number of applications, for example biophysics, require long pulse duration monostable circuits.[1,2,3*] In general, the required characteristics of these circuits are: (1) wide range of pulse duration, (2) low standby power, (3) good stability, and (4) short recovery time. The objective of this paper is to develop a pulse generator that has these characteristics.

A timing circuit consisting of a voltage comparator, a capacitor, and a charging source forms the basis of the pulse generator. If the charging current is carefully controlled and the voltage comparator is sufficiently accurate, the time required to charge the capacitor to a particular voltage can be made very stable. This time then determines the pulse duration.

A unijunction transistor (hereafter abbreviated UJT) is used as the voltage comparator because of its extremely stable peak point voltage. The pulse generator developed using the UJT has a stability of 0.03 per cent, a standby power of 10.8 milliwatts, a pulse duration variable from 3 milliseconds to 16.72 seconds, and a recovery time of 270 microseconds.

The development of the pulse generator proceeds as follows:

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*Refer to the Bibliography, page 31.

1. Unijunction transistor physics and characteristics are briefly presented and the stability of the peak point voltage is discussed.
2. Two elementary charging circuits are analyzed and compared. It is shown that the constant current circuit is superior.
3. The block diagram of the generator is discussed and the timing circuit and the reset circuit are analyzed.
4. The practical circuit is discussed and experimental results are given. Theoretical calculations are found to be in close agreement with experimental results.
5. An astable square wave generator is shown as an extension of the monostable generator. An outstanding feature of this circuit is that the time duration of each $\frac{1}{2}$ cycle is independent of the other $\frac{1}{2}$ cycle and can be varied over the entire range of the monostable circuit time durations.

Chapter 2

UNIJUNCTION TIMING CIRCUITS

2.1 UNIJUNCTION TRANSISTORS[4,5,6,7]

The unijunction transistor is a three-terminal semiconductor device which exhibits between two terminals a negative resistance region bounded by two positive resistance regions. The terminal voltage is a single valued function of the current.

A bar of n-type material (usually silicon) with ohmic contacts at opposite ends is used to make the device. A single P-N junction is formed by a p-type wire (usually aluminum) located closer to one end than the other so the device is not symmetrical. The construction and symbol together with the principal voltages and currents are shown in Figure 2.1.

A simple equivalent circuit and a typical volt-ampere characteristic for the emitter-base 1 terminals are shown in Figure 2.2 (exaggerated to show details). An interbase resistance, R_{BB}, exists between base 1 and base 2. With no emitter current flowing, the silicon bar behaves like a simple voltage divider and a fraction, η, of V_{BB} appears at the N side of the emitter junction; where η is defined as

$$\eta \triangleq \frac{R_{B1}}{R_{B1} + R_{B2}} \tag{2.1}$$

and

$$R_{BB} = R_{B1} + R_{B2} \tag{2.2}$$

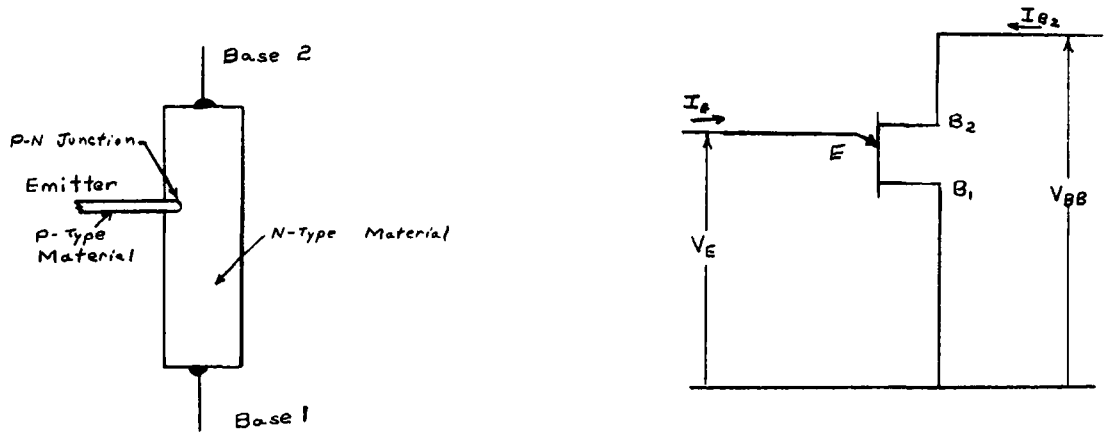
If $V_E < \eta V_{BB} + V_D$, the junction is reverse biased and only a small leakage current, I_{EO}, will flow in the emitter circuit. If $V_E > \eta V_{BB} + V_D$, the junction becomes forward biased and emitter current flows. This emitter current consists primarily of holes injected into the silicon bar. Because of the electric field within the silicon bar caused by V_{BB}, these holes move from the emitter to base 1 increasing the conductivity of this region. As the emitter current, I_E, is increased, the emitter voltage, V_E, will decrease due to the increased conductivity, thus resulting in a negative resistance characteristic between the emitter and base 1 terminals.

The two important points on the emitter characteristic curve are the peak point and the valley point. The region to the left of the peak point is the cutoff region where the emitter diode is reversed biased. Between the peak point and the valley point is the negative resistance region. The region to the right of the valley point is called the saturation region where the conduction is limited by the surface and bulk recombination of the holes and electrons.

The peak point voltage, V_P, is

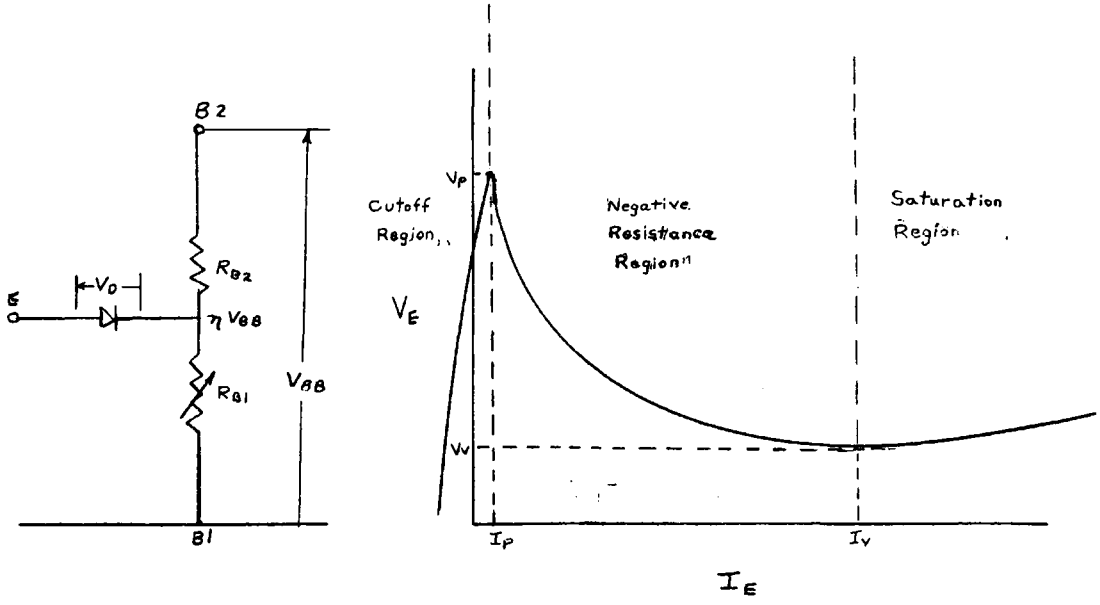
$$V_P = \eta V_{BB} + V_D \tag{2.3}$$

The peak point current, I_P, corresponds to the emitter current at the peak point. It represents the minimum current which must be applied to produce regeneration, and is usually less than 10 microamperes.



CONSTRUCTION AND SYMBOL FOR THE UNIJUNCTION TRANSISTOR

Figure 2.1



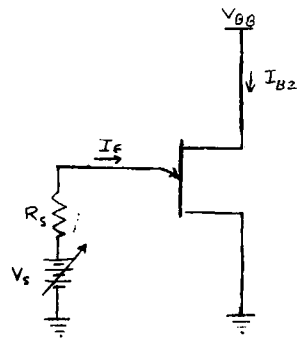
A SIMPLE EQUIVALENT CIRCUIT AND A TYPICAL EMITTER-BASE 1 VOLT-AMPERE CHARACTERISTIC FOR A UNIJUNCTION TRANSISTOR

Figure 2.2

The UJT can be used as a voltage comparator by using the parameter V_P in the following manner. A variable voltage source V_S with some internal resistance R_S is connected between the emitter and base 1 terminal as shown in Figure 2.3. This voltage source and resistance form a load line on the Emitter-Base 1 characteristic (Figure 2.4). The operating point is the intersection of the load line with the characteristic curve. If V_S is lower than V_P, the operating point is in the cutoff region (points A and B). As V_S is increased, the load line moves up as does the operating point. When V_S is increased so that the load line no longer intersects the curve in the cutoff region, the circuit is regenerative and the operating point moves down the load line until it again intersects the curve (point C). Emitter current then flows which in turn causes an increase in I_{B2} which can be detected and used as an indication that V_S has become greater than V_P.

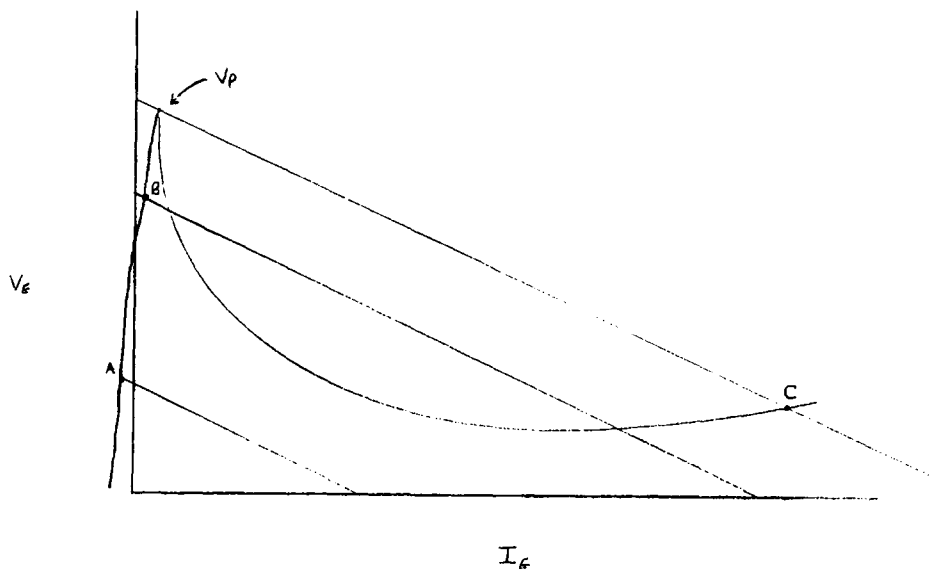
To determine the accuracy of the comparator, the stability of V_P must be investigated. It will be noted from equation (2.3) that V_P is dependent upon η and V_D. From equation (2.1), it is evident that η is independent of temperature even though R_{B1} and R_{B2} may vary with temperature as long as R_{B1} and R_{B2} have the same temperature dependence. It has been shown experimentally that the temperature coefficient of η is less than $\pm$ 0.001%/C°.[4]

V_D is dependent upon temperature and is the principal reason for the variation of V_P with temperature. V_P may be temperature compensated by the addition of a small resistor, R_2, in series with



EXAMPLE OF UJT VOLTAGE COMPARATOR

Figure 2.3



EMITTER-BASE 1 V-I CHARACTERISTIC FOR FIGURE 2.3

Figure 2.4

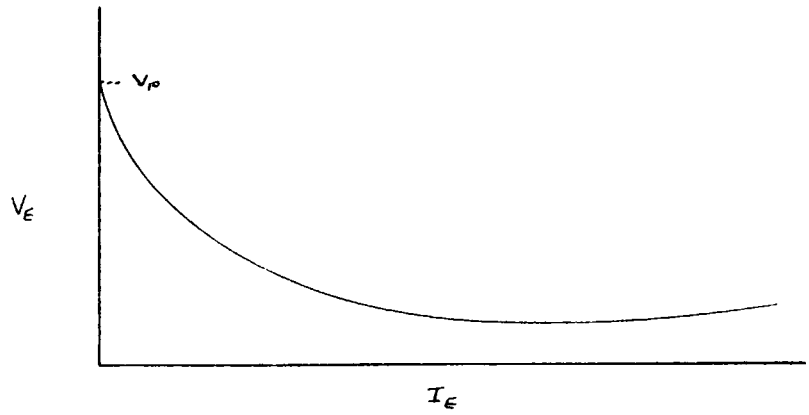
base 2. Jones[8] gives the approximate value of this resistor as

$$R_2 = \frac{.7R_{BB}}{\eta V_1} \tag{2.4}$$

where V_1 is the supply voltage. If R_2 satisfies equation (2.4),

$$V_P = \eta V_1 \tag{2.5}$$

With V_P thus compensated, the UJT is a very accurate voltage comparator. The use of the device in two simple circuits will be discussed in the next two sections. In these circuits, the emitter-base 1 V-I characteristics are idealized (Figure 2.5). The emitter reverse leakage current is neglected and the V-I characteristic is shifted to the left so that the peak point falls on the $I_E = 0$ axis. I_P will still be used as the minimum current required to produce regeneration. Most of the time the charging current will be much greater than I_P so this approximation is valid. However, when the current approaches I_P, it must be realized that the equations are only an approximation.



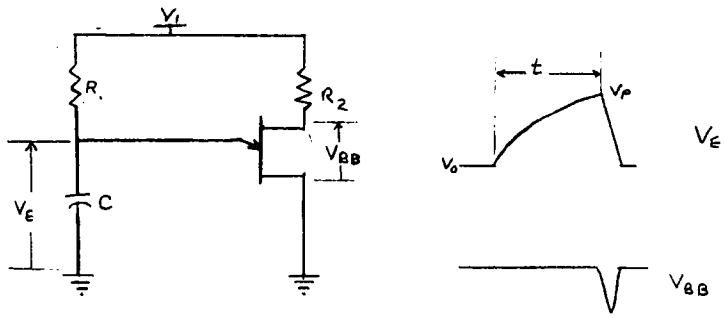
AN IDEALIZED EMITTER-BASE 1 V-I CHARACTERISTIC

Figure 2.5

2.2 RC CHARGING CIRCUIT

The UJT may be used as a voltage comparator to detect when a capacitor has charged to a specified voltage. Figure 2.6 shows an RC charging circuit consisting of a voltage source V_1, an RC network, and the UJT used as a voltage comparator. The waveforms are also shown in the figure. Assume the initial voltage of the capacitor is V_0 and V_1 is applied at t = 0. Capacitor C charges exponentially toward V_1 through R. When the voltage V_E reaches V_P, the circuit regenerates and emitter current flows discharging C. If R_2 is calculated from equation (2.4), the charging time is

$$t_{RC} = RC \ \ell n \ \frac{V_1 - V_0}{V_1(1-\eta)} \qquad (2.6)$$



AN RC CHARGING CIRCUIT

Figure 2.6

The load line formed by R and V_1 must intersect the emitter characteristics to the right of the peak point. This condition may be stated as

$$\frac{V_1 - V_P}{R} > I_P$$

or

$$R < \frac{V_1 - V_P}{I_P} \tag{2.7}$$

I_P is specified at $V_{BB} = 25$ volts and is inversely proportional to V_{BB}.[10] Equation (2.7) may be written

$$R < \frac{(1-\eta)V_1}{I_P}$$

$$I_P = \frac{25I_{PO}}{V_{BB}} \approx \frac{25I_{PO}}{V_1} \quad \text{for } R_2 \text{ small where}$$

$$I_{PO} = I_P \text{ at } V_{BB} = 25.$$

Then

$$R < \frac{(1-\eta)V_1^2}{25I_{PO}} \tag{2.8}$$

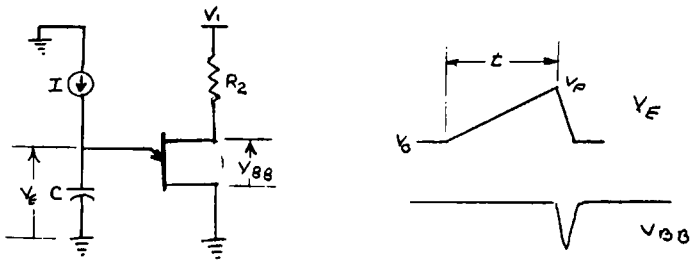
Equation (2.8) sets a maximum value for R and thus sets a maximum period for any given values of C and V_1.

2.3 CC CHARGING CIRCUIT

C can also be charged with a constant current source as shown in Figure 2.7. The increase of capacitor voltage is then approximately linear with time until V_P is reached, at which time the circuit regenerates. The charging time is given approximately by

$$t_{CC} = \frac{(V_P - V_0)C}{I} \quad \text{or} \quad \frac{(\eta V_1 - V_0)C}{I} \tag{2.9}$$

For regeneration, I must be greater than I_P. Thus the maximum charging time is set by the minimum current I_P.



A CC CHARGING CIRCUIT

Figure 2.7

2.4 COMPARISON OF RC AND CC CHARGING CIRCUITS

Since the purpose of the timing circuit is to generate a highly stable long duration time reference, it is interesting to examine and compare the two circuits as to maximum time duration and stability.

First, the maximum charging time for the two circuits will be compared. From equations (2.6)and (2.9), the maximum charging times (neglecting the reverse emitter current) are

$$t_{RC} = \frac{V_1(1-\eta)C}{I_P} \ln\left[\frac{V_1 - V_0}{V_1(1-\eta)}\right]$$

and

$$t_{CC} = \frac{(\eta V_1 - V_0)C}{I_P}$$

If we let $V_0 \approx 0$, a condition which will be satisfied in Chapter 3,

$$t_{RC} = \frac{V_1(1-\eta)C}{I_P} \ln\left(\frac{1}{1-\eta}\right)$$

$$t_{CC} = \frac{V_1 C \eta}{I_P}$$

For a typical value of $\eta = .65$:

$$t_{RC} = \frac{V_1 C .37}{I_P}$$

$$t_{CC} = \frac{V_1 C .65}{I_P}$$

Thus the constant current circuit can produce a maximum charging time almost twice that of the RC circuit.

We will now examine the change in t for a specified change in V_P (uncertainty of V_P) for the two circuits. For the RC circuit, the time duration was found to be

$$t_{RC} = RC \ln \frac{1}{1-\eta}$$

The rate of change of capacitor voltage at any point is

$$\frac{dv}{dt} = \frac{V_1 e^{-t/RC}}{RC}$$

The time duration for the CC circuit is

$$t = \frac{\eta V_1 C}{I}$$

and its capacitor voltage rate of change is

$$\frac{dv}{dt} = \frac{I}{C}$$

To make a just comparison, the time interval should be the same. This requires

$$I = \frac{\eta V_1}{R \ln\left(\frac{1}{1-\eta}\right)}$$

For small changes in V,

$$\frac{\Delta V_P}{\Delta t} = \frac{dv}{dt} \text{ or } \Delta t = \frac{1}{\frac{dv}{dt}} \Delta V_P$$

Thus $\Delta t_{RC} = \frac{RC\ e^{t/RC}}{V_1} \Delta V_P$ and $\Delta t_{CC} = \frac{RC \ln \frac{1}{1-\eta}}{\eta V_1} \Delta V_P$

Therefore, for a typical value of $\eta = .65$

$$\ln \frac{1}{1-\eta} \approx 1 \text{ and } t \approx RC$$

so that $\Delta t_{RC} = \frac{RC}{V_1}\ 2.72\, \Delta V_P$ and $\Delta t_{CC} = \frac{RC}{V_1}\ 1.54\, \Delta V_P$

Thus for the same peak point voltage uncertainty, ΔV_P, the change of time duration of the RC circuit is 1.76 times greater than that of the constant current circuit.

The CC circuit is superior both with regard to maximum time duration and sensitivity to V_P uncertainty. For these reasons, the CC circuit is the basis for a stable ultra-wide pulse generator which is discussed in the next chapter.

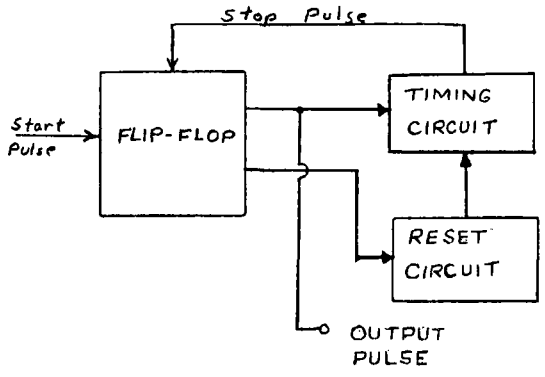
Chapter 3

AN ULTRA WIDE PULSE GENERATOR

3.1 INTRODUCTION

The constant current charging circuit developed in Chapter 2 will be incorporated in the design of a highly stable ultra wide pulse generator, the block diagram of which is shown in Figure 3.1.

The generator consists of a timing circuit, a reset circuit, and a bistable multivibrator, or flip-flop. The timing circuit and the reset circuit are switched on and off by the flip-flop.



BLOCK DIAGRAM OF ULTRA WIDE PULSE GENERATOR

Figure 3.1

Prior to the application of the start pulse (that is, standby condition) the timing circuit is off (charging source is off) and the reset circuit is on. To generate a pulse, a start pulse is applied to the flip-flop. The flip-flop changes state, turning the timing circuit on and the reset circuit off. At the end of the charging time, the timing circuit generates a stop pulse which triggers the flip-flop black into its standby state. This turns the timing circuit off and the reset circuit on. Each block of the generator will be discussed in the next sections.

3.2 TIMING CIRCUIT

The complete timing circuit including its switching elements is shown in Figure 3.2. Transistor Q_6 provides the constant current source which charges capacitor C. Q_5 is used to turn Q_6 off and on and Q_7 is used to turn on or off the voltage applied to the UJT, Q_8.

In the standby condition, Q_5 and Q_7 are turned off by the flip-flop. With Q_5 off, there is no forward bias on Q_6 so it is also off.

When the start pulse is applied to the flip-flop and it changes states, Q_5 and Q_7 are both turned on. Enough base drive is applied to these transistors to saturate them. With Q_7 saturated, V_1 (less the small saturation voltage of Q_7) is applied to base 2 of the UJT Q_8.

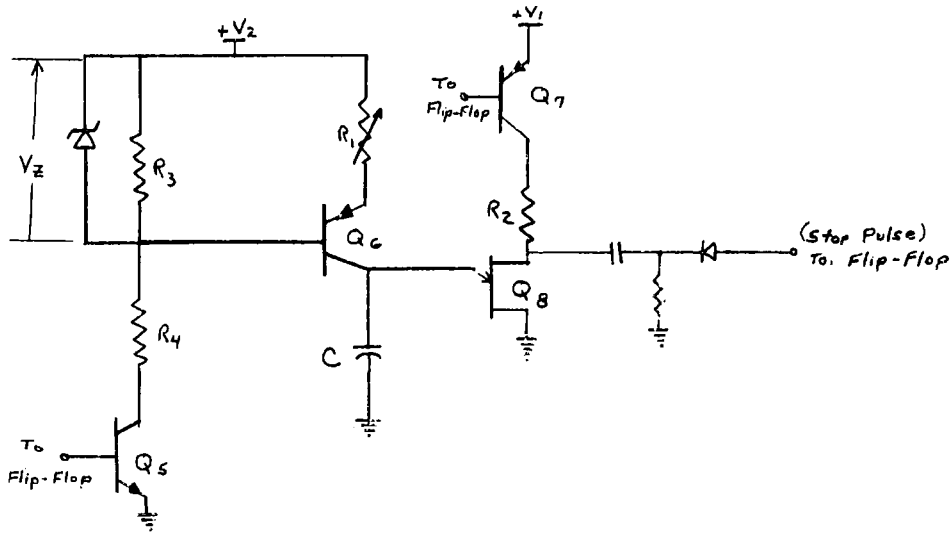
Q_5 switching into saturation causes a current to flow through R_3 and R_4. The voltage drop across R_3 is set by the zener diode D_1. This voltage, V_Z, turns on Q_6 and causes a constant cur-

rent, I_C, to flow from the collector of Q_6. I_C can be adjusted by varying R_1. The value of this current is

$$I_C = \frac{\alpha[V_Z - V_{D6}]}{R_1} \tag{3.1}$$

where V_{D6} is the emitter-base voltage drop of Q_6 and α is the common base current gain of Q_6.

This current charges C until V_p is reached, where emitter current flows in the UJT. At this time regeneration occurs and a pulse is taken from base 2 of Q_8 which triggers the flip-flop into the standby state, which in turn cuts off Q_5 and Q_6.



TIMING CIRCUIT

Figure 3.2

A novel feature of the circuit is the use of Q_7 to supply current to the UJT. It will be noted that resistor R_2 could be

connected directly to V_1 to supply bias current to the UJT. However, bias current is required only during the charging time. Thus the use of Q_7 to switch the bias current provides current at the required time but reduces the standby power of the UJT to almost zero. This, together with the use of Q_5 to switch charging current, reduces the standby power of the entire charging circuit to very nearly zero.

3.3 DISCUSSION OF PULSE DURATION

The pulse duration can be calculated by substituting equation (3.1) in equation (2.9). The pulse duration then becomes

$$t = \frac{R_1 C(\eta V_1 - V_0)}{\alpha (V_Z - V_{D6})} \tag{3.2}$$

To determine the limits on the duration, the minimum and maximum charging currents must be investigated. The minimum current that the transistor constant current source can supply is the leakage current of the transistor. The charging current must be larger than the peak point current, I_p, or the UJT will not regenerate. In general, a low leakage transistor is used for the constant current source and its leakage current is less than I_p. If this is the case, then the maximum pulse duration is set by I_p of the UJT. Thus an estimate of the maximum pulse duration may be obtained by assuming that the capacitor is charged by a current I_p to a voltage V_p

$$t_{max} \cong \frac{CV_p}{I_p} \tag{3.3}$$

There are two factors which may cause a lower limit of the pulse duration to exist: the increase of junction temperature due to power dissipation, and a maximum collector current limit due to effects other than power dissipation.

(1) The junction temperature of a transistor is a function of the power dissipation and the thermal characteristics of the transistor. For steady-state conditions, the maximum power dissipation in watts is given by

$$P_{max} = \frac{T_{j\ max} - T_a}{\theta} \tag{3.4}$$

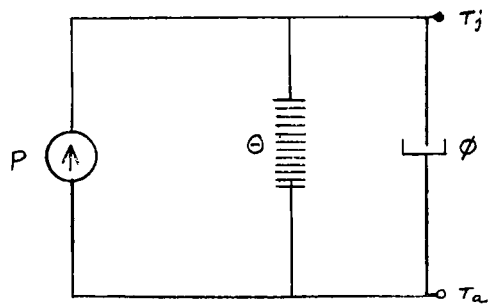
where $T_{j\ max}$ is the maximum allowable junction temperature in degrees centigrade, T_a is the ambient temperature in degrees centigrade, and θ is the thermal resistance measured in degrees centigrade per watt. Associated with the thermal resistance is a thermal capacitance, ϕ, measured in watt-seconds per degree centigrade. Thus a lumped representation of the thermal behavior of the transistor is as shown in Figure 3.3. It will be noted that the product of θ and ϕ is the thermal time constant.

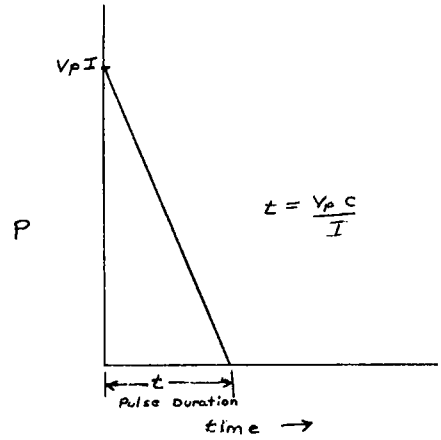
The power waveform of the charging transistor is also shown in Figure 3.3.

If the pulse duration is very small in comparison with the thermal time constant, the power, as a function of time, may be approximated by an impulse whose energy is equal to the total energy of the actual power waveform. From Figure 3.3, it will be noted that when an impulse of power is applied to the thermal cir-

cuit, all of the energy is stored in the thermal capacitance, ϕ. But the total energy of the power waveform is simply the change of energy stored in the electric capacitor C; namely

$$\int_0^t P\, dt = \frac{1}{2} C\, V_P^2 \tag{3.5}$$





A TRANSISTOR THERMAL NETWORK

Figure 3.3

Thus the change of junction temperature is simply

$$\Delta T_j = \frac{\text{energy stored}}{\text{thermal capacitance}} = \frac{CV_P^2}{2\phi} \tag{3.6}$$

If the transistor has a maximum junction temperature, $T_{j\ max}$, and is operating in an environment with ambient temperature, T_a, then the maximum allowable capacitance as the pulse duration approaches zero is

$$C_{max} = \frac{2\phi(T_{j\ max} - T_a)}{V_P^2} \tag{3.7}$$

Note that the minimum pulse duration for $C = C_{max}$ approaches zero. The maximum pulse duration, however, is now given by

$$t_{max} = \frac{C_{max} V_P}{I_P} \tag{3.8}$$

If longer pulses are required, then a larger C must be used; the minimum pulse duration will be set by other constraints such as a maximum value of collector current.

(2) If a maximum collector current, I_{max}, is specified, then the minimum pulse duration is

$$t_{min} = \frac{CV_P}{I_{max}} \tag{3.9}$$

Thus for this case, the ratio of maximum to minimum pulse duration is

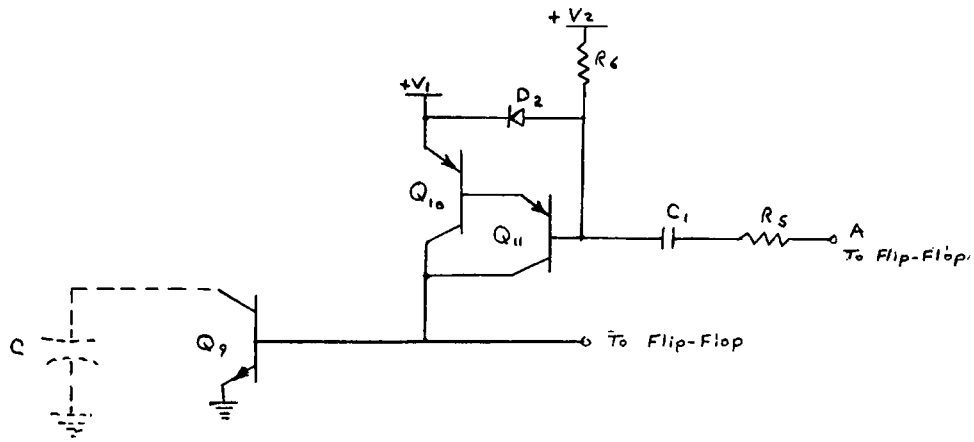
$$\frac{t_{max}}{t_{min}} = \frac{I_{max}}{I_P} \tag{3.10}$$

3.4 RESET CIRCUIT

At the end of the timing cycle, emitter current flows in the UJT discharging the capacitor C. The discharge time is dependent upon the value of the capacitor and the emitter saturation resistance of the UJT and this time is of the same order of magnitude as the minimum pulse duration. Also the UJT does not discharge the capacitor completely but regenerates back into the cutoff region when the valley voltage is reached. Any leakage current in the circuit could affect the voltage on the capacitor and if a new timing cycle is started, the initial voltage, V_0, would be different causing the

pulse duration to change.

A novel feature of the pulse generator circuit is the reset circuit, which performs two functions. First, it provides a means of rapidly discharging C. Second, it maintains a constant capacitor voltage during the standby period. It will be noted that a large current is required to discharge C rapidly and if this current were allowed to flow continuously in the standby condition, the standby power would be high. For this reason, the reset circuit is so designed that a large but transient current flows to discharge the capacitor. The reset circuit is shown in Figure 3.4.



A RESET CIRCUIT

Figure 3.4

The transient function is performed by the RC circuit R_5 and C_1, and transistors Q_{10}, Q_{11}, and Q_9. Q_{10} and Q_{11} are connected in the Darlington configuration to produce a large current gain.[9] The transistors are biased off by V_1, V_2, R_6, and D_2. When the flip-

flop switches from the timing cycle to the standby cycle, the voltage at point A switches from $+V_1$ to ground. This change of voltage is coupled by C_1 and R_S to Q_{11} and Q_{10}, turning them on and causing a large current I_{C2} to flow. When C_1 has charged to V_1, Q_{10} and Q_{11} are again cut off. The approximate equation for the current I_{C2} is

$$I_{C2} = (\beta^2 + 2\beta) \frac{V_1}{R_S} e^{-\frac{t}{R_S C_1}} \tag{3.11}$$

where β is the common emitter current gain of the transistors, and the cutoff frequency of the transistors has been assumed to be very high.

This current, I_{C2}, flows into the base of Q_9 which has been turned on by the flip-flop. BI_{C2} then discharges the capacitor. The approximate equation for discharge time is thus

$$t_r = R_S C_1 \ln\left[\frac{\eta C + (\beta^3 + 2\beta^2) C_1}{(\beta^3 + 2\beta^2) C_1}\right] \tag{3.12}$$

After the transient current ends, Q_9 is held in saturation by the flip-flop. This holds the voltage across C constant at the saturation voltage of Q_9, establishing a constant initial voltage. When the timing cycle starts, Q_9 is switched off allowing C to charge.

It is of interest to estimate the maximum duty cycle for the pulse generator. The maximum duty cycle will be obtained when the generator is operated with maximum pulse duration. For a small recovery time, equation (3.12) may be approximated as

$$t_r \cong \frac{R_S \eta C}{(\beta^3 + 2\beta^2)} \tag{3.13}$$

then

$$\frac{t_{max}}{t_r} = \frac{V_p(B^3 + 2B^2)}{I_p R_S} \qquad (2.14)$$

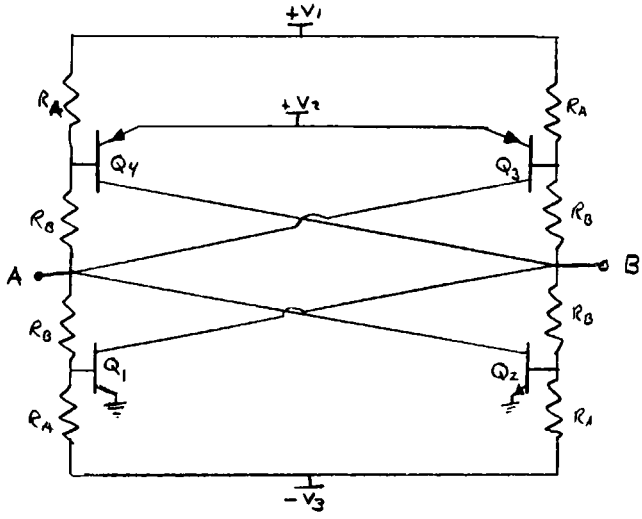
For typical values

$$\frac{t_{max}}{t_r} = 8.8 \times 10^5$$

The theoretical maximum duty cycle with maximum pulse duration is thus $(1 - .13 \times 10^{-5}) \times 100\%$.

3.5 FLIP-FLOP

Since the standby power requirement was low, several different flip-flops required investigation. A complementary symmetry flip-flop[10] was chosen because it operates with very low standby power, and at the same time provides complementary outputs. A detailed discussion of this circuit is available in the literature, and therefore it will be discussed only qualitatively here. The circuit is shown in Figure 3.5.



A COMPLEMENTARY SYMMETRY FLIP-FLOP

Figure 3.5

The flip-flop has two stable states: (1) Q_1 and Q_3 on, Q_2 and Q_4 off or (2) Q_1 and Q_3 off, Q_2 and Q_4 on. When the transistors are on, enough base current is supplied so that they are saturated. The output voltage then is approximately either V_2 or ground, and can be taken either from point A or point B or both. Points A and B are complementary outputs ($A = V_2$, $B = 0$ or $A = 0$, $B = V_2$).

Because the collector current of one of the on transistors supplies only the base current of the other on transistor, and the load current, the power in this circuit is very low (for example, the power for the flip-flop used in the generator is only 3.8 milliwatts). No additional current sources or sinks are necessary.

3.6 A PRACTICAL CIRCUIT

A practical embodiment of the pulse generator circuit is shown in Figure 3.6.

The pulse duration was measured by connecting a Hewlett-Packard Model 5240 Electronic Counter with a time interval plug-in unit to the output of the generator. Pulse duration was measured as a function of R_1. These values are plotted in Figure 3.7. Also plotted in the same figure are values calculated using equation (3.2). The measured values compared very well with the calculated values, the maximum error being 7 per cent. The maximum pulse duration was 16.72 seconds as compared with a calculated value of 16.25 seconds. For this particular circuit, the minimum time duration was determined by the maximum current limit of the power supply, namely 225 milliamperes. Thus the minimum measured pulse duration

was 3 milliseconds. Since this situation does not represent the maximum allowable collector current, or power dissipation, of the transistors, this minimum could be reduced by using a different power supply.

To determine the stability of pulse duration, the generator was set for a pulse duration of 2.0000 seconds and the measurements were taken over a period of two hours with a measurement taken approximately every 20 seconds. The maximum deviation in this period was +0.00059 seconds and -0.00043 seconds, which is a deviation of $\pm$0.03 per cent.

The calculated and measured values of reset time were 300 microseconds and 270 microseconds, respectively.

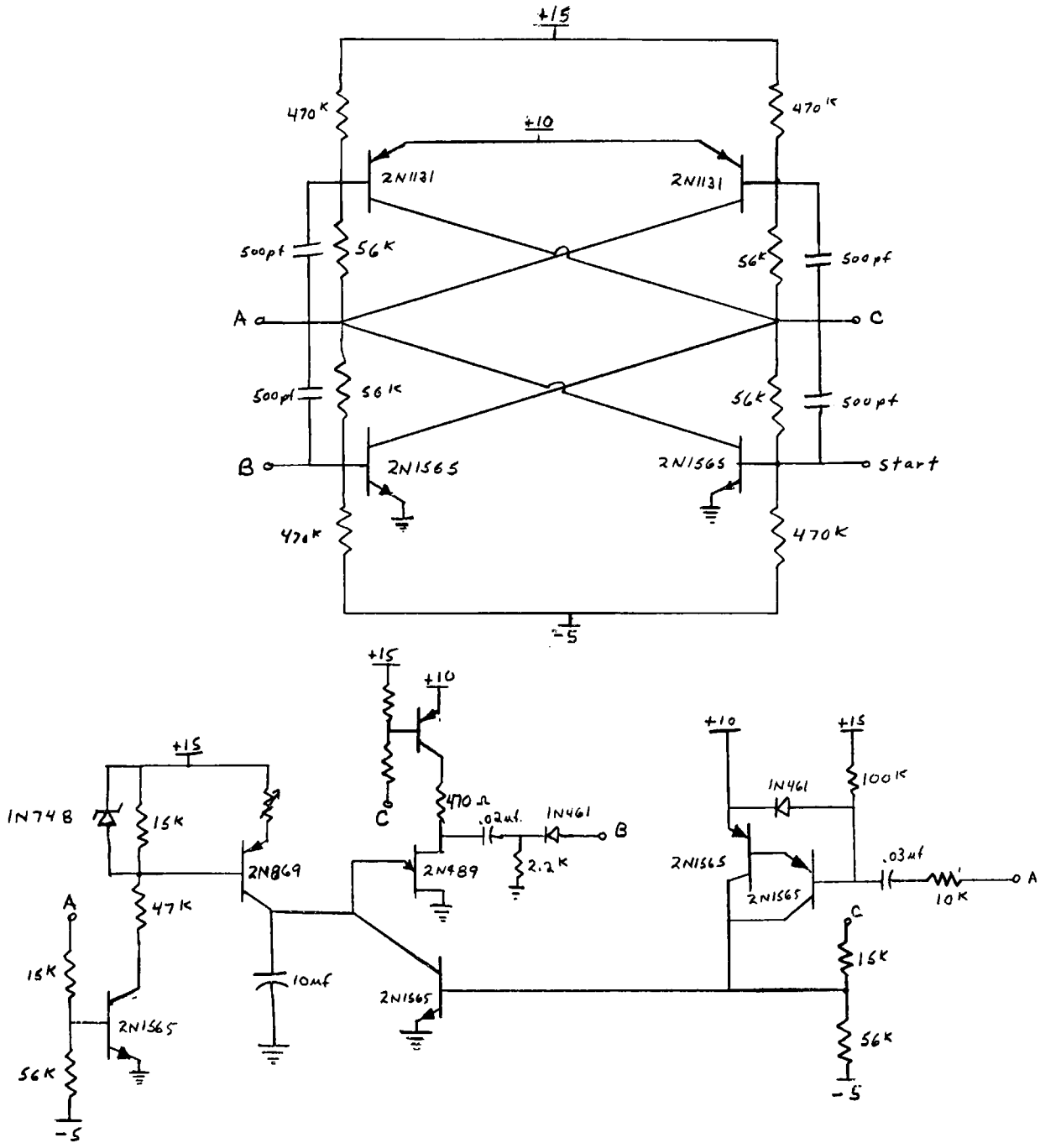
The calculated and measured values of standby power were 7.8 milliwatts and 10.8 milliwatts, respectively.

It is thus evident that the generator designed in this paper meets all the required characteristics mentioned in the introduction: (1) wide range of pulse duration, (2) low standby power, (3) high stability, and (4) short recovery time.

3.7 ASTABLE SQUARE-WAVE GENERATOR

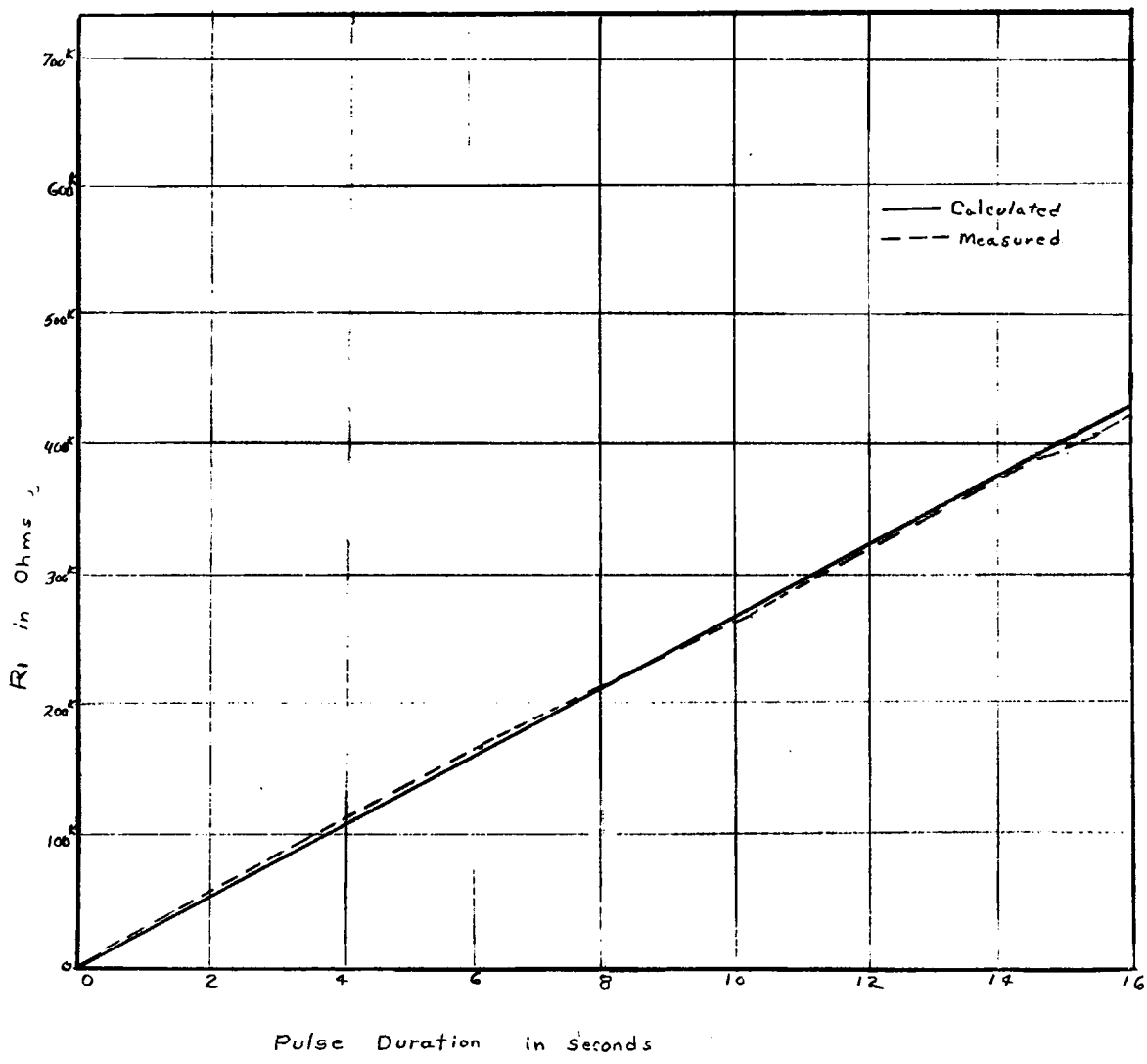
The monostable generator developed in this paper can be expanded into a versatile astable square-wave generator by the addition of another timing circuit and another reset circuit. The block diagram is shown in Figure 3.8.

It will be noted that this is essentially two monostable generators showing a common flip-flop. In this way the stop pulse of one circuit becomes the start pulse of the other circuit. The



A PRACTICAL CIRCUIT

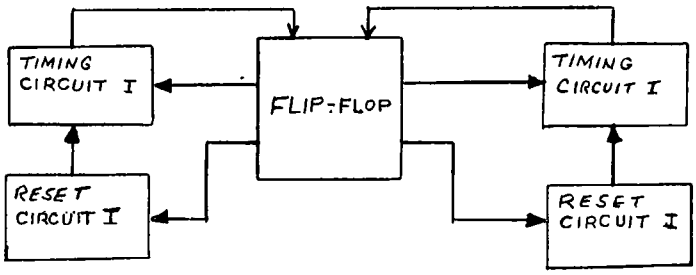
Figure 3.6



CALCULATED PULSE DURATION VERSUS MEASURED PULSE DURATION

Figure 3.7

timing circuit and the reset circuit are connected to the complementary points of the flip-flop to which the original circuits were connected.



BLOCK DIAGRAM OF AN ASTABLE SQUARE-WAVE GENERATOR

Figure 3.8

This circuit has several outstanding features.

(1) Each $\frac{1}{2}$ cycle can be varied independently of the other $\frac{1}{2}$ cycle over the entire range of the monostable circuit pulse duration.

(2) Ratio between the half cycles could be as high as the dynamic range (that is, duration of $\frac{1}{2}$ cycle equal to minimum t, duration of other equal to maximum t).

(3) Minimum frequency of symmetrical square-wave is $\frac{1}{2t_{max}}$ where t_{max} is the maximum pulse duration of the monostable circuit.

Chapter 4

CONCLUSIONS

In this paper, an ultra-wide pulse generator has been developed. The circuit makes use of the regenerative properties and the highly stable peak point of a unijunction transistor to provide an indication of the time required for a capacitor to charge through a given voltage range.

Two charging circuits have been investigated and it has been shown that the constant current charging circuit is the superior circuit. A pulse generator has been developed using the basic CC charging circuit together with a flip-flop and a reset circuit. Equations have been developed for pulse duration, limits for maximum and minimum pulse duration, recovery time, and maximum duty cycle.

The pulse generator has been constructed and tested; good agreement between calculated and measured value was obtained.

The principal contributions of the thesis are:

(1) An accurate constant current timing circuit which can be operated with low standby power.

(2) A novel low standby power reset circuit to assure fast recovery time and also set initial conditions for the timing circuit.

(3) A means of switching UJT bias current to reduce standby power.

(4) An extension of the monostable circuit to include a very low-frequency astable square-wave generator.

The temperature dependence of the pulse duration has not been investigated. Since the UJT can be reasonably compensated, it appears that the major sources of error due to temperature effects will be the CC source transistor and the discharge transistor. It should be possible to develop compensating techniques.

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