THE DESIGN OF A BUFFER FOR COMMUNICATION BETWEEN
TAPE DRIVE AND DIGITAL COMPUTER

by

Wilton J. Daniel, Jr.

A Thesis Submitted to the Faculty of the
DEPARTMENT OF ELECTRICAL ENGINEERING
In Partial Fulfillment of the Requirements
For the Degree of
MASTER OF SCIENCE
In the Graduate College
The University of Arizona

1964
STATEMENT BY AUTHOR

This thesis has been submitted in partial fulfillment of requirements for an advanced degree at the University of Arizona and is deposited in the University Library to be made available to borrowers under rules of the Library.

Brief quotations from this thesis are allowable without special permission, provided that accurate acknowledgment of source is made. Requests for permission for extended quotation from or reproduction of this manuscript in whole or in part may be granted by the head of the major department or the Dean of the Graduate College when in his judgment the proposed use of the material is in the interests of scholarship. In all other instances, however, permission must be obtained from the author.

SIGNED: [Signature]

APPROVAL BY THESIS DIRECTOR

This thesis has been approved on the date shown below:

[Signature]
GERALD R. PETERSON
Associate Professor of Electrical Engineering

Date: 14 May 1964
ACKNOWLEDGMENT

The author wishes to express his appreciation to Dr. Gerald R. Peterson for his encouragement and many helpful suggestions during the work on this thesis. I would also like to thank Michael Larriva for the time he spent discussing the problems that arose in the buffer design. Without the help of these two people, this thesis would not have been completed.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>LIST OF ILLUSTRATIONS</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>v</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td>vii</td>
</tr>
<tr>
<td>CHAPTER 1 INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>1.1 Digital Computer</td>
<td>1</td>
</tr>
<tr>
<td>1.2 Tape Drive</td>
<td>8</td>
</tr>
<tr>
<td>CHAPTER 2 SYSTEM REQUIREMENTS</td>
<td>10</td>
</tr>
<tr>
<td>2.1 Computer</td>
<td>10</td>
</tr>
<tr>
<td>2.2 Tape Drive</td>
<td>11</td>
</tr>
<tr>
<td>2.3 Sequence of Operations</td>
<td>12</td>
</tr>
<tr>
<td>CHAPTER 3 LOGIC DESIGN</td>
<td>17</td>
</tr>
<tr>
<td>3.1 Function Control Circuits</td>
<td>17</td>
</tr>
<tr>
<td>3.2 Tape Control Circuits</td>
<td>20</td>
</tr>
<tr>
<td>3.3 Write Circuits</td>
<td>25</td>
</tr>
<tr>
<td>3.4 Read Circuits</td>
<td>36</td>
</tr>
<tr>
<td>3.5 Cost Estimate</td>
<td>46</td>
</tr>
<tr>
<td>3.6 Conclusion</td>
<td>47</td>
</tr>
<tr>
<td>APPENDIX</td>
<td>48</td>
</tr>
<tr>
<td>A.1 Output Program</td>
<td>48</td>
</tr>
<tr>
<td>A.2 Input Program</td>
<td>49</td>
</tr>
<tr>
<td>A.3 Tape Format</td>
<td>51</td>
</tr>
<tr>
<td>REFERENCES</td>
<td>53</td>
</tr>
</tbody>
</table>

iv
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>COMPUTER WORD</td>
<td>2</td>
</tr>
<tr>
<td>1.2</td>
<td>COMPUTER CONTROL BLOCK DIAGRAM</td>
<td>5</td>
</tr>
<tr>
<td>1.3</td>
<td>COMPUTER DATA FLOW</td>
<td>6</td>
</tr>
<tr>
<td>1.4</td>
<td>TAPE DATA FLOW</td>
<td>9</td>
</tr>
<tr>
<td>3.1</td>
<td>BUFFER UNIT BLOCK DIAGRAM</td>
<td>18</td>
</tr>
<tr>
<td>3.2</td>
<td>LOGIC SYMBOLS</td>
<td>19</td>
</tr>
<tr>
<td>3.3</td>
<td>SELECT DECODE CIRCUIT</td>
<td>21</td>
</tr>
<tr>
<td>3.4</td>
<td>OPERATION DECODE CIRCUIT</td>
<td>21</td>
</tr>
<tr>
<td>3.5</td>
<td>TAPE CONTROL CIRCUITS</td>
<td>23</td>
</tr>
<tr>
<td>3.6</td>
<td>READ SPROCKET</td>
<td>24</td>
</tr>
<tr>
<td>3.7</td>
<td>WRITE CIRCUIT BLOCK DIAGRAM</td>
<td>27</td>
</tr>
<tr>
<td>3.8</td>
<td>DISASSEMBLY CIRCUITS</td>
<td>28</td>
</tr>
<tr>
<td>3.9</td>
<td>MODULO 5 COUNTER</td>
<td>29</td>
</tr>
<tr>
<td>3.10</td>
<td>PARITY GENERATE CIRCUITS</td>
<td>31</td>
</tr>
<tr>
<td>3.11</td>
<td>WRITE PARITY CHECK CIRCUITS</td>
<td>32</td>
</tr>
<tr>
<td>3.12</td>
<td>WRITE TAPE MOTION CIRCUITS</td>
<td>33</td>
</tr>
<tr>
<td>3.13</td>
<td>WRITE TIMING SEQUENCE CIRCUIT</td>
<td>34</td>
</tr>
<tr>
<td>3.14</td>
<td>READ CIRCUIT BLOCK DIAGRAM</td>
<td>37</td>
</tr>
<tr>
<td>3.15</td>
<td>ASSEMBLY CIRCUITS</td>
<td>38</td>
</tr>
<tr>
<td>3.16</td>
<td>READ PARITY CHECK CIRCUITS</td>
<td>40</td>
</tr>
<tr>
<td>3.17</td>
<td>LONGITUDINAL CHECK CIRCUITS</td>
<td>42</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>-------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>3.18</td>
<td>READ TAPE MOTION CIRCUITS</td>
<td>43</td>
</tr>
<tr>
<td>3.19</td>
<td>READ TIMING SEQUENCE CIRCUIT</td>
<td>44</td>
</tr>
<tr>
<td>A.1</td>
<td>OUTPUT PROGRAM</td>
<td>49</td>
</tr>
<tr>
<td>A.2</td>
<td>INPUT PROGRAM</td>
<td>50</td>
</tr>
<tr>
<td>A.3</td>
<td>TAPE FORMAT</td>
<td>52</td>
</tr>
</tbody>
</table>
ABSTRACT

This thesis presents a design of a buffer unit which controls communication between an experimental General Electric digital computer and a magnetic tape drive manufactured by International Business Machines.

First, a general discussion of the two units involved is presented. Then, the theoretical requirements to allow the digital computer to control the tape drive is discussed.

A design of a buffer unit to meet the above requirements is explained. This design is based on two basic specifications. First, the majority of control of the tape drive is performed independently of the digital computer to allow the maximum amount of internal memory to be used for other purposes. Secondly, whenever a choice in design requirements is available, the more general method is used to allow maximum flexibility.
CHAPTER 1
INTRODUCTION

The variety of jobs for which the modern, general purpose digital computer is used requires that these computers be as flexible as possible while remaining economical. The flexibility of any given machine is determined largely by the size of memory in that machine. The machine with a small memory will be less versatile than the machine with a large memory. The digital computer with which this report is concerned has an internal capacity of only 512 words. Since an IBM Tape Drive Model 727 is available, it was decided to use this unit to increase the memory in the digital computer. This thesis describes the design of a buffer unit to allow the computer to communicate with the tape drive.

1.1 Digital Computer

The digital computer, which is the center of the system, is a solid state, electronic computer utilizing diode and transistor logic. The computer uses asynchronous logic which allows each electronic circuit to operate at its own characteristic speed. Completion signals are generated within each logical block to allow the operations to shift to another control block. The speed of the computer is comparable to synchronous machines of ten megacycle clock frequency.

The computer word consists of eight octal characters plus sign (Fig. 1.1). Each octal character is formed by three binary bits, and
### FIGURE 1.1  COMPUTER WORD

<table>
<thead>
<tr>
<th>Op Code</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 Bits</td>
<td>10 Bits</td>
</tr>
</tbody>
</table>

Sign bit

| 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

Information

Instructions
the sign consists of one binary bit. Numerical data are handled in a binary coded representation. For positive numbers the normal binary coded representation is used: for negative numbers the two's complement form is used. The sign of the number is indicated by bit 25; 0 if positive, 1 if negative.

Instruction words are in a single address format. In an instruction, only bits 1-14, 15 and 25 are used. Bits 1-10 constitute the address field, while bits 11-14 designate the operation code. Special operations may be performed by inserting bits in positions 15 and 25. If bit 25 is a "one" in an instruction, indirect addressing occurs. That is, the address specified by the instruction represents the address in memory which contains the address of the data upon which the instruction is to operate. This allows the computer to treat the address of the information as data. When bit 15 is one, the computer will interrupt its program to allow data to be transmitted through the peripheral interface adapter, which consists of two 8 bit buffers and a 7 bit buffer. This interrupt feature enables the computer to operate at its ten megacycle rate without excessive time used for input-output.

The computer is organized into 16 logical control blocks. Within each control block several operations are performed simultaneously and independently of one another. As each operation is completed, a signal is generated. Only when all the completion signals for each operation in that block have been received will the machine shift in to the next control block.
Figure 1.2 represents the organization of the 16 control blocks. Blocks 1-4 and 15 constitute the analysis, or fetch cycle. In the analysis cycle the instruction is brought from memory, broken down into its separate parts, and stored in the proper registers. If an operand is necessary, it is brought into the machine from memory. The computer is now prepared to execute the command.

Blocks 5-11 and 0 represent the execute cycle. During this cycle the operation specified by the instruction is executed. All arithmetic operations and shift operations (except left bit shift) are performed by the adder in the add cycle. In the add cycle, blocks 5-8, the operands are combined one octal character at a time. The two octal inputs to the adder are dependent upon the operation to be performed. The result is stored in the accumulator.

Blocks 12-14 represent the interrupt cycle. In the interrupt cycle, the regular program is stopped, the place where it is stopped is noted, and the analysis cycle is started on the interrupt program.

A simple diagram of the flow of data within the computer is illustrated in Figure 1.3. All data flow into or out of the computer must pass through the S register (distributor). This provides one input to the adder. The A register (accumulator) acts as a temporary storage for information until the computer is ready to transfer the information to memory. The B register (auxiliary accumulator) holds information during the execute cycle. This register provides the other input to the adder. The N register (command register) stores the operation code of the instruction. The L register (memory access register) stores the address of the information being processed by
FIGURE 1.2 COMPUTER CONTROL BLOCK DIAGRAM
FIGURE 1.3 COMPUTER DATA FLOW
the computer during each cycle; the address of the instruction during the fetch cycle and the address of the data during the execute cycle. The LA register (command counter) stores the address of the next sequential instruction. The AC and AD registers act together to form a 4 bit counter. The BC-BD registers also form a 4 bit counter. These counters are used to gate inputs to the adder and to the A register during an arithmetic or shift operation. The arithmetic unit is a three-bit binary adder. It is capable of receiving two octal characters and an input carry and producing the sum with carry.

At the present time, the computer has a complement of 13 commands as follows:

- Addition
- Subtraction
- Load Accumulator
- Store Accumulator
- Branch Unconditionally
- Branch on Negative
- Branch on Non-Zero and Decrement
- Ring Shift Accumulator
- Right Shift and Clear
- Left Shift and Clear
- Left Bit Shift
- Branch on Overflow
- Branch on Non-Zero

There are several unusual features in this computer. The voltage levels are very small. The zero logic level is zero volts; the one logic level is -2.33 volts. To obtain high speed switching at a low cost, the designers of the computer made use of the inherent inductance of wire-wound resistors. The energy stored in the inductance is utilized to overdrive transistors or to discharge rapidly stray or line capacitance. Thus, high switching speeds are obtained with relatively simple circuits.
1.2 Tape Drive

The tape drive utilized in this project is a 727 model II manufactured by International Business Machines. The 727 is no longer manufactured but is a standard tape drive on all vacuum tube IBM computers. It is designed to provide storage for large amounts of sequential information on magnetic tape. Power for the electronic circuits and drive motors is obtained externally, while power for the relay circuits is self-contained. The functions of the tape drive are writing, reading, backspacing, erasing, and rewinding. Information is stored on seven tracks across the tape. Each track is independent of the other tracks, and is associated with one read/write head. The tape is fed through the machine at a speed of 75 inches per second. The density of characters is controlled by write pulses generated by an external source. The 727 tape drive is capable of recording a maximum 200 characters per inch. Information may be placed on the tape in any code desired. The interpretation of the information is controlled by the external circuitry. The tape drive uses the "non-return-to-zero-inverted" (NRZI) system to record the binary information. With this system, tape is continuously saturated in either the positive or negative direction. Within any given period of time, a change in saturation direction is called a "one," and no change is called a "zero." Figure 1.4 represents data and signal flow within the tape drive.
FIGURE 1.4 TAPE DATA FLOW
CHAPTER 2
SYSTEM REQUIREMENTS

2.1 Computer

The computer is equipped with a peripheral interface adapter, PIA, which is designed to communicate with input/output equipment. The PIA contains two buffers, a slow speed unit and a high speed unit and associated control circuits. The high speed buffer can transmit and receive information simultaneously. It consists of two registers which store seven bits of information until the computer or external equipment is ready to accept them.

When the problem of communication with a tape drive external of the computer arose, two solutions were considered. The PIA could be used as a buffer unit or a separate unit could be built. An inspection of the PIA revealed two primary difficulties with using this method. Using the buffer of the PIA necessitates a computer program to assemble the 25-bit computer word, seven bits at a time. This would require more permanent storage in the computer than is desirable. In addition, the PIA is designed to allow interruption of the main program only when the buffer indicates that it has information to be read into the computer. No facility has been provided to allow the computer to ask for information. The problems involved in modification of the PIA circuitry to allow internal interruption led to the consideration of the alternate solution.
Upon closer inspection of the separate buffer solution, several advantages were found that were not evident in the initial inspection. By building a complete new unit, the design is limited only by the requirements of the two machines involved and by the operation requirements. Thus, the operations are not limited by the buffer; the buffer is limited by the operations. The information from the buffer can be gated directly into the S register and does not have to be assembled in the machine. The original computer design utilized two memories. The primary memory, magnetic core, is still used, but the secondary memory is not used. The buffer, therefore, can use the address and the S register input lines of the secondary memory. This buffer looks like the secondary memory to the computer.

2.2 Tape Drive

The tape drive requires an external unit to supply power and control signals. The power requirements of the tape drive are as follows: 208 volts AC at 6.0 amperes three-phase; 236 volts AC regulated; +270 volts DC at 100 milliamps; +140 volts DC at 1.5 amperes; -60 volts DC at .5 amperes; -130 volts DC at 100 milliamps; -270 volts DC at 100 milliamps; and +40 volts DC at 200 milliamps. The +40 volts is used only to operate a thermal light if the temperature within the unit becomes excessive. The nominal voltage levels for the tape drive are as follows: for control, -30 volts and +10 volts; for information, -14 volts for a "zero" and +10 volts for a "one."
The inputs and outputs of the tape drive are indicated in Figure 1. Tables I and II are brief descriptions of the function of each signal line.

2.3 Sequence of Operations

In order to understand how each signal is utilized, a description of the sequence of operations for input and output should be examined.

For an output (write) operation, the following operations should occur. The computer indicates that it has information for the tape drive to store. The tape starts moving forward. The read/write status trigger is set to write status and the Sel, Rea & Wrt signal is generated. A signal is generated when the information to be stored is present at the output lines of the computer. All 25 bits of the computer word are transferred to the output register. From the register information is presented to the tape drive on its input lines seven bits at a time, and write pulses are presented on the Wrt Pul line. These write pulses control the density of the information on the tape. The maximum density for the 727 is 200 bits per inch, which requires a 15 kilocycle write pulse rate. During the output operation the information being written on the tape appears on the Echo lines for a nominal period of 10 microseconds after the write pulse.

The sequence is continued until the computer indicates that no more information is to be stored. At this time the write pulses and the Go line are cut off, and a signal appears at the Wrt IOC line. In order for the tape to be compatible with IBM tape units, the
### TABLE I

**SIGNAL LINES TO TAPE DRIVE**

<table>
<thead>
<tr>
<th>Line</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Go</td>
<td>Go</td>
<td>Controls the start-stop motion of the tape.</td>
</tr>
<tr>
<td>Backward</td>
<td>Bwk</td>
<td>Controls the reverse-forward direction of tape motion.</td>
</tr>
<tr>
<td>Select</td>
<td>Sel</td>
<td>Determines which tape drive is selected in the case of multiple tape units (10 lines).</td>
</tr>
<tr>
<td>Start Rewind</td>
<td>Rew</td>
<td>Starts the rewind tape operation.</td>
</tr>
<tr>
<td>Turn off TI</td>
<td>Off TI</td>
<td>Turns off the tape indicator light which is located on the front panel of the tape drive.</td>
</tr>
<tr>
<td>Turn On TI</td>
<td>On TI</td>
<td>Turns on the tape indicator light.</td>
</tr>
<tr>
<td>Set Write Status</td>
<td>Wrt Status</td>
<td>Sets the read/write status trigger to write status.</td>
</tr>
<tr>
<td>Write Pulse</td>
<td>Wrt Pul</td>
<td>Carries pulses which control the density of the characters recorded.</td>
</tr>
<tr>
<td>Write Bus</td>
<td>Wrt</td>
<td>Carries the information to be stored (7 lines).</td>
</tr>
<tr>
<td>Write Check Character</td>
<td>Wrt LCC</td>
<td>Controls the writing of the longitudinal check character.</td>
</tr>
<tr>
<td>Set Read Status</td>
<td>Read Status</td>
<td>Sets the read/write status trigger to read status.</td>
</tr>
</tbody>
</table>
### TABLE II

**SIGNAL LINES FROM TAPE DRIVE**

<table>
<thead>
<tr>
<th>Line</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select and At Load Point</td>
<td>Sel &amp; LP</td>
<td>Indicates that the selected tape drive is at the load point.</td>
</tr>
<tr>
<td>Select and Rewind</td>
<td>Sel &amp; Rew</td>
<td>Indicates that the selected tape drive is rewinding.</td>
</tr>
<tr>
<td>Select and TI Off</td>
<td>Sel &amp; TI Off</td>
<td>Indicates that the tape indicator light on the selected tape drive is off.</td>
</tr>
<tr>
<td>Select and TI On</td>
<td>Sel &amp; TI On</td>
<td>Indicates that the indicator light is on.</td>
</tr>
<tr>
<td>Select, Ready and Write</td>
<td>Sel, Rea &amp; Wrt</td>
<td>Indicates that the selected tape drive is ready to begin writing.</td>
</tr>
<tr>
<td>Write Echo Bus</td>
<td>Echo</td>
<td>Carries a pulse when a bit of information is written on its corresponding track (7 lines).</td>
</tr>
<tr>
<td>Select, Ready and Read</td>
<td>Sel, Rea &amp; Read</td>
<td>Indicates that the selected tape drive is ready to begin reading.</td>
</tr>
<tr>
<td>Read Bus</td>
<td>Read</td>
<td>Carries the information that is being read out (7 lines).</td>
</tr>
</tbody>
</table>
longitudinal check character must occur 133 microseconds after the last line of information. When the tape stops moving, the output operation is complete. If, during an output (write) operation, the end of tape is sensed, the tape drive automatically turns on the TI and generates a TI On signal.

For an input (read) operation, the following operations should occur. The computer indicates that it requires information from the tape drive. The tape starts moving forward, and the read/write status trigger is set to read. The Sel, Rea & Read signal is generated. Data are presented to the Read bus at discrete intervals, seven bits at a time. A signal is generated when the 25-bit computer word is presented to the input lines of the computer.

When the information requested has been read from the tape drive, the longitudinal check character is presented to the Read bus. At the end of an input sequence, the Go signal must be cut off. This completes an input operation.

In the above discussions it should be noted that the computer is much faster than the tape drive; therefore, it is assumed that the computer is ready to receive or transmit information when the tape drive requires it to do so.

Two other operations may be initiated by the computer, backspace and rewind. The computer indicates a rewind operation to the buffer which signals the tape drive on the Rew line. This sets the read/write status trigger to read. When the rewind has been completed, the Sel & Rew signal is cut off and the Sel & LP signal is generated.
The backspace operation can be initiated only by an instruction from the computer. When backspacing, the Bwk line and the Go line are cut on. Whenever the Bwk line is cut off, the tape will move forward if the Go line is on.
CHAPTER 3
LOGIC DESIGN

The circuits of the buffer unit are organized into function control, tape control, read, and write circuits (Figure 3.1). The function control circuits decode control information that is received from the computer. This information includes the select information and operation information. The tape control circuits control the operation of the tape unit. The read and write circuits provide independent read and write channels to accommodate simultaneous read and write operations when more than one tape drive is used. (At the present time only one tape drive is available. Additional tape control circuits would be needed to control more than one tape drive.) The read and write circuits utilize information from the function control circuits to direct the read and write operations.

Each main circuit group is composed of a number of smaller circuits, each of which has a specific function in a given tape operation. The following discussions present the overall function of each main group and then describe the individual circuits and the role each plays in accomplishing group functions. Figure 3.2 illustrates the logic symbols utilized in the succeeding figures.

3.1 Function Control Circuits

The function circuits receive the instruction from the computer and decode it to direct the operations of the buffer unit. There are
FIGURE 3.1 BUFFER UNIT BLOCK DIAGRAM
Inverter

Flip-Flop

"And" Gate

"Or" Gate

Delay

Single-Shot

*Note:  
\( T = \text{delay time} \)

*Note:  
\( T = \text{timing} \)

FIGURE 3.2 LOGIC SYMBOLS
two decode circuits contained in the function circuit. The select decode circuit is illustrated in Figure 3.3. This circuit decodes instruction bits six, seven, and eight to determine which tape drive the computer has selected. The operation decode circuit, Figure 3.4, decodes instruction bits zero, one, two, three, and four, to determine the operation that the tape drive is to perform (see Table III).

3.2 Tape Control Circuits

The tape unit control circuits, Figure 3.5, control the direction and motion of the tape in accordance with commands from the operation decode circuits. A separate tape control unit is required for each tape drive. A backspace instruction from the computer sets the backspace tape motion flip-flop and the tape direction flip-flop. The "true" output of the tape motion flip-flop forms the Go signal for the tape drive. The "true" output of the tape direction flip-flop forms the Backward signal for the tape drive. Four milliseconds later, after the tape has reached operating speed, the backspace read status flip-flop is set. This forms the Set Read Status signal for the tape drive. After one millisecond, the Read Sprocket signal is gated into a 266 microsecond retrigergerable delay. The delay of one millisecond is to allow the longitudinal check character to be passed over without affecting the read sprocket generator. The read sprocket generator, Figure 3.6, simply indicates when a line of information is read. The retrigergerable delay is released 266 microseconds after the last line of information in the record is read. This activates a ¼ millisecond
All lines are gated with the Tape Address signal.

FIGURE 3.3 SELECT DECODE CIRCUIT

FIGURE 3.4 OPERATION DECODE CIRCUIT
<table>
<thead>
<tr>
<th>Octal Instruction (first 10 bits)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ln01</td>
<td>Search tape n</td>
</tr>
<tr>
<td>ln03</td>
<td>Read tape n</td>
</tr>
<tr>
<td>ln02</td>
<td>Write tape n</td>
</tr>
<tr>
<td>ln06</td>
<td>Backspace tape n</td>
</tr>
<tr>
<td>ln04</td>
<td>Rewind tape n</td>
</tr>
</tbody>
</table>
FIGURE 3.5 TAPE CONTROL CIRCUITS
FIGURE 3.6 READ SPROCKET
delay which allows the read head to be positioned between records before the tape is stopped. After the 4 millisecond delay, the tape motion flip-flop and the tape direction flip-flop are reset. Two hundred milliseconds after the tape motion flip-flop is reset, the read status flip-flop is reset. At this time the tape is stopped, and the read head is spaced approximately in the middle of the inter-record gap. This completes the backspace operation.

Rewind may be initiated in two ways. A rewind instruction from the computer combined with the signal indicating that the tape drive is not rewinding will start the rewind operation. This operation may also be started automatically when the following conditions occur; the tape drive is not rewinding, the tape indicator is on, and the Go signal is off. The Rewind signal, which is generated automatically, is delayed 200 milliseconds to allow the tape to settle in the vacuum columns before accepting a signal to change direction.

The tape indicator may be turned on by a "one" in track number seven when the tape drive is reading. It may be turned off by the Select and at Load Point signal from the tape drive. The tape indicator is used to indicate an end-of-tape condition. In addition, the tape control unit stores the address of the tape drive which was previously used or which is currently being used.

3.3 Write Circuits

The function of the write circuits is to accept 25-bit computer words and control the transfer of this data to the write circuits of the tape drive. The write operation is initiated by a computer
instruction. Figure 3.7 illustrates the individual write circuits and their relation to each other.

**Output register.** The output register consists of 25 flip-flops to store the 25-bit computer word. Only the "true" inputs are used to transfer information into the register, and these inputs are gated with a transfer data signal from the write control circuit. The flip-flops are reset prior to the transfer of a word into the register.

**Disassembly circuits.** The disassembly circuits, Figure 3.8, consist of a disassembly matrix and a write register. The disassembly matrix sequentially extracts each 5-bit character from the output register and presents it to the write register inputs. This extraction is controlled by the disassembly counter. The lowest-order character in the output register is extracted first, the next lowest-order second, etc. The write register consists of five flip-flops which hold each line of data as it is being recorded on the tape. The inputs to the write register are gated with a transfer data signal from the write control circuit. The write register is cleared prior to the transfer of data into the register.

**Disassembly Counter.** The disassembly counter is a standard modulo 5 counter (Figure 3.9). The counter controls the disassembly of 25-bit computer words into five 5-bit characters. The output of the counter is interrogated at the end of a write operation to determine if the number of lines recorded was an integral multiple of five. The counter is operated by pulses from the write control circuits. It is reset to zero at the start of a write sequence by a signal from the write control circuits.
FIGURE 3.7 WRITE CIRCUIT BLOCK DIAGRAM
FIGURE 3.8 DISASSEMBLY CIRCUITS
FIGURE 3.9  MODULO 5 COUNTER
Parity generator. Each line recorded on the tape is composed of a 5-bit character, a parity bit, and an end-of-tape bit for a total of seven bits. The parity generator, Figure 3.10, makes the total number of "one" bits in a line odd for compatibility with the IBM format. The parity bit is stored in the parity flip-flop and then written in track six on the tape.

Write parity check. The write parity check, Figure 3.11, determines if a parity error has occurred during a write operation. This check is performed on the Write Echo signals from the computer. If an error occurs, the write parity error flip-flop is set. The write parity check is performed on every line that is written except the longitudinal check character.

Write control. The write control circuits contain two separate circuits: the write tape motion circuit, Figure 3.12, and the write time sequence circuit, Figure 3.13.

The write tape motion circuit is activated by a write instruction from the computer. If the selected tape unit is at the load point, a 200 millisecond delay occurs before the tape motion flip-flop is set to start the tape moving; if the tape is not at the load point, the flip-flop is set immediately. The 200 millisecond delay allows time for the tape to stabilize in the vacuum columns when a rewind operation is completed immediately preceding a write selection. The setting of the tape motion flip-flop in turn sets the write status flip-flop after a short delay. This delay is 80 milliseconds if the selected tape drive is at the load point and 4 milliseconds if it is not at the load point. When the tape drive is at the load point,
FIGURE 3.10  PARITY GENERATE CIRCUITS
FIGURE 3.11 WRITE PARITY CHECK CIRCUITS
FIGURE 3.12 WRITE TAPE MOTION CIRCUITS
FIGURE 3.13  WRITE TIMING SEQUENCE CIRCUIT
the 80 milliseconds delay allows the reflective spot on the tape to move past the write head before writing begins. Approximately six inches of tape must pass the write heads before writing begins to provide compatibility with IBM equipment (see Figure A.3 for tape format). The 4 milliseconds delay allows time for the tape to reach operating speed before writing begins and fixes the length of the inter-record gap. The output of the write status flip-flop is used as the Set Write Status signal for the tape drive and as the starting signal for the write timing sequence.

The end of a write operation is detected by an end write single shot. This single shot is triggered each time a word is ready to be transferred to the buffer unit. If no word is to be transferred, the write pulses are not gated to the tape drive, and the retriggerable delay is not triggered. After a 266 microsecond delay, the longitudinal check character is written; and after an additional 4 milliseconds, the tape motion flip-flop is reset. After an additional 200 milliseconds, the write status flip-flop is reset and the disassembly counter is checked for a length error. This completes the write operation.

The write timing sequence circuits control all the write operations. The output register is cleared initially when the write status flip-flop is set. The write status "true" starts a 15 kilo-cycle clock. The pulses out of the clock are gated with the End Write signal to perform several functions. The write register is cleared, and data are transferred to the output register if the disassembly counter is zero. After a 22 microsecond delay, five bits of the word are transferred to the write register. If the disassembly counter is zero, the Output Data Received signal is generated. After another 22
microsecond delay, the write circuits are pulsed, the write parity is checked, and the disassembly counter is pulsed. After a 10 microsecond delay and if the counter is zero, the output register is cleared. The sequence keeps repeating until the End Write signal is cut off.

3.4 Read Circuits

The function of the read circuits is to assemble information from the tape into 25-bit computer words and to control transfer of these words to the computer. This function is involved in two operations: the search operation and the read operation. These operations are initiated by computer instructions. Figure 3.14 illustrates the individual read circuits and their relation to each other.

Input register. The input register consists of 25 flip-flops to store the assembled computer word. Only the "true" bits are used to transfer information into or out of the register. The "true" outputs of the register are gated with a transfer data signal for input to the computer. The flip-flops are reset prior to the transfer of the first 5-bits of information into the register.

Assembly circuits. The assembly circuits, Figure 3.15, consist of an assembly matrix and a read register. The assembly matrix sequentially inserts each 5-bit character into the input register from the gated outputs of the read register. The outputs of the read register are gated with a transfer data signal. The assembly is controlled by the assembly counter. The lowest-order character is inserted first, the next lowest-order second, etc. The read register consists of five
FIGURE 3.14 READ CIRCUIT BLOCK DIAGRAM
FIGURE 3.15 ASSEMBLY CIRCUITS
flip-flops which receive each line of information from the tape drive during a read or search operation. The outputs from the tape drive are gated with a transfer data signal to form the inputs to the read register. The read register flip-flops are cleared prior to any transfer of information into the register.

Assembly counter. The assembly counter is constructed identically to the disassembly counter. It controls the assembly of five 5-bit characters into 25-bit computer words. The output of the counter is interrogated at the end of a read operation to determine if the number of lines read was an integral multiple of five. The counter is operated by pulses from the read control. It is reset to zero at the start of a read or search operation by a signal from the read control circuits.

Read sprocket. The read sprocket, Figure 3.6, generates a signal whenever a line of information is read by the tape drive. Since the total number of "one" bits in any given line must be odd, the simple "or" circuit generates a signal whenever a line of information appears at its inputs. The read sprocket is used to signal the end of a record.

Read parity check. The read parity check circuit, Figure 3.16, consists of two flip-flops and logic to determine whether the total number of "one" bits in any line is odd or even. The two flip-flops are necessary to store the information from tracks six and seven. If the parity checks even, a read parity error flip-flop is set. The read parity check is performed on every line that is read except the longitudinal check character.
FIGURE 3.16 READ PARITY CHECK CIRCUITS
**Longitudinal check circuits.** The longitudinal check circuits, Figure 3.17, consist of seven modulo 2 counters. Each "one" bit read triggers the counter associated with the track in which the "one" bit appeared. At the end of a read operation, the outputs of the counters are interrogated. If a "one" appears from any counter, a longitudinal check error flip-flop is set. The counters are cleared after each record.

**Read control.** The read control circuits contain two separate circuits; the read tape motion circuit, Figure 3.18, and the read time sequence circuit, Figure 3.19.

The read tape motion circuit is activated by either a read instruction or a search instruction from the computer. The operation flip-flop is set simultaneously to determine which operation is selected. If the selected tape drive is at the load point, a 200 millisecond delay is taken before the tape motion flip-flop is set to start the tape moving; if the tape is not at the load point, the flip-flop is set immediately. The 200 millisecond delay allows time for the tape to stabilize in the vacuum columns when a rewind operation is completed immediately preceding a read or search operation. The setting of the tape motion flip-flop, in turn, sets the read status flip-flop and the gate read flip-flop after a short delay. This delay is 60 milliseconds if it is not at the load point. The 60 millisecond delay allows the reflective spot on the tape to move past the read heads before reading begins. The 2 millisecond delay allows time for the tape to reach operating speed. The output of the read status flip-flop is used to set the read/write status trigger of the tape drive
FIGURE 3.17 LONGITUDINAL CHECK CIRCUITS
FIGURE 3.18 READ TAPE MOTION CIRCUITS
FIGURE 3.19 READ TIMING SEQUENCE CIRCUIT
to read and to reset the read register and the longitudinal check circuits. The output of the gate read flip-flop is used to gate information to the computer. This completes the initiation of the read operation.

If a search operation is initiated, additional operations occur. The first Read Sprocket signal starts a 300 microsecond delay. After this delay the gate read flip-flop is reset. This allows only the first computer word in any record to be read into the computer. The remaining information in the record is blocked from the computer. At the end of the record being searched, the gate read flip-flop is again set to allow the reading of the first computer word in the next record to be read into the computer. The longitudinal check is also reset at this time. This sequence continues until the computer instructs the buffer unit to start a read operation.

During a read operation, if no information is detected for 160 microseconds, the buffer starts a series of operations to halt the tape. The gate read flip-flop is reset to prevent any more information to be read into the computer. After 106 microseconds, the longitudinal check character is read into the longitudinal check circuits. Four milliseconds later, the read tape motion flip-flop is reset. After an additional 200 milliseconds, the read status flip-flop is reset and the length and longitudinal check are interrogated. This completes the read operation.

The read timing sequence circuits control all of the read operations. The presence of a signal from the read sprocket initiates
the timing sequence. This signal triggers a 26 microsecond single shot to be read information into the read register. The 26 microseconds allows for the possibility that the line of information is not parallel to the read head, and, therefore, each bit of information would not arrive at the read heads at the same time. If the assembly counter is zero, the input register is cleared. After 35 microsecond delay, the data are transferred to the input register and the read parity is checked. After an additional 15 microsecond delay, the read register is cleared and the assembly counter is advanced. When the assembly counter is reset to zero and the gate read flip-flop is set, a 10 microsecond single shot is triggered to transfer the information from the input register to the computer. The sequence continues until the end of record when the Read Sprocket signal disappears.

3.5 Cost Estimate

One of the bases for evaluating the quality of a design is cost of construction. Since this design is only a logic design, an actual construction cost cannot be calculated. However, a general estimate of cost can be made. This estimate is based on the use of S-PAC digital logic modules which were chosen because they have been successfully used in other equipment constructed at the University of Arizona.

The total number of each logic circuit used in the design is as follows: 147 inverters, 206 gates, 88 flip-flops, 2 single shots, 27 delays, and 1 clock. All of the gates were counted together because the design uses non-inverting gates and the modules are inverting gates. The price of these gates was used to obtain a cost estimate.
Using the following modules as a price base, the total cost amounted to $5,100.00: PA-20 for inverters, DN-20 for gates, FF-20 for flip-flops, DM-20 for single shots, DS-20 for delays, and MV-30 for clock. This total cost includes a 20 ampere power supply for the modules but does not include the level changing circuits which must be designed to be compatible with this system. This estimate does not include the cost of labor which cannot be determined.

3.6 Conclusion

This completes the system design which is based on the logic required to accomplish the task to be done. The actual system can be constructed primarily of commercial equipment. This enables the system to provide a communication channel between the tape drive and digital computer at a moderate cost.
APPENDIX

Figures A.1 and A.2 illustrate the program suggested for inputting and outputting information to and from the computer. The programs are based on two restrictions. First, the number of words in a record is fixed at 128. Secondly, the information to be transferred must occupy the addresses 000 through 128, inclusive. Should these two restrictions be inconvenient, the programs may easily be changed.

A.1 Output Program

The computer loads the accumulator with information from the address specified by the word in the XYZ address. The computer then stores the word on tape. The accumulator is then loaded with the word in address XYZ and one is subtracted from that word. If the result is not zero, the routine is repeated. If the result is zero, the routine is complete and the computer begins the next program.

A.2 Input Program

The accumulator is loaded with the tag word of the requested information. The first computer word in a record, the tag word, is subtracted from the accumulator. If the result is not zero, the routine is repeated, using the first computer word of the next record. If the result is zero, the accumulator is loaded with the next computer word in the record. This word is stored in the address specified by the word in address WXW. The accumulator is loaded with the word in
Information to be transferred is in addresses 0-128 inclusive.

**FIGURE A.1 OUTPUT PROGRAM**

```
BRU XYZ

LDA XYZ

STA 514

LDA XYZ

SUB XYZ

BRU XYS

Yes

BRU XXX

No

STA XYZ

514 - write Tape Add (decimal) #0
xyz - Tally Add
xyw - Constant "1"
xxxx 
xyt 
Instruction Add 
xyz
```
FIGURE A.2  INPUT PROGRAM

BRU WXW

LDA 128

SUB 513

Yes

BRN WXW

No

LDA 515

STA WXW

indirect

BRU WX5

STA WXW

Yes

LDA WXW

SUB WXW

BRN WXT

No

BRU WXR

513 - Search tape Add (Decimal) ≠ 0
515 - Read tape Add (Decimal) ≠ 0
WXW - Tally address
128 - Tag word
WXX - Constant "1"
WXY

WXT

WX5

WXR

Instruction Addresses
WXW and one is subtracted from it. If the result is not zero, it is stored in address WXW and the routing returns to load the next computer word into the computer. If the result is zero, the routine is complete and the computer begins the next program.

A.3 Tape Format

Figure A.3 illustrates the format of the data recorded on the tape in order to be compatible with IBM equipment.
Notes:
1. Oxide Side Up
2. Write freq. 15 KC ± 1%
3. Average Steady State Tape Speed - 75 ips ± 1%

FIGURE A.3 TAPE FORMAT
REFERENCES


3. ________, Instruction manual for the 1607 tape system, Control Data Corporation, Minneapolis, Minnesota; 1961.