A SIMPLIFIED HYBRID DIFFERENTIAL ANALYZER

by

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ABSTRACT

In a hybrid-code differential analyzer system, variables and parameters are represented by the combination of a coarse n-bit number and a continuously variable analog interpolation voltage. The hybrid-code system combines analog elements accurate to within p per cent of half-scale with the n-bit digital system to form an overall system with greatly improved accuracy within $(p/2^n)$ per cent of half-scale. This paper describes a hybrid-code system employing a 5-bit-plus-sign number and an analog channel accurate to within one per cent of analog half-scale. Results of the sine-loop test verify that the predicted theoretical performance is achieved in practice. Further experiments study the performance of the hybrid-code system with a passive RC integrator replacing the active integrator in the analog channel of the hybrid-code integrator. Results of the sine-loop test indicate that sufficient accuracy for practical applications cannot be achieved with a realizable passive RC integrator.

INTRODUCTION

Considerable interest is being shown in the development of hybrid and combined differential analyzers which capitalize on the best features of both analog and digital computing elements. Hybrid systems often provide an analog computer with digital storage and decision-making capability. Combined systems utilize a digital computer for operations such as coordinate transformations, precision function generation, and data storage, which are best suited to digital techniques, and analog elements for operations such as addition and integration, where higher speed and less accuracy are permissible.

This paper treats a differential analyzer employing hybrid-code representation of variables; that is, each variable or parameter is represented by a combination of a coarse n-bit word and a continuously variable analog interpolation voltage. Accuracy depends on the number of bits used and on the analog-element accuracy. The system described employs a 5-bit word.

The experiments described here study two aspects of hybrid-code computing. First, they verify that hybrid-code techniques provide a method for combining a digital system with n bits and an analog system accurate within only p per cent of half-scale to obtain an overall hybrid-code system

with greatly improved accuracy of $(p/2^n)$ per cent of half-scale. While such verification has been obtained for a system with n = 3, a more practical system requires five or more bits. This study provides a convincing verification of hybrid-code accuracy.

Second, it was suggested by previous investigators[1, 2] that if the number of bits is increased, a relatively accurate hybrid system can be maintained with simple passive elements replacing operational amplifiers in the analog channel. A system with 5 bits permits a comparison of results obtained using a passive RC integrator and those obtained using an active integrator. The passive-integrator tests determine how well accuracy can be maintained when the active analog integrator is replaced by a realizable RC integrator.

Earlier work in the area of hybrid-code systems has been carried out by H. Skramstad, H. Schmid, J. Wait, and others.[1-8] Wait's prototype system, based on a modification of Skramstad's original proposal, was the first complete operational unit. It employed a 3-bit word and an analog channel with nominal accuracy of 1 per cent of half-scale to achieve over-all hybrid-code accuracy within 0.125 per cent of half-scale.

HYBRID-CODE THEORY[1-5]

General Theory: In a hybrid-code system a variable X is represented in the form

$$X = X_D + X_A$$

where X_D is an n-bit-plus-sign number, and X_A is a continuously variable analog interpolation voltage between -E and +E volts. Either one bit or E volts represents one machine unit (m.u.). The variable X can be considered as a binary number, in which X_D contains the n most significant bits, and X_A represents the remaining less significant bits. In the computer to be described, X_D is a 5-bit plus sign number, and E equals 10 volts. Digital parts of variables are represented in a 2's complement code. The hybrid-code representation is illustrated in Fig. 1.

The independent variable, t, is divided into a sequence of COMPUTE and HOLD periods as illustrated in Fig. 2. Each COMPUTE period is T seconds long; each HOLD period is T_H seconds. During COMPUTE periods the digital part of each variable is held constant, and computation is performed by analog elements such as integrators and D/A multipliers. At the end of each COMPUTE period, the analog part of each variable is monitored. If its magnitude exceeds 1/2 m.u. (5 volts), a $\pm$ 1 m.u. increment (carry) is added to the digital part of the variable and subtracted

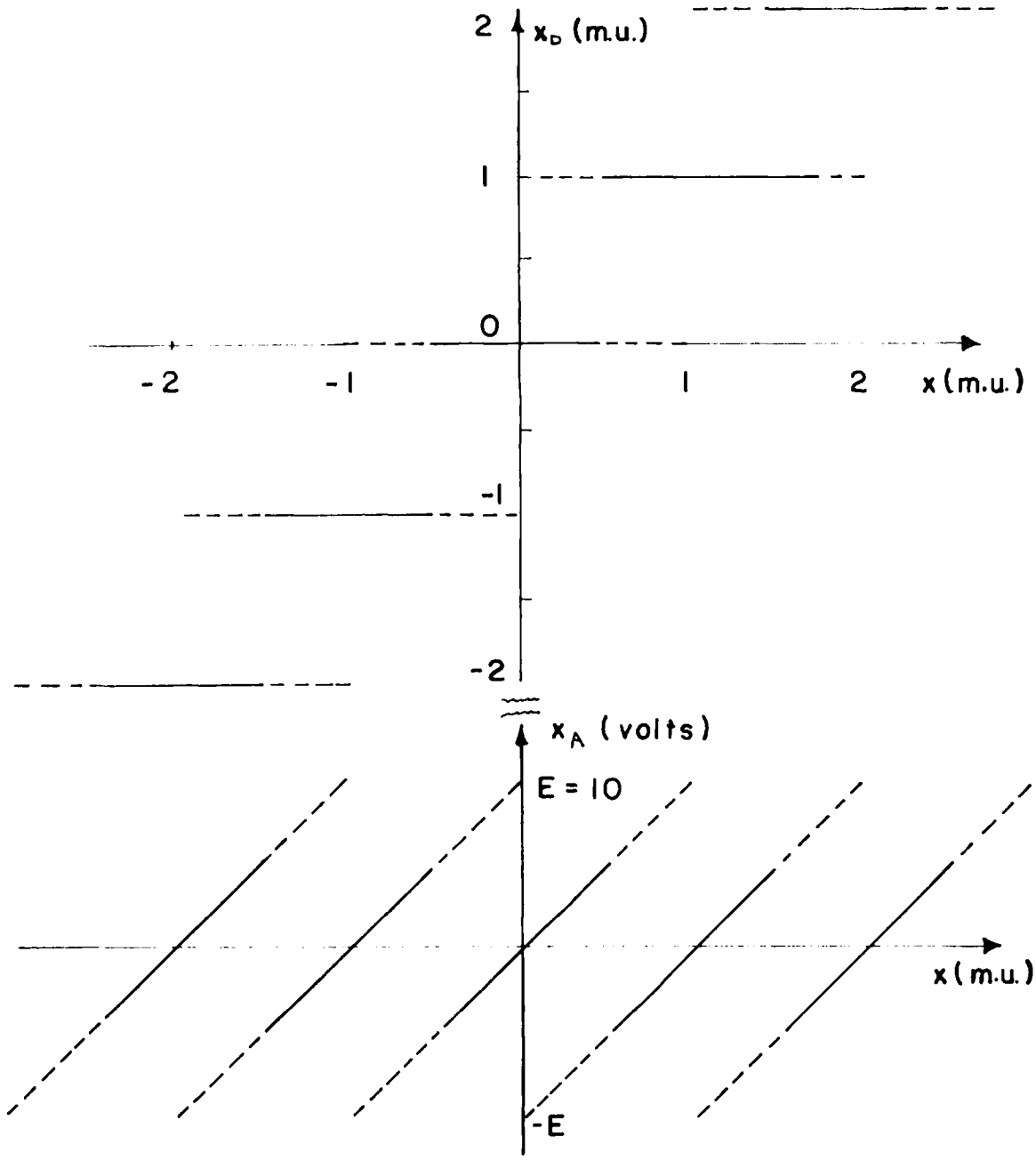
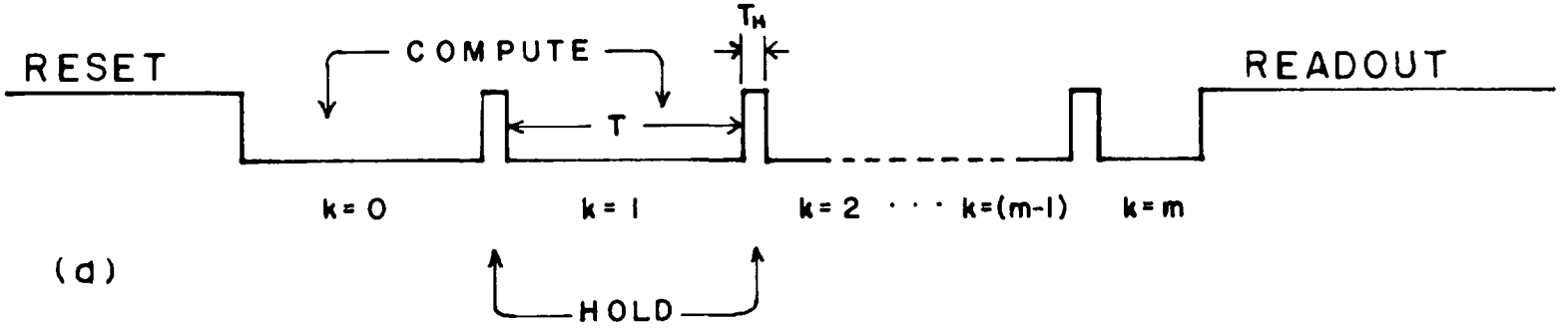


Fig. 1 Hybrid-code representation of variables

The value of the variable X (for $|X| < 3$ m.u.) is given by the sum, $X = X_D + X_A$, of the variables shown above. Note that there are two equivalent representations of each value of X. For example, X = 1.6 m.u. is given by the sum of X_D = 1 m.u. and X_A = 6.0 volts or by the sum of X_D = 2 m.u. and X_A = -4.0 volts. In the system described the range of X is given by $|X| < 32$ m.u.



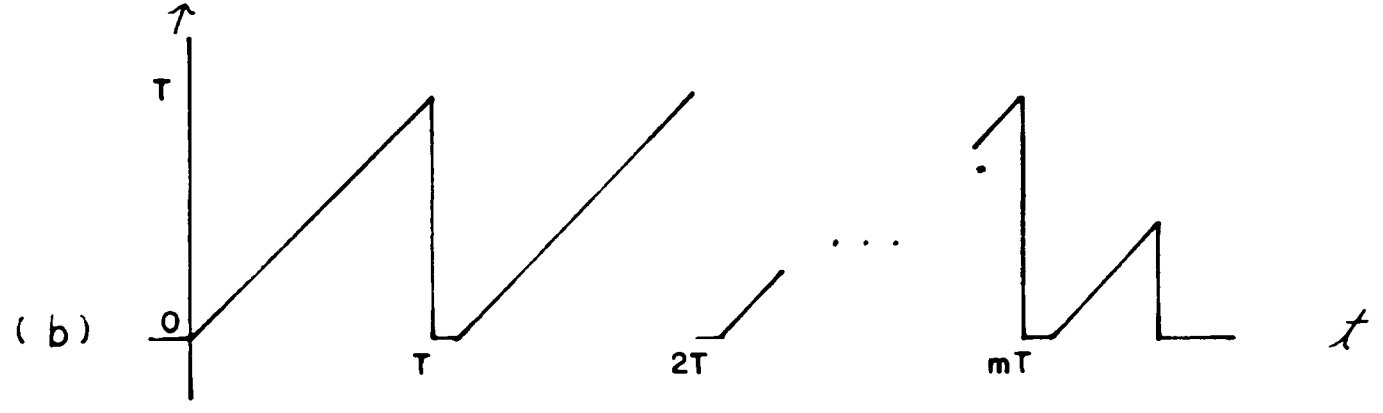


Fig. 2 (a) Modes of the system during a computation (computing run), and (b) representation of the independent variable, t

In the RESET state, initial conditions are applied to integrators. During each COMPUTE period analog computation is performed. During each HOLD period digital updating is performed. The READOUT state occurs after a preset number ($m + \tau/T$) of COMPUTE-HOLD periods. At this time, the value of the readout variable is held and displayed. Note that $T \gg T_H$.

from the analog part during the ensuing HOLD period. Note that analog computation is performed during COMPUTE periods, and digital computation, which takes the form of updating digital registers, is performed during HOLD periods.

The computer has two additional states (modes), RESET and READ OUT. In the RESET mode, variables are set to zero; then initial conditions are applied to integrators. READ OUT occurs after a preset number of COMPUTE-HOLD periods; at that time the digital and analog parts of a selected variable are displayed by a read out system.

Variables are subject to the following scaling restrictions:

$$\left|\dot{X}\right| , \ |X| < 2^n \text{ m.u.} \tag{1}$$

$$\left|\frac{d\dot{X}}{dt}\right| , \ \left|\frac{dX}{dt}\right| \leqslant (\tfrac{1}{2}/T) \text{ m.u. sec.}^{-1} \tag{2}$$

The first restriction insures that digital registers do not overflow; the second restriction insures that the digital part of each variable can change by only 1 m.u. after any COMPUTE period and that the magnitude of the analog part of each variable remains less than E volts. This permits a simple form of ternary data transfer.

These restrictions determine the hybrid bandwidth. Assuming a full-scale sine wave,

$$X = 2^n \sin(2\pi B_H t)$$

Then,

$$\dot{X} = 2^n(2\pi B_H) \cos(2\pi B_H t)$$

Also,

$$\dot{X} \leq (\tfrac{1}{2}/T) \text{ m.u. sec.}^{-1}$$

Thus,

$$B_H = \frac{1}{4\pi 2^n T}$$

We call B_H the full-scale bandwidth of the hybrid-code system. Since the analog channel accepts the full rate of change, $(\frac{1}{2}/T)$ m.u. sec.$^{-1}$, the analog elements must have a bandwidth, B_A, such that

$$B_A \geq 2^n B_H = \frac{1}{4\pi T} \tag{3}$$

In calculating B_H, the HOLD periods have been neglected: the actual bandwidth is $B_H \left(1 - \frac{T_H}{T + T_H}\right)$ which is about 2.4 cycles per second for this system.

In general, if the analog part of a variable is accurate within p per cent of analog half-scale (1 m.u.), the hybrid-code variable is accurate to $\frac{p}{2^n}$ per cent of hybrid half-scale (2^n m.u.). In effect, the use of hybrid-code techniques increases analog accuracy by a factor 2^n. In terms of a straight digital solution, the use of analog interpolation eliminates truncation and round-off errors due to quantized variables.

Integration Principles: Hybrid-code techniques can be illustrated by a specific example, the hybrid integrator. The following notation is used:

In general	During the k^{th} COMPUTE period
$X = X_D + X_A$	$X_D = {}^kX_D$
$\dot{X} = \dot{X}_D + \dot{X}_A$	$\dot{X}_D = {}^k\dot{X}_D$
$X_O = X_{DO} + X_{AO}$	$t = kT + \tau$

A hybrid integrator with gain a performs the operation

$$X(mT + \tau) = {}^mX_D + X_A(mT + \tau) = a\int_0^{mT+\tau} \dot{X}\, dt + X_O$$

where it is assumed that $|\dot{X}|$ and $|X|$ meet the scaling requirements of equation (1). Maximum gain is determined by the scaling restrictions. The change in X during a single COMPUTE period, ΔX, is

$$\Delta X = a\int_{kT}^{kT+T} \dot{X}\, dt \leq a\,|\dot{X}|_{max}\, T$$

To satisfy equation (1),

$$\Delta X \leq a\, T\, 2^n$$

To satisfy equation (2),

$$\Delta X \leq \tfrac{1}{2} \text{ m.u. in T seconds}$$

Thus,

$$a\, T\, 2^n \leq \tfrac{1}{2}$$

And,

$$a \leq \frac{1}{2^{n+1}T} \tag{4}$$

The system described uses the maximum gain, 15.625.

Consider integration for a period $(mT + \tau)$ as illustrated in Fig. 3. We may write:

$$X(mT+\tau) = X_{DO} + a\int_0^{mT+\tau} X_D\, dt + a\int_0^{mT+\tau} X_A\, dt + X_{AO}$$

$$= \left[X_{DO} + aT \sum_{k=1}^{m-1} k\dot{X}_D\right] + \left[a m\dot{X}_D\tau + a\int_0^{mT+\tau} X_A\, dt + X_{AO}\right] \tag{5}$$

To use hybrid-code techniques, we note that if $aT = (\frac{1}{2})^i$, the first bracketed expression in (5) is a binary number (X_D) for integral values of $\underline{i}$ and can be generated and stored with digital precision. The second bracketed expression can be represented by an analog voltage (X_A). Fig. 4 illustrates a hybrid integrator generating the expression (5). Its digital channel includes the n-bit plus sign input $(\dot{X})$ register, the (n + 2)-bit plus sign R register, and two D/A multipliers. The analog channel includes an analog integrator, the summing amplifier, and the analog initial-condition circuit. Note that the digital part of the hybrid integrator output is accumulated by the input register of the following computing element(s). During a computer run, the integrator performs the following operations in generating expression (5):

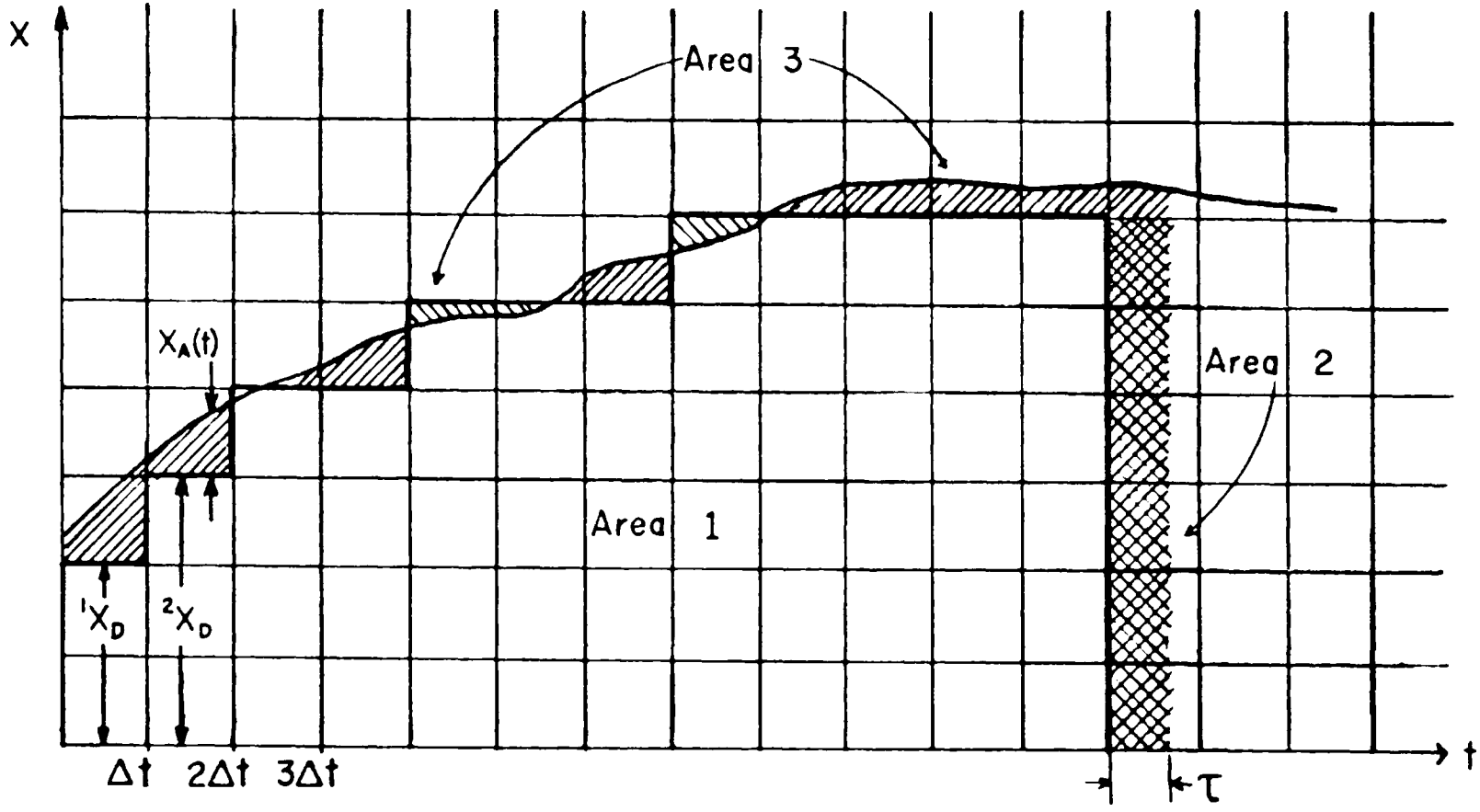


Fig. 3 Graphical representation of hybrid-code integration (from Wait, Ref. 3)

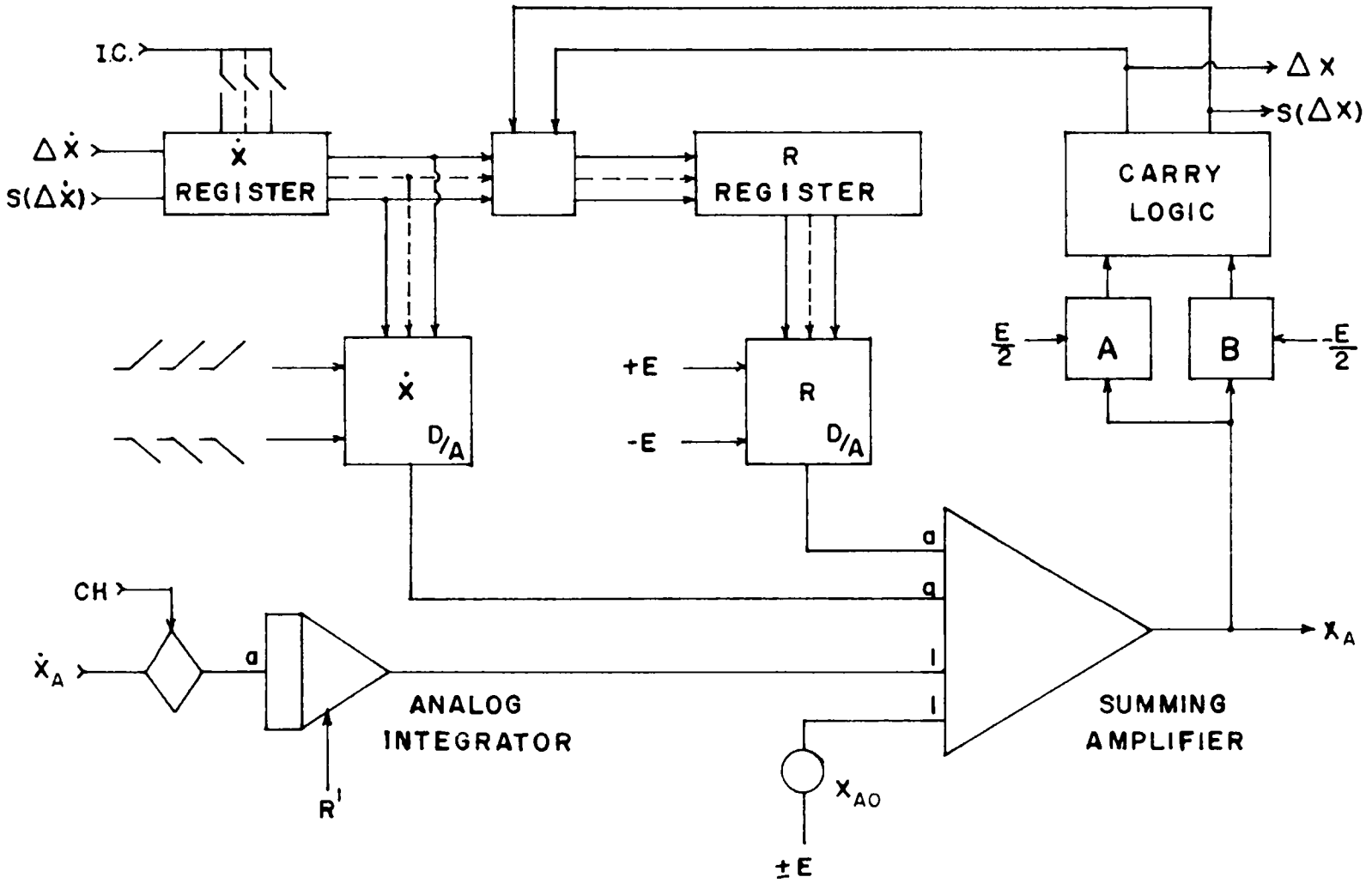


Fig. 4 Hybrid-code integrator

1. At the start of the RESET period digital registers are reset and the analog integrator capacitor is discharged. Then $\dot{X}_{DO}$ and X_{DO} are applied to the $\dot{X}$ and X registers.
2. During a computing run increments in $\dot{X}_D$ are received from the preceding element(s) and accumulated in the $\dot{X}_D$ register.
3. The quantity $R = aT \sum_{k=1}^{m-1} {}^{k}\dot{X}_D - N$, where N is the sum of the output carries generated in operation 8, is accumulated in the R register. The number ${}^{k}\dot{X}_D$ is added to the lower order bits at the start of each HOLD period to form the term $aT \sum_{k=1}^{m-1} {}^{k}\dot{X}_D$.
4. During COMPUTE periods the R D/A multiplier converts the quantity R to a d-c voltage that is a component of X_A.
5. The term $a{}^{k}\dot{X}_D\tau$ is obtained from a D/A multiplier with output proportional to a linear interpolation voltage (Area 2 of Fig. 3).
6. The term $\int_0^{mT+\tau} \dot{X}_A dt$ is the output of the analog integrator (Area 3 of Fig. 3).
7. X_{AO} is the analog part of the initial condition.
8. The terms obtained in operations (4) to (7) are summed to form X_A. Comparators A and B monitor X_A at the end of each COMPUTE period. If $X_A \geq 5$ volts, a CARRY is generated adding 1 m.u. to X_D and subtracting 1 m.u. from X_A. Subtraction from X_A is

accomplished by subtracting 1 m.u. from the R register. If $X_A \leq -5$ volts, 1 m.u. is subtracted from X_D and added to X_A.

AN IMPROVED HYBRID-CODE DIFFERENTIAL ANALYZER

The system used in performing tests is an improved version of that described in Ref. 2. It employs a 5-bit-plus-sign word and an analog channel with nominal accuracy of 1 per cent. To study errors occuring in a sine loop two integrators and an inverter are necessary to implement $\frac{d^2X}{dt^2} = -\omega^2 X$. In addition, a master control clock and read-out system are required to provide accurate timing of operations and readout of variables.

Digital information is stored in two's complement form. The scaling restrictions mentioned earlier insure that each variable changes by either 0 or $\pm$ 1 m.u. during each HOLD period. This permits a simple ternary form of digital information transfer between elements: a pulse on the (ΔX) line indicates that there is an increment, and the dc level on the S line gives its polarity.

Integrator description: Referring to Fig. 4, each integrator includes an input ($\dot{X}$) register, an R register, two D/A multipliers, an analog integrator, a summing amplifier, and two comparators. The input register is a 5-bit-plus-sign reversible counter which receives S and ($\Delta \dot{X}$) signals from previous elements. The $\dot{X}_D$ initial condition is set with toggle switches on the front panel and is applied to the $\dot{X}$ register during the RESET period. The R register is

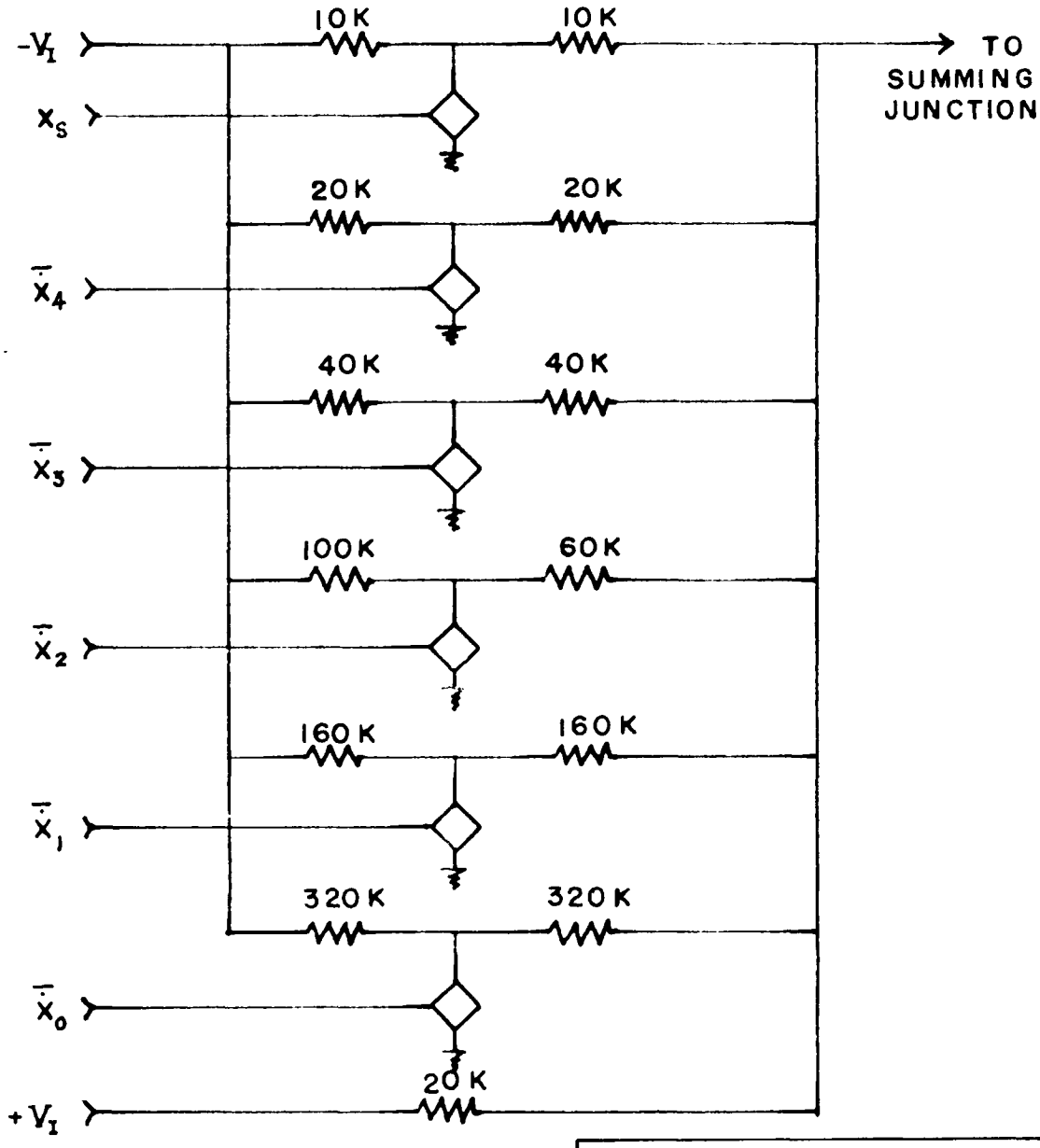
a 7-bit-plus-sign register. During each HOLD period the magnitude $^{k}\dot{X}_{D}$ in the $\dot{X}$ register is added to the five least significant bits of the R register, and the two most significant bits are determined by the sign of $^{k}\dot{X}_{D}$, the presence of a carry from the fifth bit, and the presence of a carry at the integrator's output.

The D/A multipliers convert $^{k}\dot{X}_{D}$ and R_{D} to analog signals during COMPUTE periods. The six bit $\dot{X}$ D/A multiplier is shown in Fig. 5; the eight bit R multiplier is similar. This type of unit is discussed in Ref. 9; its accuracy is better than 0.5 per cent of half scale.

The integrator and summer are operational amplifier circuits. Vacuum tube amplifiers were used because they were readily available. In studying the errors introduced by a passive RC integrator the RC network was simulated with an operational amplifier feedback circuit.

The comparators are described in Ref. 10. Because carries are generated when X_{A} exceeds $\frac{1}{2}$ m.u., rather than 1 m.u., it is possible to use a relatively simple comparator accurate to about $\frac{1}{2}$ volt.

Master Control Clock:[11] The master control clock generates precise (0.05 per cent) time intervals T = 1 millisecond and T_{H} = 0.04 milliseconds and commands precise readout time. Accurate timing is derived from a 100 kc crystal oscillator. The number of COMPUTE periods is preset with a thumbwheel switch between zero and one thousand periods in



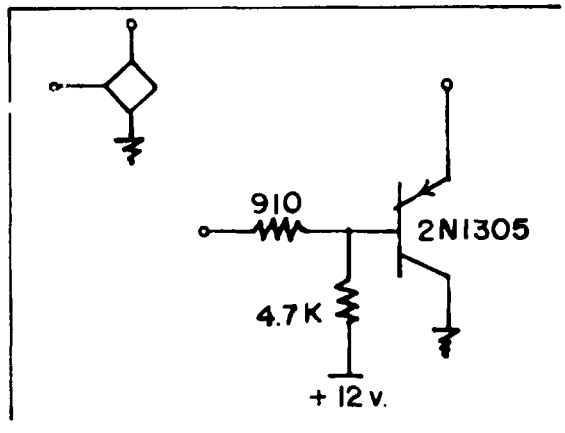


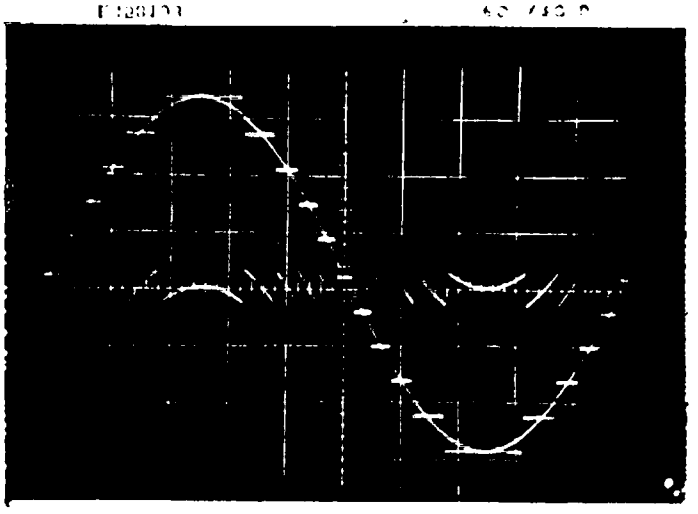
Fig. 5 6-bit D/A multiplier

steps of one hundredth of a period. Either repetitive or manual (single-run) operation is available. The master clock also generates signals which load digital initial conditions during the RESET period and controls a subroutine clock which sequences digital updating operations during each HOLD period. The subroutine clock generates nine pulses which sequence the addition of $^{k}\dot{X}_{D}$ and, if present, the integrator output carry to the R register of each integrator.

Readout System:[12] The readout system includes a digital register identical to the integrator input register and an analog sample-hold circuit. The digital and analog parts of the readout variable are patched to the readout system. The initial digital value is set with toggle switches, and increments are received during the computer run. During computation X_D is displayed by lights on the frontpanel, and X_A is tracked by a fast transistorized sample-hold circuit. At the end of the preset number of COMPUTE periods a readout signal from the master clock places the sample-hold circuit in its hold state, holding the readout value of X_A. The readout value of X_D is held in the digital register and displayed on the frontpanel lights. The readout value of X_A is displayed on a digital voltmeter. The sample-hold circuit is described in Ref. 13. It can track a ten volt sine wave with less than 5 degrees phase shift at 4 kc., and can hold within 20 millivolts for $\frac{1}{2}$

second. By changing a switch setting X_D can be converted to an analog voltage and summed with X_A to form the analog signal X for oscilloscope display of the readout variable. This is illustrated in Fig. 6

(a)



(b)

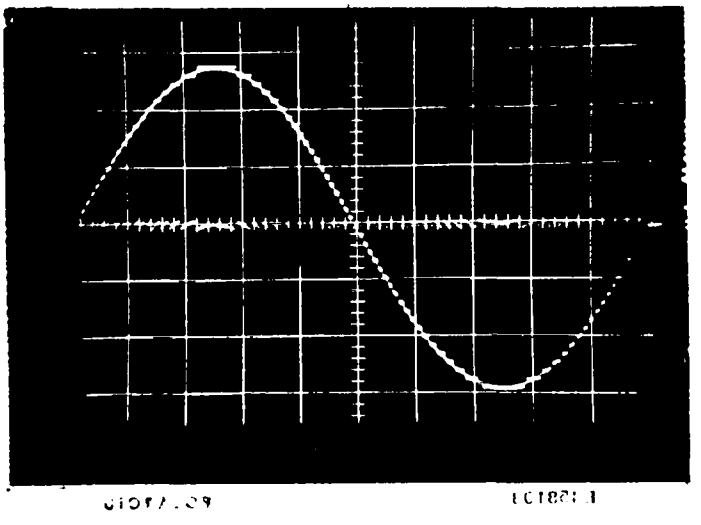


Fig. 6 Photographs showing X, X_D, and X_A for

(a) 5 m.u. sine wave and
(b) 20 m.u. sine wave

TESTS, RESULTS, AND DISCUSSION

To test the system the differential equation

$$\ddot{Y} + \left(\frac{10^3}{64}\right)^2 Y = 0, \qquad Y(0) = 30 \text{ m.u.}$$

was solved. The computer setup for this equation is the sine-loop or circle test (Fig. 7). It was selected because:

1. It provides an indication of combined error effects on computer solutions of linear differential equations.[5]
2. Earlier results indicate that it is the most stringent test of a hybrid code system.[3]
3. Its solution ranges over the full scale of positive and negative values, and the exact analytical solution can be accurately calculated for any time.

Results Using Active Analog Integrator: Figure 8 shows the results obtained with a 5-bit digital channel and an operational amplifier analog integrator. The error, the difference in millivolts between the hybrid-code solution and the correct solution, in this case 30 sin (k/64) m.u., is plotted against the number of COMPUTE periods. The absolute error is typically less than 100 millivolts (0.032 per cent of half scale). The maximum error is 150 millivolts (0.047 per cent); the average error and the rms error over

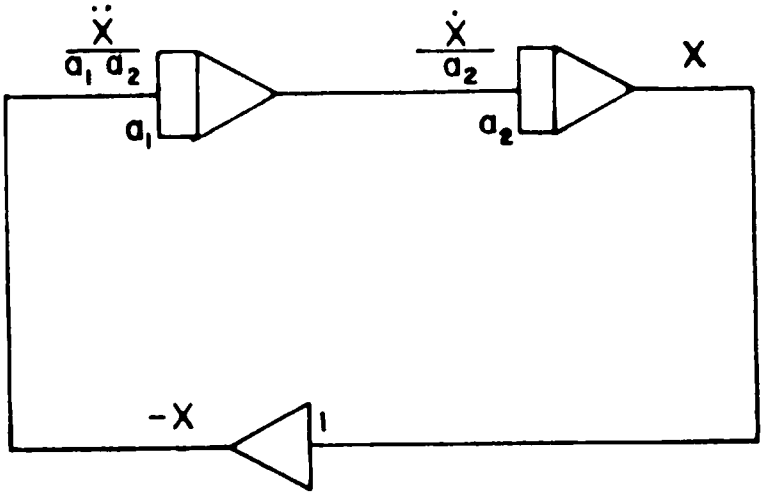


Fig. 7 Sine loop (circle) test

$a_1 = a_2 = 15.625$

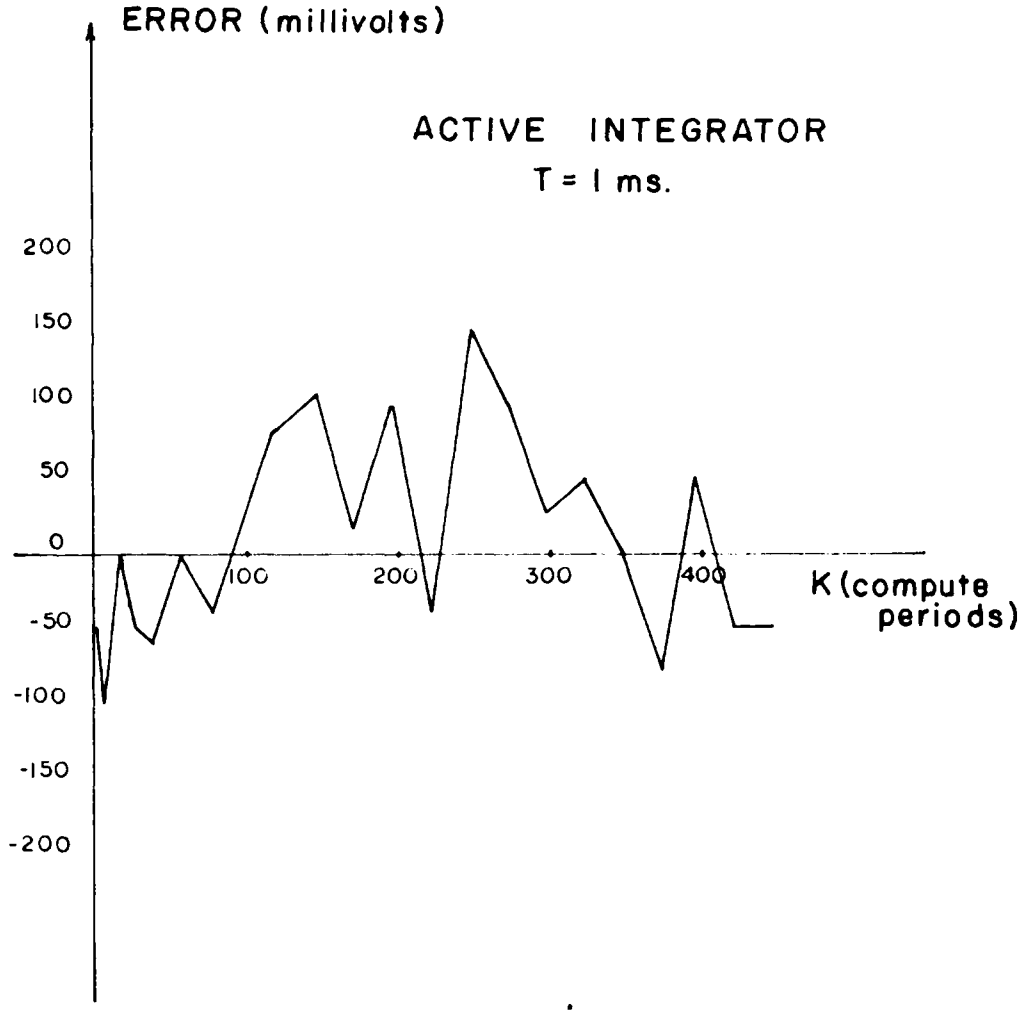


Fig. 8 Results, employing active analog integrator

Note that the magnitude of a 30 m.u. sine wave is equivalent to 300 volts.

one cycle of the solution (k = 400 periods) are 11 millivolts (0.003 per cent) and 64 millivolts (0.020 per cent) respectively. The sine wave frequency is 2.5 cps.

Discussion: The results compare favorably with those obtained previously by Wait[3] with a 3-bit digital channel and an active analog integrator. His results showed a maximum absolute error of 130 millivolts (0.163 per cent of half scale) and average error and rms error over one cycle of 17.0 millivolts (0.021 per cent) and 61 millivolts (0.076 per cent) respectively. His solution frequency was 8.0 cps, and the COMPUTE period's duration was 1.25 milliseconds.

The results verify the predicted accuracy of $(p/2^n) = (1/32)$ per cent of half-scale. In addition, by shortening the COMPUTE period to 1 millisecond the bandwidth/error quotient has been increased by 20 per cent over previous results. Note, however, that the COMPUTE period cannot be further shortened indefinitely, for switching errors in the integrator and D/A multipliers and phase shift around the sine loop become major sources of error as the period is shortened.

Results Using Passive Analog Integrator: (see Fig. A-1) The results obtained with a simulated passive RC integrator replacing the active integrator are shown in Fig. 9 for RC time constants of 1, 5, and 10 seconds. The results are shown for approximately one cycle of the solution. As

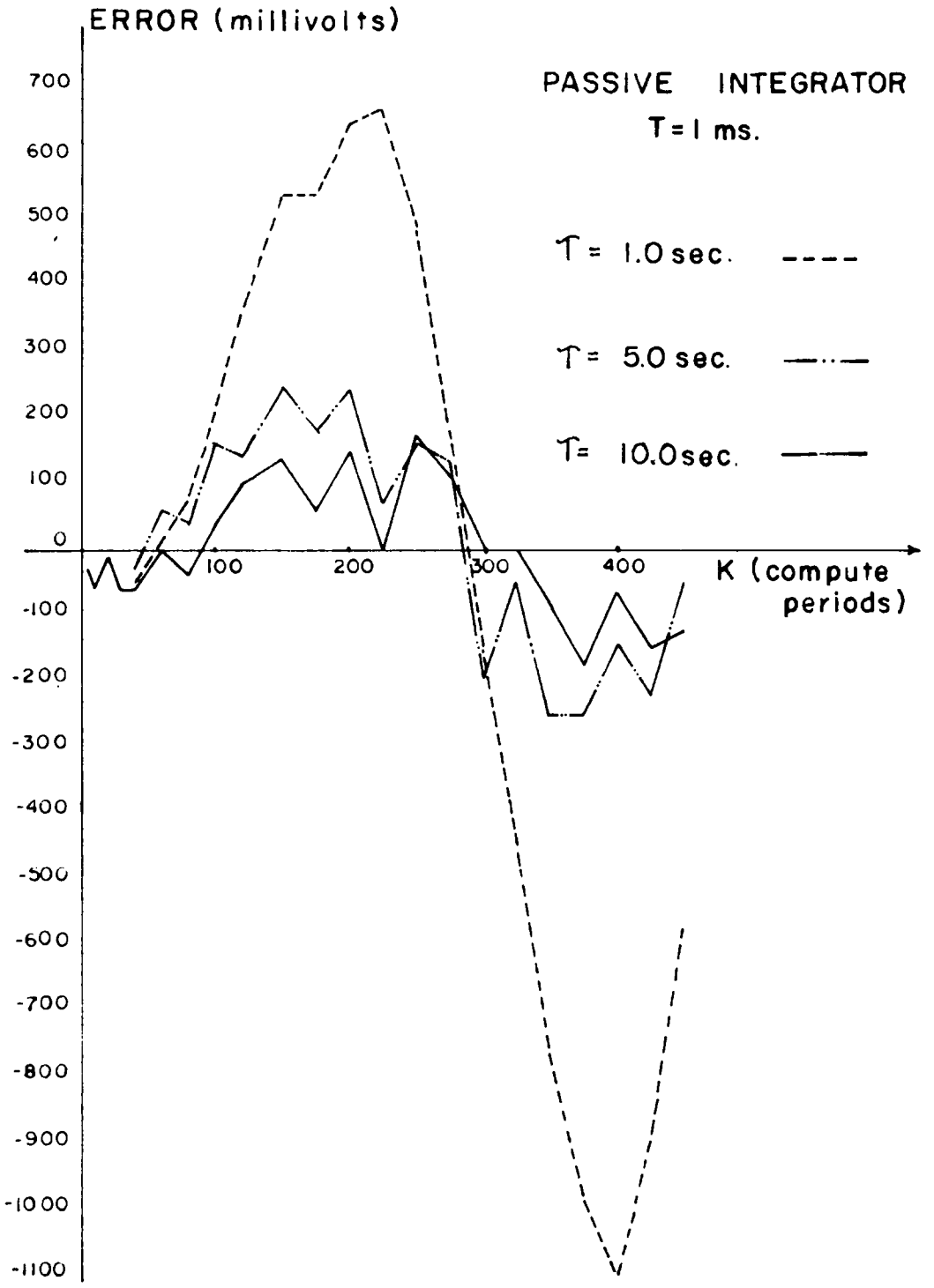


Fig. 9 Results, employing passive analog integrator

expected, relatively accurate results are obtained with time constants long compared to the solution time; accuracy decreases as the time constant decreases, and the error increases with time. With a time constant τ = 5 seconds, the maximum error is 250 millivolts (0.078 per cent). With τ = 1 second, the error is 670 millivolts (0.21 per cent) after 225 COMPUTE periods and 1.1 volt (0.344 per cent) after 400 periods.

Discussion: It is not possible to specify the overall hybrid-code accuracy required without knowing the specific nature of the problem being solved. However, for the purpose of discussion, consider the desired analog accuracy to be p = 8 per cent of analog half-scale over one cycle of the sinusoidal solution. This corresponds to an accuracy of 0.25 per cent of hybrid half-scale.

In the Appendix, some considerations in the realization of a passive analog integrator for a hybrid code system are considered. It is found that there are practical limitations on the combination of integrator gain and time constant obtainable in practice. In particular, for the system under consideration a realizable passive integrator with the necessary rate-gain has a time constant less than 0.1 second. The passive-integrator tests show that a time constant greater than 1.0 second is necessary to achieve the desired accuracy. Clearly, a 5-bit system

with COMPUTE period of 1.0 millisecond and passive analog channel does not provide the desired accuracy.

It is necessary to consider whether the desired accuracy-bandwidth can be achieved through a further increase in the number of bits and/or an increase in the clock rate, thus shortening the COMPUTE period. Increasing the number of bits both increases the accuracy and decreases the bandwidth by the same factor: the bandwidth/error quotient is unaltered. This means that the passive integrator can have a lower gain but must have a correspondingly longer time constant. This method does not alleviate the realization problem.

The prospect of increasing the clock rate is inviting because, if a given analog accuracy can be maintained, this directly increases the bandwidth/error quotient. However, it requires increasing the analog integrator gain; and, perhaps more important generally, it increases the bandwidth required in the analog channels. The latter requirement is seen in the need for faster switching in the D/A multipliers and integrator and in phase shift in the summing amplifier due to its distributed capacitance and that of its feedback resistor and the resistive networks of the D/A multipliers. The requirement of higher gain is sufficient to eliminate this as a method for increasing the bandwidth/error quotient of the 5-bit system.

The effect of the timing and phase-shift errors introduced by increasing the clock rate is illustrated in Fig. 10, which shows the results obtained with the 5-bit system when the COMPUTE period was shortened to 0.25 milliseconds. The analog channel employed the active integrator. The rapid increase of the error clearly indicates the deterioration of the accuracy of the analog channel as a result of increasing the clock rate. The same analog channel which introduces less than 1 per cent analog error with T = 1.0 milliseconds introduces more than 10 per cent error with T = 0.25 milliseconds. These results indicate a general problem faced in attempting to increase the bandwidth/error quotient by increasing the clock rate.

Finally, consider the prospect of both increasing the number of bits and shortening the COMPUTE period. The effect of the former adjustment is to increase the accuracy and decrease the bandwidth, while that of the latter is to increase the bandwidth. One hopes for an overall effect of increasing the accuracy and maintaining or increasing the bandwidth.

As an example, consider an 8-bit system with T = 50 microseconds as mentioned in Ref. 2. From eq. (3) the necessary analog bandwidth is 1.6×10^3 cps. From eq. (4) the necessary rate gain is about 40. At this operating frequency the summing amplifier's feedback resistor would have to be of the order of 10K or smaller to reduce phase

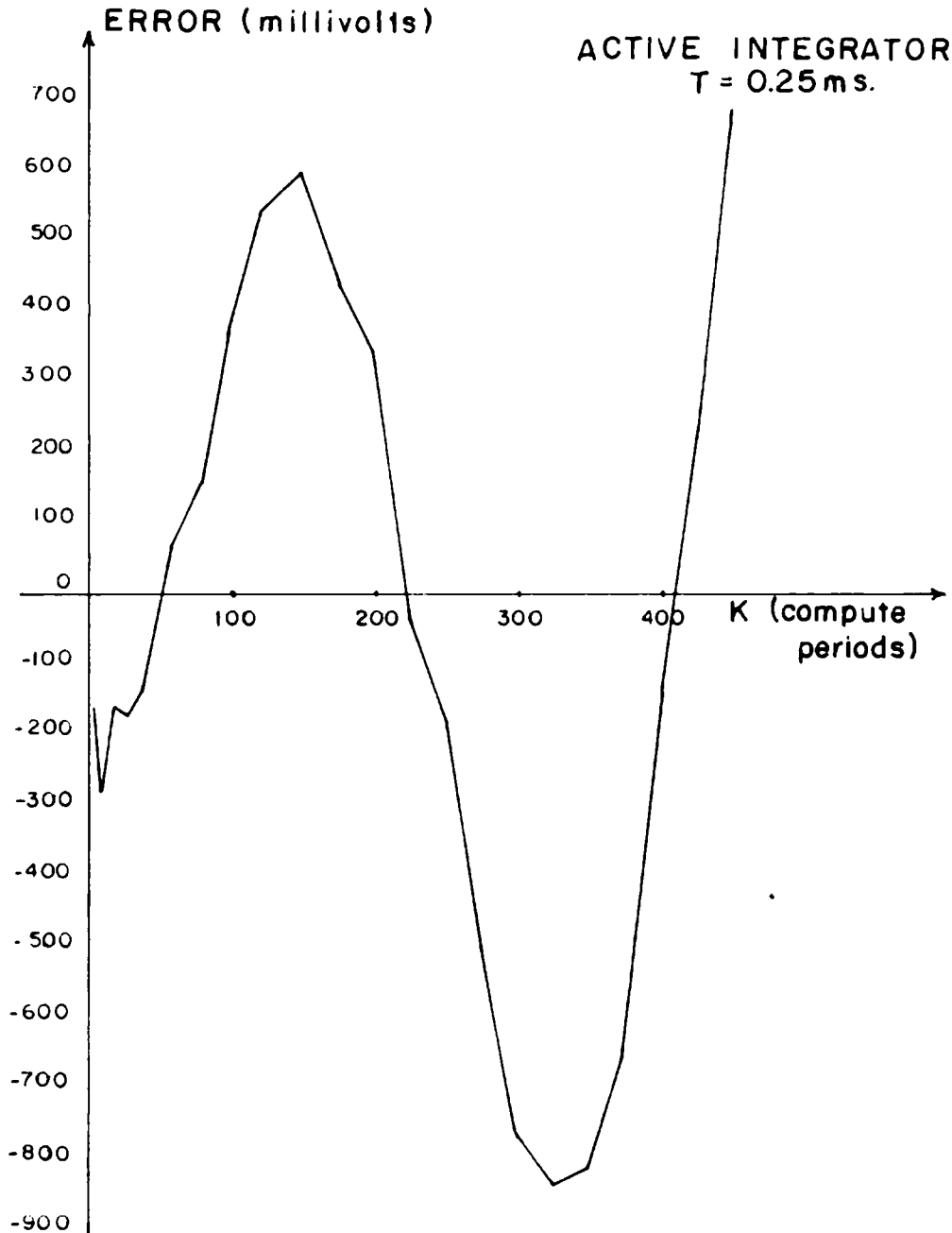


Fig. 10 Results, employing shorter COMPUTE period

shift. The passive integrator tests give a rough estimate of the time constant required to obtain a given accuracy; namely, a time constant longer than about 10 periods of the sine wave is required for 5 per cent accuracy over one cycle of the sine wave. The sine wave period for the 8-bit system is 161 milliseconds, calling for a time constant of about 1 second. It is shown in the Appendix that with 10K feedback resistor the combination of rate-gain of 40 and time constant of 1 second is not practically realizable.

CONCLUSIONS

The experiments employing the active analog integrator provide a convincing verification of the theoretically predicted accuracy of a hybrid-code system. Using an analog channel with nominal accuracy of 1 per cent of half-scale and a 5-bit plus sign digital channel, the results were well within the predicted accuracy of $(p/2^n)$ per cent (0.031 per cent) of half-scale. This accuracy was obtained while maintaining a full scale hybrid-code bandwidth of 2.5 cps, resulting in a bandwidth/error quotient considerably greater than had been previously obtained.

The experiments employing a simulated passive integrator show that for a 5-bit system sufficient accuracy cannot be achieved with a practically realizable passive analog integrator. Further, in attempting to increase the bandwidth/error quotient by increasing the clock rate (shortening the COMPUTE period), one is faced with the problems of switching errors and limited summing amplifier frequency response. Finally, the results suggest that even for a system with a greater number of bits and a shorter COMPUTE period, a realizable passive analog integrator does not in general provide an admissible combination of accuracy and bandwidth. It is unlikely that a hybrid-code system

employing a passive analog channel would provide a bandwidth/error quotient sufficient for practical application.

APPENDIX

Considerations for a Realizable Passive Analog Integrator:

A passive integrator and the analog summing amplifier are shown in Fig. A-1. The transfer function of the combination is given by the expression

$$\frac{X_A'}{X_A} = \frac{R_f}{R_1 + R_2} \times \frac{1}{1 + S \quad CR_1R_2/(R_1 + R_2)}$$

which has the form

$$\frac{X_A'}{X_A} = \alpha \times \frac{1}{1 + S\tau}$$

where (α/τ) is the rate-gain and τ is the time constant of the integrator. The transfer function can also be written in the form

$$\frac{X_A'}{X_A} = \frac{\alpha}{\tau S}\left[1 - \frac{1}{1 + S\tau}\right] \qquad \text{A-1}$$

where the first term on the right hand side of equation (A-1) is the transfer function of an ideal integrator with gain of (α/τ) and the second term represents the error due to the non-idealness of the integrator. For accurate integration τ should be large enough to make the error term negligible.

The hybrid-code configuration places restrictions on the possible values of the circuit elements. For

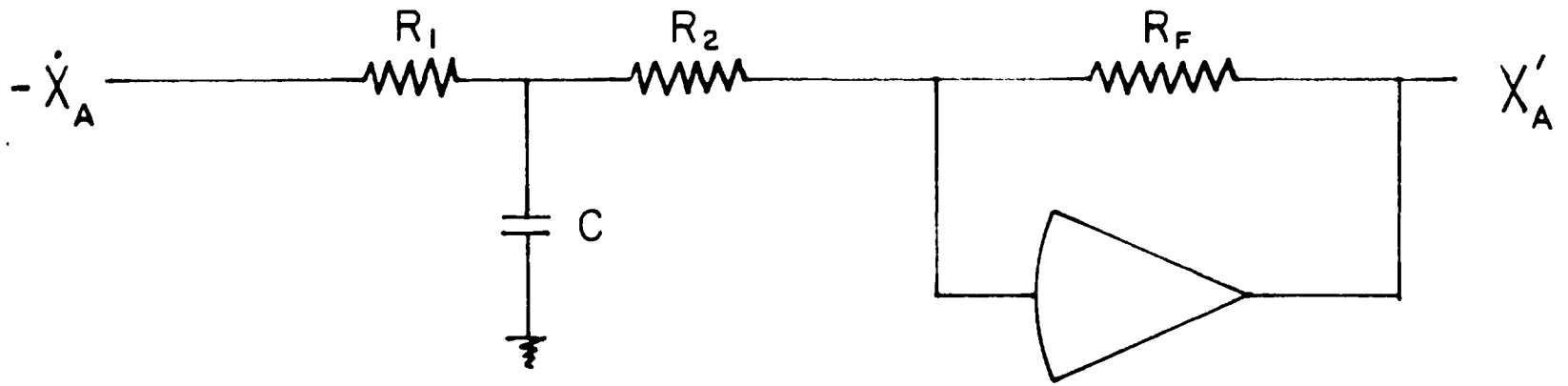


Fig. A-1 Passive analog integrator and summing amplifier

example, in this system the summing amplifier also serves as the output stage of two D/A multipliers, both of which require that R_f = 10 K. Also, by eq. (3), the rate-gain must satisfy the inequality

$$\frac{\alpha}{\tau} \leq \frac{1}{2^{n+1} T} \qquad \text{A-2}$$

Ordinarily, (α/τ) is chosen so as to satisfy the equality sign; otherwise extra bits are required in the R register.

Equation (A-2) and the definition of the time constant require that the elements satisfy the expressions

$$\frac{\alpha}{\tau} = \frac{R_f}{CR_1R_2} = \frac{1}{2^{n+1} T} \qquad \text{A-3}$$

and

$$\tau = \frac{CR_1R_2}{R_1 + R_2} \qquad \text{A-4}$$

By eq. (A-3)

$$R_2 = \frac{R_f \, 2^{n+1} T}{CR_1}$$

By eq. (A-4)

$$R_2 = \frac{\tau R_1}{CR_1 - \tau}$$

Equating the above expressions, cross-multiplying, and dividing by the coefficient of R_1^2 yields the quadratic equation

$$R_1^2 - \left[\frac{2^{n+1}\ T\ R_f}{\tau}\right] R_1 + \left[\frac{2^{n+1}\ T\ R_f}{C}\right] = 0 \qquad \text{A-5}$$

The solution of eq. (A-5) for R_1 is

$$R_1 = \frac{1}{2}\left[\frac{2^{n+1}\ T\ R_f}{\tau} \pm \sqrt{\left(\frac{2^{n+1}\ T\ R_f}{\tau}\right)^2 - 4\left(\frac{2^{n+1}\ T\ R_f}{C}\right)}\right]$$

For physical realizability, R_1 must be real valued which requires that

$$\left[\frac{2^{n+1}\ T\ R_f}{\tau}\right]^2 \geq 4\left[\frac{2^{n+1}\ T\ R_f}{C}\right] \qquad \text{A-6}$$

For fixed values of n, T, R_f, and τ the inequality (A-6) specifies the minimum value of C for a physically realizable passive integrator.

Table A-1 lists the minimum values of C for a system with n = 5 bits, T = 1.0 millisecond, and feedback resistor values of 10 K and 100 K, and time constants of 0.1, 1.0, and 10.0 seconds.

In addition to the restriction due to physical realizability, there are further restrictions if the passive analog channel is to be practically realizable. The most important of these is indicated in Ref. 3 in the results of tests determining the affect of gain errors in the integrator and in the summing amplifier. The results show that in an open-loop integration using an active analog integrator the solution error introduced by an

TABLE A-1

MINIMUM CAPACITOR VALUES FOR TIME CONSTANTS OF 0.1, 1.0, 10.0 SECONDS AND FEEDBACK RESISTORS OF 10 K and 100 K

(n = 5 bits, T = 1m sec.)

	R_f	
τ	10 K	100 K
.1	62.5 μf	6.25 μf
1.0	6,250 μf	625 μf
10.0	625,000 μf	62,500 μf

artificial 10 per cent error in the analog integrator gain builds up almost linearly with time and exceeds 15 per cent of analog half-scale after only 75 milliseconds. The conclusion to be drawn from these results is that it is necessary to maintain an accurate analog integrator gain, even when using a passive integrator.

Since the integrator gain (rate-gain) is a function of C, it is necessary to use an accurate, stable capacitor in the passive analog integrator. Such capacitors are both bulky and expensive for values greater than 1 microfarad.

In addition $\dot{X}_A$ is the output of a summing amplifier and takes on values as large as 10 volts. Most operational amplifiers deliver a maximum current of less than 50 milliamperes. For an amplifier with limited current capacity,

this restricts the minimum value of R_l that can be supplied with current. For example, an amplifier with 25 milliampere current capacity requires that R_l exceed 400 ohms. Assuming the minimum value of C, the expression for R_l is

$$R_l = \frac{2^n \; T \; R_f}{\tau}$$

With n = 5 bits, T = 1 millisecond, and R_f = 10 K, R_l is given by the equation

$$R_l = \frac{320}{\tau} \text{ ohms}$$

With n = 8 bits, T = 50 microseconds, and R_f = 10 K, R_l is given by the equation

$$R_l = \frac{128}{\tau} \text{ ohms}$$

Both of the above equations indicate that τ should be of the order of 0.1 second at most in order that a summing amplifier be capable of driving R_l.

Because it requires such a large capacitor value and such low resistances, a passive integrator with time constant longer than about 0.1 second is considered impractical.

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