COMPENSATION OF A PULSE-WIDTH-MODULATED CONTROL SYSTEM USING A HYBRID ANALOG COMPUTER

by

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ABSTRACT

Pulse-width-modulated control systems are inherently non-linear and difficult to analyze in an exact manner. However, if the input to the system is bounded and the sampling period is short compared to the significant time constant of the plant, it can be treated mathematically as a linear system. Z-transform techniques can then be used to study the characteristics of the system. If compensation is needed, an equalizer can be designed by conventional techniques.

The compensation of a pulse-width-modulated control system (PWMS) can be realized with either pulsed RC networks or a digital computer. For simulation purposes, the flexibility of a digital computer is useful, but the cost factor is often prohibitive. In this thesis, a method is introduced to compensate a PWMS with a hybrid analog computer. This method retains the flexibility of digital compensation, but allows a substantial reduction in cost.
CHAPTER 1

INTRODUCTION

Pulse-width modulation (PWM) is a process in which an input signal is sampled periodically and changed into a sequence of equally spaced pulses whose individual widths are proportional to the input at the sampling instant. The magnitude of the pulses are equal and the sign of a given pulse is the same as that of the sampled signal at the corresponding sampling instant. A pulse-width-modulated control system (PWMS) is a type of sampled data control system in which one or more signals are in pulse width modulated form. PWMS have been the subject of investigations in recent years \(1, 2, 3\), and have the advantage that the plant can be controlled by relays or on-off type electronic circuitry. This and other advantages of PWMS are discussed in Chapter 2.

PWMS are inherently non-linear and difficult to analyze analytically. However, under certain conditions, they can be approximated by a linear system, and transform techniques may be used for analysis. An approximation introduced by Andeen \(4\), which replaces the PWMS with an equivalent pulse-amplitude-modulated control system (PAMS), is used throughout this thesis. It is assumed
that the reader is familiar with z-transform techniques and has a background in the analysis of sample data systems.

The designer of a PWMS will usually find it necessary to add some type of compensation to the system in order to improve its performance characteristics. Methods of compensating PAMS can be extended to PWMS and include,

1. Cascaded RC networks
2. Pulsed RC networks
3. A digital computer

If one of the first two methods is used, the pulsed error signal can be fed directly into the compensator, since the RC network acts as a low-pass filter. If a digital computer is used, the signal must first be converted into pulse-amplitude modulated form. The advantages of each type of compensation are discussed in Chapter 3.

In some instances, particularly in simulation studies, digital compensation presents the following difficulties,

1. If the plant is simulated on an analog computer, conversion devices are needed to hook-up with the digital computer. Also, the digital computer may be in another building which would create problems in transmitting data.

2. If the complete system is simulated on a digital computer, the program may be excessively complicated.
3. The effects of varying parameters can not be readily seen.

For the above reasons, it is feasible to consider analog compensation for PWMS. In this thesis, analog techniques for the compensation of PWMS are introduced. A second order system is simulated and compensated on a hybrid analog computer and the results shown in Chapter 4. The results are discussed in Chapter 5.
CHAPTER 2

PULSE MODULATED CONTROL SYSTEMS

2-1 Introduction

Modulation is the process by which an information bearing signal is changed into a more desirable form. The input signal may be continuous, as in amplitude or frequency modulation, or it may be sampled, as in pulse modulation.

Two types of pulse modulation are pulse-amplitude modulation (PAM) and pulse-width modulation (PWM). In PAM the input signal is sampled periodically and the output consists of a pulse whose amplitude is equal to the magnitude of the input signal. This process is illustrated in Figure 2-1a & b. A hold circuit is used in conjunction with the sampler and the output appears as in Figure 2-1c. In PWM the input is again sampled periodically, but the output is a pulse of constant amplitude whose width is made proportional to the magnitude of the input signal. The sign of the pulse is the same as that of the signal. This process is illustrated in Figure 2-2. A hold circuit may be used following the sampler. This depends on the method used to obtain PWM.
Fig. 2-1 Characteristics of Pulse-Amplitude Modulation
(a) Pulse-Width Modulator

(b) Input Signal

(c) Output of Pulse-Width Modulator

Fig. 2-2 Characteristics of Pulse-Width Modulation
Other types of pulse modulation which warrant mention are pulse-code modulation (PCM) and pulse-position modulation (PPM). In PCM the signal is sampled, quantized, and converted into a sequence of coded pulses. Pulse-position modulation is similar to PWM except that the output pulses are all of the same sign and are modulated about a fixed width according to the magnitude of the input signal. A discussion of pulse modulation with applications directed toward communication systems can be found in *Modulation Theory* by Black (5).

2-2 **Applications in Control Systems**

Although pulse modulation had its beginning in communication systems, it has since been applied to control systems. These systems, which may be classified as sampled-data and digital control systems, differ from the continuous type in that the signal in one or more sections of the system is in the form of a pulse train or numerical code. Systems using pulse-code modulation generally use a digital computer or digital sensing element in the loop and may be classified as digital control systems. Control systems with PAM or PWM are classified as sampled-data systems and, in general, receive information only at discrete instants of time. They may or may not contain a digital computer in the loop depending upon the type of compensation used. An actual system may contain all three types of pulse
modulation but it is convenient for purposes of analysis to
differentiate between them. The remainder of this thesis
will be concerned with PWM and PAM control systems, with
emphasis placed on improving the characteristics of the
former.

2-3 Pulse-Amplitude-Modulated Control Systems

Pulse-amplitude-modulated control systems (PAMS)
have been discussed quite extensively in the literature
and are the subject of four texts (6, 7, 8, 9). If the
fixed plant is linear, a PAMS can be analyzed by z-
transforms. Design techniques used in continuous systems
have been extended and meaning given to terms such as
phase and gain margin for a sampled system.

An example of a PAMS is shown in Figure 2-3. The
hold circuit is of zero order and has an impulse response
given by,

\[ h(t) = U(t) - U(t - T) \]  

(2-1)

The Laplace transform of equation 2-1 is,

\[ H(s) = \frac{1 - e^{-sT}}{s} \]  

(2-2)

where \( T \) is the sampling period. If the fixed plant is
linear and has a transfer function,

\[ G(s) = \frac{a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} + \ldots + a_n}{b_0 s^m + b_1 s^{m-1} + b_2 s^{m-2} + \ldots + b_m} \]  

(2-3)
where \( n \) is less than or equal to \( m \), the closed loop transfer function can be written,

\[
K(z) = \frac{C(z)}{R(z)} = \frac{GH(z)}{1 + GH(z)}
\]  

(2-4)

where \( GH(z) \) is the \( z \)-transform of \( GH(s) \). After determining the response to various inputs, the performance characteristics of the system can be judged, and a decision made as to whether some form of compensation is needed.

In general, the designer will not be able to satisfy all of the desired performance specifications without some form of compensation. Two common schemes to improve the characteristics of PAMS are shown in Figure 2-4. Figure 2-4a shows a PAMS compensated by the insertion of a RC network in the forward path of the system. This network can be of the "lag" or "lead-lag" type used to compensate continuous systems. If it is assumed that the network has a transfer function \( G_C(s) \), the closed loop transfer function can be written,

\[
K(z) = \frac{GHG_C(z)}{1 + GHG_C(z)}
\]  

(2-5)

where \( GHG_C(z) \) is the \( z \)-transform of \( G(s)H(s)G_C(s) \). Since \( GHG_C(z) \approx G_C(z)GH(z) \), the compensation can not be treated separately from the rest of the system, and it becomes difficult analytically to evaluate the effects of various
Fig. 2-3 A Pulse-Amplitude-Modulated Control System

Fig. 2-4 Compensation of a Pulse-Amplitude-Modulated Control System

(a) Cascaded RC Network

(b) Digital Controller
networks on the over-all performance of the system. The method of compensation shown in Figure 2-4b alleviates this difficulty by including a sampler after the compensating device. The closed loop transfer function now becomes,

\[ K(z) = \frac{D(z)GH(z)}{1 + D(z)GH(z)} \]  \hspace{1cm} (2-6)

where \( D(z) \) is the transfer function relating the weighted error function, \( e^*(t) \), to the sampled error, \( e_1^*(t) \).

Solving for \( D(z) \), equation 2-6 becomes,

\[ D(z) = \frac{1}{GH(z)} \frac{K(z)}{1 + K(z)} \]  \hspace{1cm} (2-7)

\( D(z) \) can now be treated separately from the fixed plant and conventional design procedures applied.

2-4 Pulse-Width-Modulated-Control Systems

The block diagram of a PWMS is shown in Figure 2-5. Although it may be feasible to modulate a continuous signal before applying it to the plant, only systems which receive error signals in pulse-width modulated form will be considered in this thesis. Therefore, in the figure the error detector and modulator are treated as one block and \( m(t) \) is shown in pulse-width modulated form. The system described above is applicable to earthbound as well as satellite control and has the following advantages:

1. PWM signals can be multiplexed with other information.
2. The system will have a high signal-noise ratio since any variations in the incoming signal can be removed by clipping.

3. Only two control values are used. Thus, equipment complexity can be reduced and reliability increased.

The first two advantages show that the system is attractive from a communication standpoint while the third shows the desirability of keeping the control signal in pulse-width modulated form. It will be shown in Chapter 3 that additional circuitry will have to be included after any compensation device in order to return the control signal to PWM form.

The principle disadvantage of PWMS is that the modulation scheme introduces non-linearities and complicates the analysis of the system. The characteristic of the pulse-width modulator is shown in Figure 2-6. The modulator is linear in the sense that, below the saturation levels, the output pulse width due to the sum of two input signals equals the sum of the pulse widths due to the two input signals acting individually. However, superposition does not apply, and the equations representing the closed loop response of the system can not be solved with transform methods. Therefore, most of the techniques used in the analysis of PWMS are based on a linearization of the system.
Fig. 2-5 Block Diagram of a Pulse-Width-Modulated Control System

Fig. 2-6 Characteristics of the Pulse-Width Modulator
Two different types of PWM signals are shown in Figure 2-7. The pulse-width modulator used in the experimental portion of this thesis produced pulses as shown in Figure 2-7b. This type of signal has the advantage that only a small amount of power is dissipated for the no-signal case. The type of PWM signal shown in Figure 2-7c is easier to generate, but more power is used, since an output exists for the whole sampling period, even when the input is zero. The approximations considered in this thesis will be valid for both types of signals.

For the case where the maximum value of the input is limited between the saturation values of the modulator, and the sampling period is small compared to the smallest time constant of the system, Andeen\(^4\) has shown that the PWM can be approximated as a PAMS having a hold circuit with a transfer function,

\[
H(s) = \frac{E}{R_{\text{max}}} \frac{1 - e^{-\beta Ts}}{s} \tag{2-8}
\]

where \(R_{\text{max}}\) is the maximum value of the input, \(E\) is the magnitude of the output pulses, \(T\) is the sampling period, and \(\beta\) is the ratio of the maximum pulse width to the sampling period. \(\beta\) can range from 0 - 1 but will be considered unity throughout this thesis. The ratio \(E/R_{\text{max}}\) is simply a gain term and can have any value, but
Fig. 2-7 Waveforms For Pulse-Width Modulation
will also be considered equal to unity. Equation 2-8 can now be written,

\[ H(s) = \frac{1 - e^{-Ts}}{s} \]  

(2-9)

If the plant is linear, the PWM3 can now be analyzed by z-transforms. Methods of compensating PAMS can be extended to PWMS and will be discussed in the next chapter. Also, a compensation scheme employing analog storage will be introduced.
CHAPTER 3

COMPENSATION OF PULSE-WIDTH-MODULATED CONTROL SYSTEMS

3-1 Introduction

The design problem involved in the compensation of PAMS by the insertion of RC networks in the forward path was discussed in section 2-3. The same difficulty exists for PWMS. Namely, the compensator can not be treated separately from the fixed plant, and it becomes difficult analytically to evaluate the effects of various networks on the over-all performance of the system. This problem can be alleviated by introducing digital compensation into the loop. A PWMS compensated by a digital controller is shown in Figure 3-1a. The error signal is received in PWM form and demodulated before being introduced into the equalizer. The weighted error signal is then modulated and applied to the plant. (It is desirable to have the compensated error signal in pulse width modulated form so that the plant can be controlled by "on"-"off" type devices.)

A linear approximation to a compensated PWMS is shown in Figure 3-1b. The demodulator is represented by a time delay of one sampling period and the pulse-width modulator by a zero-order hold whose transfer function is
Fig. 3-1 Block Diagram of a Pulse-Width Modulated Control System Compensated By a Digital Controller
given by equation 2-9. Demodulation of PWM signals is accomplished by integrating each pulse. This process is illustrated in Figure 3-2. The output of the integrating device is set to zero at the end of each sampling period. If the output is sampled just before the end of the sampling period, the demodulated signal will be as shown in Figure 3-2d. The error signal will be delayed one sampling period due to the demodulation and this will tend to decrease the stability of the system. However, if the ratio of the dominant time constant to the sampling period is large, the effect of the time delay will be negligible.

The digital compensator, D(z), can be realized in a number of ways. A method that uses RC networks has been introduced by Sklansky(10) and a scheme utilizing a digital computer has been suggested by Barker(11). A third method which makes use of analog devices is introduced in this chapter.

3-2 Pulsed Data RC Networks

Sklansky's method involves realizing D(z) with pulsed data RC networks. The series pulse-data realization is shown in Figure 3-3b. The transfer function relating the modified pulse sequence, \( e_2^*(t) \), to the original error, \( e_1^*(t) \) is given by,
Fig. 3-2 Demodulation of a Pulse-Width Modulated Signal
Fig. 3-3  Realization of a Digital Controller With Pulsed-Data RC Networks
\[ D_s(z) = G_{ho}G(z) \]  
\[ D_s(z) = Z \left( \frac{1 - e^{-sT}}{s} \right) G(s) \]  
\[ D_s(z) = (1 - z^{-1}) Z \left( \frac{G(s)}{s} \right) \]

which becomes,
\[ Z \left( \frac{G(s)}{s} \right) = \frac{1}{1 - z^{-1}} D_s(z) \]

If \( D_s(s) \) satisfies certain restrictions (the strictest requirement is that its poles are simple, real and positive, and lie inside the unit circle, \(|z| = 1\), in the \( z \) plane) equation 3-4 can be written,
\[ Z \left( \frac{G_0(s)}{s} \right) = \frac{A_0}{1 - z^{-1}} + \sum_{k=1}^{\infty} \frac{A_k}{1 - e^{-s_k T} z^{-1}} \]

Taking the inverse \( z \) transform, this becomes,
\[ \frac{G_c(s)}{s} = \frac{A_0}{s} + \sum_{k=1}^{\infty} \frac{A_k}{s + s_k} \]

and \( G_c(s) \) may be realized as an RC network.

The feedback realization for the pulsed-data network is shown in Figure 3-3c. The transfer function, \( e_2^*(t)/e_1^*(t) \) is given by
\[ D_f(z) = \frac{1}{1 + G_{ho} H(z)} \]  \hspace{1cm} (3-7)

or,
\[ D_f(z) = Z \left\{ \frac{1 - e^{-sT}}{s} H(s) \right\} = 1 - D_f(z) \]  \hspace{1cm} (3-8)

and
\[ Z \left\{ \frac{H(s)}{s} \right\} = \frac{1}{1 - z^{-1}} \frac{1 - D_f(z)}{D_f(z)} \]  \hspace{1cm} (3-9)

If the following conditions are fulfilled:

1. The zeros of \( D(z) \) are simple, real, positive, and lie inside the unit circle of the \( z \)-plane.
2. \( D(z) \) has the same number of poles as zeros.

\( H(s) \) may be realized by an RC network.

In general, it is not possible to realize an arbitrary \( D(z) \) by a series network or a parallel network alone. In the series structure the zeros of \( D(z) \) are arbitrary, whereas in the feedback case the poles of \( D(z) \) are arbitrary. Therefore, a combination of the two procedures must be used. With the series-feedback realization of Figure 3-3d, any physically realizable pulse transfer function can be synthesized.

3-3 A Digital Computer Method

A method for realizing \( D(z) \) which makes use of a digital computer has been developed by Barker(11). Again \( D(z) \) must be physically realizable. That is, it can not
produce an output prior to the application of an input.
This condition is met if $D(z)$ can be expressed in the following form,

$$D(z) = \frac{a_0 + a_1z^{-1} + a_2z^{-2} + \ldots + a_mz^{-m}}{1 + b_1z^{-1} + b_2z^{-2} + \ldots + b_kz^{-k}}$$ \hspace{1cm} (3-10)$$

where the $a$'s and $b$'s are arbitrary. $D(z)$ can be broken up into two transfer functions,

$$D(z) = \frac{e_2(z)}{e_1(z)} = \frac{e_2(z)}{C_1(z)} \frac{C_1(z)}{e_1(z)}$$ \hspace{1cm} (3-11)$$

where,

$$\frac{C_1(z)}{e_1(z)} = \frac{1}{1 + b_1z^{-1} + b_2z^{-2} + \ldots + b_kz^{-k}}$$ \hspace{1cm} (3-12)$$

and,

$$\frac{e_2(z)}{C_1(z)} = a_0 + a_1z^{-1} + a_2z^{-2} + \ldots + a_mz^{-m}$$ \hspace{1cm} (3-13)$$

In the time domain, equation 3-12 can be written,

$$C_1(nT) = e_1(nT) - b_1C_1(n-1)T - b_2C_1(n-2)T - \ldots - b_kC_1(n-k)T$$ \hspace{1cm} (3-14)$$

and equation 3-13 becomes,

$$e_2(nT) = a_0C_1(nT) + a_1C_1(n-1)T + \ldots + a_mC_1(n-m)T$$ \hspace{1cm} (3-15)$$
\( C_1(nT) \) can be implemented as shown in Figure 3-4a. The complete realization of an arbitrary transfer function, \( D(z) \), is shown in Figure 3-4b.

Compensation can be performed by either a general or a special purpose computer. If a general purpose computer is used, the arithmetic operations can be programmed into the computer. With a special purpose computer, both digital and analog devices could be used. In each case, the number of storage elements used equals the order of \( D(z) \).

3-4 Comparison of Conventional Methods of Realizing a Digital Controller

The principle advantage of using a general purpose digital computer as a compensating device is flexibility. This is important in simulation studies since different pulse transfer functions can be realized by changing the computer program. Another advantage is that signal values can be stored indefinitely. In some applications, particularly in process control, plant time constants may be expressed in hours. This would require long sampling periods and the necessary RC element values would be unattainable.

The principle disadvantage of a digital computer realization is its high initial cost. Unless a computer is readily attainable, RC networks will usually be the
Fig. 3-4 Block Diagram of Digital Computer Realization

(a) Implementation of $C_1(nT)$

(b) Complete Realization
most feasible method for compensating PWMS. From the standpoint of cost, the use of a digital computer will usually only be justifiable for simulation studies.

3-5 Compensation With Analog Devices

Since the error signal is in analog form, it seems feasible to design a flexible compensator that uses analog rather than digital storage. An analog or hybrid analog (analog computation and storage with digital control) device would retain the advantages of the digital realization at a reduction in cost. The realization of a compensator,

\[ D(z) = \frac{a_0 + a_1z^{-1} + a_2z^{-2}}{1 + b_1z^{-1} + b_2z^{-2}} \]  

(3-16)

which uses capacitors as storage elements is shown in Figure 3-5. (D.C. amplifiers are used as summers.) In order to achieve the time delays necessary to satisfy equation 3-14, the switches are operated according to the timing diagram of Figure 3-6. When SW1 is closed, \( C_a \) charges to the value of \( C_1(nT) \). When SW2 closes, \( C_b \) charges to the voltage held by \( C_a \). Therefore, at the next sampling instant, \( t_1 \), \( C_a \) will hold the voltage \( C_1(nT) \), while \( C_b \) holds the voltage \( C_1(n-1)T \). At the same time, \( C_c \) will be charged to the value of \( C_1 \) at the \( (n-2) \) sampling instant. These voltages can be multiplied by the
Fig. 3-5 Analog Realization with Capacitor Storage

R_o -- input resistance of summer/inverter
100k -- 1M
Fig. 3-6 Timing Diagram
appropriate constants and summed in order to obtain the corrected error, \( e_2(t) \).

In designing the analog storage elements, two conflicting requirements must be met. First, since the capacitor must charge up fully, the time constant \( R_1C \) must be small compared to the "on" time of the switch. Also, to assure that the capacitor "holds" the measured voltage, the time constant \( R_2C \) must be large compared to the sampling period. For low frequency sampling, mechanical switches can be used. However, if the sampling rate is high, it may be necessary to use electronic switching, and the design will be further complicated due to the "off" resistance of each switch.

The problem of leakage can be solved by using high gain d.c. amplifiers in sample-hold circuits. This is illustrated in Figure 3-7. A current amplifier is used to supply charging current and switching is accomplished with a six diode bridge operated by push-pull pulses. The equivalent circuit for the sample-hold in "track" operation is shown in Figure 3-7b. The transfer function for the circuit is,

\[
H(s) = \frac{-1}{sR_fC_f/\Delta + 1} \quad (3-17)
\]

where \( R_f \) and \( C_f \) are the feedback elements and \( \Delta \) is the gain of the current amplifier. In "hold" operation, the
(a) Complete Circuit

(b) Circuit in "Track"

Fig. 3-7 A Sample-Hold Circuit Using a High Gain D.C. Amplifier
capacitor in the feedback-loop holds its charge while the
d.c. amplifier supplies current to the load.

A hybrid analog computer combining digitally
controlled sample-hold units with conventional analog
components (summing/inverting amplifiers and potentiometers)
would be useful in simulation studies of PWMS since the
transfer function of the compensator could be varied
quickly by changing potentiometer settings. Such a
computer has been built\(^{(13)}\), and the results of its use
in compensating a second order PWMS will be discussed in
the next chapter.
CHAPTER 4

RESULTS

4-1 Introduction

In order to demonstrate the merits of analog compensation, the University of Arizona's hybrid analog computer, Astrac I, was used to obtain experimental data. The Arizona Statistical Repetitive Analog Computer (Astrac) combines analog arithmetic and storage with digital control. Astrac is used primarily for the study of random processes but is readily adaptable to the simulation and compensation of PWMS. A description of its operation is included in Appendix A.

The hybrid computer implementation of a transfer function was discussed in Section 3-5 and experimental verification is included in this chapter. A PAMS and a PWMS are also compared, and it is shown that with the fulfillment of the conditions listed in Section 2-4 they are equivalent. The results of demodulating a PWM signal by the technique proposed in Section 3-1 are presented and compared with a conventional method. The chapter concludes with the results of a simulation study of a second order system. The system is compensated on the computer, and
the improvement in performance is shown to be the same as predicted by theory.

4-2 Demodulation Methods

Since the information carried by a pulse-width modulated (PWM) signal is stored in the area of each individual pulse, demodulation can be accomplished by passing the pulse train through a low-pass filter. The filter passes the d.c. component of each pulse which is proportional to the pulse area. Figure 4-1 shows a 3.57 cps. sine wave that has been demodulated in this manner.

Another method of demodulating PWM signals was introduced in Section 3-1. With this method, the area of each pulse is obtained directly by integration. Figure 4-2 shows an electronically reset integrator that is used with this technique. Initial conditions (in this case zero) are reapplied during reset when the diode gate is closed. When the diode switch is "off" the circuit acts as an integrator. If the output of the integrator is sampled just before reset, demodulation can be accomplished. Figure 4-3 shows a 3.57 cps. sine wave that has been demodulated by this method. Note that there is a time delay of one sampling period involved with this procedure.

If a RC network is used for compensation, demodulation of the error signal will usually not be necessary
Fig. 4-1 Demodulating a Pulse-Width Modulated Signal By Passing It Through a Low-Pass Filter
Fig. 4-2 Circuit Diagram of an Electronically Reset Integrator
Fig. 4-3  Demodulation of a Pulse-Width Modulated Signal By Integrating Each Pulse
since the network acts as a low-pass filter. However, if a PWMS is to be compensated with a computer, the error must first be changed into a continuous signal. Here again, the pulse train could be demodulated by passing it through a low-pass filter, but the phase shift added to the system by the filter may be excessive. For this reason, the method presented in Section 3-1 is preferable even though the required circuitry is more complicated. In most cases, the short time delay (one sampling period) inherent in this method will have little effect on the performance of the system.

4-3 Implementation of a Transfer Function

A method for the implementation of a digital controller with analog elements was presented in Section 3-5. To obtain experimental verification, Astrac was used to realize the transfer function,

\[ G(z) = \frac{0.22 (z + 0.845)}{(z - 1)(z - 0.671)} \]  \hspace{1cm} (4-1)

The closed loop step response was obtained using a Sanborn recorder and is compared with the theoretical response in Figure 4-4 (experimental data is included in Appendix B). It is noted that the results are well within experimental accuracy. The block diagram of the computer simulation is shown in Figure 4-5.
Fig. 4-4 Closed Loop Step Response

Sampling Instant (n)
T = 0.1 sec.

+ Experimental Values
- Calculated Points
Fig. 4-5 Implementation of $G(z) = \frac{0.22(z + 0.845)}{(z-1)(z - 0.671)}$
4-4 Approximation Study

In Section 2-4, conditions were stated by which a PWMS can be approximated by a PAMS. Briefly, the approximation is valid if the input to the system is bounded and the sampling period is small compared to the dominant time constant of the plant. This was verified experimentally for a second order system.

The transfer function,

\[ G(s) = \frac{K}{s(s + a)} \]  \hspace{1cm} (4-2)

can be simulated on an analog computer as shown in Figure 4-6. Figure 4-7 presents the step responses for a PAMS and an equivalent PWMS containing plants characterized by equation 4-2 with \( K = 50 \) and \( a = 4 \). The sampling period for both systems is .1 second. Figure 4-8 shows the step responses for the two systems with \( K = 10 \) and \( a = 1 \). Again the sampling period is .1 second. In the first case, the ratio of the plant time constant to the sampling period is 2.5. This ratio is increased to 10 in the second case and the improvement in the approximation is noted.

4-5 Compensation of a Second Order System

The step response of a PWMS with a fixed plant,

\[ G(s) = \frac{10}{s(s + 1)} \]  \hspace{1cm} (4-3)

is shown in Figure 4-8b. The peak overshoot is
Fig. 4–6 Simulation of $G(s) = \frac{K}{s(s + a)}$
(a) Pulse-Amplitude-Modulated Control System

(b) Pulse-Width-Modulated Control System

chart speed—25 mm/sec
calibration—.4 volt/cm

Fig. 4-7 Comparison of Step Responses For a PAMS and a PWMS Having Plants $G(s) = \frac{50}{s(s + 4)}$
(a) Pulse-Amplitude-Modulated Control System

(b) Pulse-Width-Modulated Control System

Chart speed—10 mm/sec  
Calibration—.4 volt/cm

Fig. 4-8  Comparison of Step Responses for a PAMS and a PWMS Having a Fixed Plant

\[ G(s) = \frac{10}{(s)(s + 1)} \]
approximately sixty percent and compensation is needed. A method for designing the equalizer is outlined as follows:

1. Approximate the PWMS as a PAMS with a hold circuit whose transfer function is given by equation 3-9.
2. Use z-transforms to find the open-loop transfer function, \( GH(z) \).
3. Transform \( GH(z) \) to the \( w \)-plane.
4. Draw the Bode diagram of \( GH(w) \).
5. Increase the phase margin with a compensator, \( G_c(w) \).
6. Transform \( G_c(w) \) to the \( z \)-plane.
7. Realize \( G_c(z) \) by one of the methods discussed in Chapter 3.

Applying this method to the PWMS described above, the open-loop transfer function can be written,

\[
GH(z) = \frac{0.048 (z + 0.984)}{(z - 1)(z - 0.905)}
\]  
(4-4)

Under the transformation,

\[
z = \frac{1 + w}{1 - w}
\]  
(4-5)

equation 4-4 becomes,

\[
GH(w) = \frac{5(1 - w)(1 + w/124)}{w(1 + w/0.049)}
\]  
(4-6)

The Bode diagram for equation 4-6 is shown in Figure 4-9. Crossover occurs at \( w = 0.16 \) and the phase margin is
Fig. 4-9 Bode Diagram of $G(w) = \frac{5(1-w)(1 + w/12^2)}{w(1 + w/0.049)}$
approximately 10 degrees. With the addition of compensation,

\[ G_c(w) = \frac{(25w + 1)^2}{(250w + 1)(2.5w + 1)} \]  

the crossover is changed to \( w = 0.06 \) and the phase margin is increased to 50 degrees.

In the z-plane, equation 4-7 can be written,

\[ G_c(z) = 0.774 \frac{(z^2 - 1.84z + 0.85)}{z^2 - 1.42z + 1} \]  

The compensator was implemented on Astrac as shown in Figure 4-10, and the PWMS was simulated according to the scheme discussed in Section 3-1. Demodulating the error signal added a time delay of one sampling period, but the decrease in phase margin was negligible since crossover occurred for \( w << 1 \) (1/z becomes 1 - w/1 + w in the w-plane and adds 90 degrees of phase shift at \( w = 1 \)). The step response of the compensated system is shown in Figure 4-11, and is compared with the theoretical response in Figure 4-12 (experimental data is included in Appendix B). It is observed that the peak overshoot has been lowered to 34 percent, and the output closely resembles that predicted by z-transform theory.
Fig. 4-10 Implementation of $G_c(z) = \frac{0.774 (z^2 - 1.84z + 0.85)}{z^2 - 1.42z + 1}$
Fig. 4-11 Step Response of Compensated System

- chart speed -- 10 mm/sec
- calibration -- 0.44 volts/cm
Fig. 4-12 Comparison of Experimental and Theoretical Values

- Experimental Curve
- Calculated Points
CHAPTER 5

CONCLUSIONS AND SUGGESTIONS FOR FURTHER RESEARCH

5-1 Conclusions

The results of Chapter 4 confirm that a hybrid analog computer can be used to compensate PWMS. From the standpoint of cost and complexity, however, a computer will usually only be warranted when flexibility is desired, as in simulation studies. In applications where the desired compensation is fixed, pulsed RC networks will probably be the most feasible. In simulation studies the compensator can be changed easily and quickly on a hybrid computer, and its effect in changing the system's response can be readily seen on an oscilloscope or brush recorder. The elements necessary to simulate the compensator (sample-hold circuits, timing circuits, etc.) can be built into a general purpose analog computer and a simulation made of the complete system. This facilitates PWMS design at a cost that may be lower than digital computer methods.

5-2 Suggestions for Further Research

The PWMS considered in this thesis had a fixed plant of the form,
\[ G(s) = \frac{K}{s(s/a + 1)} \] (5-1)

and it was required that \(1/a\) be large compared to the sampling period in order that the system could be approximated as a PAHS. A more practical transfer function would be

\[ G(s) = \frac{K}{s(s/a + 1)(s/b + 1)} \] (5-2)

where \(b\) is much greater than \(a\). In the analysis of continuous and pulse-amplitude-modulated systems, the effect of the pole at \(b\) is neglected due to its small residue, and the transfer function is taken as equation 5-1. Experimental verification is needed to assure that the effect of poles located far from the \(j\omega\) axis can be neglected when approximating a PWM as a PAHS.

This thesis has considered linear compensation for PWM. The solution proposed is not to be taken as the only possible alternative, but rather as a possible one useful in simulation. Non-linear methods of compensation may be cheaper and assure better performance. A study of non-linear techniques is out of the scope of this thesis, but could well be the basis for further study of PWM.
APPENDIX A

DESCRIPTION OF ASTRAC I

Astrac I is a high speed repetitive analog computer combining analog arithmetic and storage with digital control. The computer comprises six analog modules each containing the following elements:

1. Two electronically reset integrators and their associated switching electronics.
2. Two inverter/summing amplifiers.
3. One comparator amplifier.
4. A potentiometer panel.

For control flexibility, the integrators can be controlled by the computer reset pulse or by a change in d.c. level.

In addition to the analog modules, the computer contains a sample-hold module containing two sample-hold circuits. An oscilloscope and a digital voltmeter are also available for read-out purposes.

The Astrac I digital control unit combines a 10kc crystal oscillator with preset counters and digital circuitry to perform the following operations:

1. Reset the repetitive computer at selectable rates of 100, 50, 25, or 10 cps.
2. Furnish sampling pulses at push-button selected times, $t_1$ and $t_2$, after the start of each individual computer run.

3. Generate scanning pulses, which are advanced by $\Delta$ seconds for each computer run, to provide sampling-type readout of repetitive solutions into slow recorders.

Figure A-1 is a pictorial timing diagram showing the computer reset pulse and the $t_1$ and $t_2$ sampling pulses. When the reset pulse is positive (reset condition), all integrators are reset to their initial conditions. The computer run begins when the reset pulse goes negative (compute condition). At push-button selected times, $t_1$ and $t_2$ seconds after the start of computer run, pulses from the control unit switch the sample-hold circuits, SH-1 and SH-2, into "track" operation. The switching pulses, $t_1$ and $t_2$, can be preset anywhere within the compute period and last from ten to twenty percent of the computer run (which would be from 10 to 20 ms if the computer was being reset at 10 cps.).

It has already been mentioned that the computer has available six analog modules each containing two electronically reset integrators. These integrators can be used as sample-hold circuits by grounding their input terminals and plugging input signals into the initial
Fig. A-1 Timing Diagram

Fig. A-2 Generation of Time Delays
condition jacks. When an integrator is hooked up in this manner, the input signal will be sampled during "reset" and "held" during the compute period. This is useful in the simulation of PAMS and PWMS when a number of synchronous samplers are needed.

Time delays of two sampling periods can be achieved by cascading a sample-hold as described above with SH-1 and SH-2. This is shown in Figure A-2. During reset, the input, e(t), will be sampled. During $t_1$ the output of SH-2 will be sampled and "held" by SH-1. Likewise, e(nT) will be sampled during $t_2$ and "held" by SH-2. When the input is sampled again, the output of SH-2 will be $e(n-1)T$ while the output of SH-1 will be $e(n-2)T$. The output of the first hold-circuit will always be $e(nT)$.

A pulse-width modulator can be simulated on Astrac as shown in Figure A-3. The circuit shown is a voltage comparator with a variable "dead zone". Its input-output characteristic is shown in Figure A-4. The boundaries of the "dead-zone", $\delta_1$ and $\delta_2$, are controlled by potentiometers, $P_1$ and $P_2$, while the output magnitude, $E$, is controlled by potentiometers, $P_3$ and $P_4$. Pulse-width modulation is achieved by summing the sampled input, $x(nT)$, with the output of a "sweep" circuit (The "sweep" waveform can be generated by applying a voltage $+V$ to the input of a resetable integrator, and a voltage $-2V/T$ to the initial condition jack of the same integrator). The comparator
Fig. A-3 Simulation of a Pulse-Width Modulator
Fig. A-4 Characteristic of a Comparator With a "Dead Zone"
circuit will have an output whenever the sum of the input and the sweep voltage is greater than $\delta_1$ or less than $\delta_2$.

Demodulation of a PWM signal has been discussed in Chapter 3. This can be accomplished by driving a resetable integrator with the signal and sampling the output of the integrator with a sample-hold circuit driven by $t_2$. In this case, $t_2$ should be set as close as possible to the end of the compute period. For further information concerning Astrac, the interested reader is referred to "The Design, Development and Applications of the Astrac Computer" by T. A. Brubaker (13).
APPENDIX B

EXPERIMENTAL DATA

CLOSED LOOP STEP RESPONSE FOR $G(z) = \frac{0.22(z + 0.845)}{(z - 1)(z - 0.671)}$

$T = .1$ second

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### Step Response of Compensated System

\[ T = 0.1 \text{ second} \]

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