A NOVEL
TUNNEL DIODE CIRCUIT

by
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STATEMENT BY AUTHOR

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ABSTRACT

This thesis shows how the volt-ampere characteristics of four tunnel diodes can be combined in a circuit so that the resulting composite volt-ampere characteristic exhibits three positive resistance regions. A method of constructing the composite volt-ampere characteristic from the characteristics of the individual diodes is shown and a design procedure which maximizes certain parameters of the composite characteristic is derived. The load limitations are considered in terms of the desired mode of operation and the required quasi-stable states. Two applications of the circuit are shown, a ternary cell and a bipolar pulse generator, which illustrate how the static and dynamic load lines can be used in a particular situation and how the piecewise linear model of the composite characteristic can be used in the necessary calculations.
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Chapter 1

INTRODUCTION

This thesis is concerned with the design and application of a tunnel diode circuit. The circuit combines the volt-ampere characteristics of four tunnel diodes in such a way that the resulting composite volt-ampere characteristic exhibits three positive resistance regions separated by two negative resistance regions.

The basic element of the circuit, the tunnel diode, is a two terminal device with a volt-ampere characteristic having two positive resistance regions as shown in figure 1. Although much effort has been devoted to the application of this device, its use has been relatively limited due to the temperature dependence.

Figure 1.1 Tunnel Diode Characteristic
of the forward conduction region. To alleviate this problem, two tunnel diodes have been combined in such a manner that the volt-ampere characteristic of the resulting two-terminal circuit still exhibits two positive resistance regions as shown in figure 1.2 and, in addition, the positive resistance regions are much less temperature dependent than the forward conduction regions of the tunnel diodes. This circuit is then used in much the same way that the single tunnel diode was used.

This particular method of combining the volt-ampere characteristics of tunnel diodes has been used primarily to improve the temperature characteristics of the bistable element. It is the purpose of this thesis to extend this method to a circuit which utilizes four tunnel diodes in such a way that the resulting volt-ampere characteristic exhibits three positive resistance regions separated by two negative resistance regions as shown in figure 1.3. The positive resistance regions are still much less temperature
dependent than the forward conduction regions of the tunnel diodes used in the circuit and, since the characteristic exhibits one more positive resistance region, several new applications are possible.

It should be noted that this method of combining volt-ampere characteristics is not limited to tunnel diodes, but can be applied to other nonlinear devices to generate multistable circuits. For example, two devices which could be used in a similar manner are the four-layer diode and the avalanche transistor.

It is possible to generate a similar volt-ampere characteristic by simply connecting two tunnel diodes in series, but the circuit has limited application for two reasons. First, the magnitudes of the current peaks cannot be specified independently. Second, the resulting volt-ampere characteristic actually has four positive resistance regions and only appears to have three because two of these regions lie approximately on top of one another.

Thus, some ambiguity results in defining one of the positive resistance regions if the diodes are not ideally matched. The circuit

![Four-Diode Characteristic](image-url)
described in this thesis is not so limited because it has a unique volt-ampere characteristic and the various peaks can be specified independently.

This thesis is concerned with only the low-frequency aspects of the four-diode circuit. High-frequency considerations such as rise times and trigger requirements for the two-diode circuit have been extensively treated in a paper by Morgan, and that analysis can be easily extended to the four-diode circuit.

The development of this thesis proceeds as follows:

1. A method for constructing the composite volt-ampere characteristic of the four diode circuit from the volt-ampere characteristics of the individual diodes is described. Several regions and critical parameters of the composite characteristic are defined and the values of these critical parameters are calculated in terms of the parameters of the basic circuit elements. A design procedure is then shown which maximizes certain parameters of the composite volt-ampere characteristic. Finally, to facilitate calculations using the composite volt-ampere characteristic, a piecewise linear model of the characteristic is defined.

2. The various possible modes of operation are defined by extending the definitions of a bistable element. The general loading problem is then discussed in terms of the desired mode of operation.
3. Two possible applications of the four-diode circuit are shown: a ternary cell and a bipolar pulse generator. For the ternary cell, a simple biasing circuit is shown and a method of driving the operating point from one stable state to another is discussed. It is then shown how the circuit can be made to count by threes. For the bipolar pulse generator, the necessary biasing is shown and the durations of the various pulses are calculated. A slightly more complicated biasing network which eliminates the recovery time is shown.
Chapter 2

THE COMPOSITE VOLT-AMPERE CHARACTERISTIC

2.1 INTRODUCTION

This chapter is concerned with the volt-ampere characteristic of the four-diode circuit. The composite characteristic is constructed from the characteristics of the individual diodes; important parameters of the composite characteristic are calculated in terms of the parameters of the individual diodes; a design procedure which maximizes certain parameters is shown; and the final composite volt-ampere characteristic is approximated with a piecewise linear model.

2.2 CONSTRUCTION OF THE VOLT-AMPERE CHARACTERISTIC

To construct the volt-ampere characteristic of the four-diode circuit, the characteristics of three sub-circuits are considered first and then these characteristics are combined to form the composite characteristic. The three sub-circuits are shown in figure 2.1 as sections A, B, and C of the four diode circuit.

The volt-ampere characteristics of sections A and C are
simply the volt-ampere characteristics of those particular diodes

![Four-Diode Circuit Diagram]

Figure 2.1 Four-Diode Circuit

displaced along the voltage axis an amount equal to the supply voltage, $E$, as shown in parts a and b, respectively, of figure 2.2.

![Characteristics of Sections A and C]

Figure 2.2 Characteristics of Sections A and C

The volt-ampere characteristic of section B is only slightly more complicated. For a series circuit, the total voltage at any given current is the sum of the voltages across the individual diodes. Thus, the characteristic of section B is constructed from the characteristics of diodes 2 and 3 as shown in figure 2.3.
The composite characteristic of the complete circuit can now be constructed by considering the parallel connection of these three basic circuits. In a parallel connection, the composite characteristic is constructed by noting that the total current at any given voltage is equal to the sum of the currents in each branch. Thus, the composite characteristic is constructed from the characteristics of sections A, B, and C as shown in figure 2.4.

Figure 2.3 Characteristic of Section B

Figure 2.4 The Composite Characteristic

Note that each peak of the composite characteristic is
primarily dependent upon the peak region of one tunnel diode in the circuit. Since the peak regions of the diodes are much less temperature dependent than the valley regions, the composite characteristic is also relatively temperature independent. Also, note that the magnitudes of the current peaks are dependent upon the placement of the diodes and consequently the magnitude of the supply voltage. Shown in figure 2.5 is the composite characteristic for three values of supply voltage. Although the exact

![Composite Characteristic With Supply Variations](image)

Figure 2.5 Composite Characteristic With Supply Variations

can be seen that a point is reached where the magnitudes of the two outer peaks are maximized. Also, it can be seen that the magnitudes of the two inner peaks are relatively unaffected by variations in the supply voltage. Thus, the magnitudes of the peaks are dependent upon the supply voltage; however, it will be shown later that the dependence of the peaks on the supply voltage can be used advantageously in pulse circuits.
2.3 CHARACTERIZATION OF THE VOLT-AMPERE CHARACTERISTIC

It has been qualitatively shown how the composite volt-ampere characteristic is constructed from the characteristics of the individual diodes. The values of some of the critical parameters of the composite characteristic can now be calculated in terms of the parameters of the individual diodes.

For most practical applications, it is convenient to characterize the composite volt-ampere characteristic of the four-diode circuit by seven critical points and five regions. The critical points of the composite characteristic are the coordinates of the four peaks and the points at which the positive resistance regions intersect the voltage axis. The peaks are numbered from right to left, starting with peak 1, and the coordinates of the i'th peak will be denoted by \((I_{pi}, V_{pi})\). Similarly, the three points at which the positive resistance regions intersect the voltage axis are numbered from right to left as \(V_{c1}^{+}, V_{c2}^{+}\), and \(V_{c3}^{+}\). The various regions of the composite characteristic are the reverse, center, and forward positive resistance regions and the reverse and forward negative resistance regions. These points and regions are shown in figure 2.6.

Each of the critical points is, of course, dependent upon
the exact volt-ampere characteristic of the individual diodes used in the circuit, but the manufacturer does not usually specify the complete characteristic. Instead, several of the important points of the volt-ampere characteristic are usually specified, such as the coordinates of the peak point, \((I_p, V_p)\), the coordinates of the valley point, \((I_v, V_v)\), the forward voltage, \(V_{fp}\), and the reverse voltage, \(V_r\), where the forward and reverse voltages are measured at a current equal in magnitude to the peak current. These parameters are shown in figure 2.7. Thus, to determine the critical points of the composite characteristic using the manufacturers data sheets, one must specify these critical points in terms of the given tunnel diode parameters.

To calculate the critical points, we first consider the
current coordinate of peak 1. In the ideal case, the peak of

tunnel diode 1 is positioned directly under the valley point of tunnel diode 4 and the effective valley point of the series combination of diodes 2 and 3 as shown in figure 2.8. For this condition, the current coordinate of peak 1 is given by

\[ I_{P1} = -I_{P1} + I_{VT02} + I_{VT04} \]  \[ 2.1 \]
This value is correct for the ideal condition shown, but it is shown in the following section that this condition can only be achieved for "ideally matched" diodes. Thus, equation 2.1 gives the maximum value for the current coordinate of peak \( I \).

A minimum value for the magnitude of peak \( I \) for a given supply voltage can be found by approximating each of the diodes in the circuit with the piecewise linear model shown in figure 2.9.

![Piecewise Linear Model of Tunnel Diode](image)

The resulting composite piecewise linear model for the combination of diodes 2, 3, and 4 is shown in figure 2.10.

Assume that the peak of tunnel diode 1 is positioned between points \( a \) and \( b \), and that the valley point of diode 4 is to the left of the valley point of diode 2 as shown in figure 2.10. For this particular situation, the current coordinate of point \( A \)
is given by

$$I_A = I_{VT02} + \left[ \frac{V_{VT02} + I_{VT02} R_{RTD3} - (-E + V_{VT04})}{R_{RTD4}} \right]$$  \[2.2\]

and of point B is given by

$$I_B = I_{VT04} + \left[ \frac{V_{VT02} + I_{VT02} R_{RTD3} - (-E + V_{VT04})}{R_{RTD2} + R_{RTD3}} \right]$$  \[2.3\]

Thus, if

$$I_A > I_B$$  \[2.4\]

then

$$|I_{Pl}| > I_{PTD1} - I_A$$  \[2.5\]

Otherwise,

$$|I_{Pl}| > I_{PTD1} - I_B$$  \[2.6\]

One of these two values then gives the minimum value for the
magnitude of peak 1.

The voltage coordinate of peak 1, $V_{pl}$, is primarily dependent upon the supply voltage, $E$, and the peak voltage of tunnel diode 1, $V_{pTD1}$, but it is also somewhat dependent upon the other three diodes in the circuit. In particular, tunnel diodes 2, 3, and 4 combine to form an effective resistance in parallel with tunnel diode 1. If diode 1 is ideally positioned under the valley point of diode 4 and the effective valley of diodes 2 and 3, the parallel resistance is infinite and the resulting voltage coordinate is

$$V_{pl} = E - V_{pTD1}$$

In the practical case, however, it will probably not be possible to "ideally" position diode 1 and some parallel resistance will result.

The voltage shift due to the shunt resistance is dependent upon the "roundness" of the peak region of the diode. If the piecewise linear model shown previously is assumed, the voltage shift is zero. On the other hand, if the peak region of the diode can be approximated by a parabola centered at $(I_{pTD1}, V_{pTD1})$ and going through the origin, the voltage shift is then equal to

$$V_{SHFT} = \frac{V_p^2}{2R_a}$$

where $R_a$ is the resistance in parallel with the tunnel diode.
For this analysis, it is assumed that the voltage shift due to diodes 2, 3, and 4 is negligible and that the voltage coordinate of peak 1 is given by equation 2.7.

The coordinates of peak 2 are calculated in a similar manner. Tunnel diodes 1 and 4 are first approximated by their piecewise linear models and then are combined to form a composite piecewise linear model as shown in figure 2.11. Note, that at the origin, the effective resistance is equal to the parallel combination of $R_{nTD1}$ and $R_{nTD4}$. The current coordinate of peak 2 is then given by

$$I_{p2} = I_{PTD2} + \left( \frac{V_{PTD2} + I_{PTD2} R_{RTP3}}{R'_N} \right)$$  \hspace{1cm} (2.9)

where

$$R'_N = \frac{R_{nTD1} R_{nTD4}}{R_{nTD1} + R_{nTD4}}$$  \hspace{1cm} (2.10)
The value determined is neither a maximum nor a minimum but simply an approximate value.

The voltage coordinate of peak 2 is

\[ V_{P2} = V_{P\tau D2} + I_{P\tau D2} R_{n\tau D2} \]  \hspace{1cm} 2.11

where the voltage shift due to \( R_n \) is assumed to be negligible.

The point at which the forward positive resistance region intersects the voltage axis, \( V_{c1} \), can also be found using the piecewise linear model for diodes 2, 3, and 4. As before, assume that the composite characteristic of diodes 2, 3, and 4 is as shown in figure 2.10, and that the intersection point lies somewhere between points A and B. For this condition, the crossover voltage is approximately

\[ V_{c1} = E - I_{A} R_{p\tau D1} \]  \hspace{1cm} 2.12

Since the circuit has been assumed to be symmetrical, \( V_{c2} \) is zero and the coordinates of the other peaks and intersection points can be found by an analysis similar to the preceding one.

Thus, the values of the critical points in terms of the parameters of the individual diodes are given below.

\[ I_{p1} = -I_{P\tau D1} + I_{V\tau D2} + I_{V\tau D4} \]  \hspace{1cm} 2.13
\[ V_{p1} \equiv E - V_{PTD1} \] 2.14

\[ I_{p2} \equiv I_{PTD2} + \left( V_{VT02} + I_{VT02} R_{RTO3} \right) \left( R_{NT01} + R_{NT04} \right) \left( R_{NT01} + R_{NT04} \right) \] 2.15

\[ V_{p2} \equiv V_{PTD2} + I_{PTD2} R_{RTO3} \] 2.16

\[ I_{p3} \equiv - I_{PTD3} + \left( V_{VT03} + I_{VT03} R_{RTO2} \right) \left( R_{NT01} + R_{NT04} \right) \left( R_{NT01} + R_{NT04} \right) \] 2.17

\[ V_{p3} \equiv - V_{PTD4} - I_{PTD4} R_{RTO2} \] 2.18

\[ I_{p4} \equiv I_{PTD4} - I_{VT04} - I_{VT01} \] 2.19

\[ V_{p4} \equiv - E + V_{PTD1} \] 2.20

\[ V_{c1} = E - R_{PTD1} \left[ I_{VT02} + V_{VT02} + I_{VT02} R_{RTO3} - \left( -E + V_{VT04} \right) \right] \] 2.21
2.4 SELECTION OF THE SUPPLY VOLTAGE

The values of the critical points have been calculated and some qualitative understanding of how the placement of the diodes effects the composite characteristic has been obtained. One is now in a position to formulate a design of the circuit.

In section 2.2 it was shown qualitatively that as the supply voltage was varied over a range of values, a point was reached where the magnitude of peaks 1 and 4 were maximized. It was also shown that the supply voltage had relatively little effect on peaks 2 and 3. The optimum supply voltage is then defined as that voltage which maximizes peak 1.

In section 2.3 it was shown that the magnitude of peak 1 was maximum when the peak point of tunnel diode 1 was positioned simultaneously under the valley point of tunnel diode 4 and the effective valley point of diodes 2 and 3. For the first condition,

\[ E = \frac{V_{VTD1}}{2} + V_{VTD4} \]
and for the second condition,

\[ E = V_{VD2} + R_{RTD3} I_{VD2} + V_{PTD1} \]

Now, if diodes 1 and 4 are assumed to be identical and if 
\[ R_{RTD3} I_{VD2} \] is assumed to be negligible, these equations reduce to

\[ V_{VD2} = \frac{V_{PTD1}}{2} \]

Thus, the valley voltage of tunnel diode 1 should be approximately twice as large as the valley voltage of diode 2.

This is not a practical solution, however, since only a very limited number of diodes with different valley voltages are available. By including the source resistance as another parameter, the peak of tunnel diode 1 can be positioned under the valley of tunnel diode 4 and the effective valley of diodes 2 and 3. This is not a practical solution either since increasing the source resistance increases the slope of the two outer positive resistance regions as shown in figure 2.12.

![Figure 2.12 Composite Characteristic Showing Effect of Source Resistance](image-url)
A more practical solution is found by assuming some properties of the valley regions of the tunnel diodes and then, using these assumptions, maximize peak 1. Thus, we assume that the valley regions of all the tunnel diodes are identical in the immediate vicinity of the valley point and that they are approximately symmetrical with respect to their valley points as shown in figure 2.13. The composite characteristic of diodes 2, 3, and 4 exhibits

![Composite Characteristic Diagram](image)

Figure 2.13. Idealized Characteristics of 2, 3, and 4

a minimum at

\[ V_{\text{min}} = \frac{(V_{VT02} + I_{VT02} R_{VT02}) + (-E + V_{VT04})}{2} \]

To maximize peak 1, the peak point of tunnel diode 1 should be positioned under this minimum. Thus,

\[ E - V_{VT01} = \frac{(V_{VT02} + I_{VT02} R_{VT02}) + (-E + V_{VT04})}{2} \]

If the valley voltages of diodes 1 and 4 are equal, this equation...
reduces to

\[ E = \frac{2V_{TR1} + V_{TR2} + I_{TR2}R_{TR2} + V_{TR3}}{3} \quad 2.29 \]

Thus, to position the diodes such that peak 1 is at its absolute maximum, either the diodes have to be ideally matched as given by equation 2.26, or the source resistance has to be included as a variable. To maximize peak 1 for a circuit with a given set of diodes and a fixed source resistance, the supply voltage should be set to the value given by equation 2.29. It should be noted, however, that the valley voltage of diodes 1 and 4 should be approximately twice the valley voltage of diodes 2 and 3. If this is not the case, the two outside peaks will be considerably reduced, and the composite characteristic will be so distorted that its usefulness will be greatly limited.

2.5 A PIECEWISE LINEAR MODEL OF THE VOLT-AMPERE CHARACTERISTIC

After the initial design, the four-diode circuit is described by its composite volt-ampere characteristic, but since the complete characteristics of the individual diodes are not usually available, the characterization further reduces to specifying the approximate coordinates of the critical points. These were
calculated using a piecewise linear model of the individual diodes. It is appropriate, then, that a piecewise linear model of the composite characteristic be defined. Such a model is shown in figure 2.14. The critical points are the values determined in section 2.3 and it is assumed that between these points the composite volt-ampere characteristic can be approximated by linear resist-

![Figure 2.14 Piecewise Linear Model of the Composite Characteristic](image)

ances as shown. This model is the basis for further discussion of the four diode circuit.
Chapter 3

GENERAL LOADING LIMITATIONS

3.1. INTRODUCTION

In the previous chapter it was shown how the composite volt-ampere characteristic of the four-diode circuit is constructed from the characteristics of the individual diodes and how the peaks of the composite characteristic can be maximized by properly selecting the supply voltage. Before considering some practical applications of the four-diode circuit, some general aspects will be considered. In particular, the various modes in which the circuit can operate are defined, and the loading limitations are considered in terms of the mode desired.

3.2. MODES OF OPERATION

The various operating modes for a device such as a tunnel diode which exhibits two positive resistance regions can be defined by considering the static and dynamic load lines which, in turn, determine the stable and quasi-stable states. The static load line is determined by the d-c or steady state resistive load. Since the natural frequencies of the load circuit are assumed to be much
larger than those of the device, a dynamic load line is defined as the a-c coupled resistive load. A stable state is then defined as a point where the static load line intersects a positive resistance region and a quasi-stable state is defined as a point where the dynamic load line intersects a positive resistance region. The operating mode is defined from the number of stable states and it is tacitly assumed that the circuit is quasi-stable in the remaining positive resistance regions. Thus, if the static load line intersects only one positive resistance region, the circuit is termed monostable.

When the definition is extended to the four-diode circuit, however, some confusion can arise. For example, consider the particular characteristic shown in figure 3.1. If an inductor is connected in parallel with the circuit, the static load line coincides with the current axis and the dynamic load line coincides with voltage axis. By extending the previous definitions, this circuit would seem to be monostable. If the operating point
is pulsed to one of the quasi-stable states, however, it will continue to switch from the forward to the reverse positive resistance region and back again, giving the external characteristics of an astable circuit.

The problem then resolves itself into defining the mode from either the static load line or from the external characteristics of the circuit. In this case, the mode will be defined from the static load line viewpoint. The circuit is then termed astable, monostable, bistable, or tristable, corresponding to the number of times the static load line intersects the positive resistance regions.

3.3 LOAD LIMITATIONS

(a) Resistive Load Circuits

The load limitations are determined by the desired operating mode. Consider a resistive load connected as shown in figure 3.2. The slope of the load line, and thus the value of the

![Figure 3.2 Resistive Load](image-url)
resistance, determines the particular mode of the circuit. For zero resistance, the load line intersects the composite characteristic only at the origin and monostable operation results. As the resistance is increased, a critical value is reached where the load line intersects another positive resistance region, making the circuit bistable. As the resistance is increased still more, another positive resistance region is intersected and tristable operation results. If the magnitude of peak 1 is greater than the magnitude of peak 4, the following limits are placed on the load resistance for a given mode:

Monostable: \[ R_L < -\frac{V_{p1}}{I_{p1}} \]  \( 3.1 \)

Bistable: \[ -\frac{V_{p1}}{I_{p1}} < R_L < -\frac{V_{p4}}{I_{p4}} \]  \( 3.2 \)

Tristable: \[ -\frac{V_{p4}}{I_{p4}} < R_L \]  \( 3.3 \)

If the magnitude of peak 1 is less than the magnitude of peak 4, the load limitations for a given mode are:

Monostable: \[ R_L < -\frac{V_{p4}}{I_{p4}} \]  \( 3.4 \)

Bistable: \[ -\frac{V_{p4}}{I_{p4}} < R_L < -\frac{V_{p1}}{I_{p1}} \]  \( 3.5 \)

Tristable: \[ -\frac{V_{p1}}{I_{p1}} < R_L \]  \( 3.6 \)
(b) Resistive Loads Containing Sources

Now consider an active load which can be represented by its Norton equivalent circuit as shown in figure 3.3. Many different limitations can be obtained depending upon the relative magnitudes of the peaks and the Norton equivalent current generator. For example, assume that the current is positive in the direction shown and that peak 2 is smaller than peak 4 as shown in figure 3.4. For this particular case, five different
results can be obtained depending upon the magnitude of the current generator. For example, if the magnitude of the current generator, $I_0$, lies in region 5 as shown, two critical values for the Norton equivalent resistance exist. Thus, three regions can be defined: one for monostable operation, one for bistable operation, and one for tristable operation. If the current lies in another region, different limitations are imposed on the load resistance. All of the various possibilities will not be shown, but it is assumed that the reader can extend the method to any desired case.

(c) Load Circuits Containing Reactive Elements

To complete the discussion of loading, the two reactive load circuits shown in figure 3.5 are considered. Note that for these circuits the static and dynamic load lines do not coincide and thus quasi-stable states can result. It is assumed that the time constants of the two circuits are large compared to the switching speed of the four-diode circuit, and thus the dynamic load line appears stationary during the switching time.

![Figure 3.5 Reactive Load Circuits](image-url)
The values of the resistors are determined by the required slopes of the static and dynamic load lines. For the inductive circuit, the slope of the dynamic load line is determined by $R_1$ and the slope of the static load line is determined by $\frac{R_1 R_2}{R_1 + R_2}$. Thus for the inductive circuit, the slope of the static load line is greater than the slope of the dynamic load line.

For the capacitive circuit, however, the slope of the dynamic load line is determined by $\frac{R_3 R_4}{R_3 + R_4}$ and the slope of the static load line is determined by $R_3$, and thus the slope of the dynamic load line is greater than the slope of the static load line.

Therefore, for applications where the slope of the static load line is required to be greater than the slope of the dynamic load line, the inductive loading circuit is used and for the cases where the opposite slopes are required, the capacitive load is used. The active elements in both cases are determined by the time constant required in the particular application.

Thus, any combination of linear, single time constant load lines can be implemented using one of these two circuits.
Chapter 4

APPLICATIONS

4.1 A TERNARY CELL

Mackay and MackIntyre\(^2\) have shown how primitive tristable elements can be incorporated in ternary counters and Lowenschuss\(^3\) has formulated a switching algebra for ternary systems. The purpose of this section is to discuss a primitive ternary element which can be used in such systems.

(a) Introduction.

A ternary cell requires a circuit which has three stable states. Thus, to employ the four-diode circuit in such a system, the tristable mode must be used and the static load line must intersect all three positive resistance regions. A simple implementation of this is a linear resistor connected in parallel with the four-diode circuit, where the resistance is greater than both \(-V_{pl}/I_{pl}\) and \(-V_{p4}/I_{p4}\). Such a circuit and the resulting volt-ampere characteristic is shown in figure 4.1. The stable operating points are points \(a\), \(b\), and \(c\).
The operating point can be switched from one stable state to another by the application of a suitable current pulse. For example, assume that the operating point is at point \( b \) and a positive current pulse is applied to the circuit as shown in figure 4.2. With the application of the current pulse, the operating point moves up the center positive resistance region. If the magnitude of the current pulse is sufficient to drive the operating point over peak 2, the operating point will enter the forward negative resistance region and regenerate to the forward positive resistance region. When the current pulse is removed, the operating point then moves to stable state \( c \).
The magnitude of the current pulse required can be determined by using the piecewise linear model of the composite volt-ampere characteristic. When the operating point is in the center positive resistance region, the four-diode circuit can be represented by a linear resistor, $R_c$. Thus, the equivalent circuit for the load, the four-diode circuit, and the trigger generator is as shown in figure 4.3. The current through the four-diode circuit is then equal to

$$I_{FOC} = \frac{I R_c}{R_L + R_c}$$  \hspace{1cm} (4.1)$$

When the current through the four-diode circuit reaches $I_{p2}$, the operating point regenerates to the forward positive resistance region. Thus, the required trigger current is

$$I_{T2} = \frac{I_{p2}(R_L + R_c)}{R_L}$$  \hspace{1cm} (4.2)$$

By a similar reasoning, it can be shown that the magnitude of trigger current required to pulse the circuit from state a over peak 4 is

$$I_{T4} = \frac{I_{p4}(R_L + R_c) + V_L}{R_L}$$  \hspace{1cm} (4.3)$$

Figure 4.3 Equivalent Circuit for Calculating Required Trigger Current
When the operating point is to be pulsed over peak 1 from state \( c \) or over peak 3 from state \( b \), a negative trigger pulse is required. Otherwise, the analysis is essentially the same. Thus, the trigger current required to pulse the operating point over peak 1 from state \( c \) is

\[
I_{T1} = \frac{I_{P1}(R_L + R_F) + V_{C1}}{R_L}
\]

and that required to pulse the operating point over peak 3 from state \( b \) is

\[
I_{T3} = \frac{I_{P3}(R_C + R_L)}{R_L}
\]

The four-diode circuit can then be used as a storage element in a ternary logic system in the same way that a single tunnel diode is used as a storage element in a binary system. The inputs are current pulses of differing magnitudes and polarities depending upon which state the circuit is to be driven to, and the output is the voltage across the four-diode circuit.

(b) Standardization of the Magnitude of the Trigger Pulse

By properly choosing the static load line, the dynamic load line, and the magnitude of peak 2, the same magnitude and polarity of pulse can be used to shift the operating point from state \( b \) to state \( c \) as is required to shift the operating point from state \( a \) to state \( b \). For example, consider the case shown
in figure 4.4, where the static load line still intersects all three positive resistance regions, but the slope of the dynamic load line is greater than the slope of the static load line. Furthermore, assume that the dynamic load line is such that quasi-stable states $d$, $e$, and $f$ exist. The magnitude of trigger current necessary to pulse the operating point from stable state $a$ over peak 4 is

$$I_{Ta} = \frac{I_p(\frac{1}{R_p + R_s} + V_{c3})(\frac{1}{R_R + R_D})}{(R_R + R_s) R_D}$$ 4.6

and the trigger current necessary to pulse the operating point from quasi-stable state $d$ over peak 2 is

$$I_{Td} = \frac{I_p (R_c + R_D)(R_i + R_R) - (R_s + R_D)V_{c3}}{R_D (R_s + R_R)}$$ 4.7

If $I_{Ta}$ is less than $I_{Td}$, and the actual trigger current is less than $I_{Td}$ and greater than $I_{Ta}$, the operating point will move up the reverse positive resistance region, over peak 4, and then regenerate to the center positive resistance region. With the
removal of the trigger pulse, the operating point moves to quasi-stable state d. The circuit then "recovers" as the operating point moves to stable state b. The trigger current necessary to pulse the operating point over peak 2 from state b is

\[ I_{Ta} = \frac{I_{P2}}{R_c} \frac{R_c}{(R_c + R_D)} \]  

Thus, any trigger pulse which is larger than \( I_{Ta} \) and \( I_{Tb} \), but less than \( I_{Td} \), can be used to pulse the operating point from state a to state b or from state b to state c. This combination of load lines does not, however, standardize the polarity of the trigger pulse since a negative trigger is still necessary to pulse the operating point from state c over peak 1 or from state b over peak 3.

(c) A Ternary Counting Element

In the previous section, the dynamic load line was used to standardize the magnitude of the required trigger pulse. In this section, the dynamic load line will be used in such a way that the resulting circuit can be used to count by threes. Assume that the static load line still intersects all three positive resistance regions and, in addition, assume that the dynamic load line has zero slope. Furthermore, assume that the magnitude of peak 2 is greater than the magnitude of peak 4 and the magnitude of peak 1 is greater than the magnitude of peak 3. Such a volt-
ampere characteristic and a circuit which generates the required static and dynamic load lines are shown in figure 4.5. The operating point can still be pulsed from stable state a to stable state b with the application of a positive current pulse if the magnitude of the current pulse is greater than $I_{p4} - I_a$ and less than $I_{p2} - I_a$, and from stable state b to the forward positive resistance region with a positive pulse having a magnitude greater than $I_{p2}$. However, the operating point regenerates directly to state a from state c with the application of a negative current pulse having a magnitude greater than $I_c - I_{p1}$. If operating point a is then designated 0, point b designated 1, and point c designated 2, the circuit will count if the proper sequence of positive and negative pulses is applied.

One of the disadvantages of the counting element is the extremely large pulse necessary to switch the operating point from state b to the forward positive resistance region. The required trigger current can be reduced by using the nonlinear load line.

![Diagram](image-url)
shown in figure 4.6 which can be generated with a semiconductor diode biased as shown in figure 4.7. The slope of the dynamic load line is still zero and thus the circuit will regenerate directly to the reverse positive resistance region from state c if

The magnitude of peak 3 is less than the magnitude of peak 1.

(d) Other Methods of Triggering

A further disadvantage of the counting circuit is that the proper sequence of positive and negative pulses must be available. It would be desirable if the circuit could be made to count
pulses all of the same magnitude and polarity. This can be accomplished by using some of the interior nodes of the circuit to trigger the circuit from one state to another.

As was shown in chapter 2, the supply voltages can be used to change the magnitudes of the peaks of the composite volt-ampere characteristic. In particular, an optimum point is reached where the magnitudes of the two outer peaks are maximum. If the supply voltage is greater than this optimum value, the magnitudes of the two outer peaks are reduced but the magnitudes of the two inner peaks are increased. If the supply voltage is less than the optimum value, however, both the outer peaks and the inner peaks are reduced. The circuit can thus be triggered from one stable state to another by applying a voltage pulse to each of the supplies.

It has been shown how the dynamic load line can be used to standardize the pulse magnitude. In particular, it was shown that the slope of the dynamic load line must be greater than the slope of the static load line at points a and b if pulses with constant magnitudes are to be used. However, to be able to pulse the operating point directly from state c to state a, the slope of the static load line must be greater than the slope of the static load line at point c. Because of these two conflicting requirements, two reactive elements must be used to generate the proper combination of static and dynamic load lines.

Let the desired dynamic load line have a slope of $1/R_d$
as shown in figure 4.8. The particular combination of load lines shown can be generated using the load circuit shown in figure 4.9. It is assumed that the inductor current and the capacitor voltage remain constant during the switching time and thus

\[
C > \frac{L \left[ (M + R_L^2) + \frac{R_\Phi \sqrt{M + R_E^2}}{M^2} \right]}{M}
\]

\[M = \left( R_L R_c + R_L R_R + R_R R_c \right)\]

The restriction on \( C \) forces the circuit to be overdamped. This is desirable because if the circuit is underdamped, the current
through the four-diode circuit oscillates and could exceed $I_{p4}$, causing the operating point to regenerate to the center positive resistance region.

4.2 A BIPOLAR PULSE GENERATOR

(a) Introduction

It was shown in the previous section how the tristable mode can be used as a ternary storage element. In this section, it is shown how the monostable mode can be used to generate the bipolar voltage pulse shown in figure 4.10.

An application for such a pulse occurs in the read-write sequence of a tunnel diode memory. A "word" is stored in a particular group of cells within the memory, and to read this word out of the memory, each of these cells is pulsed to a particular state. If a particular cell is already in that state, no switching
occurs, but if the cell is in the opposite state, it will switch states. This switching is detected and the original state of the cell is determined by the presence or absence of switching. One of the disadvantages of this method of reading out of the memory is that all of the cells are pulsed to the same state and thus the information originally stored in that particular group of cells is destroyed. The purpose of the bipolar pulse shown is to first read out of the memory with the positive pulse and then to rewrite the information with the negative pulse.

To generate the pulse, the volt-ampere characteristic of the four-diode circuit is first altered by using diodes with suitable peak current ratings such that peak 2 is larger than peak 4 and peak 1 is larger, in magnitude, than peak 3. An inductor is then connected in parallel with the circuit. If the internal resistance of the inductor is negligible, the static load line coincides with the current axis. Since the static load line intersects the characteristic only at the origin, the circuit is monostable. The dynamic load line coincides with the voltage axis, however, and thus two quasi-stable states are generated. The circuit and corresponding volt-ampere characteristic are shown in figure 4.11.

When a current pulse of sufficient magnitude and duration is applied to the circuit as shown in figure 4.12, the operating point moves up the center positive resistance region, over peak 2, and regenerates to the forward positive resistance region. If the trigger pulse is sufficiently short such that the inductor current
remains negligible during the application of the pulse, the operating point moves to quasi-stable state \( a \) with the removal of the trigger pulse. Since a positive voltage is now applied across the inductor, the current in the inductor increases and the operating point moves down the forward positive resistance region until it reaches peak 1. At this time, the operating point switches to the reverse positive resistance region at point \( b \). A negative voltage is now applied across the inductor. The operating point moves up the reverse positive resistance region until it reaches peak 4 at which time it switches to the center positive resistance region at point \( c \). The current in the inductor then decays exponentially.
as the operating point moves down the center positive resistance region to the stable operating point at the origin.

(b) Pulse Duration and Recovery Time

The positive pulse duration, the negative pulse duration, and the recovery time of the bipolar pulse generator can be calculated by approximating the nonlinear volt-ampere characteristic with the piecewise-linear model discussed in chapter 2. During the time the operating point is in the forward positive resistance region, the nonlinear circuit can be represented by the linear equivalent circuit shown in figure 4.13. The initial current through the inductor is zero, the final value is \( V_{Cl}/R_F \), and the time constant is \( L/R_F \). Thus, the current through the inductor is given by

\[
I_L = \frac{V_{Cl}}{R_F} \left( 1 - e^{-\frac{-t}{L/R_F}} \right)
\]

When the current through the inductor reaches \( I_{pl} \), the operating point enters a negative resistance region, regeneration occurs,
and the operating point moves to the reverse positive resistance region, ending the positive pulse. Thus, if \( t_1 \) designates the duration of the positive pulse,

\[
I_{p1} = \frac{V_c}{R_F} \left( 1 - e^{-\frac{t_1 R_F}{L}} \right)
\]

and thus

\[
t_1 = \frac{L}{R_F} \log_e \left( \frac{V_c}{V_c - I_{p1} R_F} \right)
\]

The duration of the negative pulse is calculated in a similar manner. The initial current in the inductor is \( I_{p1} \), the final value is \( \frac{V_C}{R} \), and the time constant is \( L/R \). Thus, the duration of the negative pulse, \( t_2 \), is

\[
t_2 = \frac{L}{R} \log_e \left( \frac{I_{p1} R - V_c}{I_{p1} R - V_C} \right)
\]

The recovery time is the time required for the current in the inductor to decay to a negligible value after the termination of the negative pulse. For the circuit shown, the inductor current approaches zero exponentially with a time constant of \( L/R_c \). The recovery time is defined as three such time constants, since the inductor current has decayed to 8 percent of its initial value after this time. Thus, if \( t_3 \) designates the recovery time,

\[
t_3 \approx \frac{3L}{R_c}
\]
(c) Effect of the Inductor Resistance

In the preceding analysis it has been assumed that the internal resistance of the inductor is negligible. In some practical cases, however, this assumption is not valid and the resistance must be considered. The resistance has two effects on the operation of the circuit. First, the static load line may intersect more than one positive resistance region and the circuit ceases to be monostable. As was shown in chapter 3, the internal resistance of the inductor must be less than both \(-V_{p1}/I_{p1}\) and \(-V_{p4}/I_{p4}\) for the circuit to remain monostable. Second, the duration of the pulses and the recovery time are dependent upon the inductor resistance. When the resistance is included in the calculations for the pulse durations and the recovery time, the following modified equations result:

\[ t_1' = \frac{L}{R_E + R_L} \ln \left( \frac{V_{c1}}{V_{c1} - \frac{I_{p1}}{I_{c1}}(R_E + R_L)} \right) \quad 4.15 \]

\[ t_2' = \frac{L}{R_R + R_L} \ln \left( \frac{\frac{I_{p1}}{I_{c1}}(R_R + R_L) - V_{c3}}{\frac{I_{p4}}{I_{c4}}(R_R + R_L) - V_{c3}} \right) \quad 4.16 \]

\[ t_3' = \frac{3L}{R_R + R_L} \quad 4.17 \]
(d) Recovery Time Elimination

One disadvantage of this method of generating bipolar pulses is that if the circuit is pulsed again before the inductor current is negligible, the duration of the positive pulse will be increased.

This recovery time can be eliminated by shifting the static load line such that the stable state is located at point $c^\ast$. The operating point then regenerates directly to the stable state from the reverse positive resistance region. The active load shown in Figure 4.14 can be used for this purpose. In the stable state, the current through the four diode circuit is

$$I_{DC} = \frac{I R_L}{R_C + R_L}$$  \hspace{1cm} 4.18

For the recovery time to be eliminated, this current should be

![Figure 4.14 Circuit for Eliminating Recovery Time](image)

be equal to $I_{p4}^\ast$, and thus the current generator should be set to

$$I = \frac{I_{p4}^\ast (R_L + R_C)}{R_L}$$  \hspace{1cm} 4.19
These two applications, the ternary cell and the bipolar pulse generator, have shown how the static and dynamic load lines can be combined to perform useful functions, and how the piecewise linear model is useful for calculating trigger requirements and pulse durations.

4.3 A PRACTICAL CIRCUIT

Since the two small voltage sources required to bias the four-diode circuit are not readily available, it is convenient to generate the necessary voltages with the biasing circuit shown in figure 4.15.

![Figure 4.15 A Practical Circuit](image)

The four-diode circuit with the biasing networks replaced by their Thevenin equivalent circuits is shown in figure 4.16. The two equivalent source resistances will affect the composite characteristic, but if they are small compared to $V_{PTD1}/I_{PTD1}$, their effect can be neglected. If the source resistances are not small compared to $V_{PTD1}/I_{PTD1}$, they can be included in the construction.
of the composite volt-ampere characteristic by modifying the volt-
ampere characteristics of diode 1 and 4 as shown in Figure 4.17,

\[ R = \frac{R_L R_S}{R_L + R_S} \]
\[ E' = \frac{E R_L}{R_L + R_S} \]

Figure 4.16 Equivalent Practical Circuit

and then using the modified characteristic in the construction of
the composite characteristic.

4.4 EXPERIMENTAL RESULTS

Shown in figure 4.18 is the measured volt-ampere characteristic of an experimental four-diode circuit. Only the positive resistance regions are evident because the sweep generator is essentially a current source and thus, as the operating point
moves over a peak, it regenerates directly to the following positive resistance region. The parameters of the various diodes

Vertical Scale: 5 milliamperes/cm
Horizontal Scale: 200 millivolts/cm

Figure 4.18 Experimental Volt-Ampere Characteristic

used in the circuit are given in table 1.

<table>
<thead>
<tr>
<th>Type</th>
<th>Diode 1</th>
<th>Diode 2</th>
<th>Diode 3</th>
<th>Diode 4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Gallium Arsenide</td>
<td>Germanium</td>
<td>Germanium Arsenide</td>
<td></td>
</tr>
<tr>
<td>Peak Current</td>
<td>5.0 mA</td>
<td>10.0 mV</td>
<td>2.2 mV</td>
<td>5.0 mV</td>
</tr>
<tr>
<td>Peak Voltage</td>
<td>100 mV</td>
<td>60 mV</td>
<td>60 mV</td>
<td>100 mV</td>
</tr>
<tr>
<td>Valley Current</td>
<td>0.5 mA</td>
<td>1.3 mV</td>
<td>0.29 mV</td>
<td>0.5 mA</td>
</tr>
<tr>
<td>Valley Voltage</td>
<td>450 mV</td>
<td>350 mV</td>
<td>350 mV</td>
<td>450 mV</td>
</tr>
<tr>
<td>Forward Voltage</td>
<td>980 mV</td>
<td>500 mV</td>
<td>500 mV</td>
<td>980 mV</td>
</tr>
<tr>
<td>Reverse Voltage</td>
<td>--</td>
<td>30 mV</td>
<td>20 mV</td>
<td>--</td>
</tr>
</tbody>
</table>

Table 1. Parameters of Tunnel Diodes Used in Experimental Circuit
The particular circuit whose volt-ampere characteristic is shown in figure 4.16 was used to generate the bipolar voltage pulse shown in figure 4.19. In the lower picture, the circuit was completely recovered before it was pulsed again, whereas in the upper picture, the circuit was pulsed again before it had recovered and thus the duration of the positive pulse is increased.

![Graph showing voltage pulses with specifications](image)

**Vertical Scale:** 0.5 Volts/Division  
**Horizontal Scale:** 50 Microseconds/Division  
**Repetition Rate of Upper Pulse:** 2.8 KC  
**Repetition Rate of Lower Pulse:** 280 CPS  
**Inductance:** 10.7 Milliheneries

**Figure 4.19 An Experimental Low-Frequency Bipolar Pulse**

A high-frequency bipolar pulse is shown in figure 4.20. Note that the pulse is considerably more rounded and thus the time constant of the dynamic load is approaching the switching speed of the device.
Vertical Scale: 0.5 Volts/Division

Horizontal Scale: 1 Microsecond/Division

Repetition Rate of Upper Pulse: 1.75 MC

Repetition Rate of Lower Pulse: 175 KC

Inductance: 11. Microhenries

Figure 4.19 An Experimental High-frequency Bipolar Pulse
In this thesis, a novel tunnel diode circuit has been described. The circuit combines the volt-ampere characteristics of four tunnel diodes in such a way that the resulting composite volt-ampere characteristic exhibits three positive resistance regions connected by two negative resistance regions.

In chapter 2, the composite volt-ampere characteristic of the circuit was developed. A method for constructing the composite volt-ampere characteristic from the volt-ampere characteristics of the individual diodes was shown and some of the parameters of the composite characteristic were calculated using a piecewise linear model of the individual diodes. An optimum supply voltage which maximized the two outer peaks of the composite characteristic was found by assuming certain symmetrical properties of the valley regions of the tunnel diodes. It was then convenient to define a piecewise linear model of the composite volt-ampere characteristic in terms of the parameters which had been calculated.

Some general load limitations were considered in chapter 3. The various modes of operation were defined and it was shown that the load was limited by the desired mode and the required quasi-stable states. Both active and passive loads having both
resistive and reactive elements were analyzed. It was shown that two particular reactive loads can be used to implement many combinations of static and dynamic load lines.

In chapter 4, two particular applications of the four-diode circuit were shown: a ternary cell and a bipolar pulse generator. These two applications were included to illustrate how the static and dynamic load lines can by combined to perform a particular function and how the piecewise linear model can be used in the calculations.

The principal contributions of this thesis are:

1. The development of a novel tunnel diode circuit which exhibits three separate positive resistance regions.
2. The establishment of a bias voltage which maximizes the two outer peaks of the composite characteristic.
3. The development of the load limitations in terms of the desired mode of operation and the required quasistable states.
4. The application of the four-diode circuit to two practical situations: a ternary cell and a bipolar pulse generator.
REFERENCES

