

THE DESIGN OF A MULTIPLYING DIGITAL--TO--ANALOG  
CONVERTER FOR WIDEBAND HYBRID COMPUTATION

by

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## TABLE OF CONTENTS

	Page
LIST OF ILLUSTRATIONS . . . . .	v
LIST OF TABLES . . . . .	vi
ABSTRACT . . . . .	vii
INTRODUCTION . . . . .	1
THE DECODER NETWORK . . . . .	6
THE DESIGN OF MDAC SWITCHES . . . . .	17
MDAC Switch Configuration Selection . . . . .	17
JFET Versus MOSFET Switches . . . . .	22
The JFET Switch . . . . .	24
OFF State . . . . .	27
ON State . . . . .	28
The MOSFET Switch . . . . .	31
ERROR ANALYSIS . . . . .	34
Errors Caused by Input Voltage Variation . . . . .	35
Leakage-Current Error . . . . .	39
Errors Caused by Temperature Drift of Network Impedances . . . . .	40
High-Frequency Errors and Equalization . . . . .	44
Errors Caused by Switching Spikes . . . . .	45
CONSTRUCTION, TESTING, AND RESULTS . . . . .	47
Calibration . . . . .	48
Digital Switching Characteristics . . . . .	51
Dynamic Characteristics . . . . .	51
REFERENCES . . . . .	60

## LIST OF ILLUSTRATIONS

Figure	Page
1. (a) Ladder Network MDAC (b) Weighted Resistor Network MDAC . . . . .	8
2. 12-Bit MDAC Circuit Configuration . . . . .	15
3. (a) Bipolar Transistor Shunt Switch (b) FET Shunt Switch (c) FET Series Switch (d) FET Series-Shunt Switch . . . . .	20
4. (a) Simplified FET Model in the ON State (b) Simplified FET Model in the OFF State . . . . .	21
5. JFET Switch Circuit Schematic Diagram . . . . .	30
6. MOSFET Switch Circuit Schematic Diagram . . . . .	33
7. Fully Assembled MDAC . . . . .	50
8. MDAC Terminals On LOCUST Analog Patchbay . . . . .	50
9. Circuit For Measuring MDAC Dynamic Error . . . . .	50
10. Digital Switching Characteristics . . . . .	52
11. MDAC Switching Spikes . . . . .	53
12. (a) MDAC Dynamic Error With Frequency Equalization and (b) Dynamic Error Without Frequency Equalization . . . . .	57
13. MDAC Small-signal Frequency Response . . . . .	58
14. MDAC Operation at Computer Speed . . . . .	59
15. MDAC Resolution Near Digital Zero . . . . .	59

## LIST OF TABLES

Table	Page
I 12-Bit MDAC Specifications . . . . .	5
II MDAC Decoder Network Resistor Values . . . . .	16
III Output Error Caused By Impedance Error In Any Given Component . . . . .	36

## ABSTRACT

This paper discusses the design and testing of a high-speed, 12-bit multiplying digital-to-analog converter developed for use in wideband hybrid computers. The circuit features ease of construction with minimum component hand-selection, even though low network impedance levels are used in order to obtain accuracy at high analog computing frequencies. Zero-voltage-offset series field-effect transistor switching is utilized, and trimmer adjustment of binary weighting in the resistor network allows calibration of the fully-assembled device while it is in the computer under normal operating conditions. The multiplying digital-to-analog converter is capable of multiplying an analog signal by a digital number with a static accuracy of 0.025 per cent of half scale and a dynamic accuracy of 0.1 per cent of half scale at a computing frequency of 10 Khz.

## INTRODUCTION

The objective of this thesis project was to develop a 12-bit multiplying digital-to-analog converter (MDAC) for The University of Arizona's LOCUST/PDP-9 hybrid computer. With ordinary hybrid computers, the design of a 12-bit two's complement digital-to-analog converter (DAC), and even the more difficult design of a MDAC, is a straightforward proposition; but in our case, the MDAC design proved to be one of the most difficult tasks of the entire LOCUST project.

The difficulty in LOCUST MDAC design is due to the exceptional bandwidth requirements of the LOCUST computer, which is capable of 2000 differential-equation-solving runs per second and which must handle analog signal voltages all the way up to 100 KHz. For this reason, LOCUST operational amplifier summing resistance values are 1K ohms to 10K ohms. The LOCUST MDAC (see Table I for complete specifications) is to multiply a 10 KHz sinusoidal input by a digital word with a phaseshift error within 0.1 per cent of half scale, and its DAC network resistances must therefore also be between 2K and 10K ohms. As resistance levels are lowered, electronic switch resistance variations and offset voltages become quite critical. A second serious difficulty is that

the wideband amplifiers used in the LOCUST (30 Mhz at unity gain) faithfully transmit fast MDAC switching spikes which would never be seen in conventional analog computers. Fortunately, in most applications (optimization, random-process studies), the MDAC's usually switch only during computer RESET periods.

The reason for the requirement of 12 bits (11 bits plus sign) is not really 12 bit accuracy (LOCUST has an accuracy within only 0.1 per cent of half scale for linear computing elements) but rather is 12-bit resolution. This is needed to keep sensitive system parameters being optimized from "hunting" excessively about their optimal value. In unstable systems, such as in trajectory optimization, a very small parameter change can produce a substantial solution change.

The MDAC accepts the 12 most significant bits from the PDP-9 accumulator on an output command through a double-buffered interface (Wilkins 1969). Its output voltage on the analog computer patchbay is the voltage

$$\frac{X_A X_D}{2^{11}} = X_A \left[ X_1 (2)^{-1} + \dots + X_{11} (2)^{-11} - X_0 (2)^0 \right]$$

where  $X_A$  is a time-varying analog voltage between +10 volts and -10 volts and  $X_D$  is the binary number  $X_0 \dots X_{11}$  from the 12 most significant bits of the PDP-9 accumulator.

Important design objectives of this new MDAC are simplicity of construction, minimum calibration effort, and

reasonable cost. Construction of only a few units rather than a large number also enters into consideration.

The University of Arizona's earlier ASTRAC II/PDP-9 hybrid computer utilizes transistor shunt switches in the MDAC's. The switches must be individually compensated to minimize output error due to the offset voltages of the saturated transistors by a tedious process of resistor hand selection. The use of field-effect transistors (FET's) with zero offset voltages suggests itself as a remedy for this problem.

Most present MDAC's are designed with fixed precision resistors in the decoder networks. If the impedance levels of the MDAC are low, these resistors must be either very high-precision units or else must be hand selected. Very accurate resistors are expensive; and hand selection, which is time consuming and requires large stocks of resistors, is not too desirable when only a few units are being built for a particular system.

While transistor shunt switches require hand compensation for offset, series FET switches require either hand selection or resistor padding to account for the FET resistance. This is especially important in view of the low impedance levels used in LOCUST.

The MDAC described in this report uses FET switches for zero offset, a binary weighted resistor decoder network

to minimize the number of expensive switch components, and discrete component level converters and switch drivers for minimum cost. Trimmer adjustment of network resistances compensates for both switch resistances and resistor tolerance errors in one simple adjustment. No resistors with tolerances of less than 1 per cent are required, and only one resistor must be hand selected for the entire MDAC. Furthermore, calibration can be made on the fully assembled unit after it is in the computer under actual operating conditions. Because construction and calibration time is minimized, the design is well suited for use when a small number of high-speed, precision MDAC's are needed at a reasonable cost.

Table I 12-Bit MDAC Specifications

Analog input voltage	$\pm 10$ volts
Digital logic input levels:	
ON state	0 volts
OFF state	-3 volts
Static accuracy (% of half scale)	0.025% $\pm 1/5$ LSB
Dynamic accuracy (% of half scale)	0.1% at 10 KHz
Switching speed:	
delay	40 nsec
rise time	1.5 $\mu$ sec
settling time (within 0.025%)	5 $\mu$ sec
Output error temperature drift:	
worst case	$\pm 0.133$ LSB/ $^{\circ}$ C
typical (measured)	$\pm 0.02$ LSB/ $^{\circ}$ C
Worst-case switching spikes	$\pm 2.8$ volts (no output amplifier overloads are caused by worst-case switching spikes)
Power supply requirements	$\pm 15$ volts
Power supply regulation	$\pm 1\%$
Worst-case power supply drain	34.2 mA from +15 volts 78.5 mA from -15 volts
Maximum MDAC power dissipation	1.71 watts
Current drain from digital logic	4.1 mA at 0 volts 0 mA at -3 volts
Analog input impedance	2K ohms

## THE DECODER NETWORK

A multiplying digital-to-analog converter consists of a decoding network which converts the analog voltage into weighted currents proportional to the digital number and an operational amplifier with low output impedance. The two types of decoding networks most commonly found are the weighted-resistor network and the ladder network.

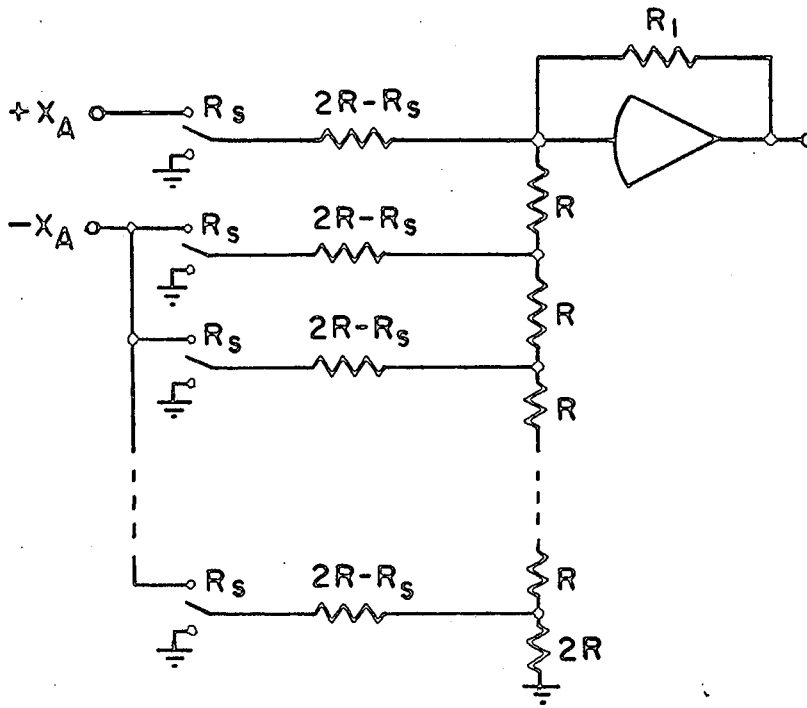
A ladder network (Fig. 1a) employs only two values of precision resistors. The analog currents flowing in the bits of a ladder network MDAC have been shown (Pearman and Popodi 1964) to be more evenly distributed through all bits than the analog bit currents flowing in an equivalent weighted-resistor network MDAC. Because analog current (and therefore power dissipation) is more equally distributed throughout the bits, and because resistance values are used which vary only by a factor of 2, the binary relationship of the ladder network bits should be easier to maintain with varying analog signal and environmental conditions.

The ladder network suffers from the disadvantage that wiring capacitances greatly increase from the most significant bit to the least significant bit due to the increasing number of resistor junction points (with their associated junction-to-ground capacitances) in the analog

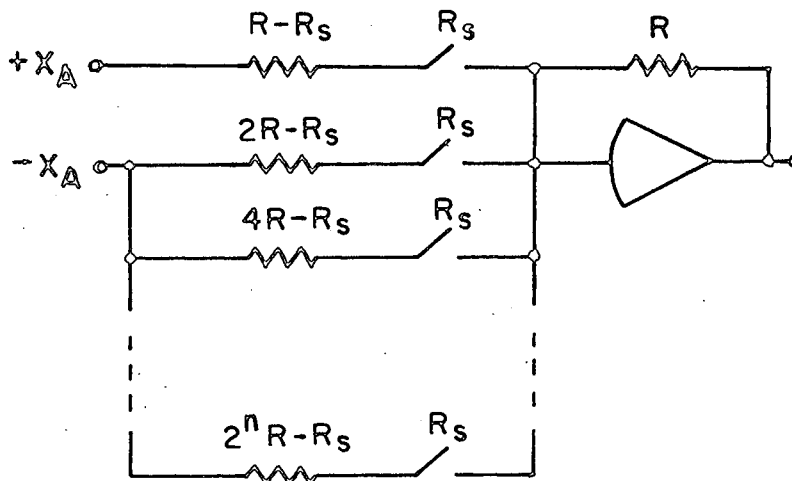
signal current path as one moves toward the least significant bit. A second disadvantage is that it requires a single-pole double-throw switch at the analog input of each bit. If FET switches are used, two of the relatively expensive FET's are necessary in each switch. More complex driving circuits are also required.

A weighted-resistor network (Fig. 1b) requires only a single-pole single-throw switch, or one FET per switch. Even if a single-pole double-throw switch is used in a series-shunt configuration (Fig. 3d) in a weighted resistor network, still only one of the transistors in each switch must be a FET. Because the FET and its associated level-shift and drive circuits are the most expensive part of each bit, one would like to minimize the number of FET's and switch components. In addition, because the impedance of each bit of a weighted-resistor network is connected directly to the amplifier summing junction, wiring capacitances in the less significant bits should be smaller than those of a ladder network. For the above reasons, and because limited space in MDAC packaging for LOCUST required use of a minimum number of components, the weighted resistor type decoder was used rather than the ladder network.

A  $n$ -bit weighted resistor decoder consists of  $n$  binary related resistors  $R, 2R, 4R, \dots, 2^n R$  as in Fig. 1b. Note that the switch resistance  $R_s$  must be included in each



(a)



(b)

Fig. 1. (a) Ladder Network MDAC (b) Weighted Resistor Network MDAC

bit. If the amplifier gain is sufficiently high, the summing junction is virtually at ground potential because of the negative feedback across the amplifier. The bit currents flowing into the summing junction are therefore binary weighted, with  $X_A/R$  in the most significant bit and  $-X_A/2^n R$  in the least significant bit.

The weighted resistors are switched in or out of the network depending on whether a digital 1 or 0 is present at the switch drive of each bit. A digital 2's complement number  $X_D = X_0 \dots X_n$  then yields an analog voltage  $X_{out}$  at the amplifier output, where

$$X_{out} = X_A [X_1 (2)^{-1} + \dots + X_n (2)^{-n} - X_0 (2)^0]$$

The impedance level of the MDAC is given by the impedance of the feedback resistor. Because of distributed capacitance effects associated with large resistances, the impedance level must be kept as low as possible for good high frequency response. On the other hand, the switch error analysis presented later in this paper indicates that 10K ohms seems to be a minimum value for the impedance level if switch errors are to remain within limits over normal operating temperature ranges. Therefore the feedback resistor and first bit resistor are chosen to be 10K. Bit resistors then double for each bit until an impedance of 20.48M ohms is reached in bit 11. Since the  $2^{11} : 1$  resistance ratio is not practical, T-networks are used for the

low-current branches. The non-zero switch resistance  $R_s$  must again be included in transfer impedance calculations for T-networks. Impedance in the T-networks must also be kept fairly low because of distributed capacitances. For good frequency response in the high-impedance bits, resistances used in T-networks were limited to a maximum of 40.2K ohms.

Other considerations in the selection of resistances for the decoder network include the feedback ratio of the output amplifier, which determines its frequency response, and the current load on the driving analog amplifier. Because phase-shift error of an operational amplifier varies approximately inversely with the feedback ratio (Korn and Korn 1964), the summing-junction-to-ground impedance must be as high as possible. Because the preceding analog stage has drive capability limitations, the input-to-ground impedance must also be high enough to keep drive requirements within these limits. Worst-case conditions for feedback ratio occur when all switches are in the ON state (logical 1). Because a shunt transistor will be used in each bit (for reasons explained later), the MDAC input impedance is independent of the switch settings.

If the switch resistance were a constant  $R_s$  for all switches, this fixed value could be considered when

selecting decoder network resistance. Unfortunately, the ON resistance of present field-effect transistors can vary quite a bit from device to device. A TIS41 JFET, for instance, can have a selection resistance of anywhere from 15 ohms to 25 ohms; and the SS2012 MOSFET can have a selection resistance of from about 150 ohms to 250 ohms. In addition, unless very high precision resistors are used, the tolerances of the resistors in each bit can add up to an impedance variation which is larger than the allowed tolerance for the transfer impedance. Such variations in switch resistance and resistor values would normally have to be compensated by hand selecting or padding resistors. This is a tedious process, which is best implemented in large production quantities.

A simple method of adjusting the transfer impedance of each bit to compensate for both the switch resistance and the resistor tolerances in one step is to add a trimmer potentiometer to the resistor network of each bit. If the network is designed so that small variations in the trimmer have negligible effect on the transfer impedance, an inexpensive carbon-film trimmer can be used in all except the first few most significant bits. Series wire-wound trimmers are used in the first 3 bits, with maximum resistances kept small (less than 2.5% of the total bit resistance) in order to minimize the effect of

trimmer capacitances and inductances. The transfer impedance for each bit is designed so that a full OFF (zero ohms) to full ON (maximum resistance) excursion of the trimmer causes only enough variation in transfer impedance to compensate for worst-case switch resistance and resistor tolerances. If this is done, the effect of the temperature coefficient of the carbon trimmers is reduced so that the output error introduced by trimmer temperature coefficients is acceptable. This statement will be justified in the error analysis later in this report.

Adjustment of each bit and of the feedback resistor, by a procedure described in a later section, eliminates static tolerance errors. Leakage currents and voltage and temperature variations then remain as the only sources of static error in MDAC resolution and monotonicity.

Worst-case design equations may be used to determine values of standard resistances which assure worst-case tolerance and switch resistance compensation for a full OFF to full ON trimmer variation. Assuming the circuit configuration and terminology of Fig. 2, the resistor values for the  $n^{\text{th}}$  bit transfer impedance must satisfy the following worst-case relations:

For bits 0-2:

$$R_{pn(\max)} = 2^n (10K)(1+\delta) - R_{ln}(1-\delta) - R_{sn(\min)}$$

$$R_l = \frac{1}{(1+\delta)} \left[ 2^n (10K\Omega)(1-\delta) - R_{sn(\max)} \right]$$

For bits 3-11:

$$\frac{R_{xn} R_{yn} (1+\delta)}{(R_{xn} + R_{yn})} \leq \frac{R_{1n} (1-\delta) [R_{2n} (1-\delta) + R_{sn(\min)}]}{[2^n (10K\Omega) (1+\delta) - R_{sn(\min)} - (R_{1n} + R_{2n}) (1-\delta)]}$$

$$\frac{R_{xn} (1-\delta) [R_{yn} (1-\delta) - R_{pn(\max)}]}{(R_{xn} + R_{yn}) (1-\delta) + R_{p(\max)}} \geq \frac{R_{1n} (1+\delta) [R_{2n} (1+\delta) + R_{sn(\max)}]}{[2^n (10K\Omega) (1-\delta) - R_{sn(\max)} - (R_{1n} + R_{2n}) (1+\delta)]}$$

where the subscripts max and min respectively indicate maximum or minimum worst-case values, and where  $\delta$  is the precision resistor tolerance.  $R_{sn}$  is the FET ON resistance of the  $n^{\text{th}}$ -bit switch, and  $R_{pn}$  is the  $n^{\text{th}}$ -bit trimmer resistance. Calculations for bits 3 through 11 were made assuming 1% tolerances. To minimize potentiometer resistance in bits 0 through 2, fixed resistor tolerances of 0.5% were assumed in the calculations for these bits.

The calculated resistor values for the transfer impedances of the 12 bits, corresponding to the terminology of Fig. 2, are shown in Table II. The type of switch used in each bit is indicated under  $R_{sn}$ . All fixed resistors are 1%. 20K trimmers are used in the design simply because of

availability of a large stock of this value in our laboratory. Since errors in the least significant bits have little effect on the output, the trimmers in the last few bits could be omitted when designing the MDAC.

The minimum possible output amplifier feedback ratio of the MDAC with all switches in the ON state is .201, and it is 1.0 with all switches OFF. Worst-case load impedance to the preceding analog stage is 2K ohms ( $\pm 5$  ma at  $\pm 10$  volts).

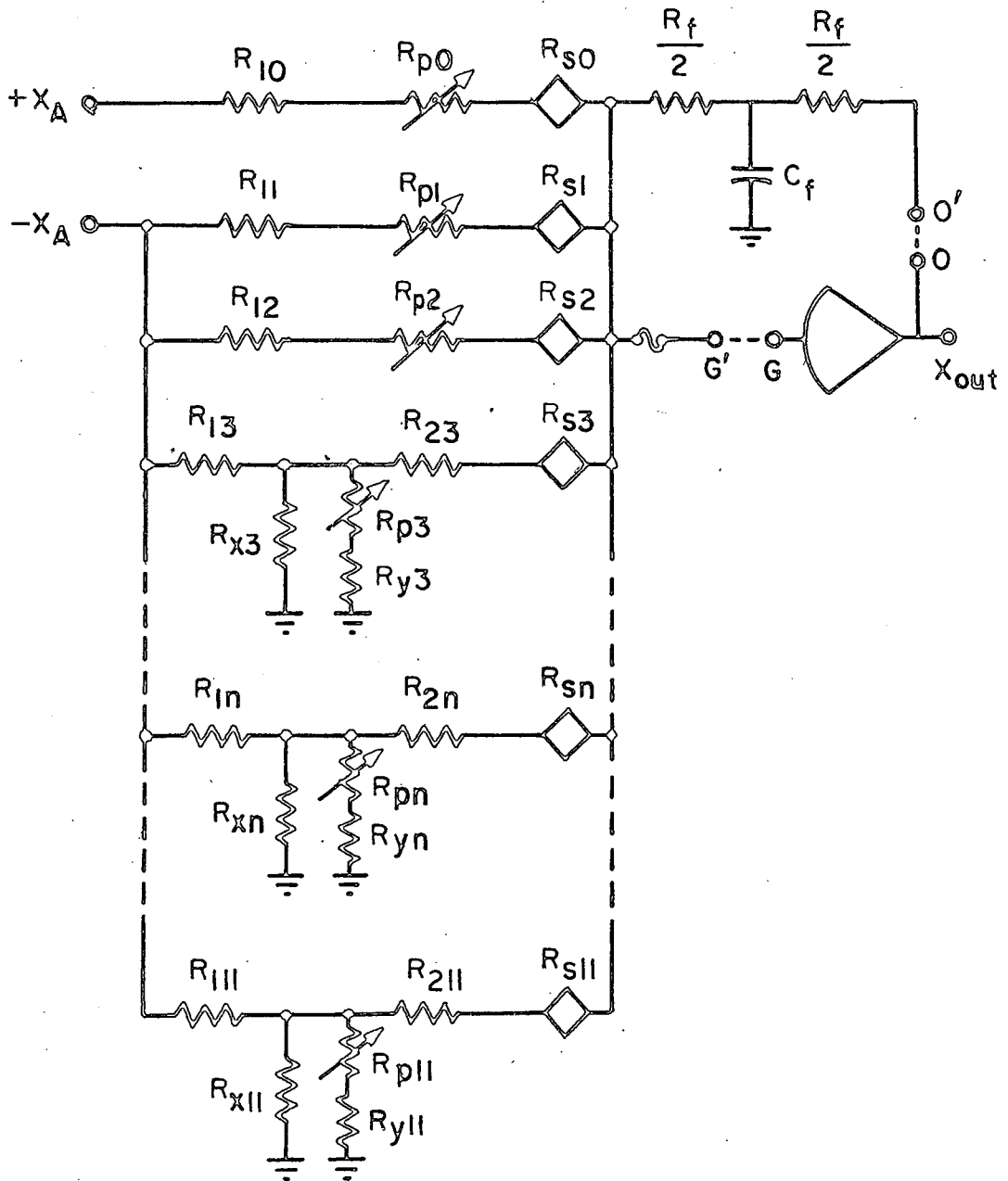


Fig. 2. 12-Bit MDAC Circuit Configuration

Table II MDAC Decoder Network Resistor Values

(Resistor notation corresponds to Fig. 2)

<u>Bit no. (n)</u>	<u>R<sub>sn</sub></u>	<u>R<sub>pn</sub></u>	<u>R<sub>1n</sub></u>	<u>R<sub>2n</sub></u>	<u>R<sub>xn</sub></u>	<u>R<sub>yn</sub></u>
0	TIS41	200	9.86K	--	--	--
1	TIS41	500	19.76K	--	--	--
2	TIS41	1K	39.5K	--	--	--
3	TIS41	20K	10K	30.1K	10K	23.7K
4	TIS41	20K	10K	40.2K	4.42K	16.9K
5	SS2012	20K	40.2K	40.2K	8.66K	25.5K
6	SS2012	20K	40.2K	40.2K	3.57K	12.1K
7	SS2012	20K	40.2K	40.2K	1.58K	7.15K
8	SS2012	20K	40.2K	40.2K	750	3.74K
9	SS2012	20K	40.2K	40.2K	348	0
10	SS2012	20K	40.2K	40.2K	178	0
11	SS2012	20K	40.2K	40.2K	82.5	0

## THE DESIGN OF MDAC SWITCHES

### MDAC Switch Configuration Selection

Bipolar transistor shunt switches, such as the one shown in Fig. 3a, create MDAC output errors due to the offset voltage and collector resistance. In a low impedance MDAC, these errors must be compensated by individual trial-and-error selection of an offset resistor for each switch in the device (O'Grady 1969). Field-effect transistors have the advantage of zero offset voltage, but higher drive voltage are required. In addition, the ON switch resistance of most FET's is higher than that of a bipolar transistor. A FET used as an analog switch may be represented simply by a variable resistance as shown in Fig. 4, with a low resistance in the ON state, and an extremely high resistance in the OFF state. When a FET is used as a shunt switch as in Fig. 3b, output voltage error appears in the OFF state due to the non-zero FET resistance. This is also undesirable.

If a FET is used in a series switch configuration (Fig. 3c), no offset voltage problems exist in either state; and no hand-selected offset compensation is necessary. The FET appears as a pure resistance in the ON state and a nearly ideal open circuit in the OFF state.

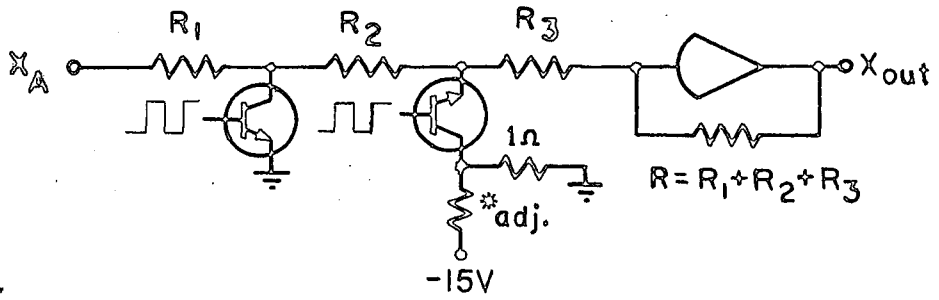
Series switches have the advantage that the feedback ratio  $\beta$  of the output amplifier always remains higher than for an equivalent shunt switch. For the single-bit shunt switches of Figs. 3a and 3b,  $\beta$  is  $\frac{1}{2}$  in the ON state and always less than  $\frac{1}{2}$  in the OFF state. For the series switches of Figs. 3c and 3d, the feedback ratio is  $\frac{1}{2}$  with the switch ON and 1 with the switch OFF. Since, as a first approximation, operational amplifier phase shift varies inversely with  $\beta$  (Korn and Korn 1964), the high-frequency error should be lower for a series-switched MDAC than for a shunt-switched MDAC of the same impedance level. Again, the input impedance seen by the preceding state is always higher in the OFF state for the series-switched bit than for the shunt-switched bit, requiring less analog current drive and less power dissipation in the precision resistors. For the above reasons, a series switch should be preferable to a shunt switch.

Most junction FET's with low ON resistance have the disadvantage that they require substantial gate-voltage swings at the gate to turn the FET off. For reasons explained later, this high gate OFF voltage requires that a bipolar shunt transistor be used to ground the source of the FET when it is turned OFF. The resulting series-shunt current switch is shown in Fig. 3d.

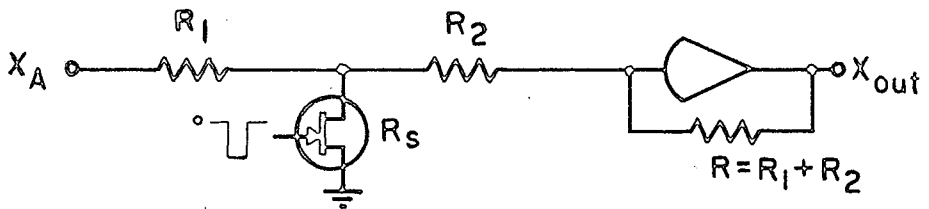
The series-shunt current switch has all the advantages of the series switch; and, since the shunt

transistor is only grounded when the FET is open, the feedback ratio is unaffected. No offset error due to the shunt transistor can appear in the OFF state because the FET is open-circuited. In addition, the shunt transistor provides a path for the analog signal current to flow to ground when the FET is OFF. If the switch is at the summing junction of the amplifier, this results in a constant impedance to the preceding analog driving stage regardless of the state of the switch. Currents in the precision resistors are constant regardless of the state of the switch, causing uniform power dissipation and thereby reducing the possibility of binary errors due to thermal variations in the resistors. Also, since the shunting transistor is driven by a signal complementary to the FET drive signal, the switching spikes of the two devices tend to cancel partially.

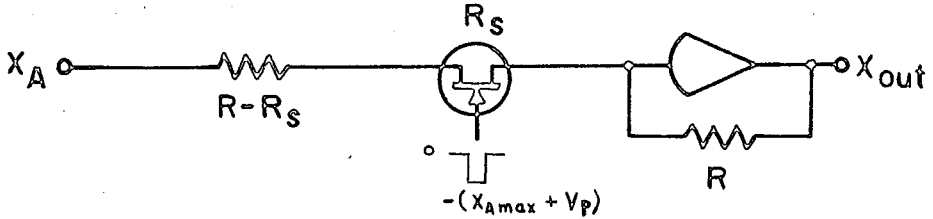
For the above reasons, the FET series-shunt current switch was chosen as the optimum configuration for switching the MDAC. In addition to the advantage of constant input impedance, placing the switch at the summing junction rather than elsewhere in the bit impedance has the advantage of lower FET gate-drive and transistor base-drive level requirements, better high-frequency switching, and better isolation of the gate drive from the analog signal.



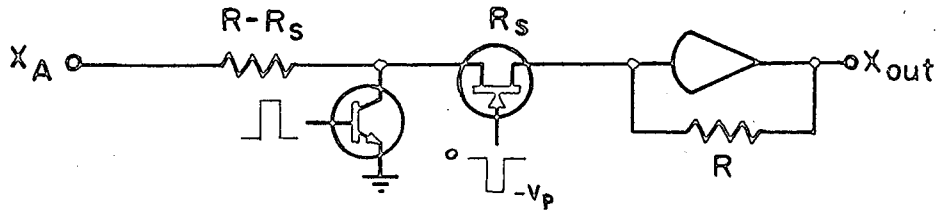
(a)



(b)

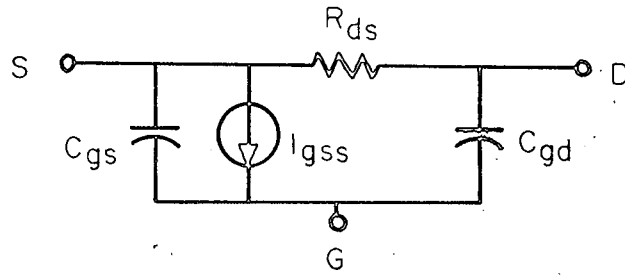


(c)

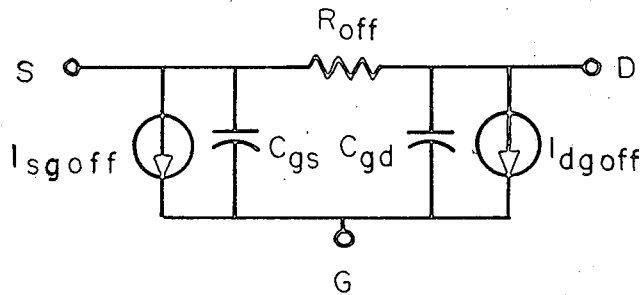


(d)

Fig. 3. (a) Bipolar Transistor Shunt Switch (b) FET Shunt Switch (c) FET Series Switch (d) FET Series-Shunt Switch



(a)



(b)

Fig. 4. (a) Simplified FET Model in the ON State  
 (b) Simplified FET Model in the OFF State

### JFET Versus MOSFET Switches

Although voltage-offset problems do not exist in FET switches, error results from the variation of drain-to-source ON resistance ( $R_{DS}$ ) with temperature, with drain current ( $I_D$ ), and with gate-to-source voltage ( $V_{GS}$ ). These variations are different for junction field-effect transistors (JFET's) and for metal-oxide-semiconductor FET's (MOSFET's).

Most inexpensive MOS field-effect transistors have relatively high drain-to-source ON resistances compared to that obtainable in junction field-effect devices. For this reason, the variation in  $R_{DS}$  with drain current is larger for MOSFET's. The variation of  $R_{DS}$  for the 25 ohm JFET used will be shown to be only a fraction of an ohm over the  $\pm 1$  mA range of the analog current in the most significant bit, while similar current variation in the 250 ohm MOSFET would cause a resistance variation of several ohms.

N-channel junction FET's have the advantage that they are in the ON state when the gate-source voltage is zero. Since the summing junction of the operational amplifier is a virtual ground, the gate need only be grounded in order to insure that the gate voltage will follow the source voltage and will thus minimize variation of  $R_{DS}$ . The ON resistance of a JFET is therefore independent of power supply drift and regulation. The MOSFET's, however,

must be biased at some positive value of gate voltage to be in the ON state. Any change in this positive gate bias due to power supply drift or power supply regulation leads to additional variation in  $R_{ds}$  for the MOSFET.

While the temperature coefficient of ON resistance is lower for MOS transistors than for JFET's, the fact that the overall drain-source resistance of the JFET is much lower still leads to a smaller variation of  $R_{ds}$  with temperature than for the MOSFET.

From the above comparison, it is obvious that the JFET would make a much more accurate series switch than would the MOSFET. Low resistance JFET's, on the other hand, are more expensive than MOSFET's; and low JFET ON resistance necessitates a large junction with associated high junction capacitance (Fig. 4). As a comparison, the TIS41 JFET has a gate-to-drain capacitance in the OFF state of more than 8 picofarads, while the SS2012 MOSFET has a maximum gate-to-drain capacitance of only 1 picofarad. Because the JFET capacitance is caused by a reverse-biased p-n junction, the capacitance increases still further when the switch is in the ON state. The high capacitance between the gate and drain causes a large surge of injected current into or out of the summing junction of the operational amplifier when the gate drive is switched between its two states. The current surge creates output voltage switching

spikes. Ordinarily, slow operational amplifiers could not follow such short, high-magnitude output spikes. The use of 30 Mhz amplifiers in the LOCUST system, however, causes these spikes to be a major problem. The switching spikes can be partially cancelled by feeding an inverted spike to the summing junction, but complete cancellation is not possible.

A tradeoff between accuracy and switching spikes indicates the use of MOSFET switches in the least significant bits for minimum switching spikes, with JFET switches in the most significant bits for static accuracy. An examination of the error variations for the two switches indicates that the current and temperature variations of  $R_{ds}$  in MOSFET switches can be tolerated in bit 5 and lower, while their use in bit 4 and higher would increase the output error significantly.

#### The JFET Switch

The MDAC switches were designed to operate from the 0 and -3 volt logic levels of the PDP-9/LOCUST interface. Each MDAC bit is OFF (passes no analog signal) when the interface output flip-flop corresponding to that bit is zero volts, and ON when the flip-flop output is below -3 volts.

A n-channel junction field-effect transistor has lower ON resistance than a p-channel device of comparable

geometry, and therefore n-channel FET's are usually used when low resistance with minimum capacitance is desired. The TIS-41 symmetrical n-channel JFET has a source-drain ON resistance of less than 25 ohms when the gate-source voltage  $V_{gs}$  is zero. As  $V_{gs}$  is made more negative, the resistance increases to an OFF resistance of several hundred megohms at  $V_{gs} = -10$  volts. Thus the 0 and -3 volt logic levels must be converted to at least -10 volts and 0 volts at the gate to drive the FET into the appropriate states. Because large logic signal swings are required to drive the JFET, standard low-level integrated-circuit logic circuits cannot be used as drivers. Integrated-circuit FET drivers capable of these large level swings are presently quite expensive. To keep MDAC cost at a minimum, discrete component drivers were therefore used.

Without a shunt transistor in the most significant bits (Fig. 3c), the voltage at the source of the JFET would follow the analog input voltage when the FET was in the OFF state. Since the gate must always be held at least 10 volts negative with respect to the source and drain, an analog input of -10 volts would mean that the gate OFF drive voltage would have to be more negative than -20 volts. Because the negative power supply voltage in the analog computer is only -15 volts, the source of the FET must be grounded when the FET is turned off. For this reason, shunt transistors

are provided in the most-significant-bit JFET switches (if JFET's were used in lower bits, where the T-networks reduce the analog swing at the source to below -5 volts when the switch is off, the shunting transistor would not be necessary).

The use of a shunt transistor has other useful advantages in addition to insuring sufficient OFF gate voltage. A common problem in JFET series voltage switches is that at high analog signal frequencies the gate-source and gate-drain capacitances (Fig. 4) provide a path for the analog signal to pass into the amplifier summing junction even when the FET is turned off. Grounding the FET sources eliminates the possibility of capacitive feedthrough from the -10 volt analog voltage swing at the source when the switch is OFF.

An additional advantage of the shunt transistor is the possibility of partial compensation of the FET switching spikes. If a NPN transistor is used as the shunt transistor, the polarity of its base drive voltage causes switching spikes complementary to those of the FET.

Because the switching spikes due to the JFET and to other capacitances in the circuit are much larger than the complementary spikes of the NPN transistor, some additional spike compensation must be included. If no additional compensation were used, switching spikes on the order of 3 to

4 volts for each JFET switch and 1 volt for each MOSFET switch could be possible. These spikes would add, so that actual overloading of the output amplifier would be possible for worst-case switching.

Switching-spike compensation is accomplished by feeding inverted spikes to the summing junction of the operational amplifier through a differentiating capacitor from the first gate drive stage. The inverter stage delay is short compared to the duration of the switching spikes, so that the major portion of the spikes can be effectively cancelled by selection of an appropriate value for this compensating capacitor.

The circuit of the complete JFET switch is shown in Fig. 5. One inverter provides the drive for the shunt transistor, and two stages provide the 0 and -10 volt gate drive for the FET. Operation of the switch in the OFF and ON states is described below.

#### OFF State

With the logic input at ground, the analog signal current is routed to ground rather than to the summing junction. Transistors  $Q_1$  and  $Q_3$  are saturated, providing approximately -13 volts at the gate of the JFET  $Q_4$  to turn it OFF. Diode  $D_7$  is reverse biased, and diodes  $D_5$  and  $D_6$  are conducting. Diodes  $D_1$ ,  $D_2$ , and  $D_3$  supply +0.7 volts

to the base of  $Q_2$  to hold it in the saturated state; and  $R_5$  provides the necessary base and diode current.  $D_1$  is a germanium diode, while  $D_2$  and  $D_3$  are silicon.

#### ON State

With the logic input at -3 volts, the analog signal current is routed to the summing junction, and the shunting switch is open. To turn the FET ON, diode  $D_5$  is placed in series with the gate, and the collector of  $Q_3$  is then driven to any voltage greater than zero. The low leakage diode  $D_5$  becomes back biased, and the gate voltage remains at zero volts. The addition of  $D_5$  by itself would cause turn-on switching time to be greatly increased because the gate would have to charge entirely through the gate-source and gate-drain capacitances during turn on. To correct this problem,  $R_7$  must be added as a low-impedance path from the gate to ground.  $R_7$  is chosen experimentally to give the desired turn-on time.

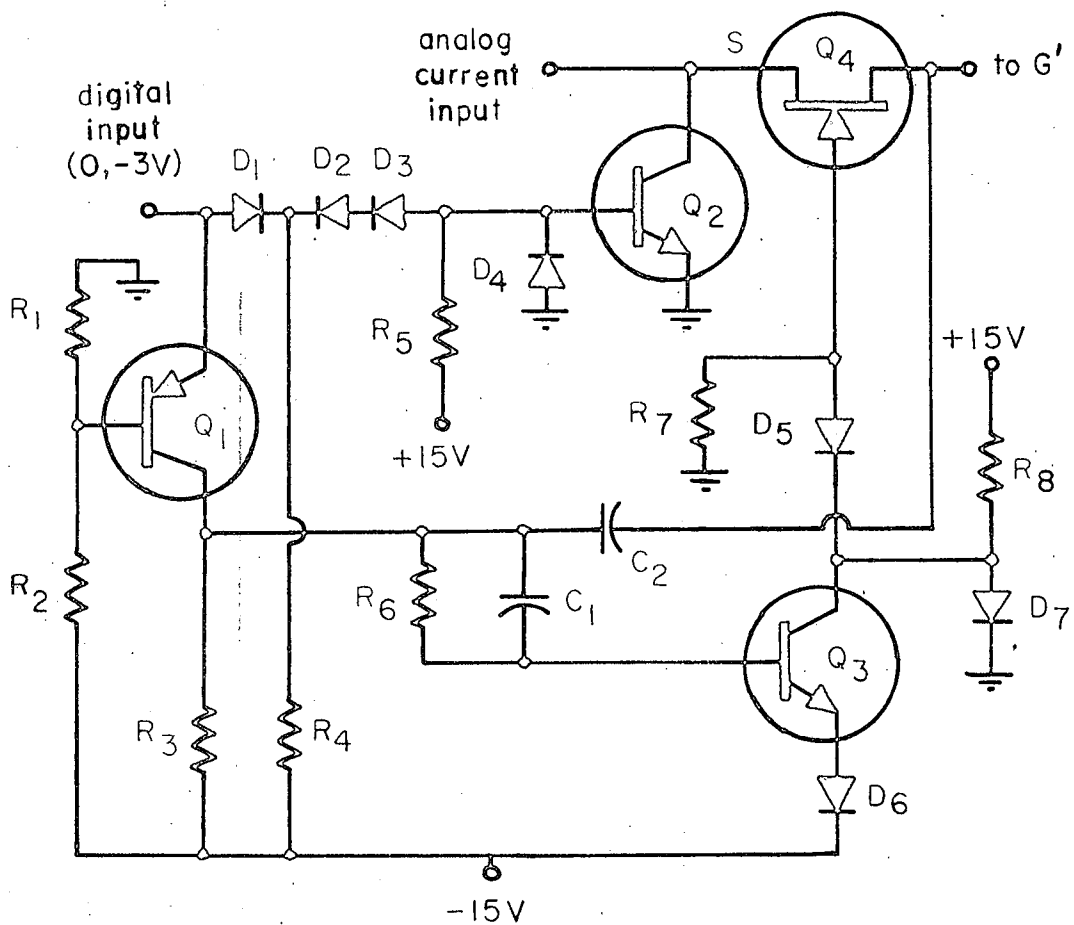
In the ON state, transistors  $Q_1$  and  $Q_3$  are OFF. The collector voltage of  $Q_3$  is +0.7 volt, and the gate voltage of  $Q_4$  is 0 volts.  $R_8$  can be very large, since its only purpose is to provide current to hold  $D_7$  slightly forward biased when the FET is on. Resistor  $R_4$  acts as a pull down resistor to turn  $Q_2$  off, and diode  $D_4$  clamps the  $Q_2$  base voltage at -0.7 volt to protect the base.

The values of  $R_1$  through  $R_8$  are calculated using

worst-case design equations, assuming resistor tolerances of 15% and power supply tolerance of 1%. Worst-case logic inputs are assumed to be -0.3 volts and -3.2 volts. Capacitor  $C_1$  is a speed-up capacitor selected experimentally.  $C_2$  is the FET switching spike compensation capacitor which is also determined experimentally. Because saturated transistor switching is used, the  $\pm 15$  volt power supply leads are filtered to isolate the MDAC transients from the analog supply.

Impedance levels in the switch are chosen to give drive signal transition times of approximately 1 microsecond as a tradeoff between switching spikes and settling time. Note that extremely fast switching times are not desirable because of the larger switching spikes created by fast drive signals in FET's. Slower drive signals are, of course, not tolerable in view of the 250 Khz maximum data output rate of the digital computer interface.

Power dissipation in the switch-driving circuits is an important consideration, since excess dissipation in the MDAC can lead to temperature drift. No current is drawn at the driver-circuit inputs when the switch is ON (digital input at -3 volts), and approximately 3.5 mA is required when the switch is OFF (digital input at ground). Power supply drain in the ON state is only 1.05 mA from +15 volts and 2.18 mA from -15 volts, and drain in the OFF state is 1.1 mA from +15 volts and 4.5 mA from -15 volts.



$Q_1=2N4125$   
 $Q_2, Q_3=2N3904$   
 $Q_4=1S41$   
 $D_1=1N281$   
 $D_2-D_7=1N914$   
 $C_1=22 \text{ pF}$   
 $C_2=7.5 \text{ pF}$

$R_1=3.3K \text{ ohms}$   
 $R_2=22K$   
 $R_3, R_7=10K$   
 $R_4=8.2K$   
 $R_5=18K$   
 $R_6=68K$   
 $R_8=100K$

Fig. 5. JFET Switch Circuit Schematic Diagram

### The MOSFET Switch

The MOSFET switch is similar to the JFET switch. The gate drive voltage, however, swings from +8 volts in the ON state to -6 volts in the OFF state.

The SS2012 operates in both the depletion and enhancement modes. The maximum ON resistance is 250 ohms for a gate-to-source voltage of greater than +5 volts. Measurements of  $R_{ds}$  versus  $V_{gs}$  for the SS2012 in the laboratory indicated that the rate of change of  $R_{ds}$  with  $V_{gs}$  decreases as  $V_{gs}$  is increased. For this reason, it is desirable to operate the MOSFET at a gate voltage larger than +5 volts in the ON state. A  $V_{gs}$  more negative than -5 volts insures depletion of the channel and turns the device off.

The circuit schematic of the complete MOSFET switch is shown in Fig. 6. Modification of the JFET switch to accommodate a MOSFET is accomplished by replacing  $D_6$ ,  $R_8$ , and  $D_7$  with  $R_9$ ,  $R_{10}$ , and  $R_{11}$  respectively.  $R_{11}$  is tied to -15 volts rather than to ground.  $D_5$  and  $R_7$  are eliminated.

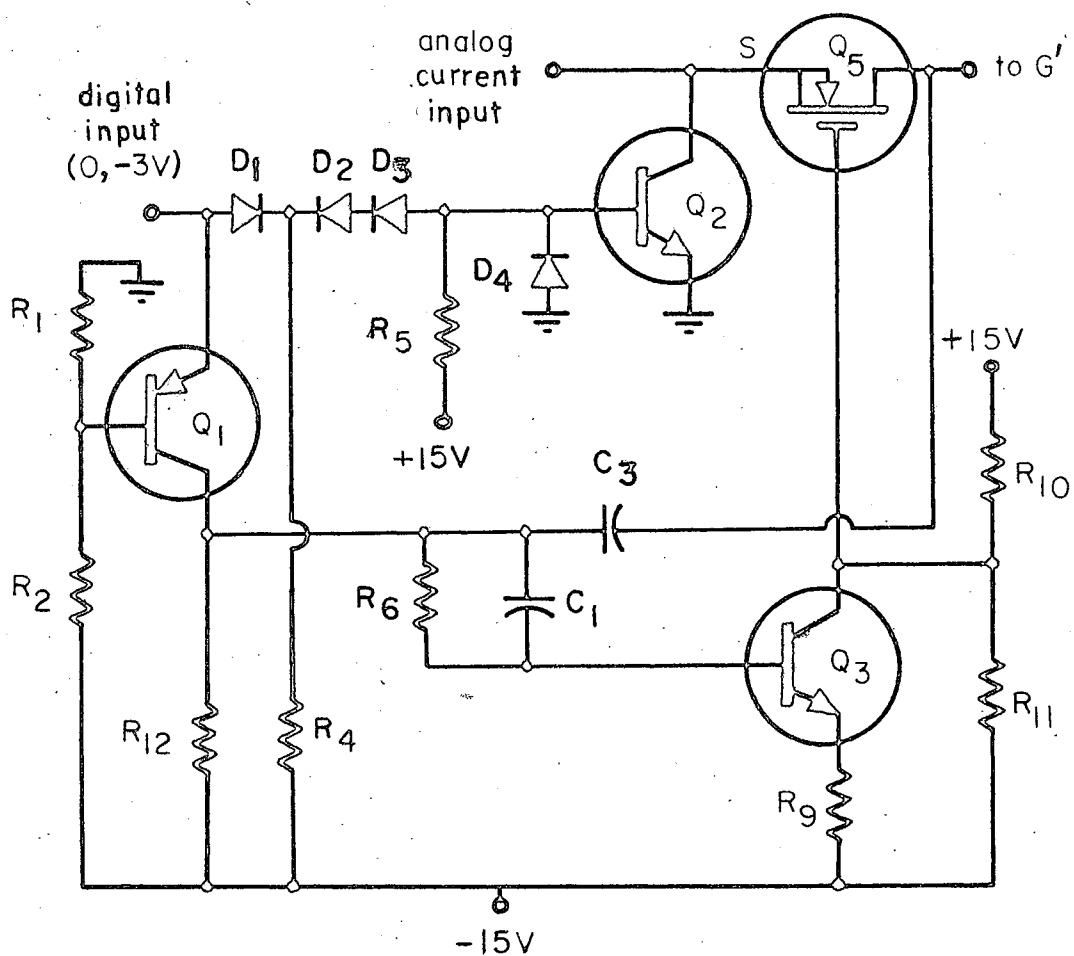
In the ON state,  $R_{10}$  and  $R_{11}$  form a voltage divider at the gate to set the +8 volt bias. In the OFF state,  $Q_3$  saturates and thus parallels  $R_9$  with  $R_{11}$  to bring  $V_{gs}$  to -6 volts.

The NPN shunt transistor is necessary in the MOSFET switch for a different reason from that for the JFET switch. The ON resistance of MOS devices increases

as the square root of source-substrate voltage  $V_{sb}$ . (Schmid 1968). To eliminate variations in  $R_{on}$  with  $V_{sb}$ , the SS2012 is constructed with the source shorted to the substrate. While this improves ON resistance behavior, it also creates a p-n junction between the source (substrate) and drain. Thus, when the MOSFET is turned OFF, the source voltage must not be allowed to become more than about 200 mv. positive with respect to the drain. If it does, the junction will become forward biased.

Worst-case design was again used to calculate resistor values, assuming the same worst-case parameters as for the JFET switch. Capacitors were chosen experimentally.

Power supply drain of the MOSFET switch in the ON state is 1.95 mA from +15 volts and 3.25 mA from -15 volts, and drain in the OFF state is 4.1 mA from +15 volts and 8 mA from -15 volts. Current required at the switch input is zero when at -3 volts and 4.1 mA when at ground.



$Q_1 = 2N4125$   
 $Q_2, Q_3 = 2N3904$   
 $Q_5 = 5S2012$   
 $D_1 = 1N281$   
 $D_2, D_3, D_4 = 1N914$   
 $C_1 = 22 \text{ pF}$   
 $C_3 = 2.5 \text{ pF}$

$R_1 = 3.3 \text{K ohms}$   
 $R_2, R_{11} = 22 \text{K}$   
 $R_4 = 8.2 \text{K}$   
 $R_5 = 18 \text{K}$   
 $R_6 = 68 \text{K}$   
 $R_9 = 2.7 \text{K}$   
 $R_{10}, R_{12} = 6.8 \text{K}$

Fig. 6. MOSFET Switch Circuit Schematic Diagram

## ERROR ANALYSIS

Calibrating the MDAC while it is in the computer under actual operating conditions allows essentially complete compensation of resistor tolerance and switch resistance variations for a given set of environmental conditions and for a given analog input voltage. For these particular conditions, because offset voltage error is zero, the only remaining static error is due to leakage currents. A change in environmental conditions or variations in the analog input voltage can, however, cause errors. In addition, dynamic errors caused by the unavoidable capacitances in the MDAC circuit become very significant as the analog signal frequency increases.

To insure 12-bit resolution, the worst-case static resolution error for any possible switch combination should be less than or equal to one-half the least significant bit (LSB). Worst-case errors in resolution occur near digital zero crossing, where all switches change state. For a 12-bit MDAC, the total allowable non-monotonic, static binary error is therefore  $\frac{1}{2}$  LSB =  $1/(2)^{12} = 0.0244\%$  of half scale. Dynamic errors in the analog output voltage caused by capacitances in the system must bring the total error to less than 0.1% at a computing frequency of 10 Khz to meet specifications of the LOCUST system.

The effect of a variation or error in the impedance of one particular component of a particular bit on overall output error can be found by differentiating the expression for MDAC output voltage with respect to the component in question. Assuming the notation for each component that is shown in Fig. 2, with T-networks in all but the 3 most significant bits, the output error caused by changes in the impedance of any given component may be expressed as per cent of half scale change in output voltage for a per cent change in the impedance of the given component. The resulting expressions are summarized in Table III for each component in the MDAC network. These relations will be used to relate the effect of various errors to overall output error.

#### Errors Caused by Input Voltage Variation

The channel resistance of both junction and MOS type field effect transistors varies as a function of drain current in the device. Time-varying values of current through the non-zero switch resistance cause the drain-to-source voltage to vary. This in turn causes variations in gate-to-source voltage and channel resistance, since FET ON resistance is a function of  $V_{gs}$ .

Table III Output Error Caused By Impedance  
Error In Any Given Component

(Component notation corresponds to Fig. 2)

Component (n <sup>th</sup> bit)	$\left[ \frac{\% \text{ error (of half scale) in MDAC output voltage}}{\% \text{ change in impedance of component}} \right]$
$R_f$	+1
$R_{10}$	$+(R_{10}/10K)$
$R_{p0}$	$+(R_{p0}/10K)$
$R_{s0}$	$+(R_{s0}/10K)$
$R_{1n}$	$-(2)^{-2n} (R_{1n}/10K)$
$R_{pn}$	$-(2)^{-2n} (R_{pn}/10K)$
$R_{sn}$	$-(2)^{-2n} (R_{sn}/10K)$
$R_{1n}$	$-(2)^{-n} \left[ 1 - \frac{(R_{2n} + R_{sn})}{2^n (10K)} \right]$
$R_{2n}$	$-(2)^{-n} \left[ 1 - \frac{R_{1n}}{2^n (10K)} \right] \left( \frac{R_{2n}}{R_{2n} + R_{sn}} \right)$
$R_{sn}$	$-(2)^{-n} \left[ 1 - \frac{R_{1n}}{2^n (10K)} \right] \left( \frac{R_{sn}}{R_{2n} + R_{sn}} \right)$
$R_{xn}$	$+(2)^{-2n} \left[ \frac{R_{1n} (R_{2n} + R_{sn})}{R_{xn} (10K)} \right]$
$R_{yn}$	$+(2)^{-2n} \left[ \frac{R_{1n} R_{yn} (R_{2n} + R_{sn})}{(R_{yn} + R_{pn})^2 (10K)} \right]$
$R_{pn}$	$+(2)^{-2n} \left[ \frac{R_{1n} R_{pn} (R_{2n} + R_{sn})}{(R_{yn} + R_{pn})^2 (10K)} \right]$

The channel resistance of a junction FET biased near zero gate-to-source voltage is given (Shipley 1964) by

$$R_{ds} = \frac{R_{ds}'}{(1 - V_{gs}/V_p)}$$

where  $R_{ds}'$  is the value of channel resistance when  $V_{gs}=0$  and  $V_p$  is the pinchoff voltage of the JFET. Differentiation of this expression with respect to  $V_{gs}$  shows that the per cent change in channel resistance for a small change in  $V_{gs}$  is given by

$$\frac{\Delta R_{ds}}{R_{ds}'} = \frac{\Delta V_{gs}}{V_p}$$

Since the maximum  $R_{ds}$  of the TIS41 is 25 ohms, the maximum variation in  $V_{gs}$  in the  $n^{\text{th}}$  bit for a  $\pm 10$  volt analog input is  $\pm (2)^{-n} (25\text{mV})$ . Assuming a minimum pinchoff voltage of 4 volts, the maximum per cent variation in switch resistance is  $\pm (2)^{-n} (0.625\%)$  of total switch resistance, or  $\pm (2)^{-n} (0.156)$  ohms. From the expressions in Table III, this results in a maximum output error of  $\pm 0.00156\%$  of half scale for bit 0,  $\mp 0.00039\%$  for bit 1,  $\mp 0.0001\%$  for bit 2, and less than  $\mp 0.00004\%$  total for bits 4 and 5.

MOSFET channel resistance varies in a more complex manner than does JFET resistance (Schmid 1968). Resistance of the SS2012 varies less than 2%/mA of drain current for gate bias voltages greater than 6 volts. The worst-case change in  $R_{ds}$  for the  $n^{\text{th}}$ -bit switch is, therefore, given by  $(2)^{-n} (4\%)$ , or  $(10/2^n)$  ohms. Output error is less than

70.000031% of half scale, because the MOSFET is used only in the low-order bits.

Assuming that all bit resistances are calibrated at one analog voltage extreme (+10 volts or -10 volts), the worst-case output error occurs when the analog input  $X$  is at the opposite extreme. Bit 0 is driven by  $X$ , and all other bits are driven by  $-X$ . The error due to bit 0 is therefore twice as great, and the error due to all other bits is zero. Maximum worst-case output error in the MDAC due to analog input variations is .00312% of half scale.

In addition to input-current variation, the SS2012 MOSFET ON resistance varies with the drive voltage  $V_{gs}$ , and therefore with power-supply drift. Variation in  $R_{ds}$  is less than 20% per volt change in  $V_{gs}$  for  $V_{gs}$  6 volts. Assuming power supply regulation of 1%, worst-case change in  $V_{gs}$  is less than 100 mV, and hence  $R_{ds}$  changes by less than 2% (or 5 ohms). Total output error for bits 5 through 11 is less than .00074% of half scale. Because the gate drives of the junction FET's used in the most significant bits are at ground when they are in the ON state, power-supply variations have no effect on the switch resistance of the first five bits. The large resistance variations in the MOSFET switches, although they have little effect on output error when used in the lower bits, are another significant reason why the MOSFET was not used for the most significant bits of the MDAC.

The precision resistors employed in the MDAC decoder network have a maximum voltage coefficient of 5 ppm/volt. Worst-case output error occurs when bit 0 is at one analog voltage extreme, and all other bits are at the other. Transfer impedances of the first 3 bits were constructed from two resistors per bit rather than one, and the maximum voltage across any precision resistor in the MDAC is thus  $\pm 5$  volts. Worst-case output error is, therefore,  $\pm 0.005\%$  of half scale.

Total worst-case output error in the MDAC due to analog input variations and power-supply drift for both the switch resistances and the bit network resistors is  $0.00886\%$ , or 0.182 LSB.

#### Leakage-Current Error

Output-voltage error due to leakage current is equal to the feedback resistance (10K ohms) times the sum of all leakage currents. In the ON state, output error is caused by collector leakage in the shunt transistor and by gate leakage in the FET. In the OFF state, error is caused by FET gate cutoff current. Because the collector-to-emitter voltage of the cutoff NPN transistor is never more than 25 mV, collector leakage of the 2N3904 was less than 40 picoamperes at 25°C in all cases measured. Specified maximum gate leakage at 25°C is 0.2 nanoamperes for the JFET and 1 picoampere for the MOSFET. Leakage currents of

both the JFET and the shunt transistor double with every  $10^{\circ}\text{C}$  of temperature increase. Because the drain is grounded in the OFF state, drain-to-source cutoff current of the FET is negligible compared to gate cutoff current. Assuming a maximum operating temperature of  $40^{\circ}\text{C}$ , worst-case total output voltage error due to leakage currents in all bits is less than 50  $\mu\text{V}$ .

Special care must be taken to remove all excess solder flux from printed-circuit boards when constructing accurate analog circuits such as a MDAC. If excess flux is not properly removed, it can produce leakage current errors larger than those due to the transistor leakage currents.

#### Errors Caused by Temperature Drift of Network Impedances

A significant error in the MDAC is that caused by variations in switch resistances, potentiometer resistances, and precision resistor values as a function of temperature. Although precision resistors with small temperature coefficients are used, the small variation can be quite significant. While switch and trimmer resistances have smaller absolute values, they have much larger temperature coefficients than the fixed resistors. Fortunately, because most of the error is due to the first few bits, temperature error can be minimized by careful design of the channels for these bits.

Because the effect on output error of the  $n^{\text{th}}$ -bit switch resistance varies as  $(2)^{-2n}$ , the error caused by the switch in bit 0 exceeds the sum of the errors in all other bits. To minimize output error, therefore, the JFET in bit 0 is selected for an ON resistance of less than 20 ohms.

Since temperature-drift effects in the switches of bits 1 to 11 tend to partially cancel the drift of the switch of bit 0 (which has an analog input of opposite polarity), the worst-case output switch-drift error occurs when only bit 0 is ON and has maximum drift.

The T1S41 has a temperature coefficient of  $+0.65\%/^{\circ}\text{C}$  to  $0.7\%/^{\circ}\text{C}$ . As a conservative estimate, the SS2012 MOSFET is assumed, for purposes of worst-case analysis, to have a minimum temperature coefficient of  $0.1\%/^{\circ}\text{C}$ . Using the relations of Table III, the maximum output voltage drift (in per cent of half scale) due to bit 0 switch drift is  $+0.0014\%/^{\circ}\text{C}$ ; and the minimum output drift due to bits 1 through 11 is  $-0.000375\%/^{\circ}\text{C}$ . The worst-case output drift is therefore  $+0.029 \text{ LSB}/^{\circ}\text{C}$ . At digital zero crossing (when all switches change state), where temperature drift is most likely to effect MDAC monotonicity, worst-case drift is  $+0.0212 \text{ LSB}/^{\circ}\text{C}$ .

Over the temperature range under consideration, the carbon trimmers have a negative temperature coefficient of

-600 ppm/°C maximum; and the wirewound trimmers have a negative coefficient of -50 ppm/°C maximum. The worst-case trimmer drift corresponding to worst-case FET drift occurs when bits 1 and 2 have maximum drift and all other trimmers are at zero. Output drift caused by the trimmers for this case is +0.000094%/°C, bringing the total worst-case output temperature drift due to trimmers and switches to +0.031 LSB/°C and the total maximum drift in resolution at digital zero crossing to +0.023 LSB/°C.

The other extreme case exists when FET drift is minimum in bit 0 and maximum in all other bits, and when trimmer drift is zero in bits 1 and 2 and maximum in all other bits. For this case, worst-case output drift due to all switches and trimmers is -0.029 LSB/°C; but maximum drift in resolution at digital zero crossing is less than -0.01 LSB/°C. Most of the error for this case comes from trimmer drift rather than from FET resistance drift.

Worst-case output error due to the temperature coefficients of the fixed metal-film resistors occurs when bit zero has maximum variation in one direction, and all other bits have maximum variation in the opposite direction. For ±50 ppm/°C resistors, this could cause an output voltage drift error of ±0.01%/°C, or approximately 1/5 LSB/°C. This would mean that, even with zero switch error, 12-bit resolution could be guaranteed over less than a ±2.5°C temperature range.

In actual fact, most of the error in MDAC's occurs in the first few bits, so that good temperature tracking of impedances in these bits would eliminate most of the temperature error. A measured sample of the particular type of metal-film resistors used was found to have positive temperature coefficients in all cases over the range of 25°C to 40°C, thereby reducing the range of possible temperature coefficients by a factor of two and reducing the worst-case output drift to 1/10 LSB/°C. Furthermore, resistors of values differing by less than an order of magnitude had similar temperature coefficients in most cases. For this reason, the first 3 bits were constructed from resistors of values varying by less than one order of magnitude in order to minimize drift in these bits. Because of the temperature-tracking properties just described, the normal expected error due to fixed resistors should be on the order of 1/20 LSB/°C.

The temperature drifts of the precision resistors are the greatest potential source of error in a high-resolution MDAC. Design under worst-case conditions would require temperature tracking of only a few ppm/°C for good temperature stability. If a MDAC is to be used where temperature conditions are not closely controlled, a single-package metal-film resistance network, and preferably a ladder network, should probably be used.

Total worst-case temperature drift due to all temperature coefficients is  $\pm 0.133$  LSB/ $^{\circ}$ C. Normal temperature drift is much lower than that indicated by worst-case analysis. Results of temperature testing of the MDAC showed a drift of less than 0.02 LSB/ $^{\circ}$ C with all switches ON.

#### High-Frequency Errors and Equalization

Unavoidable capacitances in the MDAC resistor network can lead to phase-shift errors at the output for high frequency analog inputs. Fortunately, compensating techniques are available to reduce this error.

Fixed precision resistors have capacitances associated with them. For this reason, the impedance level was limited to 10K ohms, and the maximum resistor used was limited to 40.2K ohms.

FET gate-to-source and gate-to-drain capacitances also present problems. When a FET is in the ON state, the equivalent capacitance from source to drain and from source to ground cause reduction in frequency response of the device. This error is worse for JFET's than for MOSFETS because of the larger junction capacitances in JFET's.

Another source of capacitance (and inductance) is the wirewound trimmers used in the first three bits. This capacitance and inductance varies with the trimmer setting. Because of their poor frequency response, the trimmers are

limited to a maximum of 2% of the total transfer impedance in bit 0 and 2.5% in bits 1 and 2.

Simple frequency-response equalization techniques may be used to minimize output phase-shift error if desired. The feedback resistance of the operational amplifier is split into two 5K resistors. Phase-shift error may be minimized by inserting a capacitor from the center of the feedback resistance to ground (Fig. 2). This capacitor is chosen experimentally and has a value of 10pF. to 20 pF.. When equalization is used, the total MDAC dynamic error is less than 0.1% of half scale at computing frequencies of 10 Khz (Fig. 12a).

#### Errors Caused by Switching Spikes

The gate-to-drain junction capacitances of field effect transistors cause current spikes at the summing junction when the FET is switched. The resulting output voltage spikes are not important in many high-speed hybrid computations, where MDAC's are most commonly used to change parameters in the RESET period between analog-computer runs. Switching-spike error would only come into consideration when switching is to occur many times during a computer run and when spike errors might integrate into cumulative errors. Even when used in these applications, the errors caused by switching spikes are usually negligible because of the extremely short duration of the spikes.

Capacitors used to reduce switching spikes are inserted at the summing junction rather than at the source of each FET to minimize their effect on frequency response. Because the maximum voltage swing at the summing junction is  $\pm 100 \mu\text{V}$ , the frequency-response error caused by the 55 pF equivalent capacitance of spike-compensating capacitors at the summing junction is less than  $3.5 \mu\text{V}$  at 10 KHz.

## CONSTRUCTION, TESTING, AND RESULTS

Each MDAC is mounted on two 2 7/8 in. by 9 in. printed circuit cards, with the power-supply filters and five most significant bits on one card, and with the seven least significant bits on the other. Separate digital and analog ground planes are utilized to prevent digital noise on the analog ground, to prevent high current flow in the analog ground, and to minimize resistance in the analog ground. Too much resistance in the analog ground could cause potential variation along the ground plane which would lead to errors in binary weighting of the transfer impedances in the bits using T-networks. Both power supplies are filtered with pi-network filters to keep the switch-transients away from the LOCUST power supply.

The two MDAC cards mount in a 3"x10"x1" shielded can which plugs directly into the LOCUST analog patchbay. This eliminates all analog wiring between the patchbay and the MDAC. The can is a modified version of the 2"x10"x1" can used for other LOCUST computing elements (Conant 1967), with analog-signal and power supply-inputs at one end of the can, and a 12-pin connector for the 12 digital-signal lines at the other end. Trimmer potentiometers are mounted so that they may be adjusted externally for calibration of binary weighting after the MDAC is in place in the computer.

The fully assembled MDAC is shown in Fig. 7. The operational amplifier is not included in the MDAC can, but it is patched externally on the analog patchbay and is thus available for other uses when MDAC's are not in operation. The feedback network, however, is included in the MDAC card. A fuse is placed in the amplifier input lead ( $G^i$ ) to protect the switches in the event of erroneous patching. Because the fuse is inside the amplifier feedback loop, its resistance causes negligible error. Analog patching on the LOCUST patchbay is shown in Fig. 8. Two analog inputs,  $+X_A$  and  $-X_A$ , are required, and an uncommitted amplifier is patched externally with its summing junction at  $G^i$  and its output at  $O^i$ . Four MDAC channels are included in the LOCUST system.

#### Calibration

Calibration of the MDAC is done with the device installed in the computer. Either a +10 volt or a -10 volt input is applied to both the  $+X$  and  $-X$  inputs on the analog patchbay. Calibration of binary weighting proceeds from the least significant bit to the most significant bit. To calibrate a given bit, the digital input is switched repeatedly from a digital "1" in the bit to be calibrated to digital "1"'s in all less significant bits. All other bits are at digital "0". The difference in MDAC output voltage for the two digital numbers should be 1 LSB, or 4.9 mv., in all cases. The calibrating procedure thus

consists of adjusting the trimmer in that bit until the correct voltage difference is obtained.

After binary weighting has been calibrated, the feedback resistor is matched to the resistance of the first bit. The feedback resistor is chosen by patching the feedback resistance which is to be tested from the amplifier output  $O$  to the summing junction  $G$ , with  $O'$  open circuited. The digital state of the MDAC is set to octal 4000. The feedback resistance is then selected or padded to obtain exactly  $+10$  volts at the amplifier output for  $-10$  volts at the  $+X$  analog input.

When static weighting and accuracy have been calibrated, dynamic error can be minimized by using one of the summing amplifiers in the analog computer as in Fig. 9. For an input of  $10 \sin \omega t$ , the summing amplifier output yields a convenient measure of dynamic error. Dynamic error is minimized by selecting the capacitor  $C_f$  from ground to the center of the feedback resistance (Fig. 2) so that the output of the summing amplifier at 10 KHz has minimum magnitude variation from the output magnitude at 10 Hz. Digital input to the MDAC is octal 3777. Because the output frequency response at octal 4000 is similar to that at 3777, this procedure also provides frequency response compensation for bit 0.

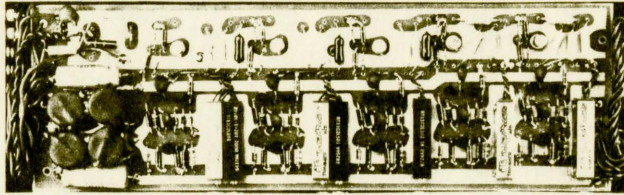


Fig. 7. Fully Assembled MDAC

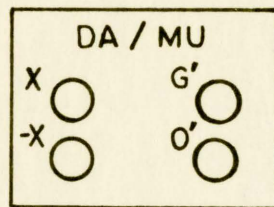


Fig. 8. MDAC Terminals On LOCUST Analog Patchbay

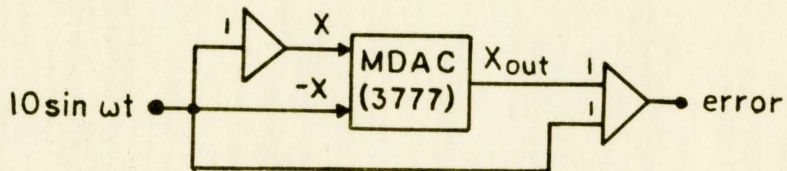


Fig. 9. Circuit For Measuring MDAC Dynamic Error

### Digital Switching Characteristics

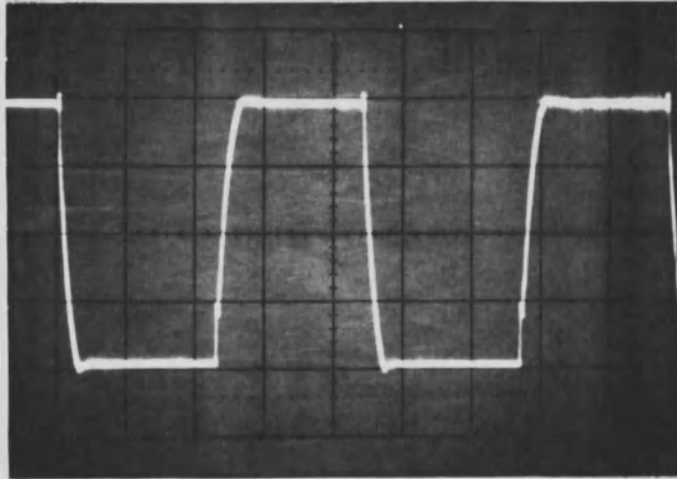
Switching delay for both the JFET and MOSFET switch is less than 40  $\mu$ sec. Settling time (to within 0.025% of half scale) at the MDAC output is less than 5  $\mu$ sec with all switches changing state, and worst-case rise and fall times when switched between +10 volts and -10 volts are less than 1.5  $\mu$ sec.

Figure 10 shows the MDAC output for a 10 volt d.c. analog input with digital states switching between octal 4000 and 3777 as an illustration of worst-case rise and fall time. Output voltage plus transient spikes remain less than  $\pm 10.5$  volts, so that the operational amplifier cannot overload because of switching spikes.

Figure 11a shows the switching spikes at the MDAC output for a typical JFET switch. The upper trace is the output voltage with  $X_A=0$ , and the lower trace is the digital drive signal at the switch input. The transient at the left is the turn-on-spike, while the turn-off spike appears at the right. Figure 11b shows switching spikes for a typical MOSFET switch, and Fig. 11c shows worst-case switching spikes occurring when all 12 switches change states. The worst-case switching spike is  $\pm 2.8$  volts.

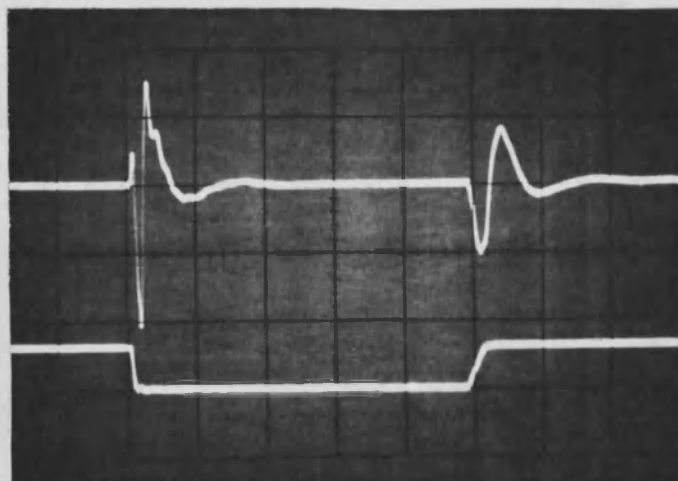
### Dynamic Characteristics

Figure 12a shows MDAC dynamic error as a function of frequency for digital states 4000, 3777, and 0000 with



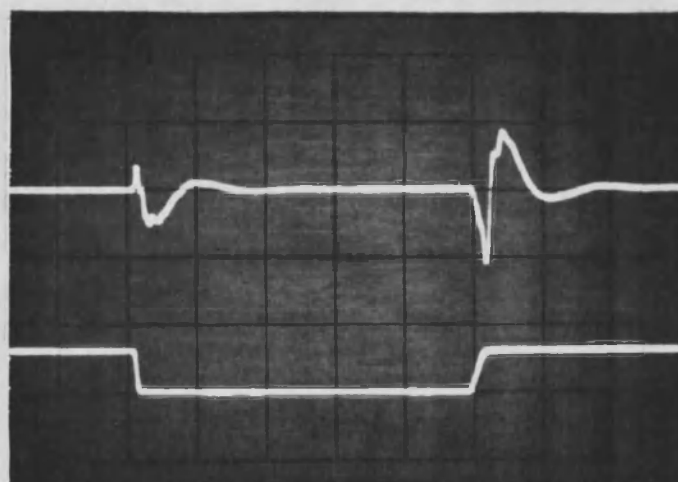
Vertical scale: 5 volts/cm  
Horizontal scale: 5  $\mu$ sec/cm

Fig. 10. Digital Switching Characteristics



Vertical scale: 0.5 volts/cm  
Horizontal scale: 1  $\mu$ sec/cm

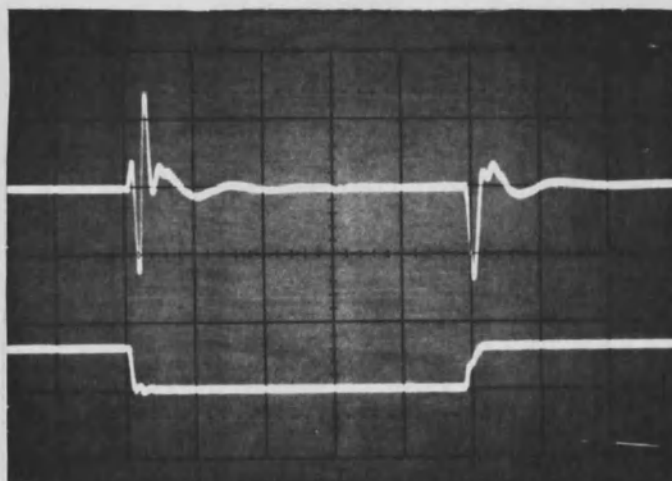
(a)



Vertical scale: 0.5 volts/cm  
Horizontal scale: 1  $\mu$ sec/cm

(b)

Fig. 11. MDAC Switching Spikes



Vertical scale: 2 volts/cm  
Horizontal scale: 1  $\mu$ sec/cm

(c)

Fig. 11. Continued. MDAC Switching Spikes

frequency response equalization of the feedback impedance. Total error is within the LOCUST specification of 0.1% at 10 KHz. Error is shown in per cent of half-scale for an analog input of  $10 \sin \omega t$ . Error at 0000 is caused by feedthrough in capacitance of the MDAC circuit card.

Figure 12b shows MDAC dynamic error for digital states 4000 and 3777 when the frequency response equalizing capacitor is not used. Error is 0.4% at 10 KHz for the uncompensated case. In comparison, the phase-shift error of the LOCUST operational amplifier when used as a unity-gain phase inverter with 10K ohm impedances is 0.15% at 10 KHz (Conant 1967).

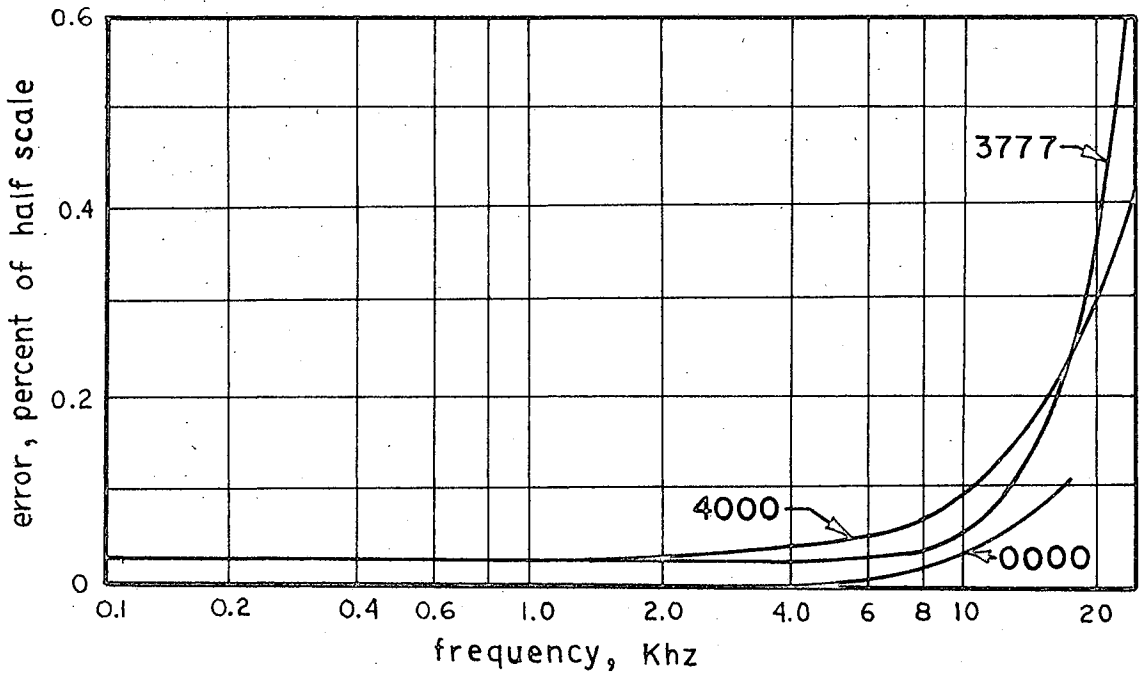
Small-signal frequency response of the MDAC is shown in Fig. 13 for digital states 4000 and 3777. Measurements were made using an analog input of  $0.1 \sin \omega t$ . Frequency response is 3 db, down at 1.5 Mhz, while frequency response of the LOCUST operational amplifier in a 10K unity gain inverter is 3 db. down at 4.5 Mhz (Conant 1967).

Temperature drift of binary resolution was measured from 25°C to 45°C for the worst-case state of octal 7777, (all switches ON) with an analog reference of +10 volts. Drift was less than 0.02 LSB/°C over the 20°C temperature range.

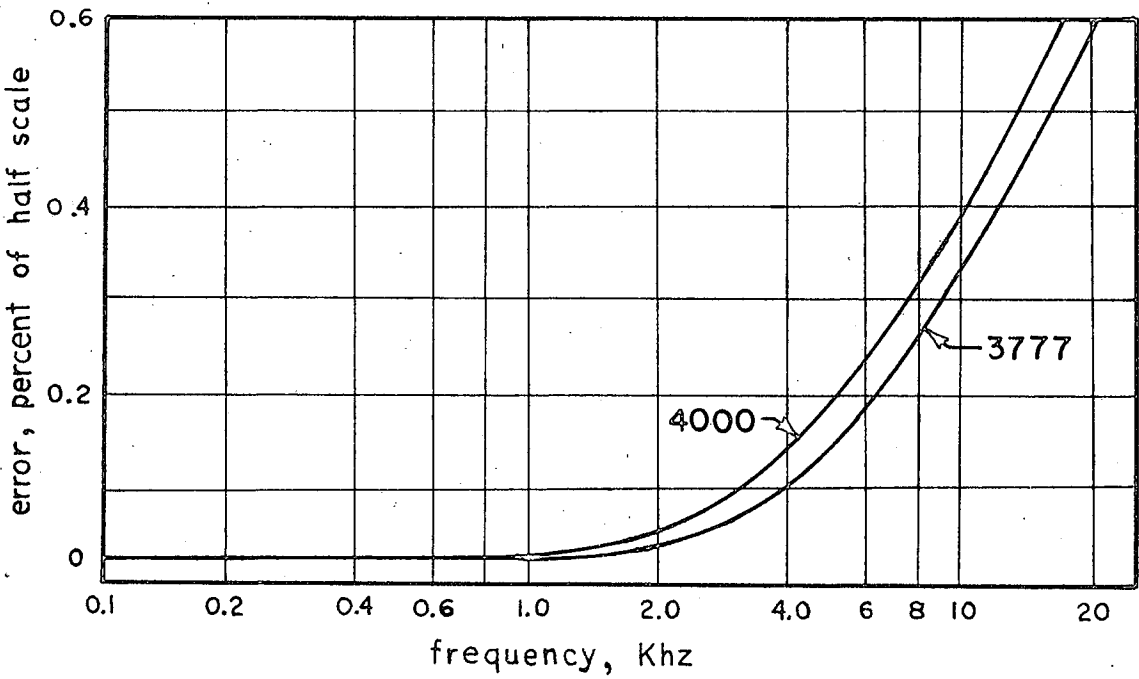
MDAC analog output response to a fast-rise-time  $\pm 10$  volt square wave applied to the analog input from a low impedance source, with the MDAC in digital state 3777, had a rise time of less than 2 microseconds, an overshoot of 7%, and a settling time (within 0.1%) of approximately 4 microseconds.

The upper trace of Fig. 14 shows the MDAC output for a 10 volt, 10 Khz. sine wave at the analog input multiplied by a digitally-generated ramp operating at maximum PDP-9 output speed. The lower trace shows MDAC output for the same 10 Khz. analog input with slowly-stepped digital attenuation.

Figure 16 shows MDAC output for a 10 volt d.c. analog input with digital steps from 7773 to 0005, illustrating MDAC monotonicity as the digital input changes sign and all switches change state.



(a)



(b)

Fig. 12. (a) MDAC Dynamic Error With Frequency Equalization and (b) Dynamic Error Without Frequency Equalization

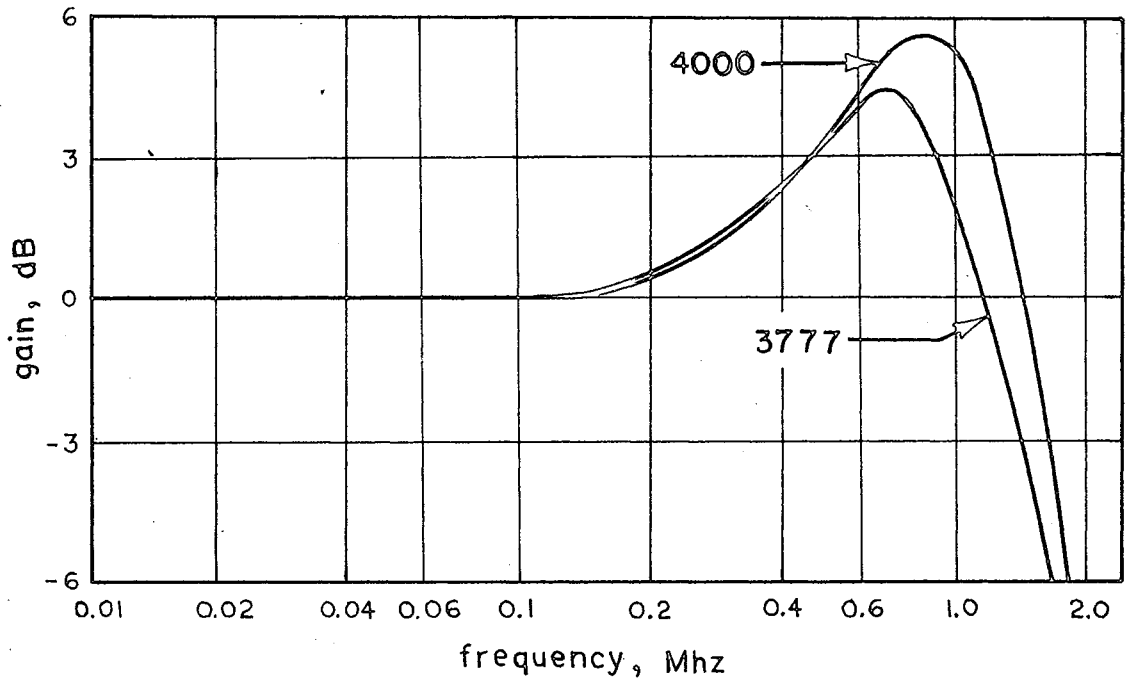
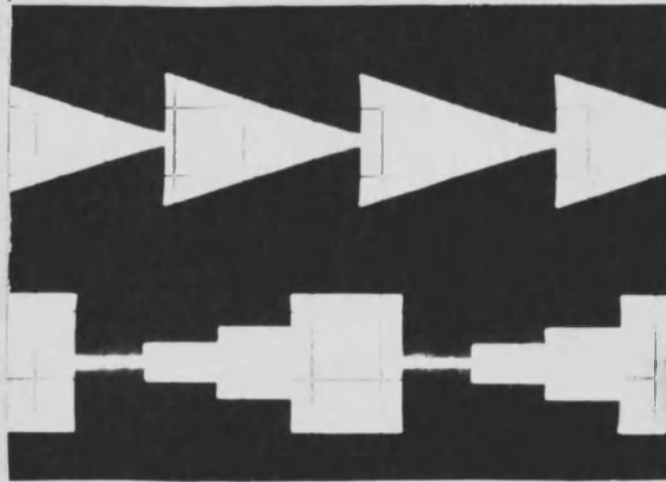
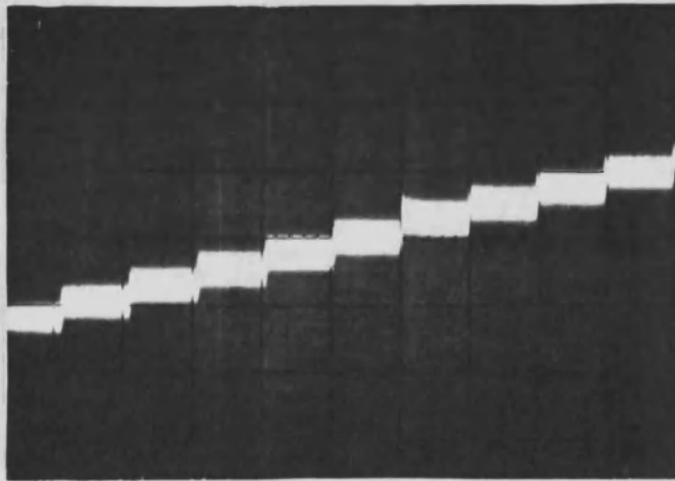


Fig. 13. MDAC Small-signal Frequency Response



Vertical scale: 10 volts/cm  
Horizontal scale: 2 msec/cm

Fig. 14. MDAC Operation at Computer Speed



Vertical scale: 20 mV/cm  
Horizontal scale: 10 msec/cm

Fig. 15. MDAC Resolution Near Digital Zero

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