THE DESIGN OF A CALIBRATION-FREE MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

by

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ABSTRACT

This paper describes the design and testing of a high-speed, 12-bit multiplying digital-to-analog converter intended for use in wideband hybrid computation. The circuit features a calibration-free bit switch employing an operational amplifier feedback loop to reduce switch forward resistance. Wideband operational amplifiers and low network impedances enhance operation at high frequencies. The multiplying digital-to-analog converter is capable of multiplying an analog signal by a digital number with a static accuracy of 0.025 per cent of half scale and a dynamic accuracy of 0.1 per cent of half scale for a ±10 volt analog input sinewave at 20 kiloHertz. Settling time for digital-input changes is 5 microseconds to within 0.025 per cent.

INTRODUCTION

This paper describes the development of a wideband 12-bit multiplying digital-to-analog converter (MDAC) with a minimum of calibration requirements.

An MDAC produces an output voltage proportional to the product of a (possibly time variable) analog input voltage and a digital number. The digital number determines the settings of n bit switches and thus the attenuation of a decoder network. To obtain good analog-input bandwidth, it is desirable to employ low resistances in the decoder network; but this makes the forward resistances of the electronic bit switches comparable to the network resistances and thus produces errors and/or the need for frequent recalibration.

The approach to this problem taken here is that of Korn, 1972, viz. to place each bit switch inside the feedback loop of an operational amplifier to reduce the switch forward resistance. This technique requires one amplifier per bit plus an output summing amplifier. If four-quadrant multiplication is desired, one more amplifier is required to invert the input signal.

Table 1. 12-Bit MDAC Specifications

Analog input voltage	±10 volts
Digital logic input levels	
ON state	+2.4 volts minimum
OFF state	+0.6 volts maximum
Static accuracy (% of half scale)	0.025% ±1/4 LSB
Dynamic accuracy (% of half scale)	0.1% at 20 kHz
Switching speed	
delay	20 ns
rise time	140 ns
settling time (within 0.025%)	1000 ns
Output error temperature drift	
worst case	±0.572 LSB/°C
typical (measured)	0.25 LSB/°C
Worst case switching spikes	±3.0 volts (no output amplifier overloads are caused by worst-case switching spikes)
Power supply requirements	±15 volts
Power supply regulation	1%
Worst case power supply drain	356 mA from +15 volts 310 mA from -15 volts
Maximum MDAC power dissipation	10.0 watts
Current drain from digital logic	0 mA at +3 volts 1.65 mA at 0 volts
Analog input impedance	1 kohms minimum

MDAC DESIGN PRINCIPLE

Figure 1 shows the principle of a weighted-resistor MDAC. The n-bit decoder network consists of n binary weighted transfer impedances (Korn and Korn, 1972), R, 2R, . . . , 2^{n-1}R as shown in Figure 1a. Since the high gain and negative feedback of the output amplifier maintain a virtual ground at its input, the bit currents flowing into the summing junction are binary weighted, with $-X_{IN}/R$ in the MSB and $X_{IN}/2^{n-1}R$ in the LSB. The individual bit currents are switched on or off depending on whether a digital 1 or 0 is present at its logic input. A digital 2's complement number, $X_D = X_0 \ . \ . \ . \ X_n$, then allows an analog voltage, X_{OUT}, at the amplifier output where

$$X_{OUT} = X_{IN} R_f [X_0/2^0R - X_1/2^1R - . . . - X_{n-1}/2^{n-1}R]$$

Figure 2 shows one of the bit networks of an MDAC employing shunt-switched T-networks to produce each binary-weighted bit current. This type of network permits reasonable resistance values even for the smallest bit currents and can use a simple single-throw electronic switch grounded at one end.

The operational amplifier switch designed for this MDAC acts as this switch. In the ON mode, the amplifier is switched out of the T-network and the grounded element of the "T" uses the amplifier input as a virtual ground. In the OFF mode, the grounded element of the "T" becomes the feedback resistor for the amplifier. Since there are no summing resistors, the amplifier output is zero thus effectively grounding the center of the T-network.

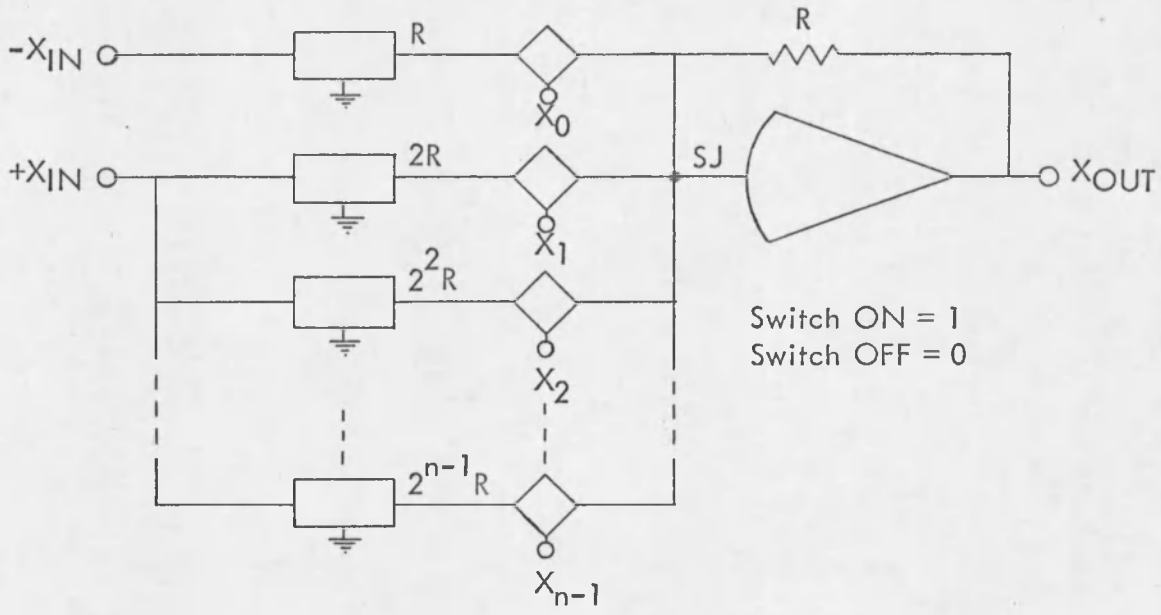


Fig. 1. n-Bit Decoder

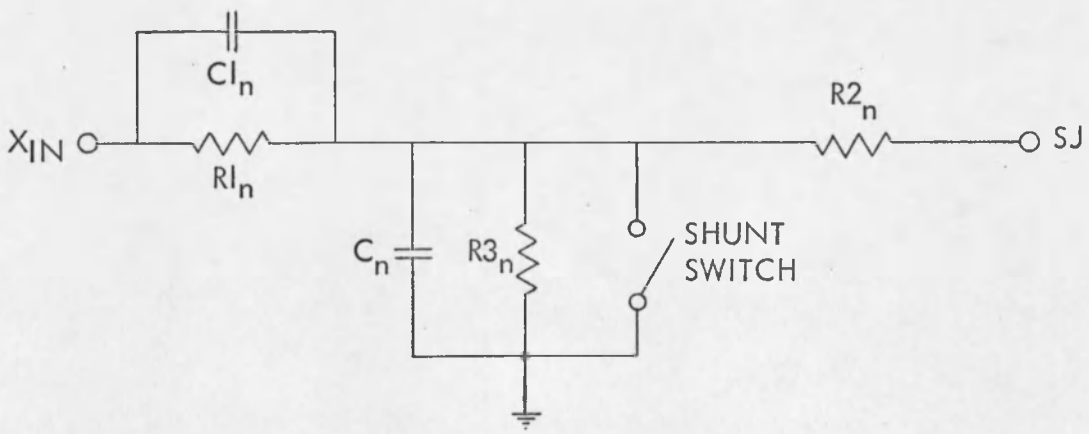


Fig. 2. n^{th} Bit Decoder

THE DECODER NETWORK

In Figure 2, C_n is the equivalent capacitance to ground of the shunt switch when opened. Note that when the switch is closed, the input impedance is equal to RI_n and the impedance seen by the output amplifier is $R2_n$. The minimum input impedance of the entire decoder network at d.c. is given by

$$Z_{IN} = \frac{1}{\sum_{n=1}^{11} \left(\frac{1}{RI_n}\right) + \frac{1}{R_x}} \tag{2}$$

where R_x is the input impedance of the inverter used to drive Bit 0. The minimum impedance seen by the operational amplifier at d.c. is given by

$$Z_a = \frac{1}{\sum_{n=0}^{11} \left(\frac{1}{R2_n}\right)} \tag{3}$$

Both of these impedances are minimized when the digital input is equal to (0 ··· 0). Since Z_{IN} presents a load on the preceding stage or source, the error is minimized when Z_{IN} is kept as large as possible.

If the operational amplifier used for the summing amplifier has a unity-gain frequency of f_s, has an open loop gain response in the region around f_s of -20 dB per decade, and if stray capacitance is neglected, the worst case -3 dB bandwidth of the summing amplifier is given in terms of the feedback ratio, $Z_a/(Z_f + Z_a)$, (Korn and Korn, 1972) as

$$F_{CL} = f_s \left(\frac{Z_a}{Z_f + Z_a}\right) \tag{4}$$

It is apparent from Equation 4 that the bandwidth is maximized when the feedback ratio, $Z_a/(Z_f + Z_a)$, is maximized. Since the value of Z_f is dictated by the MDAC gain, Z_a must be maximized.

The n^{th} bit current injected into the summing junction is directly proportional to the short circuit transfer impedance of the n^{th} bit summing network. When the switch in Figure 2 is opened, the circuit (without Cl_n) becomes a T-network having a transfer impedance given by

$$Z_{bn}(s) = Rl_n + RZ_n + \frac{Rl_n\ R2_n}{R3_n} + Rl_n\ R2_n\ C_n\ s \tag{5}$$

The ideal value for $Z_{bn}(s)$ can be found by setting $s = 0$ yielding

$$Z_{bn}(0) = Rl_n + RZ_n + Rl_n\ R2_n/R3_n \tag{5a}$$

Since the output voltage due to the n^{th} bit is inversely proportional to $Z_{bn}(s)$ as shown in Equation 1, the -3 dB bandwidth of the n^{th} bit, F_n, is the frequency where $s = j\,2\pi F_n$, i.e.

$$\left| Z_{bn}\ (j\,2\pi F_n) \right| = 2\ Z_{bn}(0) \tag{5b}$$

or where

$$Rl_n + R2_n + Rl_n\ R2_n/R3_n = \left| Rl_n\ R2_n\ C_n\ j\,2\pi F_n \right| .$$

Dividing by $Rl_n\ R2_n\ C_n\ 2\pi$ and finding the absolute value results in

$$F_n = \left(\frac{1}{Rl_n} + \frac{1}{R2_n} + \frac{1}{R3_n}\right)\ \left(\frac{1}{2\pi C_n}\right). \tag{5c}$$

To maximize F_n; Rl_n, $R2_n$, and $R3_n$ as well as C_n should be small. If C_n is constant with frequency, its effects can be compensated by capacitor, Cl_n, in parallel with Rl_n of value $R3_n\ C_n/Rl_n$. This forms a "compensated attenuator" similar to oscilloscope probes. However, due to slight peaking in the response of

the output amplifier, the required value for Cl_n was found to be smaller than $R3_n\ C_n/Rl_n$. For the six less significant bits, the value was negligible (less than 4 pF). Because of the small size of Cl_n, it was neglected in calculating values for the T-networks. The requirements indicated by the preceding equations are conflicting; therefore, a compromise must be reached between Equations 2 and 4 on the one hand and Equation 5c on the other.

OPTIMIZATION OF T-NETWORK IMPEDANCES

Two limitations were placed on the impedance values used in the decoder network. The worst-case input impedance, Z_{IN}, must be 1 kilohm or greater, and the smallest value of resistor used must be 10.1 ohms or greater. The first restriction prevents excess loading of the preceding stage and restricts the use of $C1_n$. The second restriction allows the use of commonly available metal-film resistors throughout the decoder. This restriction could be modified if wire-wound resistors or thin film networks were used in the decoder.

A compromise between reduced output-amplifier feedback (Equation 4) and reduced MDAC input impedance is achieved by setting $R1_n = R2_n$. Neglecting the inversion of bit 0, the required gain of the n^{th} bit is 2^{-n}. Therefore,

$$\frac{R_f}{R1_n + R2_n + R1_n\, R2_n/R3_n} = 2^{-n} \tag{6}$$

If $R1_n$ and $R2_n$ are set equal to $R(2^{n/2})$ and R_f is set equal to RG (scale factor G to be determined by the choice of output summing amplifier), Equation 6 is reduced to

$$2\,R(2^{n/2}) + R^2(2^n)/R3_n = RG(2^n)$$

or

$$R3_n = R/(G - 2^{1-n/2}) \tag{7}$$

Substituting for $R1_n$, $R2_n$, and $R3_n$ in Equation 5c yields

$$F_n = \frac{G}{2\pi R C_n} \tag{8}$$

Choosing a scale factor for $R1_n$ and $R2_n$ greater than $2^{n/2}$ will cause a reduction in the bandwidth of the less significant bits. If the scale factor is less than $2^{n/2}$, the value of Z_a is lowered resulting in a reduction in the bandwidth of the summing amplifier as seen in Equation 4.

The value of R is determined by substituting $R(2^{n/2})$ for $R1_n$ in Equation 2, arbitrarily setting R_x equal to 10 kilohms, and setting Z_{IN} = 1 kilohm. This yields a value of 2.613 kilohms for R.

Using the Burr-Brown Model 3400B wideband operational amplifier and the operational amplifier switch described in succeeding sections of this thesis, the value of G was determined by setting F_{CL} in Equation 4 equal to F_n in Equation 8. C_n was measured and found to be 19 picofarads, and the unity-gain bandwidth, f_s, is specified by the amplifier manufacturer as 100 megaHertz. This yields a value of 2.90 for G. Setting $R_f = RG$ yields a value of 7.582 kilohms for the feedback resistor. Using Equation 7 and setting $R1_n = R2_n = R(2^{n/2})$, the values for $R1_n$, $R2_n$, and $R3_n$ were determined and are listed in Table II.

Table II. Decoder Network Resistance Values

N	$R1_n$ (IN kΩ)	$R2_n$ (IN kΩ)	$R3_n$ (IN kΩ)
0	2.613	2.613	2.89829
1	3.69534	3.69534	1.75681
2	5.226	5.226	1.37413
3	7.39068	7.39068	1.19073
4	10.452	10.452	1.08804
5	14.7814	14.7814	1.02551
6	20.904	20.904	0.985456
7	29.5627	29.5627	0.958973
8	41.808	41.808	0.941091
9	59.1254	59.1254	0.928843
10	83.616	83.616	0.920373
11	118.251	118.251	0.914477

THE OPERATIONAL AMPLIFIER SWITCH

Basic Switch Design

The basic circuit of the operational-amplifier switch is shown in Figure 3. For the bit to be ON, S1 is opened and S2 is closed. The equivalent impedance to ground, R3' (ON) is found by assuming a voltage, E, at the junction of R1, R2, and R3 calculating the current, I, caused by the presence of E in terms of the amplifier output voltage, V, and gain, -A. R3' (ON) is the ratio of E to I:

$$I = \frac{E - V/(-A)}{R3} + \frac{E - V}{R_{OFF}} \tag{9a}$$

$$0 = \frac{E - V/(-A)}{R3} + \frac{V - V/(-A)}{R_{ON}} \tag{9b}$$

Equation 9b is found by assuming that the amplifier input current is zero and therefore the current in R3 is equal to the current in R_{ON}. By solving for V in Equation 9b, substituting it into 9a, and then dividing E by I, R3' (ON) is found to be

$$R3'\ (ON) = \frac{1}{\frac{1}{R3} + \frac{1}{R_{OFF}} + \left(\frac{1}{R_{OFF}} - \frac{1}{A\,R3}\right)\Big/\left(\frac{1}{A} + \frac{R3}{R_{ON}}\left(1 + \frac{1}{A}\right)\right)} \tag{9c}$$

If the amplifier gain, A, is large compared to $R3/R_{ON}$ and 1, Equation 9c reduces to

$$R3'\ (ON) \approx \frac{1}{\frac{1}{R3} + \frac{1 + R_{ON}/R3}{R_{OFF}} + \frac{1}{-A\,R3^2/R_{ON}}} \tag{10}$$

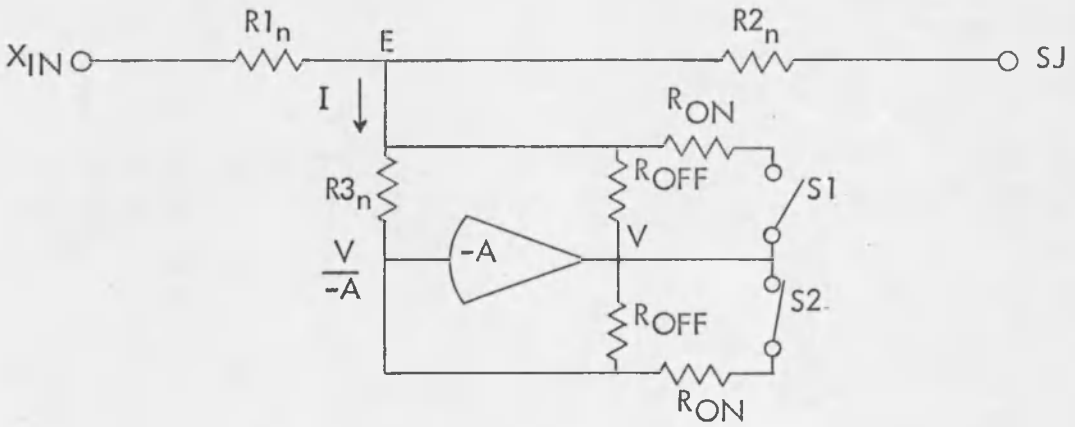
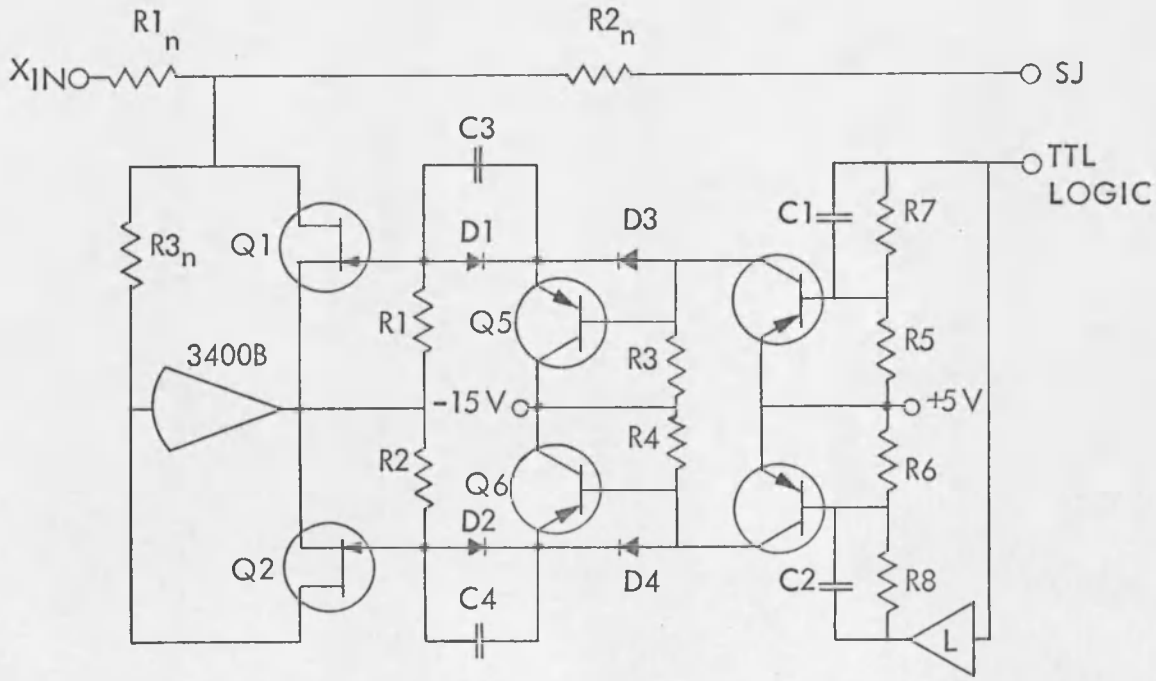


Fig. 3. Basic Operational Amplifier Switch



Q1,2	TIS41	R3,4	10 kΩ
Q3,4,5,6	2N3906	R5,6	1.5 kΩ
C1,2	100 pF	R7,8	8.2 kΩ
C3,4	22 pF	D1,2,3,4	IN4154
R1,2	18 kΩ	L	(1/6) SN7404

Fig. 4. Complete Operational Amplifier Switch

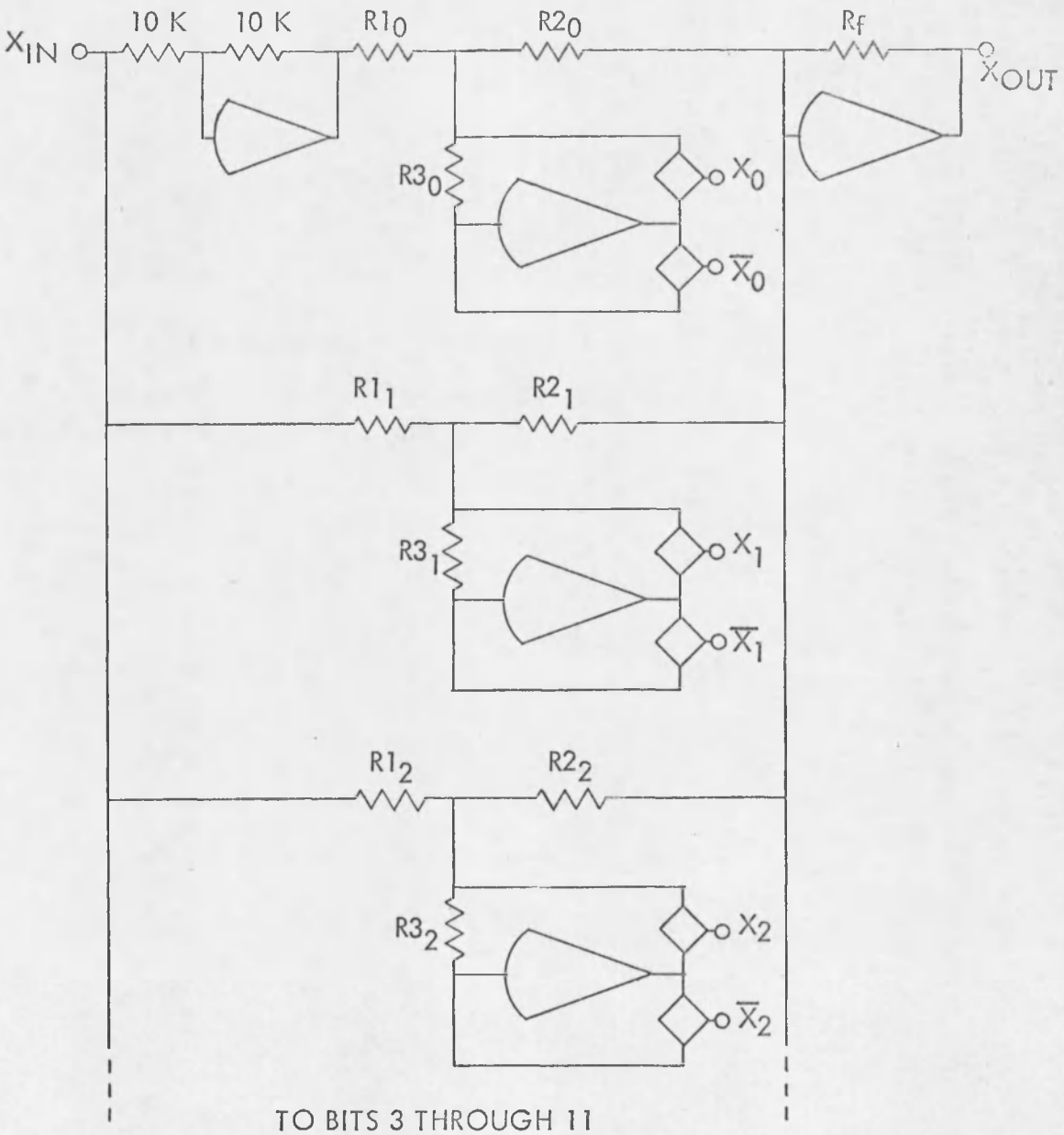


Fig. 5. MDAC Circuit

This is equivalent to three parallel resistors of values R3, $R_{OFF}/(1 + R_{ON}/R3)$, and $-A\,R3^2/R_{ON}$. The negative value of the third resistor tends to increase R3' (ON) as compared to R3. Typical values for R_{ON}, R_{OFF}, and A are 30 ohms, 100 megohms and 100,000 volts per volt at d.c. These are typical of the Texas Instruments Model TIS41 and the Burr-Brown Model 3400B. With these values and a worst case of 2.9 kilohms for R3, the second and third terms in Equation 10 are 99 megohms and -28,000 megohms. At d.c., both of these are taken into account in the initial adjustment of R3. With increasing frequency, the value of A decreases. For the Model 3400B, the open loop gain is approximately 100 volts per volt at 1 megaHertz. This allows the third term in Equation 10 to decrease to -28 megohms. This causes R3 to appear 0.01% larger which is negligible compared to phase shift errors in the output amplifier of over 5° at 1 megaHertz.

If S1 is closed and S2 opened, the bit is turned OFF. R3' (OFF) is found in the same manner as R3' (ON) and is described as

$$R3'\ (OFF) = \frac{1}{\frac{1}{R3} + \frac{1}{R_{ON}} + \left(\frac{1}{R_{ON}} - \frac{1}{A\,R3}\right) \Big/ \left(\frac{1}{A} + \frac{R3}{R_{OFF}}\left(1 + \frac{1}{A}\right)\right)} \qquad (11)$$

Again, assuming A is large compared to 1, Equation 11 reduces to

$$R3'\ (OFF) \doteq \frac{1}{\frac{1}{R3} + \frac{1 + R_{OFF}/R3}{R_{ON}} + \frac{1}{-A\,R3^2/R_{OFF}}} \qquad (12)$$

This is equivalent to three parallel resistors of values R3, $R_{ON}/(1 + R_{OFF}/R3)$, and $-A\,R3^2/R_{OFF}$. Using the typical values given earlier for R_{ON}, R_{OFF}, and A, and the value of 2.9 kilohms for R3, the second and third terms in Equation 12

are 0.88 milliohms and -8.4 kilohms. Since the desired value for R3' (OFF) is zero, there is no practical way to compensate for these values. However, the size of the third term indicates that R3' (OFF) should not increase appreciably with frequency within the useable spectrum. The 0.88 milliohms in Bit 0 causes an output error of 9.8 microvolts at d.c. as shown below:

$$E_{OUT} = E_{IN} \left(\frac{R_f}{R1 + R2 + R1R2/R3' (OFF)} \right)$$

$$E_{OUT} = 10 \left(\frac{7.58\ K}{2.61\ K + 2.61\ K + (2.61\ K)^2/0.88\ m\Omega} \right)$$

$$E_{OUT} = 9.8 \times 10^{-6} \text{ volts.}$$

The circuit of the complete operational amplifier switch is shown in Figure 4. Q1 and Q2 are the FET's which perform the switching functions of S1 and S2. Q3 and Q4 provide the high level drive required by the FET's. A standard TTL hex inverter is used to supply inverted logic to Q4.

The ON State

With the logic input at 2.4 volts minimum, Q4 is on and Q3 is off. The collector of Q4 is saturated near the 5 volt supply which reverse-biases D2 and allows R2 to hold Q2 on with $V_{GS} \approx 0$. With Q2 on, the amplifier output is within millivolts of zero, enabling R2 to maintain V_{GS} at zero. With Q3 turned off, its collector voltage is approximately -15 volts. The current through R1 is absorbed by the emitter follower, Q5, thus maintaining approximately -15 volts on the gate of Q1. This results in the largest possible off resistance of Q1.

The OFF State

With the logic input at 0.4 volts maximum, Q3 is on and Q4 is off. Since the switch drive circuitry is symmetric, Q1 will be turned on and Q2 turned off. With Q2 off, no current flows in the amplifier feedback resistor and the bit current is shunted to ground by Q1. Since no current flows in the feedback resistor, the voltage at the center node of the T-network equals the input offset voltage of the amplifier.

Transient Considerations

The switching-transistor drive circuitry was designed around a 5.0 volt supply using silicon PNP transistors. This insured that the OFF to ON transition of the FET gate voltage was faster than the ON to OFF transition, so that the amplifier always has feedback; this reduces switching transients. Base drive capacitors, C1 and C2, were added to neutralize the effects of stored charge in Q3 and Q4. Switching time was also reduced by the addition of Q5 and Q6. They isolate the collectors of Q3 and Q4 from the FET gate capacitance. C3 and C4 reduce the turn on time caused by the charging of the FET gates through R1 and R2. FET switching is accomplished within 100 nanoseconds turning on and within 300 nanoseconds turning off. The overall transient response of a given bit is then determined by the choice of amplifier, by the FET gate capacitance, and by the amplifier feedback resistor.

SELECTION OF AMPLIFIERS

The requirements placed on the amplifier used in the individual bit switches are quite simple. The frequency response needs to be as high as possible and the offset and drift of the input voltage and current need to be as small as possible. Otherwise, an inverting amplifier having an open loop gain of 60 dB and a rated output of ±1 volt at ±3 milliamperes will suffice.

The good input characteristics of FET-input amplifiers is desirable. However, the high frequency response requirement eliminates the use of monolithic and hybrid integrated circuit amplifiers. The Burr-Brown Model 3400B discrete operational amplifier was chosen because of its fast settling time and high frequency response combined with an FET-input. Using this amplifier, switching is accomplished in less than 1.0 microseconds for any combination of bits.

The inverter for bit 0 and the output summing amplifier require high slew rates and wide bandwidths. These requirements were also met by the Model 3400B.

ERROR ANALYSIS

To insure 12-bit resolution, the worst-case static error for any possible digital number should be less than or equal to one-half the least significant bit (LSB). Worst case errors in resolution occur near digital zero crossing, where all bits change state. For a 12-bit MDAC, the total allowable, non-monotonic, static binary error is therefore $1/2\ \text{LSB} = 1/(2)^{12} = 0.0244\%$ of half scale.

The effect of a variation in a given T-network component on the output voltage was found by differentiating the expression for MDAC gain with respect to that component. The expression is converted to a percentage by multiplying by the component and dividing by the gain expression.

The output, Q_n, corresponding to any one bit-input is

$$Q_n = \frac{-R_f V_{IN}}{R1 + R2 + R1R2/R3} = -\frac{R_f V_{IN}}{Z_{IN}}$$

where $R_f = RG$, $R1 = R2 = R2^{n/2}$, $R3 = R/(G-2^{1-n/2})$, and $Z_n = R\,G\,2^n$. Now

$$\frac{dQ}{dR1} = \frac{R_f V_{IN}}{Z_n^2}\left(1 + \frac{R_2}{R_3}\right) = \frac{dQ}{dR2}$$

Worst errors occur if V_{IN} = 10 volts = half-scale voltage. Therefore,

$$\frac{\%\ \text{output error (\% of half-scale)}}{\%\ \text{resistance error in R1 or R2}} = \frac{R1}{Z_n\,2^n}\left(1 + \frac{R_2}{R_3}\right)$$

$$= 2^{-n}\left(\frac{1}{G2^{n/2}} - 1\right)$$

Similarly

$$\frac{dQ}{dR3} = -\left(\frac{R_f V_{IN}}{Z_n^2}\right)\left(\frac{R1\ R2}{R3^2}\right) \text{ and therefore}$$

$$\frac{\%\text{ output error (\% of half-scale)}}{\%\text{ resistance error in R3}} = -\frac{R1\ R2}{R3\ Z_n 2^n} = -2^{-n}\left(\frac{2}{G2^{n/2}} - 1\right).$$

Table III contains a summary of these relationships.

Resistance Errors Caused by Input Voltage Variation

The precision resistors employed in the MDAC T-networks have a maximum voltage coefficient of 5 ppm/volt. Worst case error occurs when the analog input voltage is at either extreme and all bits are turned on. The voltage across RI_n is given by $V_{RI_n} = V_{IN}\,(RI_n + R3_n/(RI_n + 2\,R3_n))$ and the voltage across $R2_n$ and $R3_n$ is given by $V_{R2_n} = V_{R3_n} = V_{IN}\,(R3_n/(RI_n + 2\,R3_n))$. Setting V_{IN} = 10 volts and using the terms in Table III, the worst case output error due to input voltage variation is ±0.00883% of half scale.

Table III. Output Error Caused by T-network Impedance Errors

Component (n^{th} Bit)	% Error in Output Voltage / % Error in Component
R_f	+1
RI_n	$2^{-n}\left(\frac{1}{G \cdot 2^{n/2}} - 1\right)$
$R2_n$	$2^{-n}\left(\frac{1}{G \cdot 2^{n/2}} - 1\right)$
$R3_n$	$-2^{-n}\left(\frac{2}{G \cdot 2^{n/2}} - 1\right)$

Errors Caused by Temperature Drift

There are three sources of error related to temperature drift. The first is gain errors caused by changes in T-network or FET ON resistances. Because bit 0 is opposite bits 1 through 11 in polarity, the drift effects of bits 1 through 11 tend to cancel that of bit 0. The worst case occurs when only bit 0 is on and has maximum drift.

The TIS41 has an on resistance temperature coefficient of +0.7%/°C (Eddington, 1970). The resistors used in the T-networks have coefficients of ±100 ppm/°C max. Using the relations in Table III and Equation 10, the maximum output voltage drift is -0.0162%/°C or 0.332 LSB/°C.

The second source of error due to temperature drift is caused by the operational amplifier input offset drift. The error due to drift of a bit switch amplifier is $[G\,(2^{-n/2}) - 2^{(1-n)}]\,V_{os}$ in the on state and is $[G\,(2^{-n/2})]\,V_{os}$ in the off state where V_{os} is defined as the amplifier drift in μV/°C. The worst case is when all bits are off and all amplifiers drift in the same direction. The worst case for output amplifier drift also occurs when all bits are off causing the feedback ratio to be at its minimum. The result is $[(Z_f + Z_a)/Z_a]\,V_{os}$ due to output amplifier drift. The manufacturer's specification for V_{os} for the Model 3400B is ±50 μV/°C max. This causes a worst case output voltage drift of 1.02 mV/°C or .209 LSB/°C.

The third source of error caused by temperature drift is the two potentiometers used to adjust output voltage offset and gain. Carbon composition

pots having coefficients of -600 ppm/°C were used. The gain pot has a range of ±0.1 volt out of 10 volts which contributes -0.0006%/°C error maximum.

The output voltage offset control is a 500 ohm pot connected to the balance pin of the output amplifier. The amplifier sensitivity is specified as 50 μV/ohm referred to the input which results in 150 μV/°C or 0.0307 LSB/°C error at the output.

Total worst case temperature drift due to all error sources is ±0.572 LSB/°C. Actual temperature drift is much lower than that indicated by worst-case analysis. Results of temperature testing of the MDAC showed a drift of less than 0.25 LSB/°C using operational amplifiers rejected due to temperature drifts of greater than ±100 μV/°C. It is felt that with the use of 0.1% T-2 metal film resistors and amplifiers with voltage drift specifications of ±25 μV/°C, the actual drift would be less than 0.1 LSB/°C.

High-frequency Errors

Unavoidable capacitances in the MDAC T-networks and switch circuits can lead to phase-shift errors at the output with high frequency analog inputs. Most of this error is contributed by the capacitance to ground of the operational amplifier switch networks. The addition of small capacitors, $C1_n$ (see Figure 2) in parallel with input resistor of the six most significant bit T-networks reduced the phase-shift error to less than 0.1% for frequencies up to 20 kHz (Figure 6).

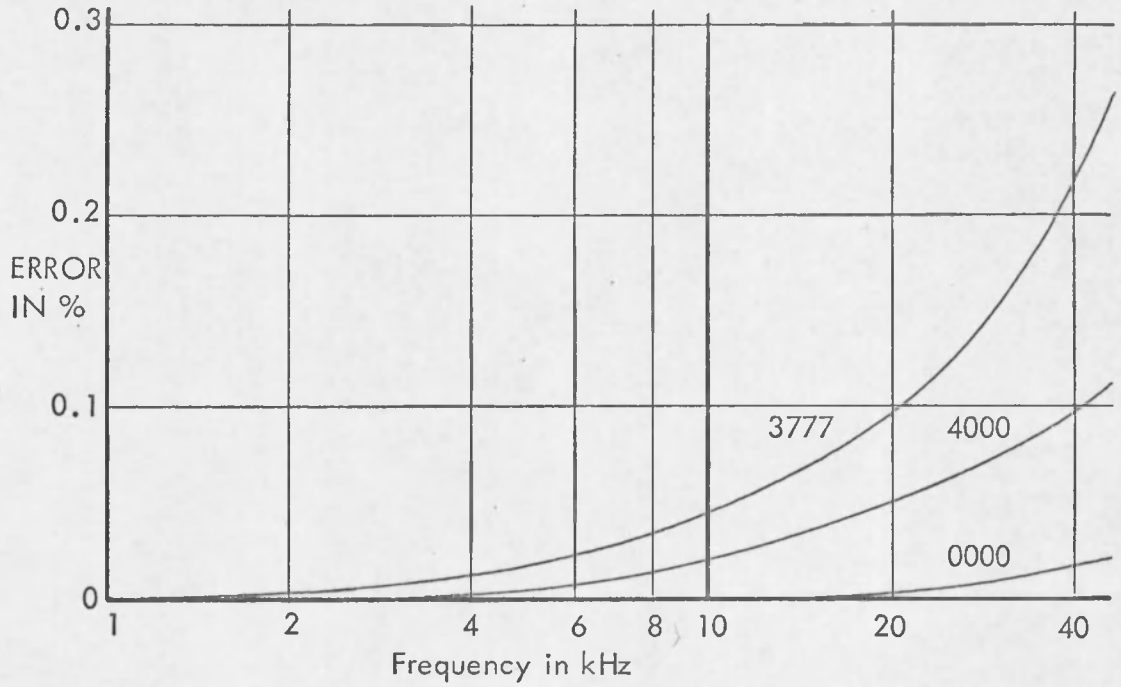


Fig. 6. MDAC Dynamic Error with Frequency Equalization

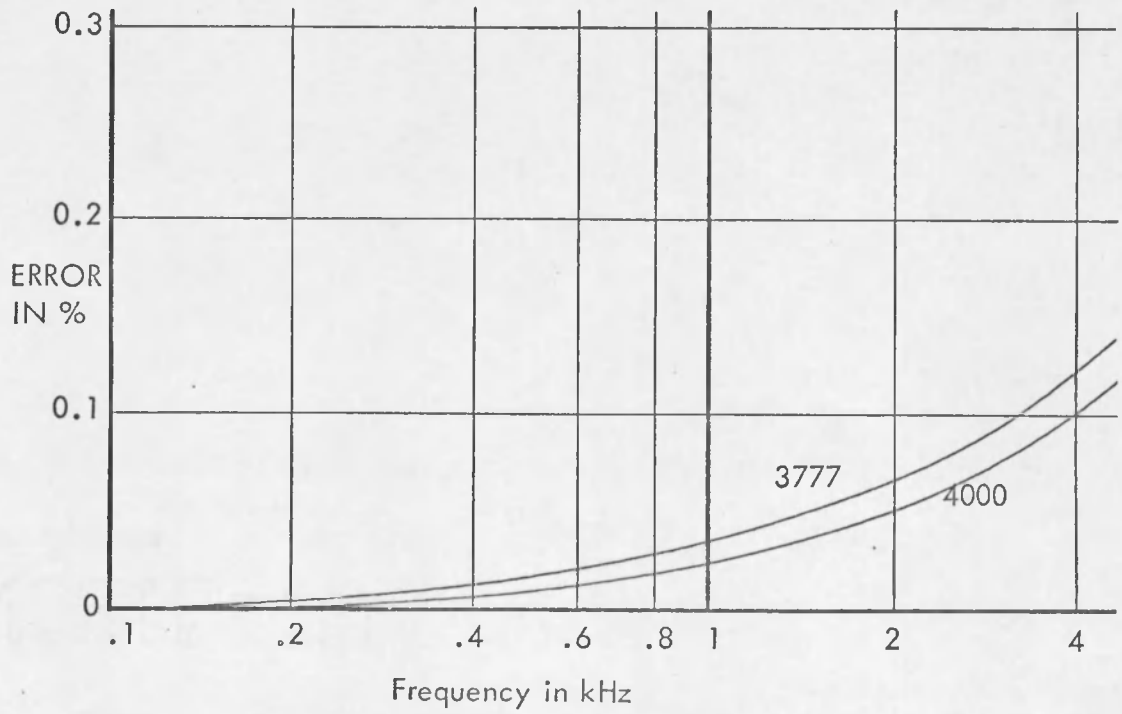


Fig. 7. Dynamic Error without Equalization

The values for $C1_n$ were: C1-0 = 22 pF, C1-1 = 15 pF, C1-2 = 10 pF, C1-3 = C1-4 = C1-5 = 5 pF, and C1-6 through C1-11 were zero. Without these capacitors, the bandwidth for 0.1% operation was 3 kHz (Figure 7). Another simple frequency-response equalization technique was attempted. The output amplifier feedback resistor was split in half and a small capacitor to ground was connected to the center of the feedback resistor. However, it was found that the Model 3400B had approximately the right peaking without this capacitor and its addition increased the error.

Errors Caused by Switching Spikes

The gate-to-drain junction capacitance of the switching transistors injects a small charge into the T-network when the bit is switched. The effect of this charge is dependent on the size of $R3_n$. The worst case switching spike occurs near zero when bit 0 is turned on and bits 1 through 11 are turned off. The short overload recovery time and high frequency response of the operational amplifiers used limits the duration of this spike to less than 300 nanoseconds.

In high speed hybrid computation, MDAC's are most commonly used to change parameters during the RESET period. Spike errors during this period do not affect computation. Switching spike error only needs considering when switching occurs during a computer run. The short duration of these spikes makes them negligible unless numerous switch changes occur during a run and are integrated by succeeding stages.

CONSTRUCTION, TESTING, AND RESULTS

Construction

In order to achieve the highest possible analog input frequency response, state-of-the-art discrete encapsulated amplifiers were chosen over the widely used integrated circuit amplifiers. A considerable savings in size and money could have been achieved using integrated circuits, but only by sacrificing analog-input bandwidth.

The wideband amplifiers chosen allowed the analog input and output to swing ±10 volts on power supplies of ±15 volts. An internal +5.0 volt supply was derived from the +15 volt supply to power the digital drive circuitry. This supply consists of a 5.1 volt zener diode shunt regulator driving a temperature compensated emitter follower. Logic levels of 0.4 volts and 2.4 volts were chosen for the digital inputs as these levels are compatible with currently available integrated circuit logic such as TTL, RTL, and DTL.

Reduction in the amount of calibration required was achieved using the following methods: all bits use 1.0%, low temperature coefficient, metal-film resistors. The individual bits were trimmed using 1% metal film and 5% carbon composition resistors. The input voltage offsets of the operational amplifiers were trimmed to within 50 microvolts of zero at 25°C using 1% metal film and 5% carbon composition resistors. Provisions were made for only two adjustments, output voltage offset and gain. The gain control allows adjustment of the full scale output

between ±9.9 volts and ±10.1 volts. The offset control allows the output offset to be set to zero at any operating temperature.

The repetition of the bit summing and switching networks was used to simplify construction. Twelve small printed circuit boards, each containing a single bit T-network and its switch drive, were stacked on two long rods. A thirteenth board containing two hex inverters and the 5 volt power supply was placed on one end of the stack. A fourteenth board with the output amplifier and the two trimming potentiometers was placed on the other end. A fifteenth board was added to hold an inverter to drive the input of bit 0. With the addition of connectors for inputs, output, and power, the completed assembly measured less than 1-3/4" x 2-3/4" x 10". The result is shown in Figure 8.

Calibration

Calibration was performed in two stages. First, the input offset voltage of the operational amplifiers used in each bit switch was set to within 50 microvolts of zero. This was done, prior to the installation of $R3_n$, using a temporary feedback circuit of one to one thousand. Then the individual T-networks were installed and $R3_n$ was trimmed with parallel resistors to set the n^{th} bit current. In order to insure monotonicity, the calibration proceeded from the least to the most significant bit. Each succeeding bit was set one LSB larger than the sum of all less significant bits.

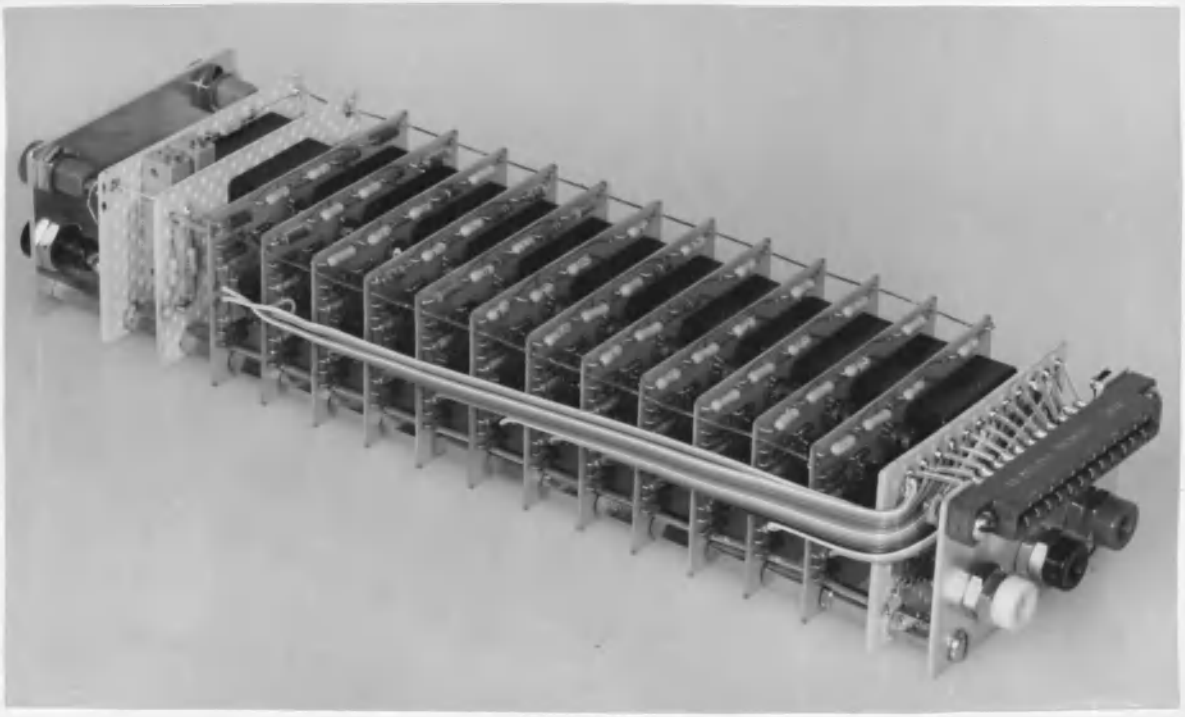


Fig. 8. Fully Assembled MDAC

After the static calibration was completed, the high frequency equalization was performed using the circuit shown in Figure 9. The basic technique was to turn on only the bit to be equalized and adjust the value of Cl_n for minimum error at 30 kHz. For bit 0, the error amplifier was changed to a frequency compensated differential amplifier.

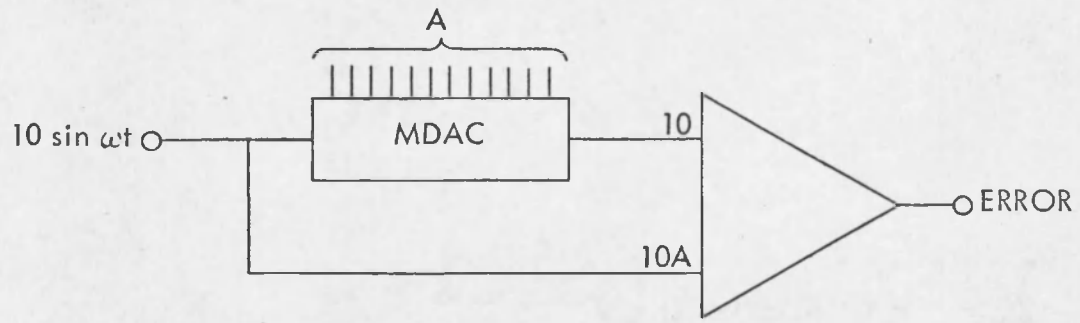
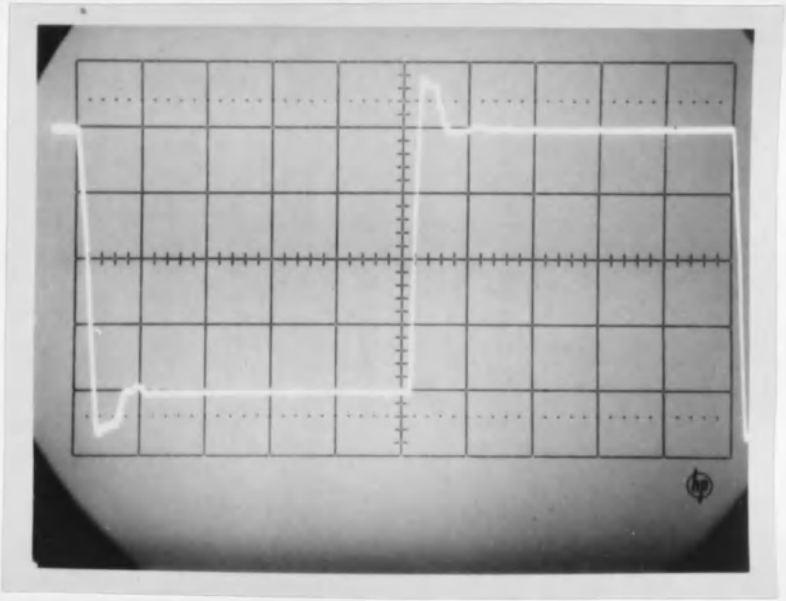


Fig. 9. Circuit for Measuring MDAC Dynamic Error

Digital Switching Characteristics

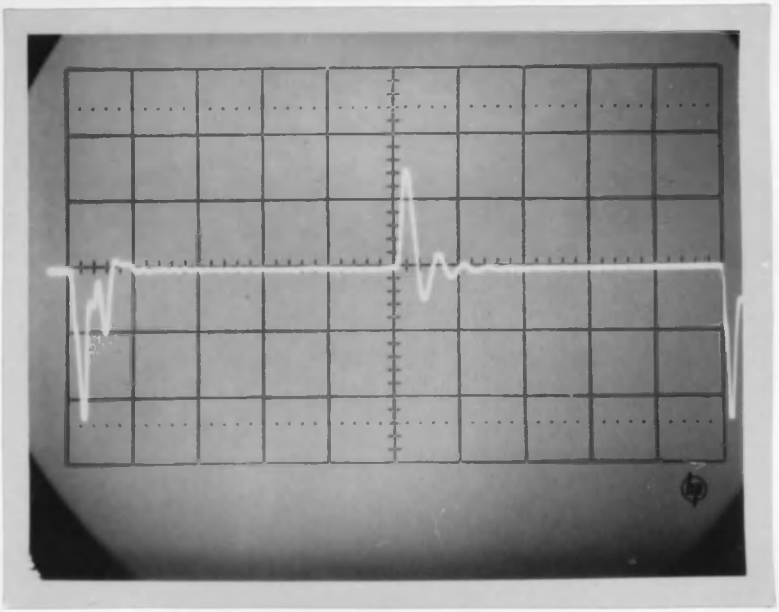
Switching of both FET's in any given bit is accomplished in less than 140 nanoseconds. Settling time (to within 0.025% of half scale) at the MDAC output is less than 5 microseconds with all switches changing state, and worst-case rise and fall times when switched between +10 volts and -10 volts are less than 200 nanoseconds.

Figure 10 shows the MDAC output for a 10 volt d.c. analog input with digital switching between octal 4000 and 3777 as an illustration of worst-case



Vertical Scale: 5 V/cm
Horizontal Scale: 0.5 μs/cm

Fig. 10. Digital Switching Characteristics



Vertical Scale: 2 V/cm
Horizontal Scale: 0.5 μs/cm

Fig. 11. MDAC Switching Spikes

rise and fall time. The switching spikes cause the amplifier to overload; however, overload recovery is extremely short (less than 300 nanoseconds).

Figure 11 shows the switching spikes occurring when all 12 bits change state.

Dynamic Characteristics

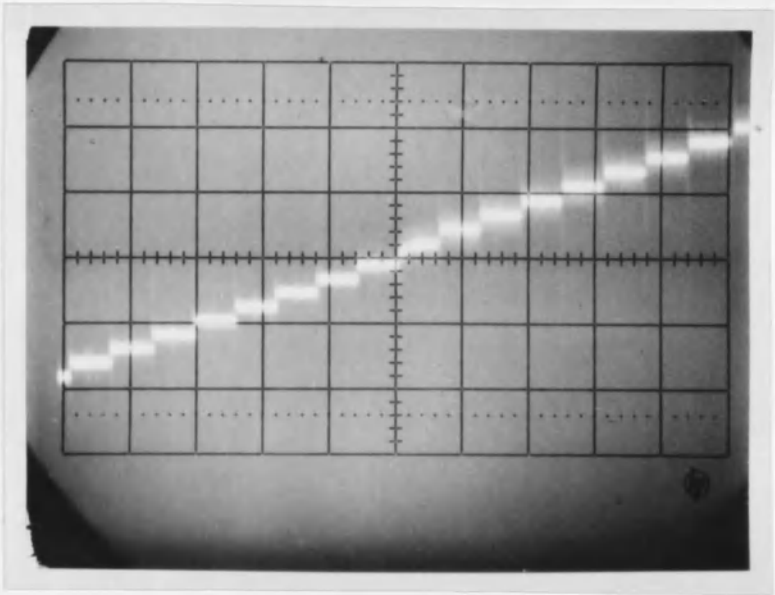
The dynamic characteristics of the MDAC are shown in Figures 12, 13, and 14. Figure 12 shows the MDAC output for a -10 volt d.c. analog input with the digital steps from 007 to 7770, illustrating MDAC monotonicity as the digital input changes sign and all switches change state.

Figure 13 shows the MDAC output for a 10 volt, 10 kHz sine wave at the analog input multiplied by a digital ramp with a clock frequency of 205 kHz. Figure 14 shows the output for a 10 volt, 1 kHz sine wave at the input multiplied by a digital ramp with a clock frequency of 1 MHz.

The analog output response to a fast-rise-time 10 volts square wave applied to the analog input from a low impedance source with the digital input set to 3777 had a rise time of less than 200 nanoseconds, an overshoot of 40%, and a settling time to within 0.025% of 5 microseconds.

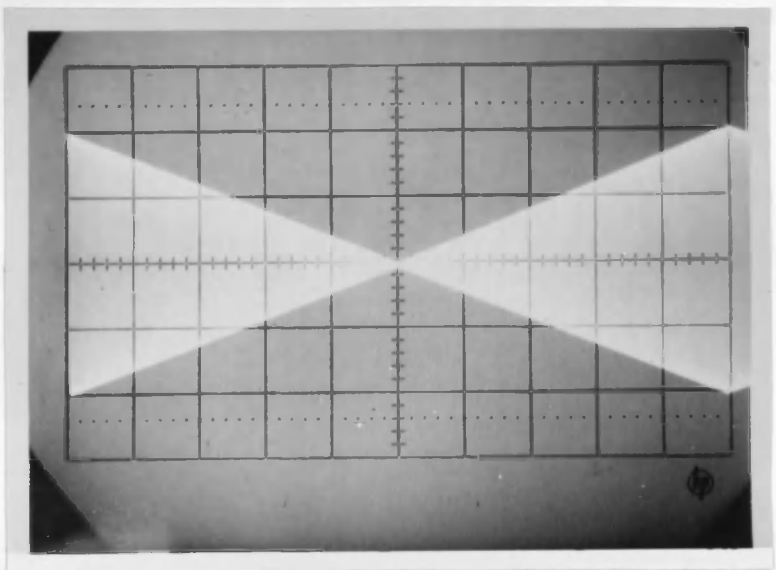
Discussion

The MDAC analog-input bandwidth achieved is believed to be a record for an MDAC of 0.1 per cent half-scale accuracy. In a commercial version, only the five most significant bits would need operational-amplifier switches. The



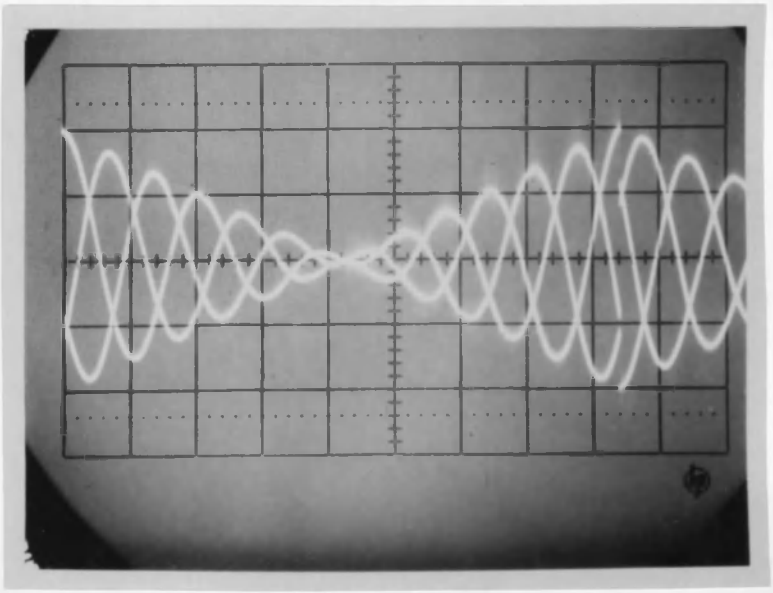
Vertical Scale: 10 mV/cm
Horizontal Scale: 50 μs/cm

Fig. 12. MDAC Resolution Near Digital Zero



Vertical Scale: 10 V/cm
Horizontal Scale: 2 ms/cm

Fig. 13. MDAC Operation at 10 kHz



Vertical Scale: 10 V/cm
Horizontal Scale: 0.5 ms/cm

Fig. 14. MDAC Operation at 1 kHz

remaining seven bits would use series or series-shunt switching (Eddington, 1970). The resulting decrease in summing amplifier feedback ratio would partially offset the loss in bandwidth caused by using hybrid or integrated circuit amplifiers. Presently available integrated circuit amplifiers have unity-gain bandwidths of 20 megaHertz as compared to 100 megaHertz for the Model 3400B. It is felt that a commercial version could be manufactured having a 10 kiloHertz bandwidth for a half-scale accuracy of 0.1 per cent.

REFERENCES

Eddington, D.J.: The Design of a Multiplying Digital-to-Analog Converter For Wideband Hybrid Computation, M.S. Thesis, Department of Electrical Engineering, University of Arizona, 1970.

Korn, G.A.: Bit Switch for a Calibration-free MDAC, CSRL Memo No. 201, Electrical Engineering Department, University of Arizona, February, 1970.

_____, and T.M. Korn: Electronic Analog and Hybrid Computers, 2nd Edition, McGraw-Hill, New York, 1972.