A DATA ACQUISITION INTERFACE UNIT

by

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Larry C. Schooley — August 5, 1974

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PREFACE

Research leading to this thesis was sponsored by the United States Army Strategic Communications Command under Contracts DAEA18-73-C-0026 and DAEA18-73-C-0310 covering the period from July 1972 to July 1974. This research involved the design, fabrication, and testing of several pieces of digital equipment to be used in the testing and evaluation of digital communications systems employed by the Safeguard Communications Agency.

The author would like to thank Dr. L. C. Schooley for his help and suggestions during the preparation of this thesis. Mr. John Goodman and Mr. William Heidergott assisted in much of the fabrication and testing of the units herein described and their efforts are greatly appreciated. Mr. Robert Semelsberger also assisted in this effort and I would like to thank him for his help.

I would like to express my special thanks to Dr. Claude A. Wiatroski and Mr. Thomas W. McCurnin for exposing me to various design techniques and "tricks" during the course of this project and without whose continual encouragement this thesis would not have been written.

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ABSTRACT

The design of special purpose equipment to be used in a data acquisition system is investigated and analyzed. To accomplish this both input signal requirements and output data formats are considered. Special consideration is given to the choice of display system to be used and a detailed functional description of the overall design is made. Methods of fabrication are outlined showing the improvements made during the design and construction stages.

CHAPTER I

INTRODUCTION

The Data Acquisition Interface Unit (DAIU) was designed to provide an electrical interface between data and timing sources and various recording equipment in a digital data acquisition system. The data acquisition system provides capabilities for monitoring and recording various disturbances on several digital communications channels.

The DAIU features two distinct operating modes designated as "two channel" and "three channel" operation. In two channel operation, two independent digital channels are monitored for bit errors while selected special events relating to the two channels may also be monitored. The three channel operating mode allows for the monitoring of errors on a third channel in place of the special events. Channels with data rates up to 50 kilobits per second may be monitored.

The Data Acquisition Interface Unit itself is a special purpose computer which contains an internal clock, error counters, temporary storage registers, data formatters, and the control circuitry required to execute its hardwired program. The DAIU provides the following functions/capabilities:

- Digital clock displayed with one second resolution
- Events detector
- Internal circuitry test

- Error detector, counter, and display capable of counting and displaying up to 5000 errors every tenth second
- Input/output buffers
- Output format processor
- External device status monitors
- Absolute delay measurement test (looped circuit)

In operation, digital data consisting of bit errors and/or the occurrence of special events are collected in tenth second sample intervals and presented to the external recording equipment along with the outputs of the digital clock. Thus, the recorded output contains a complete history of channel activity providing a record of channel errors and special events and the time interval during which they occurred.

Three recording media are employed in the DAIU. In the initial design, a Hewlitt-Packard Digital Printer (Model 5050B) was used for a quick check reference of channel performance while an HP Paper Tape Punch (Model 2753A) provided a data recording and storage medium suitable for later computer reduction. However, due to the output and mechanical limitations of these two devices, a third recording unit was later added to the DAIU. This unit, the DAIU - Digital Recorder Unit, provides for the recording of the collected data on a magnetic tape cassette (see Chapter IV). The unit may be operated with any combination of these recording devices in use.

The Data Acquisition Interface Unit is mounted in a standard equipment rack along with various pieces of Government furnished

equipment as shown in Figure 1. All of the recording equipment mounts in the rack with the DAIU due to the length constraints of their interconnecting cables. The HP printer and punch are shown in Figure 1, however, the DAIU - Digital Recorder Unit is not shown (see Chapter IV for illustration).

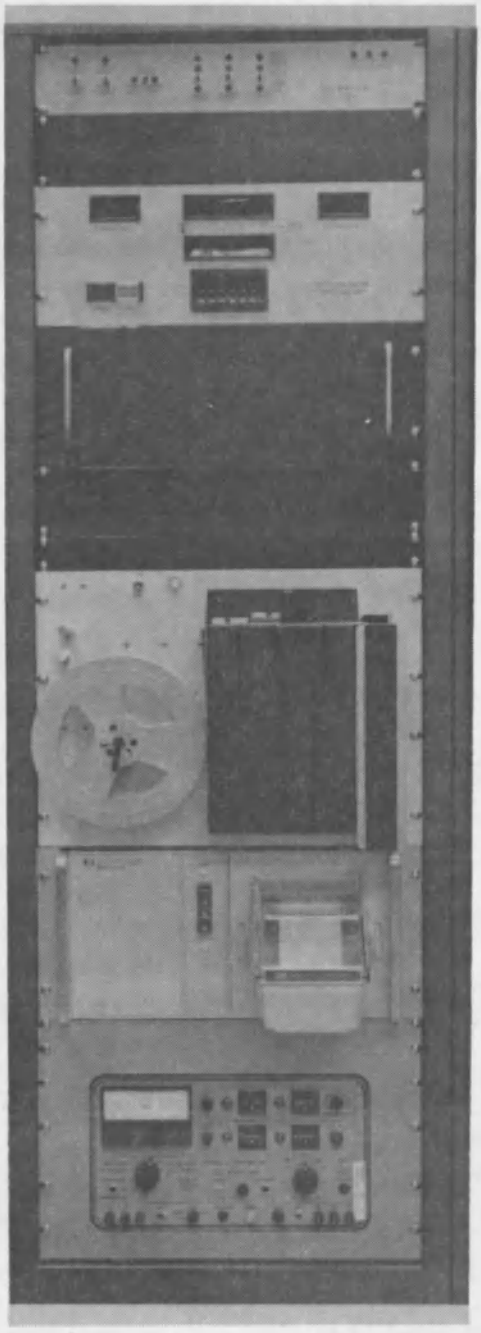

Figure 1. Rack Mounted
Data Acquisition Interface Unit

CHAPTER II

OPERATIONAL DESCRIPTION

The Data Acquisition Interface Unit was designed to operate with several external pieces of input/output equipment under the control of a hardwired program. This chapter includes a description of the manner in which this interaction is accomplished.

DAIU Test Configurations

The primary use of the Data Acquisition Interface Unit is for testing digital communications channels. Figure 2 shows a block diagram illustrating a typical test configuration utilizing the DAIU in the two channel operating mode. The data sets (modems) shown are the Bell System 303 wideband (19.2 kilobits/second) and 203 narrowband (4.8 KB/s) data sets, however, any appropriate data set (one operating at less than 50 KB/s) may be used. The data from these modems is multiplexed along with a 1 KHz tone on an adjacent voice channel and transmitted over a communications link. At the receiving end of the link, this multiplexed data is input to another set of modems. The outputs of these modems provide the inputs to the Data Acquisition Interface Unit.

For each data set, RECEIVED DATA, RECOVERED CLOCK, and MODEM DROPOUT signals are fed into the DAIU. In addition, an Hekiemian Phase Jitter Meter (Model 48) and impulse noise counter provide the

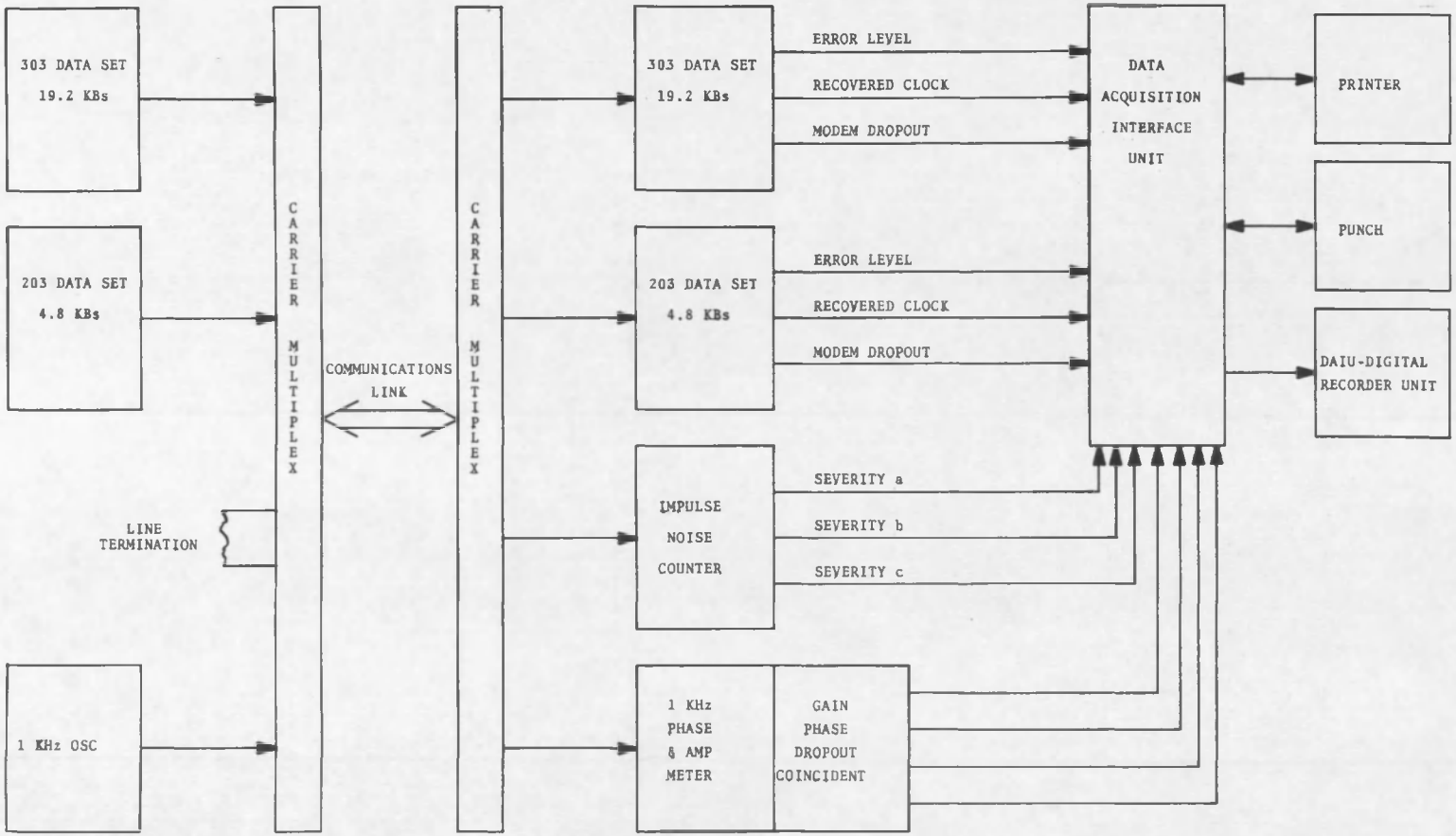

Figure 2. DAIU in Two Channel Operating Configuration

remaining special events related to the adjacent voice channels. These events are listed below and are completely defined in the input data section:

- 1 KHz Phase Hit
- 1 KHz Gain Hit
- 1 KHz Coincidence Hit
- 1 KHz Dropout
- Impulse Noise Levels of severity 1, 2, and 3

These inputs are monitored by the DAIU and formatted in slightly different forms for presentation to the external recording devices.

Figure 3 shows a similar test configuration for three channel operation. In this configuration, three data sets are employed, each operating at any data rate up to 50 KB/s (see Appendix A for printer output limitations on channel three). Although the special events inputs may remain connected to the DAIU, they will be ignored in the three channel operating mode.

Input Data

The Data Acquisition Interface Unit basically counts bit errors present at the receiving end of a digital communications channel. Digital data is transmitted in serial form and appears at the data set output (RECEIVED DATA) as one of two allowable signal levels (logical "1" and "0"). This stream of "1" and "0" levels is synchronized with the RECOVERED CLOCK output of the data set. Each clock period represents one data bit with the data held constant during this period.

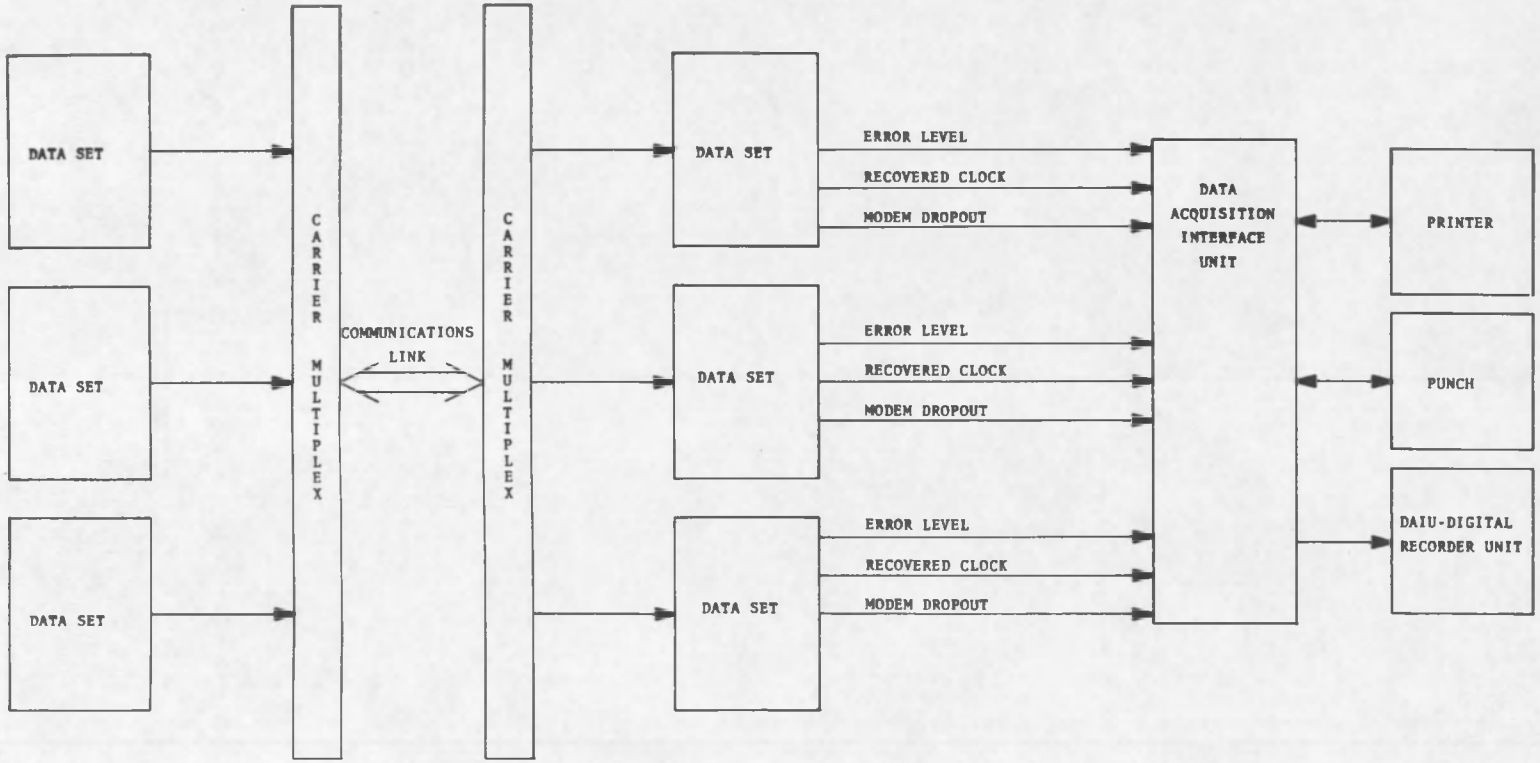

Figure 3. DAIU in Three Channel Operating Configuration

The transmitted data is received and decoded to form an all zero input stream to the DAIU (assuming no errors are present). If an error has been introduced by the channel, the decoded output will not be all zero but will have a "1" bit for each error introduced. The DAIU then counts the number of these errors occurring in each tenth second sampling interval and presents the total in the proper format for recording.

The special events monitored in the two channel operating mode are events related to adjacent voice channels associated with the digital channels. A 1 KHz tone is transmitted over one of these channels while another channel is terminated (no input signal). These channels are monitored at the receiving end by several pieces of equipment which provide the special events inputs to the DAIU. These events are defined as follows:

- 1 KHz Dropout (1KD): A -18 dB drop in the nominal signal level for a period of at least four milli-seconds
- 1 KHz Gain Hit (1KGH): A $\pm$1 dB amplitude variation in the nominal signal level for a period of at least four milli-seconds
- 1 KHz Phase Hit (1KPH): A $\pm$5 degree variation in the nominal recovered phase angle for a period of at least four milli-seconds
- 1 KHz Coincidence Hit (1KCH): A simultaneous occurrence of a gain and phase hit.
- Impulse Noise Levels low, medium, high (INL1, INL2, INL3):

A noise spike which exceeds the voice weighted levels of 66, 70, and 76 dBrn respectively

In addition, each data set provides a special event defined as the MODEM DROPOUT (M1D and M2D) indicating that the received signal level does not meet data set input requirements. Data received while a data set indicates a modem dropout will be invalid.

DAIU Program

The hardwired program of the Data Acquisition Interface Unit is shown in the flow chart of Figure 4. Basically the DAIU waits in an initial state with all counters and temporary storage registers enabled. Any errors are accumulated in the error counters while occurrences of special events are stored in temporary storage registers. When a tenth second pulse arrives, the contents of each error counter and temporary store are transferred to the tenth second data buffers. If a one second pulse is present, this data is also transferred to the one minute display data buffers. When all data has been transferred, the error counters and temporary stores are cleared and enabled for the next tenth second data interval.

If no data is present at this time (no errors or special events) program control exits and returns to its initial waiting state. However, if any data has been collected, both the printer and punch are interrogated to determine if they are busy. If either is busy, the appropriate alarm will be activated and the corresponding print or punch command will not be issued. If either device is not busy, the information in the tenth second registers will be recorded. In either

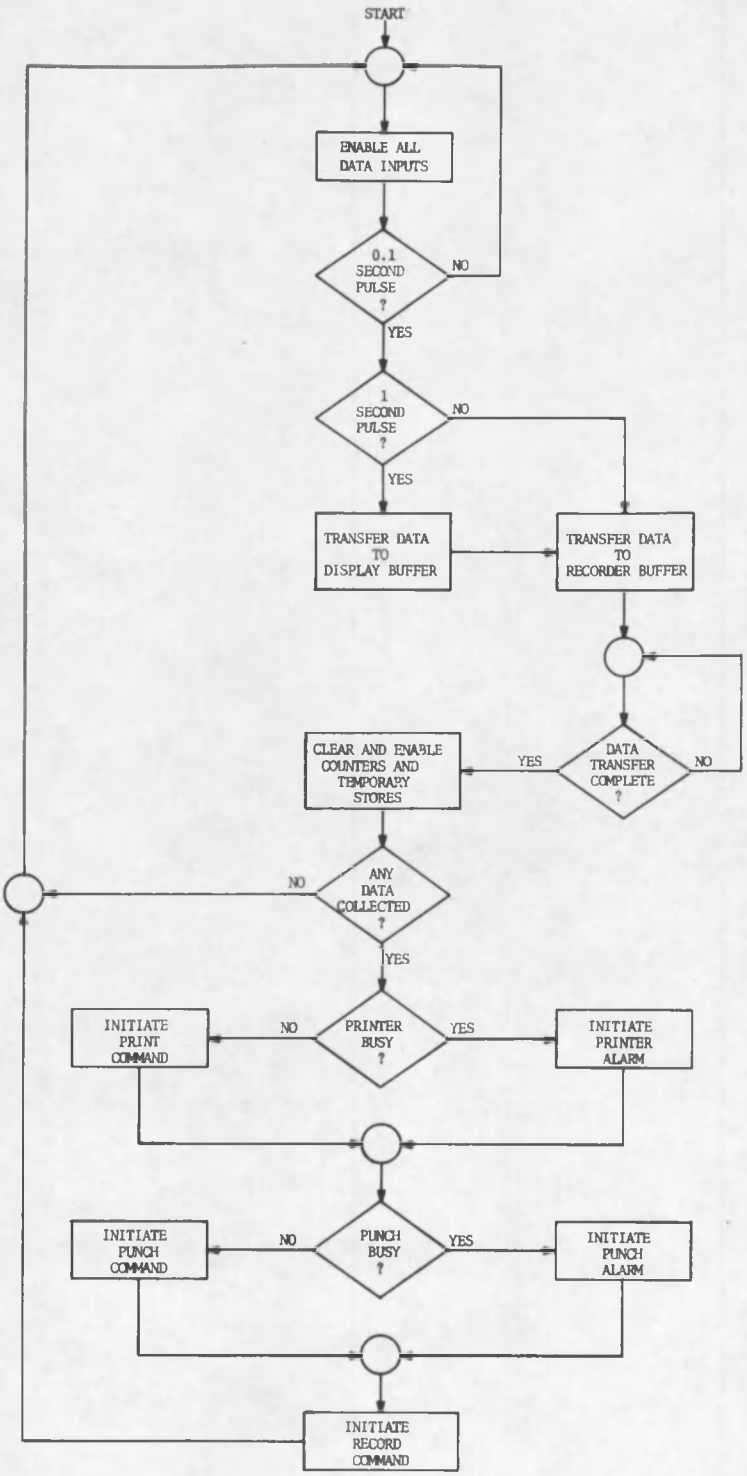

Figure 4. Flowchart of DAIU Hardwired Program

case, the DAIU - Digital Recorder Unit will be activated. When all recording commands have been issued, the program control again returns to the initial waiting state.

The front panel display operates continuously, displaying the contents of the display buffers. These buffers are updated every second. The tenth and one second transfer pulses occur relatively fast in relation to the MODEM CLOCK frequency ensuring that no errors are missed during the transfer operation.

In addition to the above program, two operator initiated tests are available. These are an absolute DELAY TEST (looped circuit) and an ERROR TEST. The DELAY TEST causes a pulse to be sent to the data set coincident with and having the width of one MODEM CLOCK pulse. The pulse is transmitted following a one second pulse. This test is normally initiated with the data set SEND DATA lead connected to the RECEIVED DATA lead. The absolute delay through the modem can then be determined by measuring the time interval between the transmitted and received pulse.

The ERROR TEST function provides a check on the internal error counting circuitry of the DAIU. This function continuously enables the error counters, overriding the MODEM DATA input and causes the counters to count the MODEM CLOCK frequency.

Front Panel Operation

Figure 5 shows the two front panels of the Data Acquisition Interface Unit. The upper panel is the DAIU Monitor and Test Panel which provides for monitoring of external device status and initiating

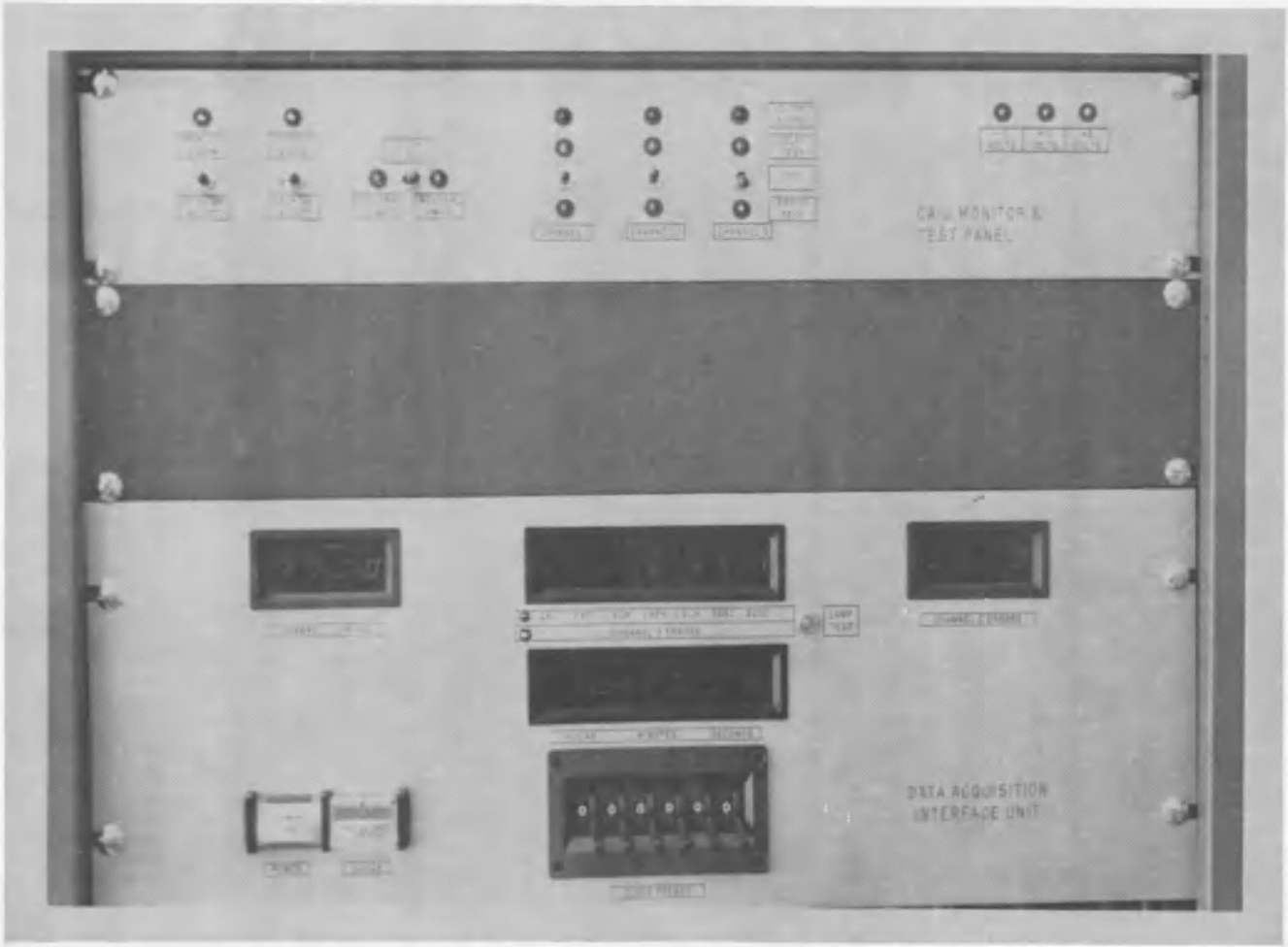

Figure 5. Front Panels of the Data Acquisition Interface Unit

of internal and external tests. The lower panel is the Main Display/ Control Panel of the Data Acquisition Interface Unit.

The main DAIU Display/Control panel provides the following functions:

- AC power ON/OFF switch
- Digital clock display, preset switches, and SET/RUN control
- Channel 1 and 2 error displays
- Channel 3 errors/special events display
- DAIU operating mode indicator lamps
- Lamp test switch (for seven segment displays only)

The channel 1 and channel 2 errors are displayed on the left and right sides of the main DAIU panel respectively. The center display serves as the channel 3 errors/special events display depending upon the operating mode of the DAIU. For two channel operation, this display will be blank except when a special event has been detected. An "H" will appear above the detected event in this case except for the INL (impulse noise level) position which will indicate a severity of 1, 2, or 3. For three channel operation, this display will indicate 0000 when no errors are detected on channel three.

Two solid state lamps indicate which operating mode the DAIU is in. For two channel operation, a red lamp is lit next to the special events legend. Similarly, for three channel operation, a green lamp is lit next to the channel 3 errors legend. In addition, a LAMP TEST switch is provided which, when depressed, causes all segments of each seven segment display to light.

If the internal clock fails, or if an external clock is selected but not provided, all seven segment displays will be blanked. This precaution is taken to ensure that no display will be destroyed by failure of the time division multiplexing scheme used in the DAIU (see Chapter III for complete details).

The DAIU Monitor and Test Panel provides the following functions:

- Printer and punch alarms and reset switches
- Channel 1, 2, and 3 clock alarms
- Internal/external clock select switch and indicator
- Channel 1, 2, and 3 DELAY and ERROR TEST switches
- DC voltage indicator lamps

When AC power is applied to the DAIU, the three voltage indicator lamps should light, indicating the presence of DC power. With no modems connected to the DAIU, the three clock alarm lamps should flash at a 1 Hz rate. The printer and punch alarm lamps similarly flash whenever the respective device is busy or off and data is present to be recorded. Either alarm lamp may be reset by depressing the appropriate reset switch. The clock source switch should normally be in the internal 1.0 MHz position and the indicator should correctly indicate this.

The six test functions and indicator lamps should normally be off. Whenever any channel error or delay test is performed, the corresponding indicator lamp will flash at a 1 Hz rate. All alarm lamps are red while other non-alarm indicators are either yellow or green.

Internal and External Connections

Several interconnections must be made between the DAIU and its various input/output devices. Parallel data inputs are required by both the HP printer and the DAIU - Digital Recorder Unit. The HP punch requires seven parallel data bits for each frame punched.

To satisfy these data requirements, two fifty pin blue ribbon connectors are provided for interconnection to the HP printer. Both a fifty pin and a twenty-five pin "D" type connector are supplied to interconnect the DAIU - Digital Recorder Unit. The connections to the HP punch are made through a barrier strip attached to the top of the DAIU card rack. The special events inputs connect to the DAIU at a barrier strip also mounted on the top of the card rack. Each channel of the DAIU has one twenty-five pin "D" type connector supplied for the modem inputs.

In addition to the above input/output connections, two fifty pin "D" type connectors are provided to connect the DAIU card rack to the two front panels. Figure 6 shows the DAIU main connector block assembly which contains these connectors (C and D) as well as those for the modem inputs and the HP printer (A and B). The BNC connector is provided for the external 10.0 MHz clock input. Complete details of these interconnections may be found in references [1] and [2].

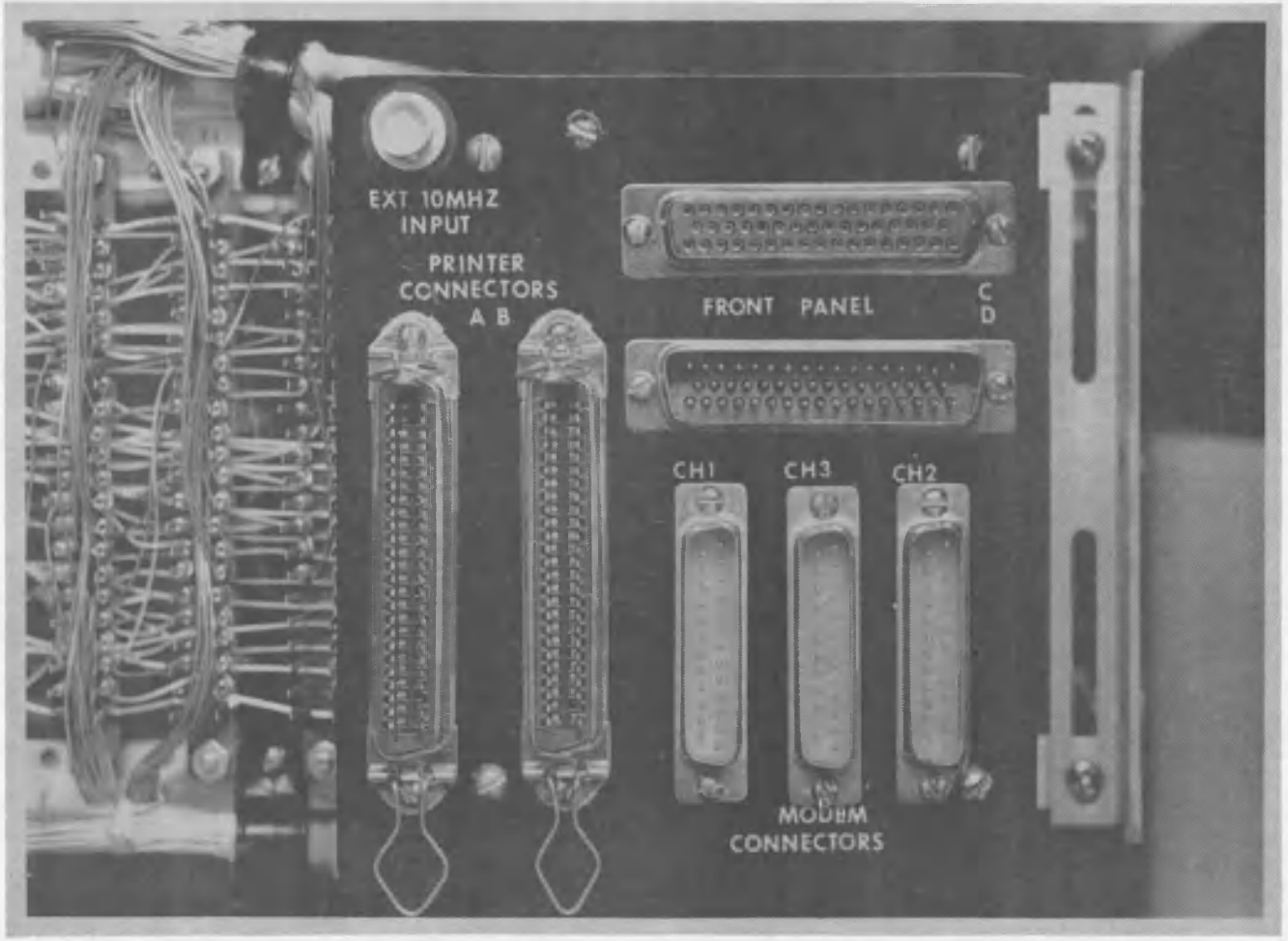

Figure 6. DAIU Main Connector Block Assembly

CHAPTER III

DETAILED DESIGN AND FUNCTIONAL DESCRIPTIONS

The design of the Data Acquisition Interface Unit involved several choices as to the exact methods to be used to accomplish the desired results. The unit itself was contractually required to be fabricated from a series of circuit boards housed in a card rack. Each board could then be replaced,if necessary,to maintain the operability of the entire system. The circuits constructed on each of these cards were designed to perform a single logical function (e.g., count errors, generate clock pulses, decode the display, etc.).

The overall unit was constructed of standard 7400 series Transistor-Transistor Logic (TTL) as this logic family provided the largest selection of logical functions and was readily available.

Modes of Operation

The Data Acquisition Interface Unit may be operated in either the two or three channel mode. The actual "mechanics" involved in switching the DAIU between these two modes comprised a considerable portion of the DAIU design. Several options were available to choose from among which were the use of a front panel switch, a T-Bar switch, and circuit card manipulation.

The switch options were quickly eliminated for reasons of fabrication difficulty and the overall component count required. The front panel switch, which provides a data selector control level, would

require at least one gate or data selector input for each function to be switched. Since two circuit boards are used for the special events and the third channel, this would result in as many as eighty functions to be switched. The T-Bar switch, although designed for this type of switching was rejected because of the number of interconnections required between it and the card rack. In addition, each of these methods would have required that both the special events circuits and the third channel circuits be provided with their own card slots. Under these conditions, all of the DAIU circuit cards would be drawing power from the DAIU power supply but in each operating mode two circuit cards would not be used.

This exploration into the various methods of changing the operating mode of the DAIU resulted in the choice of circuit card manipulation. The DAIU card rack was constructed so that the functions provided on cards occupying slots five and six would control the overall operating mode of the DAIU. Thus, when a modem interface card and an error counter card occupy these slots, three channel operation is selected. Similarly, when the special events interface and the special events display and store occupy these slots, two channel operation is selected. In both cases only twelve circuit cards are drawing power from the power supply at any time. Details of this mode selection function are provided in the circuit board functional descriptions.

Display System

The choice of a display system to be used in the Data Acquisition Interface Unit was made after a consideration of the desired reliability

and ease of fabrication. The choice was made between a continuous display for each digit and a time division multiplexing scheme involving all digits.

In the continuous display system, the binary coded decimal (BCD) data is transferred to a storage latch which holds the outputs constant during the display interval (one second in the DAIU). This BCD data is then decoded into the proper display code for the seven segment front panel displays. Each displayed digit then requires a latch, decoder, and seven current limiting resistors to control the brightness of the display. In addition, each display requires seven interconnections between the DAIU card rack where the data is received and the front panel display. For the twenty-one digits displayed on the DAIU front panel, this results in 148 interconnections.

In the time division multiplexing scheme, the BCD data is strobed onto a data "bus" consisting of four BCD data lines. BCD data from all displayed digits is transferred onto the same four lines but at different times. The control or enable signals are generated in such a manner that only one digit's information is on the bus at any given time. The data bus is then connected to a BCD-seven segment decoder whose outputs each have a single current limiting resistor. The same enabling signals that are used to gate the data onto the data bus are used to enable the appropriate display on the front panel. Thus when a digit's BCD code is gated to the bus, the same enabling signal enables the digit on the front panel and the correct information is

displayed. A twenty-one digit multiplexed display system then requires twenty-one latches and bus logic (four open collector gates for each latch), one BCD-seven segment decoder, and seven current limiting resistors plus the circuitry to generate the enable signals. The resulting system, however, requires only 28 interconnections between the DAIU card rack and front panel (seven interconnections for the display segments and one enable signal for each display).

Several possible difficulties may be encountered with a multiplexed display system. Since only one digit is enabled at any one time, the frequency at which these enable signals occur must be high enough to eliminate flickering in the display. To maintain the same brightness level in the displays as obtained with the continuous display, a much higher current is required. With twenty-one digits displayed, each digit is enabled at most for only one interval in each twenty-one. To maintain the same average current then, the multiplexed current must be twenty-one times as great as for the continuously enabled display system. In addition, a failure in the enable signal generation circuitry could result in a single digit being enabled continuously at this high current. Since this current is nearly twenty times the maximum rating of the display, the device would be destroyed in a very short time.

The DAIU display system was multiplexed with knowledge of these features primarily because of the number of interconnections and components required. Each additional interconnection made in the unit was one more that could break or be improperly connected. Furthermore, to

keep the count of circuit boards used to a minimum, the overall component count also had to be low.

The DAIU multiplexed display contains three independent busses: the clock display bus (CKDISP), channel 1 and 2 error counts (ERDISP), and the special channel display (SPDISP). The displays are multiplexed at a 10 KHz rate on a 10% duty cycle and show no visible flicker. A "fail safe" circuit is included to disable all displays if the multiplexing frequency fails. Full details of the display system are given in this chapter under the functional description of the display circuitry (boards DE-7 and DD-9).

Functional Description

The Data Acquisition Interface Unit consists essentially of a card rack housing fourteen circuit cards and the two front panels which contain all displays and control functions. The DAIU card rack provides for interconnections between twelve of the fourteen circuit cards. Two card slots are used for storage of either the channel 3 modem interface and error counter boards or the special events interface and display boards.

The card slots are numbered consecutively from right to left. Slots one and three contain modem interface cards while slots two and four contain their associated error counters. Card slots five and six serve dual purposes as well as well as controlling the DAIU operating mode as explained above. The multiplexed display circuitry is contained on cards occupying slots seven and nine. Card slot eight holds the function control circuitry. This circuitry controls the print, punch,

and record operations and formats the data presented to the printer. The digital clock and basic frequency generation circuitry are located on cards connected in slots ten and eleven. Card slot twelve houses the punch control logic card. All of the data to be punched enters this card and is correctly formatted before it is presented to the punch. Complete functional descriptions of these circuit boards are presented below.

Clock Circuitry

Board C1-10 CLOCK/OSCILLATOR. The basic clock frequencies used in the DAIU are generated on this board and on board C2-11 CLOCK DIVIDER. A schematic of board C1-10 is shown in Figure 7 with the parts list given as Table 1. This board contains a 1.0 MHz low power crystal oscillator [3] from which all required freguencies are derived. The 1.0 MHz output leaves the board on pin F and is gated with the front panel CLOCK SOURCE switch function (see board DE-9) which selects either the internal or external clock. In either case, a 1.0 MHz signal returns to this board on pin 13 as CLOCK.

This signal is applied to the clock input (pin 11) of D flip flop Z6 whose $\overline{Q}$ output is connected to the D input forming a T flip flop. This results in a frequency division by two at output pin 9. Synchronous counter Z10, D flip flop Z9, and gate Z14 provide for division by twenty-five of the 500 KHz output frequency of Z6 pin 9. A timing diagram illustrating this process is shown in Figure 8. The resulting frequency is again divided by two by D flip flop Z6 output 5. The above circuitry then divides the 1.0 MHz input down to a 10 KHz

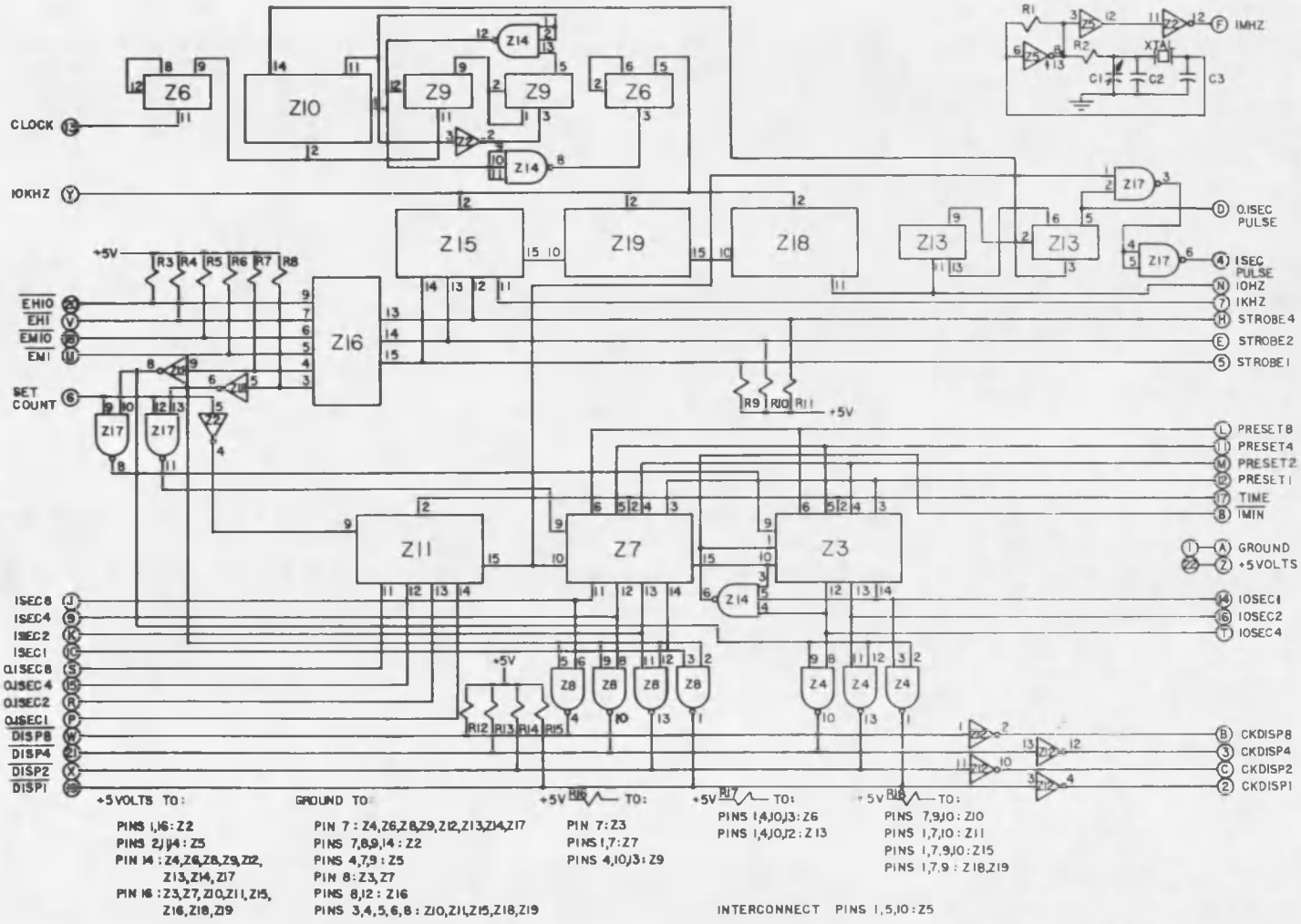

Figure 7. Board C1-10 Clock/Oscillator

Table 1. Board C1-10 Parts List

Z2	Hex inverter/buffer	(RCA) CD4009AE
Z3	Fully synchronous decade counter	SN74162N
Z4	Quad 2 input NAND gate with open collector	SN7401N
Z5	Complementary pair plus inverter	(RCA) CD4007AE
Z6	Dual D flip flop	SN7474N
Z7	Fully synchronous decade counter	SN74162N
Z8	Quad 2 input NAND gate with open collector	SN7401N
Z9	Dual D flip flop	SN7474N
Z10	Fully synchronous 4 bit binary counter	SN74163N
Z11	Fully synchronous decade counter	SN74162N
Z12	Hex inverter	SN7404N
Z13	Dual D flip flop	SN7474N
Z14	Triple 3 input NAND gate	SN7410N
Z15	Fully synchronous decade counter	SN74162N
Z16	BCD-Decimal decoder	SN74145N
Z17	Quad 2 input NAND gate	SN7400N
Z18	Fully synchronous decade counter	SN74162N
Z19	Fully synchronous decade counter	SN74162N
XTAL	AT cut crystal resonant at 1000 KHz with approximately 30 pF loading	
C1	8-50 pF capacitor, trimmer	
C2	100 pF capacitor, dipped mica	
C3	33 pF capacitor, dipped mica	
R1	22 M 1/4 watt resistor, 5%	
R2	10 K 1/8 watt resistor, 5%	
R3-R11	5.1 K 1/8 watt resistors, 5%	
R12-R18	1.0 K 1/8 watt resistors, 5%	

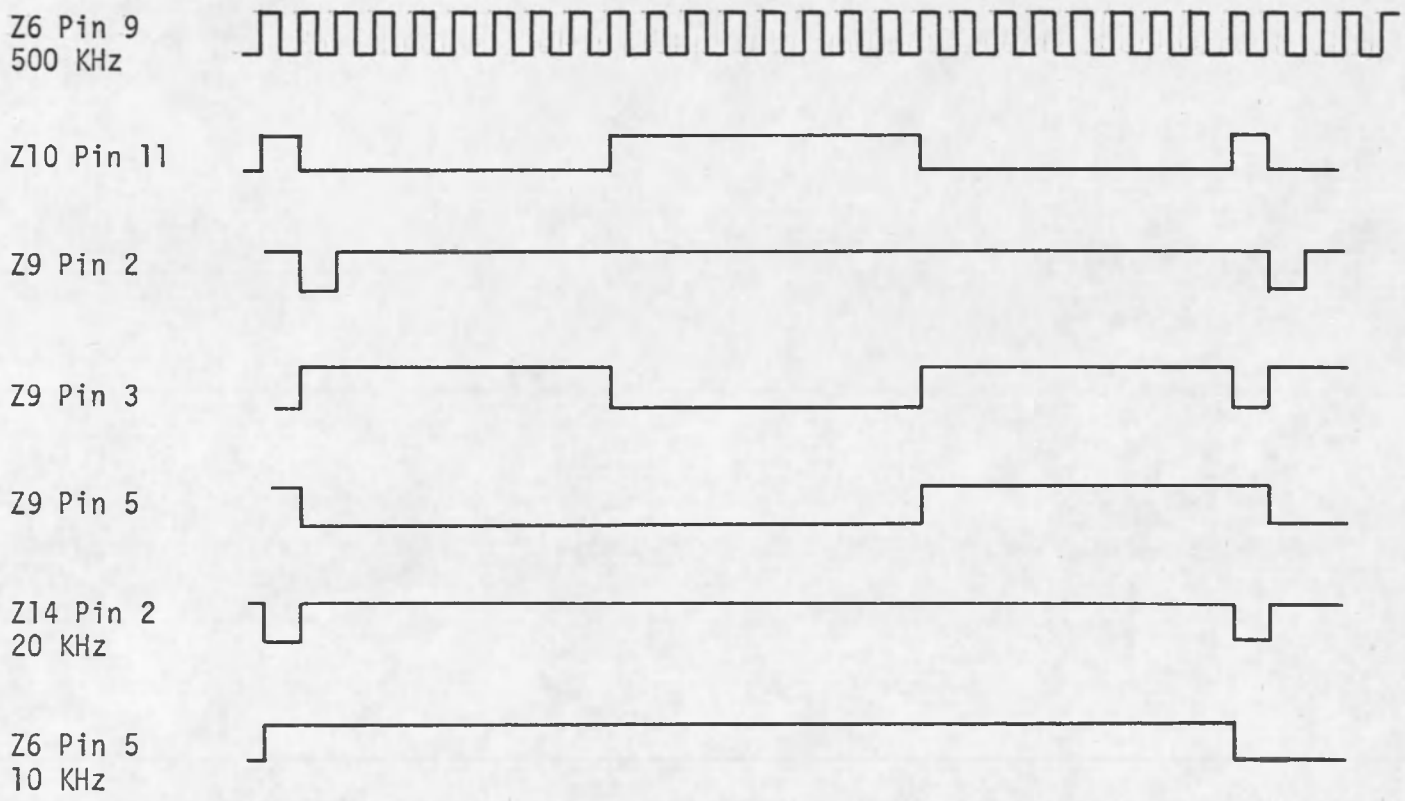

Figure 8. Timing Diagram Showing the Generation of the 10 KHz Clock Frequency

frequency with a 50% duty cycle. This frequency is used as the basic display multiplexing frequency and is further divided to provide the 10 Hz frequency which initiates program operation.

Counter chain Z15, Z19, and Z18 divides the 10 KHz frequency by 1000 at output pin 11 of Z18 providing the 10 Hz signal. The outputs of Z15 (pins 14, 13, and 12) are the multiplexing strobe frequencies and are decoded into enable signals by BCD-decimal decoder Z16. In addition, Z15 pin 11 provides a 1000 Hz signal which, although not used in any other portion of the DAIU, is a useful signal to synchronize external test equipment.

D flip flop Z13 provides the 0.1 and 1.0 second pulses which are four micro-seconds wide and synchronized with the 250 KHz output of Z10 pin 14. When Z18 pin 11 goes high (10 Hz pulse) pin 9 of Z13 is is clocked high enabling Z13 pin 2. When the next leading edge of the 250 KHz signal occurs. Z13 pin 5 is clocked high and pin 6 is clocked low forcing Z13 pin 9 low. The next leading edge of the 250 KHz signal clocks Z13 pin 5 low where it remains until the next 10 Hz pulse. The resulting output at Z13 pin 5 is a pulse occurring every 0.1 second and lasting (high) for four micro-seconds. Gates Z17 pins 3 and 6 AND this signal with one occurring every second resulting in a four micro-second wide pulse occurring every second.

The remainder of the circuitry on this board makes up the tenth, one, and ten second digits of the digital clock. All BCD outputs of the digital clock are made available to the printer and punch control logic. In addition, all digits except the tenth second digit are made available

in a multiplexed form to the clock display bus ($\overline{DISP1}$,$\overline{DISP2}$,$\overline{DISP4}$,$\overline{DISP8}$). Decade counters Z3, Z7, and Z11 provide the ten second, one second, and tenth second digits respectively. All counters are clocked by a signal named TIME which is either a 10 KHz or 10 Hz signal. The 10 KHz frequency is used only to preset the counters while the 10 Hz signal provides a real time incrementing of the clock.

Each digit of the clock is set individually to the multiplexed inputs appearing on the preset bus (PRESET8, 4, 2, 1). When pin 9 of the counter is low, information present at the preset inputs (pins 3, 4, 5, and 6) will be loaded into the counter on the next leading edge of the clock pulse. As the tenth second digit is not displayed, it is always preset to zero.

Z11 pin 15 is the carry output of the tenth second counter. This output is high for approximately one hundred milli-seconds each second and is used to generate the four micro-second wide one second pulse as explained above. The one second digit's BCD outputs (pins 14, 13, 12, and 11 of Z17) are gated onto the display bus by open collector gates Z8. Complete details of the open collector gating may be found in Section 6 of [4]. The ten second digit's BCD outputs (Z3) are similarly gated onto the display buss by gates Z4. Since the ten second digit only requires decimal digits 0 through 5, the $\overline{DISP8}$ line of the bus will always be high for this digit and hence only three gates are required. Gate Z14 pin 6 decodes a count of five so that when 59 seconds have been counted, the next count will reset the ten second digit (Z3) to zero and enable the one minute counter (on board C2-11). Details as to

shortening the counting sequences of these counters may be found in Section 9 of [4].

Board C2-11 CLOCK DIVIDER. This board contains the circuitry required to generate the minutes and hours digits of the twenty-four hour digital clock. Figure 9 shows a schematic of this board while the parts list is presented as Table 2. Devices Z7, Z11, Z15, and Z19 and their associated gating Z6 and Z14 comprise the remainder of this digital clock. The counter devices are fully sycchronous decade counters whose outputs change with the leading (rising) edge of the clock input. In normal counting operation, the counters are clocked by the 10 Hz signal generated on board C1-10. Counter Z7 is incremented once each minute through the enabling action of the 1MIN signal present at pin 10. Output pin 15 of Z7 (carry output) will similarly enable counter Z11 for one clock pulse every 10 minutes. In addition, gate Z3 pin 11 forms a 10 minute pulse four micro-seconds wide by NANDing the 10 minute enable signal with the 0.1 second pulse generated on board C1-10. Gate Z3 pin 8 merely inverts this signal.

Gate Z6 pin 8 decodes the output of counter Z11. When the count has reached five (fifty minutes) and Z7 pin 15 is high (nine minutes) this output will go low. The low is applied to the clear input of Z11 and inverted through gate Z6 pin 12 and applied to the enable input of the one hour counter Z15. Since all of these counters are fully synchronous, at the next clock pulse during which Z7 is enabled, Z11 will be reset and Z15 will be incremented to the next hour. Since Z6 pin 12

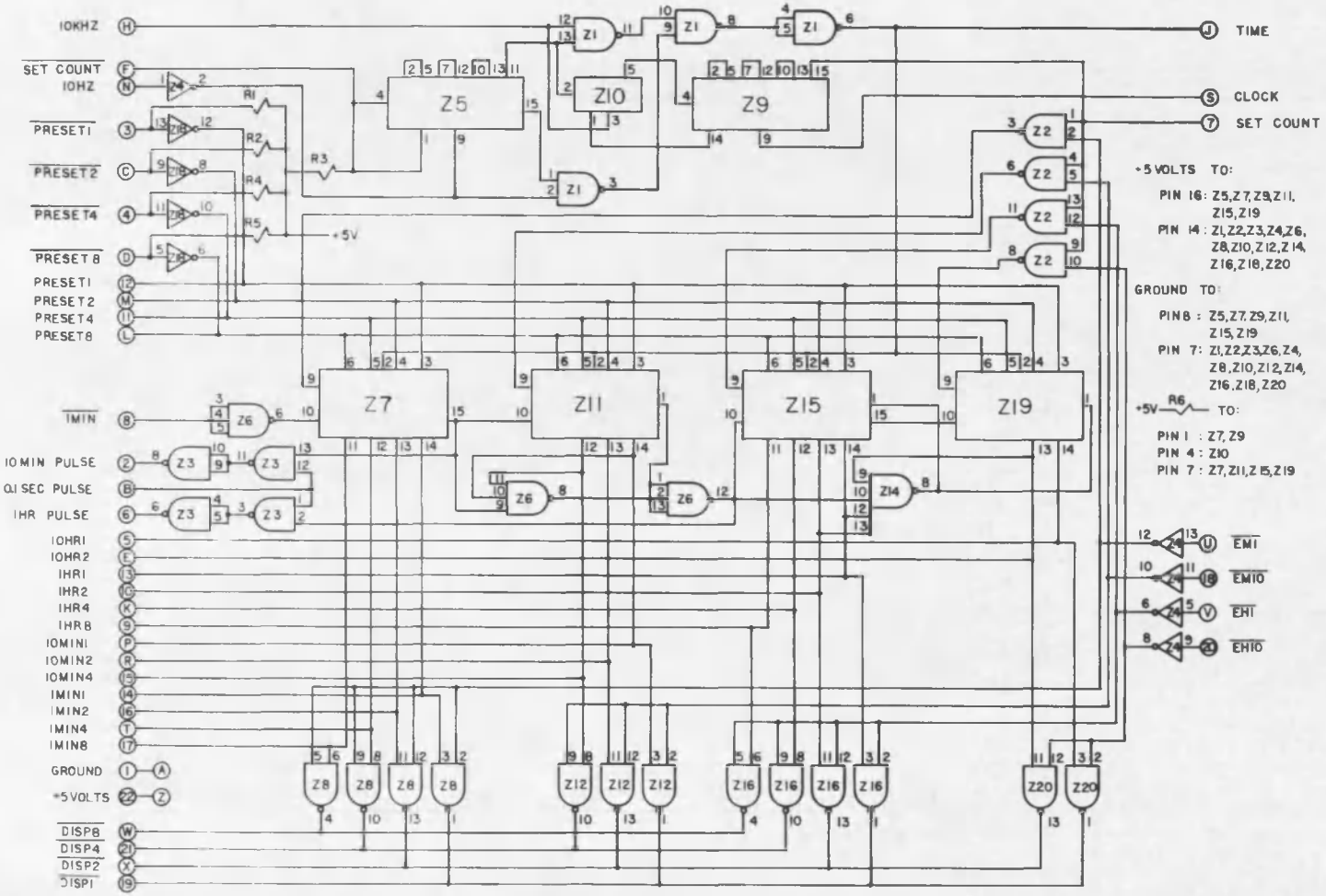

Figure 9. Board C2-11 Clock Divider

Table 2. Board C2-11 Parts List

Z1	Quad 2 input NAND gate	SN7400N
Z2	Quad 2 input NAND gate	SN7400N
Z3	Quad 2 input NAND gate	SN7400N
Z4	Hex inverter	SN7404N
Z5	Quad D type register	SN74175N
Z6	Triple 3 input NAND gate	SN7410N
Z7	Fully synchronous decade counter	SN74162N
Z8	Quad 2 input NAND gate with open collector	SN7401N
Z9	Quad D type register	SN74175N
Z10	Dual D flip flop	SN7474N
Z11	Fully synchronous decade counter	SN74162N
Z12	Quad 2 input NAND gate with open collector	SN7401N
Z14	Dual 4 input nand gate	SN7420N
Z15	Fully synchronous decade counter	SN74162N
Z16	Quad 2 input NAND gate with open collector	SN7401N
Z18	Hex Schmitt Trigger	SN7414N
Z19	Fully synchronous decade counter	SN74162N
Z20	Quad 2 input NAND gate with open collector	SN7401N
R1-R6	1.0 K 1/8 watt resistors, 5%	

goes high each hour, it is gated with the 0.1 second pulse at Z3 pin 3 and inverted to form a one hour pulse.

Counters Z15 and Z19 and gate Z14 generate the one hour and ten hour digits of the twenty-four hour clock. Z15 pin 10 is enabled for one clock pulse each hour and generates an enable signal for Z19 at pin 15. Thus these two counters will increment until both are cleared by a low signal at the output of Z14. Z14 pin 8 will go low only when counters Z15 and Z19 have counted to twenty-three and Z15 pin 10 is enabled. The next 10 Hz clock pulse will then reset both Z15 and Z19 to zero. All of the counter outputs are brought off of the board in parallel for presentation to the external recording equipment. In addition, these outputs are gated onto the clock display bus by gates Z8, Z12, Z16, and Z20.

As in the case of board C1-10, the stages of the digital clock on this board may also be preset to any desired (valid) time. Preset data is sent from a front panel switch block to Schmitt Triggers Z18 which invert this data and bus it to all stages of the digital clock.

Both Z5 and Z9 are quad D registers which are externally connected to form four bit shift registers. In normal counting operation, the $\overline{\text{SET COUNT}}$ signal will be high while Z5 pins 11 and 15 will be low and high respectively. This causes the 10 Hz clock frequency to be gated through Z1 pins 3, 8, and 6 to the TIME line, incrementing the clock in a real time fashion. Since D flip flop Z10 has pin 2 always low in this configuration, pin 5 will remain low and pin 15 of Z9 will

thus remain low forcing a high at the LOAD inputs (pin 9) and inhibiting the loading of any counter stages.

In order to preset the clock, $\overline{\text{SET COUNT}}$ must go low. This immediately sets Z5 pins 11 and 15 high and low respectively. When Z5 pin 15 is low, the 10 Hz signal is inhibited at Z1 pin 3 while the high on Z5 pin 11 enables the 10 KHz frequency and gates it onto the TIME line. Z9 provides a four micro-second delay of the input appearing on pin 4. Thus, the first 10 KHz leading edge clocks Z10 pin 5 high which results in a high at Z9 pin 15 after four micro-seconds. When Z9 pin 15 goes high, pin 14 goes low clearing Z10 pin 5 which in turn resets Z9 pin 15 low after an additional four micro-seconds.

Z9 pin 15 is the SET COUNT output. When this function is gated with the enable signals (e.g., $\overline{\text{EMT}}$) a four micro-second wide low pulse is presented to the counter corresponding to the enable signal. The enable signals are changed with the leading edge of the 10 KHz pulse and the counters are then loaded on the trailing edge of this pulse.

When $\overline{\text{SET COUNT}}$ again goes high, the counters continue to be preset for three 10 Hz pulses. On the third 10 Hz pulse, the 10 KHz preset clock is inhibited (Z5 pin 11 goes low) and Z10 pin 2 is inhibited which ensures that no SET COUNT pulses will be issued, thus locking out the front panel preset switches. When the fourth 10 Hz pulse arrives, Z5 pin 15 goes high and enables the 10 Hz counting clock through Z1 pin 3. The clock will now increment normally from the preset time. Table 3 shows the time set into the digital clock as a function of the front panel CLOCK PRESET switches.

Table 3. Clock Preset States

Switch Settings	Response					
	Seconds	Seconds X10	Minutes	Minutes X10	Hours	Hours X10
0	0	0	0	0	0	0
1	1	1	1	1	1	1
2	2	2	2	2	2	2
3	3	33	3	3	3	3*
4	4	4	4	4	4	0*
5	5	5	5	5	5	1*
6	6	6*	6	6*	6	2*
7	7	7*	7	7*	7	3*
8	8	0*	8	0*	8	0*
9	9	1*	9	1*	9	1*

*Indicates presettable states only--these states cannot be reached in normal counting.

Multiplexed Display Circuitry

Two boards, DD-7 Display Decode Logic and DE-9 Display Enable logic make up the time division multiplexed display circuitry for the DAIU. Three seperate display busses are used in the unit: Clock Display (CKDISP), Error Display (ERDISP), and Special Display (SPDISP).

Board DD-7 DISPLAY DECODE LOGIC. This board contains the circuitry required for decoding (BCD-seven segment) the three busses. The schematic for this board is shown in Figure 10 with the parts list provided as Table 4. Z1 and Z4 are BCD-seven segment decoders which decode the clock display and error displays (channels 1 and 2) respectively. The outputs are fed into the bases of the seven transistor common emitter arrays Z2 and Z5. The collectors of these transistors are then connected through current limiting resistors to the segments of the light emitting diode (LED) displays.

Z11 is a 32 X 8 read-only-memory (ROM) which has been programmed to operate as a BCD-seven segment decoder when FUNCTION SELECT is high. The lower half of the memory, corresponding to a low on FUNCTION SELECT, is programmed to display either a 1, 2, 3, or H depending on the codes presented on the SPDISP bus. The outputs of the ROM are inverted and presented to a transistor array as above. The ROM inputs are gated by Z12 and Z9 to provide a lamp test function. When the inputs to the ROM are all high, the outputs will go low causing all segments of the display to light. Z1 and Z4 have this feature built into them at pin 3.

Z3 is a retriggerable monostable multivibrator whose outputs enable the decoders Z1 and Z4 and the ROM Z11. In the event that the

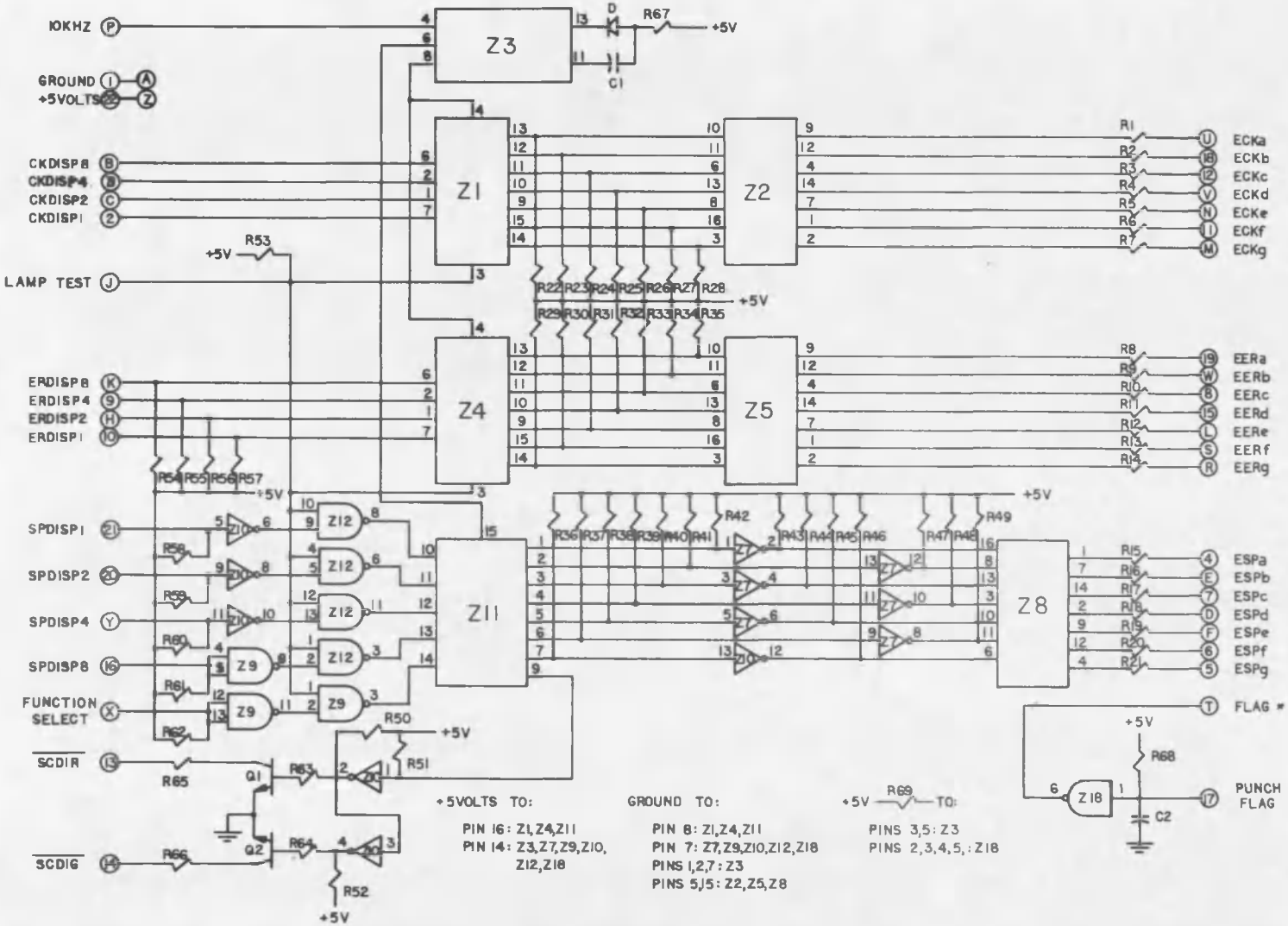

Figure 10. Board DD-7 Display Decode Logic

Table 4. Board DD-7 Parts List

Z1	BCD-7 segment decoder		SN7448N
Z2	Common emitter transistor array	(RCA)	CA3081
Z3	Retriggerable monostable multivibrator		SN74122N
Z4	BCD-7 segment decoder		SN7448N
Z5	Common emitter transistor array	(RCA)	CA3081
Z7	Hex inverter		SN7404N
Z8	Common emitter transistor array	(RCA)	CA3081
Z9	Quad 2 input NAND gate		SN7400N
Z10	Hex inverter		SN7404N
Z11	Programmable read only memory [ROM]	(INTERSIL)	IM5600CP
Z12	Quad 2 input NAND gate		SN7400N
Z18	Dual NAND Schmitt Trigger		SN7413N
R1-R21	4.7 1/8 watt resistors, 5%		
R22-R52	5.1 K 1/8 watt resistors, 5%		
R53-R64	1.0 K 1/8 watt resistors, 5%		
R65	68 1/8 watt resistor, 5%		
R66	27 1/4 watt resistor, 5%		
R67	10.0 K 1/8 watt resistor, 5%		
R68	2.7 K 1/8 watt resistor, 5%		
R69	1.0 K 1/8 watt resistor, 5%		
C1	0.47 F capacitor		
C2	1.0 F capacitor		
D	Silicon signal diode		1N154

multiplexing frequency fails, this device will change states and disable all decoder outputs resulting in a blank display. If this precaution were not taken, it would be possible for one digit to be continuously enabled. Since the multiplexing current is ten times greater than the continuous rating of the LED display, this would result in the rapid destruction of the device due to overheating.

Board DE-9 DISPLAY ENABLE LOGIC. This board contains the digit enable circuitry for the multiplexing system. Figure 11 shows the schematic of this board while Table 5 provides a parts list. Z1, Z5, and Z9 are BCD-decimal decoders. Each of these devices has the most significant bit of the address permanantly connected to a low logic level so that in effect the devices operate as three line to eight line decoders. The inputs to each decoder are the multiplex strobe address. Each of the eight addressed outputs will go low in succession as the strobe addresses are incremented.

The outputs of Z1 are routed to the front panel CLOCK PRESET switches to gate the preset data onto the preset data bus. All decoder outputs are connected to the transistors as shown. The transistor collectors are connected to the common anode connection on the seven segment display. Each transistor will thus be turned on in sequence when the corresponding decoder output goes low. This in effect switches the anode of the display to the +5 volt supply while the segment enable transistors of board DE-7 supply grounds to the correct segments. Z1 drives the clock display, Z2 drives the channel 1 and channel 2 error displays, and Z3 drives the special channel display.

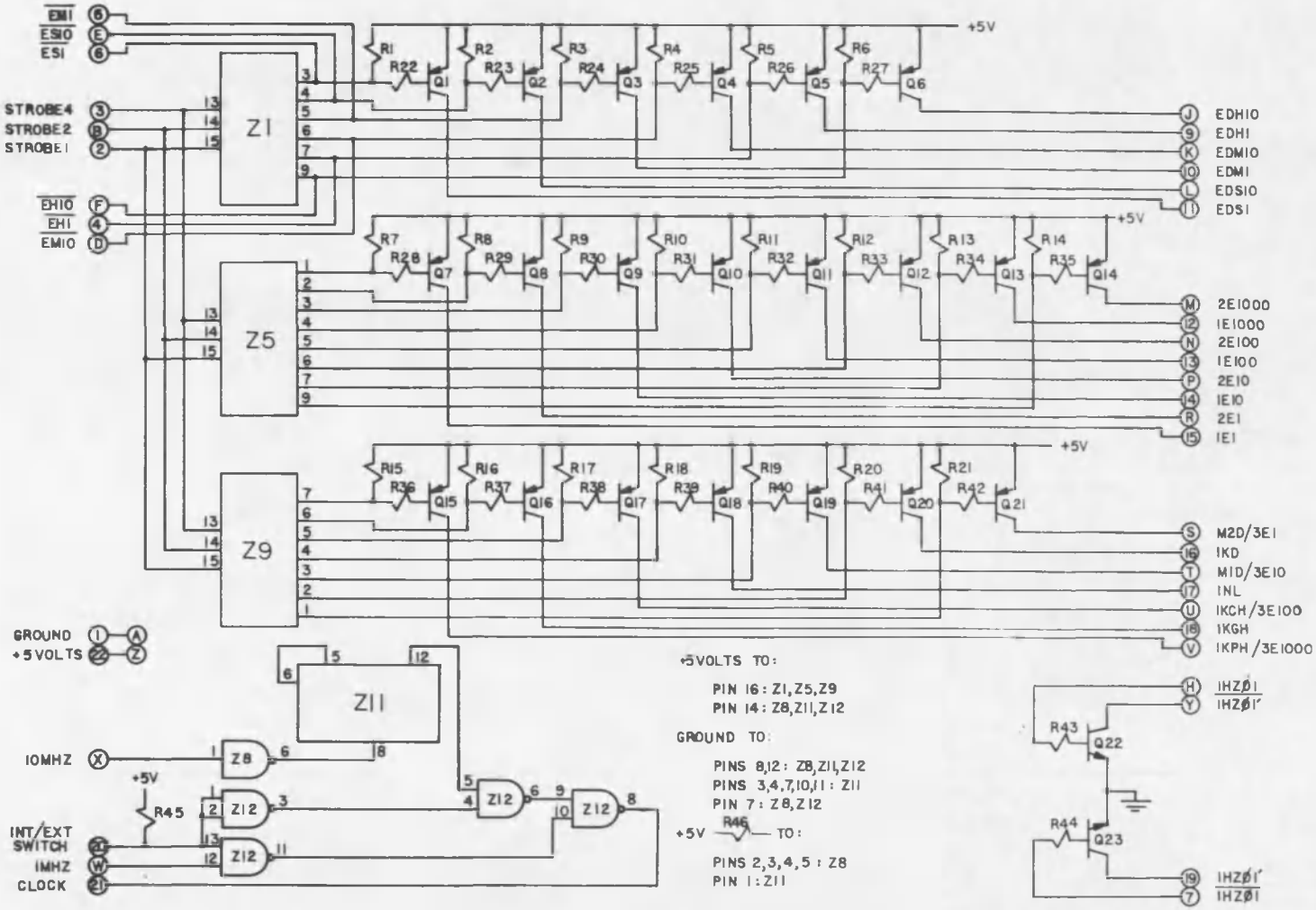

Figure 11. Board DE-9 Display Enable Logic

Table 5. Board DE-9 Parts List

Z1	BCD-Decimal decoder	SN74145N
Z5	BCD-Decimal decoder	SN74145N
Z8	Dual NAND Schmitt Trigger	SN7413N
Z9	BCD-Decimal decoder	SN74145N
Z11	Decade counter	SN74176N
Z12	Quad 2 input NAND gate	SN7400N
Q1-Q21	PNP transistors	2N5813
Q22-Q23	NPN transistors	2N2222
R1-R21	10.0 K 1/8 watt resistors,5%	
R22-R42	68 1/8 watt resistors,5%	
R43,R44	5.1 K 1/8 watt resistors,5%	
R45,R46	1.0 K 1/8 watt resistors,5%	

Transistors Q22 and Q23 provide extra current drive for the 1.0 Hz frequency used to drive warning, alarm, and test indicator LEDs. Counter Z11 divides an external 10.0 MHz signal by ten to obtain a 1.0 MHz clock frequency. Gates Z12 select which clock frequency is to be used in the DAIU. The front panel CLOCK SOURCE switch will ground Z12 pins 1, 2, and 13 for the external clock. If these pins are not grounded, the internal 1.0 MHz frequency (from the crystal oscillator of board C1-10) will be selected. An appropriate front panel LED indicator lamp will light to indicate the clock source selected.

Modem Interface and Error Counters

Boards MI-1, 3, and 5 MODEM INTERFACE. The modem interface boards provide complete interfacing between the DAIU and the modems. One interface board is required for each channel in operation. All three boards are identical with provisions for changing the actual interface circuitry. Since all three boards are identical, only one schematic, Figure 12, and parts list, Table 6, is shown. To interpret the schematics the asterisk (*) in the signal names should be replaced by the number of the channel under consideration. Thus for the channel 2 modem interface, board MI-3, the signal CH* CK ALARM becomes CH2 CK ALARM indicating a channel 2 modem clock alarm. Similarly, when channel 1 is being considered, this signal should be interpreted as CH1 CK ALARM.

The modem interface boards provide the following functions:

- Converts modem clock and data signal levels to TTL compatible levels
- Generates a series of transfer pulses

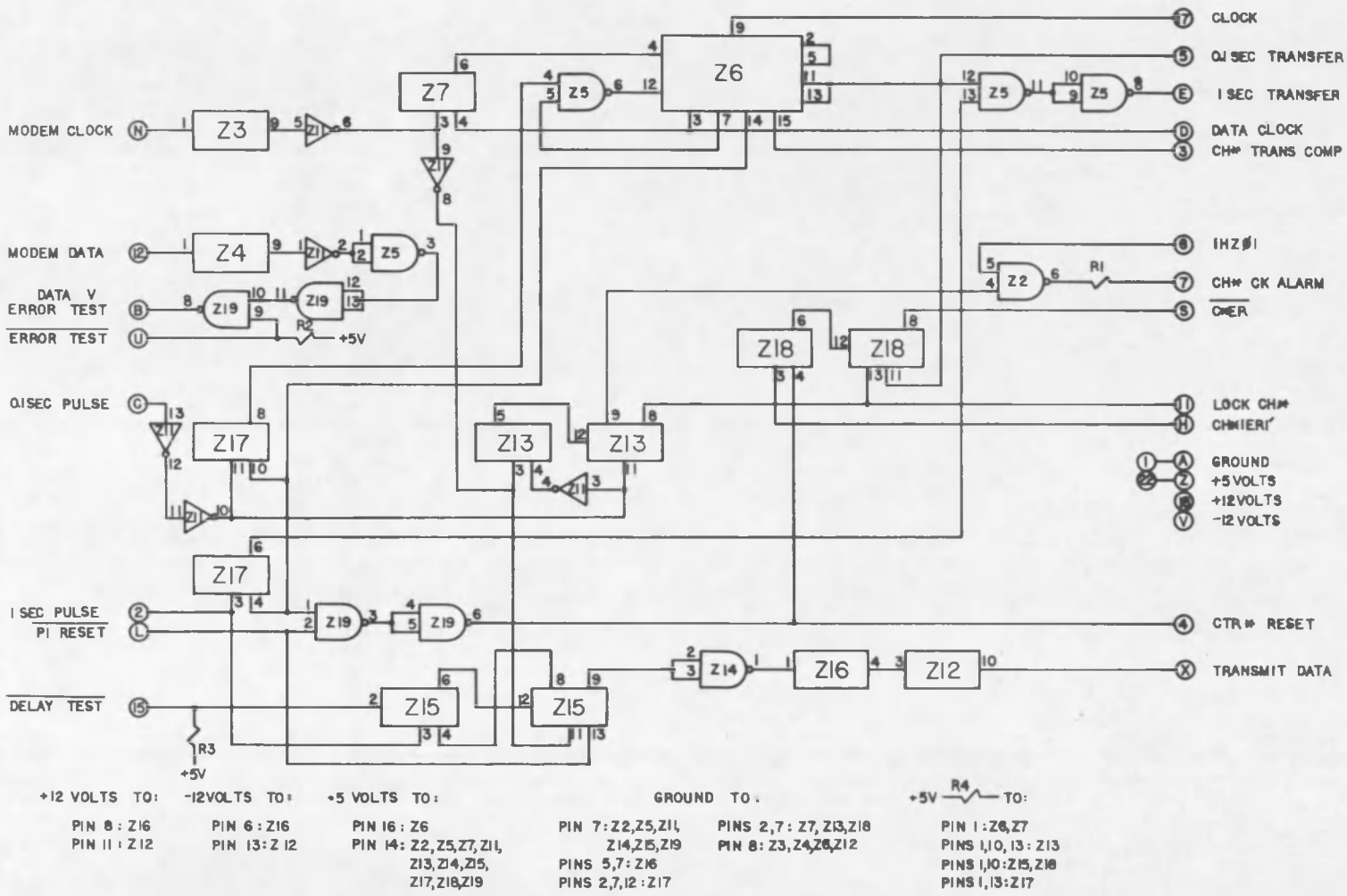

Figure 12. Boards MI-1, 3, and 5 Modem Interface

Table 6. Boards MI-1, 3, and 5 Parts List

Z2	Quad 2 input NAND gate	SN7400N
Z3	Modem interface module	M401
Z4	Modem interface module	M401
Z5	Quad 2 input NAND gate	SN7400N
Z6	Quad D flip flop	SN74175N
Z7	Dual D flip flop	SN7474N
Z11	Hex Schmitt Trigger	SN7414N
Z12	MS188 output module	M409
Z13	Dual D flip flop	SN7474N
Z14	Quad 2 input NAND gate with open collector	SN7401N
Z15	Dual D flip flop	SN7474N
Z16	MS188 level converter	M410
Z17	Dual D flip flop	SN7474N
Z18	Dual D flip flop	SN7474N
Z19	Quad 2 input NAND gate	SN7400N
R1,R2	1.0 K 1/8 watt resistors,5%	
R3	150 1/4 watt resistor, 5%	
R4	1.0 K 1/8 watt resistor, 5%	

- Generate error counter clock and enable functions
- Provide a modem clock alarm function
- provide for ERROR and DELAY TEST functions.

Modem clock and data signals are converted to TTL logic levels by interface circuits Z3 and Z4 and their respective Schmitt Triggers Z11. The schematics for these interface circuits were provided by the Government through the Mitre Corporation. As mentioned in Chapter II, the MODEM DATA line will be high whenever errors are present. The output DATA V ERROR TEST is used to enable the error counter and is generated by gating the MODEM DATA signal with an $\overline{\text{ERROR TEST}}$ level selectible by a front panel switch. Gates Z5 output pin 3 and Z19 pin 11 are used to buffer the data signal. The output at Z19 pin 8 will then be high whenever MODEM DATA is high or whenever $\overline{\text{ERROR TEST}}$ is low. This output enables the error counter.

The modem clock frequency is similarly converted to TTL levels and inverted at Z11 pin 6. The falling edge of the MODEM CLOCK clocks Z7 pin 6 high which enables the first stage of the quad D register Z6. This register is clocked at a 1.0 MHz rate (by CLOCK). Output pin 3 of Z6 is normally high, but when Z7 pin 6 goes high the next leading 1.0 MHz edge clocks pin 3 low. This low then immediately resets Z7 pin 6 low so that the next leading 1.0 MHz edge returns Z6 pin 3 high. This output, DATA CLOCK,is used to clock the error counters. Since the modem data changes at the leading edge of the modem clock, the DATA CLOCK pulse, occurring approximately midway between leading MODEM CLOCK pulses, is guaranteed to count an error if MODEM DATA is high.

At the same time Z6 pin 3 goes low, pin 2 goes high enabling the second stage of the register. Thus the leading edge of the 1.0 MHz clock which returns pin 3 high also clocks pin 7 high enabling gate Z5 pin 4. Pin 4 will be high only following a tenth second pulse (which clocks Z17 pin 8 high). If no tenth second pulse has occurred, the last two stages of Z6 will not be enabled and no transfer or clear pulses will be generated. This allows the error counter to continue counting for the full tenth second sample interval.

When the tenth second pulse clocks Z17 pin 8 high, and Z5 pin 5 is high, Z6 pin 12 is enabled clocking pin 11 high on the third 1.0 MHz leading edge following the trailing edge of the MODEM CLOCK pulse. This output is the 0.1 SECOND TRANSFER pulse which is presented to the error counters. The next leading 1.0 MHz edge resets Z6 pin 11 low and forces pins 15 and 14 high and low respectively. Pin 15 forms the TRANSFER COMPLETE signal which informs the function control logic that this channel's data has been transferred to latches and that the data is ready to be recorded. Output 14 resets the 0.1 second flip flop Z17 pin 8 low and also resets the 1 minute flip flop Z17 pin 6 low. In addition, this signal is gated with a power-on-reset function and forms the CTR* RESET signal. This signal resets the error counter when power is initially applied to the DAIU and one micro-second following the 0.1 SECOND TRANSFER pulse. The one second pulse sets the one second flip flop Z17 pin 6 high. This output is gated with the 0.1 SECOND TRANSFER pulse to obtain a 1 SECOND TRANSFER pulse. Both transfer pulses are used by the error counter board.

D flip flop Z13 and inverter Z11 provide a crude modem clock alarm function. Each leading edge of the MODEM CLOCK triggers Z13 pin 5 low. When the 0.1 second pulse arrives, it transfers the output level of pin 5 to pin 9, and at the same time sets Z13 pin 5 high. Thus pin 9 will normally be low. This inhibits the clock alarm at Z2 pin 6. At the same time Z13 pin 8 is high indicating to the function control logic that this particular channel is locked onto the modem clock frequency.

If the modem clock is interrupted, the 0.1 second pulse will set Z13 pin 5 high. If no modem clocks are received, the next 0.1 second pulse will transfer this high to pin 9 which enables the alarm function at Z2 pin 6. This in turn causes a front panel CLOCK ALARM lamp to flash at a 1.0 Hz rate. At the same time Z13 pin 8 goes low indicating to the function control logic that no clock is being detected on the corresponding channel. This condition will remain until the modem clock is restored.

D flip flop Z18 generates a signal which alerts the function control logic that at least one error has been counted by the error counter associated with this interface board. The first error counted, (CH* 1ER1') clocks Z18 pin 6 high which enables Z18 pin 12. When the 0.1 SECOND TRANSFER pulse occurs, this high is transferred to Z18 pin 9. Z18 pin 8 then goes low indicating to the function control logic that an error has been counted on this channel. The counter reset pulse, (CTR* RESET), resets Z18 pin 6 low so that the above operation may be repeated in the next tenth second sample period. If no modem clocks

are detected, Z18 pin 13 will be low forcing pin 8 high. This causes the function control logic to ignore the unclocked channel.

The only remaining function on the interface boards is the generation of a pulse used in an absolute (looped) delay test configuration. This test is initiated by grounding Z15 pin 2 through the appropriate front panel DELAY TEST switch. Under this condition, the first following one second pulse clocks Z15 pin 6 high enabling pin 12. The next modem clock pulse clocks Z15 pins 8 and 9 low and high respectively. The low on pin 8 resets pin 6 low so that the next modem clock pulse will return pin 9 low. At this point the process will repeat with the next one second pulse. The resulting output pulse at Z15 pin 9 will be a pulse which is high for one modem clock period each second. This pulse is inverted at Z14 pin 1 and converted to MIL STD 188 output by level shifting circuit Z16 and output module Z12. Schematics for these circuits may be found in Figure 13 and were provided by the Government through the Mitre Corporation.

Boards EC-2, 4, and 6 ERROR COUNTER. The error counter boards provide the circuitry to count channel errors and temporarily store this information for use by the external recording equipment. In addition, the information is also stored for presentation to the front panel displays. The schematic for the error counters is shown in Figure 14 and the parts list given as Table 7.

Counters Z5, Z9, Z13, and Z17 form a four decade counter which accumulates the errors in any tenth second interval. The counter is clocked by the DATA CLOCK signal and enabled by the DATA V ERROR TEST

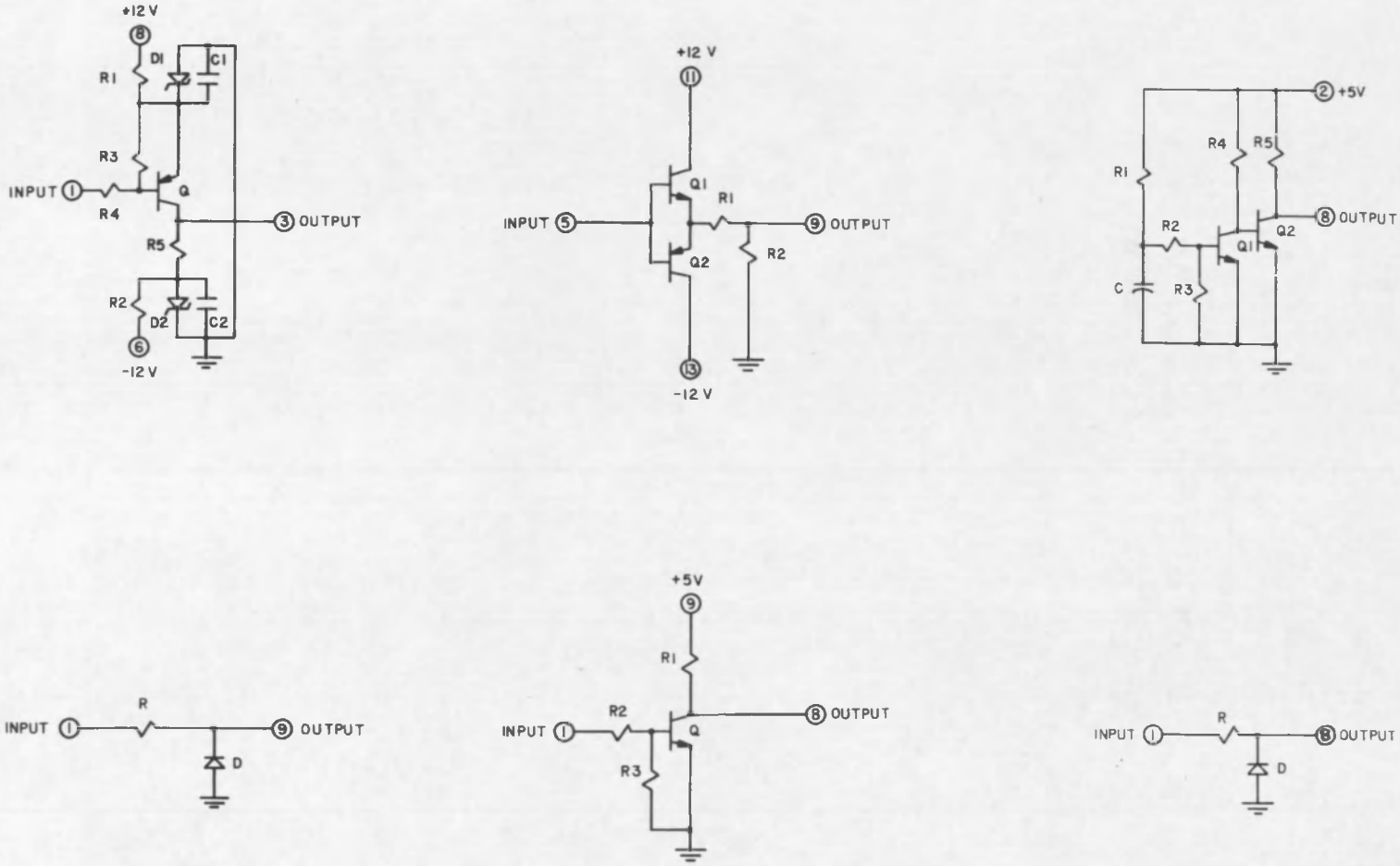

Figure 13. Discrete Modules Used in the DAIU

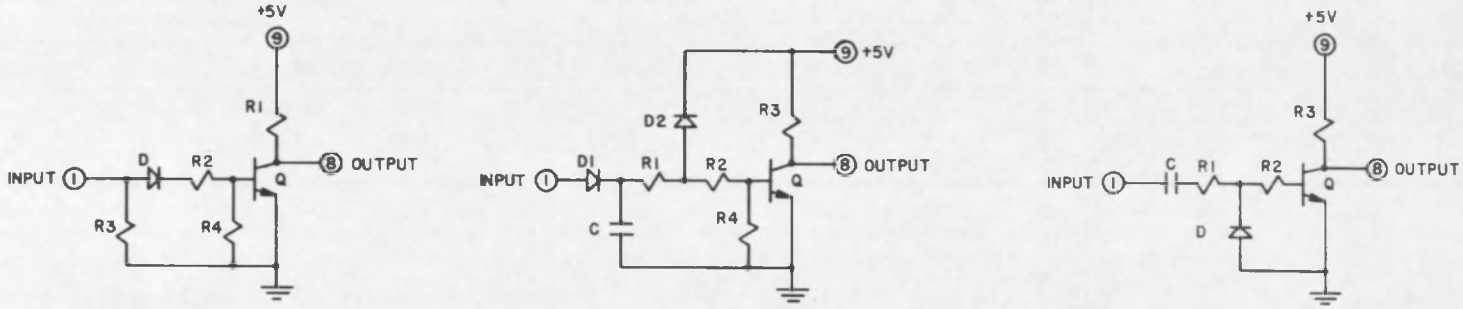

Figure 13. Continued

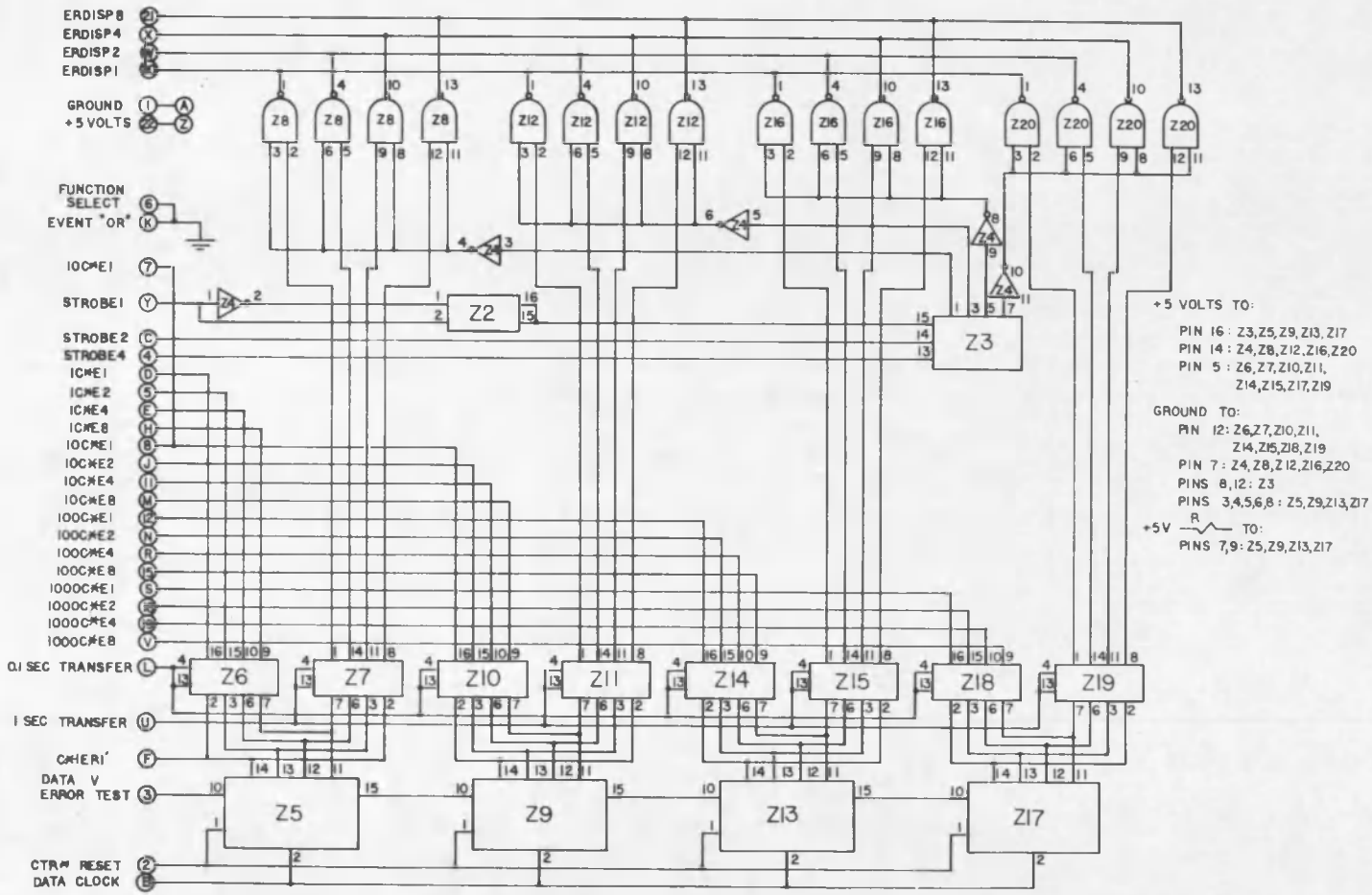

Figure 14. Boards EC-2, 4, and 6 Error Counter

Table 7. Boards EC-2, 4, and 6 Parts List

Z2	Display select module	M404 or M405*
Z3	BCD-Decimal decoder	SN7442N
Z4	Hex inverter	SN7404N
Z5	Synchronous decade counter	SN74160N
Z6	Quad latch	SN7475N
Z7	Quad latch	SN7475N
Z8	Quad 2 input NAND gate with open collector	SN7401N
Z9	Synchronous decade counter	SN74160N
Z10	Quad latch	SN7475N
Z11	Quad latch	SN7475N
Z12	Quad 2 input NAND gate with open collector	SN7401N
Z13	Synchronous decade counter	SN74160N
Z14	Quad latch	SN7475N
Z15	Quad latch	SN7475N
Z16	Quad 2 input NAND gate with open collector	SN7401N
Z17	Synchronous decade counter	SN74160N
Z18	Quad latch	SN7475N
Z19	Quad latch	SN7475N
Z20	Quad 2 input NAND gate with open collector	SN7401N
R	1.0 K 1/8 watt resistor, 5%	

*M405 is used only on boards EC-4 and EC (spare) when used in channel 2 error counter slot.

signal generated on the modem interface board. Although the fastest modem clock normally encountered is 39.0 kilobits per second, the error counter can count up to 5000 indicating a clock frequency of 50.0 KB/s.

The counter outputs are connected to two sets of temporary storage latches. Z6, Z10, Z14, and Z18 are the tenth second temporary store. This store holds the counter outputs for a tenth second period during which time this information is recorded by the external equipment. The latches are updated every tenth second by the 0.1 SECOND TRANSFER pulse. As soon as the information is transferred, the counter is reset to zero by CTR* RESET.

Latches Z7, Z11, Z15, and Z19 form the one second store. This store is updated every second by the 1 SECOND TRANSFER pulse and is used to provide data to the error display bus. The outputs of these latches are gated onto the error display bus by open collector gates Z8, Z12, Z16, and Z20 respectively. BCD-decimal decoder Z3 and the strobe addresses determine which digit of the error count is gated to the bus. Z2 is a discrete module which selects either STROBE1 or $\overline{\text{STROBE1}}$ as the least significant address bit of the decoder. This allows all error counters to be identical except for this plug-in module. If STROBE1 is selected (shorting bar from pin 2 to pin 15 of Z2), the error count will appear on the CHANNEL 1 ERRORS display. If $\overline{\text{STROBE1}}$ is selected, (shorting bar between pins 1 and 16 of Z2), the error count will appear on the CHANNEL 2 ERRORS display. For the channel three error count, the special display bus is used as described in the display section above.

Output pins 6 and K of this board are grounded as shown. These outputs have no function unless the error counter board is inserted into the third channel error counter slot. When this is done, the logical low on the FUNCTION SELECT line informs the recording equipment that three channel errors are to be recorded requiring 69 data bits as opposed to two channel errors and special events requiring only 63 data bits. A low on EVENT "OR" ensures that the corresponding input to the function control logic is specified. These two functions are more fully described in the sections relating to the special events display and store and the function control boards.

Special Events Circuitry

Board SI-5 SPECIAL EVENTS INTERFACE. This board provides for the interfacing of the special events monitored in the two channel operating mode. Figure 15 and Table 8 show the circuit schematic and parts list respectively for this board. Circuits Z1 through Z9 are discrete interface circuits (provided by the Government through the Mitre Corporation) which, along with Schmitt Triggers Z10 and Z12 convert the input levels to TTL compatible signals. The modem dropouts are level functions (Z10 pins 2 and 4) while the remaining special events produce pulsed signals. D flip flops Z13 through Z16 and Z20 are the accumulators of the special events data. When any event occurs, the corresponding flip flop output will go high. In the case of the modem dropouts, a low on Z10 pin 2 or 4 will clear Z13 forcing a high on the $\overline{Q}$ output pin 6 or 8 respectively. The remaining flip flops are clocked low by the occurrence of an event forcing the $\overline{Q}$ outputs high.

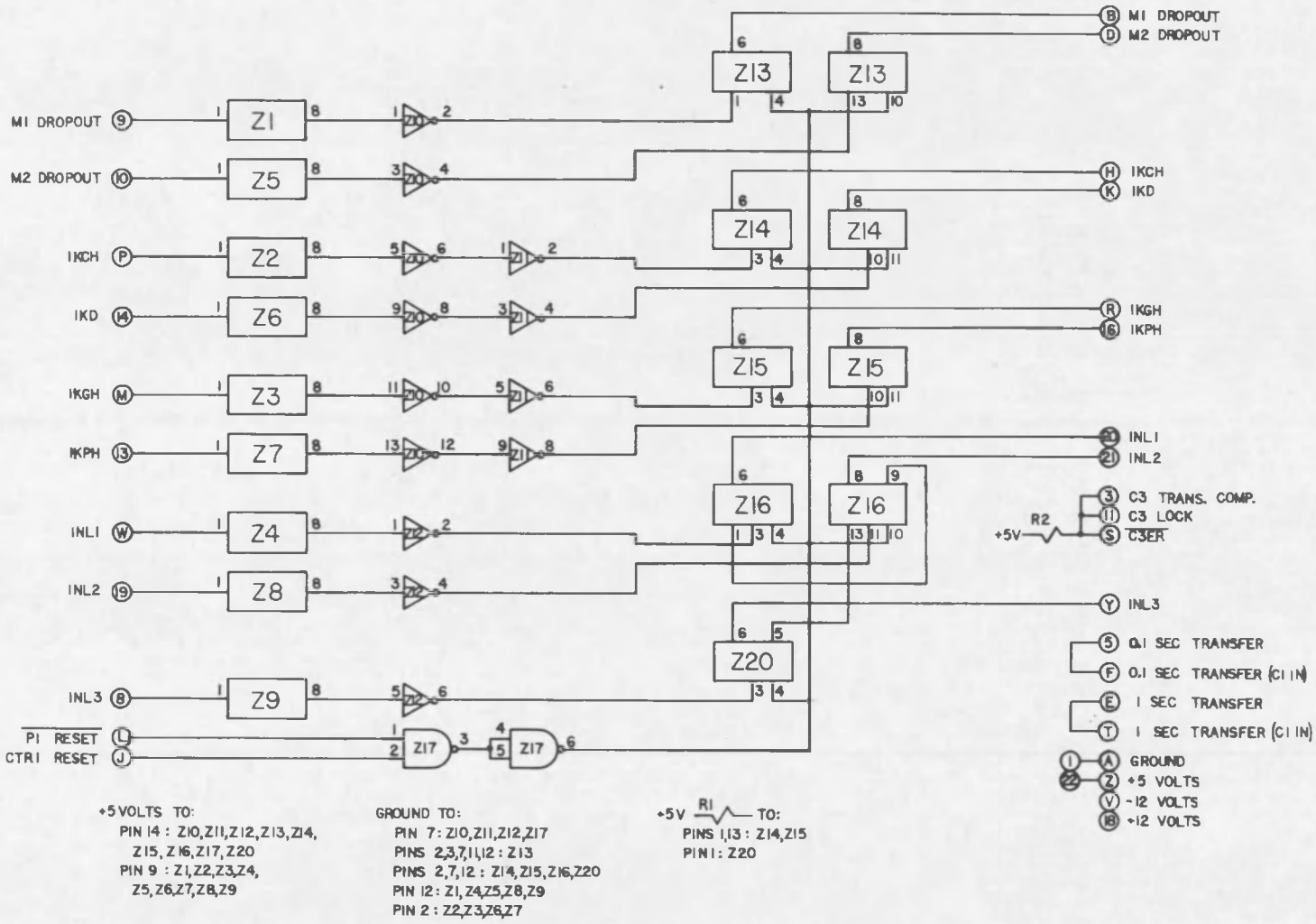

Figure 15. Board SI-5 Special Events Interface

Table 8. Board SI-5 Parts List

Z1		Channel 1 modem dropout interface	M406C*
Z2		Hekemian interface	
Z3		Hekemian interface	
Z4		INL interface	
Z5		Channel 2 modem dropout interface	M406V*
Z6		Hekemian interface	
Z7		Hekemian interface	
Z8	INL	INL interface	
Z9		INL interface	
Z10		Hex Schmitt Trigger	SN7414N
Z11		Hex inverter	SN7404N
Z12		Hex Schmitt Trigger	SN7414N
Z13		Dual D flip flop	SN7474N
Z14		Dual D flip flop	SN7474N
Z15		Dual D flip flop	SN7474N
Z16		Dual D flip flop	SN7474N
Z17		Quad 2 input NAND gate	SN7400N
Z20		Dual D flip flop	SN7474N
R1,R2		1.0 K 1/8 watt resistors, 5%	

*M406C is used for the Bell System 303 modem
M406V is used for the Bell System 203 modem

The impulse noise levels (INL1, INL2, and INL3) are not independent. If a severity 3 noise level is received, then levels 1 and 2 must also be set. Similarly, level 2 includes level 1. Thus INL1 clocks Z16 pin 6 high. INL2 clocks Z16 pins 8 and 9 high and low respectively. The low at pin 9 is connected to the clear input Z16 pin 1 and forces Z16 pin 6 (INL1) high also. Similarly, INL3 clocks Z20 pin 6 high and pin 5 low. A low on pin 5 sets Z16 pin 8 (INL2) high and pin 9 low which in turn sets Z16 pin 6 (INL1) high.

All flip flops are cleared by a power-on-reset function ($\overline{\text{P1 RESET}}$) when the unit is turned on and by the CTR1 RESET pulse generated by the modem interface board of channel 1. Outputs 3, 11, and S specify inputs to the function control logic which would otherwise remain floating. The 0.1 SECOND TRANSFER and 1 SECOND TRANSFER pulses from the channel 1 interface board also enter the board and are fed to the special events display and store board.

Board SD-6 SPECIAL EVENTS DISPLAY AND STORE. This board provides temporary storage for recording and displaying the special events information. A schematic of this board is shown in Figure 16 with the parts list given as Table 9. Quad D registers Z2 and Z6 and D flip flop Z10 form the tenth second stores while quad D registers Z15 and Z19 form the one second display store. A power-on-reset function initially clears all stores. Each 0.1 SECOND TRANSFER pulse from MI-1 transfers the special events data from the interface accumulators to the tenth second storage registers. The Q outputs of these registers will be high whenever the corresponding event has occurred. These

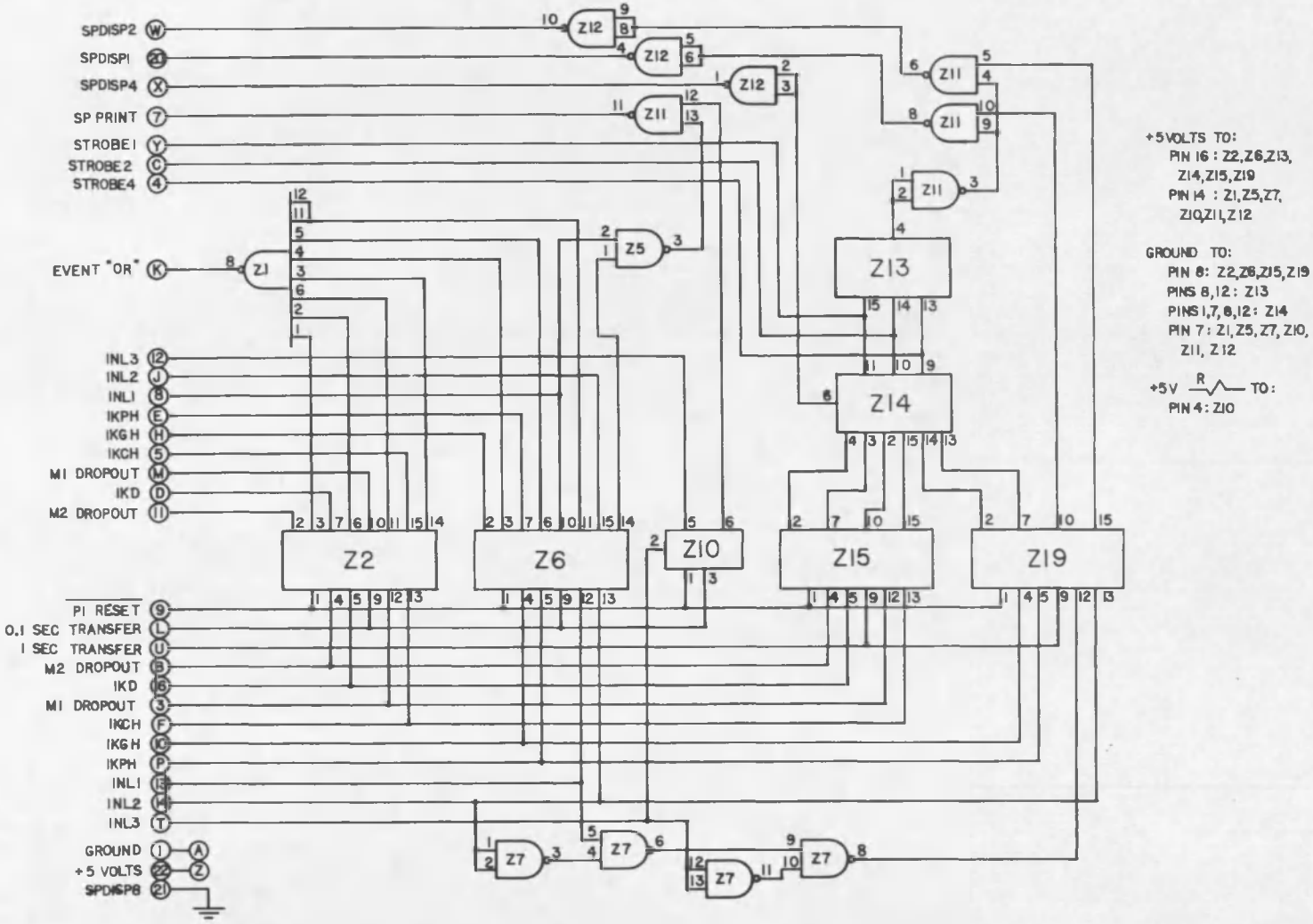

Figure 16. Board SD-6 Special Events Display and Store

Table 9. Board SD-6 Parts List

Z1	Eight input NAND gate	SN7430N
Z2	Quad D type register	SN74175N
Z5	Quad 2 input NAND gate	SN7400N
Z6	Quad D type register	SN74175N
Z7	Quad 2 input NAND gate	SN7400N
Z10	Dual D flip flop	SN7474N
Z11	Quad 2 input NAND gate	SN7400N
Z12	Quad 2 input NAND gate with open collector	SN7401N
Z13	BCD-Decimal decoder	SN7442N
Z14	8 bit data selector	SN74151N
Z15	Quad D type register	SN74175N
Z19	Quad D type register	SN74175N
R1	1.0 K 1/8 watt resistor, 5%	

outputs are brought off of the board for parallel presentation to the external recording equipment. Gate Z1 forms an "OR" function over all seven special events (INL is one event here regardless of severity) so that whenever any one or more of the events occurs, the output Z1 pin 8 will go high. This output informs the function control logic that a special event has occurred and that data is present to be recorded. Gates Z5 pin 3 and Z11 pin 11 form the function (INL1 $\wedge$ $\overline{\text{INL2}}$) $\vee$ INL3 which leaves the board on pin 7 as a SPECIAL PRINT character. Due to the limited number of printer output columns available, this special print symbol encodes the data correctly ensuring that only the highest level impulse noise is recorded by the printer. The punch and digital recorder on the other hand actually record three bits (one for each level).

The outputs of latches Z15 and Z19 are combined to produce the proper display code for the special channel. The occurrence of any event will result in an "H" on the appropriate display area while no occurrence will result in a blank display. The only exception to this is the impulse noise level which will display a blank, 1, 2, or 3 indicating the highest level of severity.

The BCD information appearing on the special channel bus (SPDISP) is decoded by the ROM of board DD-7 into the proper seven segment display code. Since only five distinct display symbols are required for the special channel, only three of the special display bus addresses are used (SPDISP8 grounded). The six events which cause an "H" to be displayed are connected to the inputs of an eight bit data selector Z14.

The actual bit selected is determined by the multiplexing strobe address lines. Table 10 shows the display code possibilities. Since the impulse noise level is the only input capable of generating a 1, 2, or 3, this information is locked out of the multiplexed bus except when the INL digit is enabled by a low on Z13 pin 4. Z14 pin 6 is the inverted output and gates the selected input onto SPDISP4.

Table 10. Special Channel Display Code

Bus Data			Symbol Displayed
SPDISP4	SPDISP2	SPDISP1	
0	0	0	Blank
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	H

Z19 pin 15 provides the function INL2 while pin 10 provides $(INL1 \wedge \overline{INL2}) \vee INL3$ to the display. Thus when the strobe address is 011, Z14 pin 6 selects pin 1 (grounded) forcing SPDISP4 low. At this time Z13 pin 4 is low enabling Z11 pins 6 and 8. For INL1, Z19 pin 10 is high and 15 is low resulting in a 001 display code (1). For INL2, Z19 pin 10 is low and pin 15 is high resulting in the 010 code (2). For INL3, both pins 10 and 15 will be high resulting in the 011 display code (3). Thus, the proper display code is generated in each instance.

Function Control Circuitry

Board FC-8 FUNCTION CONTROL. This board generates the signals required to initiate data recording by the external recording equipment. In addition, the status of the printer and punch are monitored and alarm functions are generated as required. Furthermore, the correct coding of the column 16 printer output is generated on this board. The schematic for this board is shown in Figure 17 while the parts list is given as Table 11.

Gate Z1 output pin 8 interrogates the modem interfaces and special events circuitry as well as the 0.1 second pulse. When a 0.1 second pulse arrives, Z5 pin 8 is clocked high. Z6 pin 8 will also be forced high by the arrival of the CH1 TRANS COMP pulse or by a low on the LOCK CH1 line. This ensures that data present on one channel will be recorded even though the other channels may not have any modem clock inputs. Z6 pin 6 functions in the same manner utilizing the channel 2 pulses.

When three channels are monitored, FUNCTION SELECT will be low and Z7 will provide the same information about channel 3 that Z6 provides about channels 1 and 2. When the special events are monitored, FUNCTION SELECT will be high forcing Z1 pin 13 high locking out the channel 3 status flip flop Z7. When all transfers are completed, Z1 pin 8 will go low. This enables Z5 pin 6 which goes high with the next leading edge of the 10 KHz clock. Z5 pin 5 goes low at the same time resetting Z5 pin 8, Z6, and Z8 pin 9 low. This causes Z1 pin 8 to return high which in turn resets Z5 pin 6 low at the next 10 KHz leading edge.

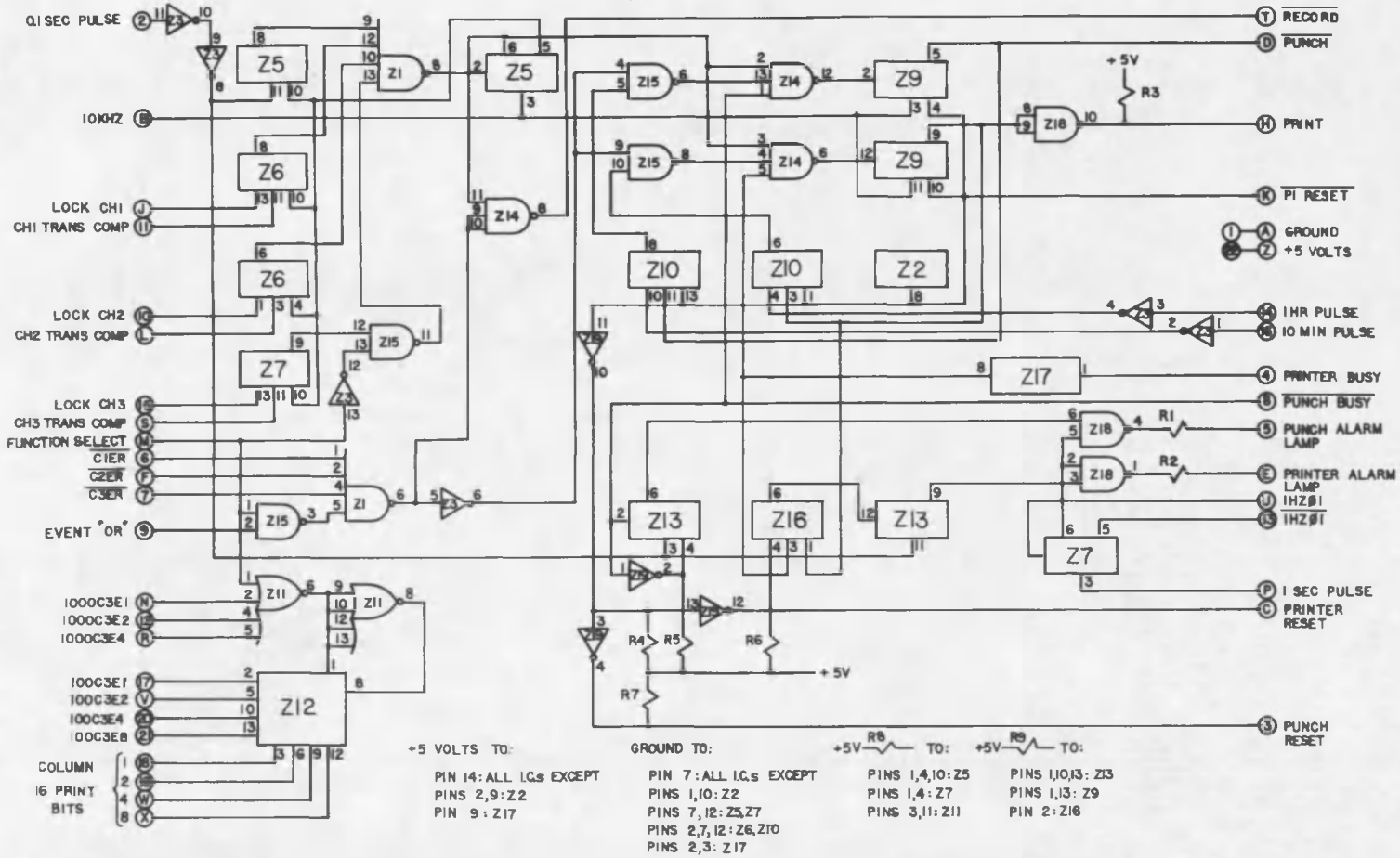

Figure 17. Board FC-8 Function Control

Table 11. Board FC-8 Parts List

Z1	Dual 4 input NAND gate	SN742ON
Z2	Power-on-reset module	
Z3	Hex inverter	SN7404N
Z5	Dual D flip flop	SN7474N
Z6	Dual D flip flop	SN7474N
Z7	Dual D flip flop	SN7474N
Z9	Dual D flip flop	SN7474N
Z10	Dual D flip flop	SN7474N
Z11	Dual 4 input NOR gate	SN7425N
Z12	4 bit true/complement, zero/one element	SN74H87N
Z13	Dual D flip flop	SN7474N
Z14	Triple 3 input NAND gate	SN7410N
Z15	Quad 2 input NAND gate	SN7400N
Z16	Dual D flip flop	SN7474N
Z17	Printer busy interface	
Z18	Quad 2 input NAND gate with open collector	SN7401N
Z19	Hex inverter	SN7404N
R1,R2	120 1/4 watt resistor, 5%	
R3-R9	1.0 K 1/8 watt resistor, 5%	

Thus, Z5 pin 6 forms a 100 micro-second wide positive pulse following the transfer of data to the recording buffers (latches).

Meanwhile, Z1 pin 6 has gone high only if data is present to record. Therefore, with data present, Z14 pin 8 will go low for 100 micro-seconds initiating a recording operation in the DAIU - Digital Recorder Unit (see Chapter IV). A high at Z1 pin 6 forces a low at Z3 pin 6. In order to record data on the paper tape punch or printer, Z15 pins 6 and 8 respectively must go high. Both will go high when Z3 pin 6 goes low. However, Z15 pin 6 will also go high whenever the 10 minute flip flop, Z10 pin 8 goes low. This guarantees that the punch mechanism will be operated every ten minutes (to prevent mechanical "freezing"). Likewise, Z15 pin 8 will go high whenever the one hour flip flop Z10 pin 6 goes low. This guarantees that the printer will be operated every hour.

Gates Z14 form the last record enable/inhibit function gating the status of the recording equipment. If the printer or punch is busy or off, Z14 pin 5 or 1 will be low, inhibiting the issuance of the corresponding print or punch command. If either of these functions are high, the corresponding Z14 outputs will be low for a maximum of 100 micro-seconds. Thus the next 10 KHz leading edge will clock Z9 pins 5 and/or 9 low for precisely 100 micro-seconds. Z9 pin 5 then resets the ten minute flip flop and activates the punch command sequencer on the punch control logic board (PC-12). Z9 pin 9 resets the one hour flip flop, is inverted and is sent to the printer as a PRINT command. The printer manual [5] contains the complete printer characteristics.

If either the printer or punch is busy (still operating on the previous block of data) no print or punch commands may be issued and an appropriate front panel alarm signal will be activated, The printer busy signal enters the board on pin 4 and is a normally low signal which goes high while the printer is operating. The printer busy interface module Z17 (supplied by the Government through the Mitre Corporation) inverts this level while converting it to a TTL compatible signal. Thus Z17 pin 8 is a normally high level which will go low while the printer operates. This signal is connected to the clock input (pin 3) of Z16 to provide a printer alarm. In addition, the signal will inhibit Z14 pin 6 and therefore prevent issuance of a printer command while the printer is operating. The printer alarm is generated by D flip flops Z16 and Z13 pin 9. When a print command is generated, Z16 pin 1 goes low for 100 micro-seconds forcing pin 6 high. The printer busy signal will go high until the printer is finished causing a low to high transition at pin 3 of Z16. If this occurs before the nest 0.1 second pulse, Z16 pin 6 will return low and Z13 pin 9 will remain low inhibiting the alarm function. However, if the printer is still busy when the 0.1 second pulse arrives, Z13 pin 9 will be clocked high, enabling Z18 pin 2 which gates a 1.0 Hz signal to a front panel alarm lamp. The lamp will continue to flash at a 1.0 Hz rate until the 0.1 second pulse following either the end of the printer busy signal or a printer reset command from a front panel switch.

The punch alarm function also prevents the issuance of any punch commands while the punch is in operation. The punch busy signal

is normally high but will go low while the punch is operating. Thus when the punch is in operation, Z13 pin 2 will be low. If a 0.1 second pulse arrives at this time, pin 6 will go high enabling Z18 pin 5 and gating a 1.0 Hz signal to the front panel alarm lamp. The lamp will continue to flash until the punch has finished operation or until Z13 pin 6 is forced low by the activation of the PUNCH RESET switch on the DAIU front panel.

Z11 and Z12 provide proper coding of the column 16 printer information. Since the printer only has 18 columns of output capability, some provision must be made to code portions of the output. When two channel operation is selected, the special events will be coded as shown in Appendix A. Column 16 will then print an asterisk (*) to seperate the error outputs from these coded effects. When three channel operation is required, only three columns are available for the channel three error count. Thus whenever 1000 or more errors are counted on this channel, some indication must be made to show a printer overflow. Again column 16 will print an asterisk (*) to indicate a printer overflow. Columns 17 and 18 will print the tens and units digits respectively of the channel 3 error count. To accomplish this, the column 16 print bits are generated by the 4 bit TRUE/COMPLEMENT, ZERO/ONE element Z12. When FUNCTION SELECT is high, Z11 pin 6 is low and pin 8 is high. These levels are applied to the control inputs (pins 1 and 8 respectively) of Z12 and force the output pins (3, 6, 9, and 12) high. With all bits high, the printer causes an asterisk (*) to be printed. This condition corresponds to the two channel operating mode.

When the three channel operating mode is required, FUNCTION SELECT will be low. As long as less than 1000 errors are counted by the channel three error counter, all inputs to Z11 (pins 1, 2, 4, and 5) will be low forcing a high on Z12 pin 1 and a low on pin 8. This control combination gates the hundreds digit bits of the channel three error count to the column 16 printer inputs. However, if 1000 or more errors are counted, Z11 pin 6 will go low forcing all outputs of Z12 high as in the two channel mode. This again results in the printing of an asterisk (*) in column 16 of the printed output. Appendix A shows the complete coding of the printer outputs.

Punch Data Formatting Circuitry

Board PC-12 PUNCH CONTROL LOGIC. The circuitry on this board formats the data to be recorded into ten or eleven characters, each consisting of seven data bits and a parity bit. The schematic for this board is shown in Figure 18 and the parts list is given as Table 12. Z1 through Z6 and Z8 are 16 bit data selectors which gate the inputs selected by address counter Z9 to the punch inputs (PUNCH LEVEL 1-7) and to the input of the parity generator Z10. The output of Z10 appears as PUNCH LEVEL 8.

When data is present to be punched, $\overline{\text{PUNCH}}$ will go low for 100 micro-seconds setting Z7 pin 5 low and pin 6 high. Z7 pin 5 is the PUNCH BUSY signal which appears as an input to the function control logic and also is sent to the punch as a PUNCH COMMAND. As long as the PUNCH COMMAND signal remains low, the punch mechanism will operate punching a frame of data (8 bits) corresponding to the punch levels,

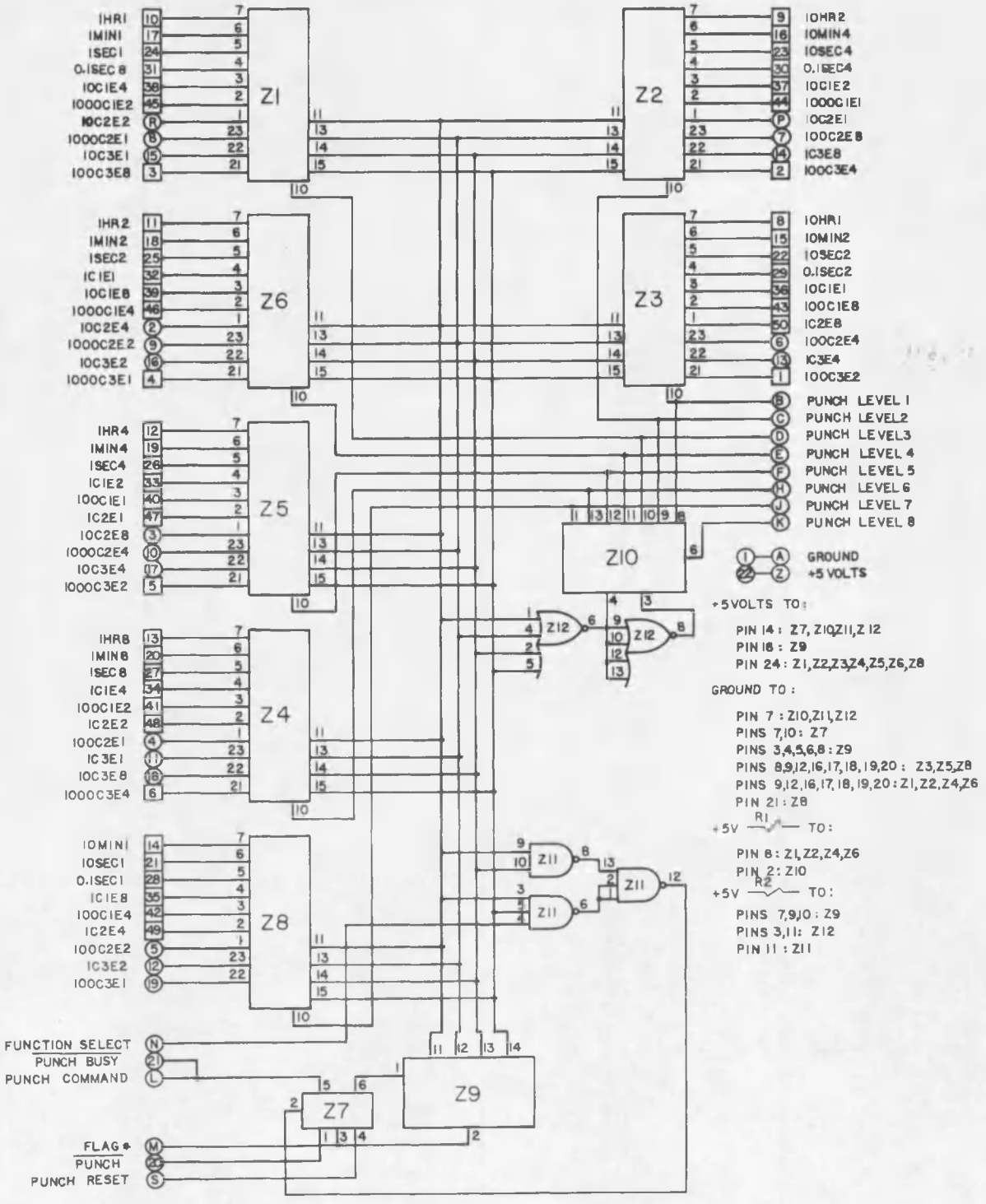

Figure 18. Board PC-12 Punch Control Logic

Table 12. Board PC-12 Parts List

Z1	16 bit data selector/multiplexer	SN74150N
Z2	16 bit data selector/multiplexer	SN74150N
Z3	16 bit data selector/multiplexer	SN74150N
Z4	16 bit data selector/multiplexer	SN74150N
Z5	16 bit data selector/multiplexer	SN74150N
Z6	16 bit data selector/multiplexer	SN74150N
Z7	Dual D flip flop	SN7474N
Z8	16 bit data selector/multiplexer	SN74150N
Z9	Synchronous 4 bit binary counter	SN74161N
Z10	8 bit odd/even parity generator	SN74180N
Z11	Triple 3 input NAND gate	SN7410N
Z12	Dual 4 input NOR gate	SN7425N
R1,R2	1.0 K 1/8 watt resistors, 5%	

advancing the tape, and punching another frame. Each time the punch dice withdraw from the paper tape, a punch flag is generated. This signal is converted to TTL logic levels by Schmitt Trigger Z18 on board DD-7 and appears as FLAG* in the punch control logic. FLAG* is a normally low signal which goes high when the punch dice withdraw from the paper tape.

When Z17 pin 5 goes low, pin 6 goes high enabling address counter Z9. This counter is initially cleared (all zero outputs) which selects the information present on pin 8 of the data selectors to be punched. This information (frame 0) contains a unique identifier which allows the tenth second data interval to be easily determined on the paper tape. As a further identification, this frame is given an even parity by Z10. Whenever the counter outputs are all low, Z12 pin 6 will be high forcing pin 8 low and selecting even parity from Z10. Any high output or combinations of high outputs on Z9 will cause Z12 pin 6 to be low while pin 8 goes high selecting an odd parity generation from Z10.

When the first frame has been punched, FLAG* will pulse high clocking Z9 and transferring the level present on Z7 pin 2 to pin 5. The second frame (frame 1) is now punched and the process continues. Gates Z11 provide address decoding which determines when all of the data has been punched. In two channel operation, FUNCTION SELECT will be high and 63 data bits must be punched. With seven data bits per character (frame) this means that ten frames must be punched (nine for the data plus one for the identifier). Thus Z11 pin 6 will go low

when the tenth frame is punched. When the dice withdraw from the tenth and final frame, FLAG* goes high clocking Z7 pin 6 low and pin 5 high. When pin 5 goes high, further action by the punch is inhibited while the low on pin 6 clears and inhibits counter Z9. This ends the punching of the tenth second data.

If FUNCTION SELECT is low (three channel mode) 69 data bits must be punched. In this case Z11 pin 8 will go low on the eleventh frame and the resetting action described above will again take place.

The punch reset function from the front panel switch will immediately terminate punch action and clear and inhibit counter Z9.

CHAPTER IV

DAIU - DIGITAL RECORDER UNIT

The DAIU - Digital Recorder Unit, shown in Figure 19, was designed to augment the recording capability of the Data Acquisition Interface Unit. The recorder unit records data on a digital magnetic tape cassette in accordance with the formats given in Appendix A. This unit was not included in the initial DAIU design but was added some time after the DAIU was completed. The unit was designed specifically to improve recording reliability and eventually replace the paper tape punch.

The recorder unit itself is self-contained requiring only AC power from the DAIU. The unit mounts between the main DAIU front panel and the monitor and test panel and requires seven inches of front panel space. All data and control signals from the DAIU enter the recorder unit through two "D" type connectors attached to the rear of the cover box.

Detailed Functional Description

The DAIU - Digital Recorder Unit consists of a circuit board, cassette deck, power supplies, and front panel. All components are mounted to the front panel. An aluminum cover box completely encloses the rear of the unit. Complete fabrication details may be found in Appendix D.

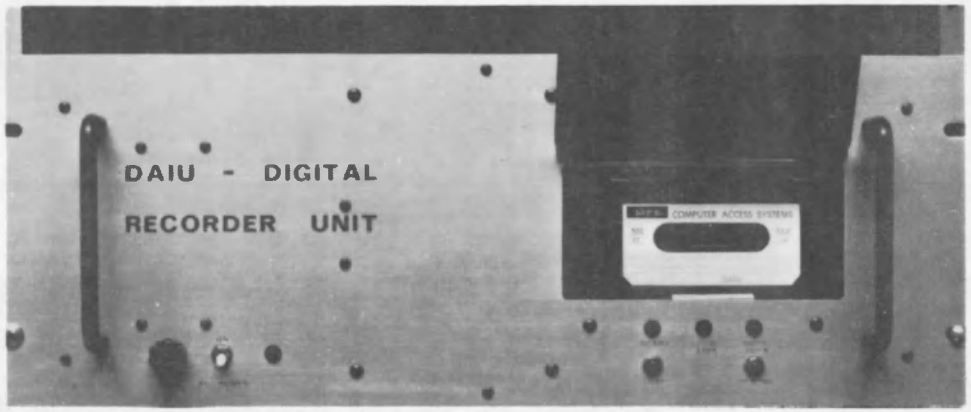

Figure 19. DAIU - Digital Recorder Unit

The schematic for the recorder unit is shown in Figures 20 and 21 and the parts list is given as Table 13. The unit consists essentially of two sub-circuits: Data Storage and Recording, and Motion Control. In this functional description, all package and pin numbers refer to the schematics of Figures 20 and 21. Additional information on the integrated circuits used may be found in [4].

Before the two sub-circuits are described, it is necessary to understand the recording technique used to write data on the magnetic tape. The MFE Corporation Model 250 magnetic tape cassette deck is used in the recorder unit. In this deck, track two of the cassette tape has a pre-recorded clock which provides timing signals used to control the tape speed and recording electronics. A "Bi-Phase Clock" recording scheme is implemented in the recorder unit and provides basically for the recording of one data bit for each three tape clock pulses. Each clock pulse of the three clock "cell" performs a different step in the recording process. The first pulse causes a flux change to be written on the tape. This flux change is required as a timing pulse in the read electronics. Pulse two causes a flux change to be written if and only if the data bit to be recorded is a "1". Pulse three advances the data stream to the next bit position after which the above process is repeated. Complete details of the "Bi- Phase Clock" recording scheme may be found on pages 17, 28, and 29 of [6].

When power is applied to the recorder unit, a power-on-reset function is activated which sets the recorder in a known state. This prevents any tape motion until the REWIND control is activated.

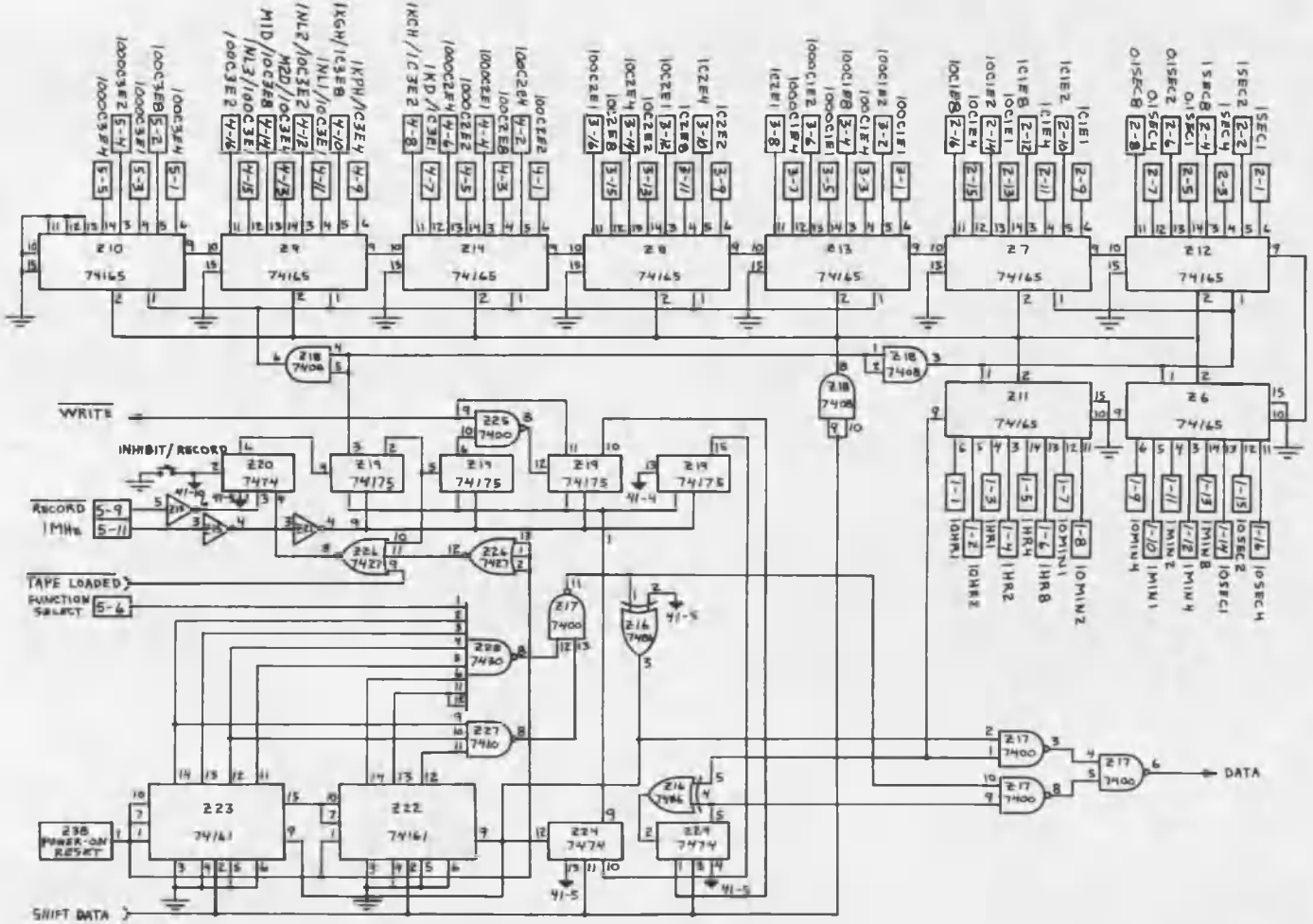

Figure 20. Data Storage and Recording

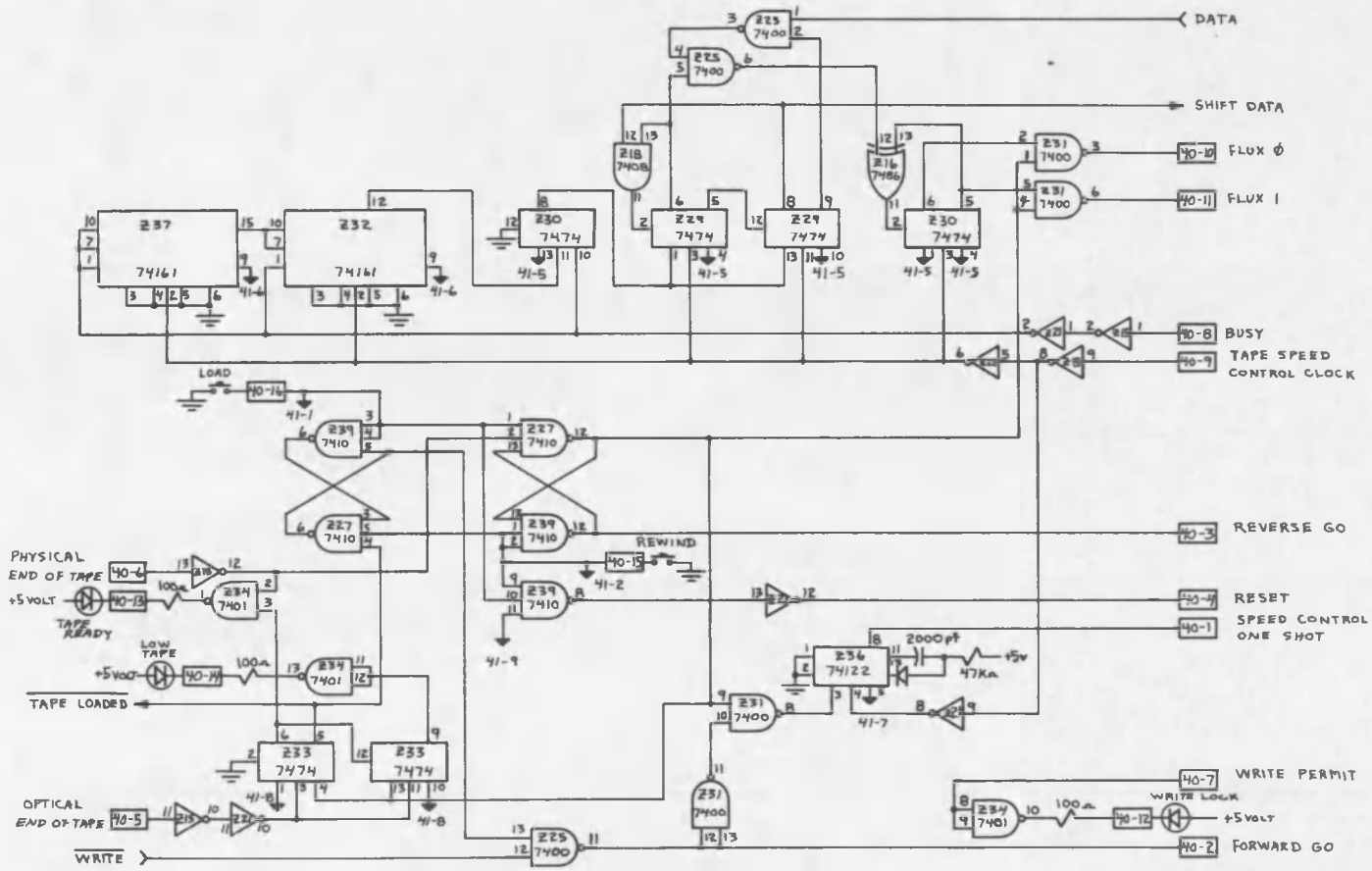

Figure 21. Motion Control

Table 13. DAIU - Digital Recorder Unit Parts List

Z1	Input cable connector	3M Co. #	3416-1
Z2	Input cable connector	3M Co. #	3416-1
Z3	Input cable connector	3M Co. #	3416-1
Z4	Input cable connector	3M Co. #	3416-1
Z5	Input cable connector	3M Co. #	3416-1
Z6	Parallel load 8 bit shift register		SN74165N
Z7	Parallel load 8 bit shift register		SN74165N
Z8	Parallel load 8 bit shift register		SN74165N
Z9	Parallel load 8 bit shift register		SN74165N
Z10	Parallel load 8 bit shift register		SN74165N
Z11	Parallel load 8 bit shift register		SN74165N
Z12	Parallel load 8 bit shift register		SN74165N
Z14	Parallel load 8 bit shift register		SN74165N
Z15	Hex Schmitt Trigger		SN7414N
Z16	Quad EXCLUSIVE OR gate		SN7486N
Z17	Quad 2 input NAND gate		SN7400N
Z18	Quad 2 input AND gate		SN7408N
Z19	Quad D register		SN74175N
Z20	Dual D flip flop		SN7474N
Z21	Hex inverter		SN7404N
Z22	Synchronous 4 bit binary counter		SN74161N
Z23	Synchronous 4 bit binary counter		SN74161N
Z24	Dual D flip flop		SN7474N
Z25	Quad 2 input NAND gate		SN7400N
Z26	Triple 3 input NOR gate		SN7427N
Z27	Triple 3 input NAND gate		SN7410N
Z28	8 input NAND gate		SN7430N
Z29	Dual D flip flop		SN7474N
Z30	Dual D flip flop		SN7474N
Z31	Quad 2 input NAND gate		SN7400N
Z32	Synchronous 4 bit binary counter		SN74161N
Z33	Dual D flip flop		SN7474N
Z34	Quad 2 input NAND gate with open collector		SN7401N
Z35	Timing circuit		
Z36	Retriggerable monostable multivibrator		SN74122N
Z37	Synchronous 4 bit binary counter		SN74161N
Z38	Power-on-reset module		
Z39	Triple 3 input NAND gate		SN7410N
Z40	Input/output connector	3M Co. #	3416-1
Z41	16 pin resistor pull-up network	Beckman #	898-1-R1.5K

Gates Z39 and Z27, output pins 12, form the rewind flip flop. When the REWIND control is activated, Z39 pins 1 and 2 are momentarily grounded, forcing the output to go high. When pin 12 of Z39 goes high, a reverse go command is applied to the cassette deck electronics causing the tape to rewind. At the same time, Z27 pin 12 goes low maintaining the reverse go command, resetting Z33, and inhibiting the outputs of gates Z31 pins 3 and 6. This prevents erasure of the tape during the rewind process. Z33 controls the tape status lamps on the front panel and "locks out" any record command by inhibiting flip flop Z20 until the tape has been loaded.

When the tape has been completely rewound, the PHYSICAL END OF TAPE input will go high, clearing the rewind flip flop and enabling the head flux through Z31. Momentarily depressing the LOAD TAPE switch forces Z39 pin 6 high which in turn causes Z27 pin 6 to go low. This level is applied to Z25 pin 13 and results in a high at output pin 11 of Z25. This is a forward go command applied to the cassette deck electronics and causes the tape to advance to the optical beginning of tape mark. When this point is reached a pulse occurs on the OPTICAL END OF TAPE line which will clock flip flop Z33 pin 5 low. This in turn resets and inhibits the load flip flop, stopping the forward tape motion. When Z33 pin 5 goes low, Z20 is enabled and pin 6 will go high lighting the TAPE READY lamp by forcing a low at output pin 1 of Z34. The unit is now ready to record and waits in this state until a record command is issued by the DAIU.

Devices Z6 through Z14 comprise a sixty-nine bit parallel in/serial out shift register. When a record command ($\overline{\text{RECORD}}$) is issued by the DAIU, the record timing sequence shown in Figure 22 is generated by Z19 and Z20. The record command clocks Z20 pin 6 high enabling Z19 pin 4. Z19 is clocked on the rising edge of the 1.0 MHz signal forcing pin 3 low and pin 2 high. When pin 2 goes high, a low is applied to Z20 pin 4 forcing pin 6 to return low. At the leading edge of the 1.0 MHz clock, Z19 pin 3 returns high and pin 6 goes low enabling pin 12. A forward go command will be issued as the next leading edge of the 1.0 MHz clock forces pin 11 low and pin 10 high. A high on pin 10 enables the parity generator Z16, Z24 which generates an even parity bit over all of the data bits recorded. Data is loaded into the shift register while Z19 pin 3 is low. When this line returns high, the data is latched in the register. Changes in the input data will have no effect until the next load pulse occurs (low on Z19 pin 3).

The record timing sequence may be summarized by the following list. The indicated actions occur at one micro-second intervals.

1. Load data into shift register
2. Initiate write sequence
3. Start tape forward and enable parity generator

When the last data bit (parity) is recorded, a clear pulse resets Z19.

Data is shifted out of the register by shift data pulses generated in the flux control logic explained below. Bit counter Z22, Z23 counts the number of bits recorded. If the DAIU output FUNCTION

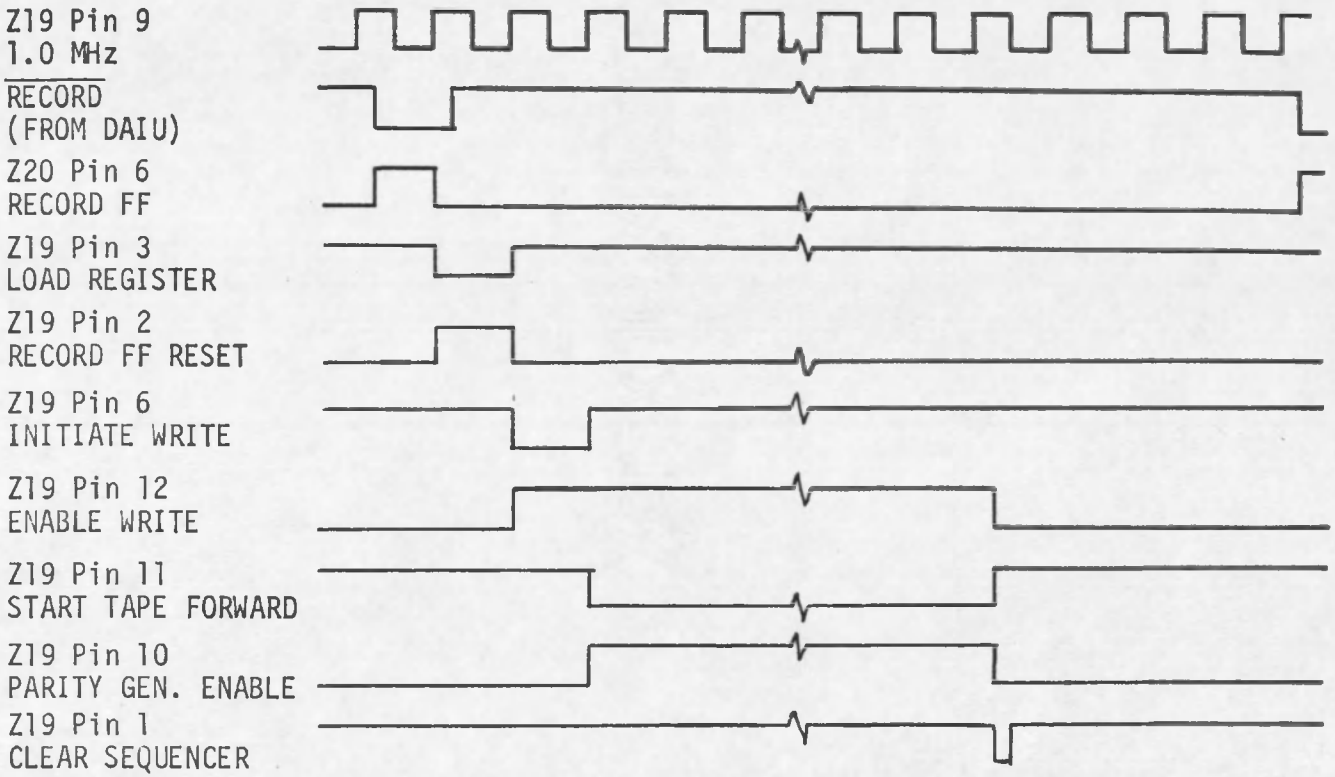

Figure 22. Timing Diagram of Record Command Sequencer

SELECT is high, sixty-three data bits will be recorded. A low on this line results in the recording of sixty-nine data bits.

Z17 pin 11 will be low while the data is being recorded. This forces Z16 pin 3 high which gates the data from the shift register Z11 pin 9 to the DATA line through gates Z17 putputs 3 and 6. When the last data bit is recorded, Z17 pin 11 will go high forcing Z16 pin 3 low. This gates the parity bit Z24 pin 5, onto the DATA line. At the same time this forces pin 9 of Z23 and Z22 (synchronous load input) and pin 12 of Z24 low. Thus, when the parity bit is recorded on the next SHIFT DATA pulse, the counter will be reset to zero and Z24 pin 9 will go low. This in turn resets pin 9 of Z24 high enabling Z19. Finally, the first 1.0 MHz clock pulse following the enabling of Z19 clocks pin 15 high enabling Z24.

The data to be recorded, including parity, enters the flux control circuitry at Z25 pin 1 in serial form. The operation of this circuitry may be explained with the aid of Figure 23. When a forward go command has been issued as a result of a record command from the DAIU, the BUSY line (Z21 pin 2) will go high. This enables the "speed" counter Z37, Z32 to count the TAPE SPEED CONTROL CLOCKS which are pre-recorded on the magnetic tape. After sixty-four pulses have been counted, the tape is assumed to be moving fast enough to allow recording of data. At this point, Z30 pin 8 goes high enabling Z29. Pulses A and B are generated as shown in figure 23. Each rising edge of Pulse A causes a flux change to be recorded on the tape. The rising edge of Pulse B causes a flux change only if the DATA line is high. Pulse B is also

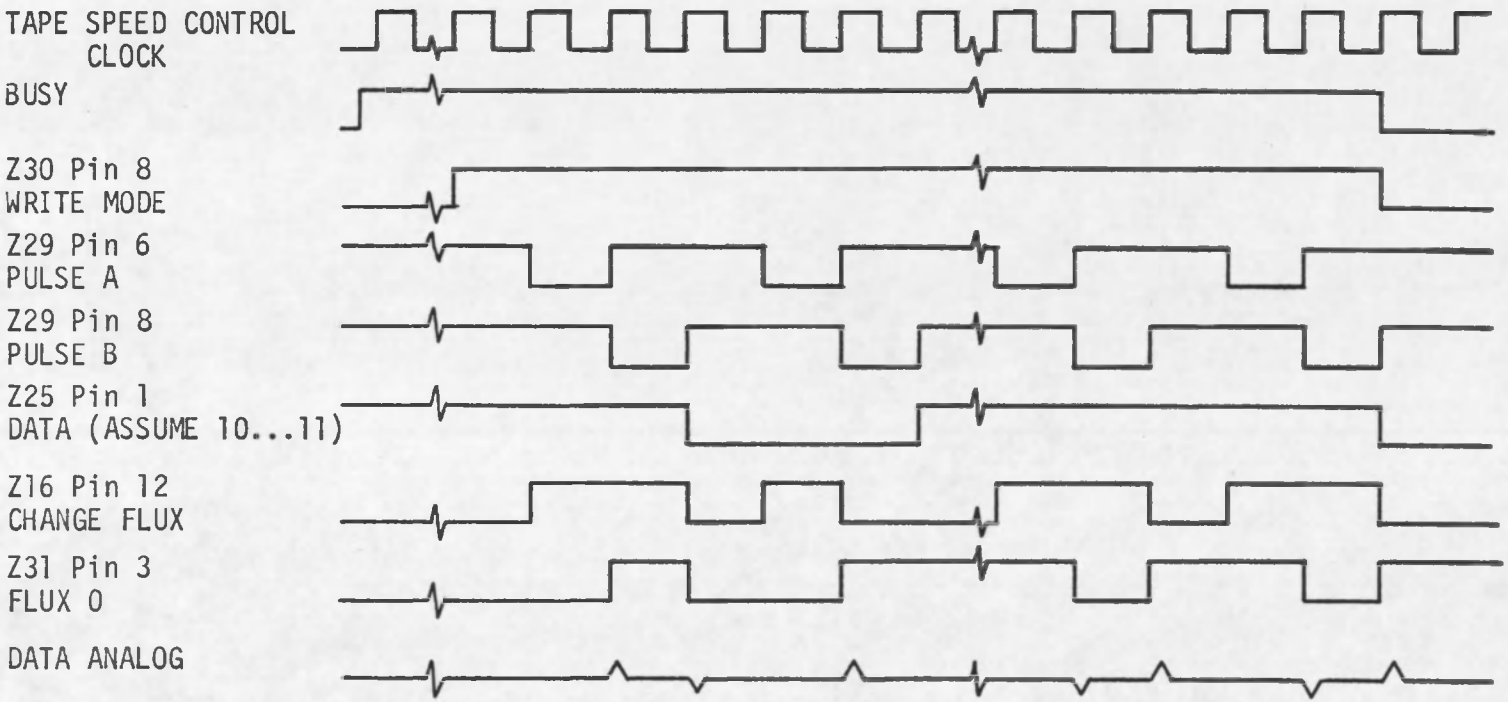

Figure 23. Flux Control Circuitry

used to shift the data out of the shift register. Thus the data is recorded and shifted by the same pulse. Figure 23 shows the recording of the data bits 10...11. When the last bit is recorded (corresponding to the parity bit) the forward go command is removed forcing the BUSY signal low. This immediately forces Pulse A and Pulse B high preventing any further flux changes and at the same time clears the "speed" counter Z37, Z32. Thus, another sixty-four TAPE SPEED CONTROL CLOCKS must be counted before data from the next sample period may be recorded.

The INHIBIT/RECORD switch function enables the recording process to be inhibited at the end of any tenth second interval during which it is activated. The function simply forces Z20 pin 2 high which causes pin 6 to be clocked low by the next $\overline{\text{RECORD}}$ pulse. But pin 6 is already low and must go high before the recording sequence may be initiated.

When the switch is in the RECORD position, Z20 pin 2 will be grounded and pin 6 will be clocked high by $\overline{\text{RECORD}}$ as desired. This function is included to enable the cassette to be changed at any point. It ensures that the cassette will not be in motion. Removal of the cassette while the tape is in motion will result in excessive head wear.

CHAPTER V

OPERATIONAL CHECKOUT

Before the operational checkout is performed, all internal and external connections must be made to the DAIU. All cables attached to the DAIU connector block assembly should be checked for proper connection. External recording equipment should also be properly connected.

The following tests should be performed to ensure system operability:

- Digital clock preset test
- Modem Clock alarm Test
- Print/punch test

During these tests, the DAIU should be configured for three channel operation.

Apply power to the DAIU by pressing the POWER switch on the main display panel. When the unit is in operation, this switch should indicate a red color. In addition, the lamps indicating the presence of the ±12 and +5 voltages on the Monitor and Test Panel should light. If these lamps fail to light, the main power switch should immediately be turned off and the cause of the failure of these lamps to light should be determined and corrected before further testing is attempted. Apply power to the DAIU - Digital Recorder Unit and note that the AC power indicator lamp lights.

The digital clock preset test consists of setting the digital clock to the desired time (normally local time). In normal operation, the CLOCK switch will indicate a green color with the legend PRESS TO SET. This switch is protected by a guard which must be lifted in order to operate the switch. When the guard is lifted and the switch is depressed, the green light will extinguish and a red light with the legend PRESS TO RUN will light. In this configuration, the clock will accept inputs from the CLOCK PRESET switches located directly below the clock display. The desired time may now be set on these switches. When the CLOCK switch is again depressed, the green light will return and the digital clock should run normally.

The modem clock alarm test is performed with the DAIU in normal operation. When a modem clock is not detected by the DAIU, the corresponding channel clock alarm lamp should flash at a 1 Hz rate. When the modem clock is re-applied, the clock alarm lamp should extinguish. This test should be performed on each channel by disconnecting their respective modem input cables.

The print/punch test may be combined with the clock preset test in the following manner. With the printer and punch both off, preset the clock to 00:40:00 and depress both PRINTER and PUNCH RESET switches on the Monitor and Test Panel. Both PRINTER ALARM and PUNCH ALARM lamps should remain off. When the clock has advanced to 00:50:00, the PUNCH ALARM lamp should begin to flash at a 1 Hz rate. Depressing the PUNCH RESET switch should cause the PUNCH ALARM lamp to extinguish. At 01:00:00 both the PRINTER ALARM and PUNCH ALARM lamps should flash at

a 1.0 Hz rate. Depressing both the PRINTER and PUNCH RESET switches should cause both alarm lamps to extinguish.

The above test should be repeated with the printer and punch turned on. The alarm lamps should now remain off. A punch should occur at 00:50:00 while both a print and punch should occur at 01:00:00. The digital recorder unit should not record at any time during this test. Complete operating instructions may be found in Section 3 of [1] and [2].

APPENDIX A

DATA COLLECTION AND FORMATS

The Data Acquisition Interface Unit was designed to output collected data on a paper tape punch, printer, and magnetic tape cassette recorder. In two channel operation, the transfer of data to these output devices is initiated by the DAIU after any of the following events have occurred:

- Channel 1 error
- Channel 2 error
- 1 KHz Dropout
- 1 KHz Phase Hit
- 1 KHz Gain Hit
- 1 KHz Coincidence Hit
- Impulse noise levels 1, 2, or 3
- Modem 1 dropout
- Modem 2 dropout

For three channel operation, the detection of an error on any channel will initiate transfer of data to these external recording devices.

Printer Output

The printer used in the DAIU provides eighteen columns of output. In two channel and three channel operation, the digital clock, channel 1 errors, and channel 2 errors require fifteen of these columns.

This leaves only three columns for the special events (in two channel operation) and the channel three error count (in the three channel mode). Thus, three columns of output are available to record any combination of occurrences of the nine special events or an error count of up to 5000. To overcome this limitation, the printer data was formatted as shown in Table 14.

The information printed in columns 17 and 18 in the two channel mode has been named Coded Multiple Effects 1 and 2 respectively. These two columns contain the special events information which has been encoded using all sixteen characters available on the printer symbol wheel. Table 15 shows the coding used and the BCD levels required at the printer inputs. These levels correspond to the Hewlitt-Packard +8421 code terminology (H=high or on and L=low or off). The following list shows the abbreviations used in this table.

Coded Multiple Effects 1 and 2	CME1 and 2
1 KHz Dropout	1KD
1 KHz Phase Hit	1KPH
1 KHz Gain Hit	1KGH
1 KHz Coincidence Hit	1KCH
Modem 1 Dropout	M1D
Modem 2 Dropout	M2D
Impulse Noise Levels 1, 2, and 3	INL1, INL2, and INL3

In the resulting printer output, the impulse noise level indicated will correspond only to the highest level encountered.

Table 14. Printer Formats

Two Channel		Three Channel	
Output Column	Information Printed	Output Column	Information Printed
1-7	Digital Clock Time	1-7	Digital Clock Time
8-11	Channel 1 Errors	8-11	Channel 1 Errors
12-15	Channel 2 Errors	12-15	Channel 2 Errors
16	Asterisk (*)	16-18	Channel 3 Errors (For counts greater than 999 column 16 will print an asterisk (*) indicating a printer overflow.)
17	Coded Multiple Effects 1		
18	Coded Multiple Effects 2		

Table 15. Coded Multiple Effects

Symbol Printed	CME1 (Col. 17)	CME2 (Col. 18)	BCD Levels 8 4 2 1
0	NONE	NONE	L L L L
1	INL1	1KD	L L L H
2	INL2	1KCH	L L H L
3	INL3	1KCH,1KPH	L L H H
4	M2D	1KPH	L H L L
5	M2D,INL1	1KPH,1KD	L H L H
6	M2D,INL2	1KPH,1KCH	L H H L
7	M2D,INL3	1KPH,1KCH,1KD	L H H H
8	M1D	1KGH	H L L L
9	M1D,INL1	1KGH,1KD	H L L H
+	M1D,INL2	1KGH,1KCH	H L H L
-	M1D,INL3	1KGH,1KCH,1KD	H L H H
V	M1D,M2D	1KGH,1KPH	H H L L
A	M1D,M2D,INL1	1KGH,1KPH,1KD	H H L H
Ω	M1D,M2D,INL2	1KGH,1KPH,LKCH	H H H L
*	M1D,M2D,INL3	1KGH,1KPH,1KCH,1KD	H H H H

Punch Output

The punch output may be considered as a two dimensional array in which eight rows (levels) and ten columns (frames) are available for two channel operation. In three channel operation, an additional frame is available to accomidate the added data. For either mode of operation, level eight is reserved for an odd parity bit for all but the first frame. The first frame is a unique identifier (punch levels 2, 3, 4, and 6) coded in even parity and is used for software locational purposes. The punch format is shown in Table 16.

As an example of the paper tape output, consider the following information gathered in a tenth second sample interval (two channel operation).

Time	23:59:59.9
Channel 1 Errors	1920
Channel 2 Errors	480
Modem 1 Dropout	YES
Modem 2 Dropout	YES
1 KHz Phase Hit	YES
1 KHz Coincidence Hit	YES
Impulse Noise Level 3	YES

Figure 24 shows a section of tape produced by the punch for the above data.

Magnetic Tape Cassette Output

The DAIU - Digital Recorder Unit records the collected data in serial form (one bit at a time) on a magnetic tape cassette. A

Table 16. Punch Formats

Frame	Level	Data Punched	
1	1-7	Unique Identifier	
2	1	10HR1	Ten hour digit of
2	2	10HR2	clock time
2	3	1HR1	
2	4	1HR2	One hour digit of
2	5	1HR4	clock time
2	6	1HR8	
2	7	10MIN1	
3	1	10MIN2	Ten minute digit of
3	2	10MIN4	clock time
3	3	1MIN1	
3	4	1MIN2	One minute digit of
3	5	1MIN4	clock time
3	6	1MIN8	
3	7	10SEC1	
4	1	10SEC2	Ten second digit of
4	2	10SEC4	clock time
4	3	1SEC1	
4	4	1SEC2	One second digit of
4	5	1SEC4	clock time
4	6	1SEC8	
4	7	0.1SEC1	
5	1	0.1SEC2	Tenth second digit of
5	2	0.1SEC4	clock time
5	3	0.1SEC8	
5	4	1C1E1	
5	5	1C1E2	Units digit of
5	6	1C1E4	Channel 1 Errors
5	7	1C1E8	
6	1	10C1E1	
6	2	10C1E2	Tens digit of
6	3	10C1E4	Channel 1 Errors
6	4	10C1E8	

Table 16 continued

Frame	Level	Data Punched	
6	5	100C1E1	
6	6	100C1E2	Hundreds digit of
6	7	100C1E4	Channel 1 Errors
7	1	100C1E8	
7	2	1000C1E1	Thousands digit of
7	3	1000C1E2	Channel 1 Errors
7	4	1000C1E4	
7	5	1C2E1	
7	6	1C2E2	Units digit of
7	7	1C2E4	Channel 2 Errors
8	1	1C2E8	
8	2	10C2E1	
8	3	10C2E2	Tens digit of
8	4	10C2E4	Channel 2 Errors
8	5	10C2E8	
8	6	100C2E1	
8	7	100C2E2	Hundreds digit of
9	1	100C2E4	Channel 2 Errors
9	2	100C2E8	
9	3	1000C2E1	Thousands digit of
9	4	1000C2E2	Channel 2 Errors
9	5	1000C2E4	
		FOR TWO CHANNEL OPERATION	
9	6	1KD	
9	7	1KCH	
10	1	1KPH	
10	2	1KGH	
10	3	INL1	
10	4	INL2	
10	5	M2D	
10	6	M1D	
10	7	INL3	

Table 16 continued

FOR THREE CHANNEL OPERATION

Frame	Level	Data Punched	
9	6	1C3E1	
9	7	1C3E2	Units digit of
10	1	1C3E4	Channel 3 Errors
10	2	1C3E8	
10	3	10C3E1	
10	4	10C3E2	Tens digit of
10	5	10C3E4	Channel 3 Errors
10	6	10C3E8	
10	7	100C3E1	
11	1	100C3E2	Hundreds digit of
11	2	100C3E4	Channel 3 Errors
11	3	100C3E8	
11	4	1000C3E1	Thousands digit of
11	5	1000C3E2	Channel 3 Errors
11	6	1000C3E4	

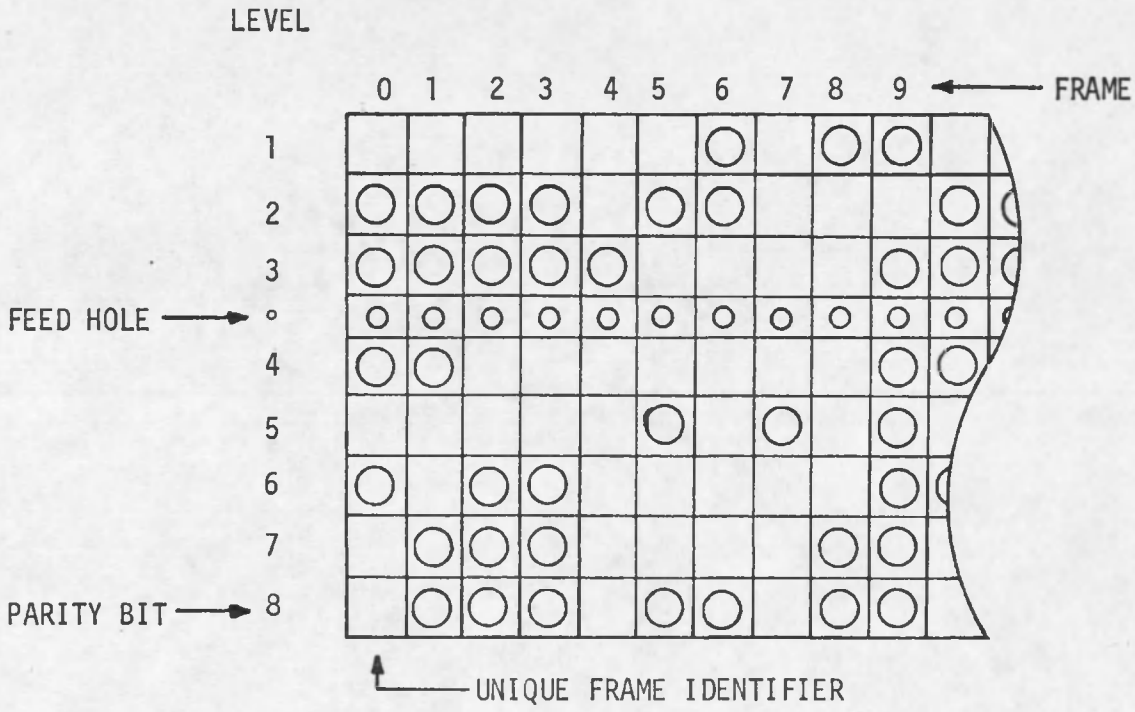

Figure 24. Sample Punched Paper Tape Output

single parity bit is generated and recorded to provide even parity over each tenth second data sample. Including this parity bit, sixty-four bits are recorded for two channel operation while seventy bits are recorded in the three channel mode for each tenth second sample interval. Table 17 shows the order in which the bits are written onto the tape.

Table 17. Magnetic Tape Formats

Bit Position	Information	Bit Position	Information
1	10HR1	44	10C2E1
2	10HR2	45	10C2E2
3	1HR1	46	10C2E4
4	1HR2	47	10C2E8
5	1HR4	48	100C2E1
6	1HR8	49	100C2E2
7	10MIN1	50	100C2E4
8	10MIN2	51	100C2E8
9	10MIN4	52	1000C2E1
10	1MIN1	53	1000C2E2
11	1MIN2	54	1000C2E4
12	1MIN4		
13	1MIN8	TWO CHANNEL OPERATION	
14	10SEC1		
15	10SEC2	55	1KD
16	10SEC4	56	1KCH
17	1SEC1	57	1KPH
18	1SEC2	58	1KGH
19	1SEC4	59	INL1
20	1SEC8	60	INL2
21	0.1SEC1	61	M2D
22	0.1SEC2	62	M1D
23	0.1SEC4	63	INL3
24	0.1SEC8	64	PARITY
25	1C1E1		
26	1C1E2	THREE CHANNEL OPERATION	
27	1C1E4		
28	1C1E8	55	1C3E1
29	10C1E1	56	1C3E2
30	10C1E2	57	1C3E4
31	10C1E4	58	1C3E8
32	10C1E8	59	10C3E1
33	100C1E1	60	10C3E2
34	100C1E2	61	10C3E4
35	100C1E4	62	10C3E8
36	100C1E8	63	100C3E1
37	1000C1E1	64	100C3E2
38	1000C1E2	65	100C3E4
39	1000C1E4	66	100C3E8
40	1C2E1	67	1000C3E1
41	1C2E2	68	1000C3E2
42	1C2E4	69	1000C3E4
43	1C2E8	70	PARITY

APPENDIX B

EVOLUTION OF FABRICATION TECHNIQUES

Several improvements in fabrication techniques were made during the interval between the construction of the Data Acquisition Interface Unit and the DAIU - Digital Recorder Unit. These changes involved new selections of circuit boards, new interconnection techniques and the use of sockets to eliminate soldering of the integrated circuits. These changes are fully described in the sections below.

Circuit Boards

In the Data Acquisition Interface Unit, fourteen circuit boards are used. Each of these boards can hold as many as twenty 14 or 16 pin dual in-line package (DIP) integrated circuits. Figure 25 shows a typical circuit board of the DAIU while Figure 26 shows the wiring side of the board. This fabrication technique involves soldering the integrated circuits onto pads provided on the boards and then soldering the interconnections on the reverse side of the board. Discrete pull-up resistors are used to provide logical high levels to selected circuit inputs. Other discrete circuits are built on these boards when required wherever space is available.

Several disadvantages are inherent in this type of construction. Since only twenty integrated circuits can be placed on any one board, the resulting functions generated require on optimal use of these

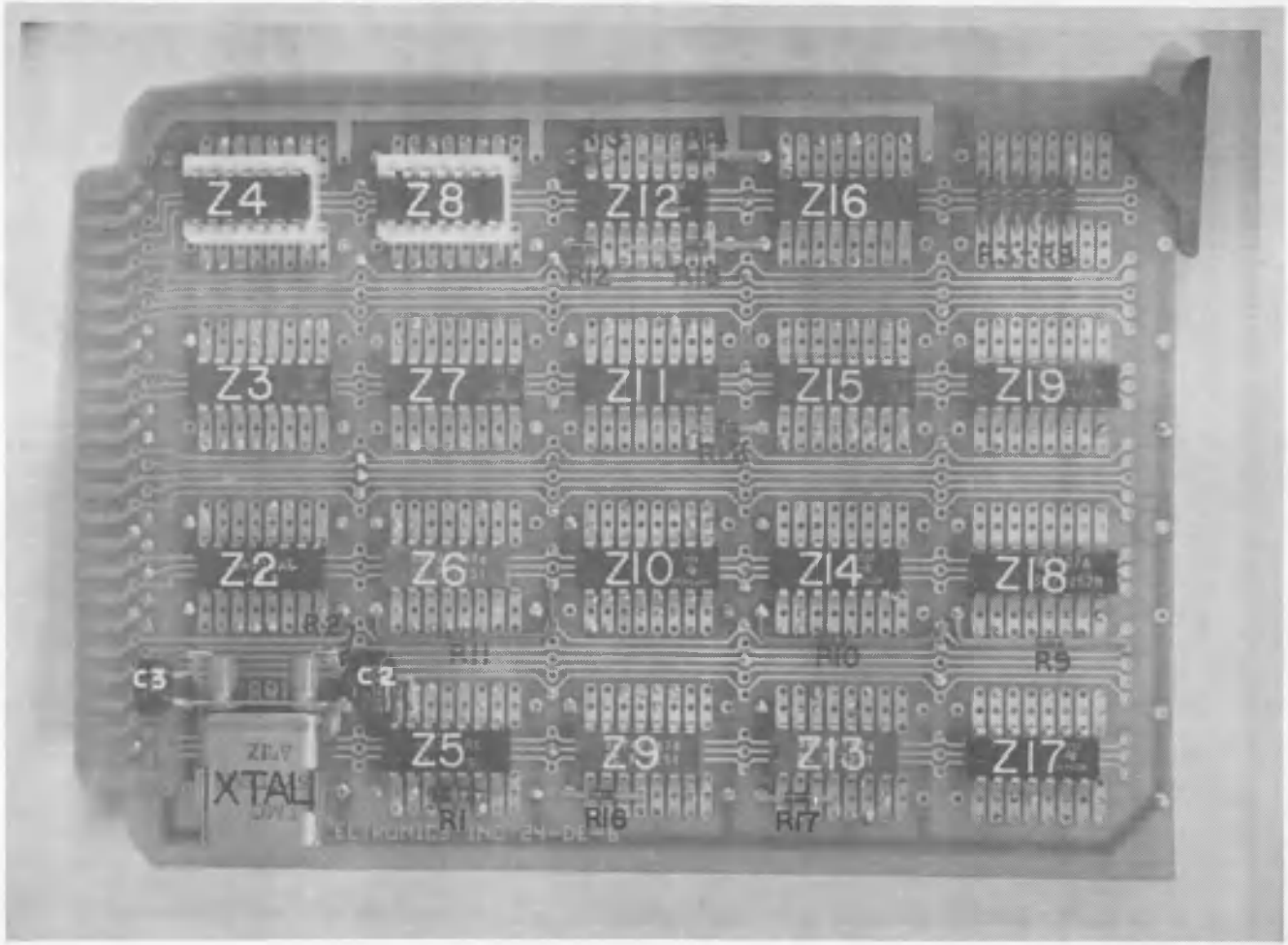

Figure 25. Illustration of a Typical DAIU Circuit Board (Component Side)

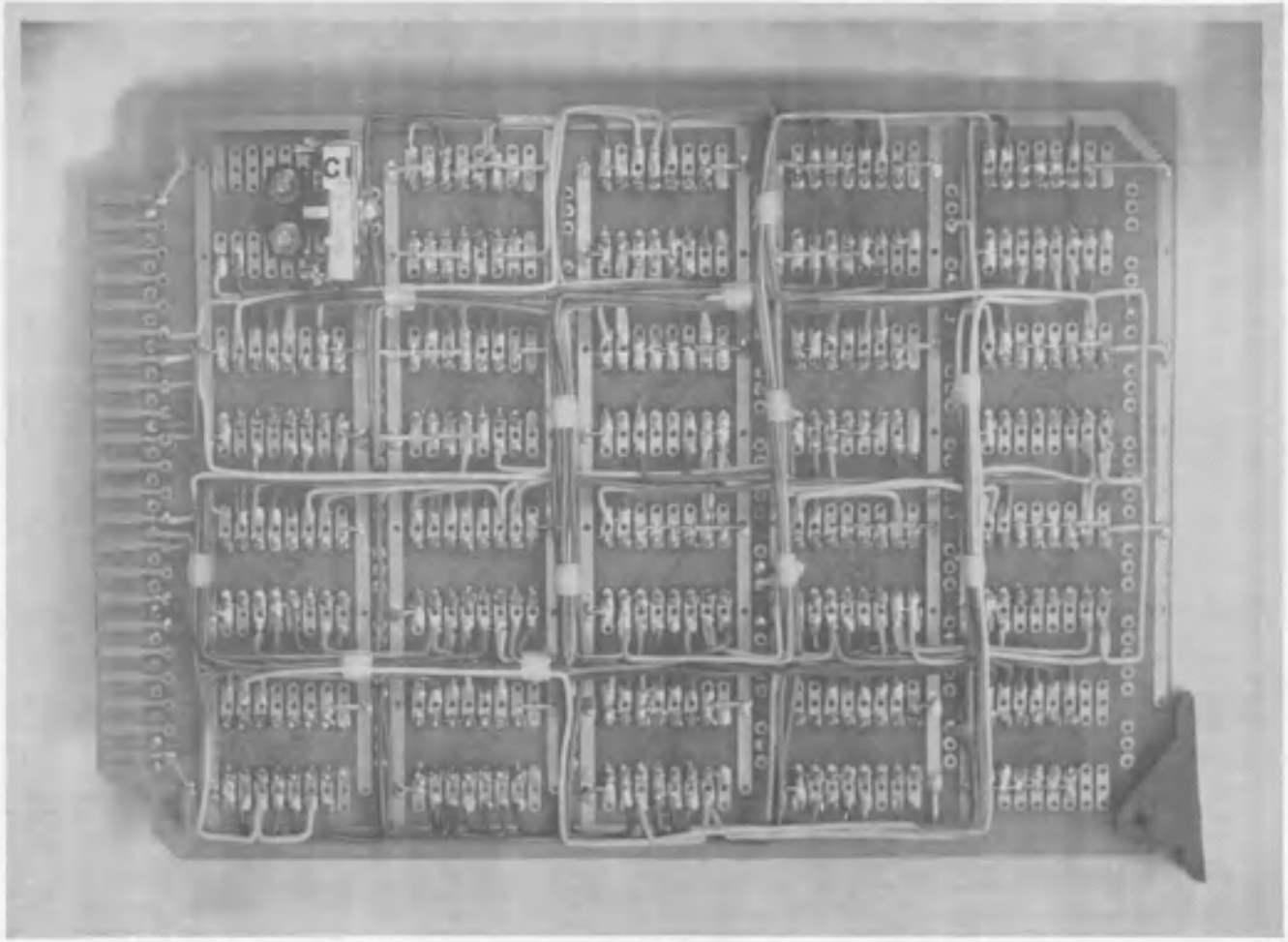

Figure 26. Illustration of a Typical DAIU Circuit Board (Wiring Side)

circuits in many cases. This in turn makes circuit or functional modifications difficult and sometimes impossible as little or no space is available for additional circuitry.

Since the functions generated on such a circuit board are somewhat limited, functions generated on other boards must provide inputs and therefore interconnections between the boards must be made. The boards used in the DAIU provide 44 pins for interconnections between boards. The interconnections are made between card edge connectors in a card rack as shown in Figure 27. Each circuit board then plugs into these edge connectors to complete the circuit. Wiring errors can then be made both on the circuit board and in the rack wiring (inter-board connections).

To overcome all of these disadvantages, the logical circuitry of the DAIU - Digital Recorder Unit was constructed on a single circuit board. This eliminated board interconnections and allowed more complex functions to be generated. Soldering of the integrated circuits was eliminated by the use of sockets on the board. All interconnections between integrated circuits were made by using wire wrap techniques also requiring no soldering.

The board used in the DAIU - Digital Recorder Unit is approximately half the size of any DAIU board yet contains twice the number of integrated circuits. The board is constructed from an epoxy-fiberglass board one sixteenth of an inch thick. Metal bus strips are attached to the board with wire wrap stakes to provide power and ground connections to the integrated circuits. Wire wrap DIP sockets of the

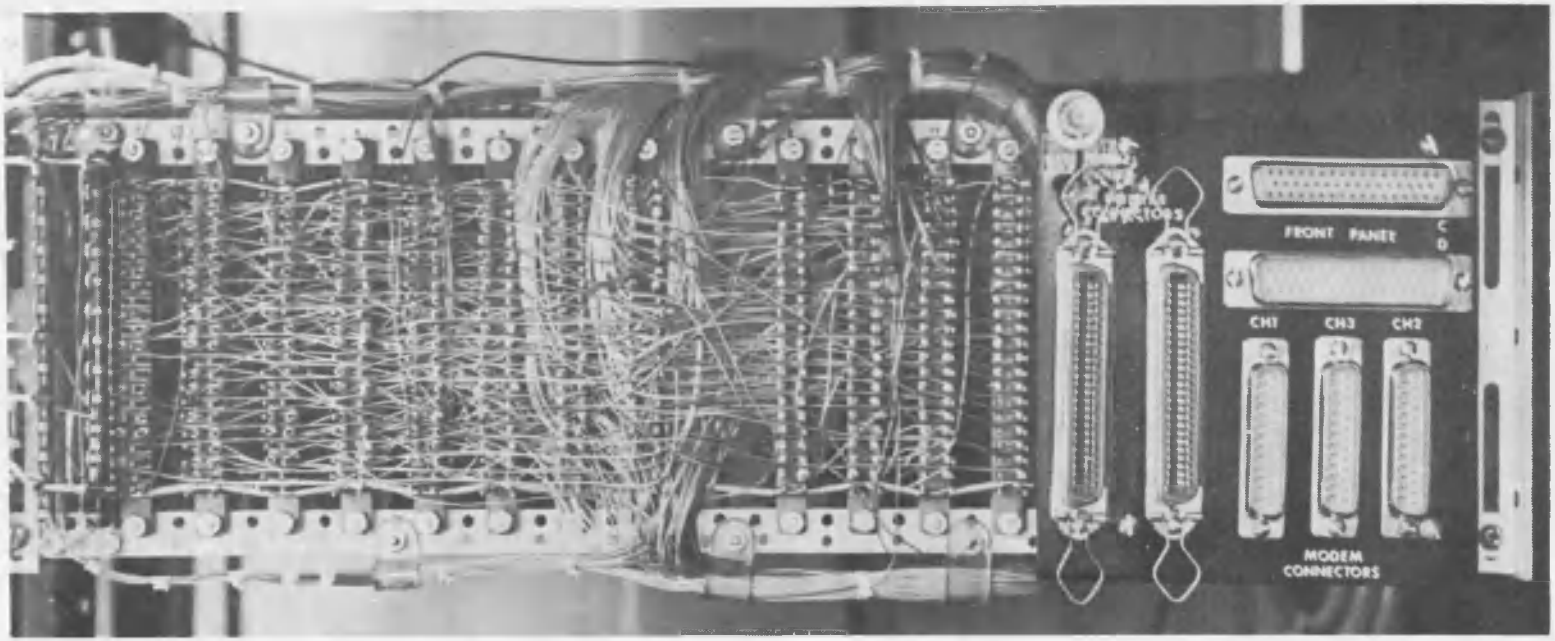

Figure 27. Rear View of DAIU Card Rack Showing Interconnections Between Edge Card Connectors

appropriate size are then inserted into the board where required and a one sixteenth inch layer of liquid fiberglass is poured onto the wiring side of the board. After this fiberglass has hardened, it firmly holds the sockets in place and the board is ready to be wire wrapped. Circuit modifications are easily made by merely unwrapping the unwanted connection and rewrapping. No soldering is required. Figure 28 shows the recorder board constructed as above.

Interconnection Techniques

As stated above, all interconnections between integrated circuits in the recorder unit are made by wire wrap as opposed to the soldering method used in the DAIU. Interconnections between circuit boards and front panel have also been improved.

In the DAIU, two fifty pin D type connectors are provided at the rear of the card rack to interconnect this rack with the front panel. A cable originating at and soldered to terminal strips on the front panel connects to these connectors. This cable is sensitive to movement and broken wires may easily occur inside it.

In the recorder unit, the circuit board is mounted to the rear of the front panel and all interconnections between it and the outside world are made by way of sixteen pin DIP plugs which mate with standard sisteen pin integrated circuit sockets. Thus, these interconnections are shorter than those in the DAIU and can be made with a more flexible wire.

The entire circuitry of the recorder unit is contained within an aluminum chassis box as oppossed to being left open as in the DAIU.

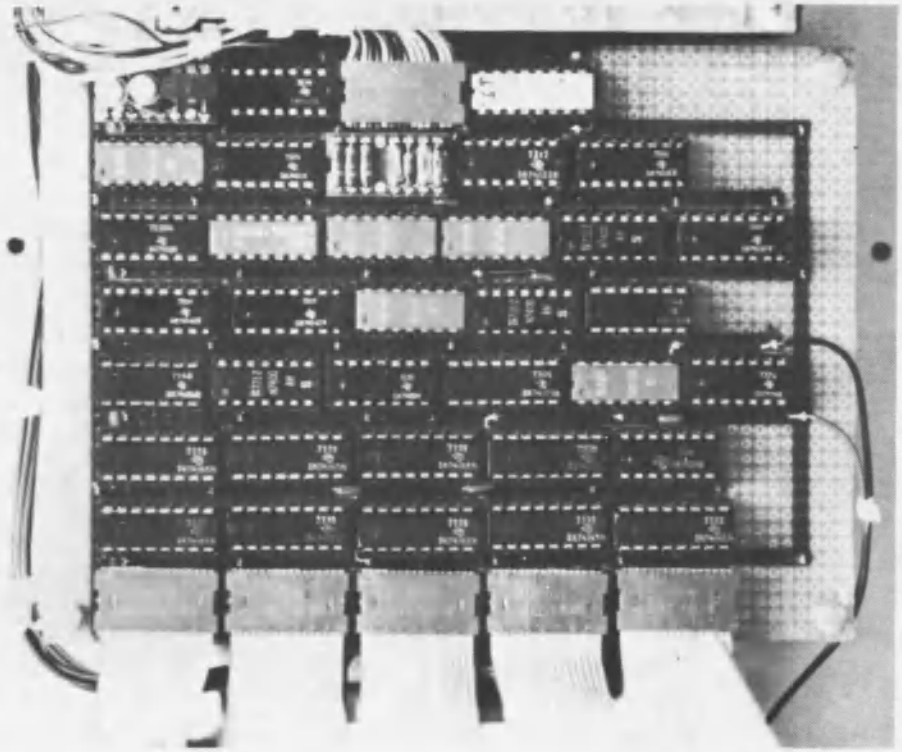

Figure 28. Circuit Board of the DAIU - Digital Recorder Unit

This construction technique prevents accidental damage to the unit and hinders unauthorized access to the circuitry.

Component Selection

The logic family used in the DAIU is the same as that employed in the recorder unit. The noticable change in components involves the use of resistor pull-up networks to provide logical high levels. Each of these resistor networks in a 16 or 14 pin DIP contains fifteen or thirteen pull-up resistors respectively. Use of these resistor networks eliminates the need for discrete pull-up resistors, saves board space, and reduces the interconnections required.

All discrete circuits in the recorder unit are constructed on 16 pin interfacing plugs which also plug into the 16 pin DIP sockets. These interfacing plugs allow for a quick change in circuit functions simply by replacing one discrete circuit with another. No desoldering is required as with some discrete circuits in the DAIU.

Circuit Performance

Both fabrication techniques provide adaquate circuit performance. The difficulty involved in initially obtaining the desired performance is probably greater for the DAIU method. Each circuit board must be probed to trace a signal,possibly requiring the removal and reinsertion of several boards. Both board wiring and card rack wiring must be checked. In the recorder unit, initial operation is easier to achieve since all of the circuitry is on a single board and is therefore readily available. As only one board is used no inter-board connections are encountered.

After each unit is operating correctly, maintenance and repair is easier with the card rack approach than the single board unit. This is because a faulty circuit in the DAIU may be quickly found by merely substituting spare boards until the unit again functions correctly. This pinpoints the immediate location of any malfunction.

The recorder unit on the other hand, will again require complete testing as it cannot be broken down into seperate subcircuits. With the low failure rates experienced with these circuits, the techniques offering the easiest fabrication procedures provides a better overall unit.

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