DISPLAY OF DIGITALLY PROCESSED DATA

by

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John R Featherston — 5 MAY 1959

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CHAPTER 1

INTRODUCTION

An important component in the communication of information to the user of a digital computer is the output equipment. Often the speed at which data is obtained is limited by this equipment. In addition, the nature of the data at the output may not be in a form which is readily analyzed and interpreted. For these reasons, considerable interest recently has been in the output devices required for digital computers. Many solutions to the problem of high speed readout with accuracy and flexibility have been proposed, are in existence, and are being developed. Among these are systems using cathode ray tubes.

1.1 Cathode Ray Tube Displays

Two approaches using cathode ray tubes (crt) have been pursued. Tubes, such as the Charactron and Typotron, have been developed which enable rapid coding of characters and positional information upon the tube face. These devices use electrons shot through a matrix of cutouts in the shape of the characters within the tube to display these symbols. The other approach, similar to the IBM 740 and 780 units, displays output information by conversion of digital-to-analog data which is then displayed on an oscilloscope. Alphabetic and numeric characters are generated by the display of points under control of routines. The IBM 740 crt recorder[1] is a digital-to-analog converter consisting of a seven-inch cathode ray tube and control circuitry used with a film recorder. The 780 display is a 21-inch cathode ray tube system which provides visual display of data being recorded in the 740 unit. The data to be displayed is transferred from the computer to the deflection registers of the display. The recorder (740) first converts the data to dual deflection voltages. After the voltages reach the desired accuracy, the crt's are unblanked and the coordinate point is displayed.

Thus, the IBM displays are of the spot positioning and printing type. A circuit used with IBM display systems has been described in literature[2]. The circuit provides the conversion of positional information from digital-to-analog in a magnetic deflection system by the use of binary weighted, constant current sources. Outputs from the switch tubes used are tied in parallel and fed to the deflection yoke. The experimental system requires selected tubes and precision resistors. Over a period of 30 hours the system remains to within an accuracy of positioning of 0.1% with no visible evidence of drift.

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[1] IBM 704 Electronic Data Processing Machine Manual of Operations - International Business Machine Corporation - 1954-55, pp. 63-65.

[2] E. J. Smura, A Binary-weighted Current Decoder, IBM Journal, October, 1957, pp. 356-362.

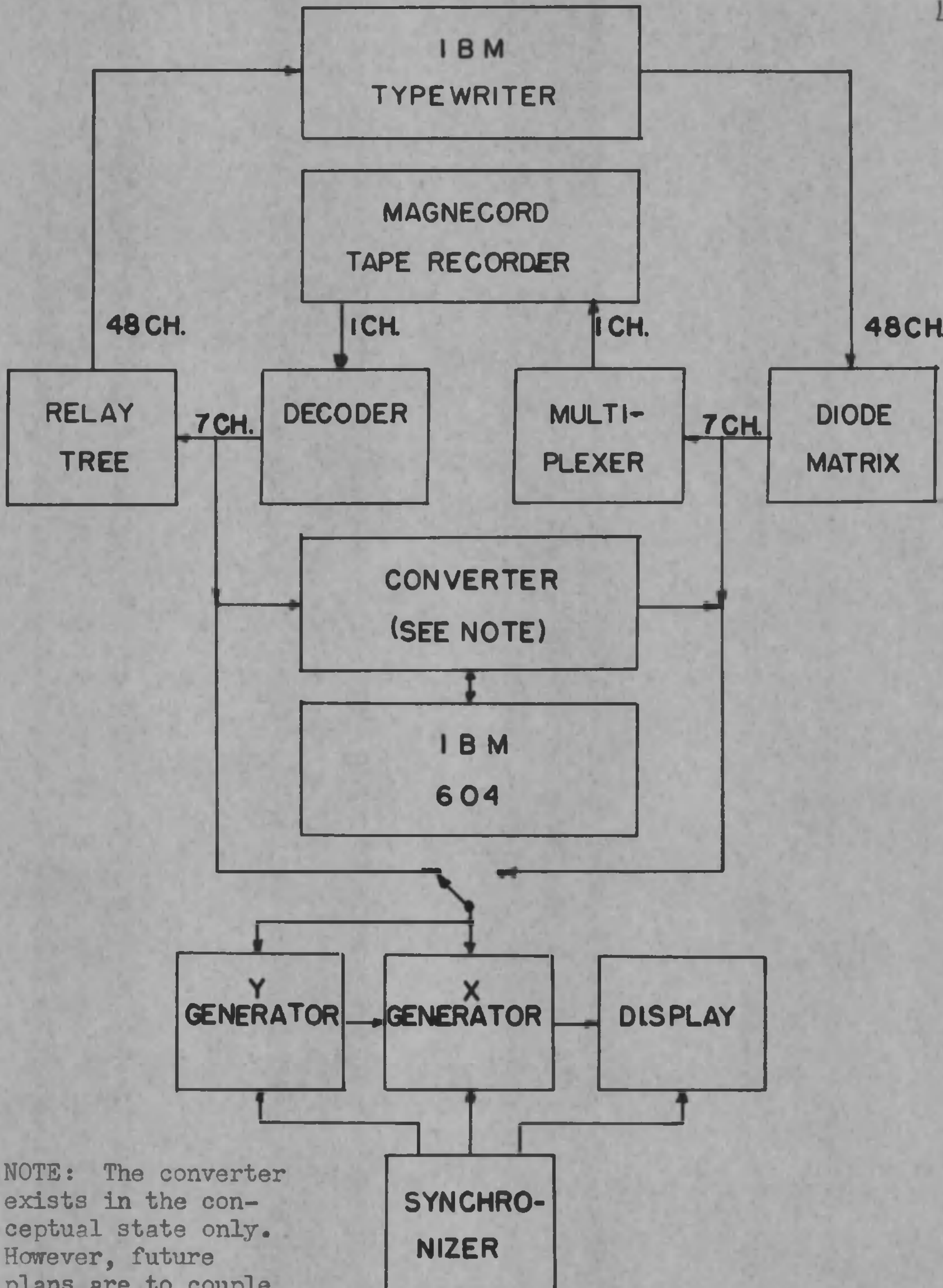
1.2 Statement of Problem

This thesis presents another original approach to the display of digitally processed data. The display system output would consist of a commercial video monitor system. The picture tube would be conventionally swept in the horizontal and vertical directions. However, the sweep signals would be electrically divided into segments by the equipment of this thesis.

These segments would be counted in binary counters. For a particular point to be displayed, the coordinate information would be compared with the count in logic circuits. A coincidence of the resultant abscissa and ordinate pulses would provide an unblanking pulse for the print axis of the cathode ray tube.

The problems of providing such a display are those of analysis of the system requirements, the design and mechanization of the electric circuitry to perform the desired quantizing and point selection, and the evaluation of the system.

The equipment of this thesis was designed to be compatible with the existing Special Purpose Arizona Computer, Experimental (SPACE) equipment and concepts. Figure 1.1 shows the equipment involved. The existing SPACE equipment consists of input-output equipment with tape memory. Binary signals from the typewriter are converted to gated audio tones and stored in this memory. This data can be taken from memory and decoded into binary signals for typing out information or to provide point information to the display equipment of this thesis.



NOTE: The converter exists in the conceptual state only. However, future plans are to couple the IBM 604 to the other SPACE equipment.

FIGURE 1.1 SPACE

The concepts involved in the SPACE program are to provide a digital computer system which will function for demonstration, research evaluation, and educational purposes. The demonstration and educational values of a display of digital procedure are obvious. The many uses of the display for research evaluation and experimentation are listed later.

CHAPTER 2

SYSTEM ANALYSIS AND DESIGN

2.1 General Description of Approach

The basic idea involved in the display system developed is the utilization of the sweep features of a standard television receiver. This would be accomplished by quantizing the sweep intervals into time segments. A count of these segments can be compared with the input data. A coincidence of signals would provide the necessary gating signal for the display tube.

This scheme provides a display of points. A detailed description of the evolved system follows.

2.2 Method of Television Scanning[1]

In order to facilitate a description of the display system, a brief discussion of the television display process will be presented.

The phosphorus screen of a television picture tube is linearly scanned by a beam of electrons. Sawtooth signals of different frequencies are applied to the horizontal and vertical deflection plates

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[1] Sid Deutsch, Theory and Design of Television Receivers, McGraw-Hill Book Co., Inc., 1951, pp. 5-17.

or coils. With the application of the sawtooth waveforms to both sets of plates or coils, the beam is moved rapidly across the screen. At the same time, it is moved slowly down the screen by the slower vertical sweep. The downward tilt is not discernible because the horizontal sweep is so much faster than the vertical sweep. The tilt is just sufficient to cause each horizontal line to begin slightly below the previous one. When the beam reaches the right side of the picture tube, a horizontal blanking pulse appears on the grid of the picture tube and cuts off the beam. Shortly after the beam has been blanked, a horizontal synchronizing pulse is received by the horizontal sweep system. This sync pulse initiates the start of the snapback of the horizontal sawtooth. The beam returns to the left side of the screen. This process is continued until the beam reaches the bottom of the scanning raster. Then, it is returned to the top by the abrupt rise of the vertical sawtooth.

Another feature used in commercial television concerned with the reduction of required video bandwidth and associated with the picture presentation is that of interlaced scanning. The horizontal lines are not scanned in sequence. By the proper selection of the horizontal and vertical scanning frequencies, every other line is scanned.

2.3 System Requirements and Concepts

Having established the manner by which television rasters are formed, the general requirements for the display system could then be determined.

Since a display of points was desired, the electron beam had to be cut off and gated on when the points were to be printed. This method is different from television display of information. In that medium, the beam is permitted to excite the phosphorus when no video signal is present, and is turned off or to less intensity by video information.

Another requirement which had to be satisfied before the display system could be established was the need for synchronous signals. The horizontal and vertical sweeps had to be properly timed. A basic timing source was needed.

In addition, a method of dividing the sweep intervals into segments was required. This division had to be the same for each sweep, that is, in synchronism with the sweep signals.

Additional requirements were imposed by the nature of the input signals which were available. Since the display equipment is to be used with a serial-parallel machine, the input circuitry was designed to permit maximum use of available features. (A serial-parallel machine is defined as one in which the bits representing a digit are sent from one location to another on parallel lines. Successive digits are sent in time sequence.)

With the above requirements as a guide, the display system was conceived. Figure 2.1 shows a block diagram of the system. Figure 2.2 shows waveforms of the signals involved.

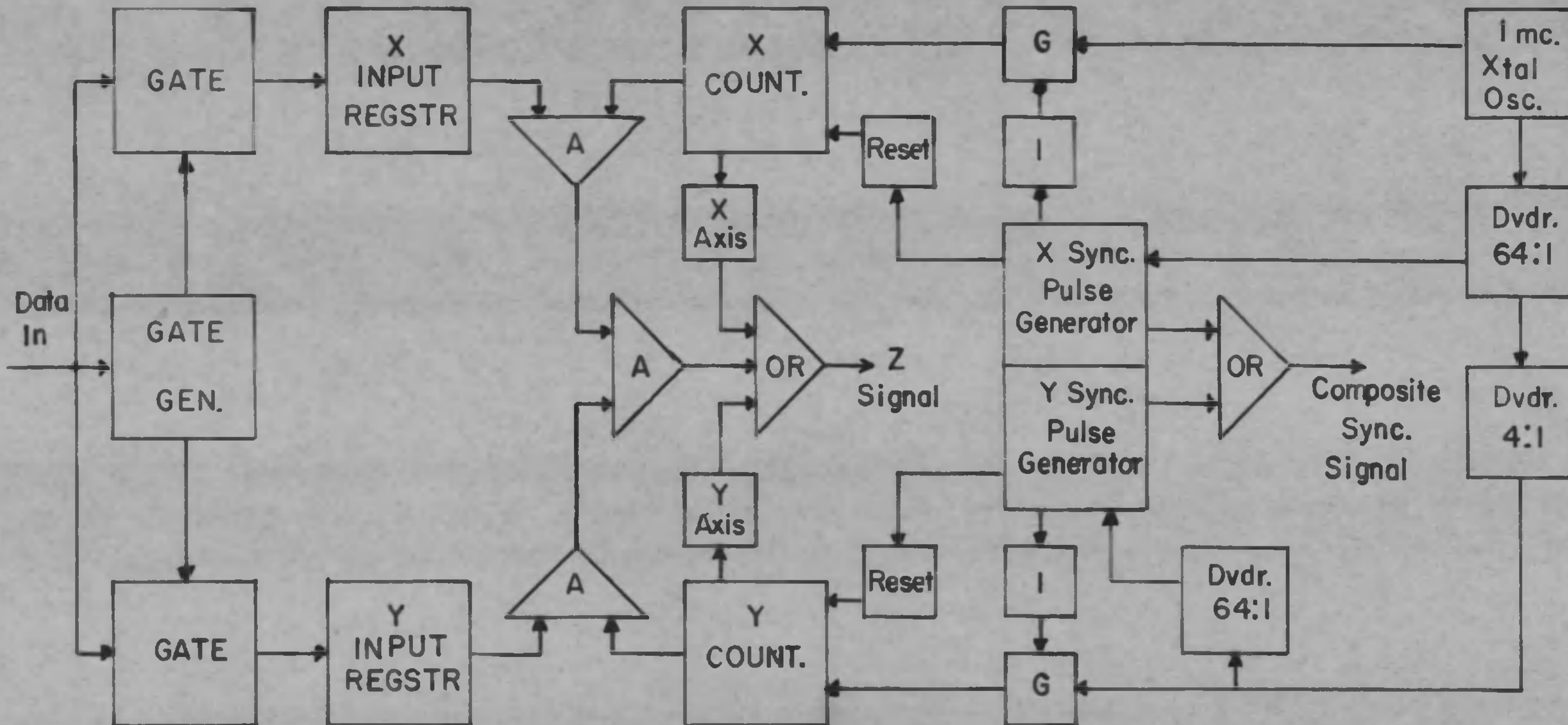

FIGURE 2.1 SYSTEM BLOCK DIAGRAM

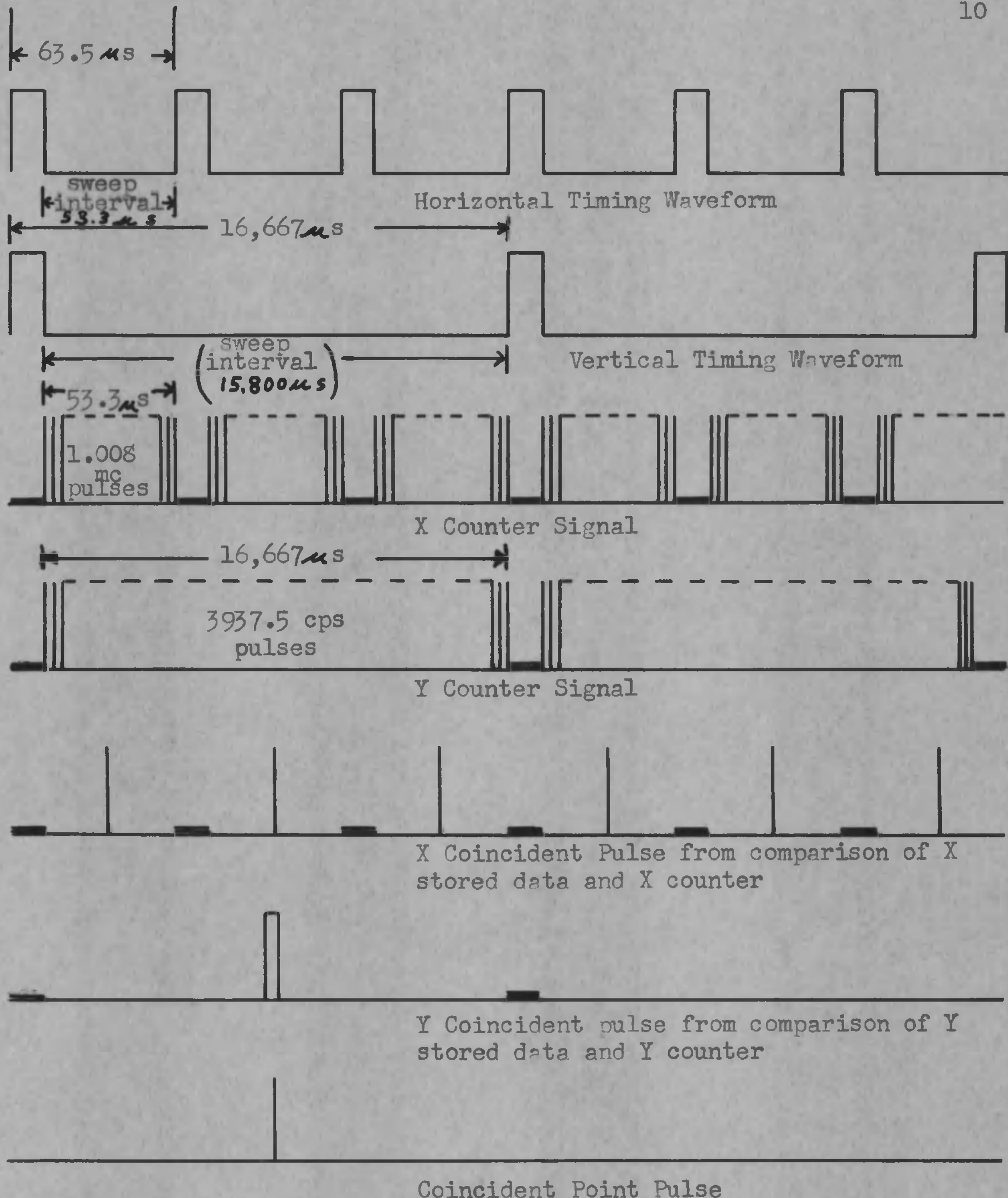

FIGURE 2.2 TIMING DIAGRAM

Six channels of binary information are available. A seventh channel presents a pulse each time data is transmitted. Since the data is presented in serial-parallel fashion, gates are required to properly direct these signals to either the X or Y input registers. The seventh channel signal is used to open and close these gates.

From six lines carrying binary information, 2^6 or 64 different numbers may be represented. Since the horizontal scanning frequency is 15,750 cycles per second, the quantizing frequency was determined to be 64 x 15,750 = 1.008 megacycles per second. Using this quantizing frequency, the horizontal sweep and retrace signal can be divided in 64 segments. At each segment then, an electrical pulse occurs. These pulses are counted in a binary counter. When the count compares exactly with the input data which has been placed in temporary storage, a coincidence can be obtained.

The interlaced scanning property of standard television reception was omitted from this initial approach. There are ways of using this display system and interlaced scanning. One of these would be to divide the frequency from 15,750 cps in a different manner than indicated and obtain the standard vertical scanning frequency. Then the display data can be gated on for every other field.

Having determined the horizontal quantizing frequency, the selection of the vertical frequencies followed. Since all signals were to be synchronous, it was decided to generate the 1.008 megacycle per second signal in a crystal oscillator. As indicated in Figure 2.1, this oscillator frequency was divided by 64 to give the horizontal scanning frequency of 15,750 cps. This frequency, in turn, was divided by 4 to give the vertical quantizing frequency of 3937.5 cps. Dividing again by 64 gave the vertical scanning frequency of 61.5 cps.

Also shown in Figure 2.1, is the generation of a composite synchronizing signal which is supplied to the television set to insure proper timing of the sweeps.

As mentioned earlier, the input data is stored in an electronic memory called a register. The time of storage depends on the manner of usage. For initial tests it was selected to be 45 milliseconds. This is a time greater than that required to read the data into both the X and Y registers and to complete one vertical sweep.

The count is then compared with the input data. A coincidence of the X data and its counter would generate a pulse in its logic circuit. This pulse, however, is not applied to the Z or print axis of the cathode ray tube unless the Y data is coincident with its counter.

Additional features are indicated on the block diagram. Generation of the X and Y axes is possible by obtaining the counter status for these points. Also, a capability of resetting the counters is needed. Since the sawtooth sweep signals applied to the deflection coils or plates require time to sweep back, the entire scan interval cannot be used. Hence, the counters must be reset to zero for the start of each sweep. The reset signal is derived from the same source which provides the horizontal and vertical gating signals.

CHAPTER 3

SYSTEM DESIGN

3.1 Properties of Digital Circuits[1]

Digital circuits are characterized by input and outputs which have two states usually defined as zero and one in binary notation. Depending on the specific components used, the two states may be represented by a contact open or closed, a voltage level high or low, or a pulse present or absent, magnetization in one direction or the other, etc.

The number of basic digital logic circuits is small. The "and", "or", and "not" operations are used in this thesis.

The "and" circuit, also called the coincidence circuit or gate, has an output of one if and only if its inputs are one. For a two-input "and" circuit, the following table can be constructed to illustrate the properties.

TABLE I

INPUT	INPUT	OUTPUT
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

[1] A. K. Susskind, Notes on Analog-Digital Conversion Techniques, Technology Press of MIT and John Wiley and Sons, Inc., pp.4.1-4.3.

The "or" circuit, also called mixer, has an output of one if any of its inputs is one. For a two-input "or" circuit, the following table can be constructed.

TABLE II

INPUT	INPUT	OUTPUT
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

The "or" and "and" operations may be realized by either diode or vacuum tube circuits.

The "not" operation is obtained in any circuit which inverts the polarity of the input pulse.

Another circuit used in digital application is the bistable multivibrator or flip-flop. This is an electronic circuit containing two tubes which can exist only in one of two stable states and which can be put into one or the other of the stable states by means of an external signal, usually a trigger pulse. After occurrence of the signal, the flip-flop remains in the newly acquired stable state until another external signal occurs which causes the flip-flop to return to the first stable state. The bistable multivibrator is used for the generation of square wave pulses, counting, and to provide electronic memory.

3.2 Input Circuitry

The input circuitry, as seen in Figure 2.1, is defined to consist of the input gates, gate generator, and registers.

The data to be displayed will be presented to the display unit in parallel-serial fashion. Either the X or Y data may be presented first. Six binary channels of information are available. A seventh channel presents a binary "one" signal whenever any data is being processed. These signals are used to generate the gating signals which determine where the data is to be placed.

The input gates, shown in Figure 3.1 were designed to accommodate positive input signals. Since an inversion takes place, the input registers, Figure 3.3, were designed to trigger on negative signals.

The input registers are required to store the data for a time dependent on the use of the display. If data is inserted in the X registers first and, then, into the Y, and neither the X nor Y is increased by increments, then the time that the data is in storage must be greater than the time to make one vertical sweep. If data is to be displayed with one parameter, probably the Y, varying in increments, then the registers would only be required to hold the data for the length of one horizontal sweep. In the equipment designed to verify the theory and logic involved, the time of holding the data in the registers was selected to be 45 milliseconds. In the discussion of applications, the time that data is in a register is chosen to be the horizontal sweep time of approximately 50 microseconds. Since

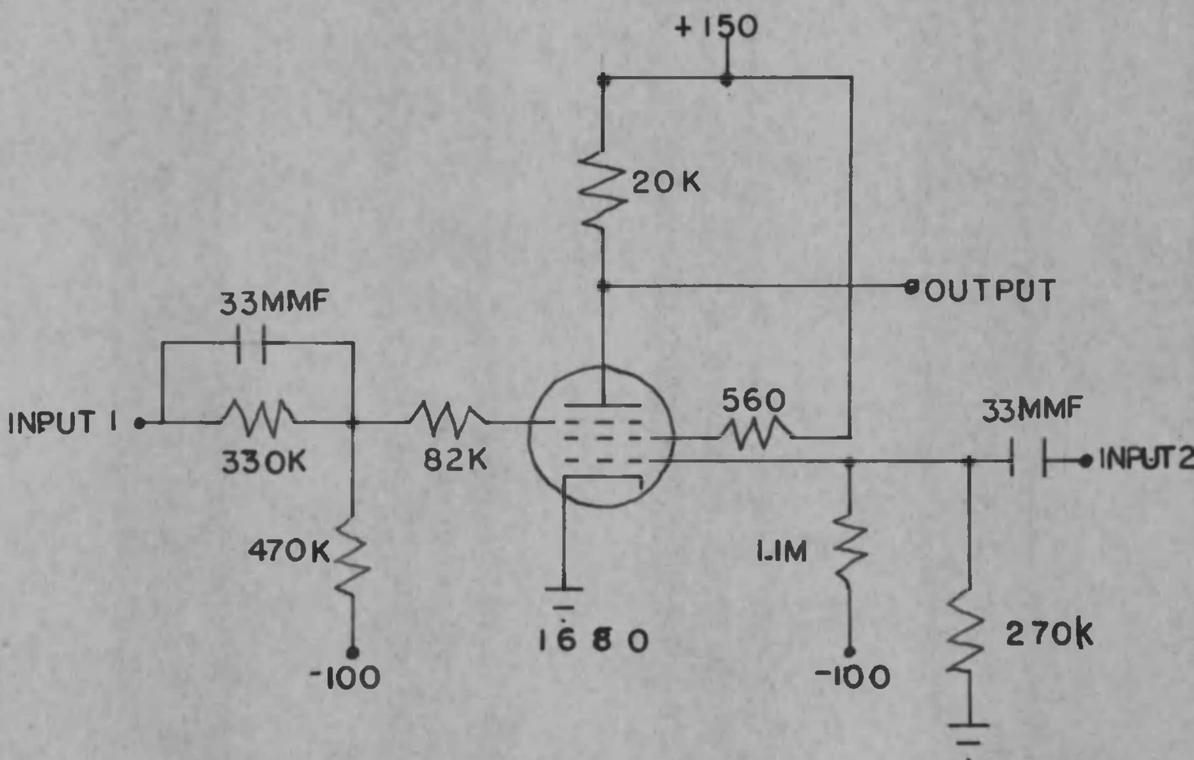

FIGURE 3.1 INPUT GATE

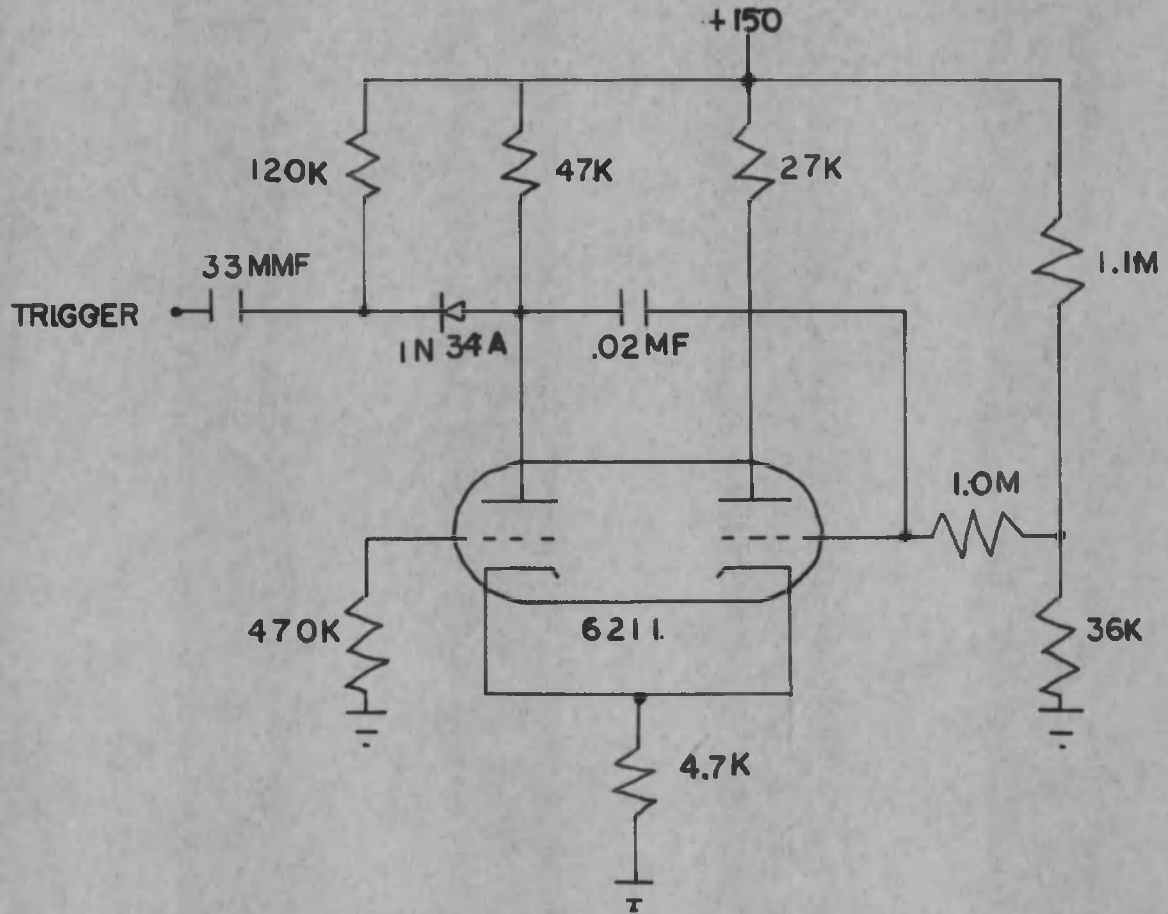

FIGURE 3.2 INPUT REGISTER

the input registers are monostable multivibrators, only one condition can be satisfied.

Conventional graphical methods[1] were used to design the monostable multivibrator used in the input registers. The final circuit is shown in Figure 3.2. Complement signals are available for use in the logic circuits which follow the registers.

3.3 Counter

The bistable multivibrator or binary has been described as a two-tube regenerative circuit which can exist indefinitely in either of two states and which can be caused to make an abrupt transition from one state to the other. The binary has two outputs, one of which is the complement of the other. Recalling that voltage levels can be given the value of 0 or 1 whether the level is low or high, it is seen that a bistable multivibrator provides such signals. If one output is called B, the other will be not B or in Boolean notation, $\overline{B}$. These are the signals referred to later in the discussion of the logic circuit.

Self-biased binaries with symmetrical triggering are used in the counter designed. The design[2] of a typical binary stage as shown in Figure 3.3 was as follows. The design is presented in detail since it differs from the reference in accounting for the method of triggering. The values of R_L and R were selected to be 36,000 ohms.

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[1] J. Millman and H. Taub, Pulse and Digital Circuits, McGraw-Hill Book Co., Inc., 1956, pp. 145-201.

[2] Ibid., p. 145.

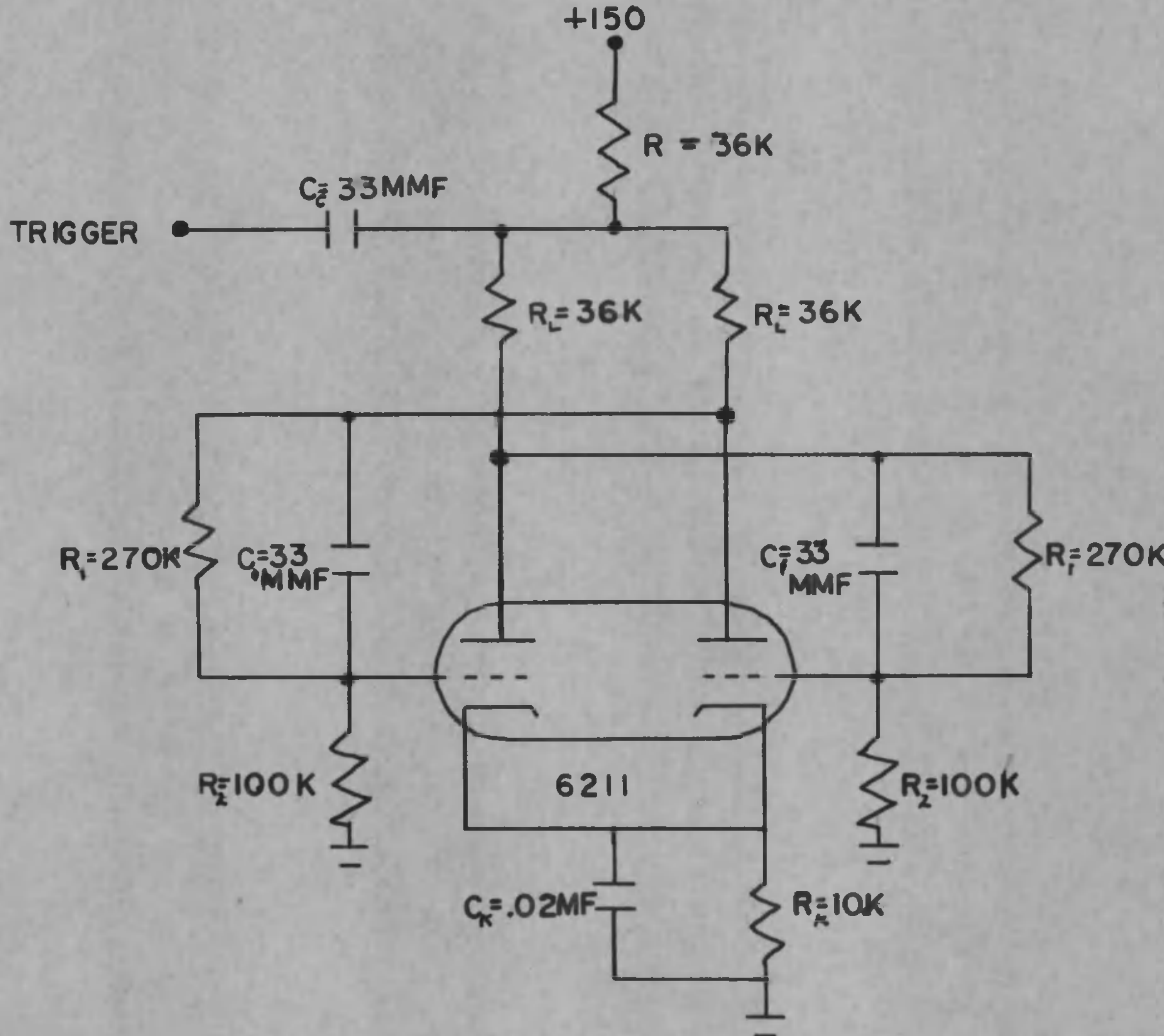


FIGURE 3.3 BISTABLE MULTIVIBRATOR

The tube was chosen to be a 6211. The cathode resistor, R_k was selected to be 10k. Since the time constant of the cathode resistor and by-pass capacitor, R_kC, must be greater than the transition time which would be about one microsecond, C was made 0.02 microfarad.

Tube T_1 of Figure 3.3 was then assumed to be cut off and tube T_2 clamped with a grid to cathode voltage equal to zero. The clamped current I_2 of T_2 was determined by drawing a load line which passed through a supply voltage of $150 - RI_2$ and had a slope corresponding to $R_L + R_k$. Several graphical trials were made before an I_2 of 1.6 milliamperes was obtained.

This value provided a cathode voltage, $E_k = 10 \times 1.6 = 16$ volts. The plate to ground voltage, E_{b2}, of T_2 became $150 - RI_2 - R_LI_2 = 35$ volts. $E'_{bb} = 150 - RI_2 = 92.5$ volts.

The grid-to-ground voltage of T_1 was found as

$$E_{gn1} = \frac{R_2}{R_1 + R_2} \times 35.$$

R_1 and R_2 were selected equal to 270k and 100k respectively. Then,

$$E_{gn1} = \frac{100}{370} \times 35 = 9.5 \text{ volts.}$$

The grid-to-cathode voltage of T_1 was

$$E_{gk1} = 9.5 - 16.0 = -6.5 \text{ volts.}$$

The cutoff voltage is approximately -3 volts for the plate voltage of T_1 as given. Hence, T_1 is truly not conducting.

Without grid current, the voltage at the grid of T_2 would be

$$E_{gn2} = 92.5 \times \frac{100}{36 + 270 + 100} = 22.5 \text{ volts.}$$

However, since the cathode voltage is at 16 volts, this grid is clamped and the original assumption is true.

The actual value of the plate voltage, E_{b1} of T_1 can be obtained by writing the nodal equation at that point. Then,

$$\frac{E_{b1} - 92.5}{36{,}000} + \frac{E_b - 16}{270{,}000} = 0$$

$$E_{b1} = 83 \text{ volts.}$$

The plate swing is 83 - 35 = 48 volts.

The capacitors, C_1, are needed to compensate for the input capacity of the tubes. The Miller effect may make this capacity as large as 25 to 50 micro-microfarads. Due to an ample supply and suitability, 33 micro-microfarads capacitors were used.

Triggering is performed with a negative pulse coupled to R as shown in Figure 3.3.

Connection of the binaries in the arrangement shown in Figure 3.4 provided the counter. The method of coupling from one binary to another is symmetrical. The first binary is driven by a pulse amplifier. The binary chain shown constitutes a scale-of-64 counter. The circuit has 64 possible different states and at the

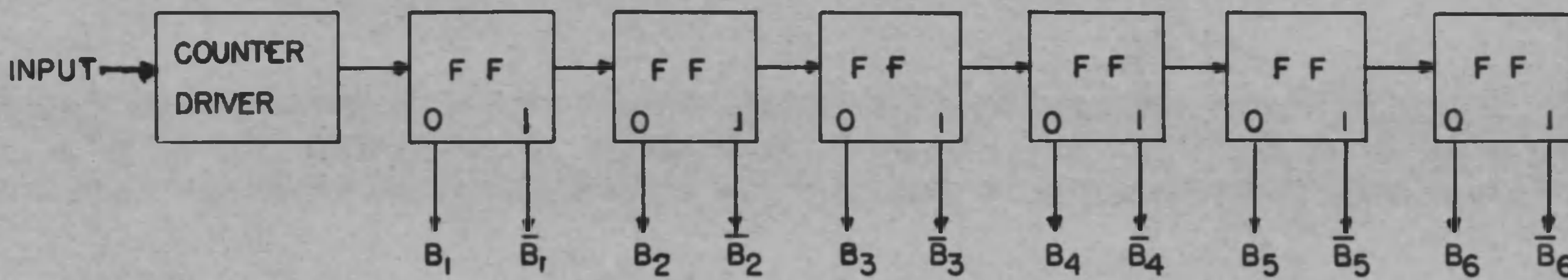


FIGURE 3.4 BINARY COUNTER

occasion of each input pulse the circuit will make a transition progressively from state to state. After 64 pulses, the circuit will return to its original state.

To read the count of the binary chain, the state of each individual binary must be determined. The counter of Figure 3.4 is in the reset or zero state.

3.4 Logic

The logic which must be satisfied before a point can be displayed is developed in this section. A Boolean expression which related the counter to the input data was required.

Two representations of a binary number which are compared will be equal and true only if each digit of that number is equal in both representations simultaneously. Since two Boolean quantities may be equal if they are both zero or both one, both cases must be considered. This can be done by expressing the terms in an "or" fashion. Further, all digits must be coincident for the proper output. The Boolean expression for the coincidence of two binary representations is

$$X = (A_1B_1 + \bar{A}_1\bar{B}_1)(A_2B_2 + \bar{A}_2\bar{B}_2)(A_3B_3 + \bar{A}_3\bar{B}_3)$$
$$(A_4B_4 + \bar{A}_4\bar{B}_4)(A_5B_5 + \bar{A}_5\bar{B}_5)(A_6B_6 + \bar{A}_6\bar{B}_6).$$

The validity of this expression can be proven by considering the comparison of a two-digit binary number with a two-stage binary counter. The following table illustrates that an output will be obtained only when the conditions of the Boolean expression are satisfied. This occurs after the counter has received three signals.

TABLE III

INPUT BOOLEAN SYMBOL	STORED BINARY NUMBER	COUNTER BOOLEAN SYMBOL	COUNTER READING 0 COUNT	1ST COUNT	2ND COUNT	3RD COUNT	4TH COUNT
A_1	1	B_1	0	1	0	1	0
$\overline{A}_1$	0	$\overline{B}_1$	1	0	1	0	1
A_2	1	B_2	0	0	1	1	0
$\overline{A}_2$	0	$\overline{B}_2$	1	1	0	0	1

The Boolean expression derived above is shown in symbolic representation in Figure 3.5. Figure 3.6 shows the actual diode circuit which was mechanized to prove the logic.

3.5 Definition of the Display System

Having given the logic, the basic requirements and the components, the display system can now be defined. Figures 3.7 and 3.8 show the required organization of electronic circuitry to provide a display of the type discussed.

The data would be read into either the X or Y subsystems through gates which are opened and closed by a generator triggered off the seventh channel. The data would be held in storage for a length of time dependent on the usage of the system. Meanwhile, the counters would be counting signals derived from the synchronizer unit to be described in Section 3.6. A comparison of the input and the count would be made in the diode logic circuit. A coincidence of the

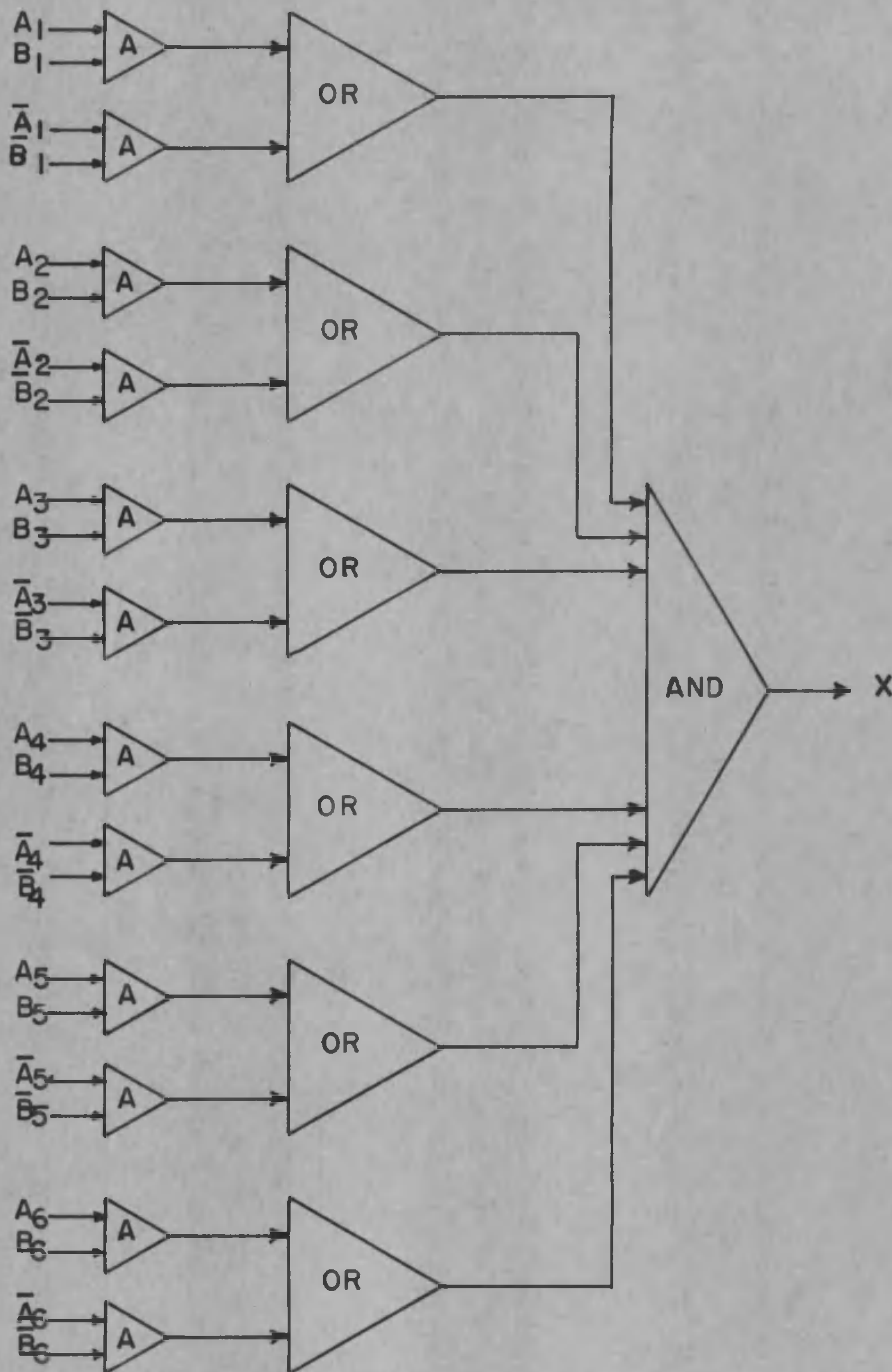


FIGURE 3.5

SYMBOLIC NETWORK OF THE BOOLEAN EXPRESSION

$$X = (A_1B_1 + \bar{A}_1\bar{B}_1)(A_2B_2 + \bar{A}_2\bar{B}_2)(A_3B_3 + \bar{A}_3\bar{B}_3)(A_4B_4 + \bar{A}_4\bar{B}_4)(A_5B_5 + \bar{A}_5\bar{B}_5)(A_6B_6 + \bar{A}_6\bar{B}_6)$$

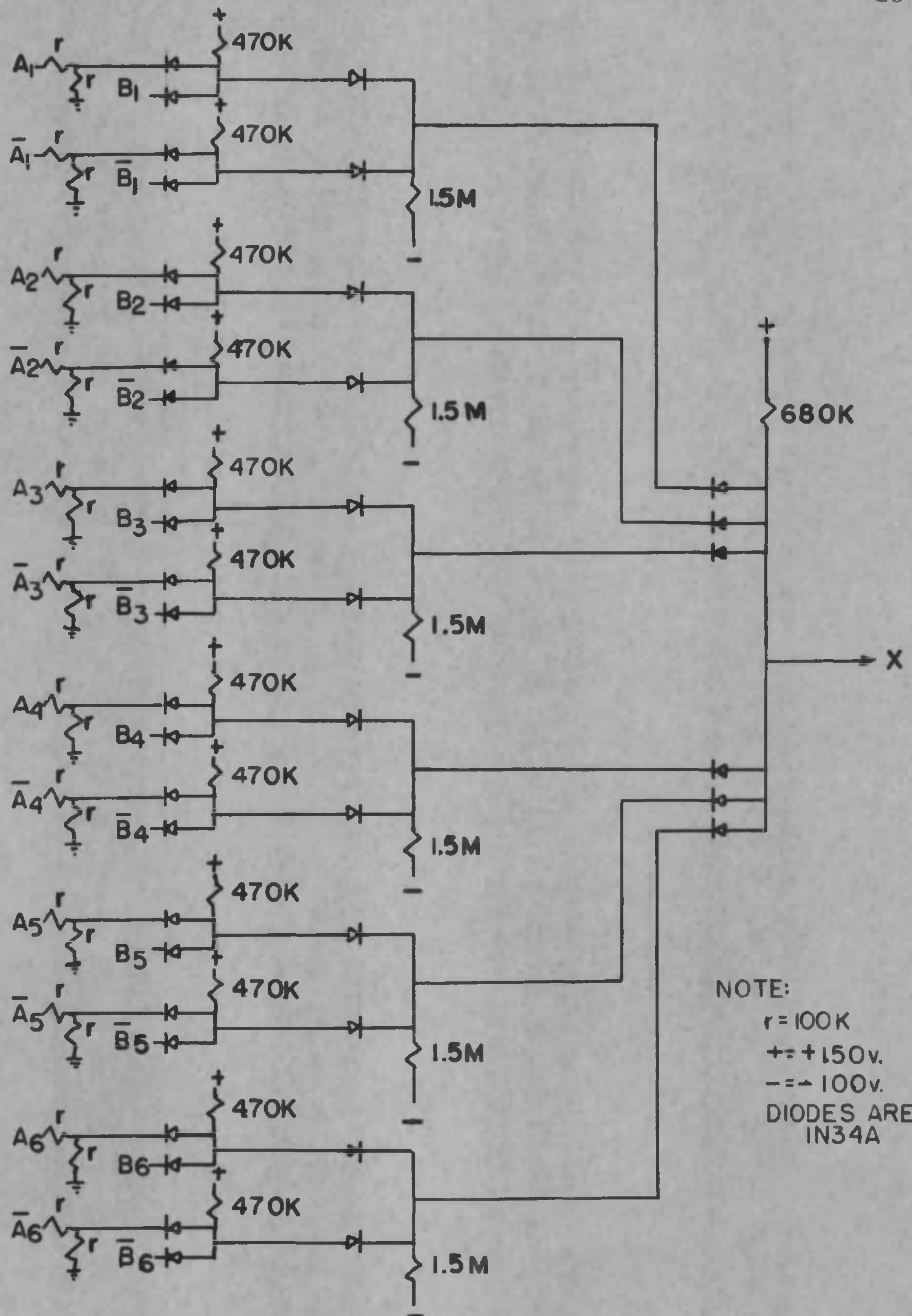
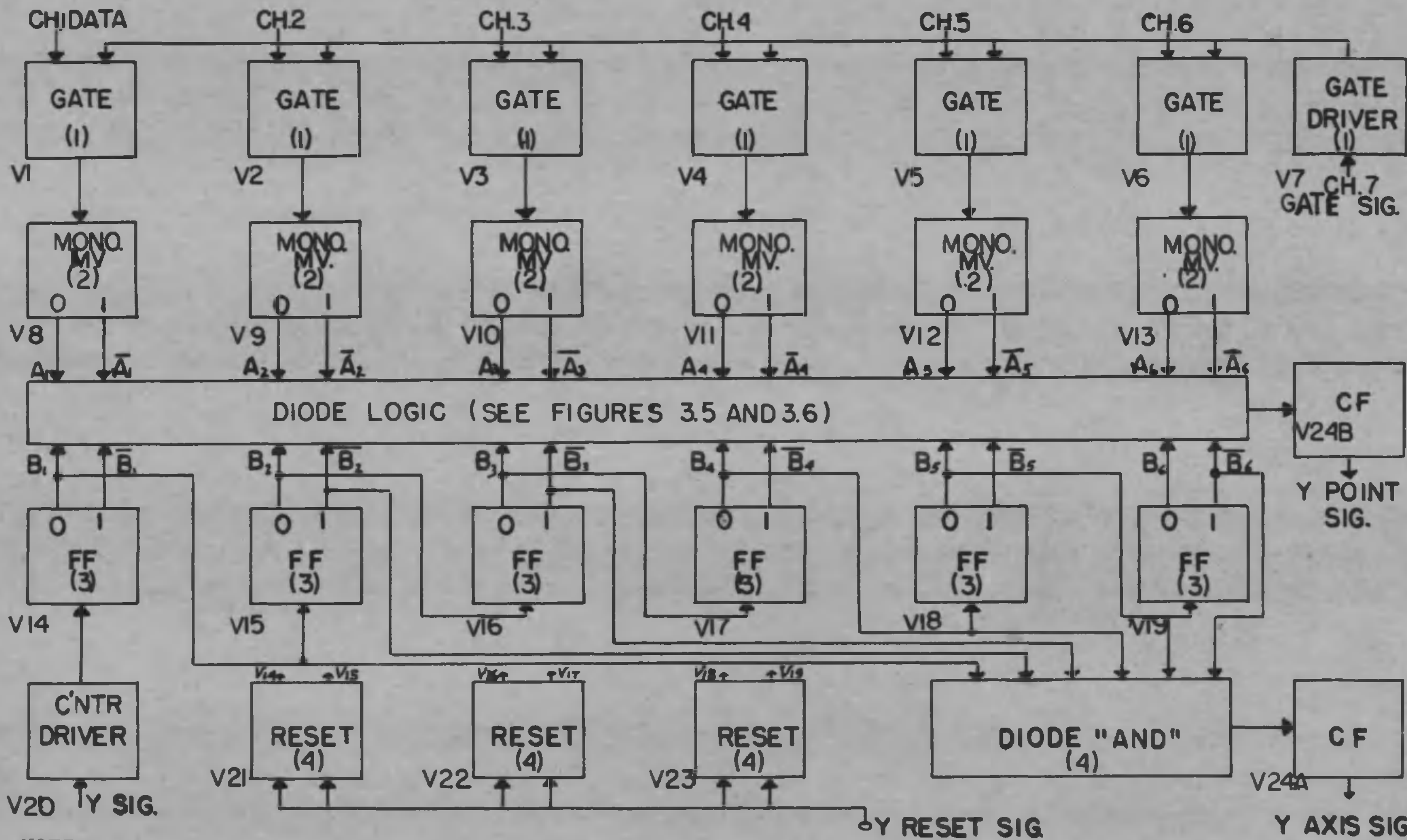


FIGURE 3.6 DIODE LOGIC CIRCUIT



NOTE:
(1) See Figure 3.1
(2) See Figure 3.2
(3) See Figure 3.3
(4) See Text, Chapter 3, Section 3.5

FIGURE 3.7 Y-SIGNAL GENERATOR

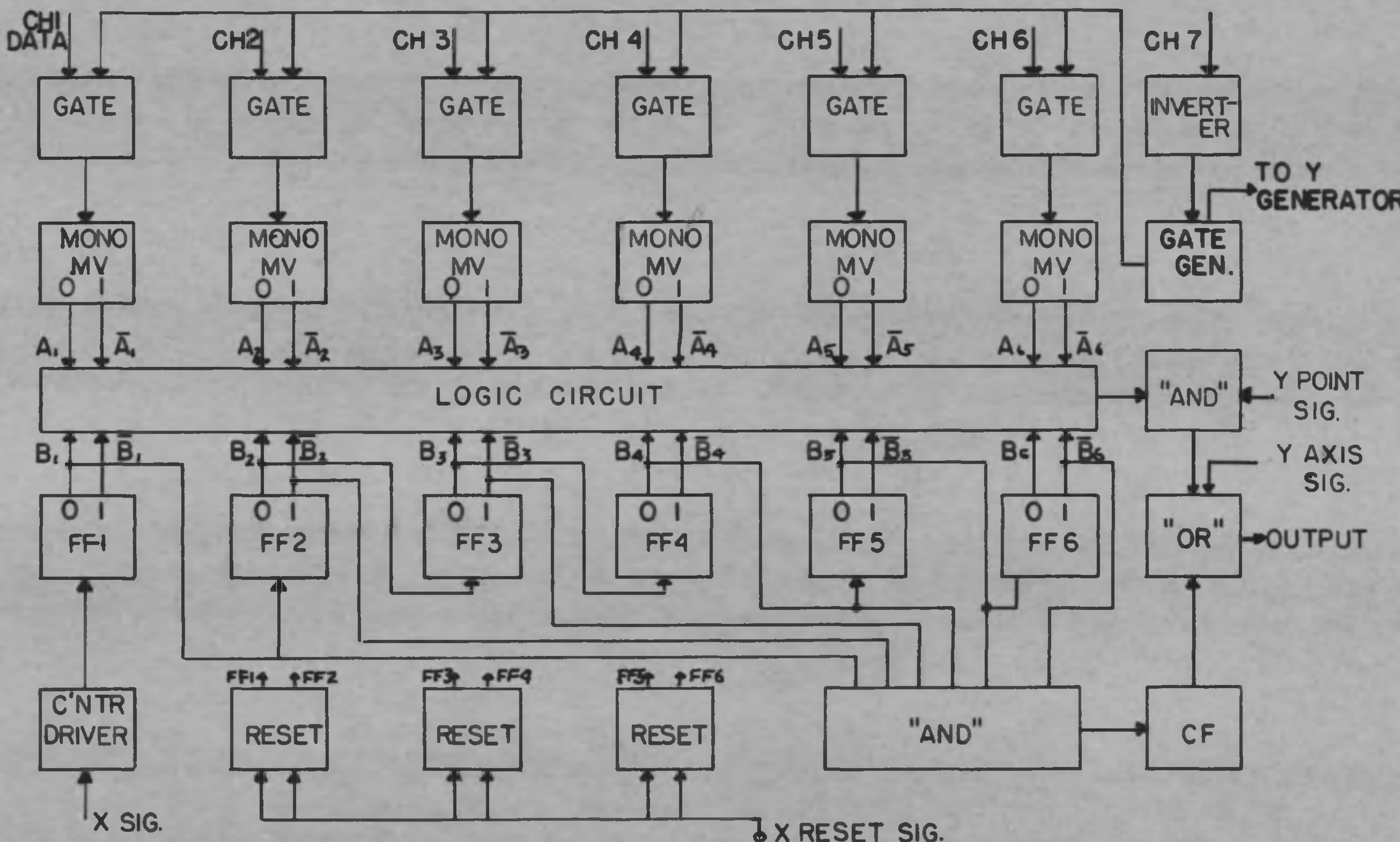


FIGURE 3.8 X-SIGNAL GENERATOR

X and Y signal would provide an output which would be used to turn on the beam of the television video monitor. The sweep signals of the television monitor are driven in synchronism with the quantizing signals. The resultant display point then would occur at the same spot on each full coverage of the screen.

As mentioned earlier, a resetting of the counters is required. This is accomplished through the use of triodes whose plates are directly connected to the section of the bistable multivibrators which was defined to be the zero condition. The horizontal and vertical reset pulses are derived in the synchronizer unit discussed in Section 3.6.

The signals required to print out the axes is obtained from the count correspoinding to the axes points. Diode "and" circuits are used to select the proper counter indication.

3.6 Synchronizer

The display system extended requires the basic waveform generators to run synchronously, that is, in step with one another, so that each signal arrives at some reference point in its cycle at the same time. The frequency stability of waveform generators is never adequate to ensure synchronism. Therefore, some method, such as frequency division, must be used.

A synchronizer unit was designed and constructed to provide the needed signals. A block diagram is shown in Figure 3.9. A complete schematic is given in Figure 3.10.

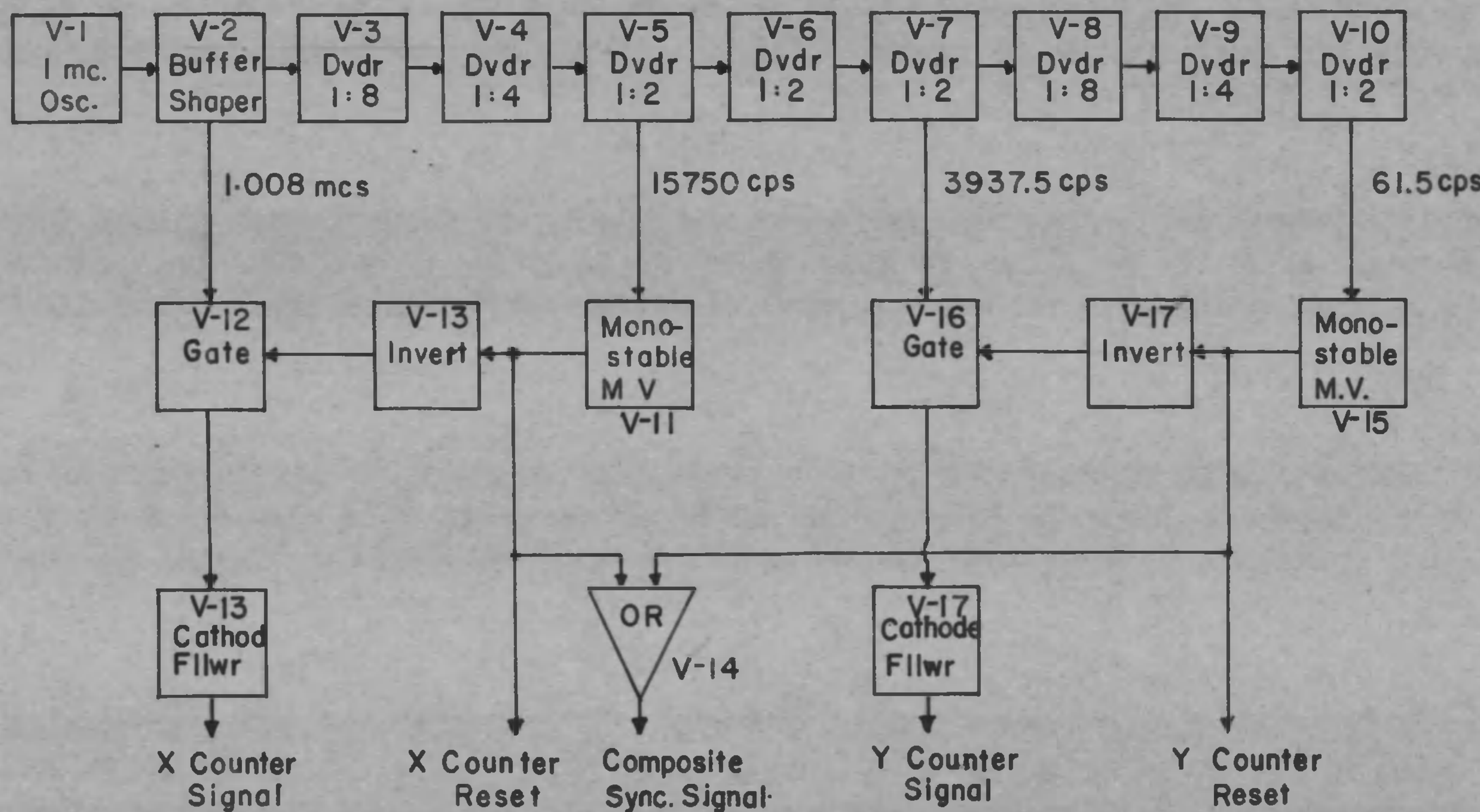


FIGURE 3.9 SYNCHRONIZER BLOCK DIAGRAM

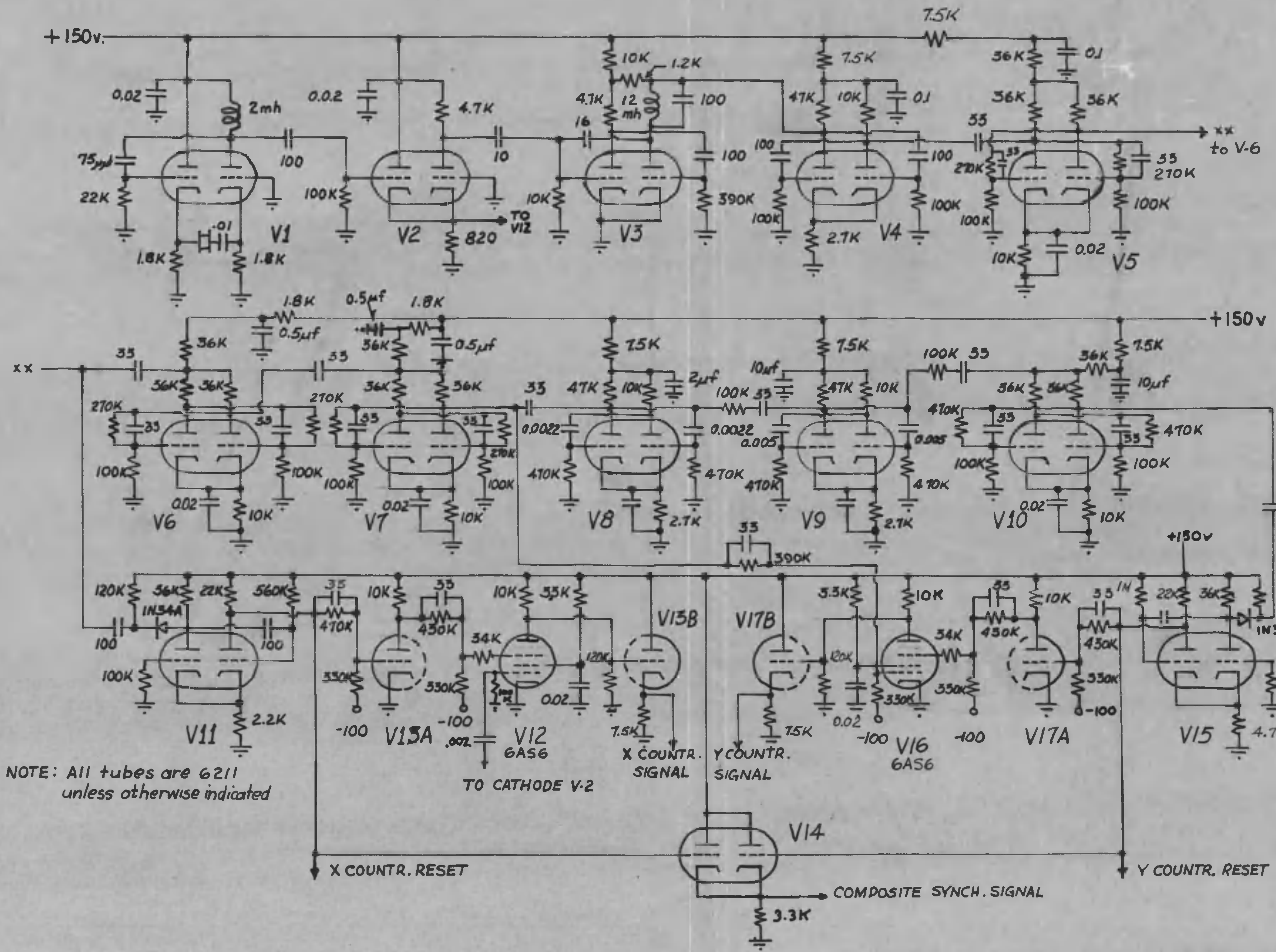


FIGURE 3.10 SYNCHRONIZER SCHEMATIC

A crystal oscillator, connected in a Butler circuit and shown as the circuit of V_1 of Figure 3.10, is used to provide a basic clock source of 1.008 megacycles per second. This signal is divided by 8 in the circuit of V_3. This circuit is an astable multivibrator which, if permitted, would oscillate at about 90 kilocycles per second. However, the pulses from the clock buffer, V_2, are superimposed on the grid return signals to provide a synchronous output which scales the input down by eight.

The next division in the chain is accomplished by the divide-by-four circuit of V_4. Again, this circuit is an astable multivibrator which normally would operate at a lower frequency than occurs when it is driven synchronously.

The bistable multivibrator of V_5 provides an output at the horizontal frequency of 15,750 cycles per second. This signal triggers a chain of two more binary circuits of V_6 and V_7. The vertical quantizing frequency of 3937.5 cycles per second is obtained from V_8.

Additional dividing by 8 in the circuit of V_8 and, again, by 4 in the circuit of V_9 is accomplished. These circuits are also astable multivibrators which are triggered into synchronism.

The last division in the chain is in the bistable multivibrator circuit of V_{10}. The output is the vertical scanning frequency of 61.5 cycles per second.

The outputs of V_5 and V_{10} also trigger monostable multivibrator circuits of V_{11} and V_{15}. These multivibrators are used to obtain the properly shaped waveforms needed to gate V_{12} and V_{16} and to form the composite signal needed for synchronizing the television sweep signals. The outputs of V_{12} and V_{16} are trains of pulses occuring during the active portion of the television sweeps. These signals would be used in the counters of the X and Y signal generators.

Additionally, the outputs of V_5 and V_{10} provide the reset signals required to reset the counters during the retrace or inactive portion of the television sweeps.

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Equipment Description

The system presented was verified to the extent that the synchronizer and vertical units were constructed and tested. The equipment was designed for rack mounting and is compatible with the other components of the SPACE system.

Figures 4.1 and 4.2 show photographs of the synchronizer and Y-signal generator units respectively. Among the construction details to be noted are the use of turret sockets and the location of filament transformers on the individual chassis.

In Figure 4.1, the layout of the synchronizer is such that the crystal oscillator is located at the lower right side of the chassis. The frequency division proceeds to the left and then back through the center row of circuits. The back row contains the gates and cathode followers indicated in the schematic.

Four rows of tube circuits are evident in Figure 4.2, the photograph of the Y-signal generator. The top row of the picture is composed of the input gates. The next row is made of the input registers. Neon indicators are used with the multivibrators to provide a visual display of the register status. The diode logic circuit is mounted on the two terminal boards in the center of the chassis. The next row down in the picture is the six-stage binary counter. The

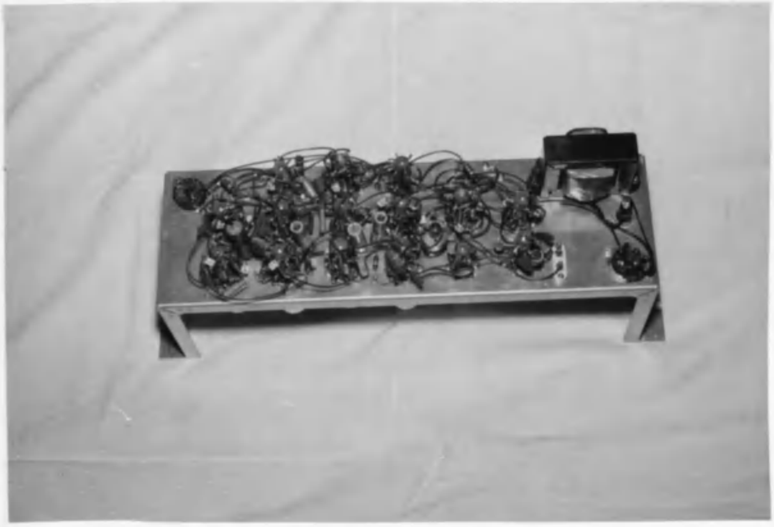


FIGURE 4.1 SYNCHRONIZER

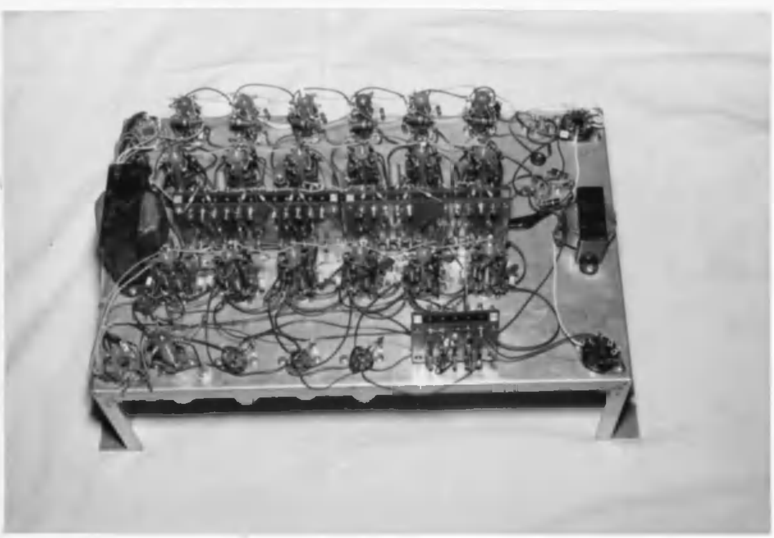


FIGURE 4.2 Y-SIGNAL GENERATOR

bottom row contains the counter drive tube, the reset tubes, and a terminal board holding the diode "and" circuit used for the axis printing.

4.2 Test Results

After proper operation had been established, the individual circuits of the units were tested by observing the results of varying the supply voltages. Additionally, the units were monitored while operating continuously for several hours. Any drift noticed was remedied.

The performance of the units constructed can be best illustrated by waveforms.

Figure 4.3 presents the one megacycle per second signal, a train of one-megacycle pulses, and the output of the divide-by-8 circuit. The division is readily verified.

The general behavior of the divide-by-4 circuit next is shown in Figure 4.4a. Figure 4.4b presents the horizontal scan frequency. Figure 4.4c gives the output of the binary that follows.

The next division of 2 gives the vertical quantizing of 3937.5 cps and is illustrated in Figure 4.5a. The operation of the divide-by-8 circuit that follows is shown and verified in Figure 4.5b. The divide-by-4 output is given in Figure 4.5c.

The 61.5-cps vertical scan frequency signal is seen in Figure 4.6a. Figure 4.6b shows the vertical sync pulses. Figure 4.6c shows the vertical count signal. The waveform does not show too clearly that the signal is composed of a number of 3937.5-cps pulses.

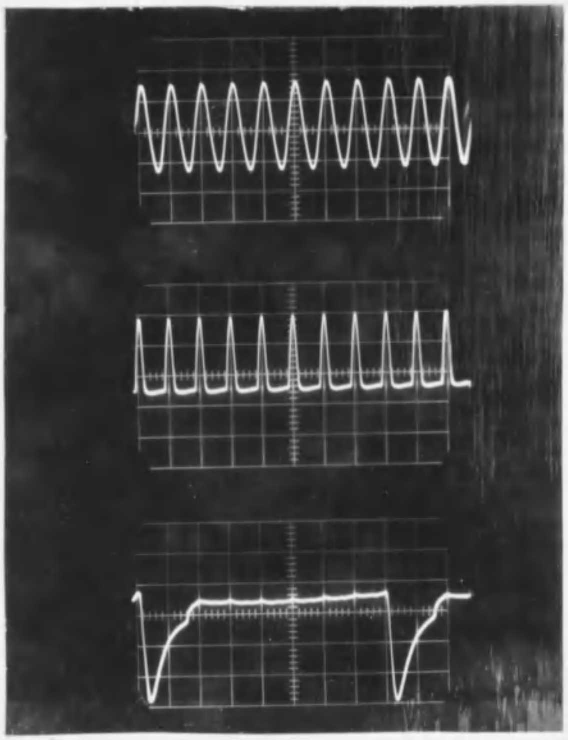


FIGURE 4.3 SYNCHRONIZER SIGNALS I
(sweep = 1μs/cm)
(amplitude = 5v/cm)

a. 1.008 mcps Sine Wave

b. 1.008 mcps Horizontal Quantizing Signal

c. 126 kcps Pulse

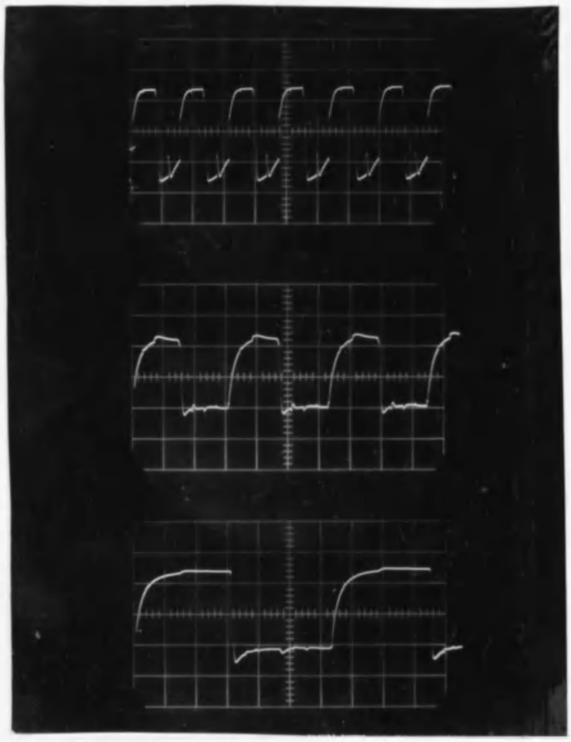


FIGURE 4.4 SYNCHRONIZER SIGNALS II
(sweep = 20μs/cm)
(amplitude = 20v/cm)

a. 31.5 kcps Square Wave

b. 15.75 kcps Horizontal Scan Frequency

c. 7.875 kcps Square Wave

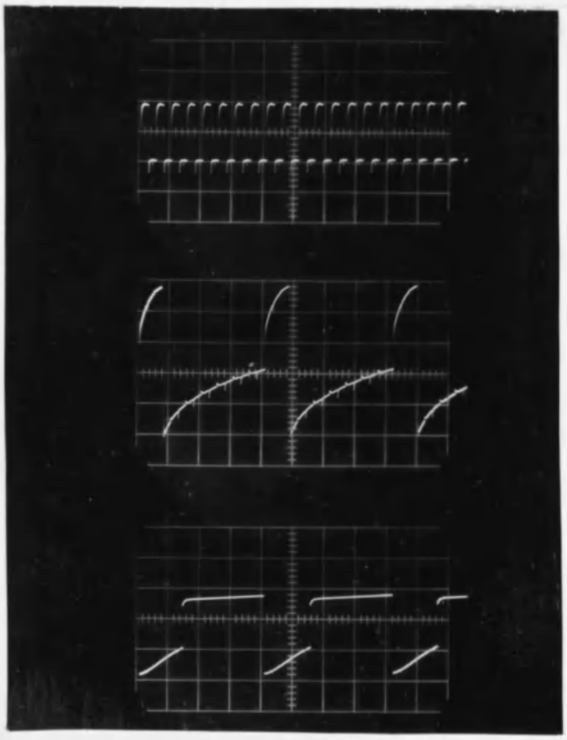


FIGURE 4.5 SYNCHRONIZER SIGNALS III
(amplitude = 20v/cm)

a. 3937.5 cps Vertical Quantizing Frequency
(sweep = 500μs/cm)

b. 492.8 cps Pulse
(sweep = 500μs/cm)

c. 123.0 cps Pulse
(sweep = 2ms/cm)

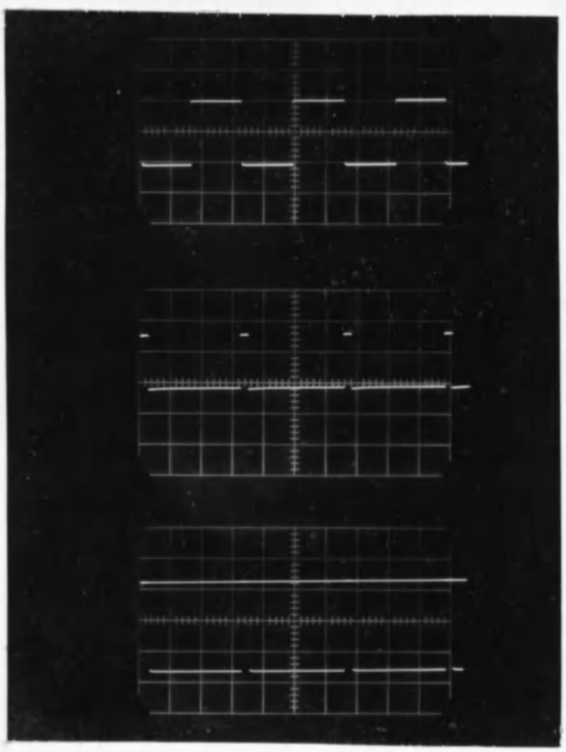


FIGURE 4.6 VERTICAL SIGNALS
(sweep = 5ms/cm)
(Scope sync. with vertical sync pulse)

a. 61.5 cps Vertical Scan Frequency
(amplitude = 20v/cm)

b. 61.5 cps Vertical Sync and Reset Pulse
(amplitude = 50v/cm)

c. 61.5 cps Vertical Count Signal
(amplitude = 20v/cm)

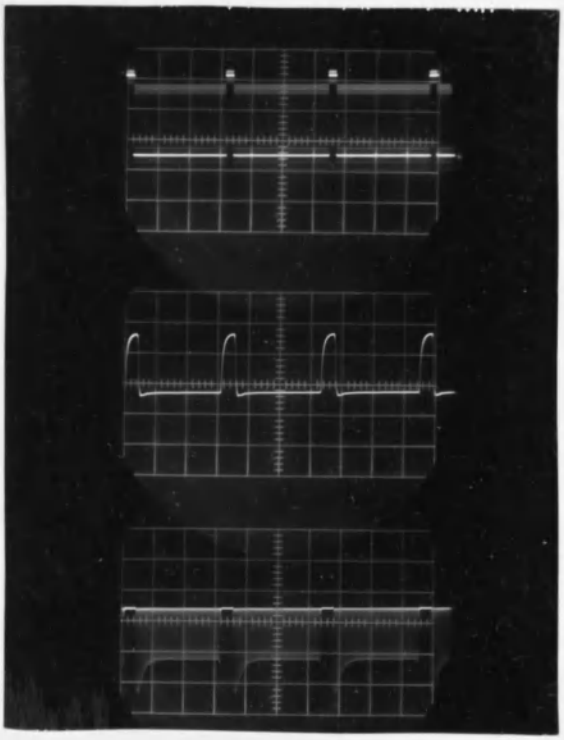


FIGURE 4.7 HORIZONTAL SIGNALS

a. Composite Sync Signal
(sweep = 5 ms/cm)
(amplitude = 2v/cm)
(Scope sync. to vertical sync pulse)

b. Horizontal Sync and Reset Pulse
(sweep = 20 μs/cm)
(amplitude = 50v/cm)
(Scope sync. to horizontal sync pulse)

c. Horizontal Count Signal
(sweep = 20 μs/cm)
(amplitude = 20v/cm)
(Scope sync. to horizontal sync pulse)

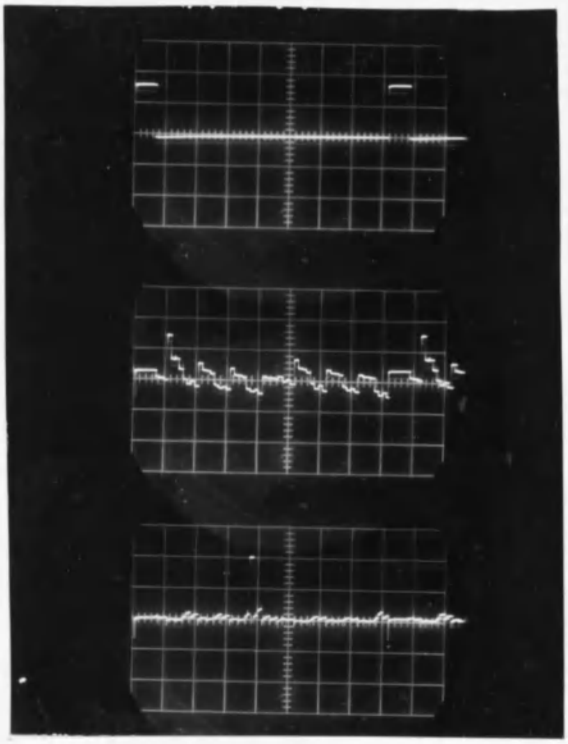


FIGURE 4.8 LOGIC SIGNALS
(sweep = 2 ms/cm)
(Scope sync. to vertical sync pulse)

a. Vertical Sync Pulse
(amplitude = 50v/cm)

b. Logic Circuit Output
(amplitude = 5v/cm)

c. Vertical Axis Pulse
(amplitude = 20v/cm)

However, these pulses cause the two line appearance.

The composite sync signal is shown in Figure 4.7a. Again, the horizontal sync pulses are not shown too clearly. A picture of the horizontal sync pulses is shown in Figure 4.7b. The last picture of Figure 4.7c shows the composition of the horizontal count signal.

The verification of the logic of displaying data in the manner described is shown in Figure 4.8a. The oscilloscope, in this case, was synchronized to the vertical sync pulse. This pulse is also shown in the photograph to provide a time reference. The two important results are shown in b and c of Figure 4.8.

Figure 4.8b shows the output of the diode logic circuit for a signal placed in on channel 3. Close examination will show the time when the counter is reset to zero and the switching performance of the logic circuits. The largest pulse represents the point to be printed. It can be removed from the other extraneous signals by biasing the following stages properly.

The pulse of Figure 4.8c represents the Y-axis. Since this signal is derived through one level of diodes, it is considerably clearer.

4.3 Design Limitations and Problems

This section is presented to indicate the nature of problems which were observed during construction and testing. The synchronizer uses divide-by-8 and 4 circuits which are astable multivibrators driven in synchronism. The design of these is subject to tube cut off characteristics which vary from tube to tube and with aging. These circuits are also very sensitive to the amplitude of the trigger signal. A complete investigation into these division circuits is warranted if optimization and reliability are to be achieved.

The diode circuits connected in cascade will require a low impedance driving source if used at the higher frequencies required for the X-signal generator. Additional problems of waveform preservation or generation are to be expected at higher frequencies.

The method of resetting the counters used is not attractive since a tube is required for every binary used. Another method discovered after construction had been completed, is to connect the grid return of all the binaries to a cathode follower of low impedance. A positive pulse would provide resetting.

CHAPTER 5

A PRACTICAL APPLICATION

5.1 Introductory Remarks

In order to appreciate the value of the display extended, a discussion is offered here on the method and type of display which might be obtained for a particular design problem.

The practical problem selected was an analysis of the pulse waveform of a hard tube modulator. The appendix contains the mathematical derivation of the equations which describe the pulse. Inspecting the equations and their restrictions will show that this problem would be difficult to program on an analogue computer. A digital computer can perform the calculations readily and accurately. The resultant output would be a number of points. The display device described could present these points in an accurate representation of the waveform.

Once the waveform is obtained, the design engineer must analyze it to obtain the information needed to intelligently select circuit components to perform the modulation. The maximum excursions define the peak ratings which the components must withstand. The power requirements and dissipations can be obtained by integration of the area under the given curve and others of the circuit which could be calculated in a similiar fashion.

5.2 Description of the Display

The waveform which would be printed on the cathode ray tube by points obtained in the manner described would appear similar to the one in Figure 5.1. The true plot of the waveform appears in Figure 5.2. The appearance of the display curve was obtained by the following analysis.

A 17-inch television set has a picture area which can be approximated by considering the picture equal to that defined by the aspect ratio. Then,

$$(3x)^2 + (4x)^2 = 17^2$$

$$25x^2 = 17^2$$

$$x = \frac{17}{5}.$$

where

$$\text{height} = \frac{3 \times 17}{5} = 10.2 \text{ inches}$$

$$\text{width} = \frac{4 \times 17}{5} = 13.6 \text{ inches}.$$

The plot was scaled by 1/2 in order to fit the curve on the paper. The display area of Figure 5.1 would be about 5.1 inches by 6.8 inches. This area was then subdivded into a matrix of 50 x 50. The point display was generated by superimposing the true curve on the matrix and noting a coincidence of the X and Y lines. This implies that only whole numbers of X and Y are processed from the computer and represents a condition of a few number of points displayed. This method of displaying points is similar to the manner in which curves are manually plotted.

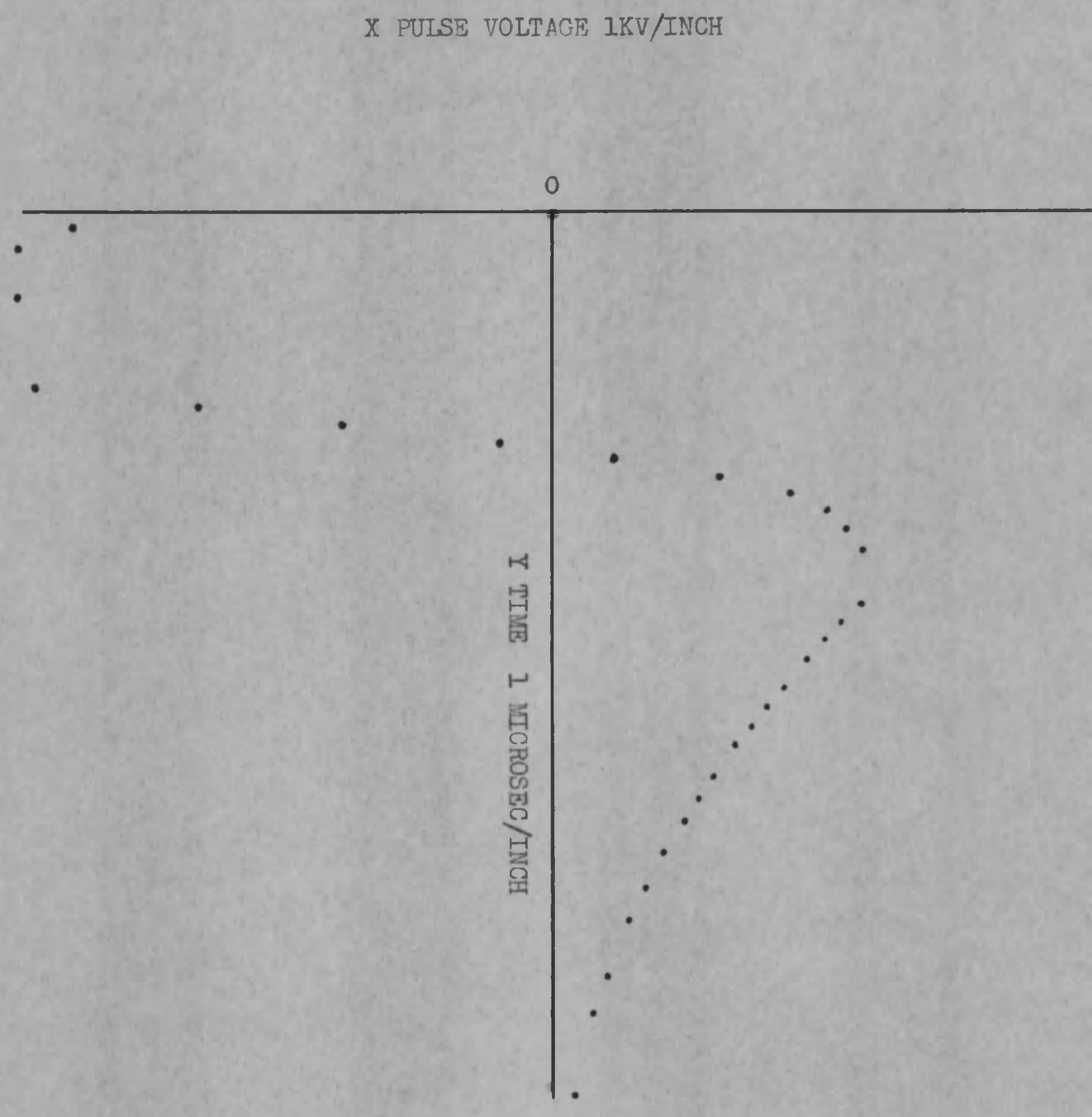


FIGURE 5.1 DISPLAY OF HARD TUBE MODULATOR PULSE

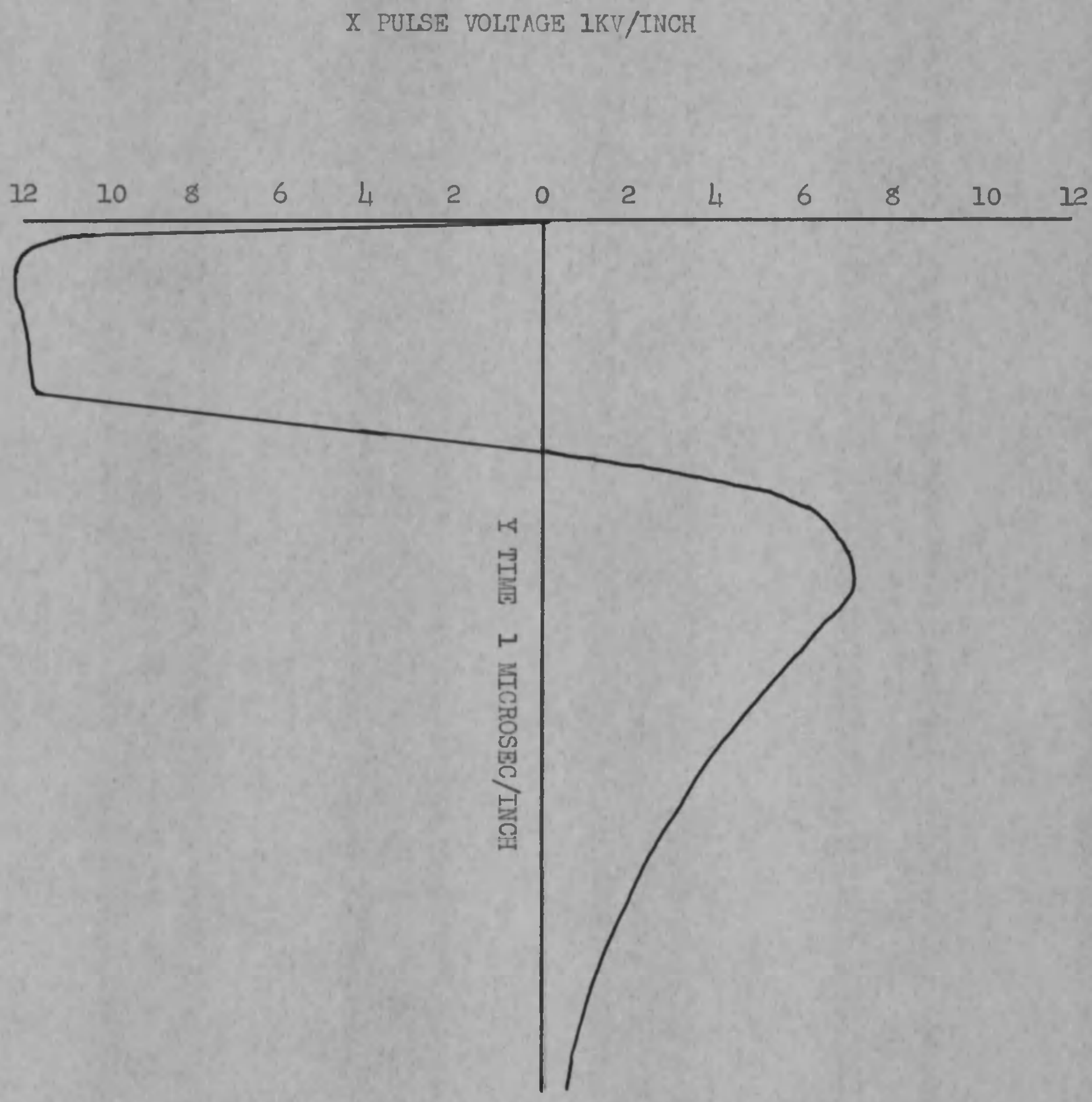


FIGURE 5.2 COMPUTED HARD TUBE MODULATOR PULSE

Increasing the number of quantizing intervals would provide a smoother and more defined curve. However, mechanization problems would increase.

5.3 Data Transfer

For the use described here, the data is visualized as being calculated and transferred to the display unit in the following fashion.

The computer would be programmed to perform the operations of the mathematical equations over the range of 0 to 5 microseconds. Since 50 intervals are desired, the Y increment would be $\frac{5}{50} = 0.1$ microsecond. The computer would start at Y = 0 and proceed to calculate the X or pulse voltage value. The time required to perform the calculation depends on the number of mathematical operations which have to be performed. These calculations can be performed during the active portion of the horizontal sweeps and the results transferred to the display input registers during the retrace interval. If more time to perform the calculations is required, the vertical sweep interval can be used. The X data then would be transferred on successive sweeps.

Any scaling required would be accomplished in the digital computer.

CHAPTER 6

CONCLUSIONS

6.1 Review of Approach

A display system capable of displaying digitally processed data was defined. The system requirements were examined and the design established. The logic which was needed for mechanization was developed, constructed, and tested. Finally, a practical use of the display was presented.

6.2 Conclusive Statements

The study made on the display system based on quantizing the horizontal and vertical sweep signals of a television cathode ray tube showed that the idea is feasible and practical. The mechanization of the logic circuits provided signals which were commensurate with the theory.

Several apparent advantages exist for the display system described over those using digital-to-analog conversion. One such advantage would be the use of an existing display device, the television cathode ray tube, to present data from digital systems. No special deflection and display system has to be developed.

Another advantage over analog systems is that precision components are not required. Thus, the display drift and stabilization problems are minimized.

Other comparisons with analog display systems as to the speed of processing, the ease of mechanization, the linearity and accuracy of the display, would be revealed by the evaluation of a complete system.

The system extended provides many new possibilities for experimentation. The use of the device as the output of a digital system in the field of graphical display and analysis would be a great aid in the communication of information.

CHAPTER 7

SUGGESTIONS FOR FURTHER STUDY

7.1 Graphical Interpretations of Computer Results

Additional work is required in order to fully realize the display system conceived. Some of the problems associated with the mechanization of the entire system have been discussed in Chapter 4, Section 4.3.

Once the system is established, experimentation can be conducted into the many areas of interest. This thesis has been mainly concerned with the graphic interpretation of computer results. Besides investigation into different techniques of display, equipment investigation can be conducted. A possibility of obtaining the integral of a function by the counting of the coincident, weighted pulses exists.

7.2 Additional Areas

Other areas which may be investigated for possible uses of the display system are:

(1) Multiple representation or overlay of information. Since the cathode ray tube is scanned, it is conceivable that information from various sources can be presented over one another by time sharing techniques. A possibility of superimposing video and computer signals exists.

(2) Real time display. Flight patterns and traffic flow can be displayed.

(3) Alphanumeric readout of computer data. Computer output information can be visually observed.

(4) Tabulation of computer results.

(5) Reduction of test data by elimination of undesirable or unwanted data.

(6) Human engineering investigation in visual perception and related topics.

(7) Simulation of video presentations.

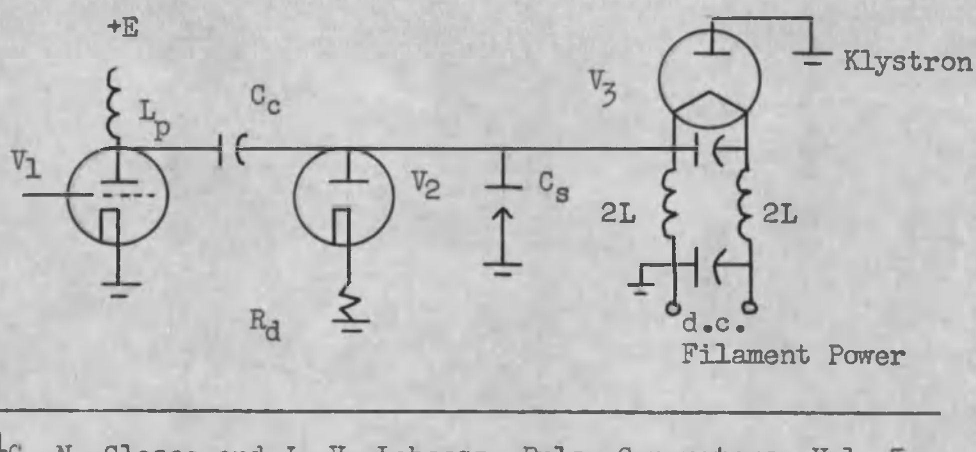
APPENDIX

WAVEFORM ANALYSIS

A familiar circuit in radar systems which require multiple pulses at short time intervals is the hard tube modulator. This circuit supplies the high voltage video pulse needed by either magnetrons or klystrons to generate the radio frequency pulses.

In the development of any new radar system requiring hard tube modulators, it is essential to analyze that circuit in order to be able to specify the components needed. Such an analysis is necessary since the components are usually special items which are not normally available or which must be designed.

The analysis which follows is original. However, reference was made to the excellent treatment of modulators by Glasoe and Lebacqz[1]. The circuit of a hard tube modulator can be represented as:



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[1] G. N. Glasoe and J. V. Lebacqz, Pulse Generators, Vol. 5, Radiation Laboratory Series, McGraw-Hill Book Co., Inc., 1948

The circuit components and parameters are:

V_1 = Switch tube

V_2 = Inverse diode

V_3 = Klystron

C_s = Stray capacity

C_c = Coupling capacity

L = Shunt inductors - permits development of pulse across the klystron while permitting d.c. filament flow

R_k = Load resistance offered by V_3

r_p = Plate resistance of V_1

L_p = Charging inductor

In the analysis, the nonlinearities of the R_k and r_p were neglected. In addition, L_p was assumed to be so large that no current flows from the power supply during the pulse time. Also, C_c was assumed to be large. Therefore, it could be replaced by a battery.

This circuit can be analyzed by considering the three sequential modes of operation. They are as follows:

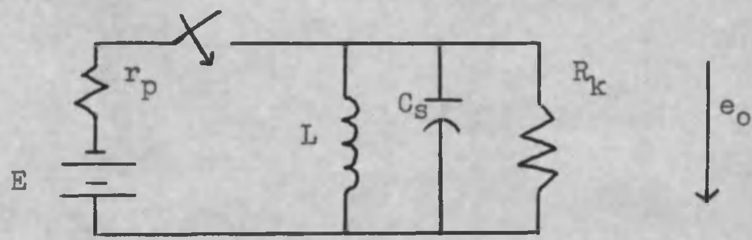
(1) The switch tube is turned on

(2) The switch tube is turned off

(3) The inverse diode conducts.

(1) Switch tube on

The equivalent circuit becomes:



$$\frac{E - e_o}{r_p} = \left(\frac{1}{L_p} + C_{sp} + \frac{1}{R_k}\right) e_o$$

then

$$e_o = \frac{E}{r_p \left(\frac{1}{L_p} + C_{sp} + \frac{1}{R_{eq}}\right)} \qquad \text{where } R_{eq} = \frac{r_p R_k}{r_p + R_k}$$

Using Laplace Transforms,

$$E_o(s) = \frac{E}{r_p C_s} \qquad \frac{1}{\left(s^2 + \frac{s}{R_{eq} C_s} + \frac{1}{C_s L}\right)}$$

let

$$a = \frac{1}{2\, R_{eq} C_s} + \frac{1}{2}\sqrt{\left(\frac{1}{R_{eq} C_s}\right)^2 - \frac{4}{C_s L}}$$

$$b = \frac{1}{2\, R_{eq} C_s} - \frac{1}{2}\sqrt{\left(\frac{1}{R_{eq} C_s}\right)^2 - \frac{4}{C_s L}}$$

then

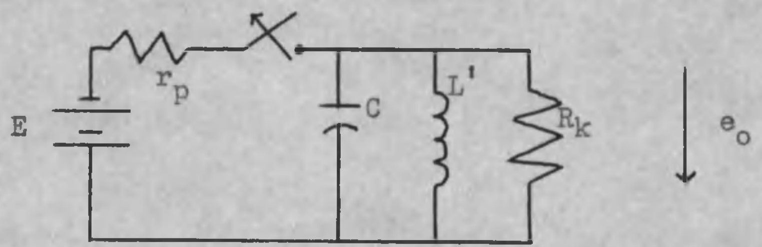
$$E_o\,(s) = \frac{E}{r_p C_s}\left(\frac{A}{s + a} + \frac{B}{s + b}\right)$$

$$= \frac{E}{r_p C_s}\left(\frac{\frac{1}{b - a}}{s + a} - \frac{\frac{1}{b - a}}{s + b}\right)$$

or

$$e_o\,(t) = \frac{E}{r_p C_s \sqrt{\left(\frac{1}{R_{eq} C_s}\right)^2 - \frac{4}{C_s L}}}\left[e^{-at} - e^{-bt}\right] \quad (1)$$

(2) Switch tube off



where

$L' = \frac{L L_p}{L_p + L}$, E_p = value of voltage across C at time of switching, and τ = pulse width

$$i_{L'} + i_c + i_R = 0$$

$$\frac{e_o}{L' p} + pCe_o + \frac{e_o}{R} = 0$$

or

$$\frac{E_o'(s)}{L's} + \frac{\int_0^{\tau} E_o(\tau)\,dt}{L'(s)} + sCE_o(s) - CE_p + \frac{E_o(s)}{R_k} = 0$$

$$E_o(s)\left[\frac{1}{L's} + sC + \frac{1}{R_k}\right] = CE_p - \frac{\int_0^{\tau} E_o(\tau)\,dt}{L's}$$

$$E_o(s) = \left(\frac{1}{\frac{1}{L's} + sC + \frac{1}{R_k}}\right)\left[CE_p - \frac{K}{L's}\right]$$

where K is the value of the first integration of E_o (t) obtained in part (1) evaluated at $t = \tau$. Then,

$$K = \frac{E_p}{r_pC_s}\left[\frac{1}{ab} + \frac{1}{a(a-b)}e^{-a\tau} - \frac{e^{-b\tau}}{b(a-b)}\right]$$

$$E_o(s) = \frac{E_o\left(s - \frac{K}{E_pCL'}\right)}{S^2 + \frac{1}{R_kC}S + \frac{1}{L'C}}$$

let

$$a' = +\frac{1}{2R_kC} + \frac{1}{2}\sqrt{\left(\frac{1}{R_kC}\right)^2 - \frac{4}{L'C}}$$

$$b' = +\frac{1}{2R_kC} - \frac{1}{2}\sqrt{\left(\frac{1}{R_kC}\right)^2 - \frac{4}{L'C}}$$

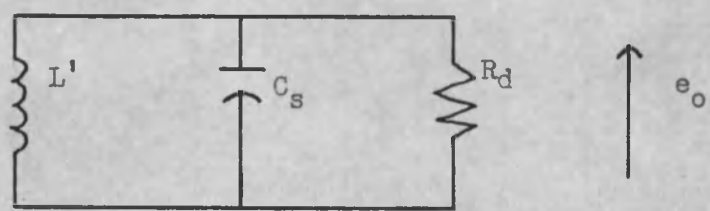
and

$$q = - \frac{K}{E_p C L'}$$

$$E_o\ (s) = \frac{E_p\ (s + q)}{(s + a')(s + b')}$$

$$e_o\ (t) = E_p \left[\frac{(q - a')\ e^{-a't} - (q - b')\ e^{-b't}}{b' - a'} \right] \qquad (2)$$

(3) Inverse diode on



$$\frac{e_o}{R_d} + Cpe_o + \frac{e_o}{L'p} = 0$$

$$\frac{E_o\ (s)}{R_d} + C_s E_o\ (s) + \frac{E_o\ (s)}{L's} + \frac{\int_0^{t_1} e_o\ (t)\ dt}{L's} = 0$$

$$E_o\ (s) = - \frac{\int_0^{t_1} e_o\ (t_1)\ dt}{L's} \left[\frac{1}{\frac{1}{R_d} + C_s + \frac{1}{L's}} \right]$$

$$= \frac{-\int_0^{t_1} e_o\,(t_1)\,dt}{CL'} \qquad \frac{1}{s^2 + \frac{s}{CR_d} + \frac{1}{L'C}}$$

where t_1 is evaluated from considering the $e_o\,(t)$ of (2)

or

$$0 = (q - a')\,e^{-a't_1} - (q - b')\,e^{-bt_1}$$

$$0 = \ln\,(q - a') - a't_1 - \ln\,(q - b') + b't_1$$

and
$$t_1 = \frac{\ln \frac{(q - a')}{(q - b')}}{b' - a'}$$

then
$$\int_0^{t_1} e_o\,(t_1)\,dt = K_1 + E_p \left[\frac{q}{a'b'} + \frac{(q - a') + e^{-a't_1}}{a'\,(a' - b')} + \frac{(q - b')\,e^{-b't_1}}{b'\,(b' - a')} \right] = K_2$$

then

$$E_o\,(s) = \frac{-K_2}{CL'} \left[\frac{1}{(s + a_2)(s + b_2)} \right]$$

$$e_o\,(t) = \frac{-K_2}{CL'} \left(\frac{e^{-b_2t} - e^{-a_2t}}{a_2 - b_2} \right) \qquad (3)$$

Equations (1), (2) and (3) describe the output pulse which will be obtained. Other equations for currents and voltages through the other components can also be derived. A complete analysis would present detailed information needed to specify such things as tube ratings, efficiency, power requirements, etc.

Using the voltage equations derived, the output waveform for the following typical parameters was calculated.

Let r_p = 100 ohms	C_e = 4000 micro-microfarad
τ = 1 microsecond	E = 13,000 volts
R_k = 12,000 ohms	C_s = 50 micro-microfarad
L = 13 millihenries	R_d = 7000 ohms (Critically damped case)
L_p = 40 millihenries	

The output waveform is shown plotted in Figure 5.2.

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