THE ANALYSIS OF A TRANSISTORIZED FAST RISE BLOCKING OSCILLATOR

By

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June 30, 1960

Date

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The author is grateful to the Sprague Electric Company which constructed several pulse transformers specifically for this thesis and to Motorola, Inc., which supplied the transistors. Thanks are also extended to over fifty other companies which supplied information and material for this thesis.

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LIST OF ILLUSTRATIONS

LIST OF SYMBOLS

Symbol	Identification
a	A general constant
α	Common-base short-circuit current-amplification factor
α_o	Low-frequency α
α_r	Reverse α
b	A general constant
c	A general constant
C_c	Collector-junction capacitance
C_e	Emitter-junction and diffusion capacitance
D_n	Diffusion constant for electrons
i_b	Base current (upper case I indicates d-c value)
i_c	Collector current (upper case I indicates d-c value)
I_{cd}	Collector current due to diffusion through base
i_{CR}	Closed collector-base diode current
$i_{CR}(0)$	Initial value of i_{CR}
i_e	Emitter current (upper case I indicates d-c value)
i_m	Instantaneous magnetizing current

k	Coefficient of coupling
L	Equivalent magnetizing inductance ($k^2 L_p$)
L_p	Magnetizing inductance
λ	Series leakage inductance
m	Turns ratio
μ	Damping ratio
n	Turns ratio
n_o	Optimum turns ratio
ns	Nanosecond (millimicrosecond)
ω_c	Alpha-cutoff frequency (radians per second)
ω_n	Undamped natural angular frequency
Ω	Sag
pf	Picofarad (micromicrofarad)
r_b	Intrinsic base resistance
r_e	Emitter resistance
s	Laplace operator
t_f	Pulse fall time
t_r	Pulse rise time
t_s	Storage time
t_w	Pulse width
γ	Lifetime, time constant

V_{BB}	Base circuit battery voltage
V_{BE}	A d-c emitter-to-base bias voltage
V_{cc}	Collector circuit battery voltage
v_{CB}	Instantaneous total collector-to-base voltage
v_{EB}	Instantaneous total emitter-to-base voltage
W	Effective base width

Chapter 1

INTRODUCTION

1.1 STATEMENT OF THE PROBLEM

The junction-transistor blocking oscillator is a circuit used to generate short pulses with small rise times. It is a one-transistor circuit which is faster than conventional two-transistor pulse circuits such as multivibrators. It is a regenerative circuit which produces pulses of fairly constant shape when actuated by a variety of different triggers or when self-cycled. It is essentially a single stage amplifier with positive feedback.

In order to achieve proper operation, the blocking oscillator circuit must contain three essential elements: (1) an amplifying element which makes possible the regenerative responses; (2) a non-linear element to terminate regeneration and control circuit stability; and (3) a magnetic storage element. In the case of the transistor blocking oscillator, the transistor supplies elements (1) and (2) and element (3) is furnished by the pulse transformer.

These circuit elements define the pulse response to be attained from the blocking oscillator. It is the purpose of this thesis to

ascertain both analytically and experimentally the scope of each element's influence on the circuit pulse response with particular emphasis on switching performance.

The ingress of high alpha cutoff frequency transistors and fast rise pulse transformers into industry has facilitated the design of extremely fast blocking oscillators but has also brought new analytical complications. To avoid these, a set of analytical equations must be developed which are based on a succession of cogent approximations and which allow a fairly simple design procedure to be developed for fast rise blocking oscillators.

1.2 NEED FOR REGENERATIVE FAST RISE PULSES

The simplicity of the blocking oscillator and its suitability in producing square output pulses make it a useful component in pulse systems. For instance, the blocking oscillator output may be used as a gating waveform with a very short switching time. Or it may be used in ring counters and frequency dividers with great economy. It is especially useful in regenerative pulse amplifiers and pulse generators or as a monostable circuit to obtain abrupt pulses from a slowly varying input triggering voltage. It can be used as a low impedance switch to discharge a capacitor quickly as in storage counters or as a master oscillator to supply triggers for synchronizing a system of pulse-type waveforms. These and many other applications point up the importance of the blocking oscillator in pulse circuits.

In many of these applications, a pulse with a fast rise time

is extremely important. The faster the rise time, the more accurate and valuable is its role in the circuit. It is for this reason that emphasis is placed in this thesis on those circuit parameters which influence the blocking oscillator pulse rise time and on design techniques which enhance this switching speed.

1.3 GENERAL APPROACH TO THE PROBLEM

The initial problem is to clarify the basic circuit operation of the transistor blocking oscillator. With this as the starting point, the basic circuit concepts then become the building blocks for any comprehensive analytical study of the blocking oscillator.

After the basic circuit operation is clarified, the transistor and pulse transformer can be considered separately and analyzed from the standpoint of high frequency response. With the results of this analysis, the most desirable blocking oscillator circuit configuration for fast response can be selected.

Then the task of analyzing the total blocking oscillator circuit can be undertaken with the analytical results of the separate components as the foundation. Equations can be developed to analytically describe the circuit behavior for various conditions of triggering, loading, and transformer turns ratio. These equations can be modified, by appropriate approximations, to a workable form. Then experimental substantiation of these design equations can be instituted.

Finally, conclusions can be evolved which indicate the validity of the developed analytical equations on the basis of the experimental results, and which evidence the worth of those equations.

1.4 REVIEW OF LITERATURE AVAILABLE ON THE SUBJECT

The realization of the importance of the transistor blocking oscillator in pulse circuits has produced numerous articles on the subject in technical literature. However, since it is still a relatively new and narrow subject, most of these articles and sections of text-books are based on a mere handful of really creative and contributory articles. Only this type of reference is discussed here.

An early work by Ebers and Moll[1] analyzes the large-signal characteristics of junction transistors. This analysis is helpful in understanding and predicting the behavior of the transistor in the blocking oscillator circuit. The transition of the transistor switch from open to closed, or vice versa, is discussed as well as the effects of minority carrier storage. Equivalent circuits for the transistor are developed for all regions of operation and the impact of this development is still evident in most of the recent treatments of transistor switching circuits.

In another article, Moll[2] deals only with the transient response of the transistor in the active region. The transistor small-signal characterization is used to calculate switching and storage times. The

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[1] J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors," Proc. of the IRE, Dec., 1954, pp. 1761-1772.

[2] J. L. Moll, "Large-Signal Transient Response of Junction Transistors", Proc. of the IRE, Dec., 1954, pp. 1773-1784.

methods employed in this article form the basis for most new approaches to the transistor switching-time problem.

The most important work, relevant to this thesis, is done by Linvill and Mattson.[3] This article develops approximants for the transistor blocking oscillator in its various stages of operation and performs an analysis of these approximants. From this analysis, analytical expressions are evolved which describe circuit response to various triggers, loads, and turns ratios. These expressions are then validated experimentally. The real significance of this work is in lighting the way to approximating methods in blocking oscillator analysis.

An analytical method which differs significantly from previous approaches is devised by Narud and Aaron.[4] This analysis deals with the nonlinear dependence of collector current and base voltage upon base current. Unfortunately, the nonlinear differential equations governing circuit performance which are derived require analog and digital computer solutions. In other words, the results are splendid from a theoretician's standpoint, but are much too cumbersome to be used in design and for that reason this work is almost totally ignored in this thesis.

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[3] J. G. Linvill and R. H. Mattson, "Junction Transistor Blocking Oscillators," Proc. of the IRE, Nov., 1955, pp. 1632-1639.

[4] J. A. Narud and M. R. Aaron, "Analysis and Design of a Transistor Blocking Oscillator Including Inherent Non-Linearities," Bell System Technical Journal, Vol. XXXVIII, May, 1959, pp. 785-852.

As the transistor blocking oscillator is adapted for use in new applications, the need for extension of these basic ideas and neoteric thinking in terms of circuit adjustments arises. As a result, several new approaches to the analysis of transistor blocking oscillators have been developed which are useful in this present treatment. Typical among these is an article by Hamilton[5] which develops a design procedure for using blocking oscillators as a building block in digital systems. This design method virtually precludes variations of pulse shape with changing transistor parameters.

There are, of course, numerous other articles and books which enhance the contributions of the works mentioned above. Many of these will be listed in the Bibliography and referenced in the text of this thesis.

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[5] D. J. Hamilton, "A Transistor Pulse Generator for Digital Systems," IRE Transactions of Electronic Computers, Vol. EC-7, Sept., 1958, pp. 244-249.

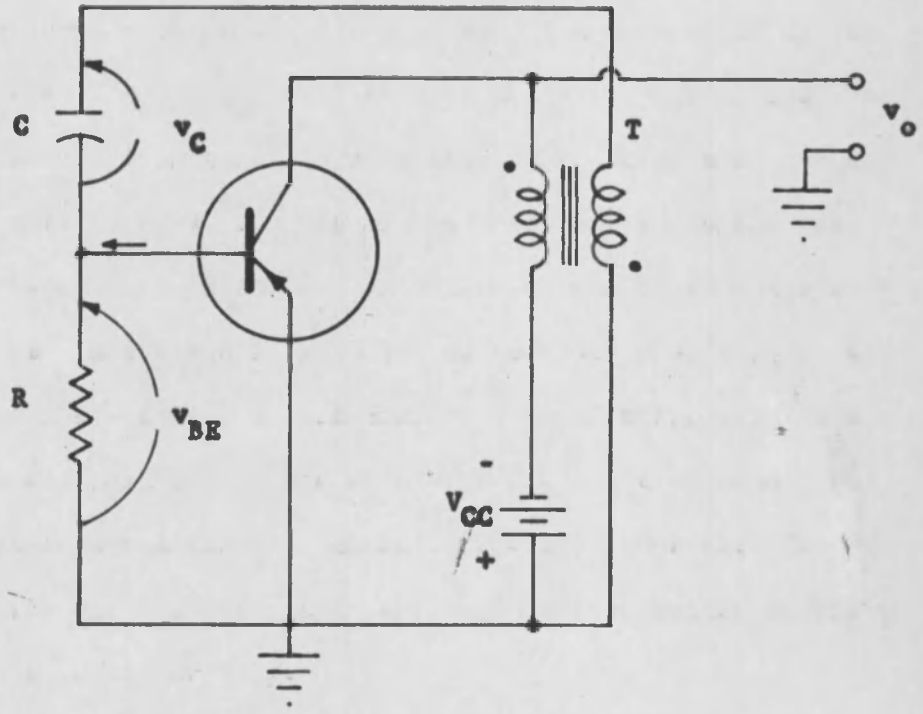
Chapter 2

THE BASIC TRANSISTOR BLOCKING OSCILLATOR

2.1 FREE RUNNING BLOCKING OSCILLATORS

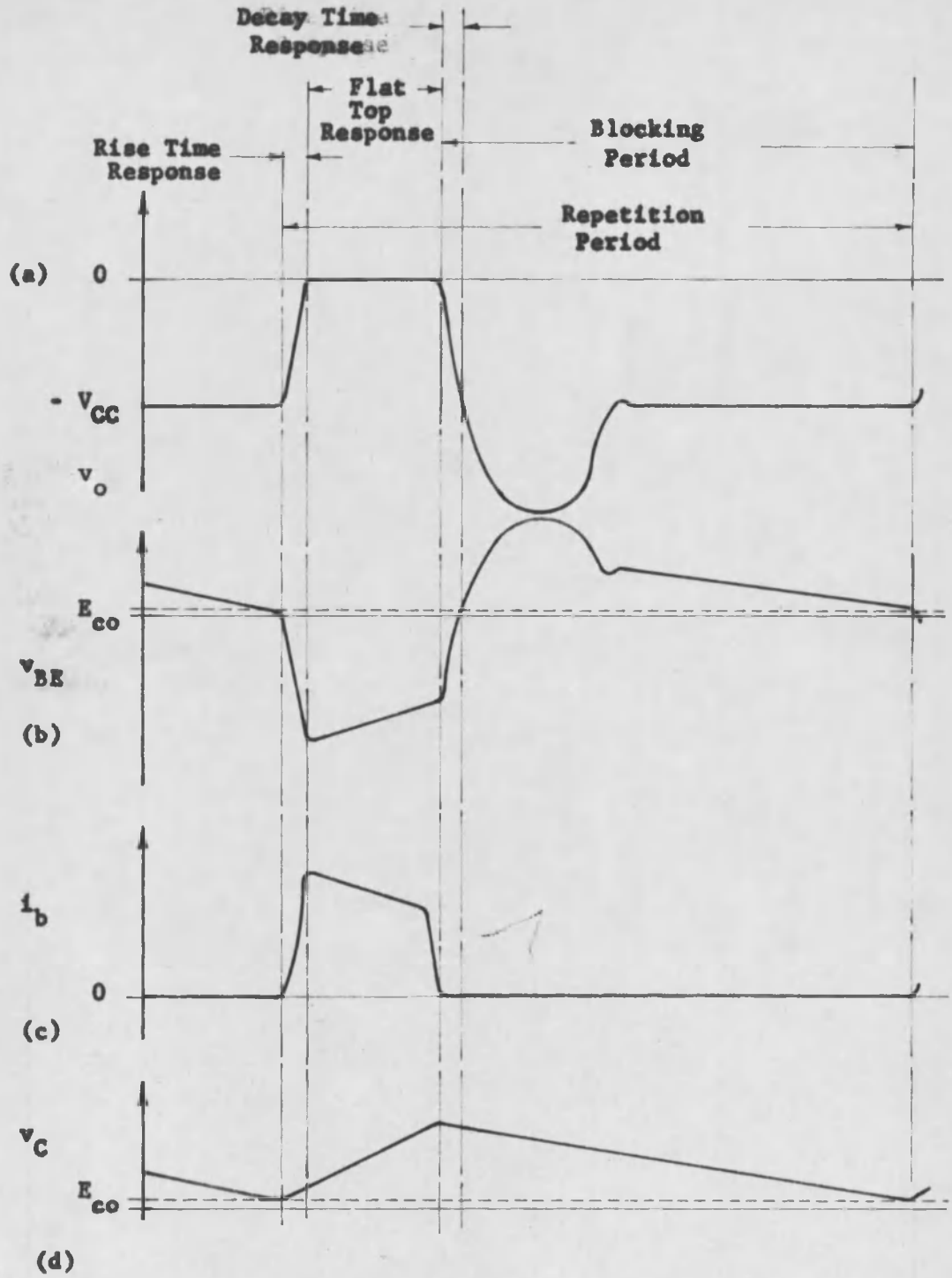
One circuit arrangement for an astable, common emitter, PNP junction-transistor blocking oscillator is shown in Figure 2.1. When the circuit is energized there is a forward bias established between the base and emitter by V_{CC}. This causes a rapid rise in the base driving current which in turn increases the current flow in the collector circuit. This increasing collector current induces a negative voltage in the base-winding of transformer T which charges capacitor C through the small forward resistance of the base-emitter diode, and appears across this resistance increasing the forward bias. When the loop gain of the circuit exceeds unity, regenerative action causes the transistor to saturate rapidly.

At saturation, the collector current stops increasing and the induced voltage in the base winding of transformer T decreases to zero. Capacitor C now discharges through resistor R. The field in the transformer base winding collapses and induces a voltage in the winding in the reverse direction causing a reversed base bias. The base current decreases and through regenerative action quickly drives the collector current to cutoff. The transistor is held at cutoff until capacitor C,



ASTABLE BLOCKING OSCILLATOR

Figure 2.1



WAVEFORMS IN THE BLOCKING OSCILLATOR

Figure 2.2

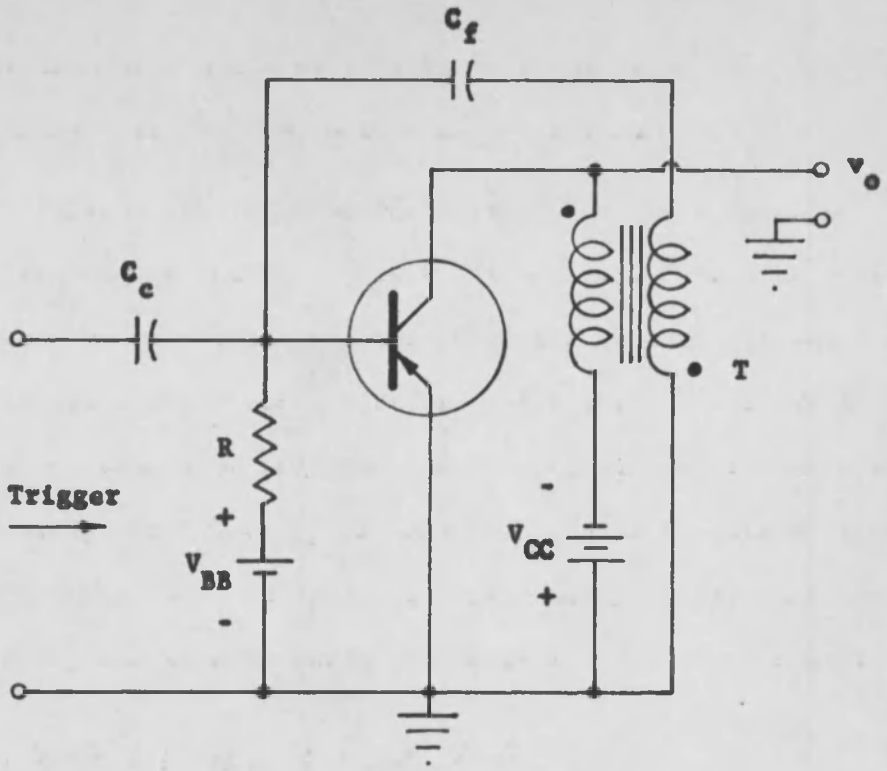
discharging through resistor R, reaches the point at which the transistor is forward-biased and conduction begins again.

Typical waveforms of the circuit operation are shown in Figure 2.2. Parameter notation refers to Figure 2.1. The rise time and fall time response is governed by the pulse transformer characteristics and the high frequency characteristics of the transistor. These attributes are investigated thoroughly in Chapters 3, 4, and 5. The flat top period is primarily determined by the base winding of the transformer and will be examined in Chapters 4 and 5. The resting or blocking time is determined by the time constant of resistor R and capacitor C.

2.2 TRIGGERED BLOCKING OSCILLATORS

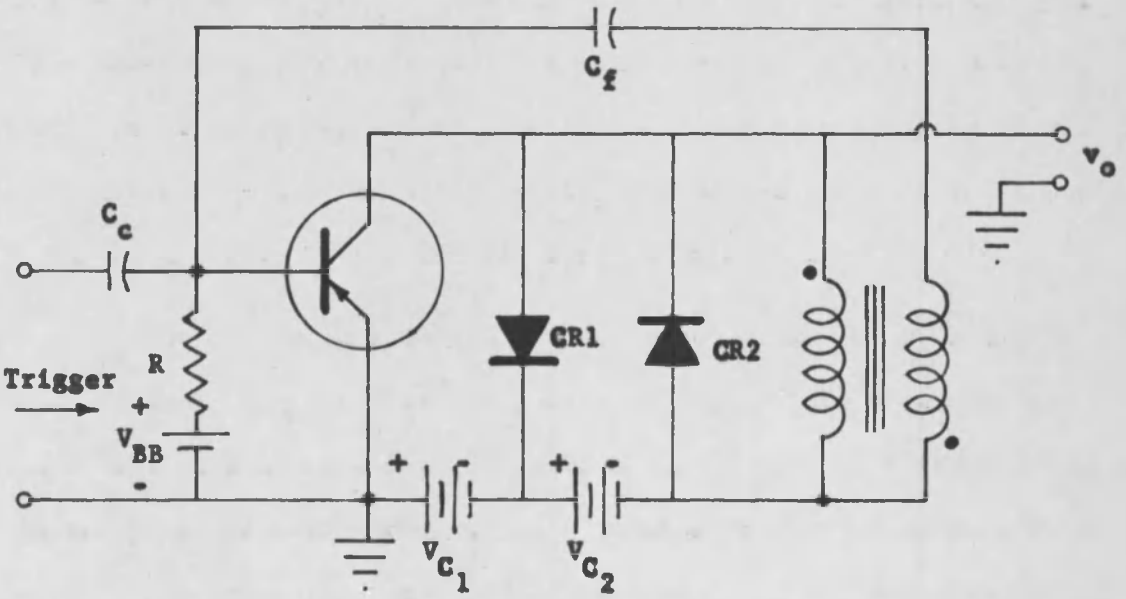
The blocking oscillator may be triggered from an independent source so that it produces one output pulse for each input trigger. This mode of operation is called a triggered or monostable blocking oscillator. A common emitter monostable circuit is shown in Figure 2.3. It differs from the astable circuit in Figure 2.1 in that the transistor is held at cutoff by the reverse bias voltage V_{BB}.

The application of a negative pulse at the input initiates conduction in the transistor. Collector current flows through the collector winding of the pulse transformer inducing a voltage of opposite polarity in the base winding. This voltage is coupled through capacitor C_F and appears at the base of the transistor. Regenerative action continues as in Section 2.1 until the transistor is driven into saturation.



Triggered Blocking Oscillator

Figure 2.3



Nonsaturating Blocking Oscillator

Figure 2.4

At this point the collector current ceases to increase and regenerative feedback terminates. The reverse bias provided by V_{BB} cuts off the transistor but the collector current continues to flow for a short while because of minority carrier storage.

When the collector current ceases to flow, the collapsing field around the base winding of the transformer induces a voltage in the collector winding which backswings beyond the collector-base junction bias voltage V_{CC} (see Figure 2.2 (a)). This backswing voltage may possibly exceed the collector breakdown voltage of the transistor. In addition, driving the transistor into the saturation region, introduces the undesired effect of minority carrier storage which is treated in Section 3.2. These two effects can be precluded by the use of clamping diodes as in the circuit shown in Figure 2.4. This circuit is a common emitter version of the common base configuration employed by Linvill and Mattson[1] in their classic treatment of junction transistor blocking oscillators which forms the foundation for the analysis of Chapter 5.

The theory of operation of this circuit is similar to that described for the circuit in Figure 2.3. In the quiescent state, diode CR1 is reverse-biased and diode CR2 has no bias applied. A negative trigger pulse at the input initiates regeneration resulting

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[1] J. G. Linvill and R. H. Mattson, "Junction Transistor Blocking Oscillators," Proceedings of the IRE, November, 1955, pp. 1632-1633.

in a rapid increase in the collector current. The collector voltage rises from the negative combined value of V_{C_1} and V_{C_2} until the reverse-bias potential applied to diode CR1 reaches a value equal to V_{C_1}. Further increase of collector potential results in diode CR1 becoming forward-biased and it then maintains the collector voltage at the value of V_{C_1}. Since CR1 also acts as a short circuit to the collector winding of the transformer, the transistor is prevented from going into saturation. As the magnetic field on the transformer begins to collapse, the bias voltage across diode CR1 reverts to its nonconducting state when the value of V_{C_1} is exceeded.

The collector voltage continues decreasing until it reaches the value of $V_{C_1} + V_{C_2}$. At this point the induced voltage in the transformer attempts to decrease further the voltage at the collector, but CR2, which is conducting, prevents this from happening. Diode CR2 also serves to clamp out any oscillation after the pulse.

A critical question in this thesis is whether causing a diode to go into saturation to prevent the transistor from doing so is worthwhile or not. This question is considered in Chapters 5 and 6 from both the theoretical and practical aspects. The matter of protecting the collector junction from high inductive voltages if diodes are not used is readily handled by a judicious choice of transformer parameters as discussed in Chapter 4.

2.3 TRIGGERING CONSIDERATIONS

The triggering requirements for the blocking oscillator circuit in Figure 2.3 are not at all intractable if the output pulse requirements are not too rigid. Triggering may be readily accomplished by voltage pulses in the base circuit or current pulses in either the collector or emitter circuits. Linvill and Mattson[2] approach the triggering problem by comparing trigger source energy requirements of the various triggering modes to initiate the blocking oscillator regenerative cycle. The consequences of the various triggering mode source impedances is also considered. Yet another approach to the triggering problem will be undertaken in Chapter 5 whereby triggering mode selection is optimized to obtain fast rise pulses at the output of the blocking oscillator.

In the "garden-variety" transistor blocking oscillator, the trigger input, regardless of circuit constants, should have at least a few volts of amplitude and a rise time of somewhat less than 100 nanoseconds (millimicroseconds). The trigger duration (pulse width) should either be comparable to the rise time of the blocking oscillator output pulse or longer than the period of the blocking oscillator cycle. Since the former, in most cases, requires such a short pulse with extremely fast rise and fall times, the latter is predominantly used. If the duration of the trigger pulse is such that it is removed while

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[2] Ibid., pp. 1636-1637.

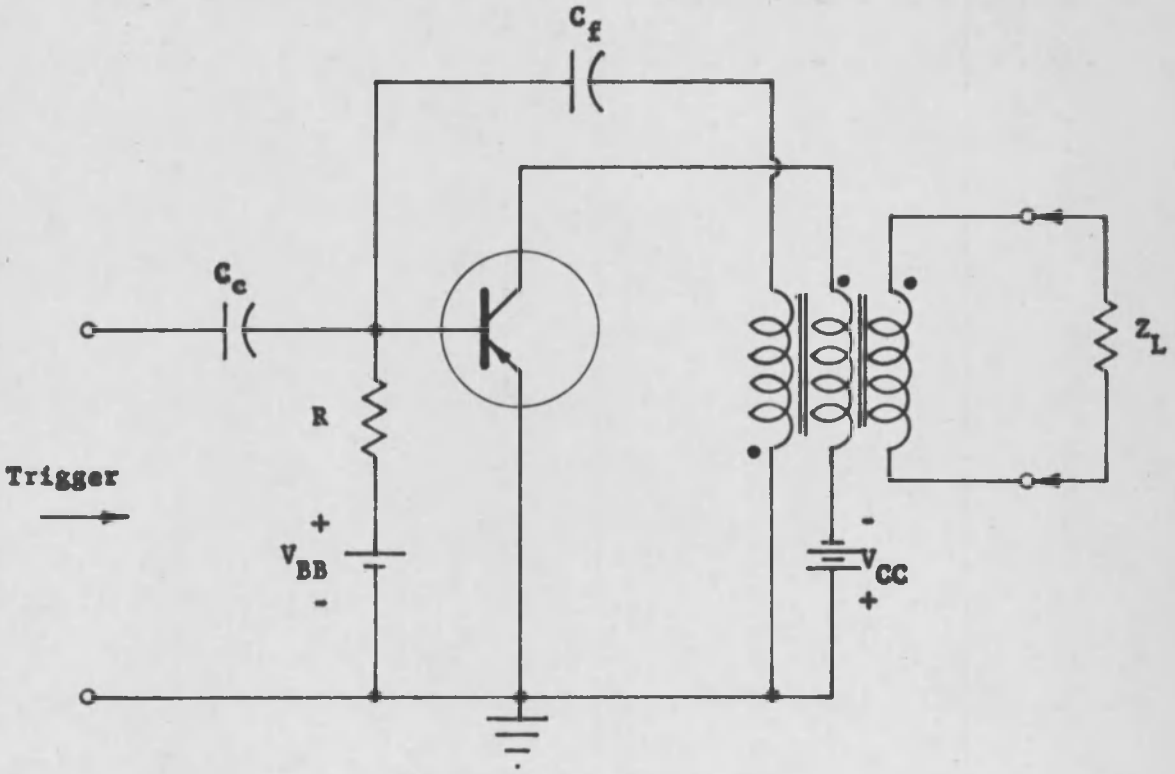
the output pulse top is being generated, an irregularity will occur in the output waveform at the time the input pulse fall time occurs. It is possible that this will halt the regenerative cycle. This phenomenon is investigated in Chapter 6. As can then be seen, if the trigger duration is wider than the output pulse, no detrimental results are evident and the circuit will still generate only one pulse for each trigger.

Trigger pulse rise time is extemely important if fast rise output pulses are desired. This aspect is treated at some length in Section 5.5 and experimental substantiation of this premise is given in Section 6.3. It is not necessary to match the trigger generator impedance to the input impedance of the blocking oscillator circuit since maximum transfer of power is not required here. Mismatch should not be so great, however, that the minimum trigger requirements are not met.

2.4 LOADING CONSIDERATIONS

The preceding sections of this chapter have dealt with blocking oscillators operating into an infinite load impedance. Since the practical blocking oscillator must operate into finite impedances, it is necessary to consider this parameter's effect on circuit performance. The load impedance can be placed across the v_o terminals in Figure 2.3 or inductively coupled to the output circuit as shown in Figure 2.5. A complete analysis of loading consequences on blocking oscillator performance is given in Chapter 5. It can be seen that

the cyclic evolution of the circuit remains essentially the same as in the case of an infinite load impedance, but that the switching time is slowed as a result of loading. A further impediment is the necessity of altering the transformer design as the load is changed in order to optimize the circuit switching speed. The experimental results of Chapter 6 point up the nature of these difficulties.



LOADED BLOCKING OSCILLATOR

Figure 2.5

Chapter 3

TRANSISTOR SWITCHING LIMITATIONS

3.1 LARGE-SIGNAL EQUIVALENT CIRCUITS

In preparing for the comprehensive circuit analysis of Chapter 5, equivalent circuits of the large-signal deportment of a junction transistor must be developed. This is done with as little committment to a specific circuit configuration as possible to allow facility for the choice of common base or common emitter in Chapter 5. When the transistor is used as a switch, as is the case with the blocking oscillator, it finds itself in three conditions of operation defined by Anderson[1] as follows:

Region I: collector current cutoff or collector voltage saturation,

Region II: active region, and

Region III: collector current saturation, or collector voltage cutoff

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[1] A. E. Anderson, "Transistors in Switching Circuits," Proc. of the IRE, Vol. 40, pp. 1541-1548, November, 1952

Approximate equivalent circuits of the transistor for these regions appear in Figure 3.1.

The NPN embodiment is employed here but the reasoning applies to the PNP type by merely changing polarity signs. During cutoff the transistor is essentially an open circuit as shown in Figure 3.1(a). In the active region the transistor behaves approximately as in Figure 3.1(b). Resistor r_e' is roughly the reciprocal of the appropriate $I_B - E_{BE}$ curve in the region of operation. During saturation, the transistor is a comparative short circuit as in Figure 3.1(c). Yet another region of operation which should be considered is when the emitter junction is reversed-biased and the collector junction is forward-biased. This is the reverse active region and is represented as in Figure 3.1(d).

The approximants in Figure 3.1 are useful as a conceptual aid but lack the verity required for the analysis in Chapter 5. There are several more rigorous equivalent circuits available in varying degrees of exactness. The one which lends itself most readily to the approach adopted in this treatment, while still maintaining rigor, is depicted in Figure 3.2,[2] where C_e combines emitter junction capacitance and diffusion capacitance, C_c is collector junction capacitance, and α_o is measured at low frequencies. The circuit in Figure 3.2 can now be

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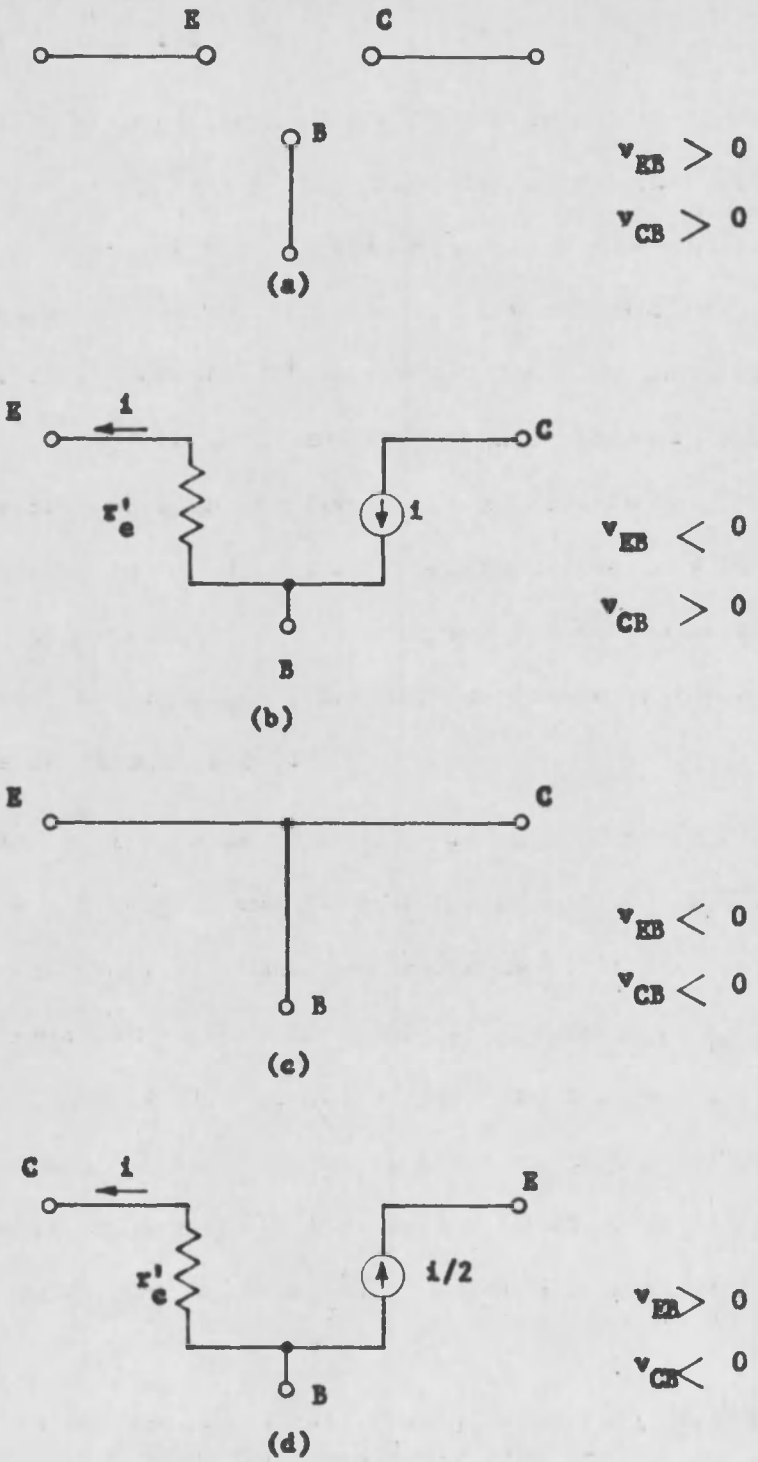
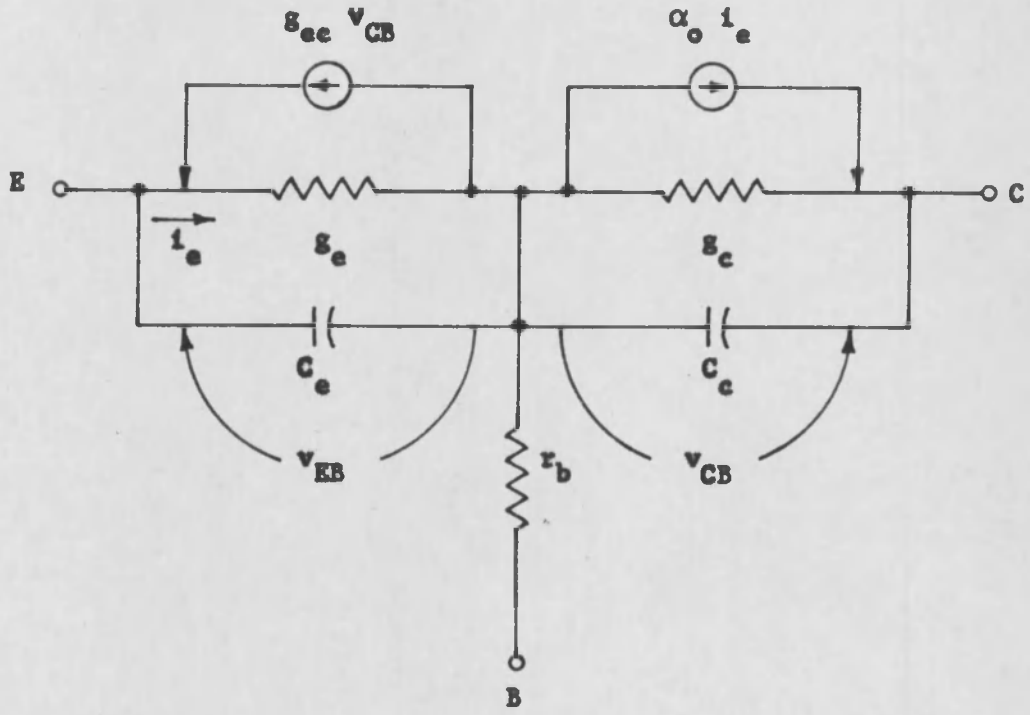
[2] D. Dewitt and A. L. Rossoff, Transistor Electronics, 3rd Ed., McGraw-Hill Book Company, Inc., 1957, p. 268.



NPN TRANSISTOR SWITCHING APPROXIMANTS

Figure 3.1



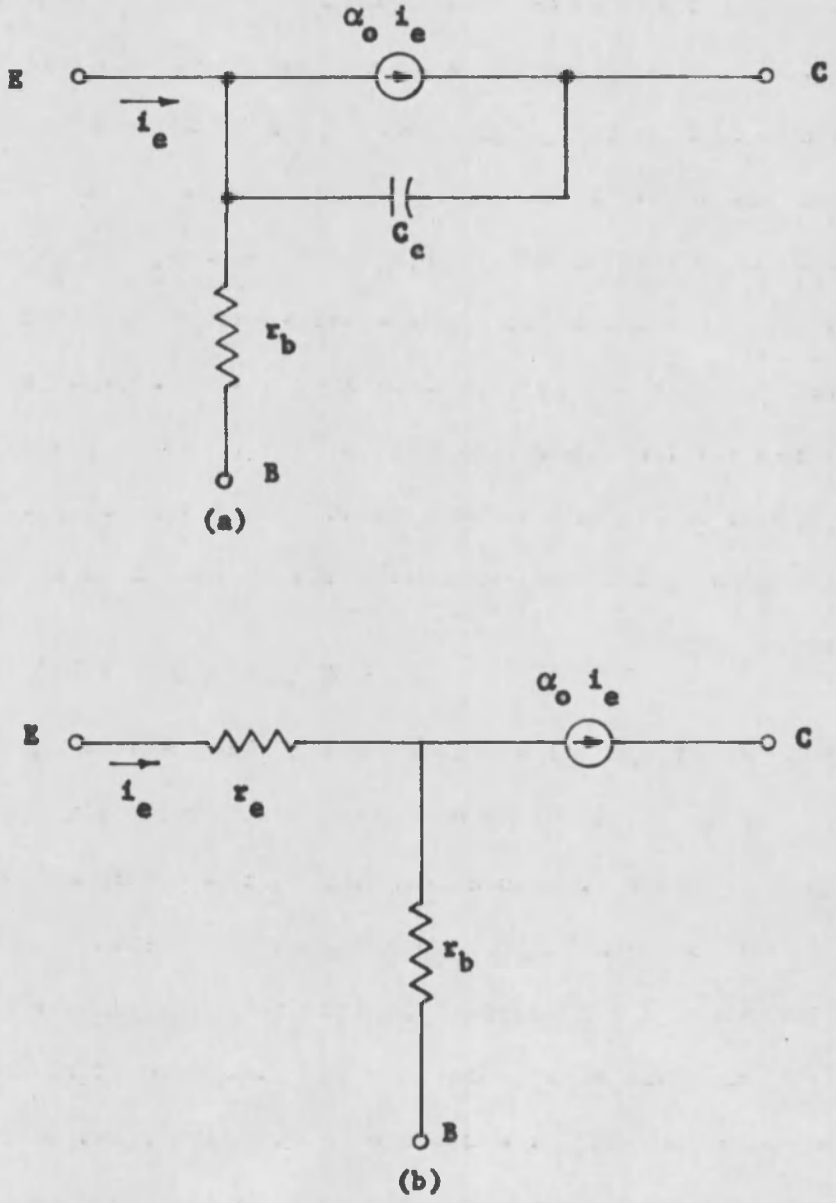
TRANSISTOR EQUIVALENT CIRCUIT

Figure 3.2

adapted to any of the operating regions mentioned above. During the important switching portion of the cycle, if the operation of the transistor is assumed to behave in an essentially linear manner, the equivalent circuit becomes as shown in Figure 3.3(a). Here the transistor is approximated to have negligible emitter resistance, negligible collector conductance, and a unity alpha and current gain. During the "ON" portion of the cycle, the current gain of the transistor is approximately constant and the effect of the collector capacitance can be neglected. The effect of the emitter resistance assumes significance, however, and the equivalent circuit becomes as in Figure 3.3(b). The significance and meaning of the equivalent circuits in this section are elaborated on in the following sections.

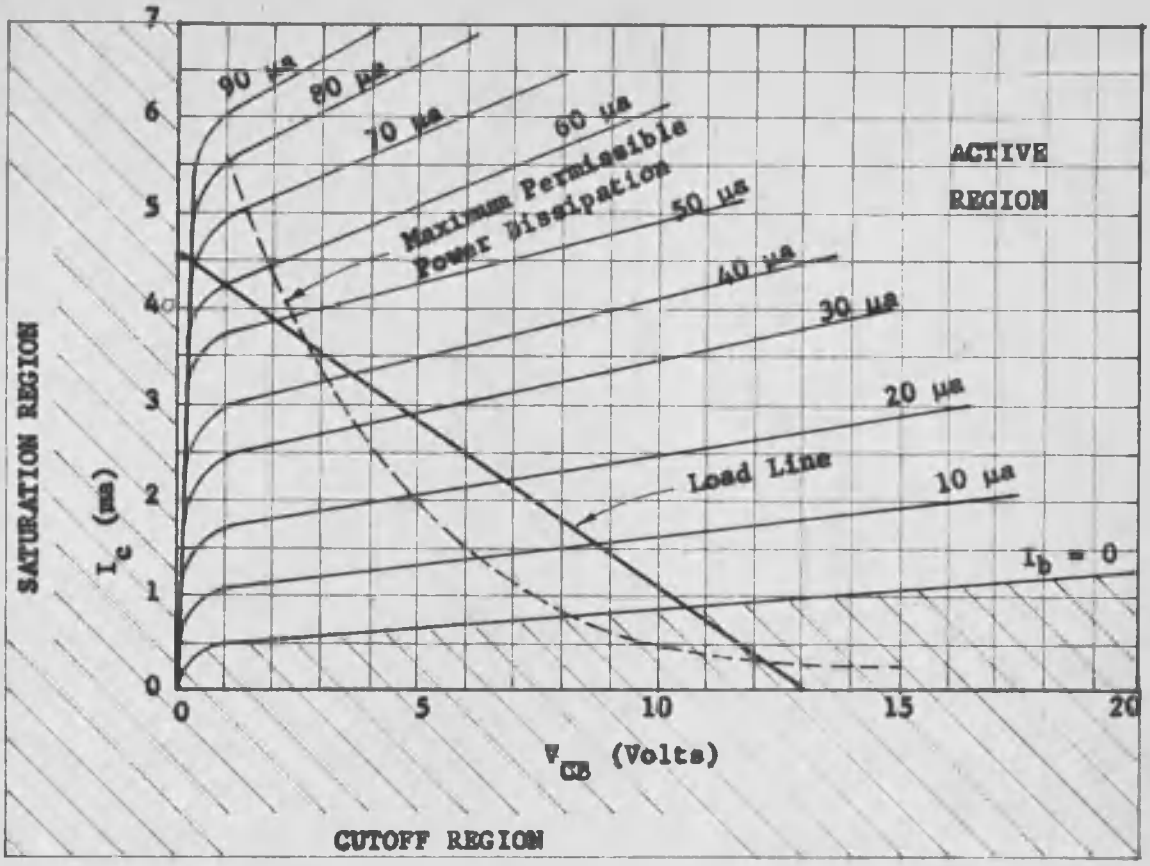
3.2 LARGE-SIGNAL OPERATION

In large-signal or nonlinear operation, the transistor behaves as an overdriven amplifier with resultant changes in the conduction state as described in the preceding section. These states represent regions of operation in the characteristic curves of the transistor. The common emitter output characteristics of a typical NPN transistor are shown in Figure 3.4. The characteristics are arranged in three regions: cutoff, active, and saturation. The dotted curve represents the maximum permissible power dissipation of the transistor. The arbitrarily chosen load line is allowed to invade the excess power dissipation region because of the extremely short time which it abides there. The cutoff and saturation regions are considered the stable



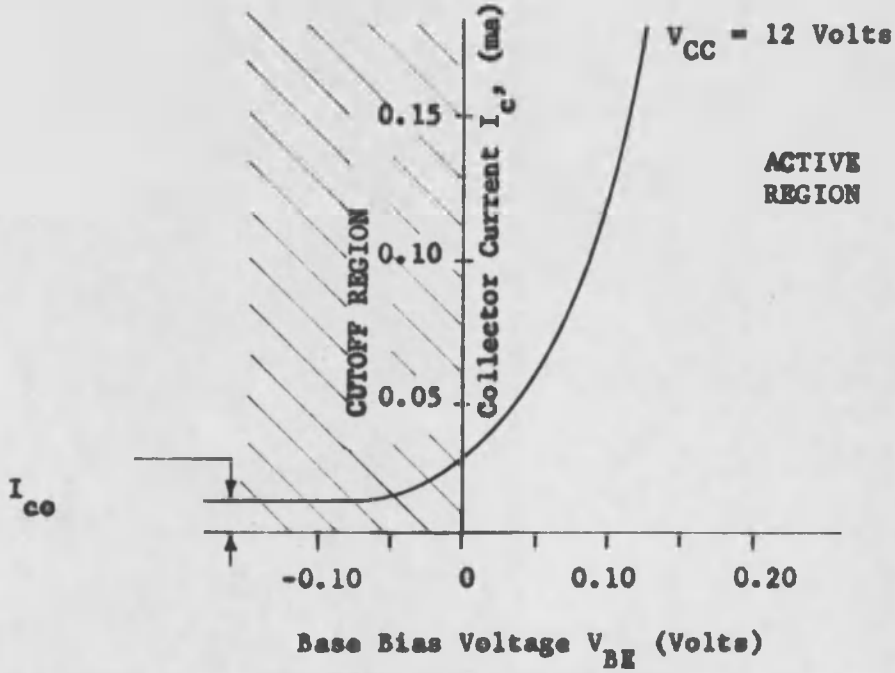
MODIFIED EQUIVALENT CIRCUITS

Figure 3.3



COMMON-EMITTER-COLLECTOR-CHARACTERISTIC FAMILY

Figure 3.4



COMMON-EMITTER REVERSE-TRANSFER-ADMITTANCE FAMILY - Figure 3.5

or quiescent regions of operation while the active region is considered the unstable or transient region through which operation passes while changing from the "OFF" to the "ON" state. The effect of the base bias voltage V_{BE} on collector current I_C is shown in Figure 3.5.

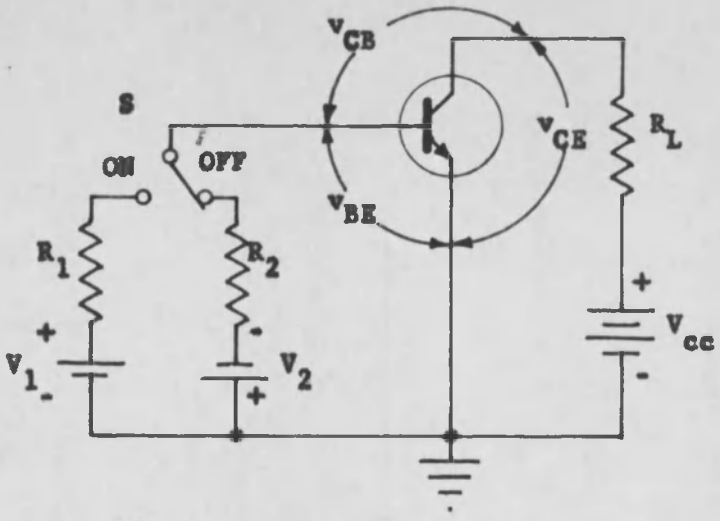
A basic NPN transistor switching circuit is shown in Figure 3.6. Typical circuit characteristics relevant to this treatment are compiled in Table 3.1. The cutoff region includes the area below the zero base-current curve in Figure 3.4. Ideally, with no initial base current, there would be zero collector current and the collector potential would equal the battery voltage V_{CC}. However, because of the saturation currents caused by minority carriers in the emitter, base, and collector regions, this situation is realized only in the approximate sense. These saturation currents, which are of important significance in many transistor applications, will be disregarded here with little deleterious effect on the calculations for the blocking oscillator.

The active linear region in Figure 3.4 is the only region providing normal amplifier gain. Transient response of the output signal is essentially determined by the transistor characteristics in this region. Operation of switch S in Figure 3.6 to the "ON" position is comparable to the application of a positive step voltage. Forward bias is established by battery V_1 and the base current and collector current become transitory in nature, passing through the

ITEM	REGION OF OPERATION		
	Cutoff	Active	Saturation
Input Impedance	High (infinite)	Low (zero)	Low (zero)
Output Impedance	High (infinite)	High	Low (zero)
Current Gain	Zero	Normal	Zero
Emitter-Base Junction	Reverse-Biased	Forward-Biased	Forward-Biased
Collector-Base Junction	Reverse Biased	Reverse-Biased	Forward Biased
Base Current	Zero	Transitory	High
Base Voltage	Negative	Positive (Transitory)	Positive
Collector Current	Zero	Transitory	High (Maximum)
Collector Voltage	Positive (High)	Positive (Transitory)	Zero

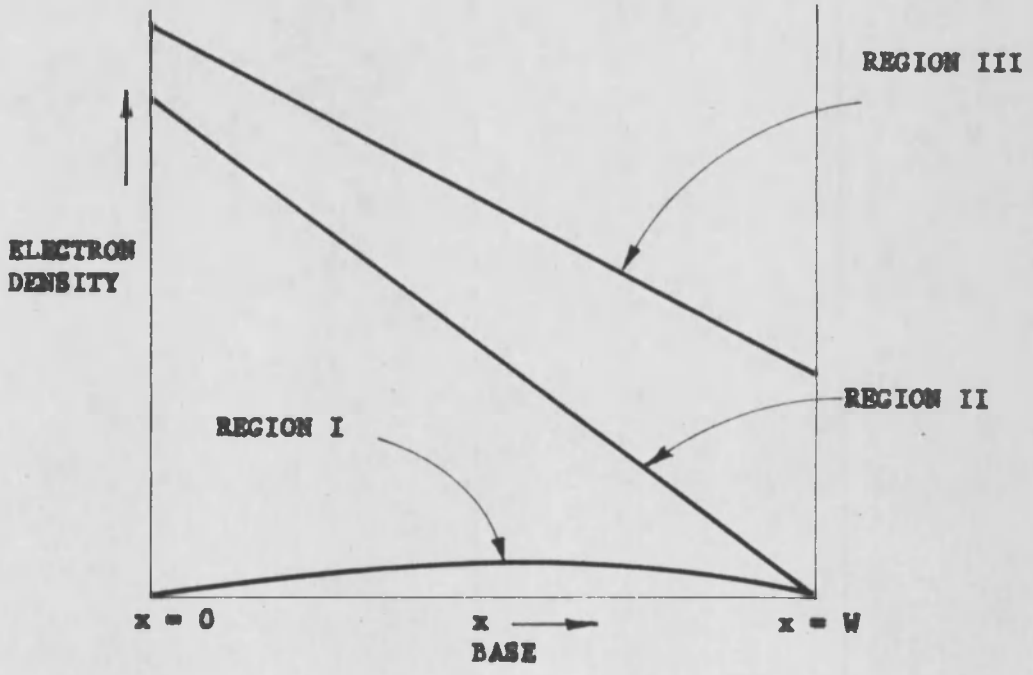
Table 3.1

Typical Switching Circuit Characteristics



TRANSISTOR SWITCHING CIRCUIT

Figure 3.6



ELECTRON DISTRIBUTIONS IN THE THREE REGIONS OF OPERATION

Figure 3.7

active region very rapidly. The saturation region is reached when an increase in base current no longer causes an appreciable increase in collector current. This occurs when the rise of collector current reaches the point where nearly all the supply voltage appears across the load. However, it is still possible to increase the total electron storage in the base to the point where the reciprocal of the lifetime γ of the electrons times the total stored charge equals the base current. The parameter γ is the length of time in which the base equilibrium disturbance decays to 1/e of its original value.

These regions of operation have best been described by Dewitt and Rossoff[3] through a knowledge of the electron charge stored in the base as a function of distance x along the base and time t, and of the charges stored in C_e and C_c as functions of t (see Figure 3.2). The electron distribution behavior in the base for the three regions of operation of an NPN transistor as designated in Section 3.1 is found in Figure 3.7 where W is the effective base width. In Region I, both junctions are reverse-biased and collect all of the electrons thermally generated in the base. Each junction draws about half of the saturation current I_{co} resulting in the symmetrical distribution curve shown.

In order to turn the transistor "ON" in Region II, electrons must be stored in the base. Electrons cannot be stored faster than

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[3] Ibid., pp. 269-272

the base lead can supply neutralizing holes, thereby making the base current the limiting factor in rate of storage. Since the collector-base junction remains reverse biased, electron density at x = W is still zero. When the saturation Region III is reached, both the collector voltage and current are clamped, independent of the magnitude and duration of the input signal. The electron distribution in this region has a nearly constant slope, $-\partial n/\partial x$, over the base and can be approximated by

$$\frac{I_c}{qD_n}$$

where

$q = 1.6 \times 10^{-19}$ coulombs

D_n = diffusion constant for electrons

The appreciable electron density at x = W establishes a very small negative value of v_{CB}.

When the saturated transistor is turned "OFF" by reversing switch S in Figure 3.6, the total of stored electrons drops but $-\partial n/\partial x$ remains nearly constant until v_{CB} starts to recover. This time lag until v_{CB} goes positive again is called storage time. Once v_{CB} becomes positive, the transistor drops to its original "OFF" state, which is the fall time.

3.3 THE SWITCHING TIME PROBLEM

In the present treatment, the time required to change the operating point of a transistor from Region I to Region III is of paramount importance. Dewitt and Rossoff[4] approach this problem through base charge storage considerations. By this method, the amount of time required to get the transistor from one state to another is found by computing the total base charge prior to the transition and after its completion, then determining the time for the transistor mechanism to effect this change. The total base charge is the sum of the charge Q_1 stored during Region II and the charge Q_2 stored during Region III. In addition, the collector capacitance C_c and the emitter capacitance C_e (see Figure 3.2) must have charge added or taken away to effect this change. That is, to get the transistor from Region I to Region III, the total base charge must be changed from Q_I to Q_{III}, the collector capacitance charge changed by

$$\int_{t_I}^{t_{III}} C_c \; d \; v_{CB}$$

and the emitter capacitance charge changed by

$$\int_{t_I}^{t_{III}} C_e \; d \; v_{EB}$$

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[4] Ibid, pp. 272-280

The mechanism which accomplishes this is the flow of base current I_b less the recombination current Q/γ. This charge transfer may be represented by

$$\int_{t_I}^{t_{III}} \left(I_b - \frac{Q}{\gamma}\right) dt = \int_{t_I}^{t_{III}} \left| C_c \, d\, v_{CB} + C_e \, d\, v_{EB} + dQ \right| \qquad (3.1)$$

or

$$\int_{t_I}^{t_{III}} \left(I_b - \frac{Q}{\gamma}\right) dt = \int_{I}^{III} C_c \, d\, v_{CB} + \int_{I}^{III} C_e \, d\, v_{EB} + (Q_{III} - Q_I) \qquad (3.2)$$

where the left side of each equation represents the total charge delivered by I_b between t_I and t_{III} less the charge lost by recombination during that interval. Equation (3.1) forms the basis for the computation of switching and storage times in the next sections.

3.4 RISE TIME

The rise time t_r is the time required for the leading edge of the pulse to increase in amplitude from 10 to 90 percent of its maximum value. In the switching transistor it represents the time from emitter cutoff (Region I) to current saturation (Region III) and

can be obtained from just a knowledge of the active region parameters. In calculating t_r, the right hand terms of Equation (3.1) represent charges which must be calculated for the circuit in Figure 3.6 as follows:

1. The charge transferred to the collector capacitance going from Region I to Region III is

$$Q_c = \int_{V_{cc}}^{0} C_c \, d\, v_{CB} \tag{3.3}$$

2. Changes in the emitter capacitance charge can be neglected since in the "OFF" condition, v_{EB} is only slightly negative.

3. The charge which must be stored in the base when the collector diffusion current I_{cd} reaches V_{CC}/R_L is

$$Q_{11} = V_{CC}/R_L \, \omega_c' \tag{3.4}$$

where ω_c' is the alpha cutoff frequency ω_c in radians per second when the collector voltage v_{CB} equals zero and I_c equals its maximum value of V_{CC}/R_L.

Substituting these values of charge transfer in Equation (3.1), the expression for rise time t_r becomes

$$t_r = \frac{Q_c + Q_{11}}{I_{b_1} - a\, Q_{11/\gamma}} \qquad (3.5)$$

where I_{b_1} is the total base current during the rise time and "a" is a constant approximately equal to 0.5.

The rise time clearly depends on the amount of drive, the current gain, and the frequency response of the transistor. In order to compare the rise time of the common emitter and common base connections, the rise time as a function of driving current must be known. This has been done graphically by Ebers and Moll[5] for comparable transistors. Their results, which are plotted in Figure 3.8, indicate that for equal driving currents, the common emitter connection switches "ON" faster than the common base circuit. Also, at some sacrifice in speed, a given current can be controlled with smaller drive for the common emitter case.

3.5 STORAGE TIME

Storage time results from injected minority carriers being present in the base region of the transistor at the moment when the input current is cut off. These carriers require a definite length of time to be collected. The length of storage time is essentially

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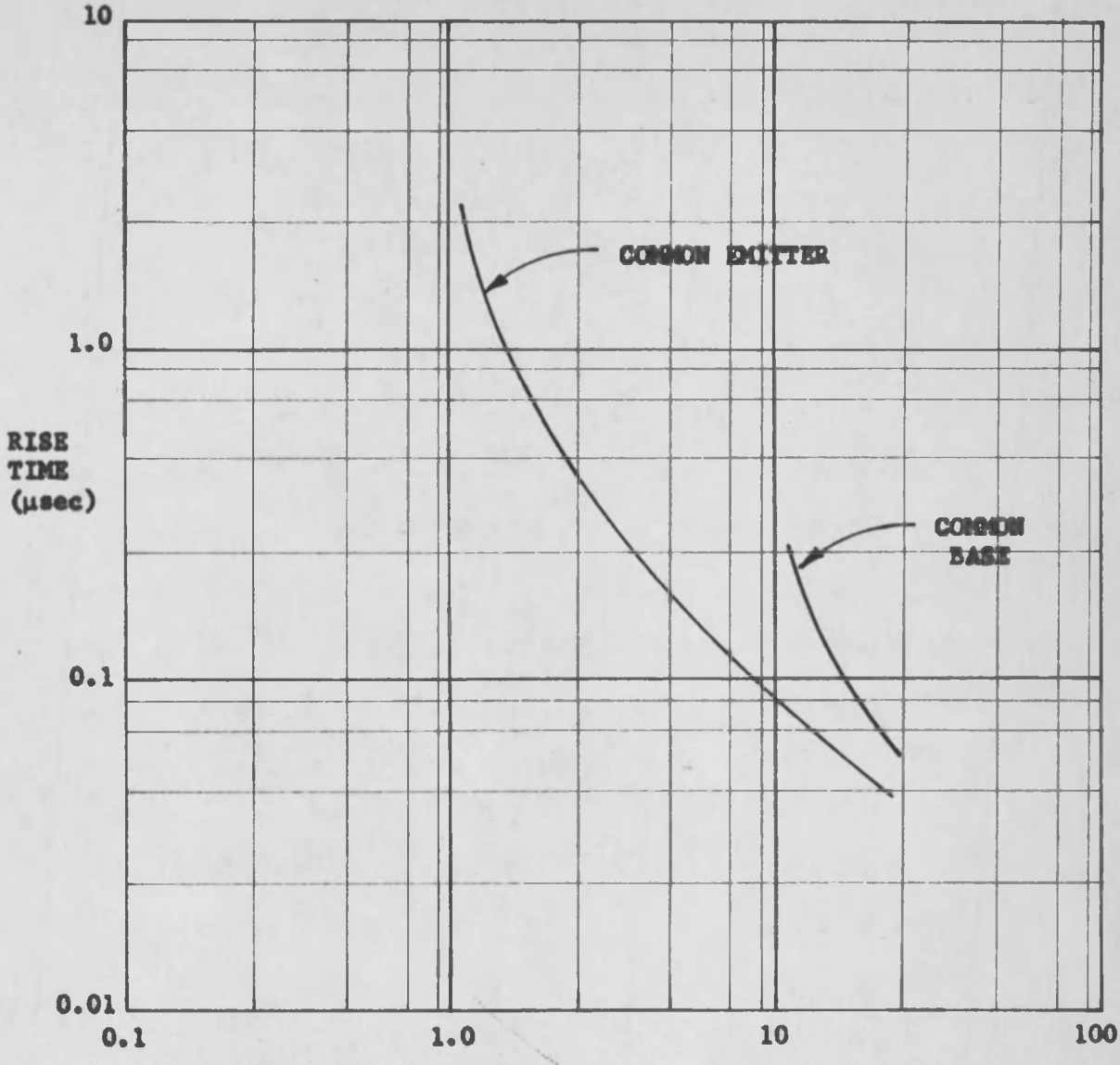
[5] J. J. Ebers and J. C. Moll, "Large-Signal Behavior of Junction Transistors," Proc. of the IRE., Vol. 42, Dec., 1954, pp. 1761-1772.



RISE TIME AS A FUNCTION OF DRIVING CURRENT

Figure 3.8

governed by the degree of saturation into which the transistor is driven and the time spent in saturation. The base current reversal that occurs at the end of the input pulse is the result of the stored carriers contributed by the current gain at the transistor multiplied by the initial input current, I_{b_1}. When this current value decays to the value of maximum current at saturation, the collector-base diode becomes reverse-biased, and I_b and I_c decay exponentially to zero.

Storage time t_s can be computed by using Equation (3.1) and the circuit in Figure 3.6 to obtain

$$t_s = \gamma \ln \frac{Q_{22} + I_{b_2} \gamma}{Q_{11} + I_{b_2} \gamma} \qquad (3.6)$$

where Q_{11} is from Equation (3.4), I_{b_2} is the total reversed value of base current, and Q_{22} is the total base charge stored at the instant of base current reversal.

Storage time is an undesirable condition for high speed switching. Since it does not curtail the rise time, and since repetition rate is not of importance here, measures to eliminate its effect such as collector clamping are not undertaken in this thesis.

3.6 FALL TIME

The decay transient, after the collector junction has "recovered" to Region II operation, is controlled by the normal active region parameters. The fall time t_f is defined as the time for the amplitude

of the pulse to fall from 90 to 10 percent of its Region III value. This time is not to be confused with "turn-off" time which is used by most authors to indicate the sum of storage and fall times.

The approach employed in Section 3.5 can be used here to find an expression for t_f. At the beginning of fall time, the stored base charge in excess of Q_{11} has diminished to zero and the collector is unclamped. v_{CB} goes positive causing C_c to discharge and I_{b_2} carries the sum of $C_c \frac{d\, v_{CB}}{dt}$ and the base discharge current. Assuming that the stored base charge goes from Q_{11} to zero during fall time, t_f can be expressed as

$$t_f = \frac{Q_c + Q_{11}}{I_{b_2} + c\, Q_{11}/\gamma}$$

where Q_c is defined in Equation (3.3), Q_{11} in Equation (3.4), I_{b_2} in Equation (3.6) and "c" is a constant approximately equal to 0.5.

The analytical approach and concepts of this chapter are extended to the total blocking oscillator analysis in Chapter 5.

Chapter 4

PULSE TRANSFORMER ANALYSIS FOR FAST RISE PULSES

4.1 THE PULSE TRANSFORMER

The electromagnetic pulse transformer is used for many applications in a wide range of circuits. In the blocking oscillator circuit it is used as a regenerative facility which has the ability to transmit pulses of short duration with a relatively small amount of pulse distortion. The properties of lumped pulse transformers have been thoroughly investigated in the microsecond range. Fortunately, it has been found by Moody, et al,[1] that existing design theory is applicable in the nanosecond range. On this basis, the present treatment will follow classical transformer analysis techniques.

There are primarily two ways in which the response of a pulse transformer to an impressed square wave can be found. The first involves a resolution of the square wave into a number of sinusoids by Fourier methods. The number of harmonics to be computed in the series depends on the accuracy of analysis required and the celerity with

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[1] N. F. Moody, C. J. R. McLusky, and M. O. Deighton, "Millimicrosecond Pulse Techniques," Electronic Engineering, Vol. 24, 1952, pp 214-219.

which the magnitude of the Fourier coefficients approaches zero. The response of the circuit to each frequency is determined and these are summed to obtain the total response. This method is cumbersome at best and can accumulate excessive error if great care is not taken. The second method is more suitable to this treatment and will be used here. This method involves determination of the transient circuit response to the slope discontinuities of the square wave. This permits a valid equivalent circuit for the transformer to be used for a complete transient analysis. The principal presupposition made here is that the leading-edge transient of the square wave vanishes before the trailing-edge one begins. This assumption is valid in most blocking oscillator applications.

The analysis and design results of this chapter are employed in Chapter 5 where the aggregate blocking oscillator circuit is analyzed.

4.2 EQUIVALENT CIRCUIT

The pulse transformer can be represented effectively by either lumped or distributed parameters. Since the latter involves awkward, intricate techniques which in the present treatment does little to increase accuracy, lumped parameters are used throughout. The equivalent circuit development in this section is taken from the work by Millman and Taub.[2]

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[2] J. Millman and H. Taub, Pulse and Digital Circuits, McGraw-Hill Book Co., Inc., 1956, pp. 253-263.

When the pulse transformer in Figure 4.1 responds to fast pulse waveforms, it behaves as a reasonable approximation to a perfect transformer. By representing the actual transformer by an ideal one together with additional circuitry to delineate the departure from perfection, Millman and Taub finally arrive at the equivalent circuit in Figure 4.2. In this circuit λ represents a series leakage inductance given by

$$\lambda = L_p (1 - k^2) \qquad (4.1)$$

where L_p is the magnetizing inductance and k is the coefficient of coupling defined by $k = \frac{M}{(L_p L_s)^{1/2}}$ as in Figure 4.1.

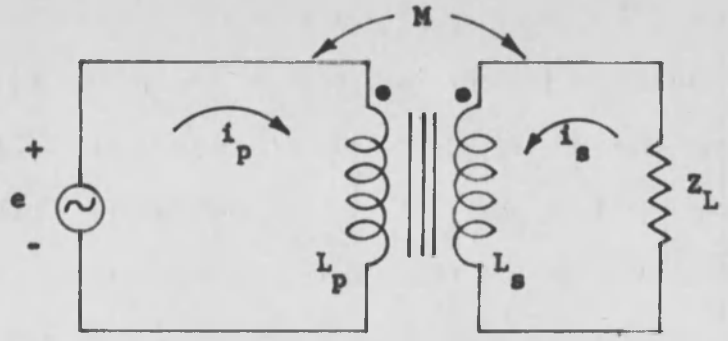
L is a modified magnetizing inductance given by

$$L = k^2 L_p \qquad (4.2)$$

and approaches the value of L_p as k approaches 1. The resistance R_1 is the sum of the generator impedance, assumed purely resistive, and the primary winding resistance. R_2 is the sum of the secondary winding resistance and the load resistance, transformed through the ideal 1:n transformer. The capacitance C is given by

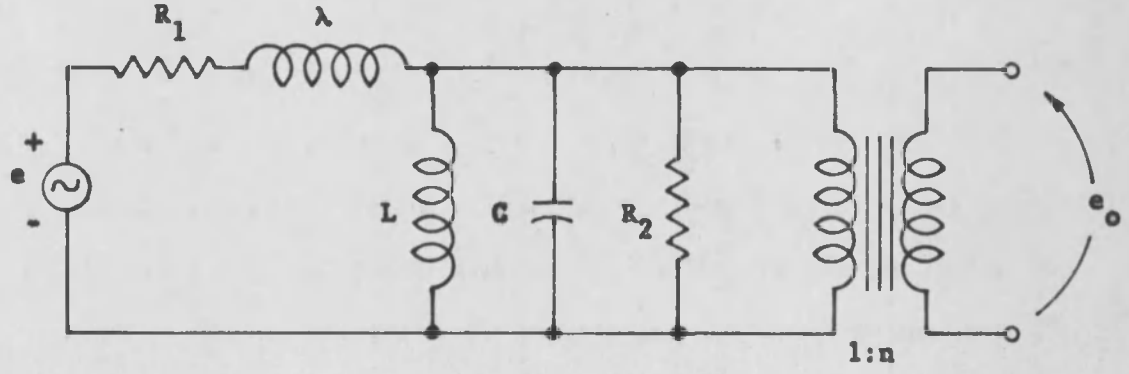
$$C = n^2 C_L + (n - 1)^2 \frac{C_o}{3} \qquad (4.3)$$

where C_L is the capacitance shunting the secondary terminals, n is the turns ratio as in Figure 4.2, and C_o is the interwinding capacitance. The interturn capacitance is negligibly small in comparison with the capacitance between windings and is therefore



PULSE TRANSFORMER SCHEMATIC DIAGRAM

Figure 4.1



PULSE TRANSFORMER EQUIVALENT CIRCUIT

Figure 4.2

neglected.

The circuit in Figure 4.2 is the one used in the analysis of the following sections.

4.3 PULSE-RISE RESPONSE

Employing the approach adopted in Section 4.1, the transformer pulse response can be examined sectionally. The pulse rise time analysis can be conducted on the modified version of the circuit in Figure 4.2 shown in Figure 4.3. The effect of the magnetizing inductance L is small relative to the capacitance C at the higher frequency components of interest and can therefore be disregarded. The effect of the leakage inductance λ, however, is important during the buildup time.

When switch S in Figure 4.3 closes, the step of voltage E impressed on the circuit simulates the leading-edge of a pulse. The transfer function for this circuit in Laplace notation is given by

$$\frac{e_o(s)}{nE} = \frac{1}{\lambda C} \quad \frac{1}{s\left[s^2 + \left(\frac{1}{R_2C} + \frac{R_1}{\lambda}\right)s + \frac{R_1 + R_2}{R_2\,\lambda C}\right]} \tag{4.4}$$

and from this equation the roots s of the characteristic equation are

$$s_1, s_2 = -\left(\frac{1}{2R_2C} + \frac{R_1}{2\lambda}\right) \pm \left[\left(\frac{R_1}{2\lambda} + \frac{1}{2R_2C}\right)^2 - \frac{R_1 + R_2}{R_2\,\lambda\,C}\right]^{1/2} \tag{4.5}$$

The steady state attenuation factor "a" of this circuit is $a = \frac{R_2}{R_1 + R_2}$ yielding a circuit time constant $\gamma = 2\pi\ (\lambda\ Ca)^{1/2}$. Manipulating Equation (4.5) into a standard form[3] the damping ratio μ is found to be

$$\mu = \frac{\gamma}{4\pi}\left(\frac{R_1}{\lambda} + \frac{1}{R_2\ C}\right) \tag{4.6}$$

and Equation (4.5) may be written in the form

$$s_1,\ s_2 = -\mu\ \omega_n \pm \omega_n\ (\mu^2 - 1)^{1/2} \tag{4.7}$$

where $\omega_n = 2\pi/\gamma$ is the undamped natural angular frequency of the circuit. Conditions of over damping, critical damping, and under damping occur when the damping ratio μ is greater than, equal to, and less than unity respectively. The behavior of the roots of the characteristic equation as the damping ratio μ varies from zero to infinity is shown in Figure 4.4. The real part of equation (4.7) is $\sigma = -\mu\ \omega_n$ and the imaginary part is $\omega = \pm\ \omega_n\ (1 - \mu^2)^{1/2}$.

Adequate information is now available so that the influence of the transformer constants on the leading edge of the pulse can be presented in a form amenable to the analysis in Chapter 5. To do this a graphical display similar to one used by Lee[4] is employed.

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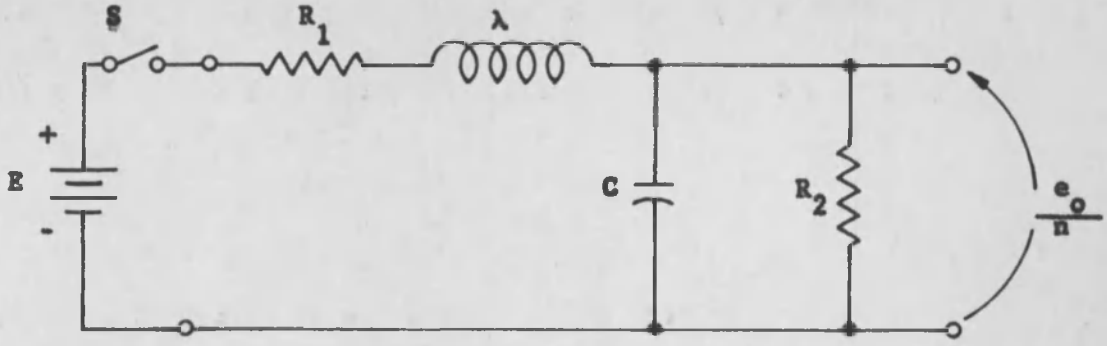
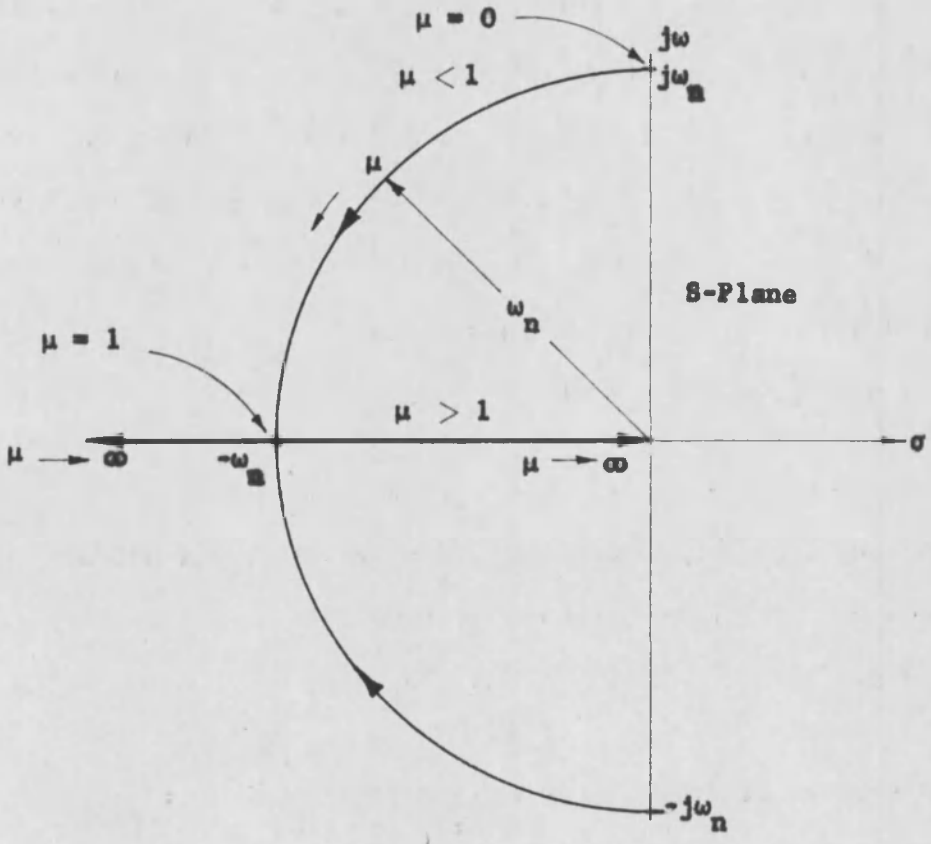
[3] M. E. Van Valkenburg, Network Analysis, Prentice-Hall, Inc., Sixth Printing, 1959, p. 104.

[4] R. Lee, Electronic Transformers and Circuits, 2nd Edition, John Wiley & Sons, Inc., 1958, p. 297.



RISE-TIME EQUIVALENT CIRCUIT

Figure 4.3



CHARACTERISTIC EQUATION ROOT LOCUS WITH μ

Figure 4.4

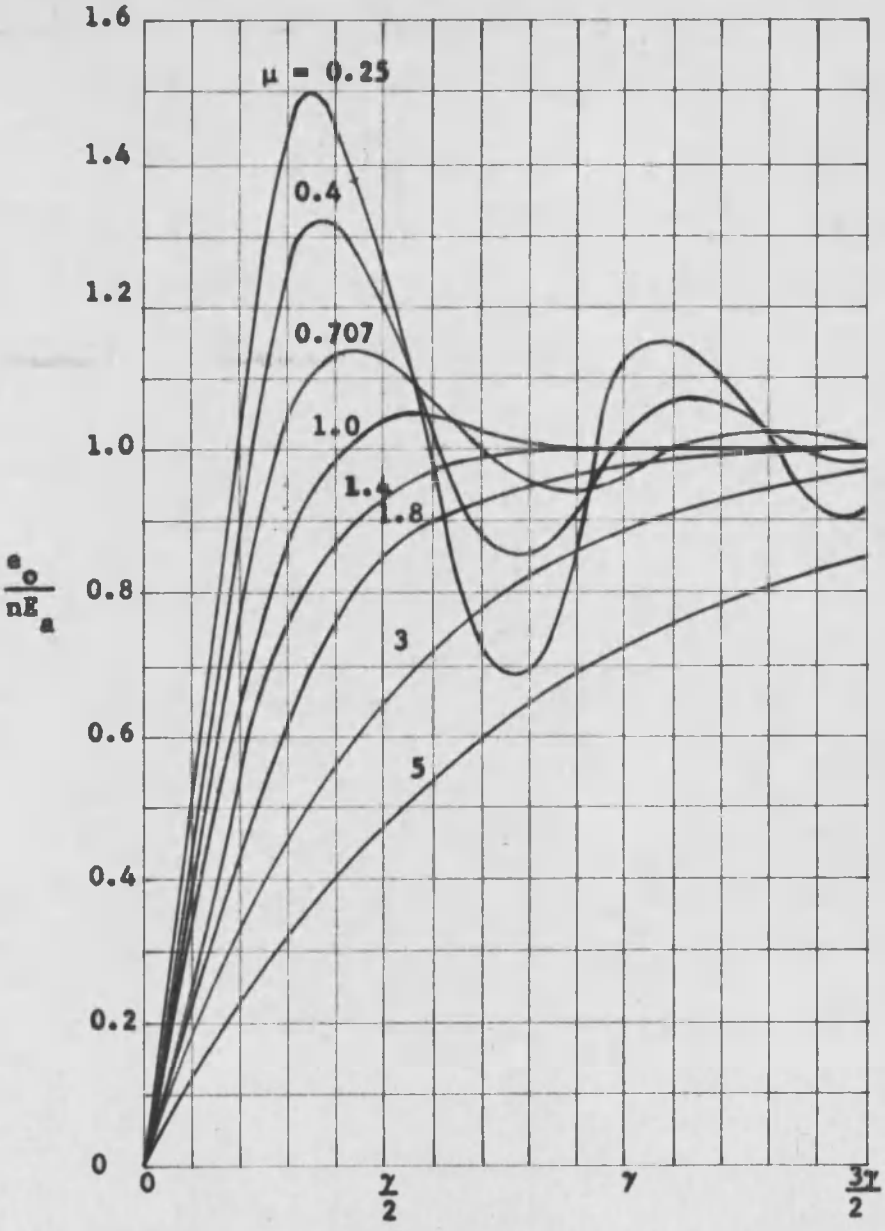
This display appears in Figure 4.5 where $E_a = E \frac{R_2}{R_1 + R_2}$, $R_1 = R_2$, and γ and μ are as defined above. It is obvious that the greater the transformer leakage inductance λ and distributed capacitance C, the slower will be the rate of rise, making small values of these parameters essential to this thesis. The resistances R_1 and R_2 also affect the damping ratio μ and must be considered in the analysis. The greater the amount of oscillations which can be indulged, the faster the rise time of the output pulse. High oscillatory peaks occur if the circuit is underdamped, and the leading edge rises slowly if it is overdamped. Designing μ close to unity will avoid these conditions.

4.4 PULSE-TOP RESPONSE

During the flat-top or "ON" portion of the pulse, the transformer can be represented by the equivalent circuit in Figure 4.6. The resistances R_1 and R_2 remain the same as shown in Figure 4.2. Capacitance C can be neglected since the rate of voltage change during this period is relatively small. The leakage inductance is neglected here since it is usually quite small compared with the magnetizing inductance L.

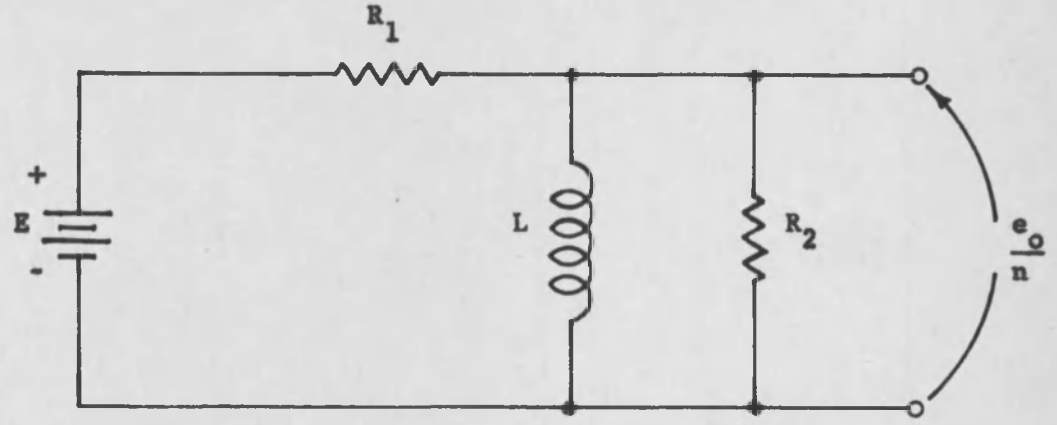
To facilitate computations, the Thevenin equivalent of the circuit in Figure 4.6 is shown in Figure 4.7. From that figure the output is seen to be

$$\frac{e_o}{n} = E' e^{\frac{-R' t}{L}} \qquad (4.8)$$



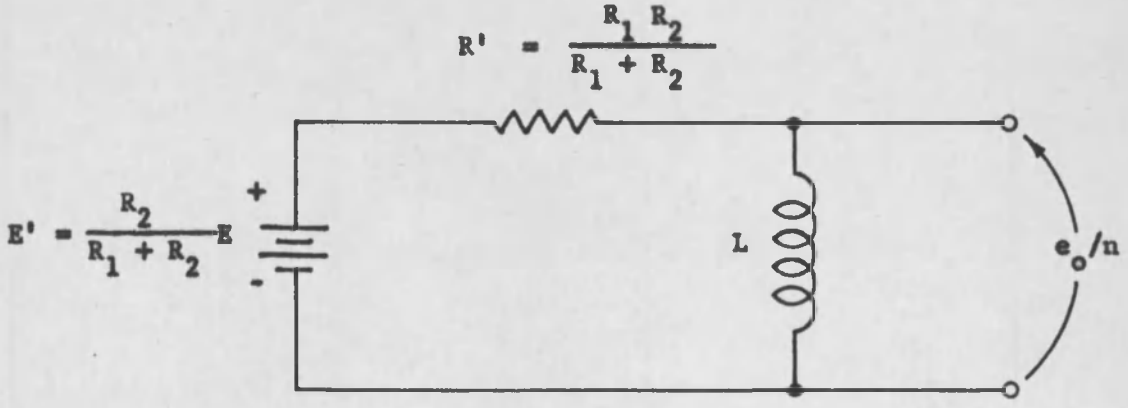
PULSE TRANSFORMER RISE-TIME RESPONSE

Figure 4.5



PULSE-TOP EQUIVALENT CIRCUIT

Figure 4.6



SIMPLIFIED PULSE-TOP EQUIVALENT CIRCUIT

Figure 4.7

and if the pulse width is t_w, the sag Ω is given by

$$\Omega \text{ in percent} = \left(1 - e^{-\frac{R' t_w}{L}}\right) \times 100 \text{ percent} \qquad (4.9)$$

It is obvious that sag is quite sensitive to R' and hence to the ratio R_2/R_1 in the expression $R' = \frac{R_1 R_2}{R_1 + R_2}$. If R_2 is much smaller than R_1, the sag is only slight; but as R_2 approaches infinity, the sag becomes excessive.

The major assumption adopted here is that the magnetizing inductance L is a constant. This is a valid assumption providing the core does not saturate. Caution is exercised to avoid this radically non-linear region in Chapter 5.

4.5 TRAILING-EDGE RESPONSE

The trailing-edge of the output pulse starts when the input pulse falls to zero, simulated by the opening of switch S in Figure 4.8. The magnetizing inductance L has an initial current I_o flowing in it and the capacitance C has an initial voltage V_o across it when this switching begins. The nature of the output pulse decay results largely from the decay of I_o. To investigate this response, the equivalent circuit in Figure 4.8 can be modified to that in Figure 4.9. The magnetizing current I_o at the end of the pulse (see Figure 4.7) can be determined by

$$I_o = \frac{(1 - \Omega)\, E'}{R'} \left(1 - e^{-\frac{R' t_w}{L}}\right) \qquad (4.10)$$

where

Ω is sag, $E' = \frac{R_2}{R_1 + R_2} E$, $R' = R_1 R_2 / R_1 + R_2$, and

t_w = pulse width period. The initial capacitor voltage V_o is equal to $(1 - \Omega) E'$.

The time equation for the pulse voltage decline can now be written as

$$\frac{e_o(t)}{n} = \frac{(1 - \Omega) E'}{R_2 C} \left[\left(\beta_1 + \frac{R_2 C I_o}{I_R} \right) e^{-\beta_1 t} - \left(\beta_2 + \frac{R_2 C I_o}{I_R} \right) e^{\beta_2 t} \right] \quad (4.11)$$

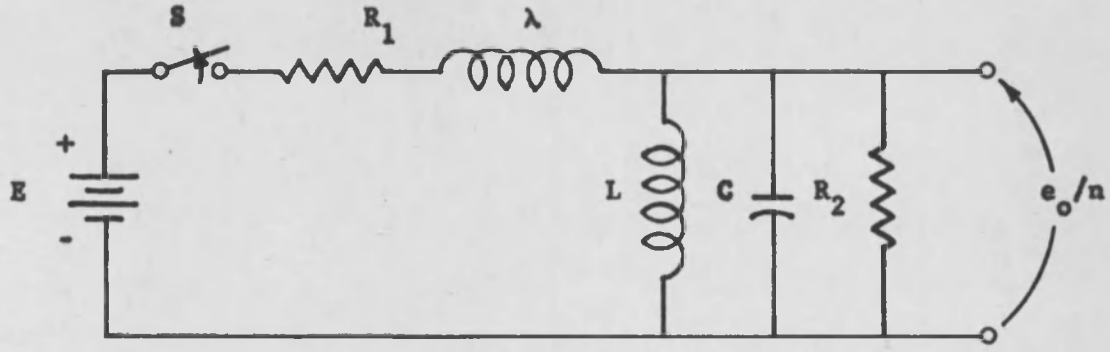
where

$$\beta_1, \beta_2 = \frac{1}{2} R_2 C \left[1 \pm (1 - \frac{1}{\alpha^2})^{1/2} \right]$$

I_R = primary load current

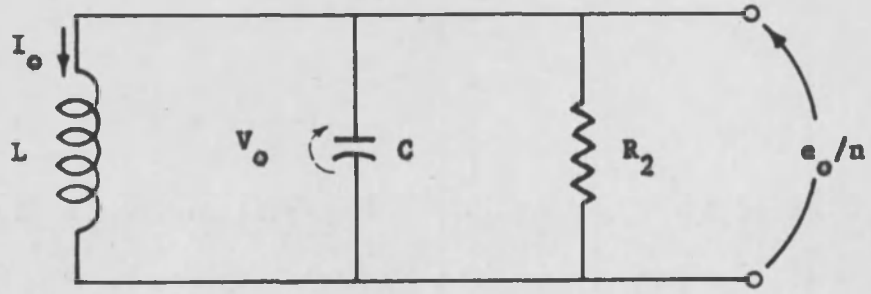
$$\alpha = \frac{1}{2 R_2} \left(\frac{L}{C} \right)^{1/2}$$

From this equation it can be inferred that fall time and backswing increase as the ratio α decreases. For this reason it is important to keep the capacitance of the transformer small. It is also necessary to keep the ratio I_o/I_R small if trailing pulse shape is important. This can be done by designing for shorter pulse widths and a judicious selection of transformer materials.



TRAILING-EDGE EQUIVALENT CIRCUIT

Figure 4.8



MODIFIED TRAILING-EDGE EQUIVALENT CIRCUIT

Figure 4.9

4.6 OVERALL RESPONSE

By applying the information in the preceding sections, the general shape of the pulse transformer output with a square pulse input can be predicted. The rise time portion, marked A in Figure 4.10, is dependent primarily on the magnitude of the leakage inductance λ and the equivalent primary capacitance C (see Figure 4.3). The droop of the pulse-top portion B is contingent on the combined circuit resistance R' and magnetizing inductance L time constant (see Figure 4.7). The fall time portion C and backswing portion D depend primarily upon the amount of magnetizing current I_o built up during the "ON" time of the pulse, and the magnitude of capacitance C.

When the transformer is connected in a blocking oscillator circuit, as is done for the analysis of Chapter 5, other characteristics become involved. The width of the pulse becomes a function of transformer parameters and is primarily determined by the transformer magnetizing inductance and distributed capacitance. An increase in either one causes a proportional increase in width. For the best pulse shape, the impedance $\left(\frac{L}{C}\right)^{1/2}$ (see Figures 4.1 and 4.2) should be made approximately equal to the load impedance Z_L. This is usually done by the adjustment of the thickness of layer insulation.[5]

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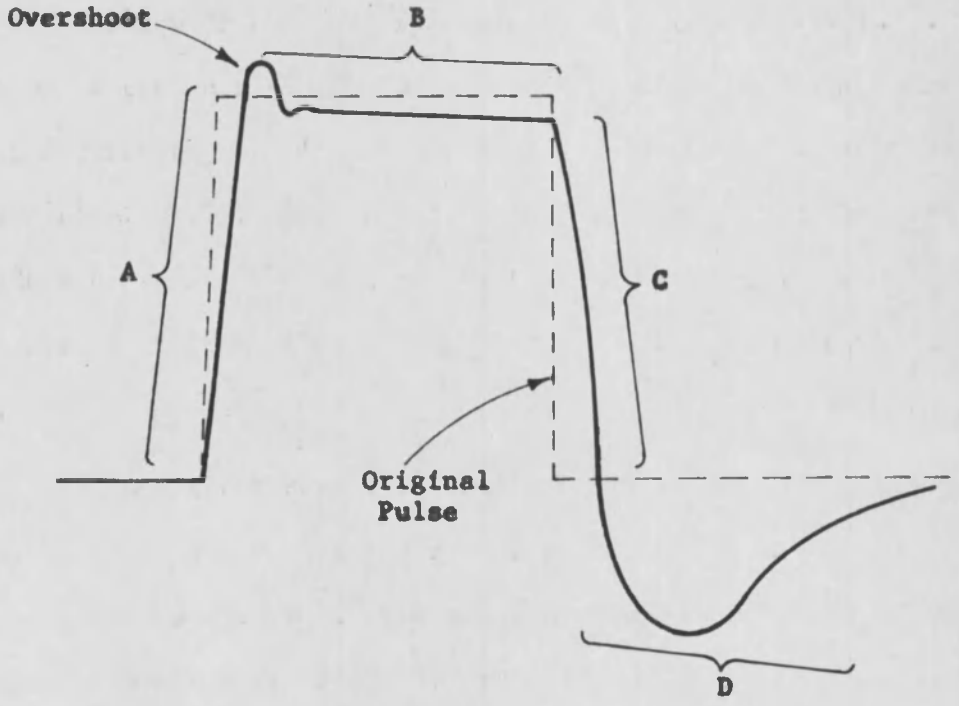
[5] R. D. McCartney, "Designing Transformers for Blocking Oscillators," Electronics, Vol. 31, No. 9, 1958, p. 80.



PULSE TRANSFORMER OVERALL RESPONSE

Figure 4.10

Other design considerations of the pulse transformer are noteworthy in preparing for the analysis of Chapter 5. Core permeability is important because with high-permeability core material less turns are required in order to obtain the necessary magnetizing inductance. Flux density should be as high as possible for small size, but not so high as to result in excessive magnetizing current and backswing voltage. The rise time response can be improved by physical manipulation of several of the transformer parameters such as the number of turns, core size, insulation, and the like. However, even though small core dimensions are desirable for low leakage inductance and distributed capacitance, a small core area may require excessive turns to fit the core.

Chapter 5

ANALYSIS OF THE FAST RISE BLOCKING OSCILLATOR

5.1 GENERAL

The most critical part of the design of a blocking oscillator is in choosing a pulse transformer and a transistor which are compatible and will produce a pulse of the desired width with a minimum rise time. As indicated in the last two chapters, the pulse transformer and the transistor each have a finite rise time and the combination of the two will always produce a rise time greater than that of either element. The purpose of this chapter is to analyze the blocking oscillator, emphasizing those features which influence the switching time, and to present a simple design procedure based on the results of this analysis.

Much of the analysis performed in this chapter is based upon the work by Linvill and Mattson;[1] however, considerable extension and elaboration to that work is undertaken to accommodate the faster rise times desired here. In the case of extremely fast switching, when the alpha cutoff frequency of the transistor is ultrahigh, the

[1] J. G. Linvill and R. H. Mattson, Op. Cit., pp. 1632-1639.

pulse transformer plays the limiting role in the analysis. The analysis that follows is performed independently on separate portions of the pulse time response curve as defined in Figure 4.10. However, to facilitate the analysis, the fall time and the rise time are considered together. This procedure is valid since they are functions of the same sequence of events, though in reverse order. The two times are observed to be approximately equal.

The question of transistor configuration choice for best rise time becomes rather arbitrary even though a comparison of the diffusion equations might indicate that the switching time required for the common emitter circuit is considerably longer than that of the common base circuit. The reason for this is that for a given natural frequency corresponding to a growing transient in the common emitter configuration there is another transformer turns ratio which will produce the same natural frequency in the common base configuration.[2] If m is the turns ratio used in the common emitter circuit and n in the common base circuit, then if $m = n - 1$ there is no essential difference between the two circuits as far as rise times are concerned. The circuit configuration to be employed in this thesis is that shown in Figure 5.1. It is a common base configuration but has "emitter control" as defined by Hamilton.

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[2] D. J. Hamilton, Op. Cit., p. 245.

Collector clamping (see Section 2.2) is not utilized in the circuit to be analyzed in Figure 5.1 for two reasons: First, collector saturation and its consequences do not affect the rise time which is the primary consideration here; and second, it is unlikely that the deleterious effects of letting the transistor saturate are much worse than causing a diode to saturate in its stead. If the storage time for the transistor is computed[3] and compared to that of a fast switching silicon diode, this is found to be true.

The operation of the common base blocking oscillator circuit is essentially the same as the common emitter one described in Section 2.2 and will not be repeated here. It is assumed in Sections 5.3 and 5.4 that a trigger is supplied from some source and is just sufficient to cause operation. The limitations imposed by various triggers is discussed in Section 5.5.

To avoid confusion between the time domain and the s-plane, time domain variables are lower case letters and the s-plane variables, as functions of the Laplace operator, s, are upper case letters. A PNP transistor will be used in this analysis since one is employed for the experimental results in Chapter 6.

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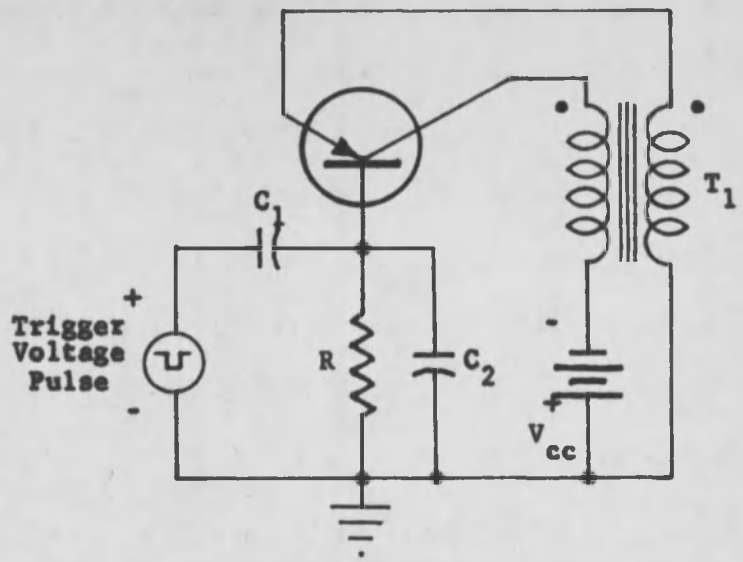
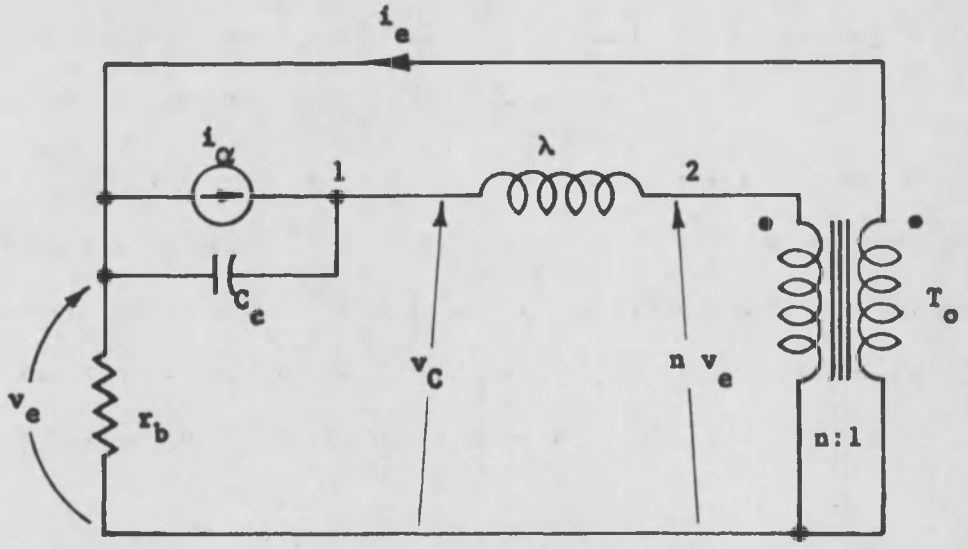
[3] D. J. Hamilton, "A Transistor Pulse Generator," Hughes Aircraft Company Report, September, 1958, p. 6.



A COMMON BASE PNP TRANSISTOR BLOCKING OSCILLATOR

Figure 5.1



EQUIVALENT CIRCUIT FOR THE SWITCHING PERIOD

Figure 5.2

5.2 NETWORK APPROXIMATIONS

The equivalent tee circuit for the transistor in Figure 3.3(a) and the equivalent circuit for the transformer in Figure 4.3 can be combined to yield an equivalent circuit for the rise time analysis. To simplify this combination, the following assumptions are made:

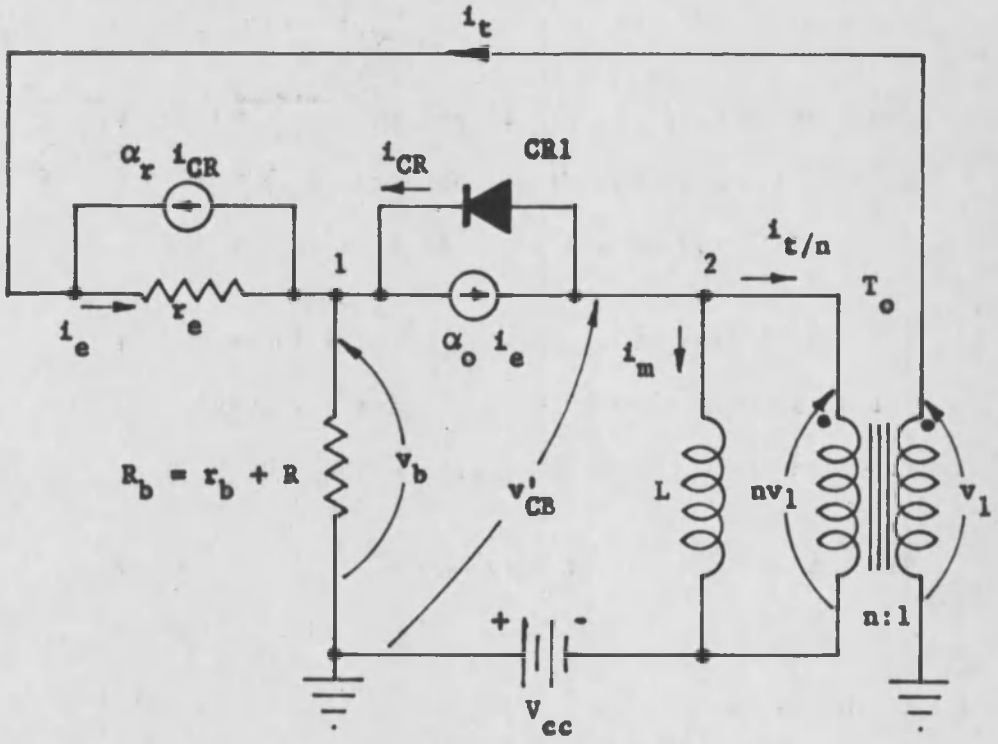
1. R_1 and R_2 in Figure 4.3 are omitted since the circuit is unloaded and the generator source of the transformer is the transistor.

2. The transistor is considered to have negligible emitter resistance and collector conductance. Unity alpha and current gain are also assumed.

3. The transformer shunt capacitance is considered negligible.

These seemingly radical approximations are necessary for computations which are manageable; they prove to be feasible when the analytical results are compared with the experimental results. The equivalent circuit in Figure 5.2 is the result of these simplifications.

To analyze the pulse top, the transistor equivalent circuit in Figure 3.3(b) can be combined with the transformer low frequency equivalent circuit in Figure 4.6. The result is the equivalent circuit in Figure 5.3 where the resistors R_1 and R_2 in Figure 4.6



EQUIVALENT CIRCUIT FOR THE PULSE TOP

Figure 5.3

are omitted as explained above. The diode CR1 represents the base collector internal diode of the transistor during saturation and α_r is the reverse alpha. α_r is typically equal to 0.6 in most transistors.

5.3 ANALYSIS OF THE RISE TIME

In order to determine the rise time, the circuit in Figure 5.2 must be analyzed. This also provides information as to the values of turns ratio of the transformer to be employed for fast response. Referring to Figure 5.2, the current generator i_α can be related to the emitter current i_e by the diffusion equation[4] of the transistor during this switching period as

$$i_e = i_\alpha + \frac{1}{\omega_c} \frac{d\, i_\alpha}{dt} \tag{5.1}$$

where ω_c is the α cutoff frequency in radians per second. The base resistance r_b may be transformed to $n^2\, r_b$ on the high impedance side of the transformer.

Summing the currents at nodes 1 and 2, the circuit equations are

$$\left(s\, C_c + \frac{1}{s\lambda} \right) v_c - \left(s\, C_c + \frac{n}{s\lambda} \right) v_e = I_\alpha \tag{5.2}$$

$$-\left(s\, C_c + \frac{n}{s\lambda} \right) v_c + \left(s\, C_c + \frac{n^2}{s\lambda} + g_b \right) v_e = -I_a \tag{5.3}$$

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[4] D. Dewitt and A. L. Rossoff, Op. Cit., pp. 92-94.

where the upper case letters denote Laplaced functions and $g_b = 1/r_b$. The emitter current can be calculated as

$$i_e = \frac{n}{\lambda} \int (v_c - n v_e)\, dt \tag{5.4}$$

Combining and transforming Equations (5.1) and (5.4), a third independent equation is obtained as

$$\left(\frac{n}{s\lambda}\right) V_c - \left(\frac{n^2}{s\lambda}\right) V_e = \left(1 + \frac{s}{\omega_c}\right) I_\alpha \tag{5.5}$$

The matrix equation of the system formed from Equations (5.2), (5.3), and (5.5) is

$$\begin{vmatrix} V_c \\ V_e \\ I_\alpha \end{vmatrix} \begin{vmatrix} s C_c + \frac{1}{s\lambda} & - s C_c + \frac{n}{s\lambda} & - 1 \\ - s C_c + \frac{n}{s\lambda} & s C_c + \frac{n^2}{s\lambda} + g_b & + 1 \\ \frac{n}{s\lambda} & - \frac{n^2}{s\lambda} & 1 + \frac{s}{\omega_c} \end{vmatrix} = \begin{vmatrix} 0 \\ 0 \\ 0 \end{vmatrix} \tag{5.6}$$

The characteristic equation of the system may be obtained from Equation (5.6) by equating its determinant to zero. After substantial algebraic manipulations, the following characteristic equation results:

$$s^3 + \left[\frac{(n-1)^2}{g_b \lambda} + \omega_c\right] s^2 + \left[\frac{1}{\lambda C_c} + \frac{\omega_c (n-1)^2}{g_b \lambda}\right] s - \frac{\omega_c (n-1)}{\lambda C_c} = 0 \tag{5.7}$$

That the s^3 term in this equation is considerably smaller than the other terms can be seen by replacing λ with $L(1 - k^2)$ (see Equations (4.1) and (4.2) and multiplying through Equation (5.7) by $(1 - \beta^2)$ to get

$$(1 - k^2)\, s^3 + \left[\frac{(n-1)^2}{g_b L} + (1 - k^2)\,\omega_c\right] s^2 + \left[\frac{\omega_c (n-1)^2}{g_b L} + \frac{1}{L C_c}\right] s - \frac{\omega_c (n-1)}{L C_c} = 0 \qquad (5.8)$$

The assumption that the s^3 term approaches zero here is seen to be valid, especially if the coefficient of coupling is very near unity.

A further approximation that can be made to simplify the calculations is that ω_c is much less than $\frac{(n-1)^2}{g_b \lambda}$ for n greater than 1. Since ω_c is high in this treatment, λ must be kept very small for validity. Then Equation (5.8) becomes

$$\frac{(n-1)^2}{g_b L} s^2 + \left[\frac{\omega_c (n-1)^2}{g_b L} + \frac{1}{L C_c}\right] s - \frac{\omega_c (n-1)}{L C_c} \doteq 0 \qquad (5.9)$$

and multiplying through by $g_b L/(n-1)^2$ alters Equation (5.9) to

$$s^2 + \left[\omega_c + \frac{1}{r_b C_c (n-1)^2}\right] s - \frac{\omega_c}{r_b C_c (n-1)} \doteq 0 \qquad (5.10)$$

If a radian frequency ω' is defined as

$$\omega' = \frac{1}{r_b C_c (n-1)^2} \qquad (5.11)$$

then Equation (5.10) becomes

$$s^2 + (\omega_c + \omega') \; s - \omega_c \, \omega' \; (n - 1) \doteq 0 \qquad (5.12)$$

The roots of this quadratic equation are

$$s_1, \; s_2 \doteq \frac{1}{2}\left[- \; (\omega_c + \omega') \; \pm \left[(\omega_c + \omega')^2 + 4 \; \omega_c \; \omega' \; (n - 1) \right]^{\frac{1}{2}} \right] \qquad (5.13)$$

where s_1 is the positive root and corresponds to a rising exponential which becomes the dominant root of the expression. The rise time t_r can be computed from this dominant root as[5]

$$t_r = \frac{2.2}{s_1} \qquad (5.14)$$

Therefore, the rise time t_r can be found by solving Equation (5.13) for s_1 and then solving Equation (5.14).

The optimum turns ratio yielding the smallest value of t_r is determined from Equation (5.13) by maximizing the s_1 root. This is done by setting $\partial s_1 / \partial n$ equal to zero and solving for n. However, this becomes rather difficult since ω' is a function of n, and it is simpler to apply function chain rules to get

$$\frac{\partial s_1}{\partial n} = \frac{\partial s_1}{\partial \omega_c} \frac{\partial \omega_c}{\partial n} + \frac{\partial s_1}{\partial \omega'} \frac{\partial \omega'}{\partial n} + \frac{\partial s_1}{\partial n} \frac{\partial n}{\partial n} = 0 \qquad (5.15)$$

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[5] J. Millman and H. Taub, Op. Cit., p. 276.

where

$$\frac{\partial \omega_c}{\partial n} = 0 \tag{5.16}$$

$$\frac{\partial s_1}{\partial \omega'} = \frac{1}{2}\left[\frac{2\,(2n-1)\,\omega_c + 2\omega'}{\left[\omega_c^{\,2} + 2\,(2n-1)\,\omega_c\,\omega' + (\omega')^2\right]^{\frac{1}{2}}}\right] - \frac{1}{2} \tag{5.17}$$

$$\frac{\partial \omega'}{\partial n} = -\frac{2}{r_b\,C_c\,(n-1)^3} = -2\,(n-1)\,(\omega')^2 \tag{5.18}$$

$$\frac{\partial s_1}{\partial n}\,\frac{\partial n}{\partial n} = \frac{2\,\omega_c\,\omega'}{\left[\omega_c^{\,2} + 2\,(2n-1)\,\omega_c\omega' + (\omega')^2\right]^{\frac{1}{2}}} \tag{5.19}$$

When Equations 5.16 through 5.19 are substituted into Equation 5.15, it becomes

$$\left[\omega_c^{\,2} + 2\,(2n-1)\,\omega_c\,\omega' + (\omega')^2\right]^{1/2}(n-1)\,(\omega')^2 - 2\,(n-1)\,(2n-1)\,(\omega')^2\,\omega_c + 2\,(n-1)\,(\omega')^3 + 2\,\omega_c\,\omega' \triangleq 0 \tag{5.20}$$

Assuming that ω_c is much less than $(\omega')^2\,(n-1)$, which is valid under all practical considerations, the optimum turns ratio n_o is

computed as

$$n_o \doteq \frac{1}{2}\left[1 + \left(1 + \frac{2}{r_b C_c \omega_c}\right)^{1/2}\right] \qquad (5.21)$$

This equation affords an approximate means by which n_o can be computed for design purposes if r_b, C_c, and ω_c are known.

5.4 ANALYSIS OF THE PULSE TOP

In order to develop an analytical expression for the pulse width t_w for the circuit in Figure 5.3, certain simplifying approximations must be made. It is assumed, for instance, that while the transistor is in the saturation Region III, v'_{CB} is clamped at zero. It is further supposed that the magnetizing current i_m is equal to zero at the beginning of the pulse top. This is a valid assumption considering the extemely fast rise times being dealt with here.

Referring to the circuit in Figure 5.3, the feedback current i_t is given by

$$i_t = i_e - \alpha_r i_{CR} \qquad (5.22)$$

where i_{CR} is the current drawn through the closed collector-base diode during saturation and α_r is the reverse alpha of the transistor. Summing the currents at node 1 for the initial condition $i_m = 0$ yields

$$i_e = \frac{(\alpha_r - 1)\, i_{CR}(0) + G_b v_b}{1 - \alpha_o} \qquad (5.23)$$

where $i_{CR}(0)$ is the value of i_{CR} at the beginning of the pulse top and $G_b = 1/R_b$. Summing the currents at node 2 gives

$$\alpha_o i_e = i_t/n + i_{CR}(0) \tag{5.24}$$

Combining Equations (5.22) and (5.24) gives

$$i_e = \frac{i_{CR}(0) \quad (1 - \frac{\alpha_r}{n})}{\alpha_o - \frac{1}{n}} \tag{5.25}$$

and finally combining Equations (5.23) and (5.25) yields the expression for $i_{CR}(0)$,

$$i_{CR}(0) = \frac{G_b v_b \left| n \alpha_o - 1 \right|}{(n - 1)(1 - \alpha_o \alpha_r)} \tag{5.26}$$

This equation unfortumately contains v_b, but since it is a function of the trigger voltage (see Figure 5.1) an approximate expression for it is

$$v_b \triangleq \frac{V_T}{R} (r_b + R) \tag{5.27}$$

where V_T is the trigger voltage amplitude.

The pulse width t_w may now be expressed to a first order approximation by considering the "ON" time equal to the amount of time it takes the magnetizing inductance L to charge to the point where i_{CR} goes to zero and the transistor reverts to operating Region II. The sum of incremental current changes at node 2 is

$$\Delta i_{CR} = \Delta i_m + \frac{\Delta i_t}{n} \tag{5.28}$$

where $\alpha_o i_e$ is assumed to be constant. If the assumption that $v'_{CB} = 0$ during saturation is now made, then the charging voltage across L is V_{cc} and the pulse width can be obtained from

$$i_{CR}(0) = \frac{V_{cc}}{L} t + \frac{\alpha_r i_{CR}(0)}{n} \tag{5.29}$$

Solving for $t = t_w$ in Equation (5.29), the pulse width is found to be

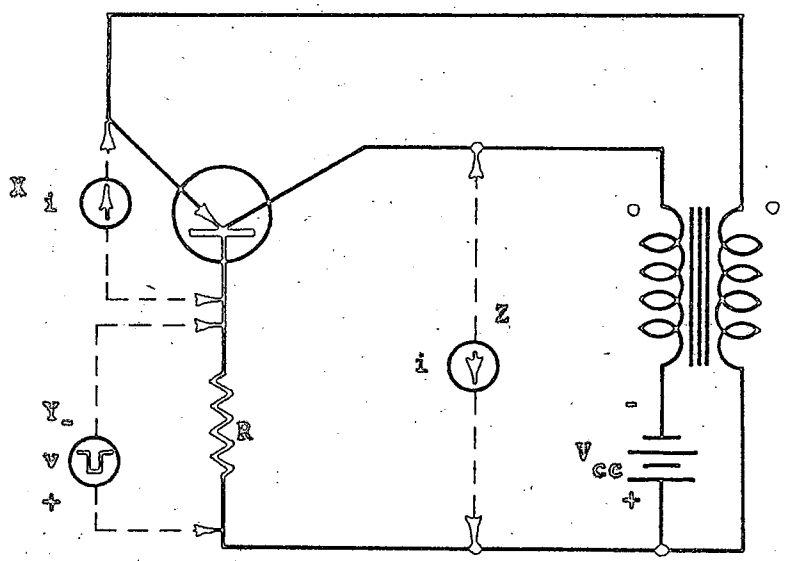
$$t_w = \frac{L}{V_{cc}} \left(1 - \frac{\alpha_r}{n}\right) i_{CR}(0) \tag{5.30}$$

where $i_{CR}(0)$ is given by Equations (5.26) and (5.27).

5.5 TRIGGERING LIMITATIONS

The blocking oscillator in Figure 5.1 can be triggered in a number of ways as discussed briefly in Section 2.3. The three most important methods of triggering are indicated in Figure 5.4. Linvill and Mattson compare these triggering modes through source energy and source impedance considerations. The differences in source energy requirements for triggering in the various modes is not widely different, although base triggering does require somewhat more energy than the other two modes.

The source impedance requirements in the different places does, however, vary considerably. Base triggering, marked "Y" in Figure 5.4, has the best source impedance performance with an essentially constant, moderate value throughout the rise time of the pulse. Emitter



BLOCKING OSCILLATOR TRIGGERING POINTS

Figure 5.4

triggering at "X", however, changes from a moderate source impedance at the start of switching, then drops to a low value, and finally recovers as the top of the pulse is reached. For the case of collector triggering at "Z", the source impedance begins at a moderate value then rises over tenfold by the end of the rise time. From these considerations it would seem that base triggering is the most attractive.

The most important consideration in this treatment, however, is the pulse output rise time. Since the base triggering mode develops its trigger across a base resistor R, resultant increased total base resistance r_b in Equations (5.11), (5.13), and (5.14) indicates a longer rise time. This effect is avoided, however, by providing a signal bypass to R by the capacitor C_2 in Figure 5.1.

The trigger characteristic which has the greatest influence upon the output pulse rise time is the rise time of the trigger pulse. It is intuitively apparent that the faster the transistor is driven into and through its regenerative switching state, the faster is its rise time. The rise time analytical development in Section 5.3 is predicated on a trigger with infinite leading edge slope and does not lend itself readily for triggers with finite slope. Therefore, consideration of the behavior of output pulse rise times with varying trigger rise times will be postponed to Section 6.5 where experimental results clearly point up this dependence.

5.6 LOADING CONSIDERATIONS

The analysis conducted thus far in this chapter deals with blocking oscillators working into infinite impedance. In practical applications blocking oscillators are required to deliver useful power to finite loads and therefore it is necessary to adapt the resultant equations of Sections 5.3 and 5.4 to this situation.

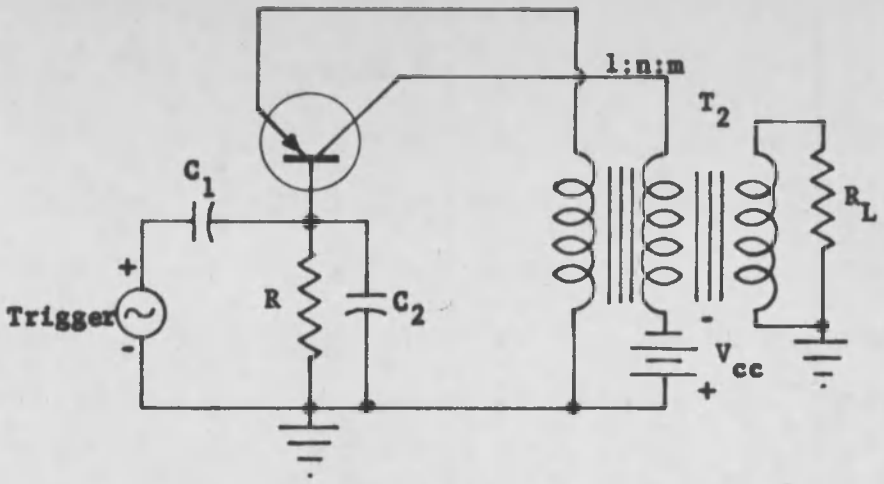
A loaded version of the circuit in Figure 5.1 is shown in Figure 5.5. The load is transformer coupled to the blocking oscillator. Usually the turns ratio m is made equal to n, but for complete generality different symbols are employed. The collector circuit sees a load impedance equal to $\frac{n^2 R_L}{m^2}$ and the emitter circuit sees R_L/m^2.

The circuit in Figure 5.6 is the equivalent circuit for the switching period with the load included. The load resistance R_L appears across the base resistance r_b as $\frac{R_L}{m^2}$. As a conductance it is $m^2 G_L$. Replacing g_b in Equation (5.9) by $g_b + m^2 G_L$, Equation (5.10) becomes

$$s^2 + \left[\omega_c + \frac{g_b + m^2 G_L}{C_c (n-1)^2}\right] s - \frac{\omega_c (g_b + m^2 G_L)}{C_c (n-1)} = 0 \qquad (5.31)$$

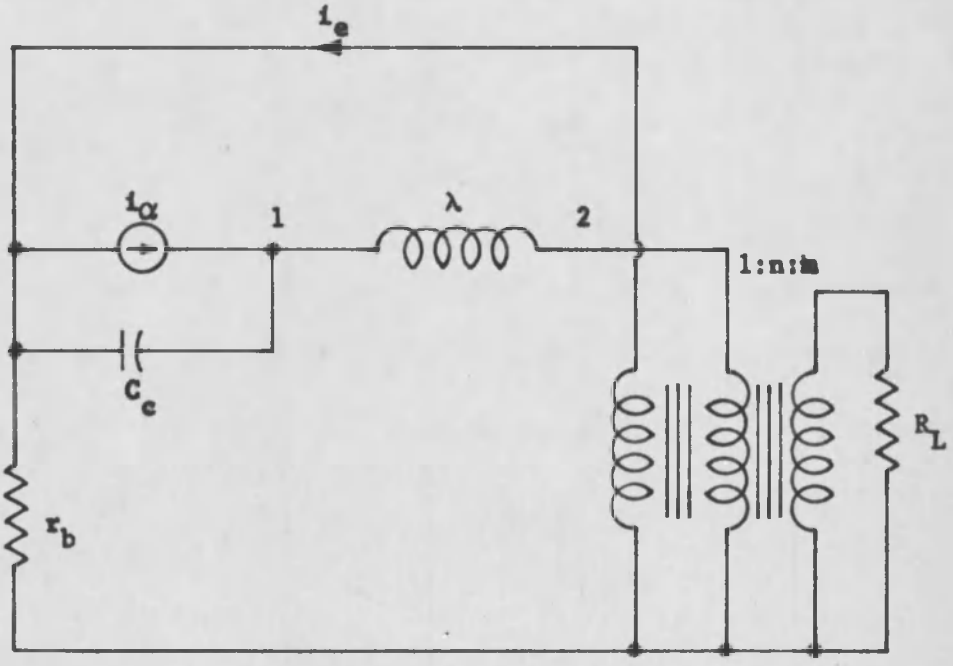
The positive root of this quadratic equation becomes

$$s_1 = \frac{1}{2}\left[-(\omega_c + \omega'') + \left[(\omega_c + \omega'')^2 + 4\,\omega_c \omega'' (n-1)\right]^{1/2}\right] \qquad (5.32)$$



LOADED BLOCKING OSCILLATOR

Figure 5.5



LOADED BLOCKING OSCILLATOR EQUIVALENT CIRCUIT FOR THE SWITCHING PERIOD

Figure 5.6

where $\omega'' = \dfrac{g_b + m^2 G_L}{C_c (n-1)^2}$

The optimum turns ratio is determined to be

$$n_o \doteq \frac{1}{2}\left[1 + \left(1 + \frac{2 g_b + 2 m^2 G_L}{C_c \omega_c}\right)^{\frac{1}{2}}\right] \qquad (5.33)$$

The effect of a load on the pulse top of a blocking oscillator can be evaluated by considering the equivalent circuit in Figure 5.7. The load impedance R_L acts as a current divider across the magnetizing inductance L with a conductance of $\frac{m^2 G_L}{n^2}$. This means another current, $\frac{m i_L}{n}$, flows at node 2 and Equation (5.24) becomes

$$\alpha_o i_e = i_{t/n} + i_{CR}(0) + \frac{m i_L}{n} \qquad (5.34)$$

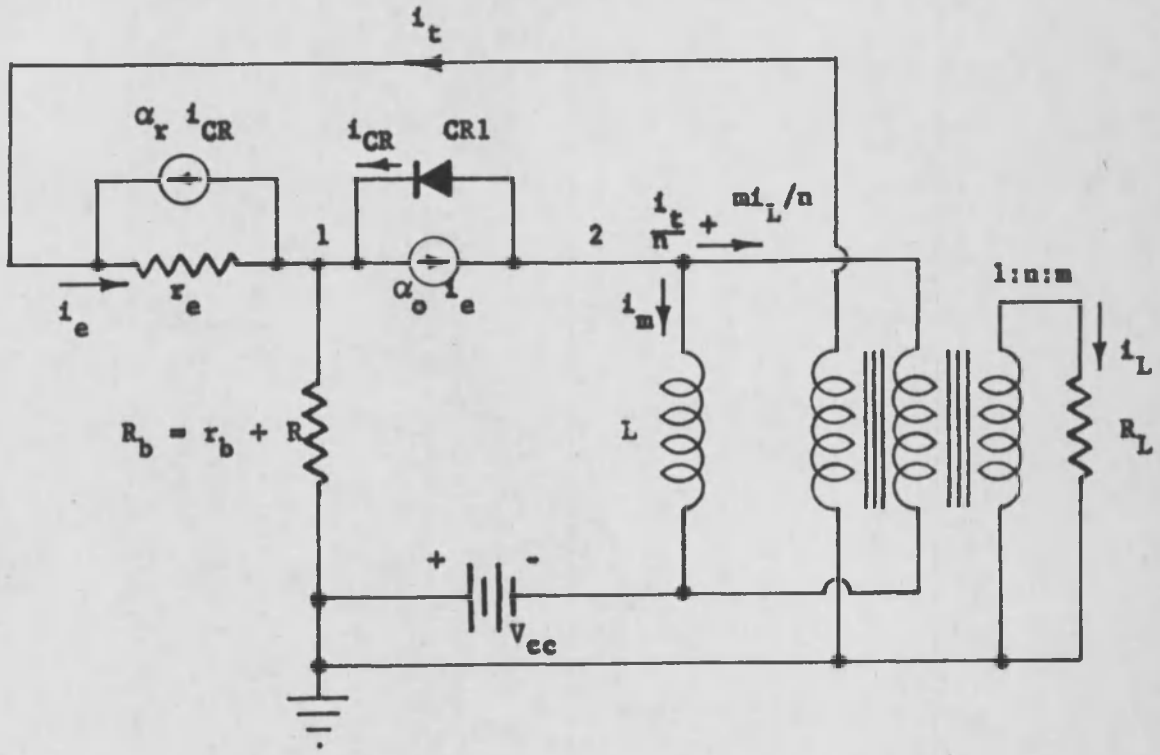
Equation (5.25) becomes

$$i_e = \frac{i_{CR}(0)\left(1 - \frac{\alpha_r}{n}\right) + \frac{m i_L}{n}}{\alpha_o - \frac{1}{n}} \qquad (5.35)$$

Combining Equations (5.23) and (5.35) now yields

$$i_{CR}(0) = \frac{n^2 (n \alpha_o - 1) G_b v_b - m^3 G_L V_{cc} (1 - \alpha_o)}{n^2 (n-1)(1 - \alpha_o \alpha_r)} \qquad (5.36)$$

where i_L in Equation (5.35) is replaced by $\frac{m^2 G_L V_{cc}}{n^2}$ with the assumptions of Section 5.4.



LOADED BLOCKING OSCILLATOR EQUIVALENT CIRCUIT FOR THE PULSE TOP

Figure 5.7

Since i_L remains essentially constant during saturation, the pulse width is still given by Equation (5.30) only with $i_{CR}(0)$ evaluated as in Equation (5.36).

5.7 DESIGN PROCEDURE

The equations developed in the past sections lend themselves nicely to a fairly simple design procedure for the transistor blocking oscillator. The equations for the positive root of the characteristic equation (Equation 5.13), the rise time (Equation 5.14), the optimum turns ratio (Equation 5.21), and the pulse width (Equation 5.30), are the four basic design equations. If loading is to be considered, Equations (5.32), (5.14), (5.33), and (5.30) with (5.36) substituted should be employed. Other design procedures can be derived from these basic equations.

The usual problem is to design a blocking oscillator when specifications of maximum rise time, pulse width, and load are given. The basic procedure is to select a transistor and then to design a pulse transformer that satisfies the specifications.

The design procedure is as follows:

1. Select a transistor on considerations of high alpha cutoff frequency and low $r_b C_c$ product. The alpha of the transistor is not critical but should be relatively low for narrow pulses.

2. Calculate the optimum turns ratio from Equations (5.21) or (5.33).

3. Calculate the positive root of the characteristic equation from Equations (5.13) or (5.32).

4. Compute the rise time from Equation (5.14) and if it does not satisfy the specifications then a transistor with a higher ω_c and a lower $r_b C_c$ product must be selected and steps 1 - 4 repeated.

5. Determine the magnetizing inductance from the pulse width Equations (5.30), (5.26), and (5.36).

6. Design a pulse transformer having the turns ratio calculated in step 2 and a magnetizing inductance determined in step 5. The coefficient of coupling should be as close to unity as possible. The leakage inductance and distributed capacitance should be as small as possible.

The derivation of the basic design equations involves certain assumptions and limitations. In summary these are as follows:

1. Coefficient of coupling k near unity.

2. ω_c much less than $\frac{(n-1)^2}{g_b \lambda}$ for n greater than 1.

3. ω_c much less than $\frac{1}{r_b C_c (n-1)}$

4. Magnetizing current i_m equal to zero at beginning of pulse top.

5. v'_{CB} in Figure 5.3 clamped at zero while transistor is saturated.

These basic design equations form the foundation for the design of a fast rise transistor blocking oscillator. Because of the approximations involved they must be used with caution and the results modified from experimental observation. In Chapter 6 these equations are employed in the design of a blocking oscillator. The oscillator is constructed and experimentally tested. Theoretical and experimental results are compared.

Chapter 6

EXPERIMENTAL RESULTS

6.1 SELECTING THE CIRCUIT COMPONENTS

In order to validate the design equations developed in Chapter 5, a typical fast rise blocking oscillator must be designed and tested experimentally. This is done by following the procedure of Section 5.7, and the results are presented in this chapter. The design requirements are for a 10 volt pulse with a pulse width of 1.5 μsec, working into a load of 1000 ohms, and with as short a rise time as possible. The latter requirement is met by a judicious choice of the transistor and the pulse transformer.

The transistor is selected on the basis of high alpha cutoff frequency and low $r_b C_c$ product. The transistor chosen is the Motorola Mesa Transistor Type 2N695. It is a germanium PNP diffused junction transistor designed primarily for operation in ultra high speed switching applications. It has a high maximum junction temperature of 100° C which permits it to be operated reliably in applications where Germanium transistors have not been previously considered. Typical characteristics for the 2N695 are:

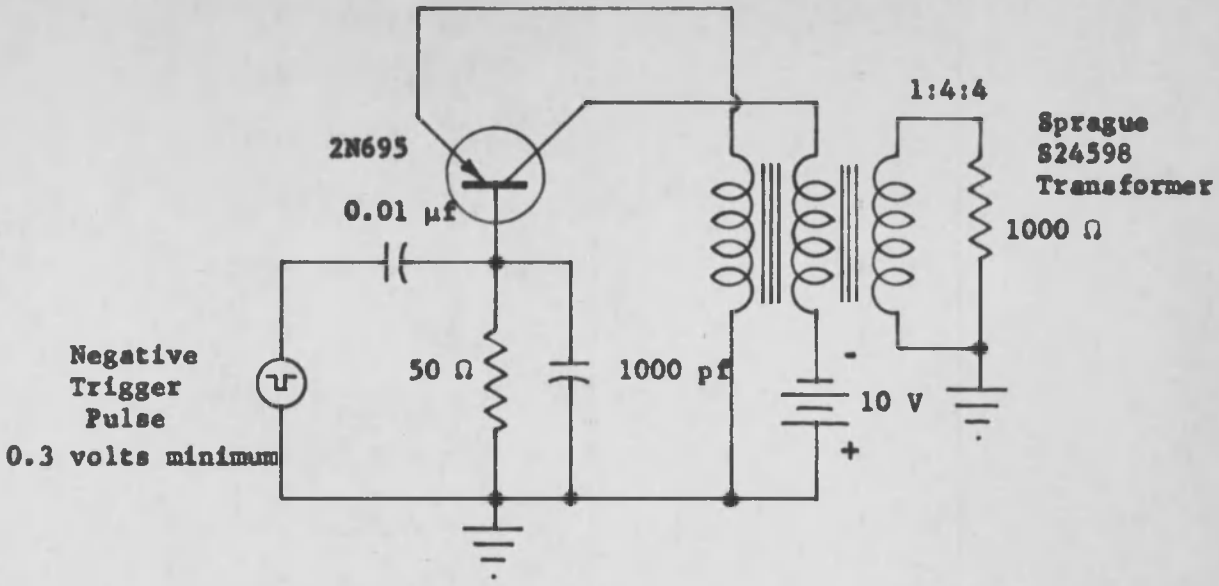
Alpha cutoff frequency	60 mcs (377×10^6 rad/sec.)
Base resistance, r_b	75 ohms
Collector capacitance, C_c (grounded case)	3.5 pfd

Forward alpha, α_o	0.95
Reverse alpha, α_r	0.6
Emitter resistance, r_e	2 ohms
Emitter resistance Optimum rise time, t_r	1.6 ns
Optimum storage time, t_s	2.0 ns
Optimum fall time, t_f	1.3 ns
Maximum collector to base voltage	15 volts
Maximum collector to emitter voltage	15 volts
Maximum emitter to base voltage	3.5 volts

The optimum turns ratio, with m = n, is computed from Equation (5.33) to be $n_0 = 3.90$; for convenience in wiring the approximate value of $n_0 = 4.0$ is used. Using this value for n, with m = n, the positive root of the characteristic equation is found from Equation (5.32) to be $s_1 = 0.54 \times 10^{-9}$ rad/sec. The predicted rise time is determined from Equation (5.14) as $t_r = 4.1$ nanoseconds.

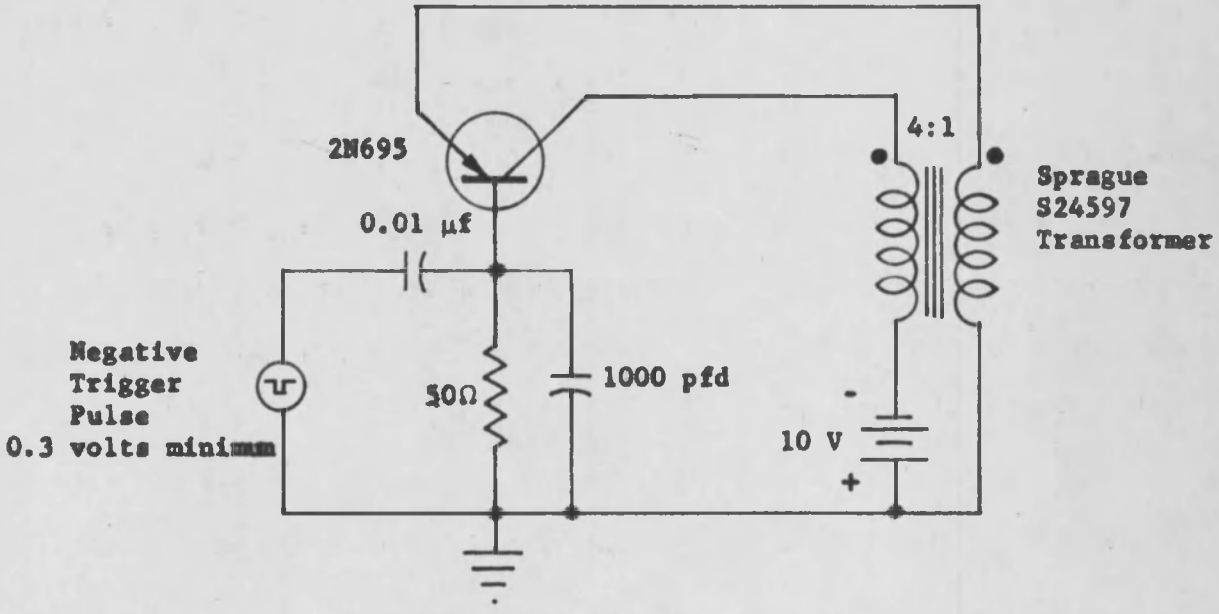
The magnetizing inductance L can be found from Equations (5.27), (5.36), and (5.30) by using the circuit values in Figure 6.1. The approximate solution of these equations, for a pulse width of 1.5 μsec, is L = 190 μhy. Sufficient information is now available to design the pulse transformer for the circuit in Figure 6.1 with the caution that the coefficient of coupling k must be kept close to unity and the leakage inductance λ and distributed capacitance C must be small.

The pulse transformer used here is one constructed by the Sprague Electric Company to the above design specifications for this



CIRCUIT FOR LOADING STUDIES

Figure 6.1



CIRCUIT FOR NO-LOAD STUDIES

Figure 6.2

thesis. It is transformer No. S24598 shown schematically in Figure 6.1 and has the following characteristics:

Turns Ratio	4:1:4 (n:1:m)
Magnetizing Inductance, L	160 μhy
Leakage Inductance, λ	0.6 μhy
Equivalent Capacitance, C	10 pfd (PRI. to SEC_1)
	16 pfd (PRI. to SEC_2)
Toroid Core Dimensions	0.230" O.D. X 0.120" I.D. X 0.060" H
Core Permeability	1500
Turns	28:7:28
Primary Wire Size	No. 38 AWG
SEC_1 Wire Size	No. 34 AWG
SEC_2 Wire Size	No. 38 AWG
Type of Winding	Windings uniformly spaced over 3/4 core, one over another.

6.2 CIRCUITS TESTED

The circuit used for loading studies is shown in Figure 6.1. The transistor and pulse transformer are those selected in the preceding section. The 50 Ω biasing resistor develops the negative trigger across it as discussed in Section 5.5. The load is a 1000 ohm, 1/2 watt, composition resistor. The signal bypass to the biasing resistor is a 1000 pfd mica capacitor whose value is computed to a first approximation from[1]

$$C = \frac{R + r_b}{4 R r_b} t_w \qquad (6.1)$$

where

$R = 50\ \Omega$

$r_b = 75\ \Omega$

$t_w = 1.5\ \mu sec$

Because of the fast responses desired here, high frequency wiring techniques are used in assembling the circuit. All signal leads are kept as short as possible by point-to-point wiring and components are separated significantly. The circuit will fire on a negative trigger with a minimum amplitude of 0.3 volts. The output pulse rise time is a function of the trigger rise time, therefore the trigger should be as fast as possible. The trigger pulse amplitude [illegible]

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[1] D. J. Hamilton, "A Transistor Pulse Generator for Digital Systems," IRE Transactions on Electronic Computers, Vol. EC-7, Sept., 1958, p. 248.

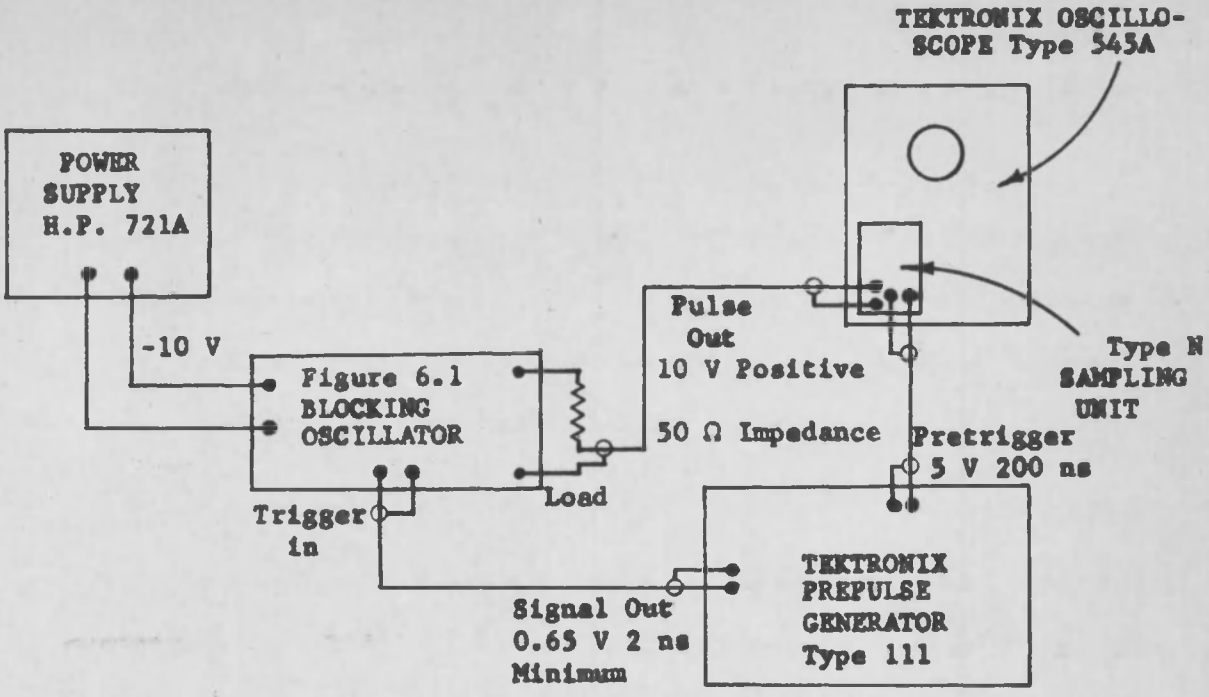
also influences the output pulse rise time and should ideally be around 2 volts.

The circuit in Figure 6.2 is used for no-load studies and has the fastest rise time possible for the circuit components used. The trigger characteristics should be the same as above with the trigger rise time even more critical here.

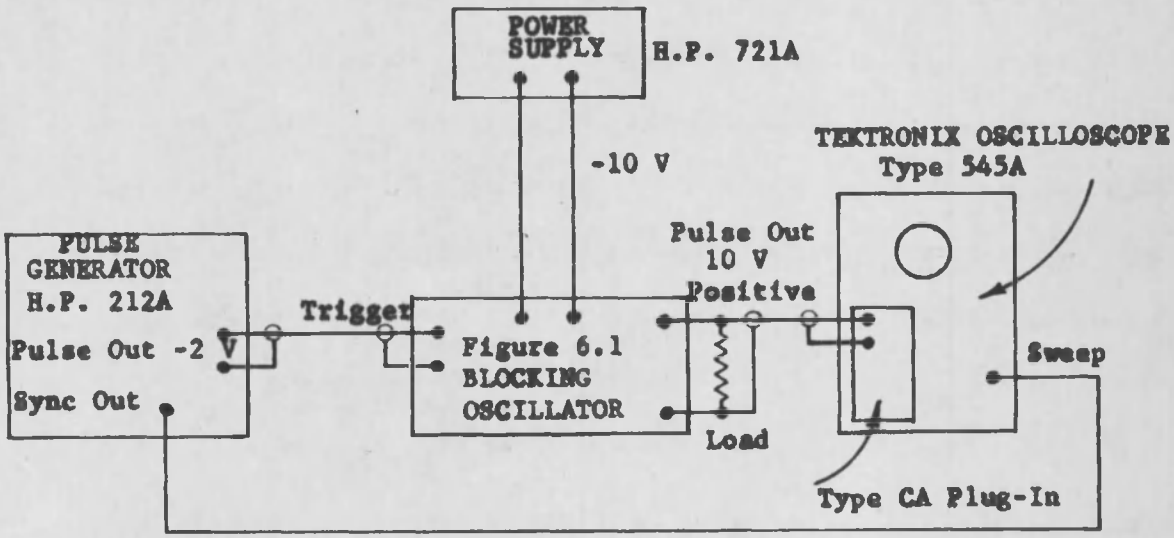
6.3 TEST PROCEDURE

The most difficult requirement in measuring the extremely fast rise times incident here is that the equipment used must have a frequency response sufficiently high to pass these sharp leading edges. This strict requirement can be avoided, however, by using an oscilloscope which merely "samples" one point on the blocking oscillator output waveform everytime it sweeps across that waveform. By advancing the "sample" point after each sweep, the waveform can be traced out by a series of points with relatively low frequency response equipment. A Tektronix Type N Sampling Unit plugged into a Tektronix Type 545A Oscilloscope was used for measuring t_r. The oscilloscope alone has a frequency response of only 30 mcs, but when used in conjunction with the sampling unit, it is capable of measuring rise times of less than 1.0 nanoseconds.

A block diagram of the test setup using this equipment is shown in Figure 6.3(a). The sampling unit requires a pretrigger pulse at least 40 nanoseconds prior to the arrival of the blocking oscillator output pulse in order to trigger its sweep. This pulse is obtained



(a)



(b)

TEST SETUP FOR BLOCKING OSCILLATOR ANALYSIS

Figure 6.3

from a Tektronix Prepulse Generator, Type 111, which also supplies a one nanosecond rise time, 0.65 volt trigger for the blocking oscillator. Unfortunately, the input impedance of the sampling unit is only 50 ohms which means that it must be wired in series with the load. This also means that it cannot be used for no-load measurements.

The test setup in Figure 6.3(b) is used for the no load measurements and to examine the overall output pulse under load conditions. The Type CA Plug-in Unit has a relatively slow rise time of 20 nanoseconds invalidating rise time measurements made with it, but its slower sweep speeds facilitate total response investigation. The Hewlett Packard Type 212A Pulse Generator delivers a negative 2 volt pulse with a rise time of 20 nanoseconds. The power supply used in both Figures 6.3(a) and 6.3(b) is a Hewlett Packard Type 721A which supplies V_{cc} to the blocking oscillator circuits.

In summary, all rise time readings must be taken with the setup in Figure 6.3(a) and all total response studies must be made with the one in Figure 6.3(b). The unloaded blocking oscillator in Figure 6.2 can only be tested with the circuit in Figure 6.3(b). Both test arrangements can employ either trigger source.

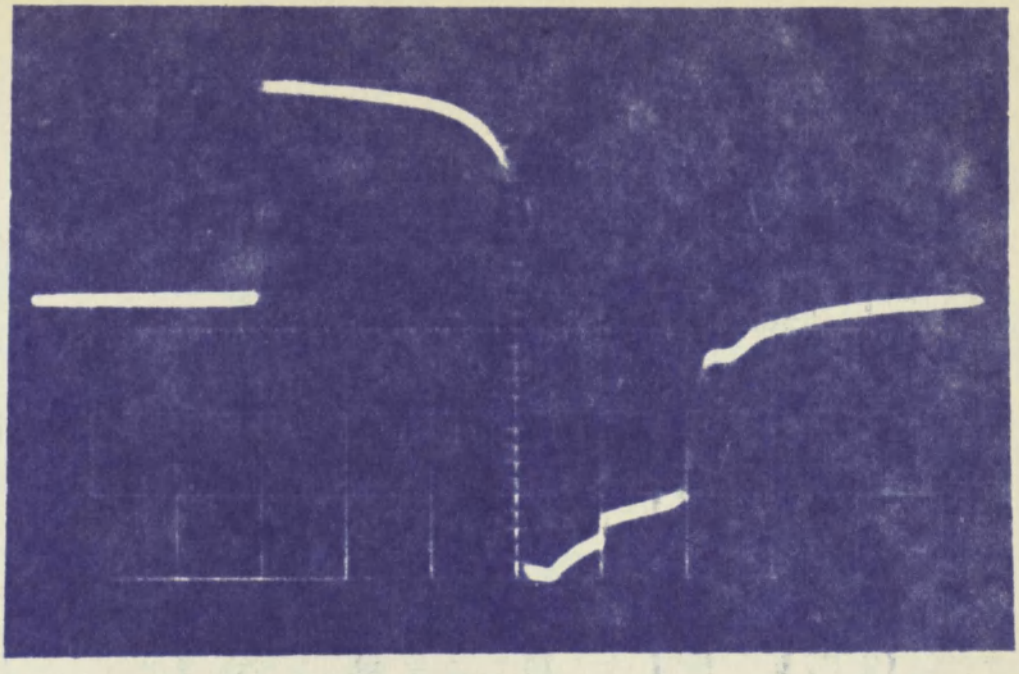
6.4 OUTPUT WAVEFORMS

The output waveforms of the blocking oscillator circuits under test require accurate records for precise comparison with predicted analytical results. The best record, of course, is a clear photograph of the waveform. This method is used here employing a Dumont Type 297 Camera with Polapan 200/Type 42 Polaroid film.

The complete output waveform of the circuit in Figure 6.1, using the test setup in Figure 6.3(b), is shown in Figure 6.4. The pulse width t_w is seen to be 1.5 μsec which is the desired value. The pulse amplitude is 10 volts as required and can be changed by adjusting V_{cc}, but only slightly if the design equations are to remain valid. The jump in the center of the undershoot is caused by removal of the trigger pulse at that instant.

The rise time must be investigated with the test setup in Figure 6.3(a). Figure 6.5 shows the blocking oscillator trigger pulse from the Prepulse Generator. It is a 2 nanosecond negative pulse of 0.65 volts amplitude and a rise time of less than a nanosecond. The rise time of the output pulse is shown in Figure 6.6 using two different sweep scales for clarity. The rise time t_r is seen to be approximately 8 nanoseconds. This compares favorably with the predicted quantity of 4.1 nanoseconds computed in Section 6.1 considering the approximations which were made. Also, since the shunt wiring and component capacitances were not considered, the experimental value of rise time can be expected to exceed the calculated value.

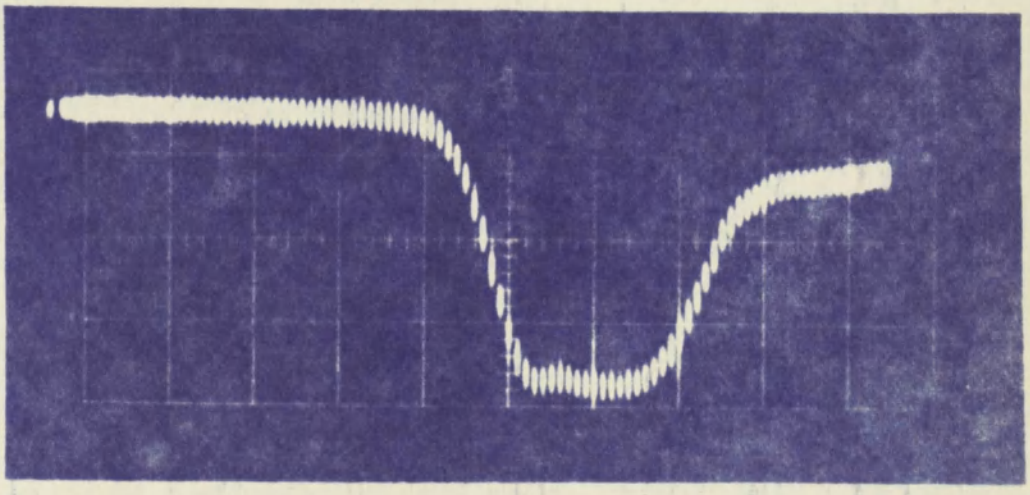
There is essentially no difference observed in the output pulse characteristics when two other 2N695 transistors are substituted in the circuit in Figure 6.1. For this reason, only data obtained using one particular transistor, are presented here.



Scale: Sweep - 0.5 μs/cm
Vertical - 3.5 V/cm

BLOCKING OSCILLATOR OUTPUT WAVEFORM

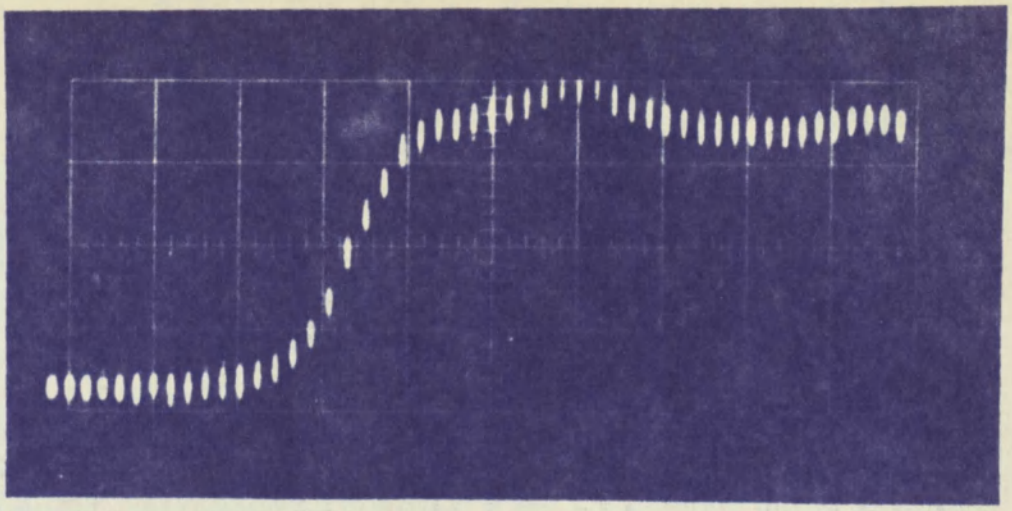
Figure 6.4



Scale: Sweep - 1 ns/cm
Vertical - 0.2 V/cm

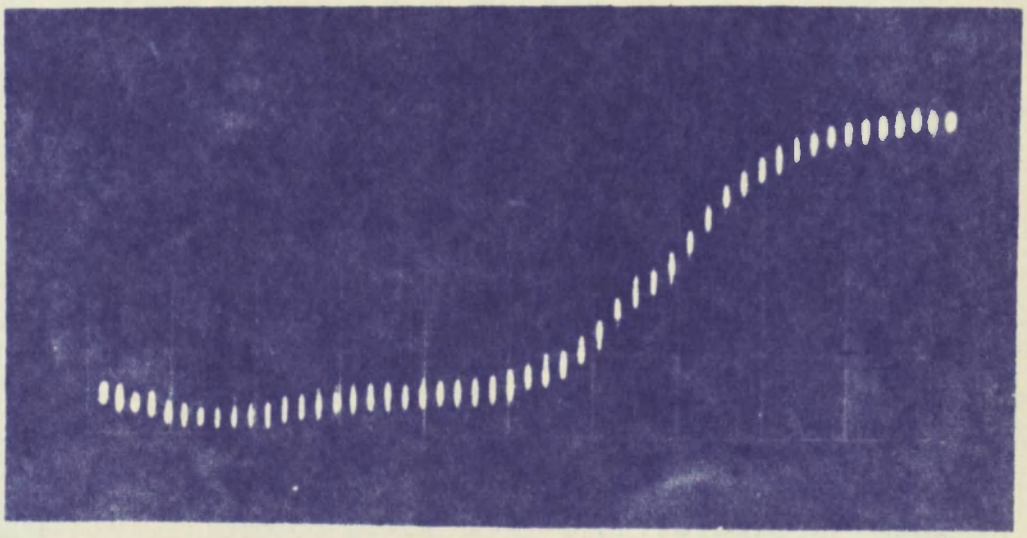
PREPULSE GENERATOR TRIGGER OUTPUT

Figure 6.5



Scale: Sweep - 5 ns/cm
Vertical - 2.5 V/cm

(a)



Scale: Sweep - 2 ns/cm
Vertical - 2.5 V/cm

(b)

OUTPUT PULSE RISE TIME

Figure 6.6

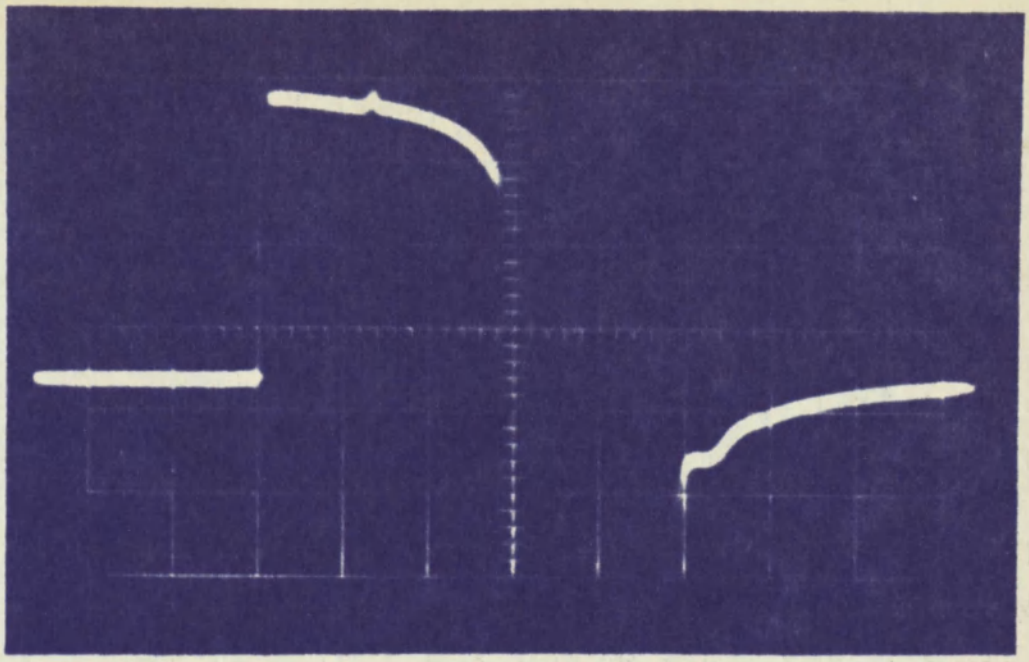
6.5 TIME RESPONSE TO VARIOUS TRIGGERS

The effect of removing the triggering pulse while the pulse top is being generated is discussed in Section 2.3. The irregularity caused by doing this is shown in Figure 6.7 where the trigger pulse in Figure 6.3(b) is approximately 0.7 μsec wide. As evident, the irregularity occurs at the fall time of the trigger pulse.

The triggering discussion in Section 5.5 concludes that the output pulse rise time is a function of the trigger pulse rise time. This effect is illustrated in Figure 6.8 where the time response of the output pulse to two different triggers is indicated. The slow wave is the output pulse response to the trigger from the Hewlett Packard Pulse Generator, used in the test setup in Figure 6.3(a). This trigger has an approximate rise time of 20 nanoseconds and yields a pulse rise time of slightly over this amount. The fast wave of about 8 nanoseconds rise time is derived from the Prepulse Generator trigger of 1 nanosecond, also used in Figure 6.3(a). The desirability of using fast rise triggers for blocking oscillators is clearly indicated.

6.6 TIME RESPONSE TO VARIOUS LOADS

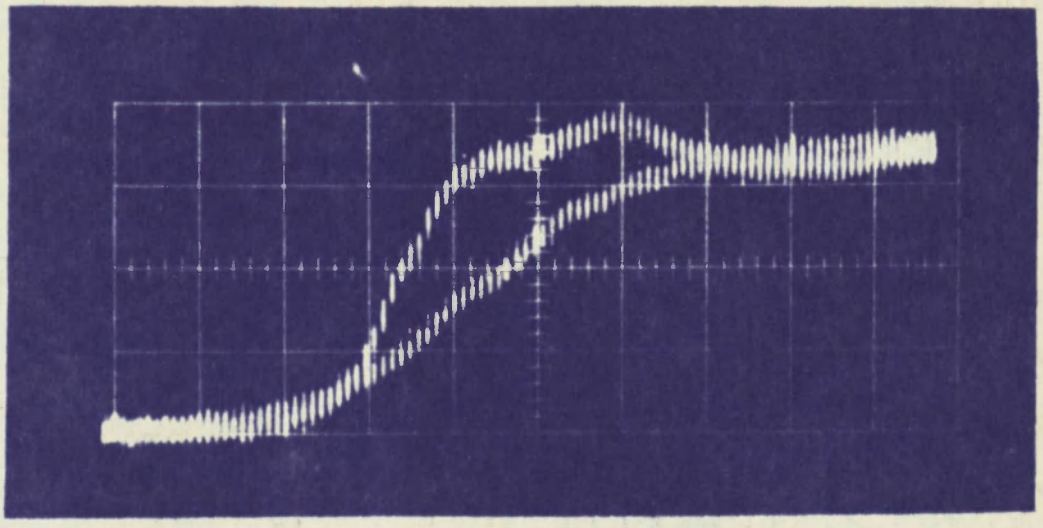
It is apparent from Equations (5.32) and (5.14) that as the load resistance becomes lower, the output pulse rise time increases. Evidence of this is shown in Figure 6.9. The upper curve is obtained with a load of 100 ohms and has a rise time of approximately 15 nanoseconds. The lower curve, which corresponds to a load of 1000 ohms, has a rise time of 8 nanoseconds.



Scale: Sweep - 0.5 μs/cm
Vertical - 3.0 V/cm

PULSE TOP WITH IRREGULARITY

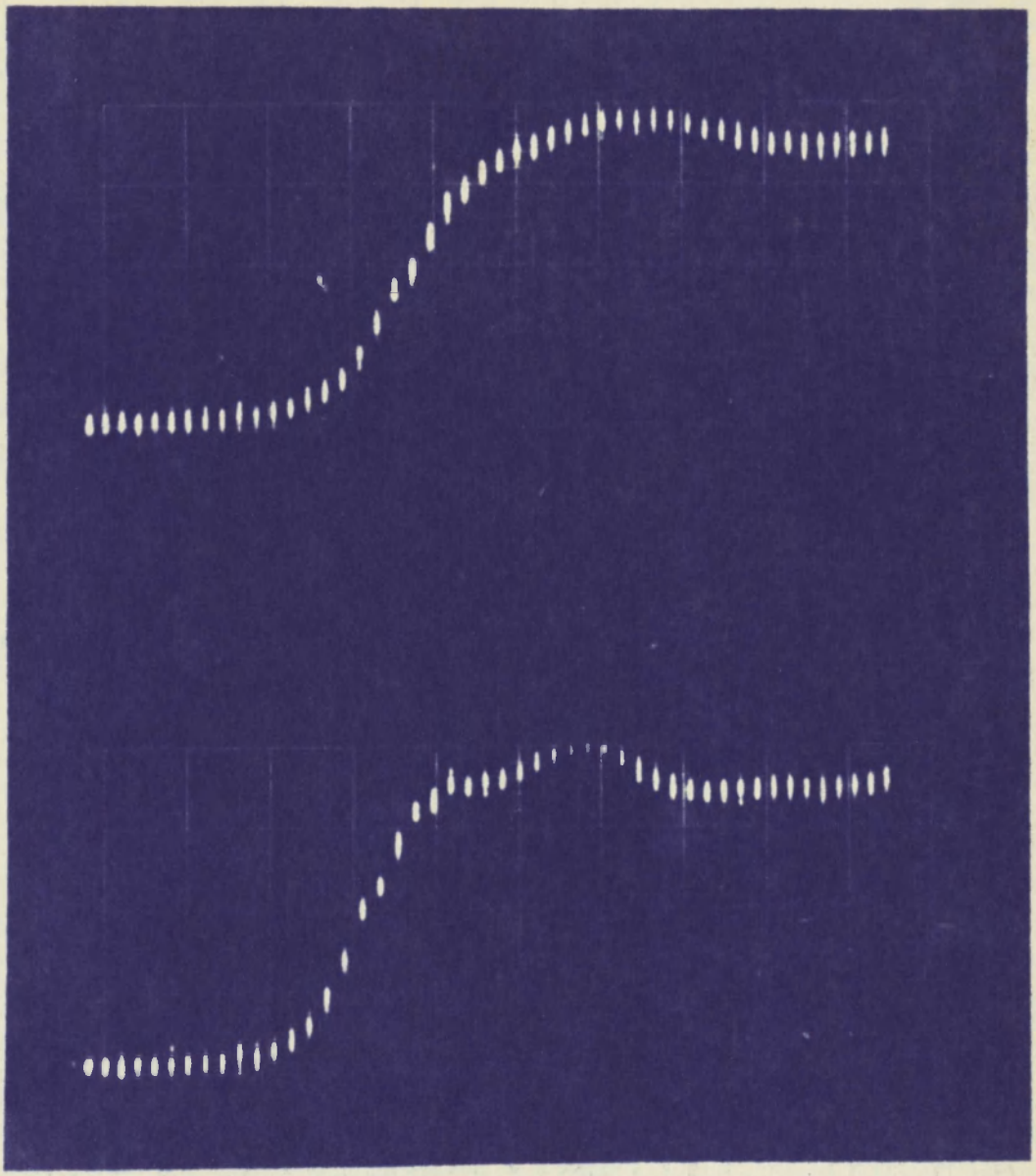
Figure 6.7



Scale: Sweep - 5 ns/cm
Vertical - 2.5 V/cm

TIME RESPONSE TO DIFFERENT TRIGGERS

Figure 6.8



Scale: Sweep - 5 ns/cm
Vertical - 2.5 V/cm

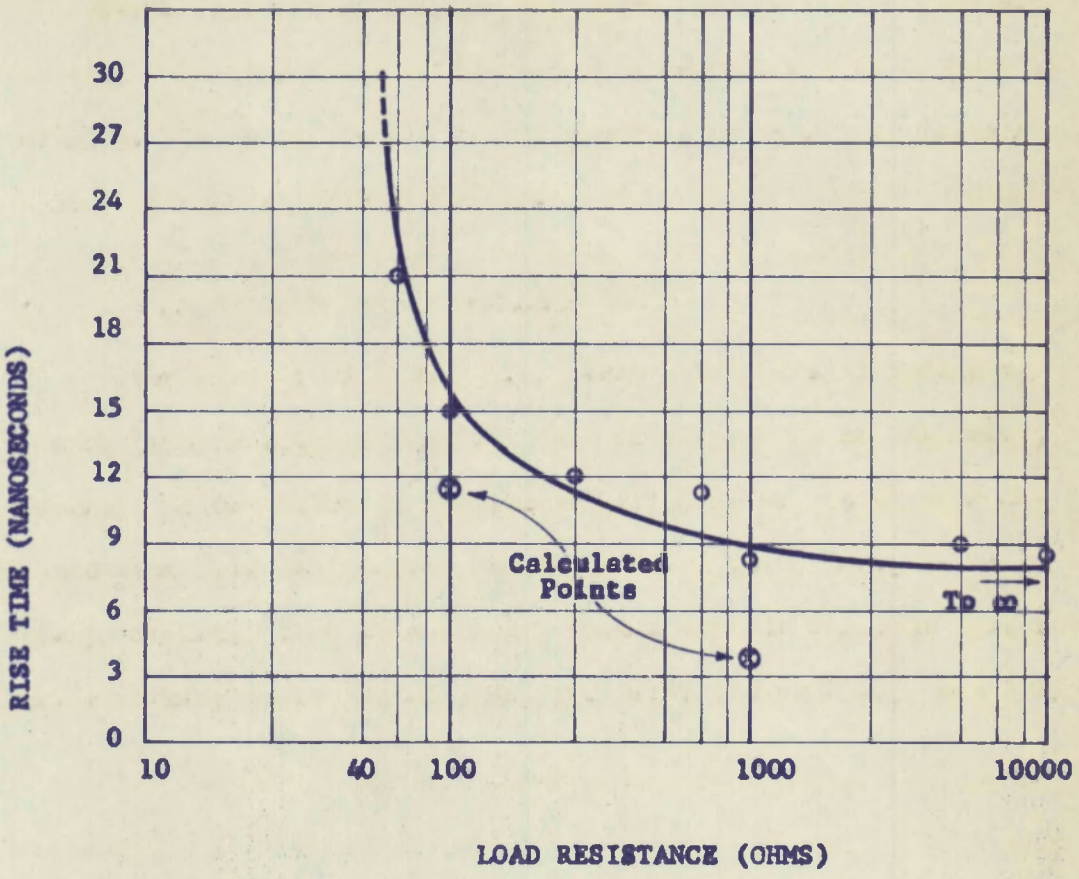
TIME RESPONSE TO DIFFERENT LOADS

Figure 6.9

The time response of the output pulse for several different values of load is shown in Figure 6.10. This graph shows experimental rise time versus load resistance and two calculated points for comparison. The rise time approaches approximately 6 nanoseconds as R_L goes to infinity. It is impossible to get readings below a load resistance of 56 ohms because of overloading.

6.7 LONG TERM STABILITY AND PERFORMANCE

The circuit in Figure 6.1, after four weeks of continual pulsing using a trigger from the Hewlett Packard Pulse Generator, evidenced no variation in its output performance. Using data obtained from Sprague Electric Company and Motorola, Inc., it is safely predicted that this circuit should exhibit constant performance characteristics for at least two years and probably much longer.



EXPERIMENTAL TIME RESPONSE TO VARIOUS LOADS

Figure 6.10

Chapter 7

CONCLUSIONS

7.1 GENERAL

The fast rise blocking oscillator design procedure presented in Section 5.7 is valid to a first order of approximation. It may be used with high alpha cutoff frequency transistors that have low $r_b C_c$ products. As faster rise time pulses are required, the pulse transformer becomes the limiting factor in design. To accommodate the higher alpha cutoff frequencies in the design procedure, the pulse transformer must have smaller and smaller leakage inductance and distributed capacitance. The practical limit of this diminution defines the extent to which switching speeds can be increased.

In using the design procedure the assumptions and approximations used in deriving the design equations must be adjudged in terms of the particular design problem under consideration. For instance, if the specified rise time is rather slow, the assumption of zero magnetizing current at the beginning of the pulse top is invalidated. And in contrast, if design for an ultra-fast rise time calls for an alpha cutoff frequency above the order of 200 megacycles, then the design equations are bounded by practical pulse transformer limitations. However, if these design equations are used with caution and insight,

they are quite valuable in the design of fast rise blocking oscillators.

7.2 AREAS FOR FURTHER STUDY

Since the transistor version of the blocking oscillator is still relatively new there remain many areas of application to be investigated. For example, the area of significant power output from this circuit has generally been avoided until recently and would justify examination.

There are still enigmas surrounding the question of pulse width dependence on circuit parameters other than magnetizing inductance. For instance, means by which pulse width can be regulated versus changing V_{cc} warrants consideration.

It is evident that the pulse transformer will become more and more a limitation to fast rise pulse design as available transistor alpha cutoff frequencies increase, seemingly without bound. It might be possible, therefore, to eliminate the pulse transformer altogether and use in its stead some other comparable storage device which would not limit operation. Such a device might be a voltage variable capacitor whose storage capabilities change with varying voltage across it. Undoubtedly other possibilities may suggest themselves to the reader.

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