DESIGN OF A DIRECT-COUPLED TRANSISTORIZED NEGATIVE-IMPEDANCE CONVERTER

by

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ABSTRACT

A circuit is developed which is capable of Negative-Impedance Converter action at zero frequency; experimentally determined compensation extends the useful range of the device to approximately 100KC. The steady-state and transient responses are graphically recorded. The capabilities and limitations of the circuit are discussed.

The methods of Active RC Synthesis are employed to obtain a simple second-order, variable-Q, bandpass filter; a center frequency of 100 cps emphasizes the potential advantages of active methods over conventional passive filters at low frequencies.

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APPROVAL BY THESIS DIRECTOR

This thesis has been approved on the date shown below:

L P Hueltman

LAWRENCE P. HUELSMAN
Associate Professor of
Electrical Engineering

April 30, 1963
Date

ACKNOWLEDGMENT

This thesis was prepared under the supervision of Dr. L. P. Huelsman; his unfailing patience, enthusiasm, and encouragement are gratefully acknowledged. The friendly encouragement, freely given by all members of the faculty and staff of the department, made a trying time much easier.

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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

SECTION 1

INTRODUCTION

Modern network theory has recently recognized several new, ideal elements[1r*]. Negative-Immittance Converters[3r] abbreviated NIC, are prominent members of this new group. NIC(s) are often characterized by their ABCD parameters

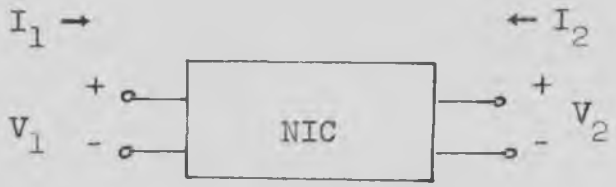


FIG. 1

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \pm 1 & 0 \\ 0 & \mp 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad (1)$$

Choice of the upper sign yields a Current-Inversion Negative-Immittance Converter, abbreviated INIC; a 3-terminal, controlled-source representation of such an ideal two-port device is shown below.

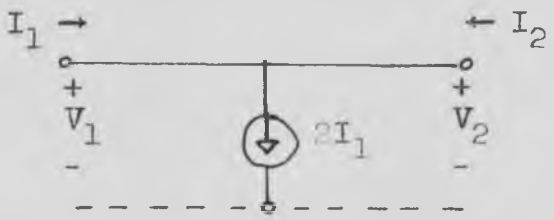


FIG. 2

*References are listed on page 43

Realization of very general rational network functions has been achieved by imbedding Gyrators[lr], NIC(s), or simply controlled sources in RC networks[lr]; the systematic study of such methods has received the name Active RC Synthesis. Several RC realization schemes of practical importance employ the INIC.

Potential applications in the areas of Automatic Control and Analog Simulation suggest the desirability of operation at ultra-low frequencies.

This thesis undertakes the design of an INIC circuit capable of zero-frequency operation.

SECTION 2

PRELIMINARY DISCUSSION

2.1 The Larky Circuit

A survey of the literature reveals a circuit proposed by Larky[2r] as the only design with which it is feasible to obtain unbalanced INIC action. The essential Larky circuit is diagrammed below.

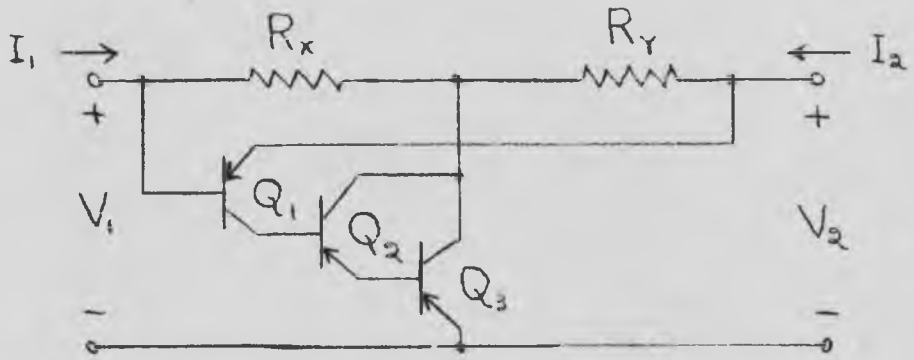


FIG. 3

Let $r_b = r_e = V_{be} \approx 0$, and $r_c >> R_x$ or R_y; the expression given by eq. (2) obtains:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -k \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad (2)$$

Equation (3) expresses the current transfer ratio.

$$-k = \frac{\left[\beta_1(\beta_2\beta_3+\beta_2+\beta_3+1)R_y - (\beta_1+1)R_y - R_x\right]}{\left[\beta_1(\beta_2\beta_3+\beta_2+\beta_3+1)R_x + (\beta_1+1)R_y + R_y\right]} \qquad (3)$$

Assume $R_x = R_y$, and $\beta_1 = \beta_2 = \beta_3 = \beta$

$$-k = \frac{(\beta^3+2\beta^2-2)}{(\beta^3+2\beta^2+2\beta+2)} \qquad (4)$$

$$-k = \frac{(\beta-0.84)(\beta^2+2.84\beta+2.39)}{(\beta+1.54)(\beta^2+0.46\beta+1.29)} \qquad (5)$$

Let $\beta = \frac{\beta_0\omega_0}{S+\omega_0}$, $S = \beta_0\omega_0 p$; and assume $\beta_0^2 >> \beta_0 >> 1$.

$$-k \approx \frac{1.01(p-1.19)(p^2+1.19p+0.42)}{(p+0.65)(p^2+0.36p+0.77)} \qquad (6)$$

The idealized analysis culminating in eq. (6) reveals three important features of the Larky circuit: the circuit is non-reciprocal; the input impedance at port I is unstable; and the current transfer ratio has complex poles.

2.2 Zero-Frequency Operation

Zero-frequency operation requires that some means be made available to distinguish between bias potentials and zero-frequency signals (see Voltage Null Control in appendix B).

Direct coupling compounds the difficulty of obtaining correct bias for the transistors; some simplification results from the use of both n-p-n and p-n-p type transistors (see Bias Adjustments in appendix B).

2.3 The Modified Larky Circuit

Typical applications will require that the INIC be driven by a high-impedance source. Bias considerations will require the circuit to be driven at port I. The input impedance at port I was made OC stable by the addition of another CE stage.

The output impedance of a CE stage was too low to work with the desired range of impedance levels; this difficulty was corrected by the addition of a CB stage.

The final circuit employed, minus compensation and bias networks, is shown in Fig. 4.

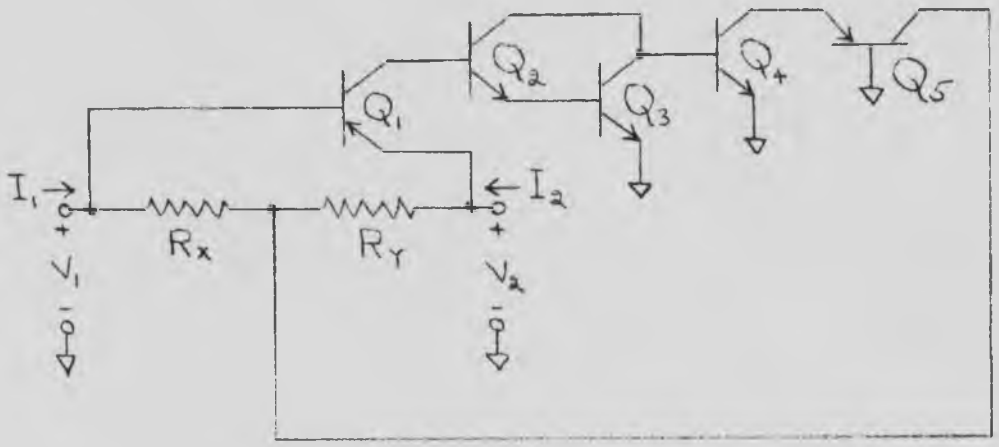


FIG. 4

2.4 Design Requirements

Solely as a matter of convenience, the circuit of this thesis was designed to operate with signal magnitudes of the order of 0.5 volt peak to peak.

A median impedance level of 5K ohms was chosen for the termination; terminating impedances from 1K to 9K ohms are satisfactorily accommodated by the circuit. Large biasing resistors are obtained with the use of ±150 volt supplies; the high impedance level of the bias networks relieves signal loading and swamps out changes in the external circuit.

DC operation requires the terminating impedance to pass a portion of the emitter bias current of transistor Q_1. The principle of NIC action guarantees that this requirement can always be satisfied.

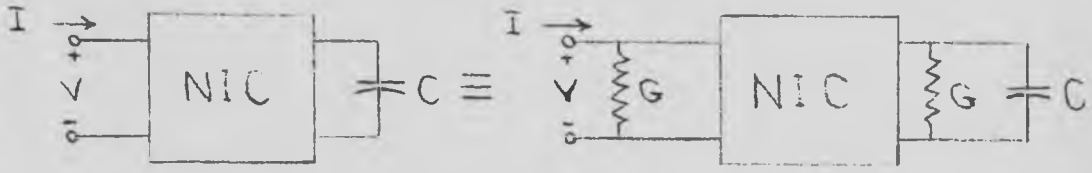


FIG. 5

2.5 Practical Problems

Quantitative solutions of the problems mentioned here were obtained experimentally. A detailed discussion of specific circuits and their purposes is presented in appendix A.

The loss of high-frequency gain is compensated by the use of RC interstage coupling networks. Peaking inductors, large enough to be of value, introduced ringing effects that were uncontrollable under changes in the terminating impedance; their use was accordingly avoided.

The interstage networks and some additional RC networks minimize the phase distortion.

Feedback swamps out the fluctuations in component values, improves the bandwidth, and stabilizes the amplifier against possible regeneration.

Two independent controls are provided to compensate the effects of the external circuit; these same controls are used to suppress the characteristic response of the amplifier (see C_1 and C_2 in appendix B).

SECTION 3

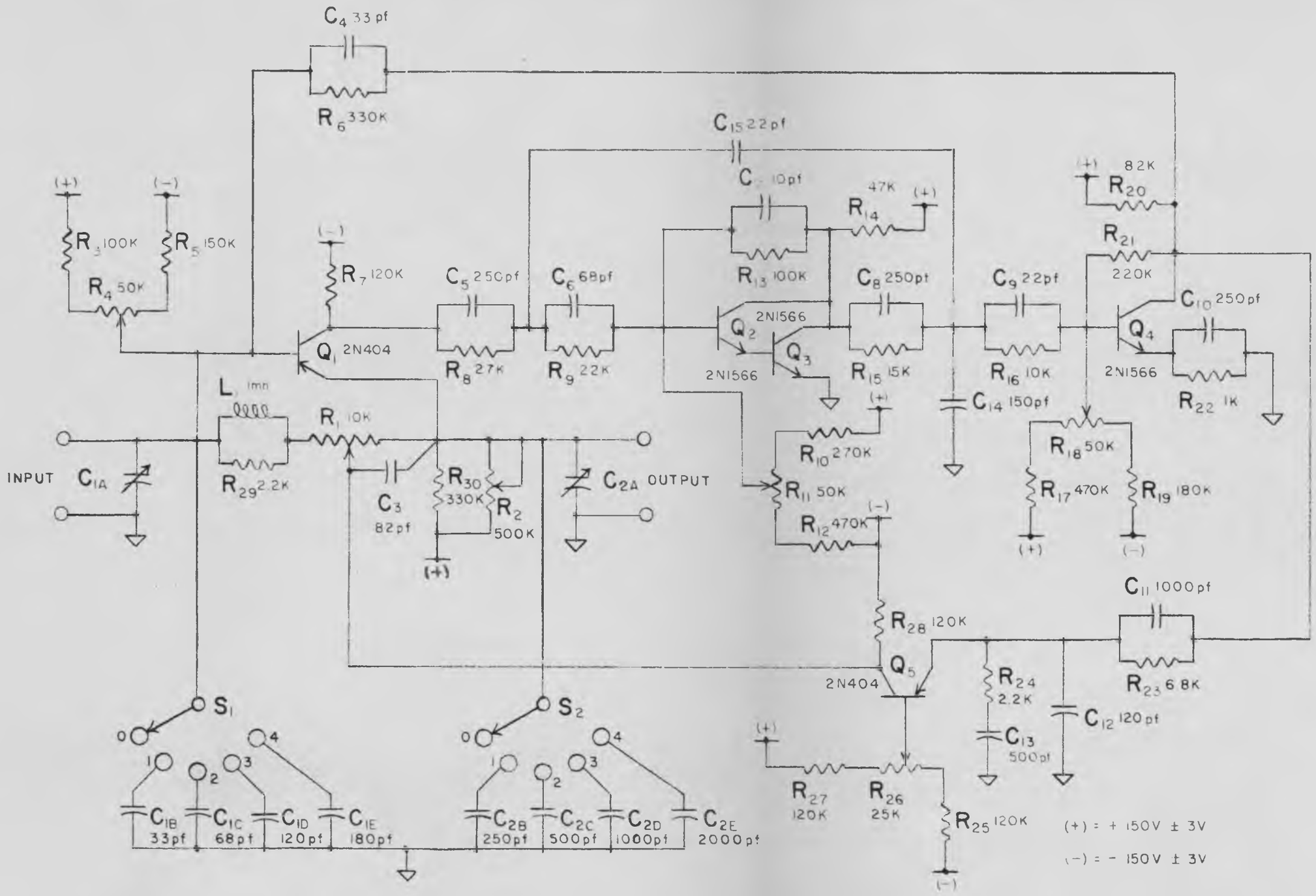
THE ACTUAL CIRCUIT

The complete schematic diagram is presented in Fig. 6 on page 9; a comprehensive discussion may be found in the appendices.

Figures 7, 8, 9 and 10 are photographs of the physical unit; the position and identification of controls are easily seen.

TRANSISTORIZED NEGATIVE IMPEDANCE CONVERTER (INIC)

DESIGNED AND DRAWN BY EDWYN D. SMITH



ALL RESISTORS ARE ± 10%, 1/2W

ALL CAPACITORS ARE ± 10%, 200V

FIG 6

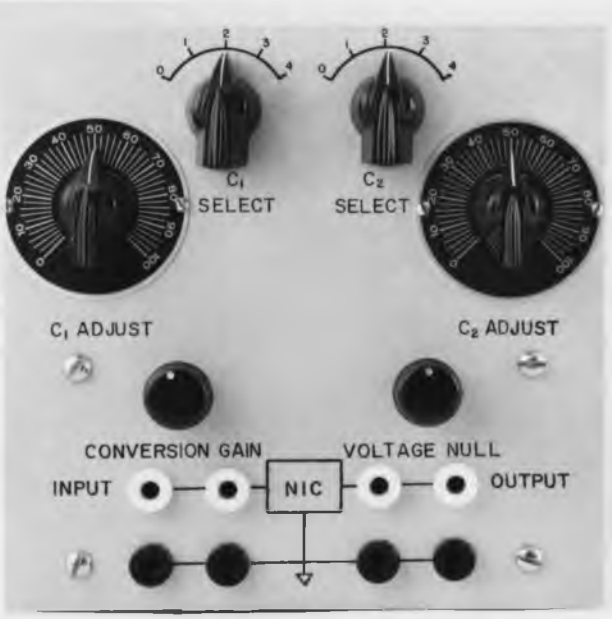


Fig. 7 Front View

Fig. 8 Rear View

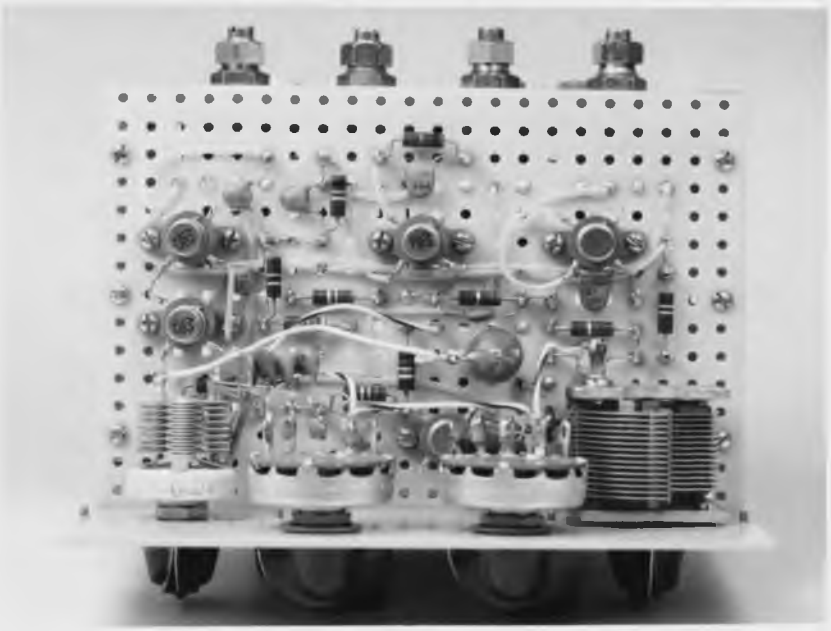


Fig. 9 Top View

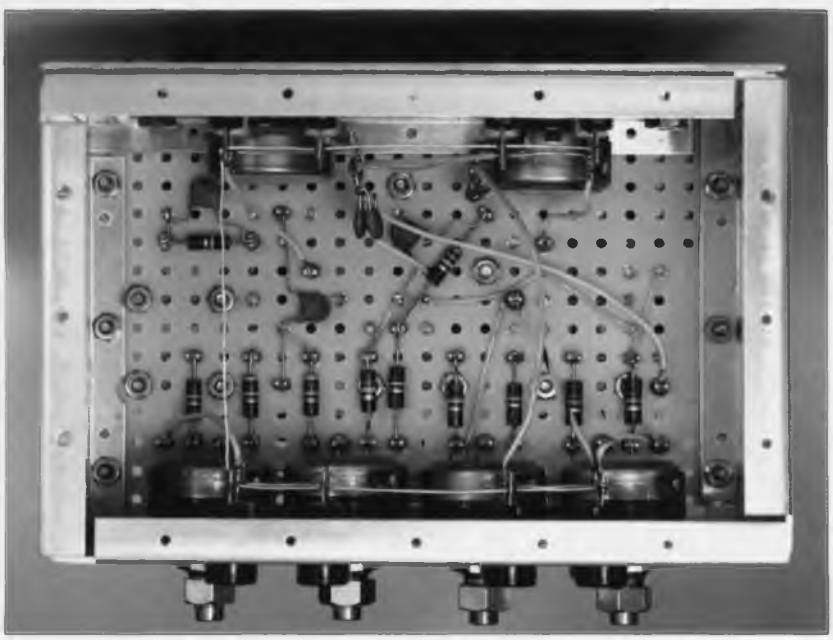


Fig. 10 Bottom View

SECTION 4

PERFORMANCE MEASUREMENTS

Performance measurements were obtained with the configuration shown below.

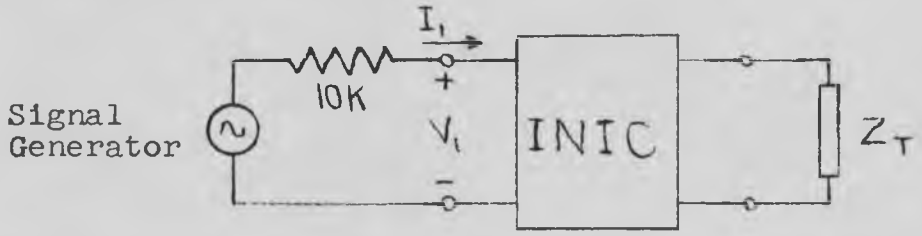


FIG. 11

Define: $|Z_1(j\omega)| = \dfrac{|V_1(j\omega)|}{|I_1(j\omega)|}$

$\Phi(j\omega)$ = the phase angle of $Z_1(j\omega)$

Plots of $|Z_1(j\omega)|$ and $\Phi(j\omega)$ versus frequency are given for each of four different terminations; the theoretical response is plotted on the same graph for comparison.

Photographs of the total response, when excited by a symmetrical 10KC square wave, are presented for the same four terminations. Three of the terminations are purely resistive; expanded-scale photographs, showing the transient response in detail, are provided for these. The list of figures containing the data referred to above is tabulated on the following page.

(a) Z_t = 1K Resistance

Steady-State Response: Fig. 12, page 14

Square-Wave Response: Fig. 13, page 15

Transient Response: Fig. 14, page 15

(b) Z_t = 5K Resistance

Steady-State Response: Fig. 15, page 16

Square-Wave Response: Fig. 16, page 17

Transient Response: Fig. 17, page 17

(c) Z_t = 9K Resistance

Steady-State Response: Fig. 18, page 18

Square-Wave Response: Fig. 19, page 19

Transient Response: Fig. 20, page 19

(d) Z_t = 

Steady-State Response: Fig. 21, page 20

Square-Wave Response: Fig. 22, page 21

STEADY-STATE RESPONSE

$\frac{|V_1(j\omega)|}{|I_1(j\omega)|_{1K}}$

Z_t = 1K Resistance

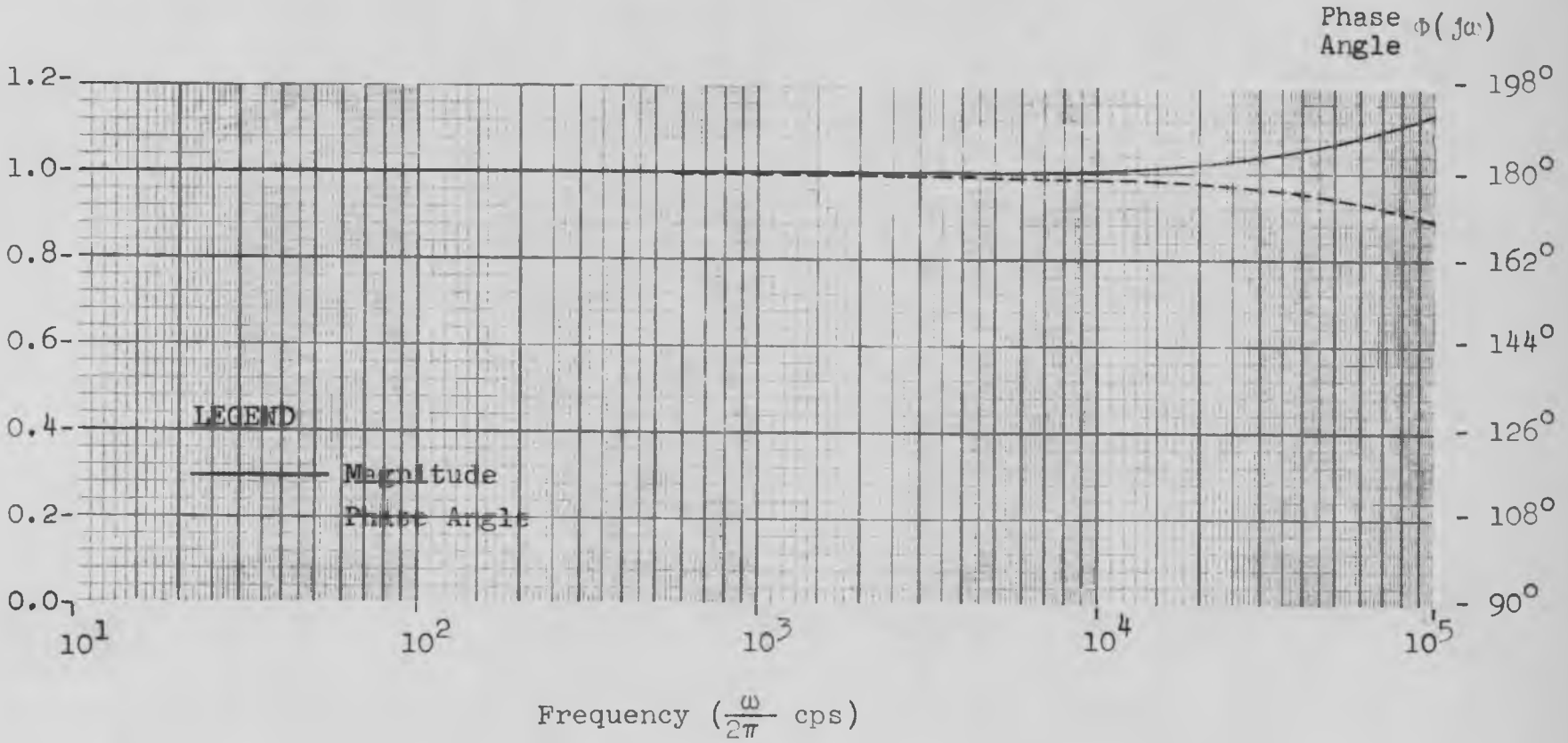


FIG. 12

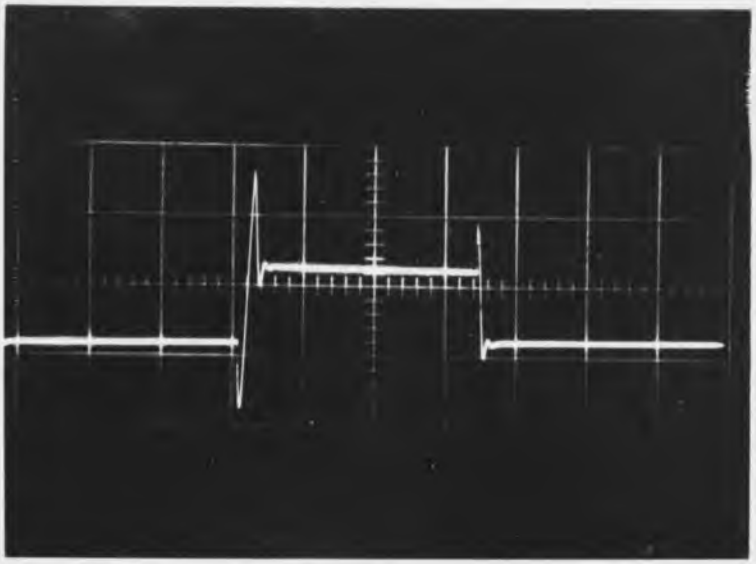


Fig. 13

Response of -1K Resistance to a 10KC Square Wave
Sweep Speed: 15μSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

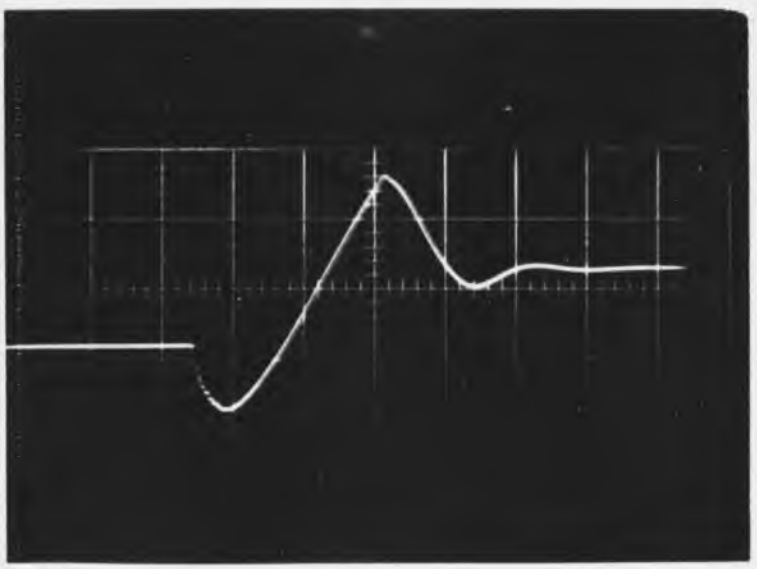


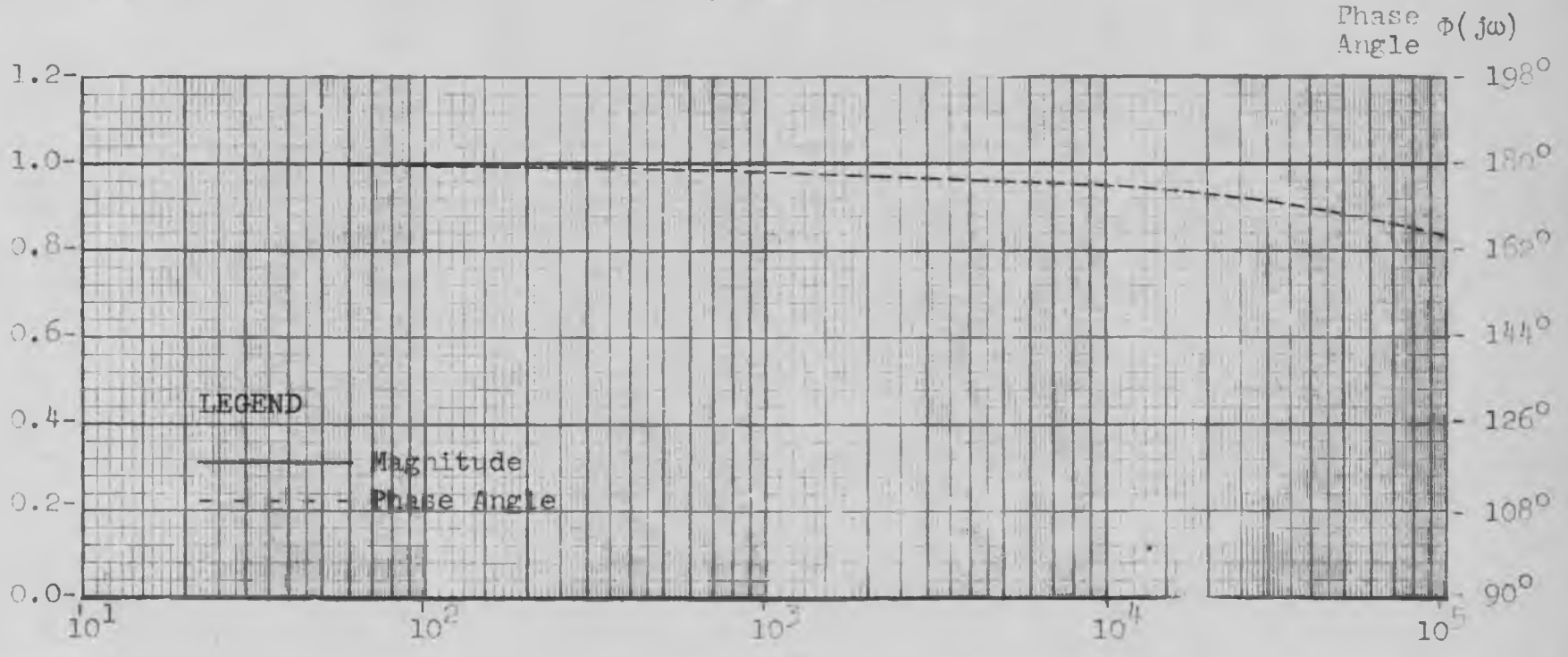
Fig. 14

Transient Response of -1K Resistance
Sweep Speed: 1.0μSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

STEADY-STATE RESPONSE

$\frac{|V_1(j\omega)|}{|I_1(j\omega)|}$ K

R_t = 5K Resistance



Frequency ($\frac{\omega}{2\pi}$ cps)

FIG. 15

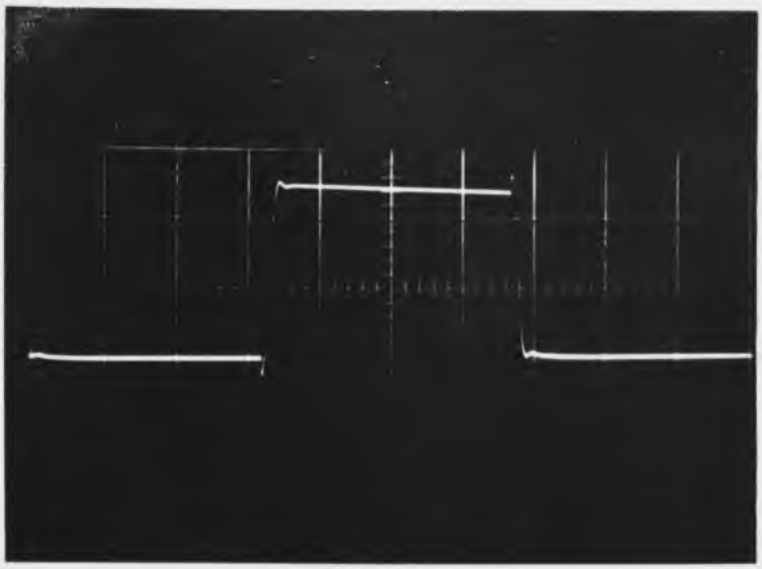


FIG. 16
Response of -5K Resistance to a 10KC Square Wave
Sweep Speed: 15μSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

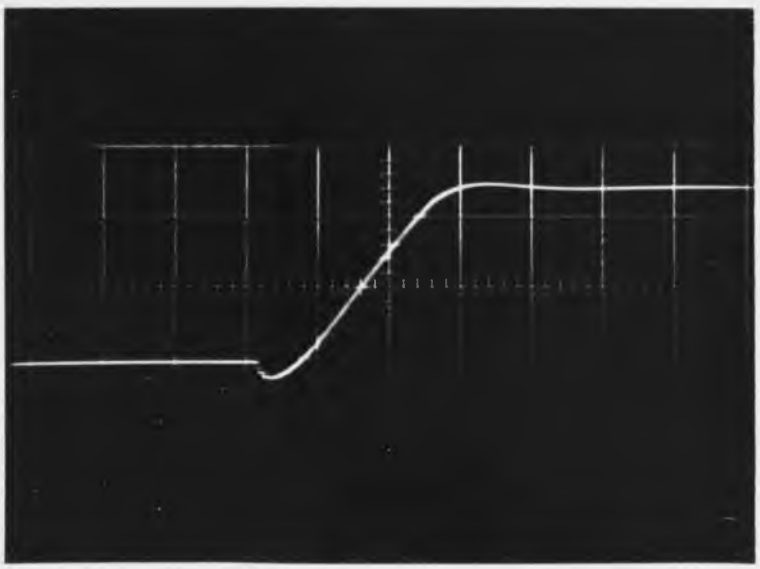
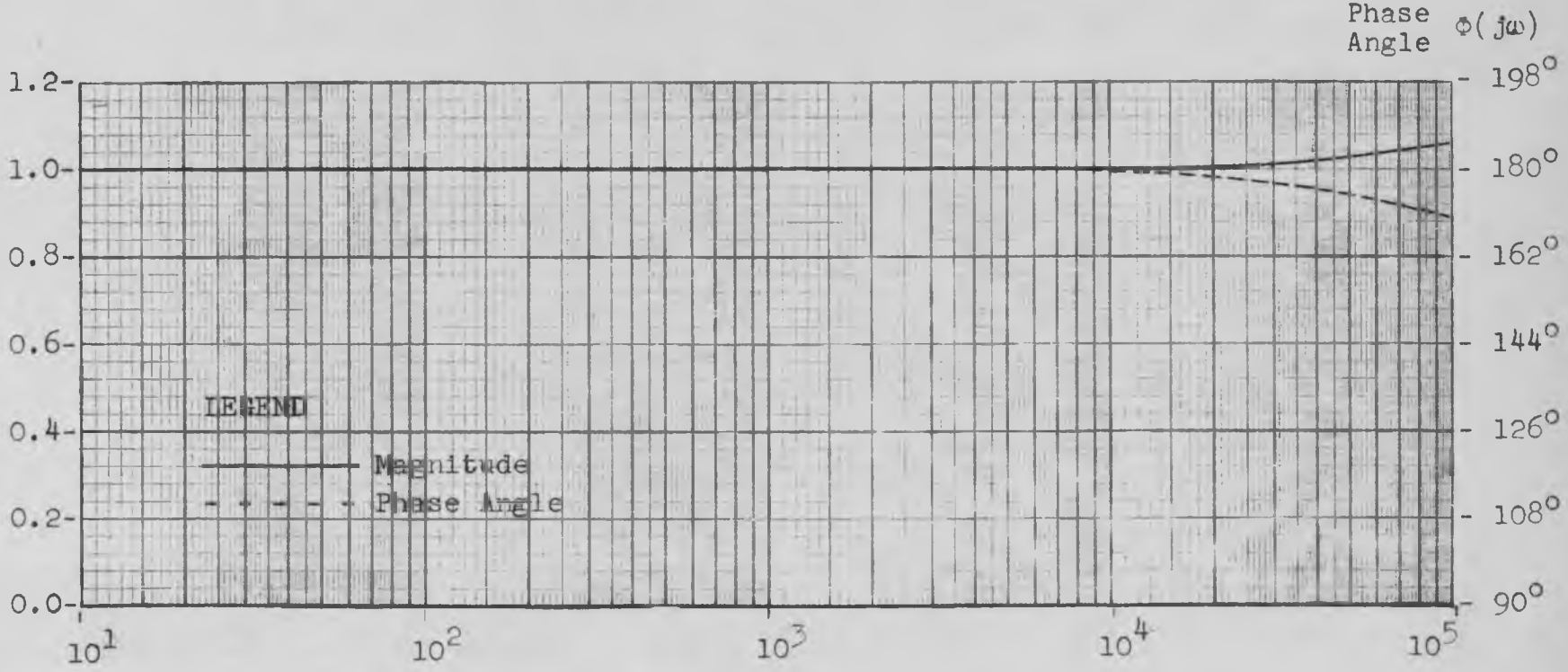


FIG. 17
Transient Response of -5K Resistance
Sweep Speed: 1.0μSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

STEADY-STATE RESPONSE

$\frac{|V_1(j\omega)|}{|I_1(j\omega)|_{9K}}$

Z_t = 9K Resistance



Frequency ($\frac{\omega}{2\pi}$ cps)

FIG. 18

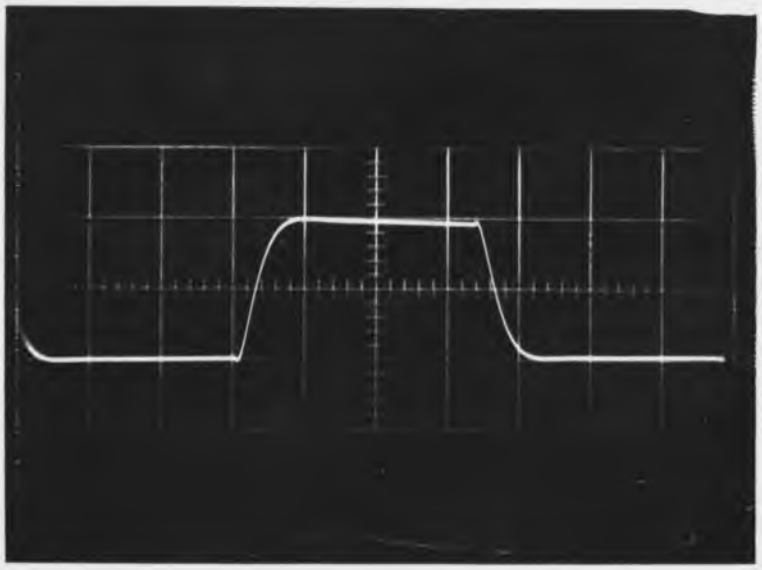


Fig. 19

Response of -9K Resistance to a 10KC Square Wave
Sweep Speed: 15μSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

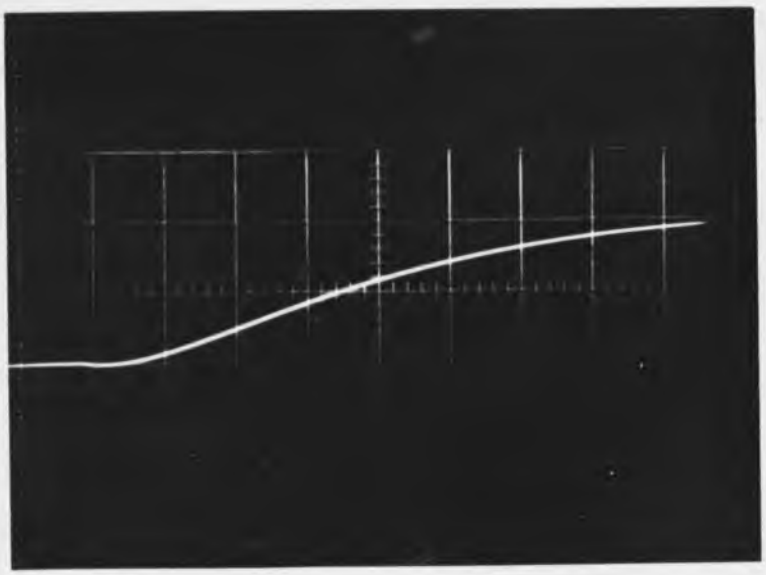


Fig. 20

Transient Response of -9K Resistance
Sweep Speed: 1.0μSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

STEADY-STATE RESPONSE

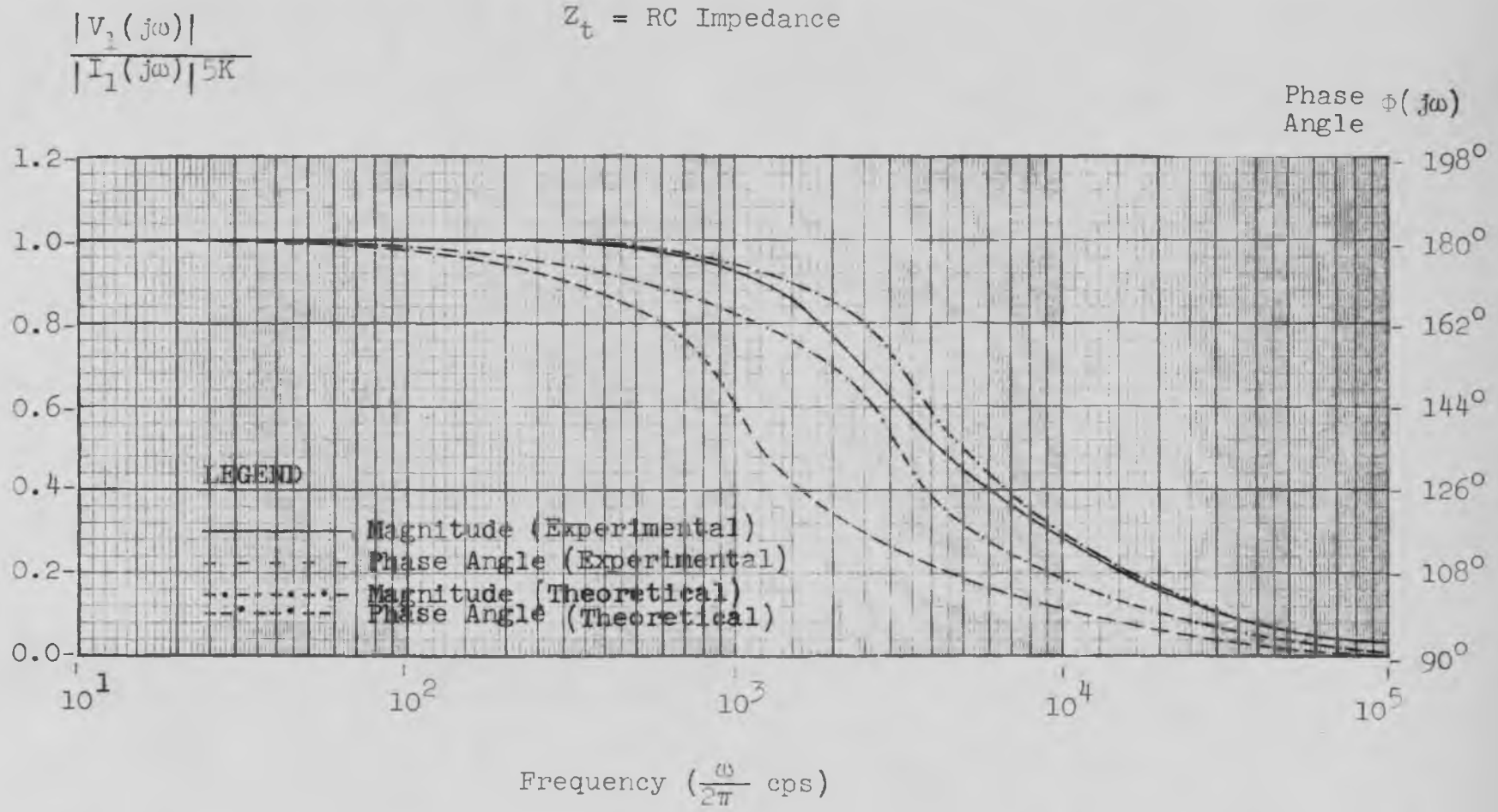


FIG. 21

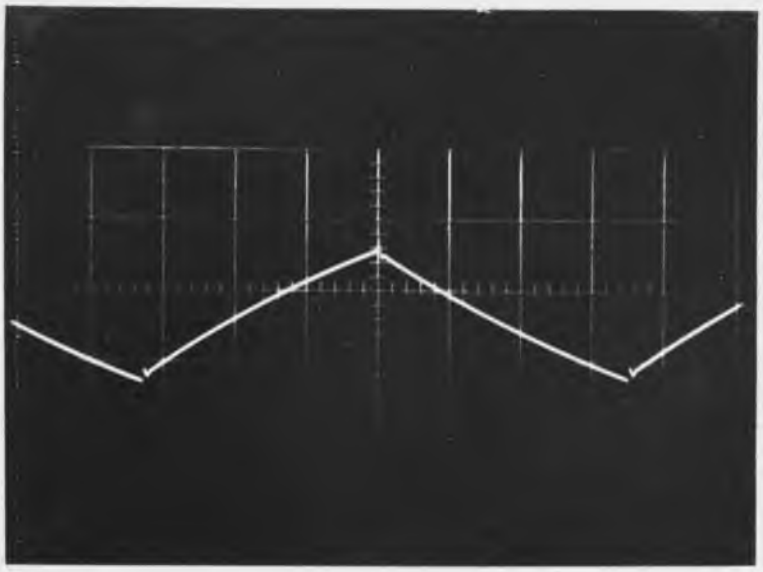


Fig. 22

Response of -RC Impedance to a 10KC Square Wave
Sweep Speed: 15μSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

SECTION 5

SAMPLE RC REALIZATION

5.1 Discussion

The circuit of Fig. 23 is derived from the Yanagisawa[4r] synthesis of a voltage transfer function.

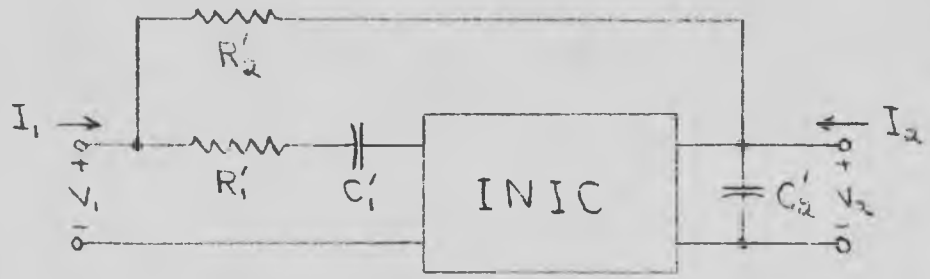


FIG. 23

A simple node analysis will verify the results shown below.

$$\frac{V_2}{V_1} = \frac{\dfrac{(R_1'-R_2')S}{R_1'R_2'C_2'} + \dfrac{1}{R_1'R_2'C_1'C_2'}}{S^2 + \left(\dfrac{1}{R_1'C_1'} + \dfrac{1}{R_2'C_2'} - \dfrac{1}{R_1'C_2'}\right)S + \dfrac{1}{R_1'R_2'C_1'C_2'}} \qquad (7)$$

When $\dfrac{V_2}{V_1} = \dfrac{\omega_n^2}{S^2+2\zeta\omega_n S+\omega_n^2}$, there obtains

$$R_1' = R_2' = R \qquad (8)$$

$$\omega_n = \frac{1}{R\sqrt{C_1'C_2'}} \qquad (9)$$

$$\zeta = \frac{\sqrt{C_1' C_2'}}{2C_1'} \tag{10}$$

R is arbitrarily chosen as 5K ohms to provide a convenient impedance level. To emphasize the low-frequency capabilities of the circuit, ω_n is maintained at 200π rps. C_1' and C_2' are successively chosen to yield values of the damping factor equal to 1.0, 0.2, 0.05, and 0.01; the very low values of damping factor are intended to illustrate the ability of the circuit to function as a simple high-Q filter at low audio frequencies.

The quality factor of the function under consideration is not well defined. If $\zeta \leq 0.2$, then two finite, non-zero 3 db cutoff frequencies exist. Q may then be defined by eq. (11).

$$Q \triangleq \frac{\omega_0}{BW} \tag{11}$$

where: $\dfrac{|V_2(j\omega_0)|}{|V_1(j\omega_0)|}$ is a maximum

The quantity ω_0/BW tends asymptotically to $1/2\zeta$ as ζ tends to zero; eq. (12) provides a satisfactory approximation; this approximation is derived in appendix C.

$$Q \approx \frac{1}{2\zeta} \quad , \zeta \leq 0.2 \tag{12}$$

The values of Q, corresponding to the values of ζ, are approximately 0.5, 2.5, 10, and 50.

5.2 Experimental Verification

The circuit of Fig. 23 was set up using the INIC of this thesis; the magnitude of the steady-state response was obtained and compared with the theoretical; the step-function response was recorded photographically. The results obtained are presented in the Figures listed below.

$\zeta = 1.0$

Steady-State Response: Fig. 24, page 25

Step-Function Response: Fig. 25, page 26

$\zeta = 0.2$

Steady-State Response: Fig. 27, page 27

Step-Function Response: Fig. 26, page 26

$\zeta = 0.05$

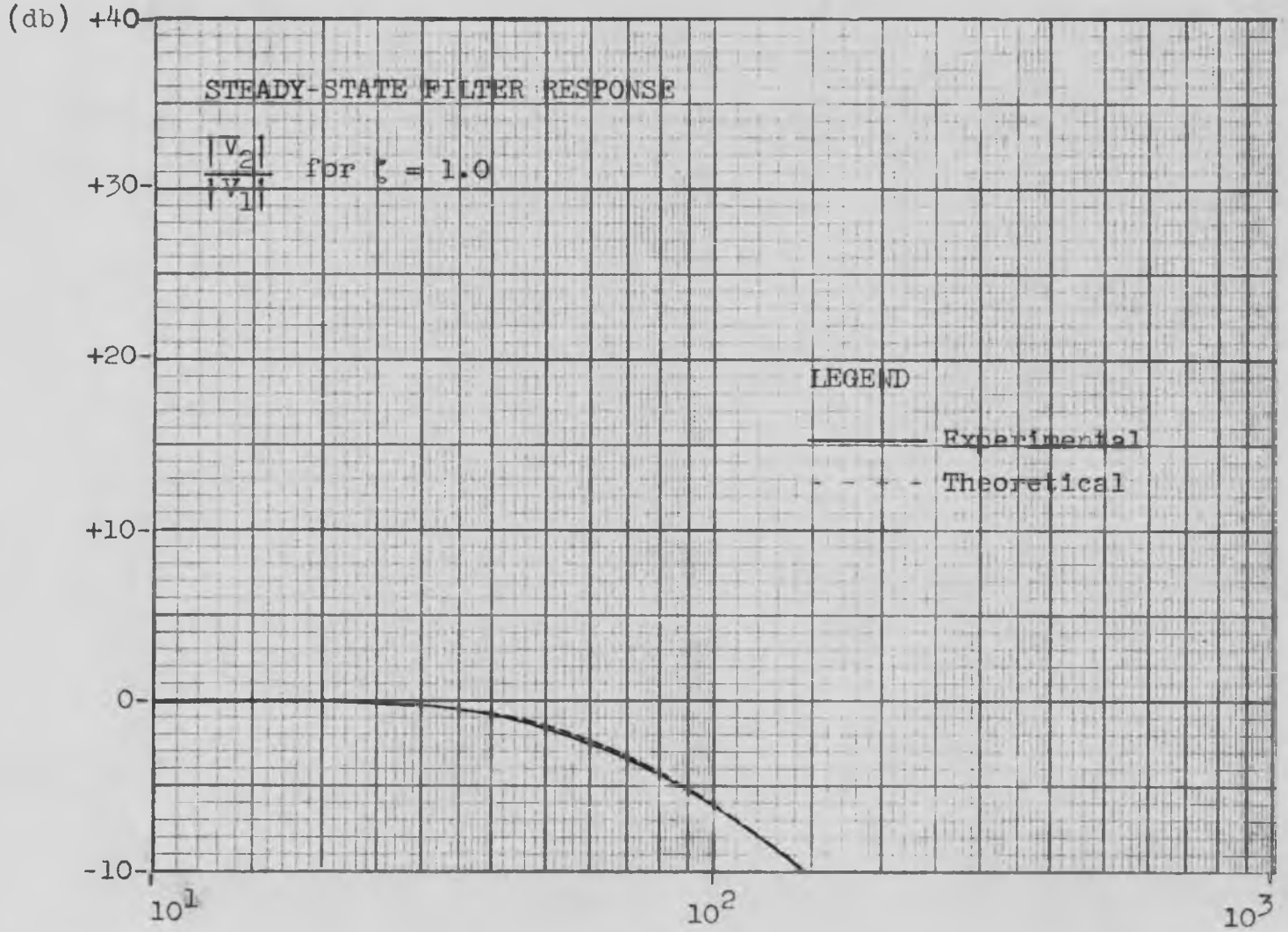
Steady-State Response: Fig. 28, page 28

Step-Function Response: Fig. 29, page 29

$\zeta = 0.01$

Steady-State Response: Fig. 31, page 30

Step-Function Response: Fig. 30, page 29



Frequency ($\frac{\omega}{2\pi}$ cps)

FIG. 24

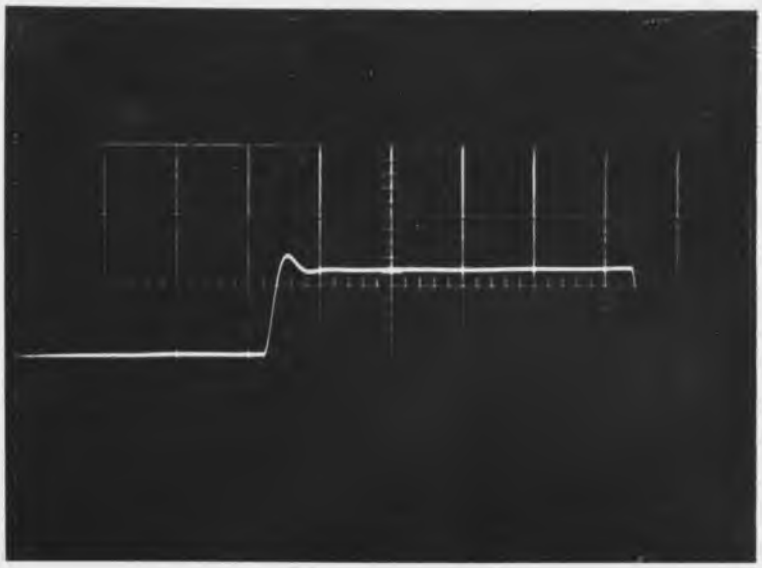


Fig. 25
Step-Function Response of Filter Circuit
with $\zeta = 1.0$
Sweep Speed: 15mSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

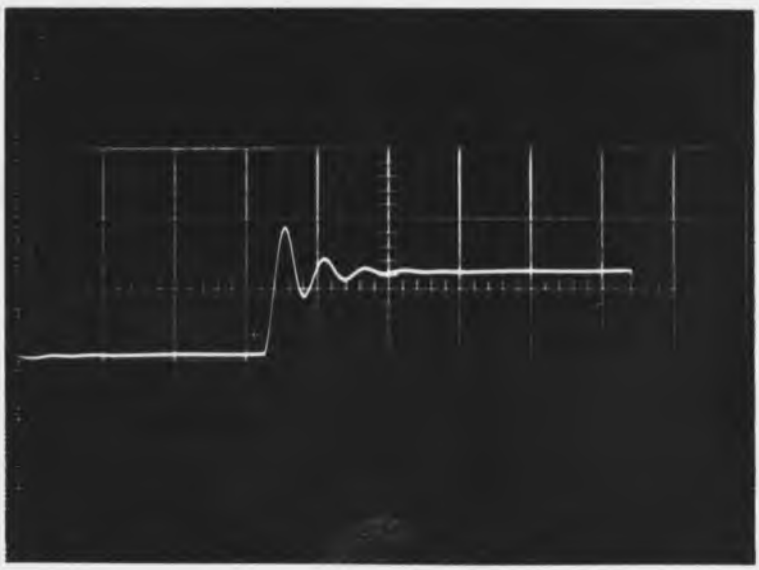


Fig. 26
Step-Function Response of Filter Circuit
with $\zeta = 0.2$
Sweep Speed: 15mSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

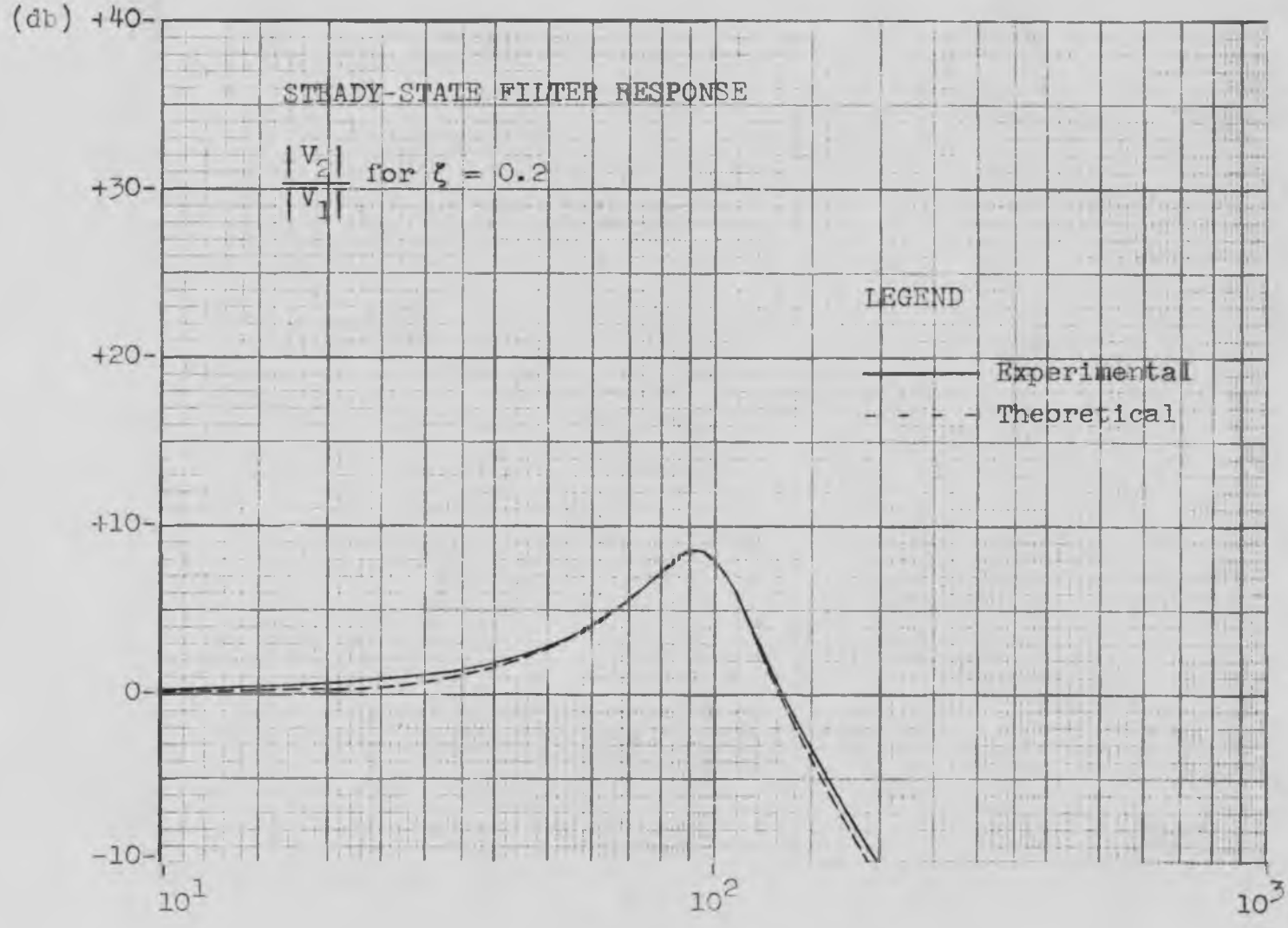

(db) +40-
+30-
+20-
+10-
0-
-10-
STEADY-STATE FILTER RESPONSE
$\frac{|V_2|}{|V_1|}$ for $\zeta = 0.2$
LEGEND
Experimental
Theoretical
10^1
10^2
10^3
Frequency ($\frac{\omega}{2\pi}$ cps)

FIG. 27

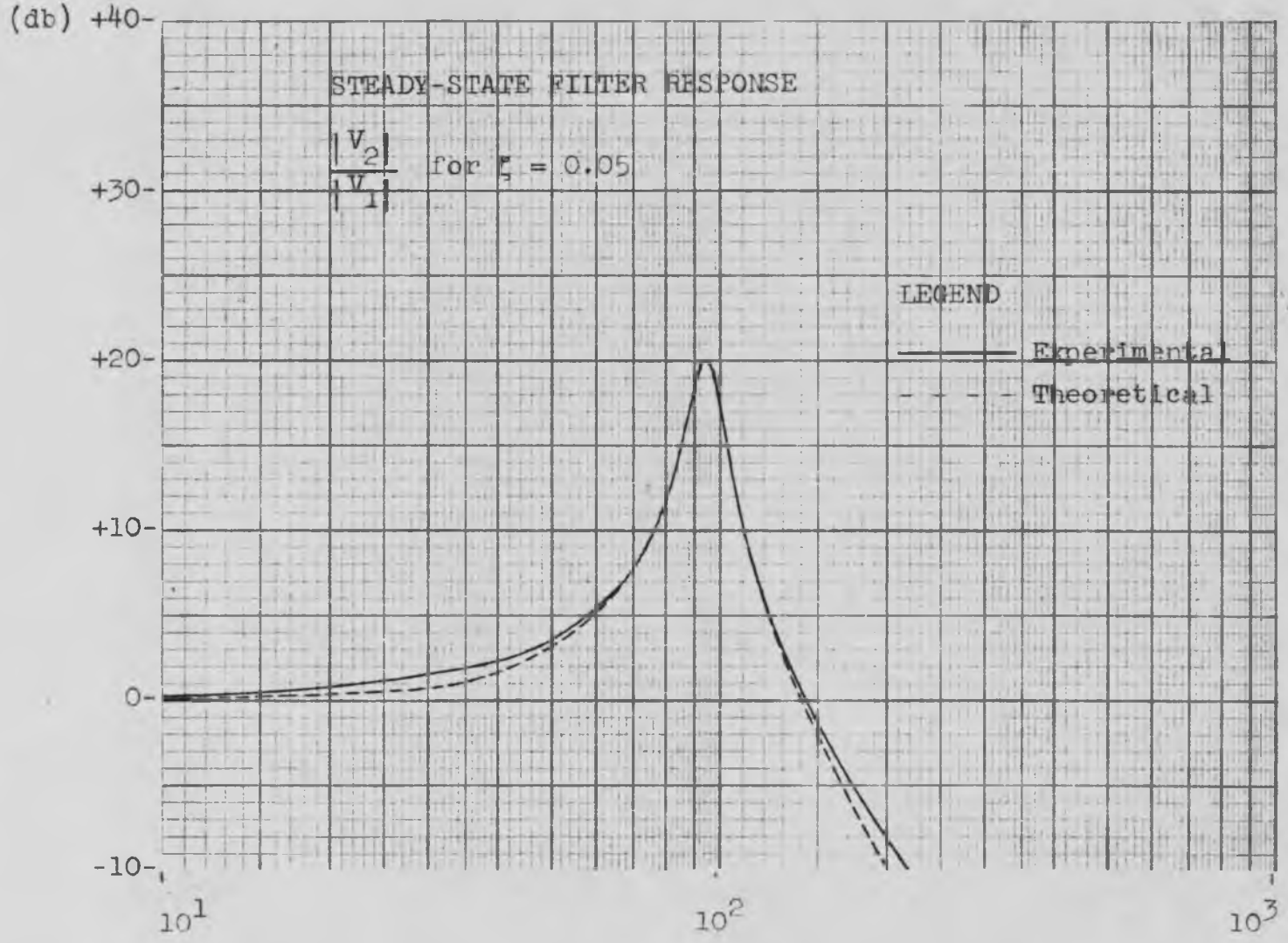

(db) +40-
+30-
+20-
+10-
0-
-10-
STEADY-STATE FILTER RESPONSE
$\left|\frac{V_2}{V_1}\right|$ for $\zeta = 0.05$
LEGEND
Experimental
Theoretical
10^1
10^2
10^3
Frequency ($\frac{\omega}{2\pi}$ cps)

FIG. 28

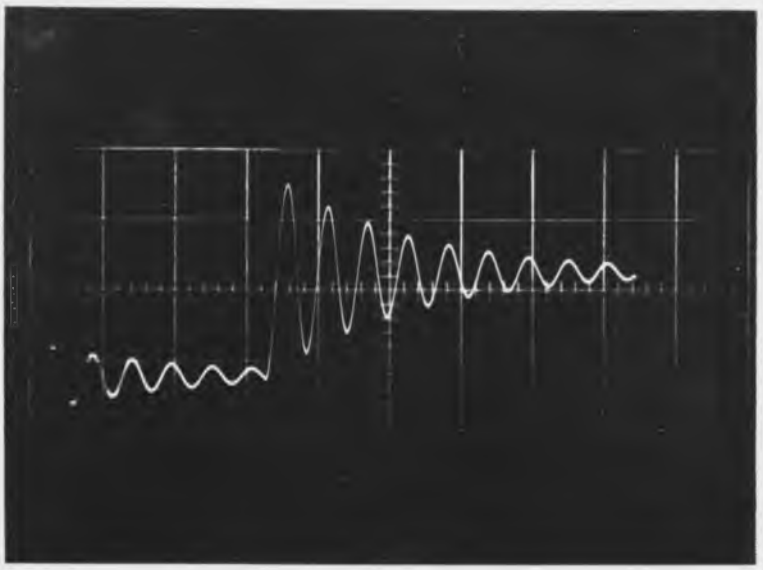


Fig. 29
Step-Function Response of Filter Circuit with $\zeta = 0.05$
Sweep Speed: 15mSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

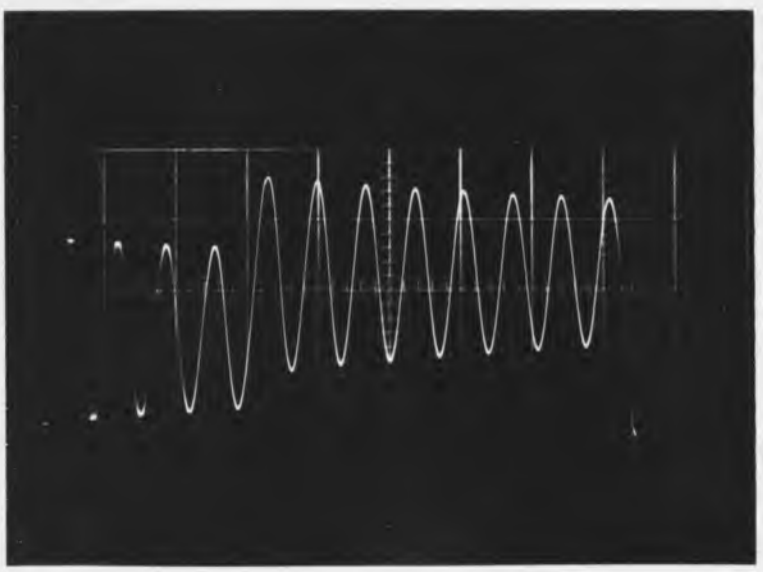


Fig. 30
Step-Function Response of Filter Circuit with $\zeta = 0.01$
Sweep Speed: 15mSEC/CM
Deflection Sensitivity: 0.25 VOLTS/CM

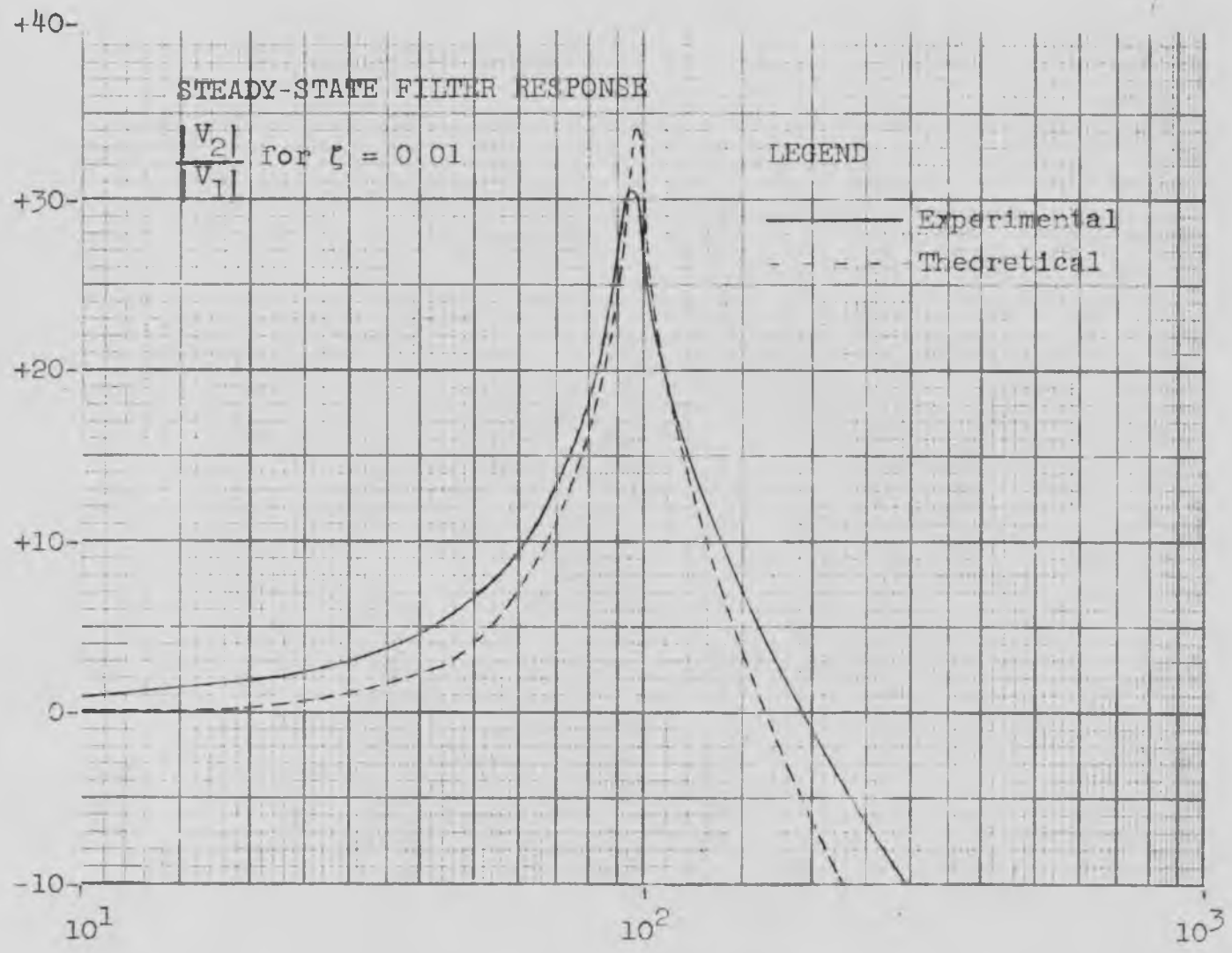

(dB) +40
+30
+20
+10
0
-10
STEADY-STATE FILTER RESPONSE
$\frac{|V_2|}{|V_1|}$ for ζ = 0.01
LEGEND
Experimental
Theoretical
10^1
10^2
10^3
Frequency ($\frac{\omega}{2\pi}$ cps)

FIG. 31

SECTION 6

CONCLUSION

The work described in this thesis proves the feasibility of NIC action at zero frequency. The circuit evolved performs satisfactorily in low-frequency, high-Q active band-pass filters.

The two principal problems associated with any NIC are stability and maintenance of a constant current transfer ratio; direct-coupled NIC(s) add to this list the classic problem of drift. The practical design of high performance NIC(s) seems to fall into the three well-established amplifier categories: direct-coupled, wide-band, and band-pass.

The theory of active synthesis has developed rapidly in recent years; hardware development has barely begun. The essential value of active synthesis is embodied in the following fact: in many areas of application, the fundamental theoretical limitations of passive synthesis are replaced by practical design problems which can be solved.

Any suggestions for further work must inevitably include refinements of the work described (chopper stabilization, etc.); a most challenging and intriguing problem would be the design of a general high performance band-pass NIC. Extricated from its telephone applications, this device has great potential in fast acting, voltage-tuned filters.

APPENDIX A

DISCUSSION OF THE PRACTICAL CIRCUIT

A-1 Problems

High-frequency gain falls off due to transistor cutoff and distributed capacity. Cumulative phase shift, introduced by the transistors and the capacity, causes phase distortion and creates instability problems.

Instability results from two distinct causes: the closed-loop current amplifier may become regenerative at critical frequencies; stray capacity present at port I is shunted by the negative conductance component of the converted impedance at port II.

The source impedance loads the base bias circuit of transistor Q_1. Quiescent bias voltage present at the open-circuited terminals of port I represents a zero-frequency error signal to the external circuit. The twin problems, stabilizing the operating point of Q_1 and eliminating the error voltage, would both be solved if the quiescent base voltage of Q_1 were zero.

The terminating impedance connected at port II appears in the emitter circuit of Q_1; the characteristic response of the amplifier depends in part upon the arbitrary terminating impedance.

A-2 Discussion

The two CE stages composed of Q_2/Q_3 and Q_4 each employ negative shunt feedback. Negative feedback

stabilizes the current gain against variations in the transistor parameters; the bandwidth is also improved by feedback. The input and output impedances are lowered by shunt feedback; the drop in output impedance is undesirable but unavoidable. The Q_2/Q_3 stage requires greater feedback than the following stage by reason of its larger gain. The phase shift introduced by the Darlington Compounded Pair becomes very pronounced at frequencies above cutoff; the feedback capacitor C_7 is added to reduce the gain at frequencies where the phase shift is intolerable.

The Q_4 stage also employs emitter degeneration to boost the high-frequency gain. Series feedback leaves the current gain practically unchanged; input impedance decreases with increasing frequency due to the bypass action of capacitor C_{10}. The change in output impedance is swamped by the very low input impedance presented by the emitter of Q_5.

The ideal interstage network would maintain a current transfer ratio independent of frequency. Assume the input impedance of the stage fed by the interstage network is negligibly small.

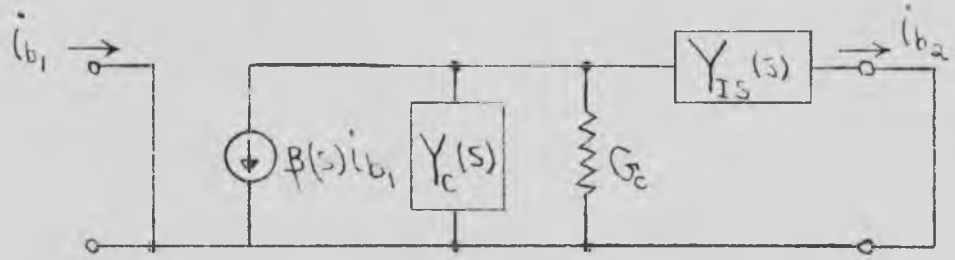


FIG. 32

$$\frac{i_{b2}}{i_{b_1}} = \frac{-\beta(s)\ Y_{Is}(s)}{Y_c(s)+G_c+Y_{Is}(s)} = -k \qquad (13)$$

where: k = a real constant

$\beta(s)$= complex transistor current gain

G_c = conductance of the collector resistor

$Y_c(s)$ = collector admittance

$Y_{Is}(s)$ = admittance of the interstage network

$$Y_{Is}(s) = \frac{k\left[G_c+Y_c(s)\right]}{\left[\beta(s) - k\ \right]} \qquad (14)$$

Assume $\beta(s) = \dfrac{\beta_0}{1+s/\omega_\beta}$ and $Y_c(s) = g_c+C_c s$.

$$Y_{Is}(s) = \frac{-k\left[C_c s^2 + (C_c\omega_\beta+G_c+g_c)\ s + \omega_\beta(G_c+g_c)\right]}{ks - \omega} \qquad (15)$$

Synthesis of a passive driving point admittance of the form given by eq. (15) is manifestly impossible; the circuit shown in Fig. 33 is a crude approximation at

frequencies well below the transistor cutoff frequency.

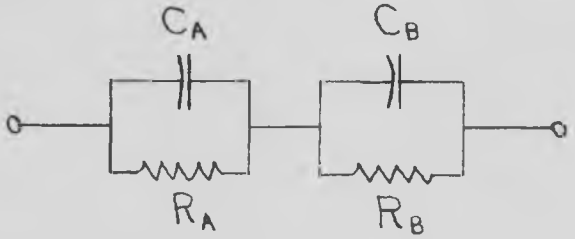


FIG. 33

The values of R_A, R_B, C_A, and C_B are adjusted experimentally to obtain optimum results.

The RC network composed of C_{12}, C_{13}, and R_{24} modify the complex input impedance of Q_5 to secure an improved phase characteristic. The effect of this network is a materially improved transient response.

Feedback capacitor C_{15} and bypass capacitor C_{14} represent an additional effort to improve the phase response and the relative stability. The primary effect of C_{14} and C_{15} is to damp out high-frequency oscillations in the transient response.

The RC feedback path from the collector of Q_4 to the base of Q_1 provides the necessary degeneration to stabilize the current amplifier. The gain and stability of the amplifier are dependent upon the arbitrary termination connected at port II. If an application requires a large unneutralized capacity connected at port II, the high-frequency gain and relative instability increase; feedback capacitor C_4 is chosen to maintain the amplifier

stable with the largest value of terminating capacitor expected to be used. The feedback loop described is essential for unconditional stability.

The RC-RL network composed of R_1, R_{29}, L_1, and C_3 serves the primary purpose of increasing the high-frequency gain; this network also affects some phase shift correction.

APPENDIX B

CONTROLS AND ADJUSTMENTS

B-1 Bias Adjustments

The transistors selected, 2N404 and 2N1566, preserve their essential characteristics over a reasonably wide range of bias voltages and currents; the heavy negative feedback employed significantly reduces the dependence of the circuit performance upon the transistor operating points. The bias adjustments are interdependent; but a very few readjustments of potentiometers R_4, R_{11}, R_{18}, and R_{26} will suffice to obtain a satisfactory setting. Bias adjustment must be made with the terminating impedance connected; the conductance component of the termination is an essential path for the bias current of transistor Q_1. A satisfactory bias setting requires the base voltage of Q_1 to be near zero (±0.25V); care should be taken that this is achieved with the Voltage Null Control at a position which permits of adjustment. Acceptable performance will be obtained with a variety of settings; the collector voltages tabulated in Table 1, measured with respect to ground, are satisfactory.

Transistor	Collector Voltage
Q_1	-10V
Q_2/Q_3	+10V
Q_4	+12V
Q_5	-5V

TABLE 1

B-2 Conversion Gain

Potentiometer R_1 is called the Conversion Gain Control; Conversion Gain adjusts the ratio $| I_1 | / | I_2 |$. This ratio is nominally unity, and the potentiometer permits readjustment when necessitated by changes in the termination or the internal characteristics of the circuit.

B-3 Voltage Null

Perturbations in the transistor operating points, changes in the resistances of the external circuit, or fluctuations in the bias supply voltages cause small variations in the open-circuit voltage at the input terminals. These variations can be of the same order of magnitude as the zero-frequency signals. Potentiometer R_2,

called the Voltage Null Control, is provided to cancel these changes, assuming they remain reasonably constant with time for a given condition. The action of R_2 can be explained most readily in terms of the analogous circuits shown below.

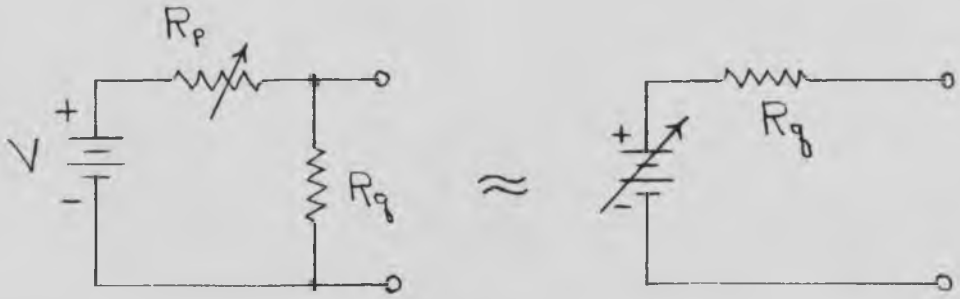


FIG. 34

where $\overline{R}_p >> R_q$

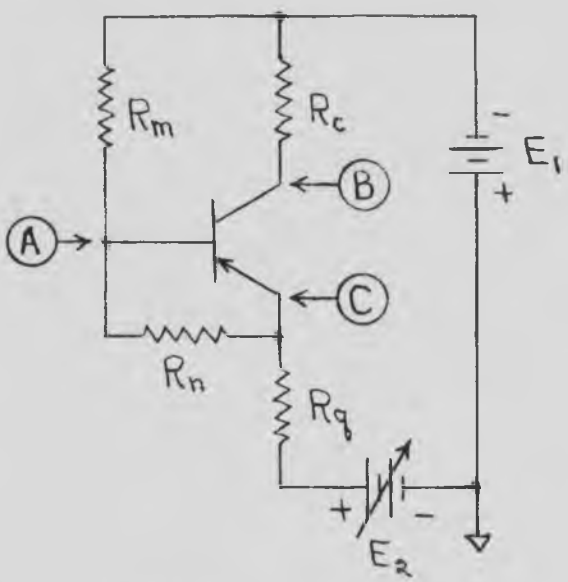


FIG. 35

Fig. 34 exhibits the basic mechanism of R_2; voltages at points A, B, and C may be changed, relative to ground, by varying E_2; the voltages, relative to one another, remain approximately undisturbed. The normal changes of E_2 are of the order of 0.1% of (E_1+E_2); such small changes have a negligible effect upon the operating point of the transistor. The actual circuit does not have the ideal isolation of ground suggested by Fig. 34; however, the approximation to Fig. 34 is quite adequate in practice. Potentiometer R_2 is shunted by a fixed resistor, R_{30}; this arrangement serves only the need for a mechanically smooth, finely-adjustable control.

B-4 Capacitors C_1 and C_2

Capacitor C_1 directly shunts the input. Capacitor C_{1A} is continuously variable from 8pf to 60pf. Switch S_1, labeled C_1 Select, enables any one of four fixed capacitors to be placed in parallel with C_{1A}; this arrangement permits continuous adjustment of C_1 from 8pf to 250pf. The capacitance increases with increasing numbers associated with the positions of switch C_1 Select. Capacitor C_2 directly shunts the output; an arrangement, identical to that of C_1, allows C_2 to vary from 15pf to 2000pf.

NIC action causes C_1 and C_2 to neutralize each other; a resultant positive or negative capacitance may be obtained

at either port. Bias considerations require the termination to have a conductance component; this component appears as a negative conductance at the input terminals. If a resultant positive capacitance appears across the input, relaxation oscillations will be initiated. Unwanted capacity shunting the termination results in appreciable distortion. Changes in the termination cause significant variations in the characteristic response of the amplifier. C_1 and C_2 provide two independent means of control over these three effects. Even qualitative evaluation of the distortion in the transient response of a complex impedance is extremely difficult. Experiment has proven the following procedure to be feasible: remove all elements of the termination except the shunt conductance; drive the input with a high-impedance square wave generator of frequency 10KC or less; C_1 and C_2 are then adjusted for the best possible response. Increases in C_1 tend to improve the rise time and decrease the relative stability; an increase in C_2 tends to damp out the oscillatory nature of the response. A general rule suggests the following: the smaller the terminating conductance, the larger C_2 should be made. If a complex termination is to be employed, the remaining elements of the termination should be restored after the adjustment, as described, has been made.

The small input capacity of high impedance measuring instruments connected at the ports may cause severe changes in the transient response.

APPENDIX C

DERIVATION OF Q

$$\frac{V_2}{V_1} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{16}$$

Let $s = \omega_n p$, $\omega' = \frac{\omega}{\omega n}$

$$\frac{|V_2(j\omega')|}{|V_1(j\omega')|} \qquad \frac{1}{\left[\omega'^4 - 2(1-2\zeta^2)\omega'^2 + 1\right]^{1/2}} \tag{17}$$

The maximum modulus will occur when $\omega' = \omega_0$.

$$\omega_0 = \sqrt{1-2\zeta^2} \tag{18}$$

The 3db cutoff frequencies, whenever they exist, are given by equations (19) and (20).

$$\omega_1 = \omega_0 \left[1 + \frac{2\zeta\sqrt{1-\zeta^2}}{(1-2\zeta^2)}\right]^{1/2} \tag{19}$$

$$\omega_2 = \omega_0 \left[1 - \frac{2\zeta\sqrt{1-\zeta^2}}{(1-2\zeta^2)}\right]^{1/2} \tag{20}$$

When $x \ll 1$, $(1\pm x)^{1/2} \approx 1 \pm x/2$

Assume $\zeta \ll 1$, then $\sqrt{1-2\zeta^2} \approx \sqrt{1-\zeta^2} \approx 1$

$$Q \triangleq \frac{\omega_0}{BW} = \frac{\omega_0}{\omega_1 - \omega_2} \approx \frac{1}{2\zeta} \tag{21}$$

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