AN ANALOG-DIGITAL CONVERSION SYSTEM FOR AN ASYNCHRONOUS DIGITAL COMPUTER

by

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A Thesis Submitted to the Faculty of the

DEPARTMENT OF ELECTRICAL ENGINEERING

In Partial Fulfillment of the Requirements
For the Degree of

MASTER OF SCIENCE

In the Graduate College

THE UNIVERSITY OF ARIZONA

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ACKNOWLEDGMENT

The author would like to thank Dr. G. R. Peterson for his guidance and assistance in preparing this thesis.

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ABSTRACT

The design of a system to link together an iterative differential analyzer and a general purpose asynchronous digital computer is described. The design takes into account the type of problems to be simulated and the operational characteristics of the two computers linked.

Three different methods of analog-to-digital conversion are examined: intermediate conversion to a time interval, cascaded stages, and the closed loop method. The closed loop method is the best for this conversion system.

Two different methods of digital-to-analog conversion are considered, the ladder network and the weighted resistor method. Both methods are found adequate for this conversion system.

The control logic for the conversion system is designed to allow one to four analog voltages to be sampled at different times and then coded for use by the computer. One digital output is decoded. Special circuits for logical level change and gating are designed.

The conversion processes proceed at the fastest rate allowed by the conversion and digital computer input-output times.

CHAPTER 1

INTRODUCTION

The use of digital or analog computers to aid in the solution of technical problems has been highly developed in the past two decades. In the course of this development, problems have been encountered that can be solved more readily by a computing system that has some of the characteristics of both analog and digital computers. A hybrid computing system should have the desirable analog computer characteristics of parallel operation for high speed and the ability to perform efficiently integration, multiplication, addition, and function generation. A hybrid system should also have the digital computer capabilities of logical decision, numerical storage, long time delay, and extremely high accuracy.

There are numerous approaches to combining analog and digital operation. The most common approach to obtaining these desired characteristics is the interconnection of complete analog and digital computers to form a hybrid system.

The first large scale hybrid computing system using this technique was constructed in 1956.[1] The number and range of application of hybrid computing systems has been increasing ever since.

The many ways that the analog and digital computers can be interconnected gives rise to many possible hybrid systems. The two general categories of hybrid linkage are unilateral and bilateral.[2] In unilateral linkage, information flows in only one direction across the analog-digital interface. In the bilateral linkage, information flows in both directions across the interface (figure 1).

At the interface an analog-to-digital converter changes analog voltage to the appropriate digital code. A digital-to-analog converter changes a digital word to an analog voltage. Other important parts of a hybrid system are track-holds or sample-holds to store analog signals, analog multiplexers for time sharing, buffer registers for temporary storage of digital numbers, and logic circuits to control the various units involved.

In this thesis a system for linking an iterative differential analyzer to a general purpose asynchronous digital computer is designed. The system is bilateral with the digital computer used to perform specialized tasks that the iterative differential analyzer cannot accomplish efficiently. The hybrid system will not be a "balanced" linkage system because the digital computer shall be subordinate to the iterative differential analyzer.

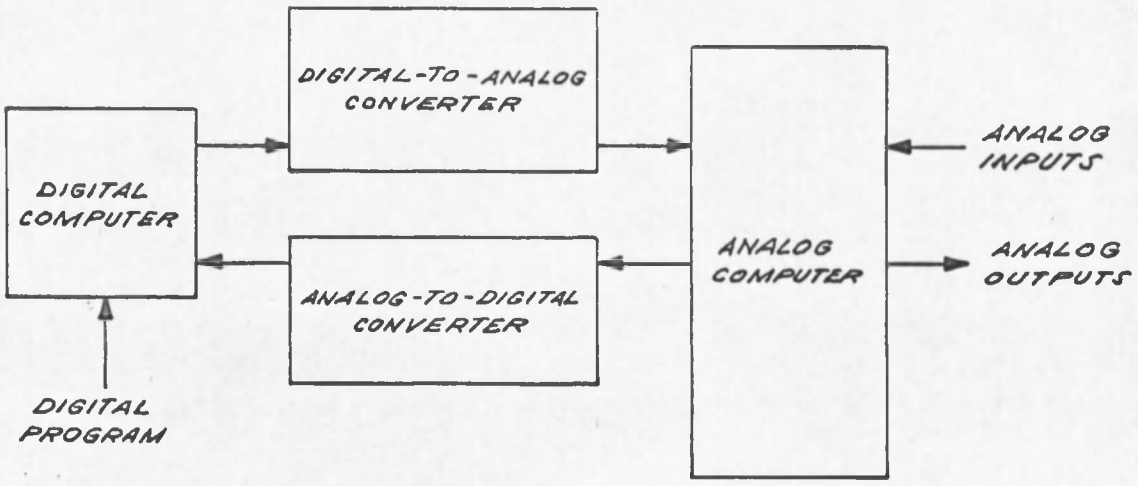


Figure 1. A Bilateral System

CHAPTER 2

COMPUTERS CONNECTED BY THE CONVERSION SYSTEM

2.1 Astrac II

Astrac II is an iterative differential analyzer. It consists of a digital control unit, 10 to 20 operational amplifiers which may be used as track-hold units or as integrators, analog comparators, multipliers, and a statistics computer. The statistics computer contains a noise generator, an amplitude distribution analyzer, and a statistical averaging unit. Astrac II also has coefficient-setting potentiometers, and various noncommitted analog switches, flip-flops, AND gates, OR gates, and NAND gates. The connection between components is made on a removable patchboard. The analog voltage range is ±10 volts with ±0.5 percent of full scale static accuracy.[3]

The digital control unit utilizes Computer Control Company S-Pac digital modules. The logical levels are logical zero ≡ 0 volt and logical one ≡ -6 volts. The clock in the control unit is a 4 Mc crystal oscillator with a counter chain providing pulses at 1 Mc, 100 kc, 25 kc, and 10 kc rates. One of these pulse rates is selected and divided by 1,000 in the master timing counter to provide the basic computer rate. The selected pulse rates are also divided by 10 and 100 to provide timing mark pulses. This

same selected pulse rate is divided by 1,000 in another counter to obtain a pulse that can be set to occur at any one of 1,000 equally spaced increments of the basic compute period as set by a thumbwheel decade switch. The occurrence during the basic computer period of a pulse from the master timing counter is set by another thumbwheel three-decade switch. The timing diagram of the control unit pulses is shown in figure 2. Both the basic computer control pulse and the two delayed pulses have a duration of 1/10 of the basic compute period. The control unit also has a subroutine counter that counts to any preset number of pulses less than 20,000.[4] The computer can also use a single run mode to operate as a conventional analog computer.

The track-hold or integrator circuit uses Burr-Brown Model 1607A operational amplifiers. The drift of these amplifiers is ±25 microvolts/°C and the voltage range is ±10 volts. The dc gain is 90 db and the cutoff frequency is 10 Mc in the unity gain inverting form. The maximum output current is 30 milliamperes. The amplifier is used in the circuit of figure 3.

The circuit is in the track-hold mode when the U_1 and R_1 analog switches are used. The initial condition, $-X_o$, is placed on the output during the reset pulse R_1, while U_1 equals zero. When R_1 changes to zero, $-X_o$ is the output until U_1 occurs. When U_1 occurs, the output follows $-X_1$ until U_1 goes back to zero. Now the value of $-X_1$ at the

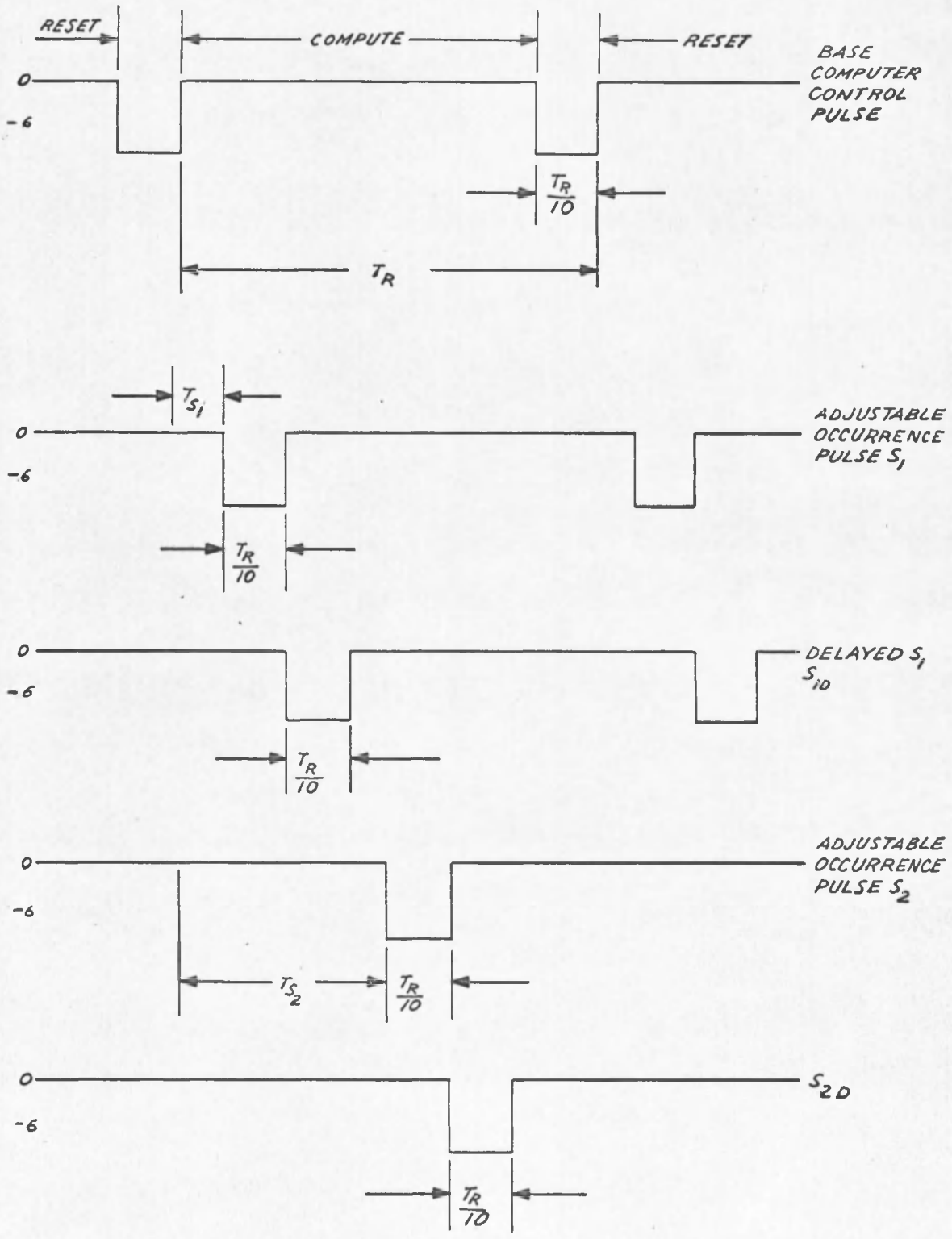
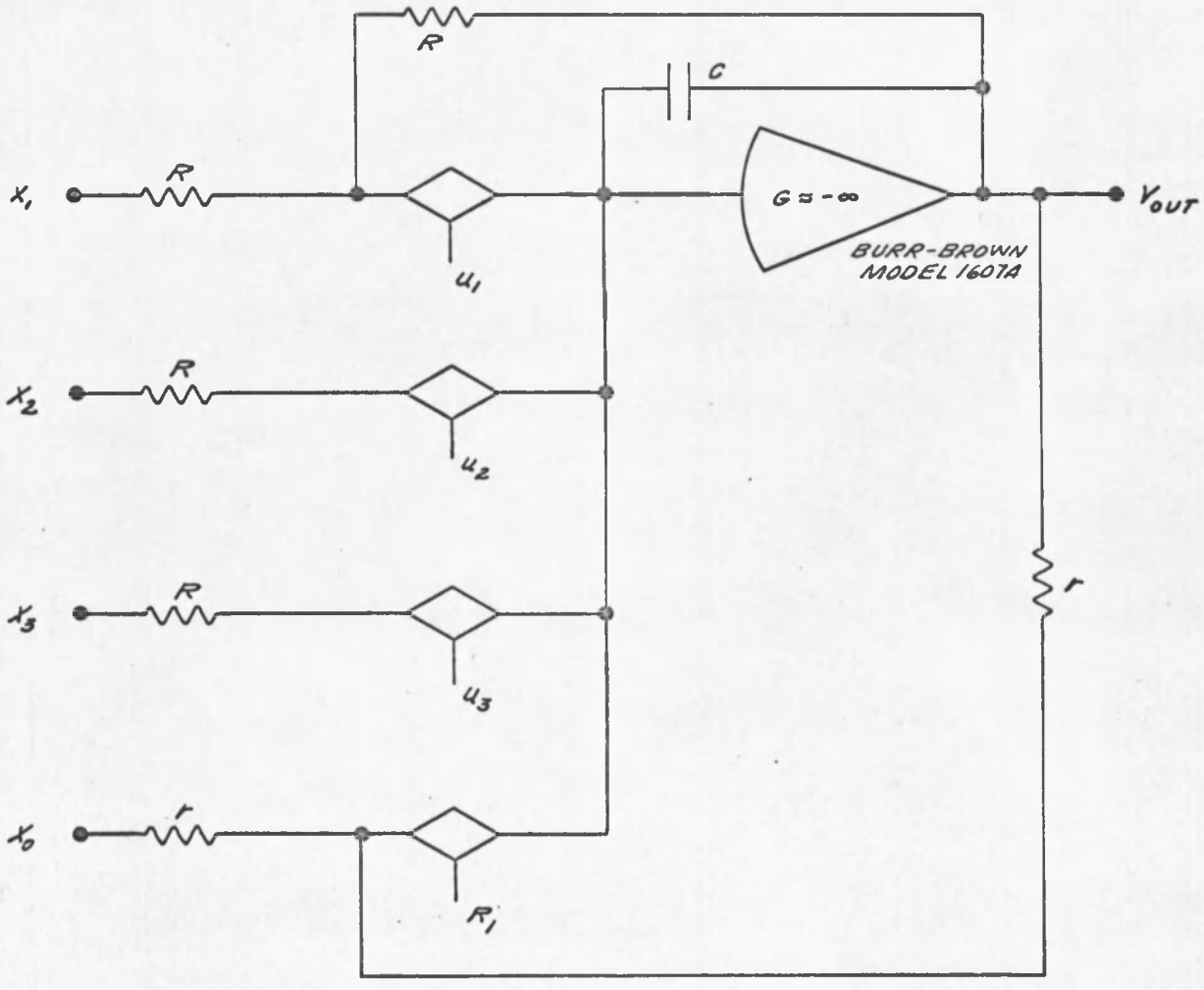


Figure 2. Astrac II Control Unit Pulses



Note: The electronic switch is on when U = -6 volts and off when U = 0 volts.

Figure 3. Track-Hold or Integrator Circuit

end of the track pulse U_1 is held until the next reset pulse. The circuit is in the switched integrator mode when the U_2 and U_3 switches are used. The output is the integral of $-(X_2 + X_3)$ when the pulses U_2 and U_3 are present. An initial condition is placed on the output in the same manner as before. The circuit becomes a switched summing amplifier when the capacitor, C, is replaced by a resistor and the U_2 and U_3 switches are used.

The design of the analog switch for Astrac II is not complete. The most likely form is a nonsaturating four-transistor bridge using two PNP and two NPN transistors. The forward resistance of the electronic switch should be 10 ohms or less. The settling time is about 0.2 microsecond.

Astrac II has a +10 and a -10 volt reference source that is accurate within ±0.01 percent.

The other units of Astrac II are not of interest in designing the conversion system.

2.2 General Electric Asynchronous Computer

The General Electric asynchronous computer is a high speed, general purpose machine suitable for use in the proposed hybrid system.

The GE computer is a completely asynchronous machine, depending on the generation of completion signals to control the timing of the computational sequences. The normal computation sequence is broken down into 11 "control blocks." When the sequence enters a given control block, a number of

parallel operations, appropriate to the particular command, start simultaneously. Each operation then proceeds at its own inherent speed, but the computer does not move on to the next control block until all operations in the current control block have generated completion signals.

The speed of the GE computer is approximately equivalent to a synchronous computer with a 10 Mc clock. The word length is 24 bits plus a sign bit. Negative numbers are represented in 2's complement form. The logic is negative with 0 ≡ 0 volt and 1 ≡ -2.33 volts. The high speed core memory can store 504 words. A magnetic tape unit is also available as a slow access time memory of large capacity.

The GE computer peripheral interface adapter contains three buffer units. Each buffer has its own asynchronous control block to direct the buffer operation. One 6-bit input-output buffer connects the digital computer to a typewriter or Flexowriter.

A 7-bit input buffer, called the peripheral interface adapter receive buffer, is available for use as the input buffer for the conversion system. Information can be placed in the receive buffer by placing a negative signal on the Receive Buffer Clock Input (line IRCLIR). This input signals the Receive Buffer Control Block to start the input process. The Receive Buffer Control Block then interrupts the regular program at a step in the computations allowed by

the program and transmits the contents of the receive buffer to the "S" register (figure 4). The Receive Buffer Control Block then returns to a state of readiness to receive more information. Outputs are available from the Receive Buffer Control Block to signal that the buffer contents have been transferred (line CCRB) and that more information can be received (line CCRBIP).

Four successive groups of bits from the receive buffer may be sent through the adder to the accumulator to be assembled into a full word. From the accumulator the word may then be sent back through the "S" register to the memory. A 7-bit output buffer, called the peripheral interface adapter transmit buffer, is available for use as the digital computer output buffer for the conversion system. The placing of information in the transmit buffer is indicated to the conversion unit by a negative signal on line DTWMIP. After a word has been received, the Transmit Buffer Control Block does not allow the transmit buffer to receive more information from the computer until an external completion signal is received (on line JTCRIT) indicating that the transmit buffer contents have been read out. The pulse shapes of the buffer outputs are shown in figure 5.

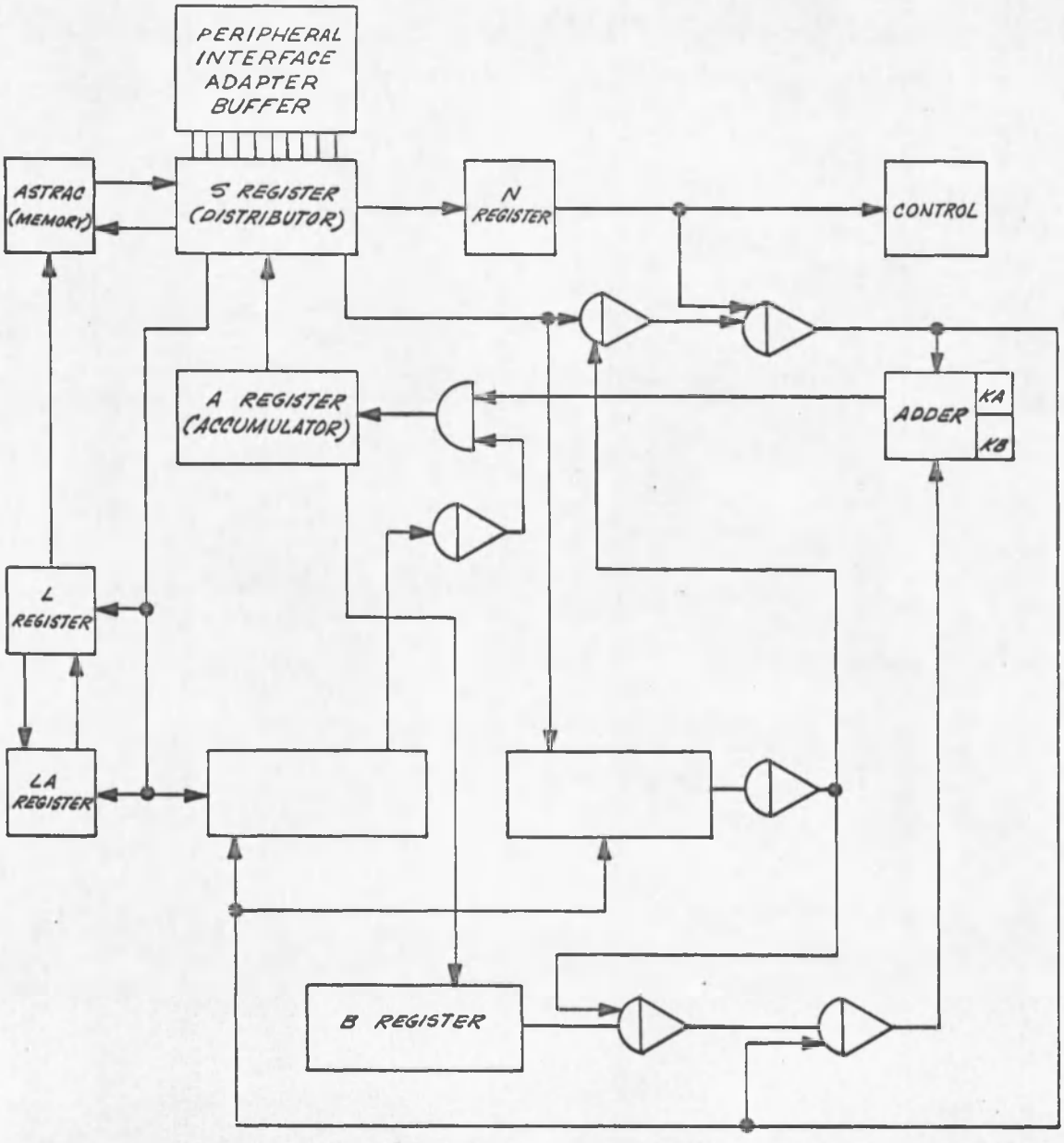
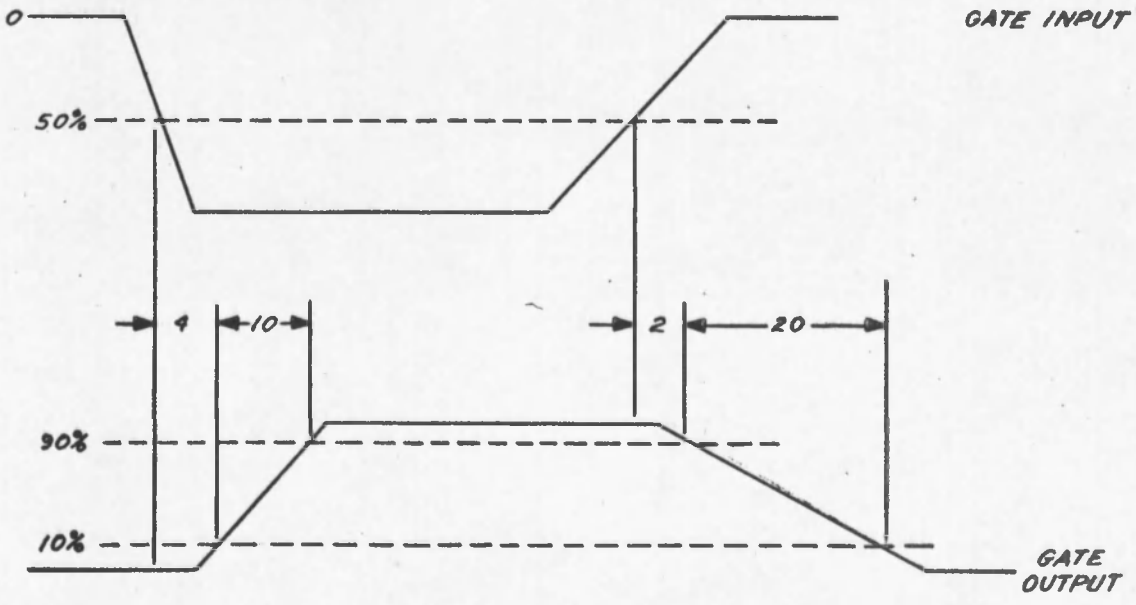


Figure 4. GE Asynchronous Computer Block Diagram



Time in Nanoseconds

Figure 5. GE Computer Pulse Shape

CHAPTER 3

SYSTEM DESIGN CRITERION

3.1 Computation to be Performed

A hybrid computing system can be used to advantage in many situations.

The problem may be one of optimization where up to four different analog voltages are sampled once during a computing run of Astrac II (Astrac II being run in an iterative mode). Each voltage can be sampled at a different time during the compute period. Each voltage must be coded in a form usable by the digital computer. The digital computer then uses these samples, and past samples, to perform the logical decisions for the optimum strategy of parametric adjustment so the analog system can be modified automatically in an optimum manner for the next Astrac II computing run.[5]

Another type of problem may have Astrac II run as a noniterative analog computer and the GE asynchronous digital computer simulating a digital computer used in a sampled data control system. Up to four different voltages may be sampled at the same rate for use by the digital computer. The digital computer can use these samples to implement a digital controller derived from sampled data control system theory. To simulate a digital controller the value of previously sampled voltages would be stored in the digital

computer memory for use in solving the controller equations.

The sampled analog voltages also could be state variables that would then be used in equations solved by the digital computer to obtain an optimum control signal or another state variable. In either case it is desirable that the digital computer solution be available at the start of the next sample period to minimize the time delay in a closed loop control system.

In this type of simulation it should be possible to vary the sampling rate and the analog quantization value to find the effects on system performance.

The digital computer should also have the capability within a hybrid system to simulate a pure time delay, to perform nonlinear function generation, or to perform computations where accuracy beyond that of an analog computer is required.

3.2 Desired System Performance

The analog-digital conversion system specifications are determined mainly by the analog and digital computers already described and the various problems to be studied.

The analog-to-digital converter should be able to change to binary form four voltages, or less, and sample the four voltages at the same time or at four different times. All four voltages are sampled at the same rate. Astrac II

has a ±10 volt range and a static accuracy of ±0.50 percent of full scale which of course requires that both converters have a ±10 volt range. The overall conversion system accuracy must be at least ±0.1 percent to preserve the ±0.50 percent of full-scale Astrac II accuracy. The analog-to-digital converter, therefore, must have at least 10 bits plus a sign bit, since with 10 volts coded into binary with 10 bits used, the quantization step is 10 millivolts or ±0.05 percent of full scale.

Clock pulses must be available to control the sampling and the conversion rate. The clock rate should be variable from 10 cps to 1000 cps. The least time available to convert and perform the digital computations is the length of the shortest Astrac II reset pulse, 100 microseconds. This worst case time interval may be too short a time to perform the analog-to-digital conversion of four analog voltages and still have time remaining for useful digital computation. If this happens, the Astrac II clock rate can be slowed down to gain more computing time.

The solution of the digital computation has to be available in analog form at any desired time after the digital computations are complete.

3.3 Specially Designed Circuits

In the analog-digital conversion system certain types of Computer Control Corporation S-Pac digital modules will be used. The S-Pacs have been selected for use in

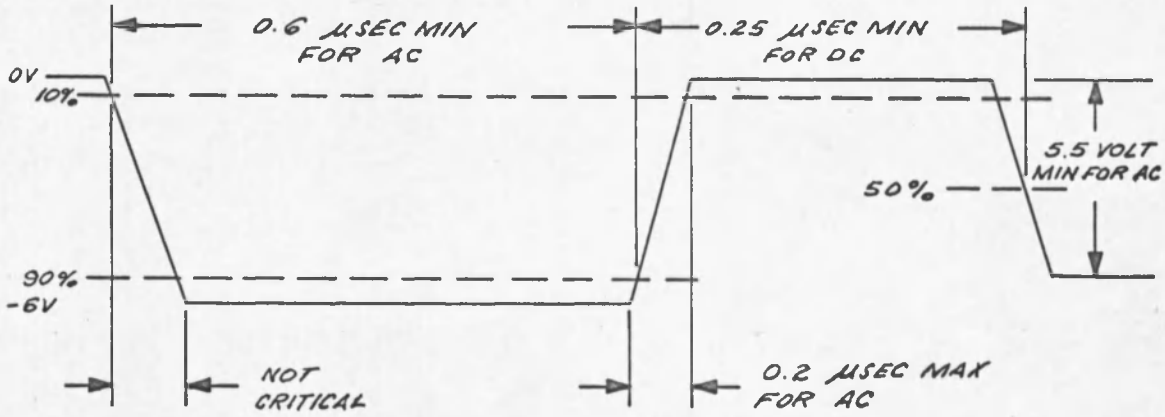
computer systems at the University of Arizona because of their reliability and versatility.

The Nand gate, Model DI-30, and the Universal flip-flop, Model UF-30, have been selected as standard. The speed requirements of the conversion system are such that 1 Mc logic has adequate speed.

The S-Pacs have negative logic with logical $1 \equiv -6$ volts and logical $0 \equiv 0$ volts. The pulse requirements for the S-Pacs are shown in figure 6.

The Nand gate card, Model DI-30, consists of eight diode-transistor Nand gates (figure 7) with two inputs each. Each gate has a fan-in of 10 and can drive seven other S-Pac inputs.

The Universal flip-flop card, Model UF-30, contains two identical flip-flops (figure 8). The main difference is that the Universal flip-flop has single pedestal and double pedestal gates on the inputs plus the dc inputs. The flip-flop changes state on a positive going transition of the ac input. The ac inputs require twice the input current of the other logic circuits.[6]



Trailing edge trigger mode used

Figure 6. Signal Requirements for S-Pacs

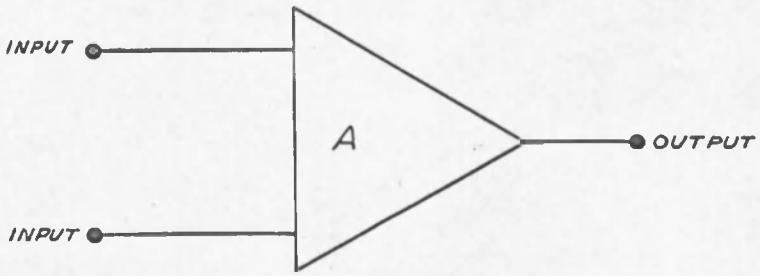
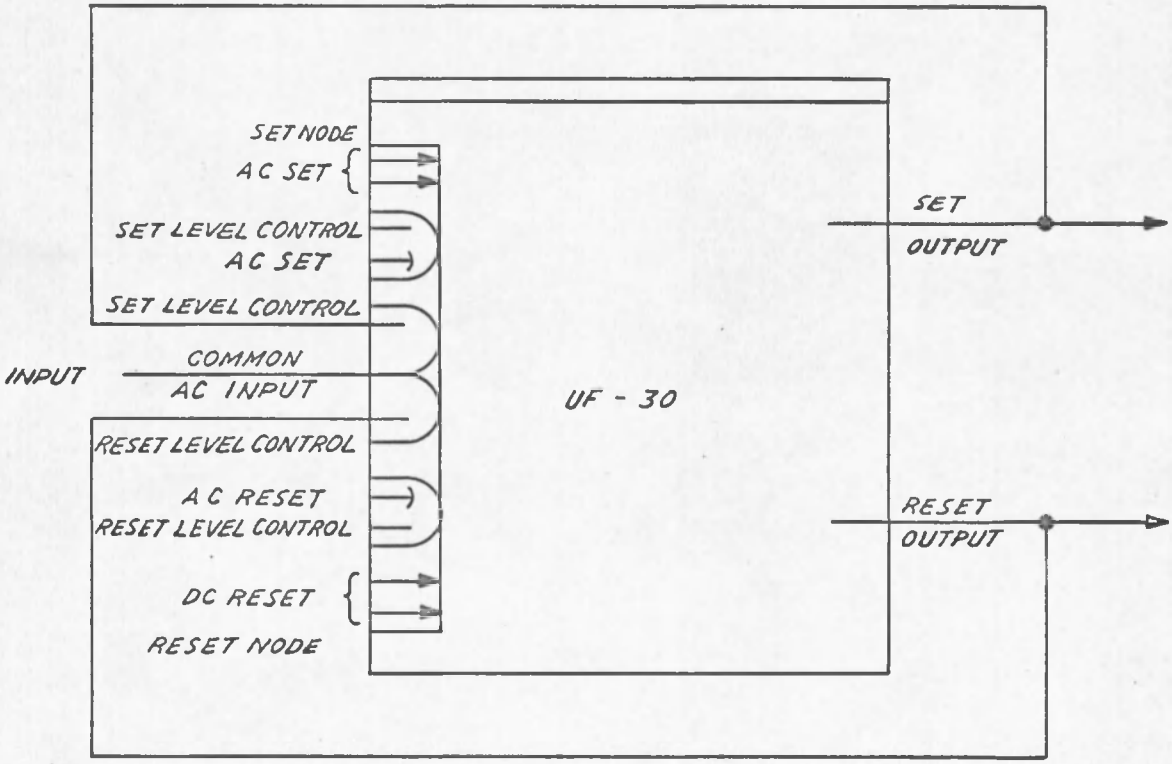


Figure 7. The Nand Gate Symbol



Common ac input is usually called the trigger input.

Figure 8. Universal Flip-Flop Block Diagram, Connected as a Binary Counter

CHAPTER 4

SYSTEM DESIGN

4.1 Basic Elements

The analog-digital conversion system consists of an analog-to-digital converter and a digital-to-analog converter controlled by a logic network. To simplify the design procedure each unit will be considered separately and then the overall system developed.

4.2 Analog-to-Digital Conversion

There are three basic methods used to convert an analog voltage to a digital word.

The first coding method considered is intermediate conversion to a time-interval. A block diagram of the basic time-interval conversion circuit is shown in figure 9. The coding process begins when a start pulse changes the state of the start-stop circuit. The change of state opens a gate that then passes oscillator pulses through to the counter and to the sawtooth generator. The first oscillator pulse starts the sawtooth generator. The output of the sawtooth generator increases linearly with time until it equals the input voltage. At the instant the sawtooth voltage equals the input voltage, the comparison circuit emits a stop pulse that closes the gate and resets the sawtooth generator to its initial state. The length of time that oscillator

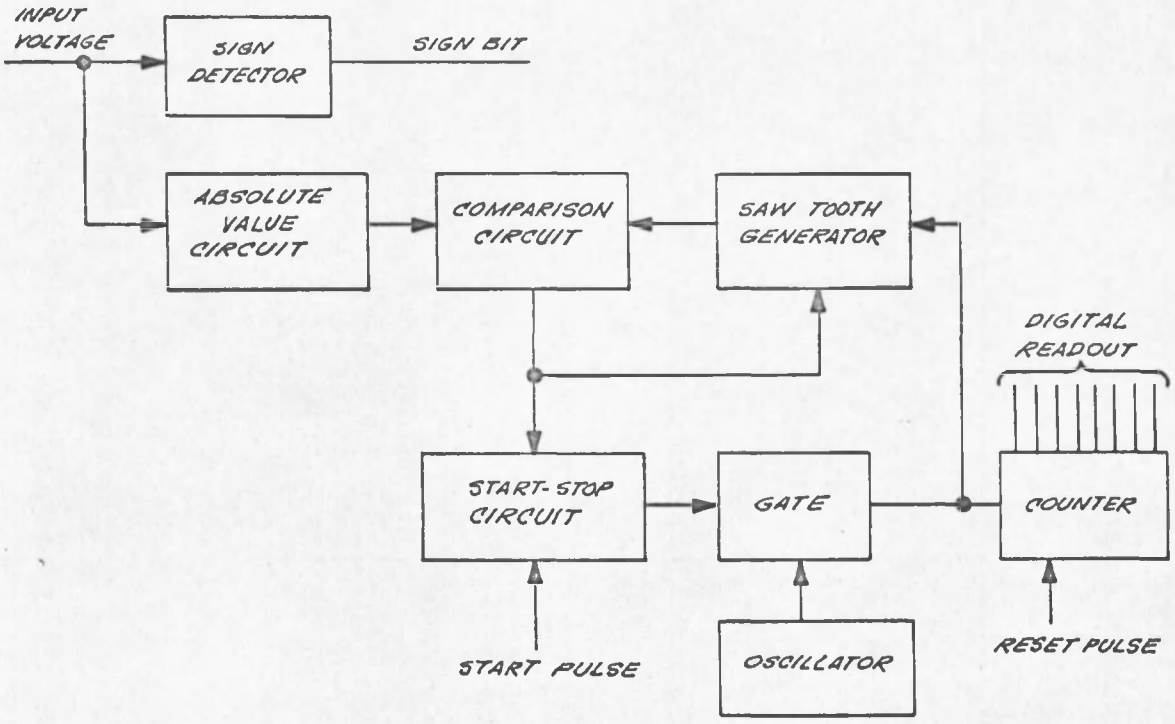


Figure 9. Time Interval Coder

pulses have passed through the opened gate is directly proportional to the input voltage. Thus the number of pulses counted by the counter is proportional to the input voltage. If the pulse rate and sawtooth slope are selected correctly, the counter output is the binary representation of the input voltage. To convert more than one voltage at the same time only one oscillator and one sawtooth generator still are used. A comparison circuit and counter are used for each input. The conversion time for more than one input need be no longer than for one input.[7]

At least a 10-bit counter is necessary so the counter must count up to 1023 pulses. The fastest practical counter can use 5 Mc pulses. The counter reset and reaction time can be about 1 microsecond. The maximum conversion time t_{max} is:

$$t_{max} = \frac{1023}{5 \times 10^6} + 1 \times 10^{-6} \approx 206 \text{ microseconds}$$

A conversion time of 206 microseconds is too slow for use in this analog-digital conversion system. The accuracy of about 0.1 percent is acceptable.

Coding by cascaded stages is the next method to be considered.[8] A block diagram of a cascaded stages coder is shown in figure 10. The input voltage is compared to a reference voltage, and if the input is greater than or equal to the reference voltage, the Schmitt circuit connects the negative reference to the next stage. V_{n-2} then equals

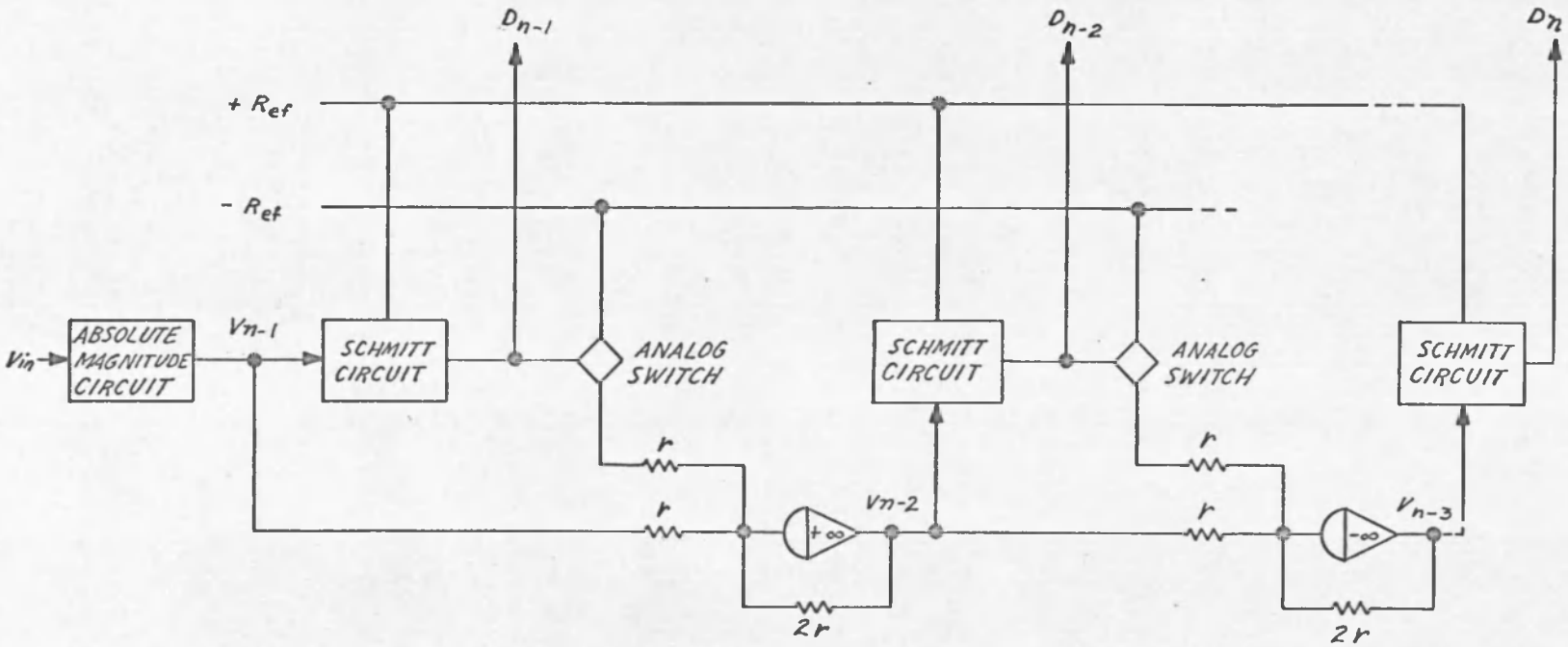


Figure 10. Coding with Cascaded Stages

$2(V_{in} - R_{ef})$ or $2(V_{in})$ depending on the value of V_{in}. V_{n-2} is compared to the positive reference and the process continues. The positive and negative reference voltages have equal magnitudes.

As an example of this method let the number of stages equal three, R_{ef} = 4 volts, and V_{in} = +5 volts.

For the first stage: $V_2 = 5$ volts $> R_{ef}$

$\therefore D_2 = 1$ and $V_1 = 2(5-4) = 2$ volts

For the second stage: $V_1 = 2$ volts $< R_{ef}$

$\therefore D_1 = 0$ and $V_0 = 2(2-0) = 4$ volts

For the last stage: $V_0 = 4$ volts $= R_{ef}$

$\therefore D_0 = 1$

For the binary representation of 5 volts, 101 is obtained.

The speed of this method is limited by the delay times of the components. The delay time per stage can be about 2 microseconds. The conversion time for a 10-bit word is about 20 microseconds. The accuracy is limited to about 0.25 percent because of the subtracter circuits in series. The method of cascaded stages is too inaccurate to be used in this analog-digital conversion system.

The last analog-to-digital conversion method to be considered is the closed-loop method (figure 11).[9]

In this method the start pulse begins a process that changes the contents of the digital register until the digital representation on the output is the coded form of the input voltage. The digital output is converted to an

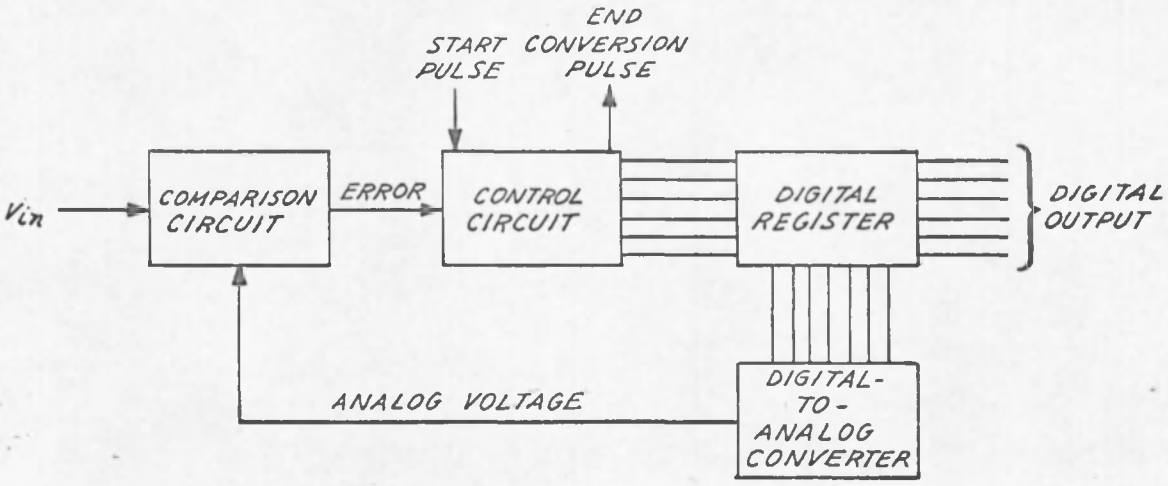


Figure 11. Closed Loop Analog-to-Digital Conversion System

analog voltage and the comparison circuit produces an error signal until this analog voltage equals the input voltage. The control circuit uses this error signal to modify the number in the digital register.

There are three different modes a control circuit can use to change the number in the digital register. In one mode the control circuit has the digital register count up in binary from zero until there is no error signal. This mode has about the same speed as the time interval converter and therefore is too slow.

Another control circuit mode is the successive approximation method. With this method the digital register is reset to zero and then the most significant bit is changed to one. If the input voltage is still greater than the decoder output, the bit is left one; if not, it is set back to zero. The control circuit continues the process with each bit in the register. The time required is about the number of bits times the time for one approximation. For an 11-bit word the conversion time is typically around 50 microseconds. The accuracy is limited by the digital-to-analog converter and the comparison circuit. A typical value is ±0.05 percent of full scale. The speed and accuracy of this mode is acceptable for use in the conversion system.

The last control circuit mode considered is the incremental converter. In this mode the digital register

is not reset to zero. The comparison circuit indicates if there is any difference between the input voltage and the digital-to-analog converter output. If the difference is positive, the number in the register is increased one least significant bit at a time until the error is zero. This mode is faster than the successive approximation mode if the voltage change between conversions is small. If the input is multiplexed, the voltage change is apt to be large and the conversion time is not much less than for the first mode considered. This mode is not suitable because it is too slow for multiplexed inputs.

As seen from the comparison of the various conversion methods the closed-loop type converter using the successive approximation mode is the best method for this particular system.

An analog-to-digital converter of this type can be obtained in three ways. One way is by designing and building the converter from the start. Another way to obtain a converter is to design and build the converter using commercially available digital modules. A third way would be to purchase a converter to perform the analog-to-digital conversion. It would be difficult to obtain the desired performance and reliability from an analog-to-digital converter designed and built from the start. The savings obtained by building the whole converter would not be worth the labor involved. If digital modules are bought and

assembled, there is only a small saving over buying a complete converter composed of these modules. The best way, therefore, to perform the analog-to-digital conversion is to use a commercial converter of the closed loop method in the successive approximation mode.

Table 1 lists a representative sample of presently available analog-to-digital converters. The best model considering the cost-performance tradeoff is the Packard-Bell model ADC23-12B. This model is only a few hundred dollars more than the cheapest model with acceptable performance and has the second fastest conversion time and second accuracy rank.

4.3 Digital-to-Analog Conversion

A digital number is changed to a proportional analog voltage by using the coded number to switch sources into a resistor network. Two types of resistor networks are most commonly used to decode a digital number, the weighted-resistor decoder and the ladder-network decoder.[10]

The basic form of the decoding ladder is shown in figure 12. The single-pole double-throw switch is used to connect the end of the resistor to ground or to E_R depending on the value of B_k, the controlling bit. The equation for the output voltage is:

$$e_{out} = \frac{E_R R_L}{2R_L + R}\left[B_n + \frac{B_{n-1}}{2} + \ldots + \frac{B_2}{2^{n-2}} + \frac{B_1}{2^{n-1}} + \frac{B_0}{2^n}\right]$$

where $B_k = 0$ or 1

TABLE 1

ANALOG-TO-DIGITAL CONVERTERS

	Company	Model No.	Number of Bits	Code and Logic Levels	Voltage Range	Pulse at Start of Conversion	Pulse at End of Conversion	Accuracy Percent of Full Scale	Accuracy Rank	Price with Power Supply	Price Rank	Conversion Time for One Word	Speed Rank	Remarks
1	Adage, Inc.	VR10-AB/NE	10 + sign	Binary 1 = +2.5v 0 = -2.5v	±10	Yes	Yes	±0.05% ±1/2 least bit	3	$3,700	5	59 µsec	6	
2	Adage	VR12-AB	12 + sign	Same	±10	Yes	Yes	±0.02% ±1/2 least bit	1	$3,800	6	66.6 µsec	7	
3	Dynamic System Electronics (DSE)	ADC-6A	11 + sign	2's complement 0 = -1v 1 = -7v	±10v	Yes	?	±0.05% ±1/2 least bit	3	$3,615	3	< 100 µsec	9	
4	DSE	ADC-6B	11 + sign	Binary 0 = -1v 1 = -7v	±10v	Yes	?	Same	3	$3,695	4	< 100 µsec	9	
5	DSE	ADC-3B	10 + sign	Binary 1 = -6v 0 = 0v	±10v	Yes	?	Same	3	$3,835	7	50 µsec	5	
6	DSE	ADC-3C	10 + sign	2's complement 1 = -6v 0 = 0v	±10v	Yes	?	Same	3	$4,670	9	33.3 µsec	3	
7	Epsco	TB-712	11 + sign	Binary 1 = +5v 0 = -5v	±10v	Yes	Yes	±0.025% ±1 least bit	2	$3,500	2	80 µsec	8	
8	Systems Engineering Laboratories	ADC-1B	11 + sign	Binary 0 = 0v 1 = -6v	±10v	Yes	?	±0.025% ±1/2 least bit	2	$6,504	11	≈46 µsec	4	Has track-hold
9	Radiator Inc.	5516	11 + sign	Binary 1 = -10v 0 = 0v	±10v	Yes	?	±0.025% ±1/2 least bit	2	$6,100	10	20 µsec	1	Has sample-hold
10	Packard Bell Corp.	ADC23-12B	11 + sign	2's complement 1 = -8v 0 = 0v	±10v	Yes	Yes	±0.025% ±1/2 least bit	2	$3,900	8	25 µsec	2	
11	Navcor	2202	10	Binary 1 = -6v 0 = -0.2v	±10v	Yes	Yes	±0.05%	3	$2,550	1	125 µsec	10	

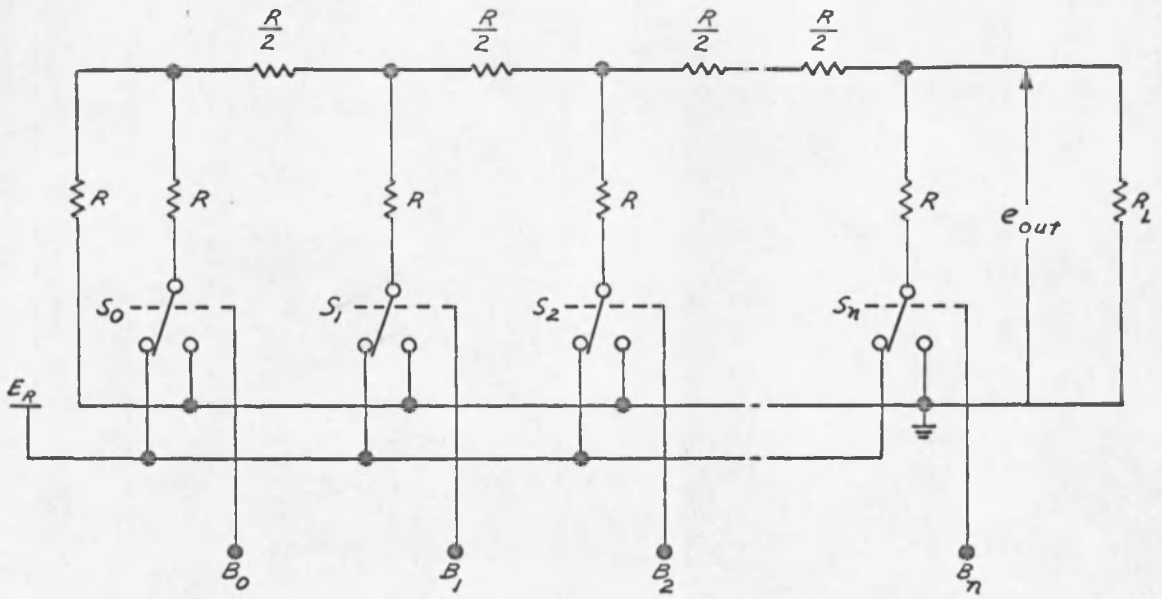


Figure 12. Voltage Decoding Ladder

A single-pole double-throw electronic switch is used in the ladder. This electronic switch can be constructed using a complementary NPN, PNP transistor pair with a driving circuit. A switch of this type is used because with the single-pole double-throw switch the decoding ladder always presents a constant impedance to the load.[11]

The weighted-resistor decoder is shown in figure 13. The equation for the output voltage here is:

$$e_{out} = \frac{E_R}{\frac{R}{R_L} + 2^{n+1} - 1}\left[E_o 2^n + B_1 2^{n-1} + \ldots + B_{n-1} 2 + B_n\right]$$

where $B_k = 0$ or 1 depending on the value of the input bit. The same type of single-pole double-throw electronic switch can be used in this decoder to obtain the same advantage.

Both types of decoders have the same theoretical accuracy. In practice a ladder decoder can have better accuracy than a weighted-resistor decoder because the ladder has a more uniform current distribution, and only two different size resistors are required. The weighted-resistor decoder is the faster of the two types because it has less wiring capacitance than the ladder network.[12]

An operational amplifier can be used with either type decoder to give better accuracy because of the high input impedance and low output impedance of the operational amplifier. In this application the accuracy and speed requirements are not too severe so either type of decoder can be used in the conversion system.

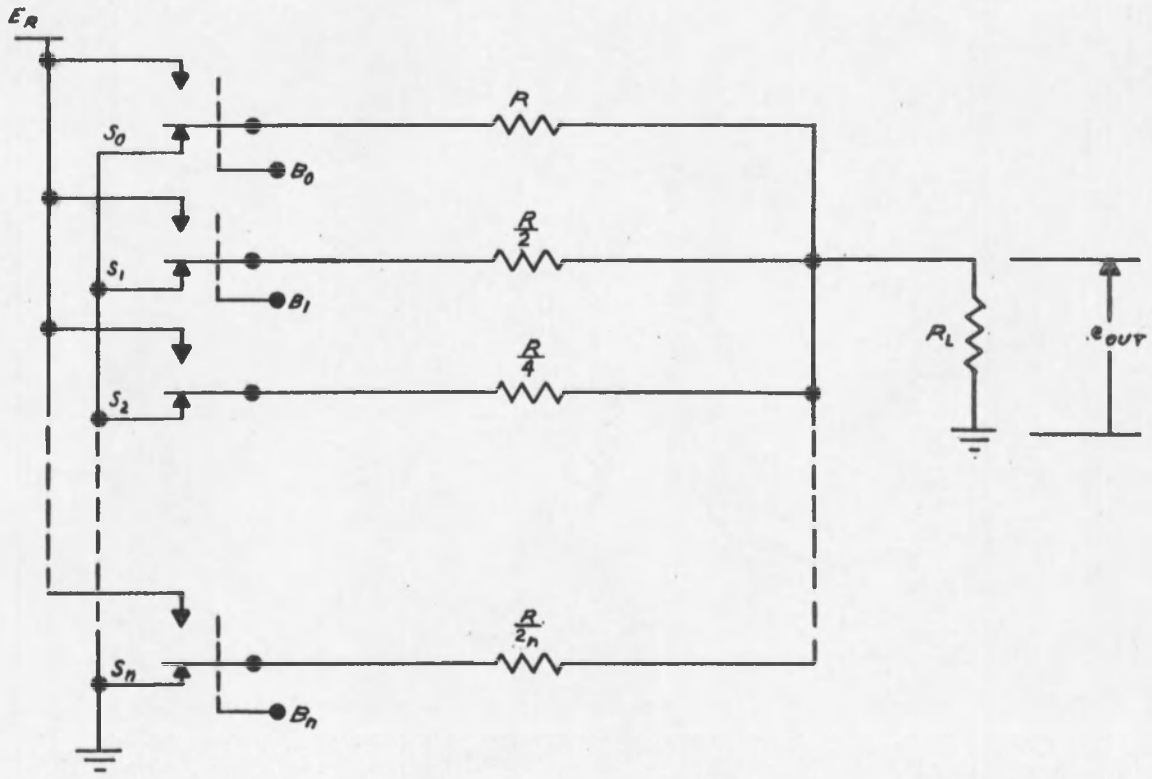


Figure 13. Voltage Decoder with Weighted Resistors

An output register is required to assemble the 11-bit output word because it is transmitted in two segments from the 7-bit transmit buffer. The output register also stores the output word to provide an input for the digital-to-analog converter.

The output register is to be made up of S-Pac flip-flops for the reasons stated previously. The Computer Control Corporation has a digital-to-analog converter of the weighted-resistor type that can be driven by the register flip-flops.[13] This decoder has acceptable performance and is compatible with the rest of the system. The block diagram of the decoder is shown in figure 14.

As shown in figure 15 the weighted decoder resistors are used as the summing resistors of an operational amplifier. To decode the 2's complement computer solution an additional summing resistor for the sign bit is required in addition to the 10 resistors of the S-Pac decoder. A reference voltage of -10 volts is used for the S-Pac decoder and a +10 volts reference is switched to the 6k resistor if the digital output is negative. The Astrac II reference source (±10 volts, ±0.01 percent) may be used here.

As the gain of the operational amplifier approaches minus infinity and the input impedance approaches infinity, a very good approximation of the output voltage is:

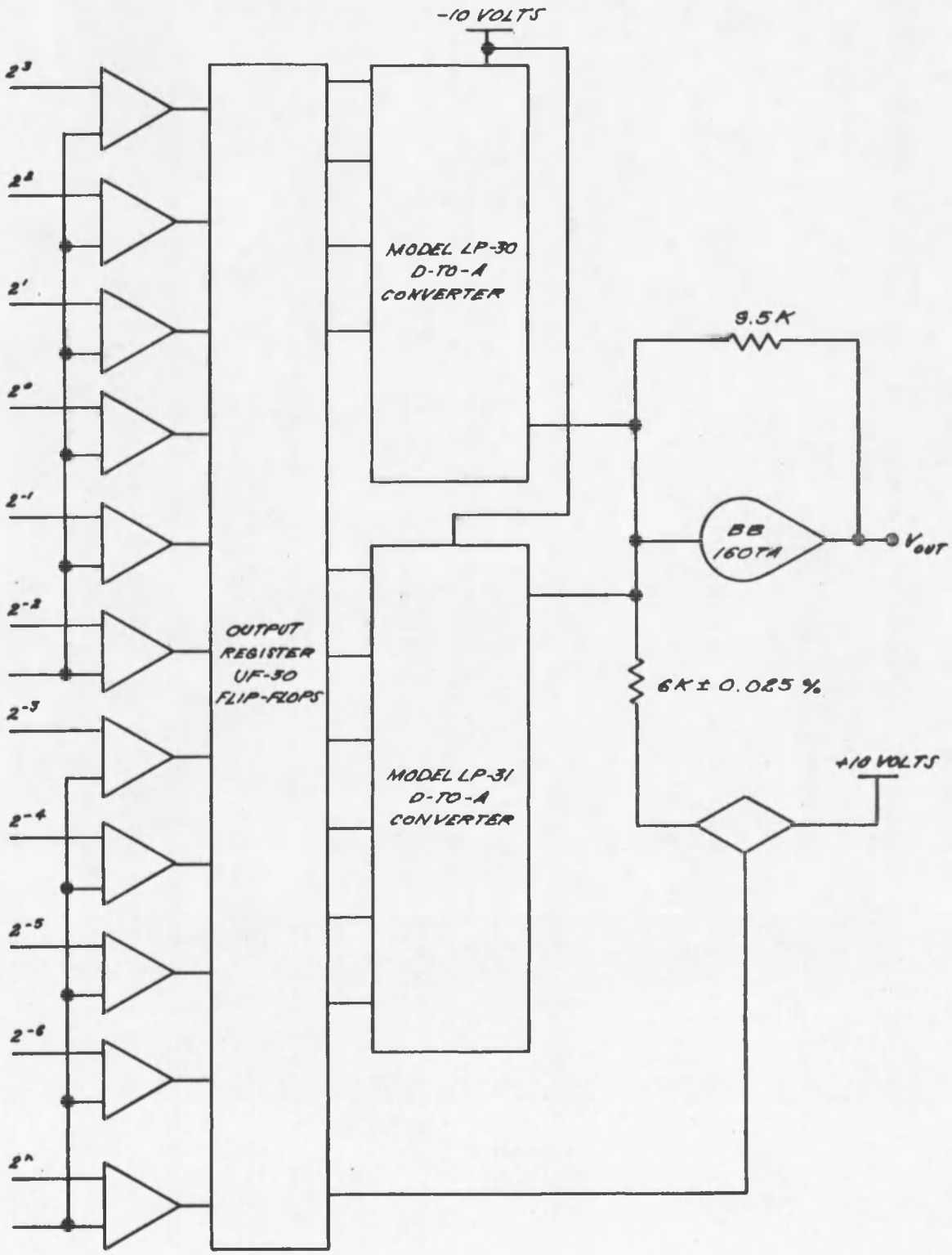


Figure 14. Digital-to-Analog Conversion System

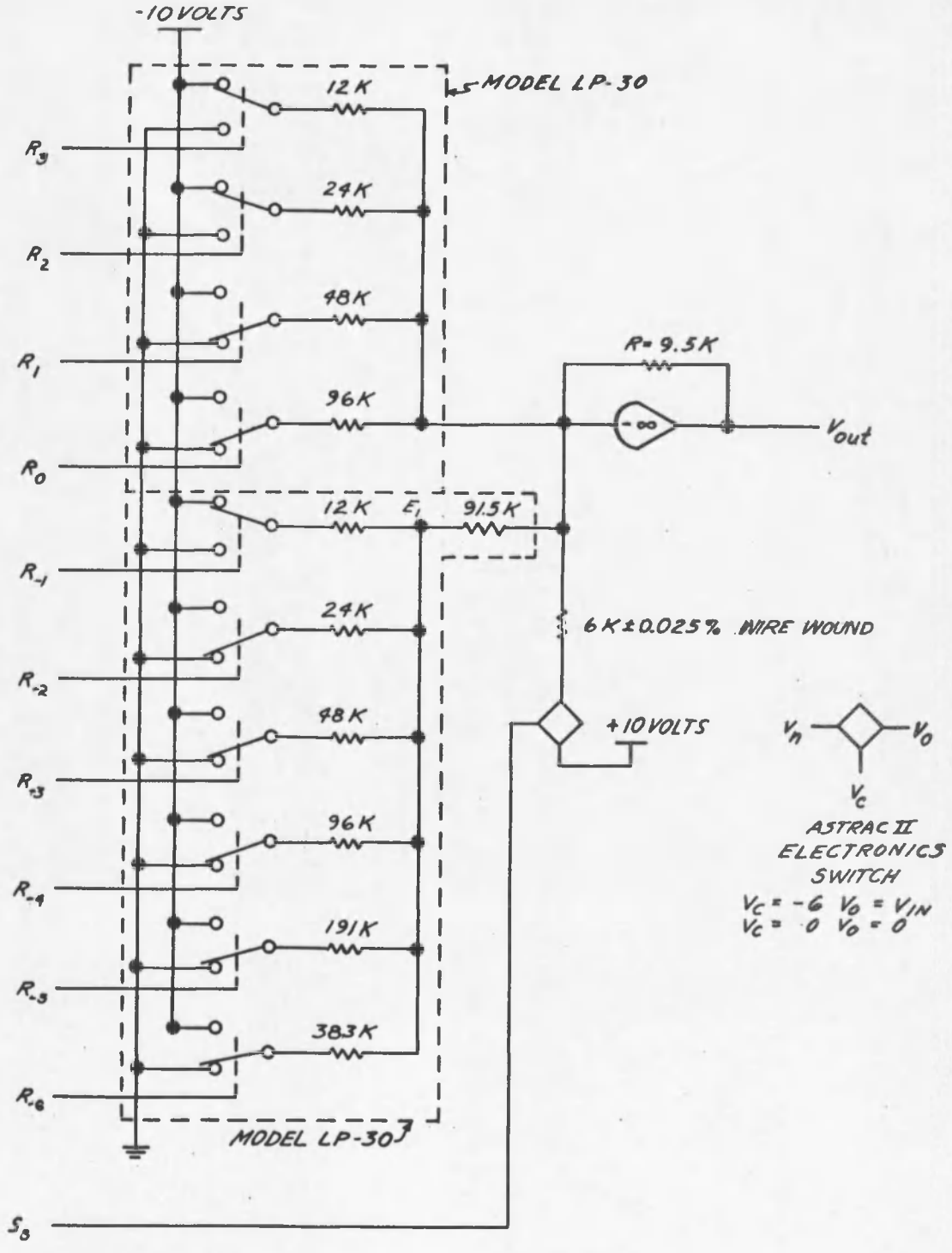


Figure 15. S-Pac Decoder Using Weighted Resistors

$$V_{out} = 8\left(R_3 + \frac{R_2}{2} + \frac{R_1}{4} + \frac{R_0}{8}\right) + \frac{8}{16}\left(R_{-1} + \frac{R_{-2}}{2} + \frac{R_{-3}}{4} + \frac{R_{-4}}{8} + \frac{R_{-6}}{16}\right) - 16\, S_s$$

where R_k = the logical value of the 2^k significant bit.

The decoding accuracy is ±0.05 percent of the reference voltage or ±0.06 percent overall. The maximum error in decoding is ±6 millivolts. The settling time of the weighted resistor network, including electronic switches is about 5 microseconds.

4.4 Control Logic

The basic aim of the control logic is to use the track-hold pulses, the analog-to-digital converter pulse output, and the completion pulses of the digital computer to synchronize the operation of these units in order to provide fast and accurate operation of the complete hybrid system.

The track-hold pulses from the Astrac II clock operate four track-hold circuits in a preset sequence. The track-holds store the selected voltages until they can be converted to digital form. The outputs of the track-hold circuits are connected to a multiplexer consisting of an Astrac II electronic switch which connects each voltage in turn to a summing resistor of an operational amplifier. The output of the multiplexer is the voltage input to the Packard Bell Model ADC23-12B analog-to-digital converter.

The block diagram of the analog-to-digital conversion system is shown in figure 16.

The first track-hold pulse resets all the hold-pulse and selector counter flip-flops with its leading edge (figure 17). The trailing edge of this pulse sets the first hold-pulse flip-flop to the one state which in turn switches the multiplexer to the first input voltage and starts the analog-to-digital converter after a 1.4 microsecond delay.[14] The 1.4 microsecond delay is introduced to delay the start of the conversion until the switching transients of the multiplexer have time to decay.

The end of the conversion process is signaled by an end-of-conversion pulse from the analog-to-digital converter. When the conversion is complete, the 11-bit parallel output of the analog-to-digital converter has to be sent to the digital computer. The peripheral interface adapter receive buffer has a size of only 7 bits so the input process takes two steps. The first 6 bits are transmitted to the receive buffer when the end-of-conversion pulse resets flip-flop FF-1 to connect the first six inputs to the receive buffer (figure 18). The end-of-conversion pulse also signals the receive buffer control block to start the receive process. After the first 6 bits are transmitted through the receive buffer to the "S" register, an output signal (CCRB) from the receive buffer control block triggers the flip-flop FF-1 to connect the other 5 inputs to the receive buffer. The

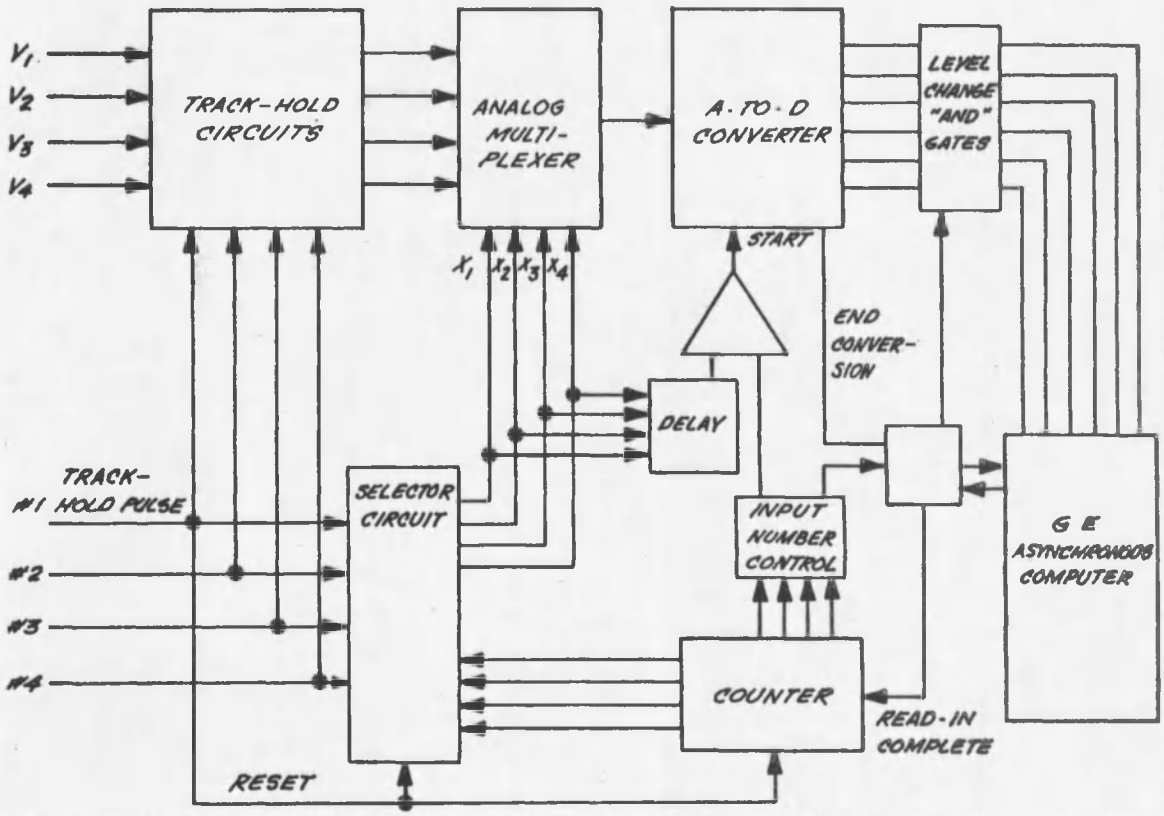


Figure 16. Analog-to-Digital Conversion System

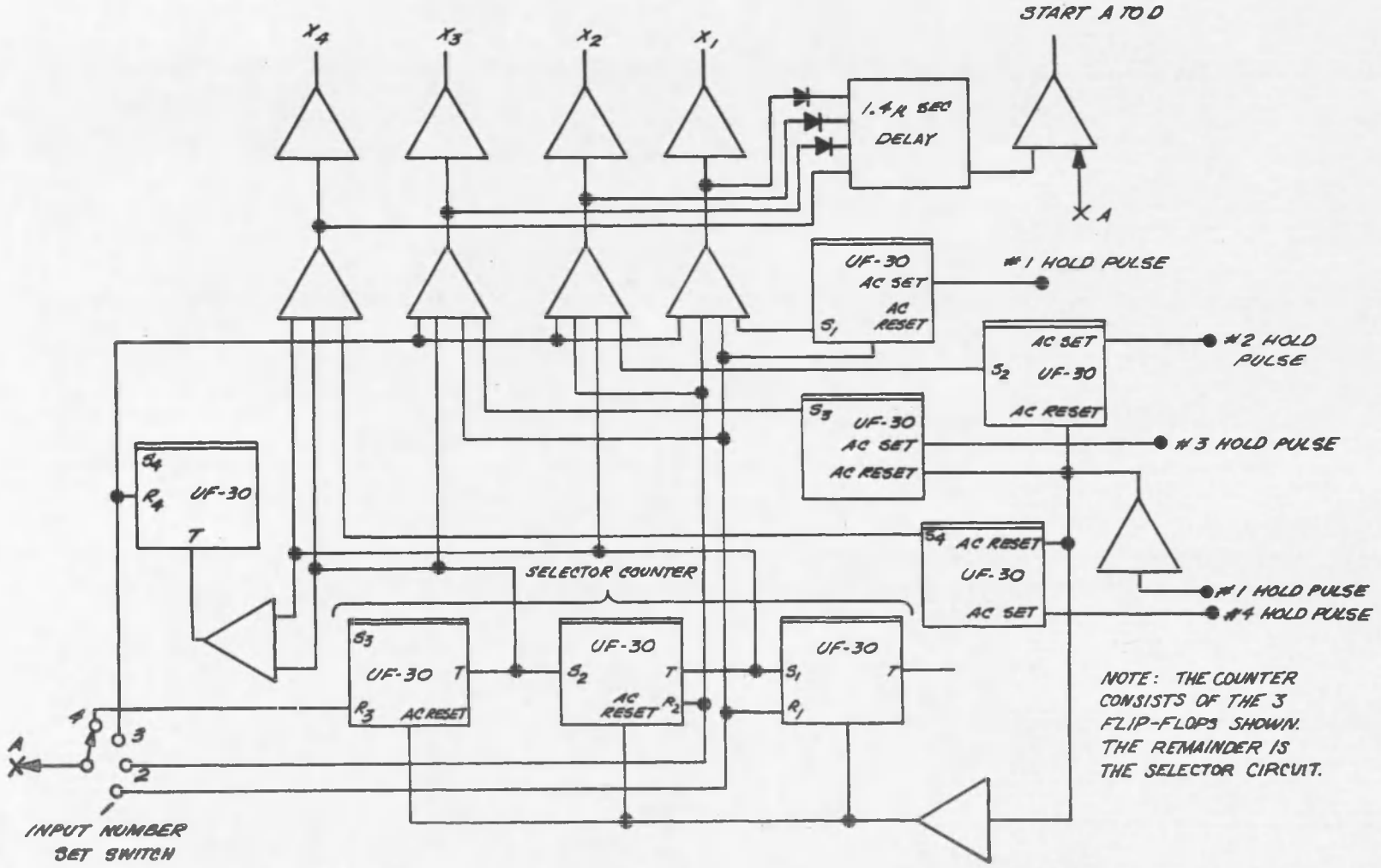


Figure 17. Control Logic

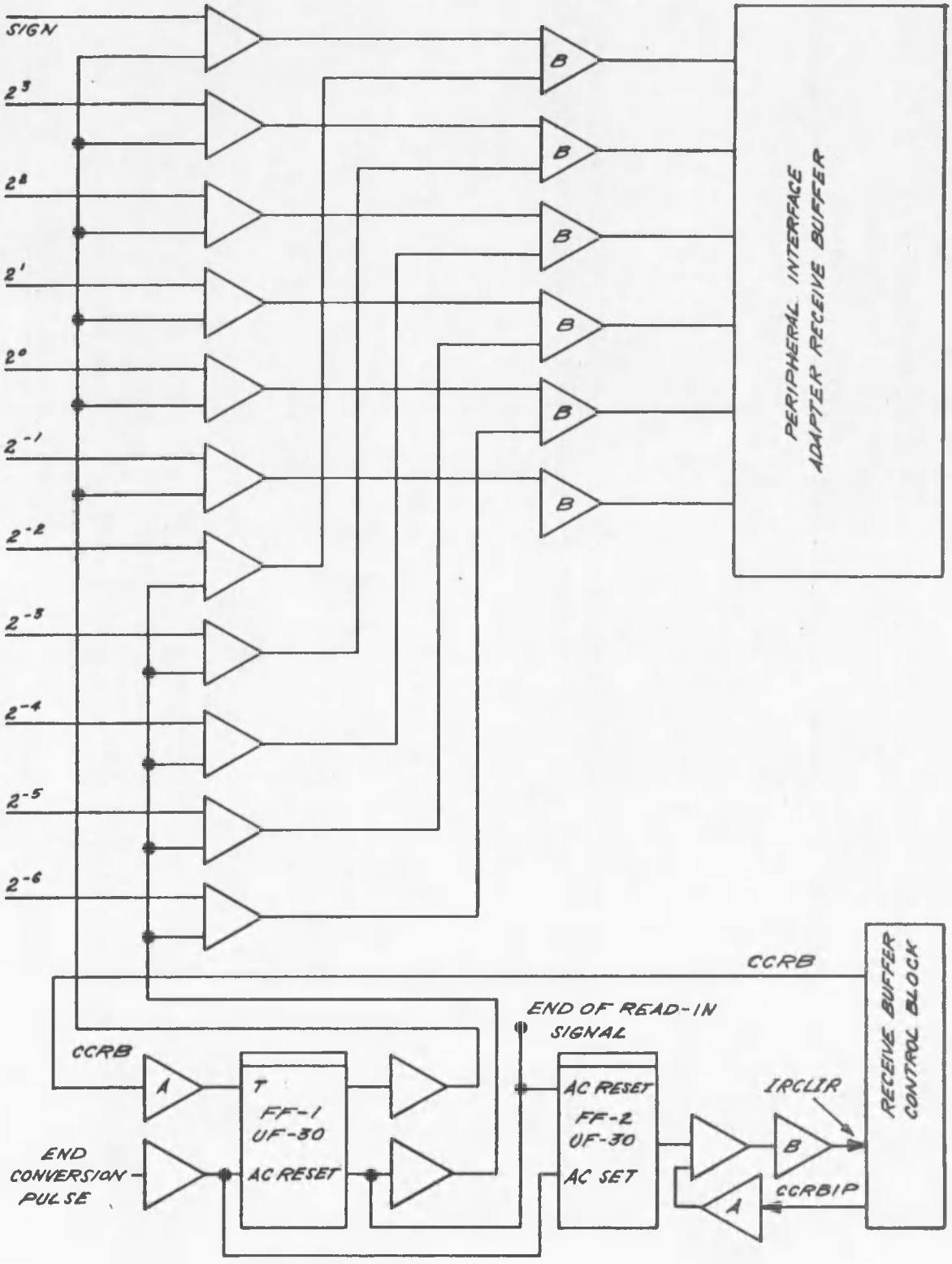


Figure 18. Read-In Logic

computer must be programmed to assemble the two groups of bits into a single 11-bit word in the accumulator, after which the word may be used in computations or stored in memory as desired.

The digital computer is controlled by the conversion system to the degree that when a coded word is available from the analog-to-digital converter, a pulse on the TRCLIR input will signal the receive buffer control block to interrupt the computations in progress in order to receive the coded word.

The computer output signal (CCRB) that connects the second set of inputs to the receive buffer also is the read-in complete input to the selector counter.

The first read-in complete pulse sets the selector counter to 001. As the other hold pulses occur, they are each recorded by setting a hold pulse flip-flop. When the selector counter is set to 001 and the second hold pulse flip-flop has been set, the second input voltage is connected to the analog-to-digital converter and a delayed pulse starts the converter.

The second read-in complete pulse sets the selector counter to 010. To avoid an error during the transition time when both the first and second selector counter flip-flops may be zero, the first read-in complete pulse resets the first hold pulse flip-flop.

When both the second read-in complete pulse and the third track-hold pulse have occurred, the third input is connected to the analog-to-digital converter and the conversion process is started.

Next, the third read-in complete pulse sets the selector counter to the 011 state. This state triggers a flip-flop that locks the outputs X_1, X_2, and X_3 preventing the next read-in complete pulse from starting another conversion process.

After both the third read-in complete pulse and the fourth track-hold pulse occur, the final conversion process in the cycle is started. When the fourth read-in complete pulse sets the selector counter to the 100 state, any extraneous analog-to-digital converter start pulses and/or read-in complete pulses are blocked out by the third selector counter flip-flop output.

The conversion process for less than four inputs is just like the process described above except that a different selector counter output blocks off the converter-start and read-in complete pulses. The control logic is set to the number of inputs used by a switch that connects the appropriate selector counter output to the block-out line.

The buffer output control logic (figure 19) is made necessary by the 7-bit size of the peripheral interface adapter transmit buffer. A signal is available from the transmit buffer control block when there is information in

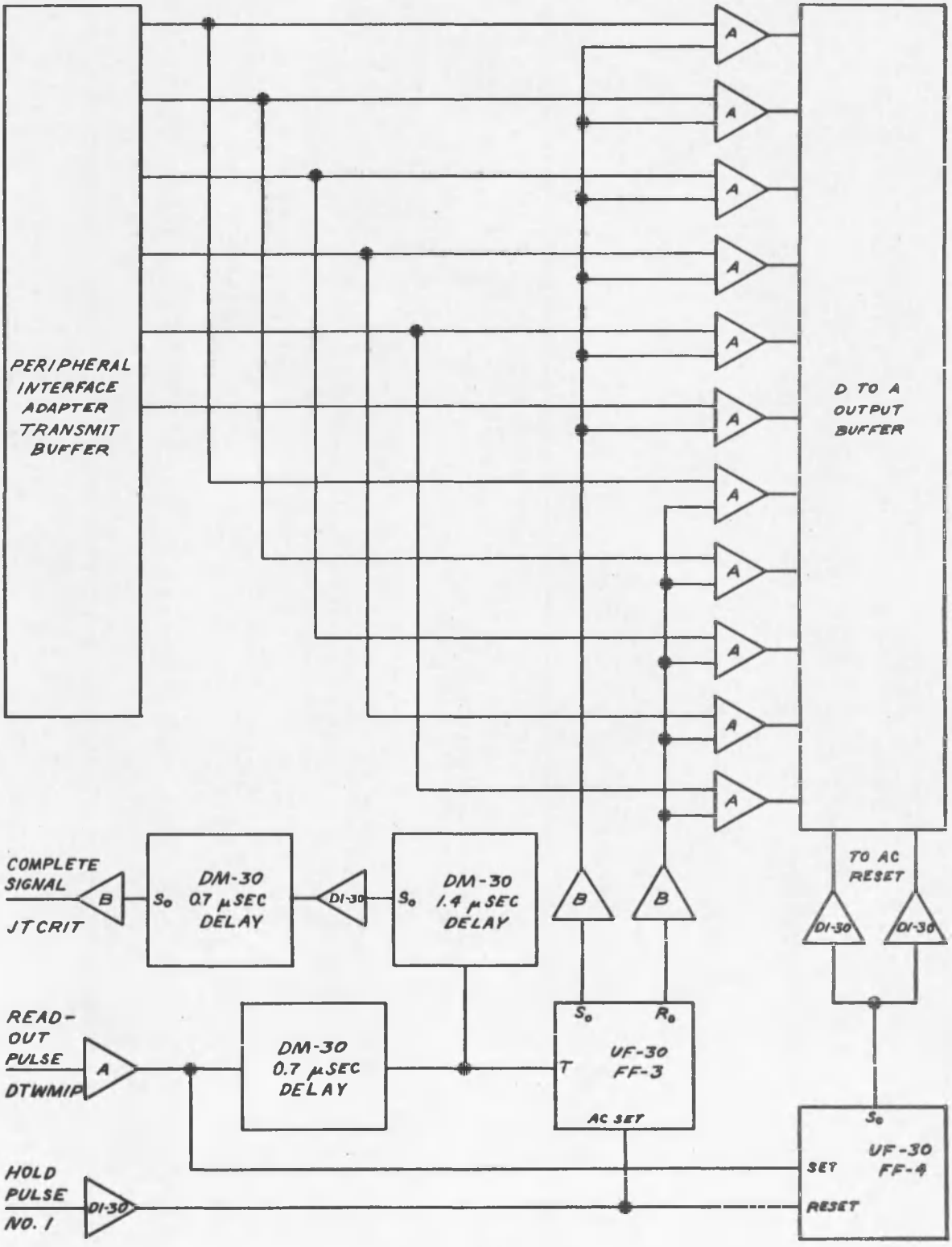


Figure 19. Output Logic

the transmit buffer. This read-out pulse from the transmit buffer control block resets the digital-to-analog output buffer and after a 0.7 microsecond delay connects the transmit buffer to the inputs of the six most significant bit positions of the digital-to-analog output buffer. A complete signal 1.4 microseconds after the two buffers are connected together is sent to the transmit buffer control block (input JTCRIT) to allow the next 5 bits of the output word to be placed in the transmit buffer. Another read-out pulse then connects the transmit buffer to the inputs of the remaining five positions of the digital-to-analog output buffer. Another complete signal is sent to the transmit buffer control block, allowing the transmit buffer again to send information when the next output word arrives.

The leading edge of the first hold pulse places the two output control flip-flops, FF-3 and FF-4, in the correct states for the next output cycle.

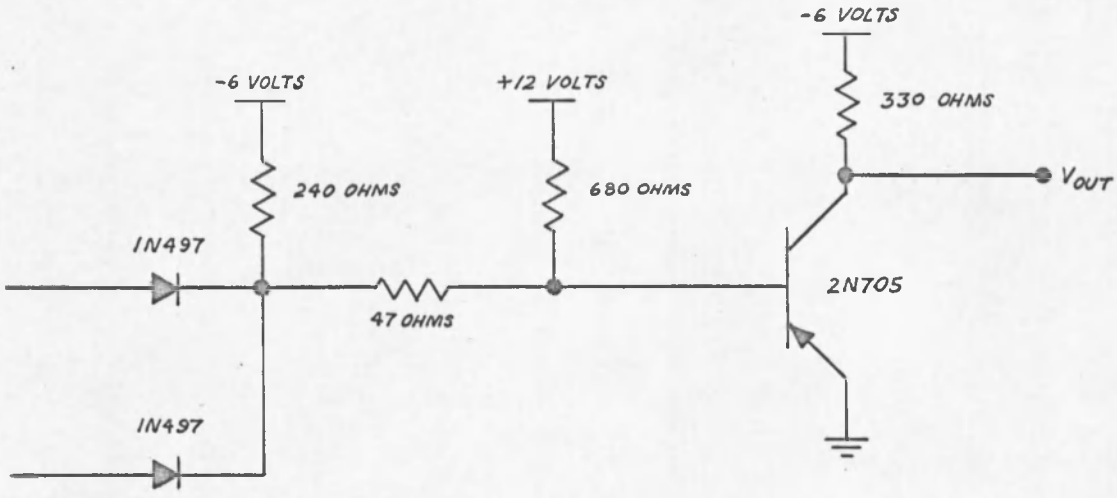
4.5 Specially Designed Circuits

The logic voltage levels are not the same throughout the digital-analog conversion system. The GE digital computer logic levels are $0 \equiv 0$ volt and $1 \equiv -2.33$ volts. The S-Pac digital modules have $0 \equiv 0$ volt and $1 \equiv -6$ volts logic levels. The Packard Bell analog-to-digital converter has $0 \equiv 0$ volt and $1 \equiv -8$ volts. The three parts of the system all use negative logic.

To change the logic levels of the digital computer so the output word can be placed in the digital-to-analog output register on arrival of the readout pulse requires a Nand gate. The Nand gate inputs have the digital computer voltage levels and the outputs, the S-Pac logic levels. Nand gate type A performs the above operations as shown in figure 20. The design was arrived at by using the worst case method.

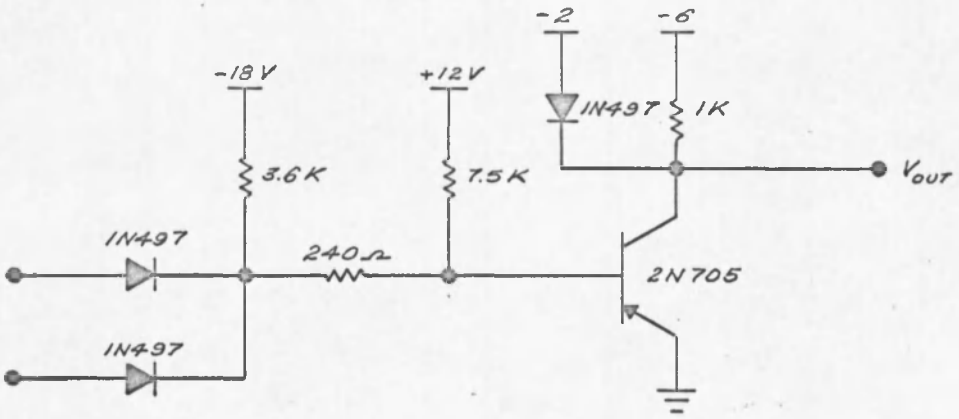
The logic level of the analog-to-digital converter is changed in order to be an input to the digital computer using the Nand gate shown in figure 21 (type B). To accurately clamp the Nand gate B output at -2.33 volts, a -2 volt reference supply is necessary.[15] The circuit for the -2 volt supply is shown in figure 22.

The end conversion pulse of the analog-to-digital converter and the parallel coded output must operate to an S-Pac Nand gate. The -8 volt level can be changed to -6 volt input with a simple resistor divider network.



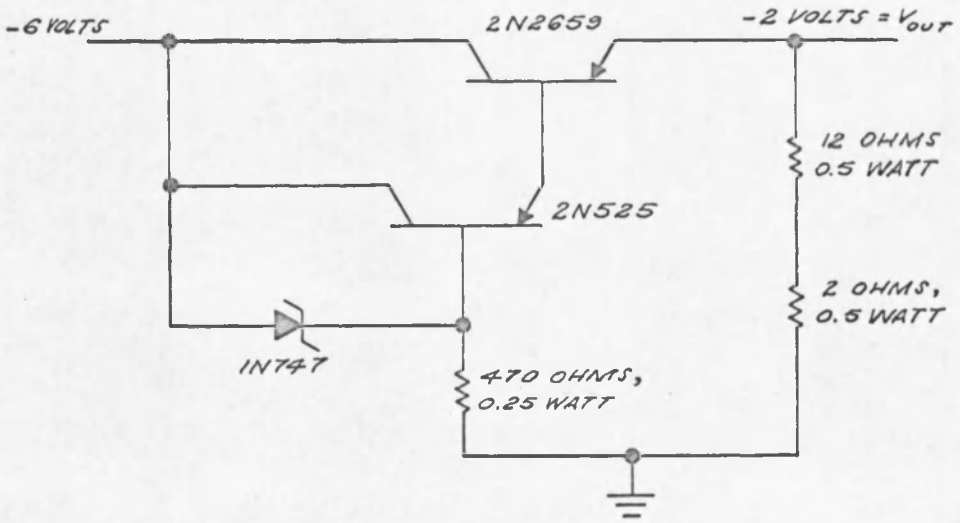
Notes: 1. Input Levels: -2.33 volts ≡ 1, 0 volts ≡ 0;
Output Levels: -6 volts ≡ 1, 0 volts ≡ 0.
2. All resistors 5 percent, 1/4 watt.
3. 14 gates of this type used.

Figure 20. Nand Gate, Type A



Notes: 1. Input Levels: -6 volts, -8 volts ≡ 1, 0 volts ≡ 0;
Output Levels: -2.3 volts ≡ 1, 0 volts ≡ 0.
2. All resistors 5 percent, 1/4 watt.
3. 10 gates of this type used.

Figure 21. Nand Gate, Type B



All resistors 5 percent

Figure 22. -2 Volt, 150 MA Reference Supply

CHAPTER 5

CONVERSION SYSTEM CHARACTERISTICS

5.1 Operation

Astrac II and the GE digital computer can be used in several different modes in conjunction with the conversion system. In any mode the conversion system is still controlled by the Astrac II clock and selector asynchronous digital computer pulses.

Each sampling can be done at a different time during a cycle but there is only one sampling rate. The number of inputs used is set on the input number switch, and the respective track-hold pulses are connected with jumper wires to the conversion system. The particular mode used is set on Astrac II and in the digital computer program, not in the conversion system.

5.2 Performance

The maximum length of time it takes to convert a voltage input to a word stored in the digital computer memory is 40 microseconds. This value is an estimate since the exact computer read-in time is not known. A digital word can be converted to an analog output in about 10 microseconds. If all four voltage inputs are used, the total conversion, analog-to-digital and digital-to-analog, will

take about 170 microseconds at the longest. The time available before the next sample for computation by the digital computer in the mode where all voltages are sampled simultaneously and at the fastest sampling rate is 730 microseconds. If it is desired to perform all digital computations during the reset period, and sample four voltages, the Astrac II clock rate should be held under 200 cps.

Errors in the conversion process start with the quantizing of the input voltage in the analog-to-digital conversion. With the 10-bit plus sign analog-to-digital conversion used, the quantizing error is ±1/2 least bit = ±5 millivolts. The maximum error in decoding the digital output is ±6 millivolts. The maximum analog-to-digital and digital-to-analog conversion error is ±11 millivolts or ±0.11 percent of full scale.

The above comprises the static accuracy. In addition there may be sampling error if there are frequency components greater than one-half the sampling frequency in the input.[16] The sampling rates selected must take this fact into account.

5.3 Conversion System Cost

The cost breakdown of the conversion system is shown in table 2. The largest single item is the analog-to-digital converter. The total cost of the S-Pacs is $1,694.00.

TABLE 2

CONVERSION SYSTEM COST BREAKDOWN

1	1	Model ADC-12B-B A/D Converter	$3,900.00
2	12	Model UF-30 Universal Flip-Flop Pac	730.00
3	2	Model DM-30 Delay Multivibrator Pac	262.00
4	1	Model DC-30 Diode Pac	40.25
5	3	Model DI-30 Nand Gate Pac	244.50
6	1	Model LP-30 Precision D/A Converter Pac	138.50
7	1	Model LP-31 Precision D/A Converter Pac	118.75
8	2	Burr-Brown 1607A Operational Amplifier	380.00
9	5	Electronic Switch Burr-Brown	≈ 900.00
10	6	±0.025 Percent Precision Resistors	40.00
11		Resistor, Transistor, Diodes for Gates and Level Change	100.00
And if necessary			
12	1	Model RP-30 Power Supply	395.00
		Total Less Power Supply	$6,841.00
		Total	$7,236.00

The power requirements for the conversion system are 1.4 amperes at -6 volts, 360 milliamperes at +12 volts, and 1.200 amperes at -18 volts. If this power is supplied by the Astrac II power supplies, the cost of the conversion system will be $400 less. The total cost of the conversion system not including labor but with a power supply is $7,400, assuming no special discount.

5.4 Conversion System Reliability

The conversion system reliability should be quite good. The major part of the system is assembled from CCC-Pac digital modules. The S-Pac modules were designed using very conservative assumptions on power dissipation, transistor and diode characteristics, and the change in component values with time. The S-Pacs are probably the most reliable digital modules made for general use.

The Packard Bell analog-to-digital converter is of a proven design that is in wide use. The converter performance is warranted for one year.

The logic circuits made especially for the conversion system were designed using worst case methods and should give reliable service if each gate is thoroughly tested.

CHAPTER 6

CONCLUSION

The overall analog-digital conversion system is shown in figure 23. The conversion system of figure 23 was arrived at by examining three basic methods of analog-to-digital conversion and two basic methods of digital-to-analog conversion.

The final system meets all the design criteria of Chapter 3 including an analog-to-digital, digital-to-analog conversion accuracy of about ±0.11 percent of full scale. The cost of $7,000 is the lowest price that could be obtained commensurate with performance and reliability. The analog-digital conversion system designed will connect Astrac II and the GE asynchronous computer together in a hybrid computing system that will be fast, accurate, and reliable.

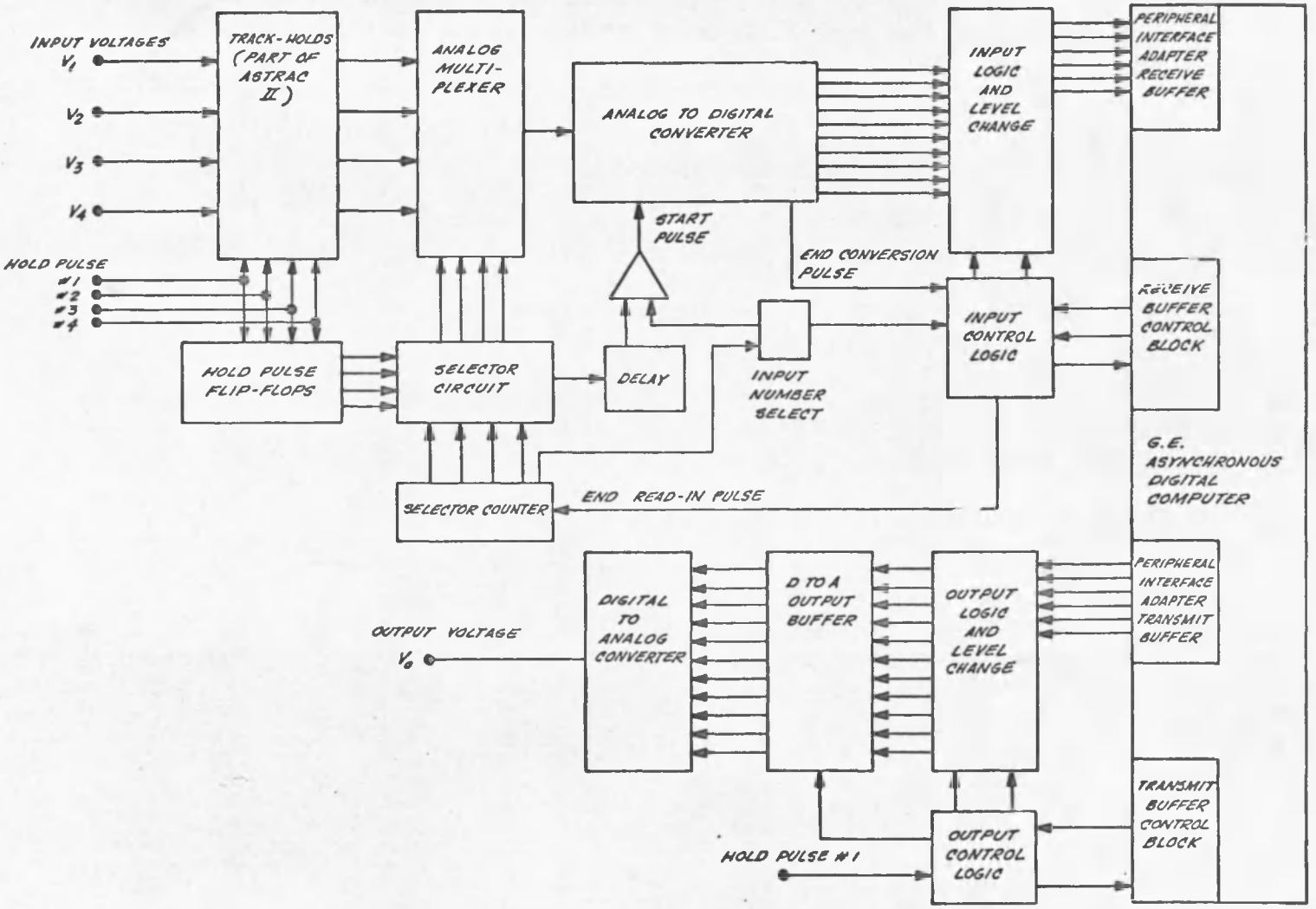


Figure 23. Complete Analog-Digital Converter

LIST OF REFERENCES

1. BEKEY, G. A.: Notes on Hybrid Computing Techniques. Department of Engineering, University of California, Los Angeles, 1963, Chapter 12, p. 1.
2. KARPLUS, W. J.: Notes on Hybrid Computing Techniques. Department of Engineering, University of California, Los Angeles, 1963, Chapter 1, pp. 11-13.
3. KORN, G. A.: Notes on Hybrid Computing Techniques. Department of Engineering, University of California, Los Angeles, 1963, Chapter 18, p. 21.
4. ECKES, H. R. and KORN, G. A.: Digital Program Control of Iterative Differential Analyzers. ACL Memo No. 86. College of Engineering, Department of Electrical Engineering, The University of Arizona, Tucson, Arizona, 1963.
5. BEKEY, G. A.: Notes on Hybrid Computing Techniques. Department of Engineering, University of California, Los Angeles, 1963, Chapter 2, p. 6.
6. Instruction Manual for S-Pac Digital Modules. Computer Control Company, Incorporated, Framingham, Massachusetts, Chapter 2, p. 2, Chapter 3, pp. 35-36 and 241-248.
7. SUSSKIND, A. K. (Ed): Notes on Analog-Digital Conversion Techniques. The Technology Press, Boston, 1957, Chapter 5, pp. 2-19.

LIST OF REFERENCES (cont)

8. SUSSKIND, A. K. (Ed): Notes on Analog-Digital Conversion Techniques. The Technology Press, Boston, 1957, Chapter 5, pp. 56-60.

9. SUSSKIND, A. K. (Ed): Notes on Analog-Digital Conversion Techniques. The Technology Press, Boston, 1957, Chapter 5, pp. 54-56.

10. SUSSKIND, A. K. (Ed): Notes on Analog-Digital Conversion Techniques. The Technology Press, Boston, 1957, Chapter 5, pp. 28-40.

11. PEARMAN, C. R. and POPODI, A. E.: How to Design High-Speed D-A Converters. Electronics. February 21, 1964, pp. 28-32.

12. PEARMAN, C. R. and POPODI, A. E.: How to Design High-Speed D-A Converters. Electronics. February 21, 1964, p. 29.

13. Instruction Manual for S-Pac Digital Modules. Computer Control Company, Incorporated, Framingham, Massachusetts, Chapter 3, pp. 123-134

14. Instruction Manual for S-Pac Digital Modules. Computer Control Company, Incorporated, Framingham, Massachusetts, Chapter 3, pp. 53-60.

15. JOYCE, M. V. and CLARKE, K. K.: Transistor Circuit Analysis. Addison-Wesley Publishing Company, Reading, Pennsylvania, 1962, pp. 206-211.

LIST OF REFERENCES (cont)

16. RAGAZZINI, J. R. and FRANKLIN, G. F.: Sampled-Data Control Systems. McGraw-Hill Book Company, New York, 1958, pp. 16-19.