A FAST QUARTER-SQUARE MULTIPLIER

by

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2/17/64
DATE

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ABSTRACT

This report describes the design and performance of a fast wideband quarter-square diode multiplier designed to work with the ±10 volt low-impedance computing circuits of a high-speed iterative differential analyzer (ASTRAC II), or in other hybrid analog-digital computer systems. To reduce cost, the new multiplier employs absolute-value squaring circuits and does not require committed computer amplifiers. Improved combination shunt-series switching circuits and low resistance values ensure wide bandwidth (± 0.5 per cent of half scale dynamic error at 10 Kc, 1 degree phase shift at 70 Kc). Temperature-compensating diodes in the bias networks reduce thermal drift below 0.7 mv/deg C, so that the multiplier static accuracy of ± 0.20 per cent of half scale is maintained from 15 to 40 degrees C. A number of useful design hints are listed.

Chapter 1

INTRODUCTION

This report describes the design of a new analog multiplier developed for a high-speed iterative differential analyzer, ASTRAC II (Arizona Statistical Repetitive Analog Computer II). ASTRAC II is a fast iterative analog computer with sophisticated digital controls and special components for statistical and optimization problems.[1] The large bandwidth of its analog computing components permits up to 1000 repetitions per second as well as real-time simulation. A large sample of solutions can be obtained quickly enough so that simulated-system statistics taken over 1000 to 10,000 computer runs can be optimized manually or automatically in a very short time.

Because of the low computing impedances used with ASTRAC II (1 K and 5 K summing resistors), its speed is basically determined by the bandwidth of the operational amplifiers, rather than by the effects of external capacitances. ASTRAC II's operational amplifiers (similar to Burr-Brown type 1607A) have their unity-gain (0db) frequency at a minimum of 20 megacycles. Their small physical size permits them to be plugged directly into the rear of the computer patchbay without any signal wiring whatsoever, and their high current capability (30 Milliamperes at $\pm$ 10 volts up to 1 Mc) enables them to drive the remaining stray capacitance to relatively high frequencies. Other analog computing components--such as quarter-square multipliers--also plug directly into the rear of the patchbay (Fig. 1).

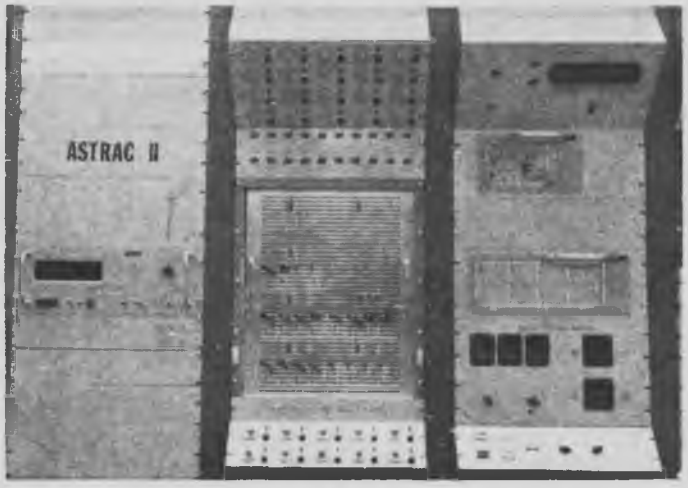


Fig. 1 ASTRAC II (Arizona Statistical Repetitive Analog Computer II)

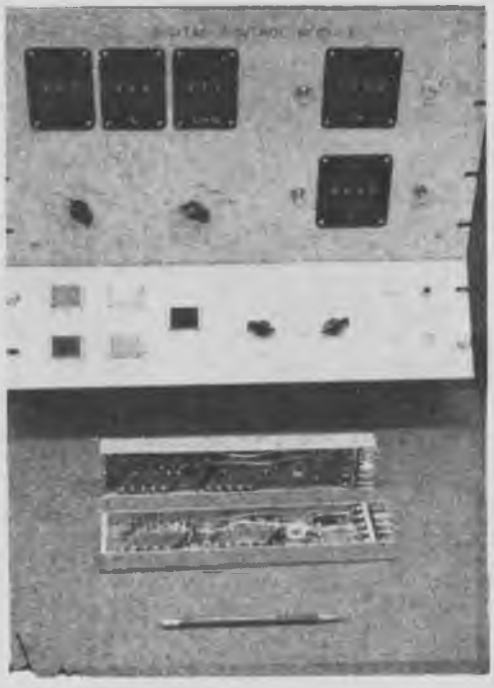


Fig. 2 Quarter-Square Multiplier Plug-In Modules

TABLE 1 ASTRAC II MULTIPLIER SPECIFICATIONS

Static accuracy.....± 0.20 per cent of half scale from 15 to 40 deg C. ± 0.10 per cent at 25 deg C.

Thermal drift.....Less than 0.7 mv/deg C.

Dynamic error

$XY/10 = (0)\ (10 \sin 2\pi ft)$

f(Kc)	E(± per cent of half scale)
0.1	0.10
1.0	0.10
10.0	0.20
50.0	0.80
100.	1.30

$XY/10 = (10)\ (10 \sin 2\pi ft)$

0.1	0.10
1.0	0.15
10.0	0.50
50.0	1.50
100.	2.50

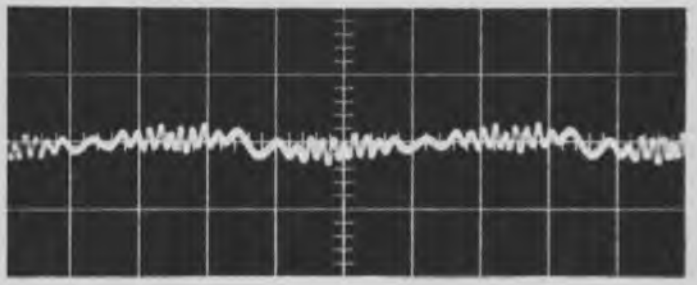
Driving Current Required.....17 ma from each driving amplifier
(See Fig. 6 for special low-current squaring inputs)

Maximum current to summing junction of output amplifier.....2 ma

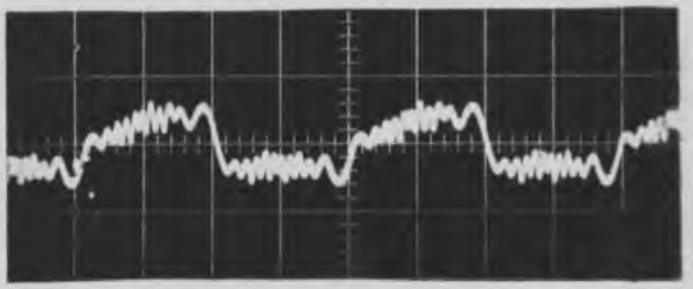
Input voltage range.....± 10 volts

Reference supplies.....± 10.000 volts at 4 ma each

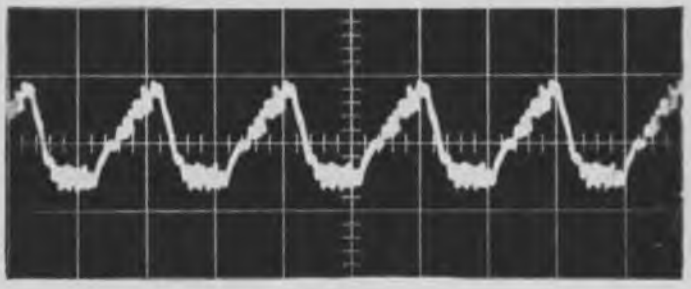
Fig. 3 In (a), (b), and (c) error photographs show the multiplier error in multiplying 10 times 10 sin $2\pi ft$ for f = 1 Kc, 5 Kc, and 10 Kc. The scale is 50 mv/cm or 0.50 per cent-of-half-scale/cm. (c) Clearly shows dynamic error is less than $\pm$ 0.50 per cent-of-half-scale at 10 Kc. In (d) a dual trace photograph shows the input and output of the multiplier for a $\pm$ 10 volt 10 Kc square wave multiplied by Y = -10. Different scale factors were used so that the two wave forms could be distinguished (the input is shown at 10 v/cm and the output at 5 v/cm).



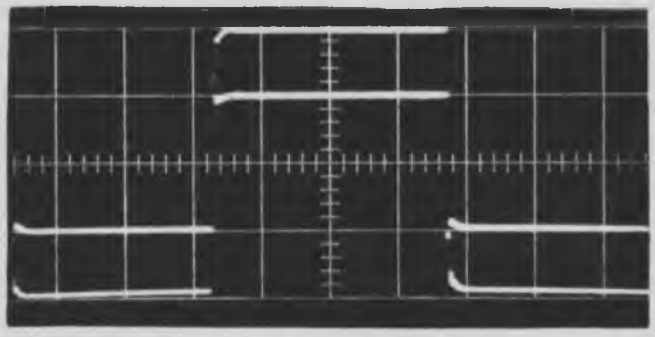
(a) 1 Kc



(b) 5 Kc



(c) 10 Kc



(d) 10 Kc

Fig. 3

Fig. 4. The positive absolut-value circuit shown generates a current proportional to $(X + Y)^2$. The circuit for $-(X - Y)^2$ is identical except that the diodes and bias polarities are reversed. A total of nine temperature-stabilizing diodes per squaring circuit in the bias line reduced thermal-drift error from $\pm$ 7 mv/deg C to $\pm$ 0.7 mv/deg C for squaring. A 15 pf capacitor and series resistor and capacitor to ground for phase-shift compensation are shown. This phase compensation extended the 0.5 per cent of half-scale error frequency by about one octave. Trimmer potentiometers are used to adjust the breakpoints for maximum accuracy of the square-law characteristic.

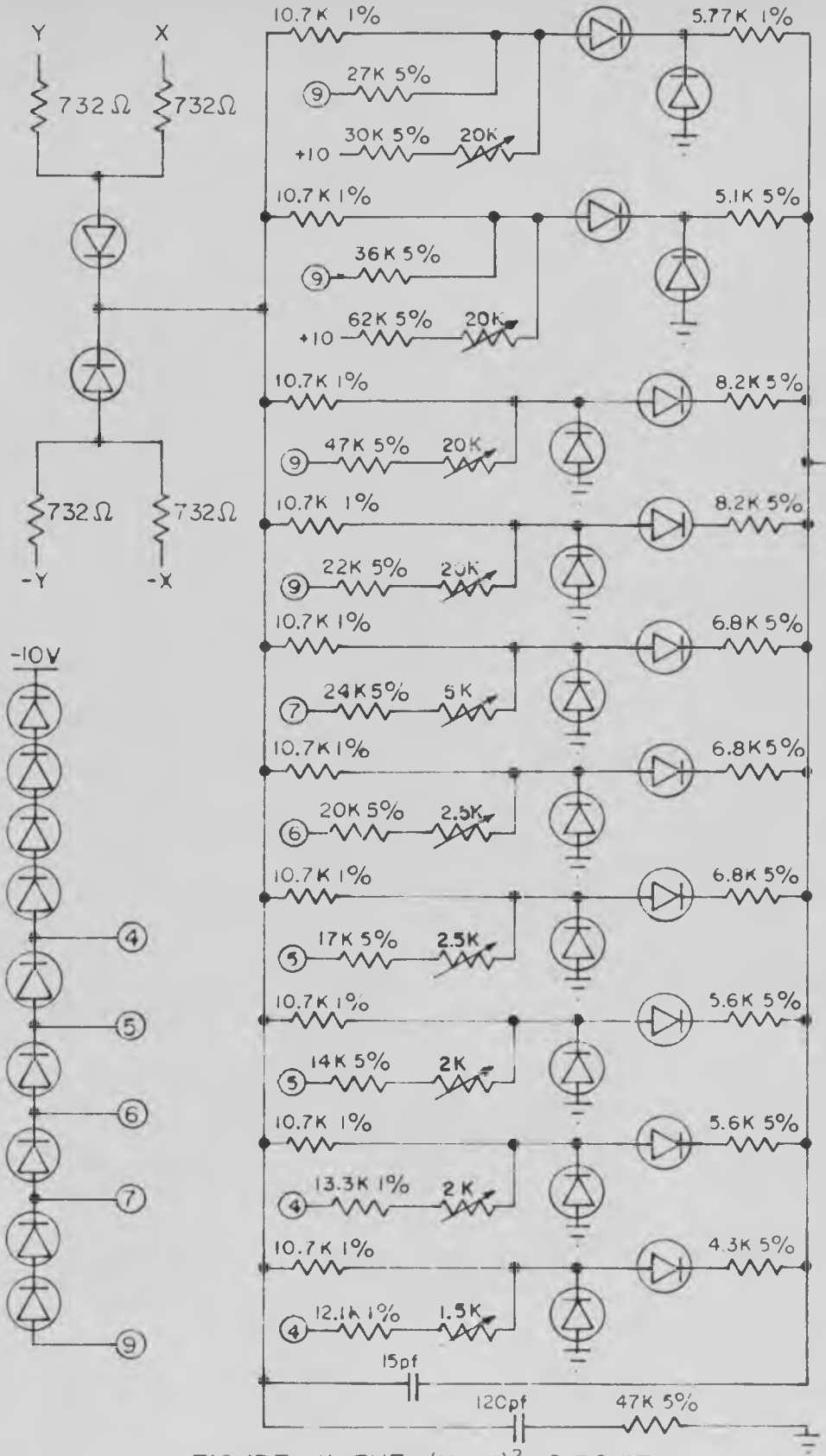


FIGURE 4. THE $(X+Y)^2$ CIRCUIT

Fig. 5. Two absolute-value squaring circuits implement quarter square multiplication. Special "Z" inputs permit squaring with reduced input current. In the multiplier module, the X and Y inputs to the positive squaring network are connected to the X and Y inputs of the negative squaring network also (this results in simpler patching); so, special inputs are necessary for using the positive network alone. Use of the multiplier inputs with X = Y for squaring would require 34 ma each for the two inputs (X = Y and -X = -Y), whereas with special squaring inputs, the current requirement is only 6 ma each. (The "Z" inputs are also useful for taking square-roots with the network placed in an operational-amplifier feedback loop.

Fig. 6. An equivalent loading circuit enables one to calculate the current requirements of the multiplier in any application. In normal multiplication, as a cost of the low-impedance wideband design, each of the four inputs can require up to 17 ma of driving current. The special squaring inputs require up to 6 ma only.

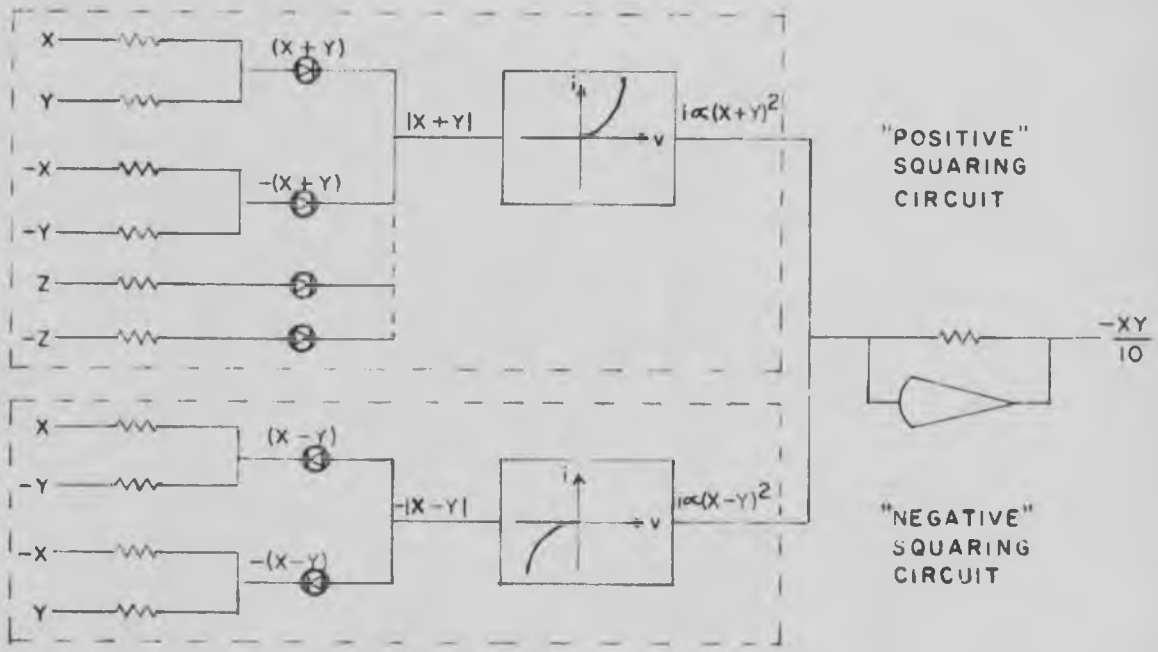

X
Y
-X
-Y
Z
-Z
(X + Y)
-(X + Y)
|X + Y|
i
v
i∝(X+Y)²
"POSITIVE" SQUARING CIRCUIT
-XY/10
X
-Y
-X
Y
(X - Y)
-(X - Y)
-|X - Y|
i∝(X-Y)²
"NEGATIVE" SQUARING CIRCUIT

Fig. 5

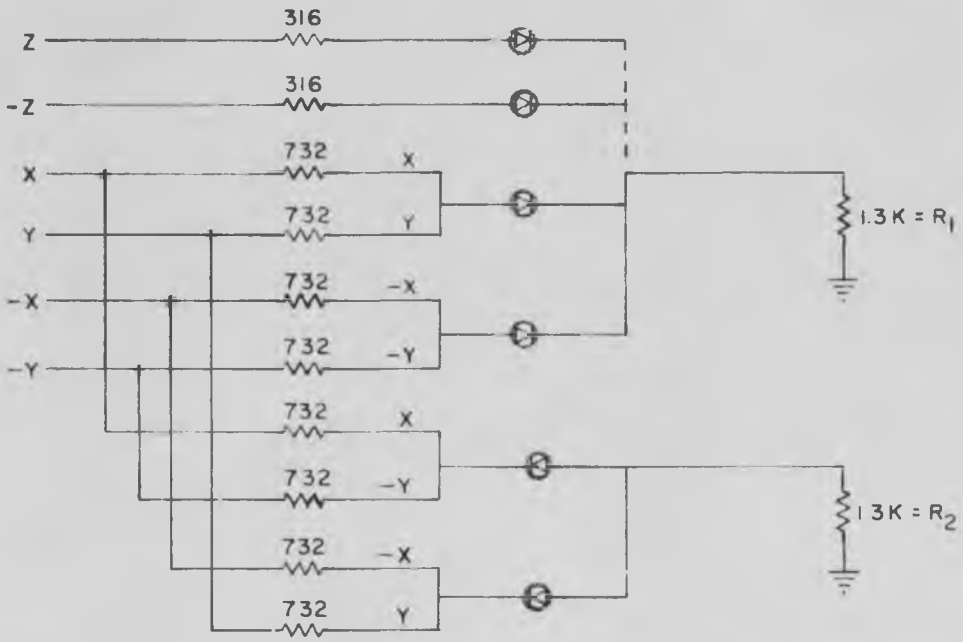

Z
-Z
X
Y
-X
-Y
316
316
732
732
732
732
732
732
732
732
X
Y
-X
-Y
X
-Y
-X
Y
1.3K = R1
1.3K = R2

Fig. 6

These compact all-solid-state circuits appear ideal for high frequency analog/hybrid computation.

A quarter-square multiplier network to be patched to an uncommitted computer amplifier and limited in dynamic accuracy only by the phase shift of the computer amplifiers themselves was desired. It was to employ absolute-value squaring circuits to reduce cost and to have a temperature-compensated static accuracy better than $\pm$ 0.20 per cent of half scale. The multipliers were to use $\pm$ 10 volt reference supplies and to be packaged in the standard plug-in module used for all of ASTRAC II's analog computing elements (Fig. 2). All these design goals were attained, as shown by the measured specifications of Table 1, and the error photographs in Fig. 3. Frequent adjustments are unnecessary, so that it is practical to plug the multiplier out of reach into the back of the computer patchbay.

Figure 4 shows one of the multiplier's two absolute-value squaring circuits. Figure 5 illustrates the principle of quarter-square multiplication with two absolute-value squaring circuits. This figure also shows special squaring inputs for squaring with reduced current requirement (See also Fig. 6). Figure 6 shows the equivalent loading circuit used to calculate the required input current.

Chapter 2

ANALYSIS OF CIRCUIT PERFORMANCE

Basic Principles

Quarter-square multipliers implement the relation

$$XY/V = \frac{1}{4V}\left[(X + Y)^2 - (X - Y)^2\right]. \qquad (1)$$

Fast and accurate squaring devices are required, one to square $(X + Y)$, and one to form $-(X - Y)^2$. Maximum errors from each of these two devices can add; for, if one has a maximum error for an input voltage V_1, and the other has a maximum error of the same sign for an input voltage V_2, then for X, Y, such that

$$\begin{aligned} X + Y &= V_1 \\ X - Y &= V_2 \end{aligned} \qquad (2)$$

the two maximum errors will add in Eq. (1). Consequently, $\pm$ 0.10 per cent of half-scale multipliers require $\pm$ 0.05 per cent of half scale squaring devices.

Absolute-Value Squaring

Diode squaring circuits can use separate diode networks to form the positive and negative halves of the parabolic transfer characteristic $Y^2 = aX^2$, or a single network preceded by an absolute-value circuit may be employed (Fig. 5). The latter alternative was chosen because

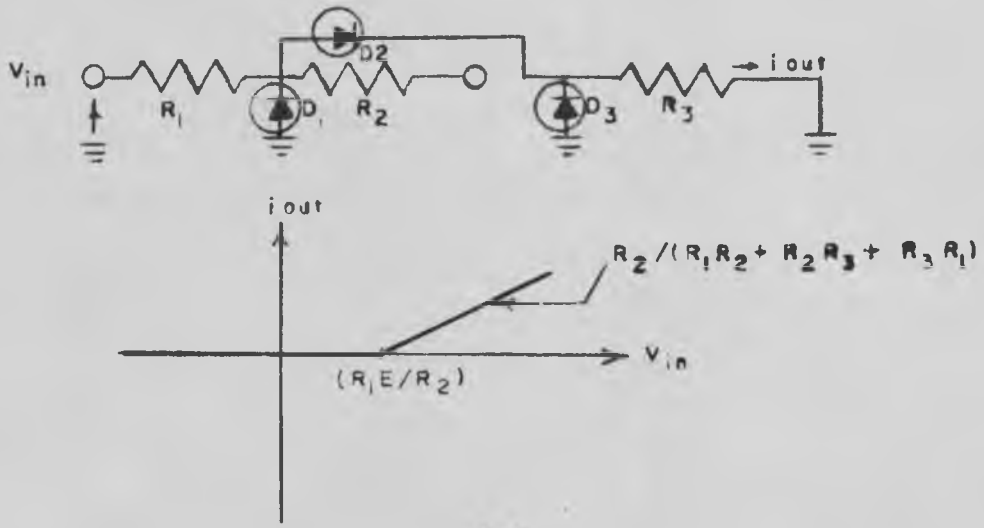
1. It is easier to trim a two-diode absolute-value circuit for symmetry than to match two complete diode networks.
2. It is less expensive and more compact.

Absolute-value squarers are, on the other hand, more difficult to design because of the complications inherent in cascaded diode limiters.

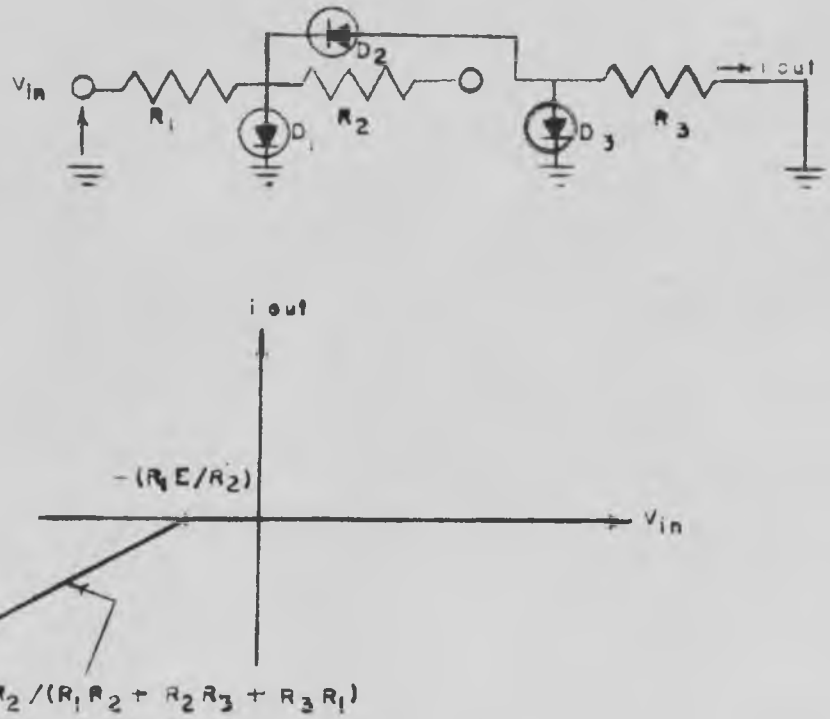
Error sources in the absolute-value circuit are the forward bias required to turn the diodes on, their nonlinearity after they are on, their finite recovery or turnoff time, their capacitance, and mismatch in their characteristics. These problems were overcome by slightly forward biasing the two diodes for zero input, by designing the square-law network for an accurate overall transfer characteristic which takes into consideration nonlinearities in the absolute-value circuit as well as nonlinear loading of the summing resistors (as diodes switch off and on), by using fast-recovery low-capacitance diodes, and by matching the two absolute-value circuit diodes for equal forward-voltage drops $\pm$ 0.5 mv at 2 ma of forward current to make the output of the absolute-value circuit for positive and negative $(X \pm Y)$ very nearly the same. With these precautions, the absolute-value circuit probably contributes very little to the total error.

The summing resistors were also matched $\pm$ 0.01 per cent, so that summing error probably contributes little to the total error also. The primary source of error then is the piecewise linear approximation to a squaring curve.

Fig. 7. (a) shows a "positive" diode limiter channel and its transfer characteristic. Similarly, (b) shows a "negative" limiter channel. Only positive slopes are possible with passive elements. Three diodes are shown in each channel. If these were ideal diodes, any one of the three would suffice; with practical diodes, however, a combination of shunt and series limiting can greatly reduce effects of diode capacitance. D_1 (called a "catching" diode) and D_3 perform shunt limiting, and D_2 performs series limiting. As shown in Fig. 9, with $R_1 > R_3$, as in each multiplier channel, then catching diode D_1 used with D_2 reduces the effect of diode capacitance more than D_3 with D_2. In the multiplier the catching diode D_1 with D_2 gave approximately one octave higher frequency for a given error than D_3 and D_2 (which agrees with the fact that in each limiter channel $R_1 \simeq 2R_3$, see Fig. 9). The improvement obtained with all three diodes did not justify the added expense; but a single diode was markedly inferior to a pair of diodes. The breakpoints and slopes are indicated on the figure. The slope is the conductance of one side of the "delta" which is equivalent to the "wye" formed by R_1, R_2, and R_3. The breakpoint is that value of V_{in} for which the voltage across the catching diode D_1 is zero. If R_3 is set equal to zero, the slope reduces to $1/R_1$. R_1 could be chosen for the proper slope, and then R_2 chosen for the proper breakpoint, so that R_3 is not required at all for the circuit function; however, R_3 permits the designer to adjust the slope without affecting the breakpoint.


V_{in}
R_1
D_1
D_2
R_2
D_3
R_3
i out
i out
$R_2/(R_1R_2 + R_2R_3 + R_3R_1)$
V_{in}
(R_1E/R_2)

(a)


V_{in}
R_1
D_1
D_2
R_2
D_3
R_3
i out
i out
$-(R_1E/R_2)$
V_{in}
$R_2/(R_1R_2 + R_2R_3 + R_3R_1)$

(b)

Fig. 7

Fig. 8. The error in an exactly piecewise linear approximation to a square-law characteristic has the appearance of a series of parabolic segments. The maximum absolute error is $E_s = 12.5/n^2$ per cent of half-scale, where n is the number of segments per quadrant in the approximation.

Fig. 9. The effectiveness of a catching diode D_1 with a series diode D_2 as compared to a shunt diode D_3 with D_2 in reducing the effects of diode capacitance depends on the relative size of the resistors R_1 and R_3. The back impedance (or impedance of a reverse biased diode) is symbolized by r_b, while the forward impedance is symbolized by r_f. The equivalent circuits for the channel-off state are shown (for D_1 and D_2 and for D_3 and D_2 in (a) and (b) respectively). The transfer impedance of the two "T" networks may be written immediately by inspection using the "Y" to "Δ" transformation and taking the 1-2 side. In (a), $Z_{12} = (R_1 r_f + R_1(r_b + R_3) + r_f(r_b + R_3))/r_f \approx R_1 r_b/r_f$ when $r_b \gg \max(R_1, R_3)$ and $r_f \ll \min(R_1, R_3)$. Similarly, in (b), $Z_{12} \approx R_3 r_b/r_f$. Thus, the transfer impedances are approximately equal for $R_1 = R_3$; but for $R_1 > R_3$ as in the multiplier, the catching diode in (a) gives higher transfer impedance. In each channel of the multiplier $R_1 \approx 2R_3$, and it was found experimentally that approximately one octave higher frequency for a given error was possible in the multiplier with catching diodes than with the other shunt diodes, which shows that r_b acts like a capacitance.

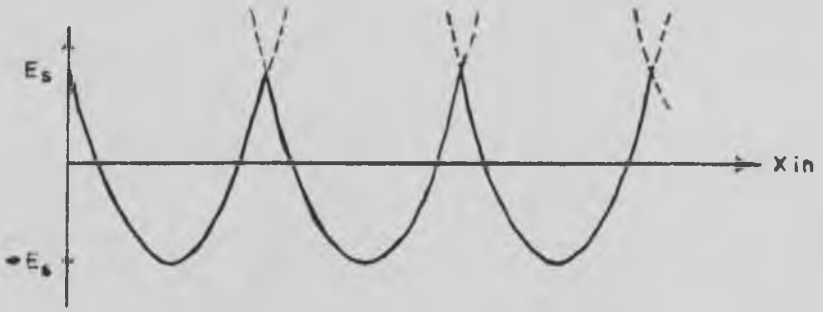
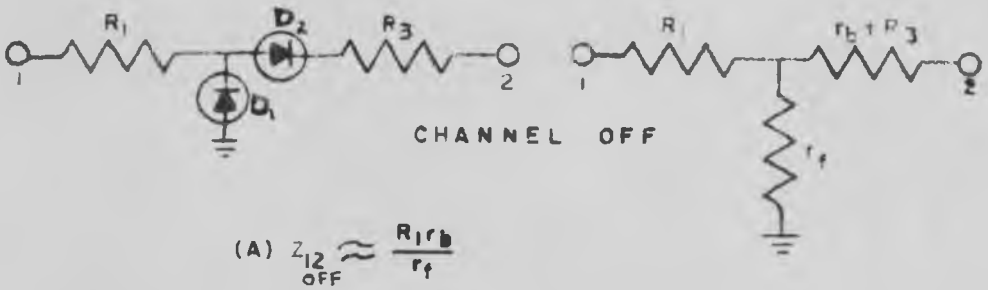
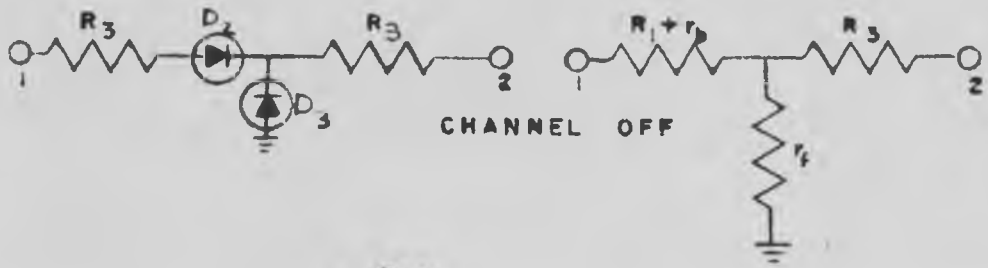


Fig. 8



(A) $Z_{12}{}_{OFF} \approx \frac{R_1 r_b}{r_f}$

(a)



(B) $Z_{12}{}_{OFF} \approx \frac{R_3 r_b}{r_f}$

(b)

Fig. 9

The Diode Squaring Circuits

Figure 7 illustrates the operation of the basic diode-limiter circuit. The transfer characteristic shows zero output current for input voltages smaller than the "breakpoint" voltage V_{bp}. For input voltages greater than V_{bp}, the channel switches "on" and produces positive output current which increases linearly with the input voltage. The rate of increase (slope or transfer admittance) can be specified independently of the breakpoint. The channel with the nonzero part of its transfer characteristic in the first quandrant for positive output current will be called a "positive" channel; reversal of diodes and bias polarity yields a "negative" channel.

When several positive channels are driven by the same input and their output currents are summed at the summing junction of an operational amplifier, their composite transfer characteristic can be made to approximate the first quadrant of a square-law characteristic. If several negative channels are connected in parallel, a 3rd quadrant "square-law" characteristic can be obtained.

Figure 8 illustrates the error due to polygonal approximation of a square-law characteristic. It can be shown that the maximum absolute error will be smallest if the breakpoints are equally spaced, the slope increases by an equal amount at each breakpoint except the origin, and the slope of the first segment at the origin equals one-half the increment in slope at subsequent breakpoints.

The error then is the series of parabolic segments shown, and the maximum absolute error is

$$E_s = (12.5/n^2) \text{ per cent of half-scale} \quad (3)$$

where n is the number of approximating segments per quadrant. The error in the multiplier will be twice this or

$$E_{multiplier} = (25/n^2) \text{ per cent of half-scale} \quad (4)$$

In low impedance $\pm$10 v circuits the variation in diode conductance is more significant than in high-impedance $\pm$100 v circuits. Although this effect makes analytical design more difficult, it also permits "diode rounding" to approximately double the accuracy; the measured maximum absolute error was approximately one-half of that given by Eq. (4).

Increasing the number of the segments per quadrant in the piecewise-linear approximation to a square-law characteristic will not increase the accuracy past a certain point determined by the component tolerances. Since very accurate resistors and selected diodes would have been prohibitively expensive, trimming potentiometers were used to make the bias resistors variable by about 10 per cent, which permitted $\pm$0.05 per cent of half scale squaring accuracy (at 25 deg C) using 1 per cent and 5 per cent resistors, and unmatched diodes in the squaring network. The slopes as well as the breakpoints were considered for adjustment, but breakpoint adjustment is superior, for normal manufacturing variations from diode to diode cause variations in

the breakpoints. Breakpoint adjustments permit diode variations to be "adjusted out". Variations in the slopes, on the otherhand, are caused by resistance variation, and the tolerance of the resistors can readily be made as small as necessary for repeatable results. It was found that with adjustable breakpoints the tolerance of the slopes could be rather large. The combination of 1 per cent and 5 per cent resistors used (stock values) gave a net slope tolerance of about 3 per cent. On several of the fourteen squaring circuits which have been built, one or two of the resistors in series with trim pots had to be changed to a higher or lower value in order to change the range of adjustment slightly. A smaller tolerance on the "slope adjusting" resistor R_3 would avoid this difficulty; but the change required was obvious and easily made when the circuit was adjusted. The slope adjusting resistor, R_3, is illustrated in Figs. 7 and 9.

Use of Catching Diodes

As shown in Fig. 9, with $R_1 \gg R_3$, as in the multiplier, the catching diode D_1 with D_2 is superior to D_3 and D_2 in improving the frequency response. Besides improving the frequency response, the catching diodes D_1 also reduce the mutual interaction of the breakpoint adjustments, and this results in a simpler adjustment procedure. In addition, the catching diodes present a more constant load to the absolute-value circuits as limiter diodes switch off and on.

It is interesting to note that shunt diodes did not seem to improve the operation of the absolute-value circuits.

Fig. 10. Twice the curvature (caused by "diode rounding" as the diodes turn on) at the origin where the increment in slope is one-half the increment in slope at later breakpoints improves the accuracy by the same amount as the diode rounding at the later breakpoints. This is a bonus provided by the cascading of a diode in the absolute-value circuit and one in the first limiter channel which turn on together.

Fig. 11. The 100 pf capacitor shown is optimum for the circuit shown for extending the 0.5 per cent of half-scale error frequency of an inverter (similar to Burr Brown 1607A) by one decade (from approximately 30 Kc to 300 Kc). This would be an especially suitable way to phase compensate an amplifier with a complicated summing network. The shunt capacitor adds phase lead to compensate for the normal phase lag of the amplifier.

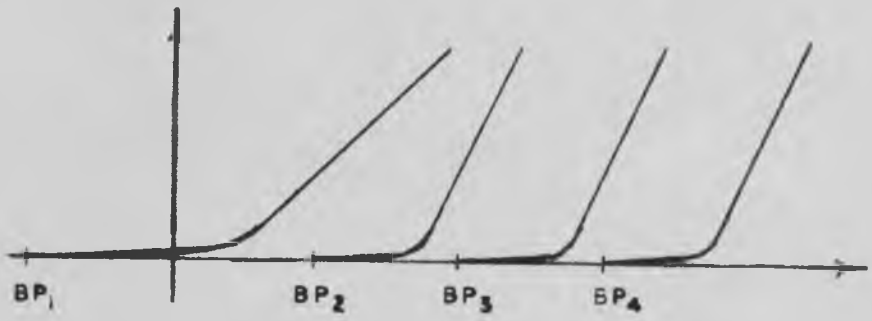


Fig. 10

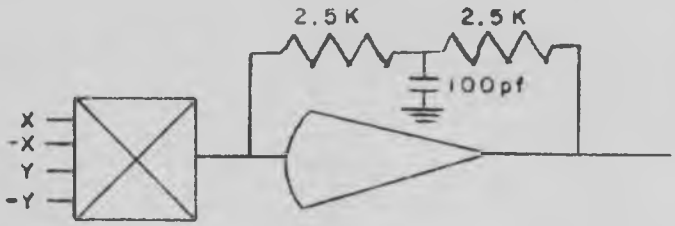


Fig. 11

Improvement of Accuracy Near Zero

Figure 10 shows that two diodes in series (one in the absolute-value circuit and one in the first limiter channel) turning on together at the origin were required to improve the accuracy by the same amount as one diode turning on at other breakpoints.

Slight forward biasing of the absolute-value circuit diodes for zero input was required for high accuracy near zero. Optimum forward bias was about 0.100 volts. In addition, the first two limiter channels were slightly forward biased for zero input. This resulted in canceling $\pm$3 mv d.c. offsets from the two squaring circuits.

Choice of Diode Type

Selection of diode type was based on observation of the rectification of a 300 kilocycle sine wave, and on a survey of diode specifications vs. cost. To multiply accurately at 100 Kc the squaring circuits would have to generate accurate 200 Kc sine waves. Both inexpensive low-conductance diodes and expensive high-conductance diodes were tried. It was found that they had similar characteristics near the origin (forward currents less than 0.2 ma) so that inexpensive low-conductance diodes perform nearly as well as high-conductance ones. Substitution of different diode types, including germanium diodes, for the catching diode did not change the circuit performance.

The type of diode chosen was the IN4009 type, which is an inexpensively available high-quality silicon junction diode intended for the Skybolt program. D.A.T.A. Semiconductor and SCR Tabulation gives its

recovery time as 4 nanoseconds and its capacitance as 4 picofarads. The limiting factor in its performance is its capacitance. Diodes with lower capacitance are available, but smaller capacitance is obtained by a smaller junction crossection which results in greater thermal drift. The 1N4009's are particularly resistanct to heat damage.* (1N4009's are approximately 33 cents each in lots of 100.)

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*The writer held a 25 watt Ungar soldering iron immersed in a drop of solder about the lead (for good thermal contact) against the glass at one end of the diode while observing the voltage drop at 2 ma forward current. After several minutes the voltage drop reached a new steady state value. Both the anode and the cathode were so treated in an attempt to alter the room-temperature characteristic slightly. The diode was not damaged, and its room-temperature characteristic was not altered ($\pm$0.5 mv). Three diodes were tested in this manner and all three results were the same.

Temperature-drift Compensation

The forward voltage required to turn a junction diode on decreases with increasing temperature. This makes each diode limiter channel turn on sooner at higher temperatures which results in a severe drift in the composite characteristic. In the uncompensated circuit for a temperature increase of 30 degrees C each limiter channel turned on 20 mv too soon; after the 10th channel had turned on the total drift error was 200 mv. Temperature stabilization was achieved by placing diodes in the bias lines. When the temperature increases, these diodes produce less drop in the bias line, so the bias increases and compensates for the tendency of the series diodes to turn on sooner. The temperature compensation was designed empirically on one squaring circuit and found to work equally well on a second squaring network without special matching of thermal characteristics. Since the temperature compensation required diodes in the reverse bias lines, and since the first two diode-limiter channels were slightly forward biased in order to get the required accuracy near zero, offsetting positive and negative bias voltages were applied to these two channels to simultaneously obtain temperature stabilization and net forward bias.

Frequency-Response Equalization

A 15 PF lead capacitor from the output of the absolute-value circuit to the network's output (to a summing junction) reduced the multiplier phase error, but caused amplitude error with increasing frequency. A roll-off network consisting of another capacitor and a resistor in series connected from the absolute-value circuit output to

ground corrected this amplitude error to about 100 kilocycles. Capacitors across resistors in the individual diode limiters were tried, but were not as effective. Phase shift measured with different amplifiers was not exactly the same. Hence a compromise phase compensation was used, and typical error is given in table 1.

An alternate and possibly better method of compensation would be to split the 5K feedback resistor into two 2.5 K resistors with a 100 picofarad shunt capacitor to ground between them (Fig. 11). This extends the 0.5 per cent of half scale phase-shift-error frequency for an inverter (similar to Burr Brown 1607A) by approximately one decade.

Tables 2 and 3 give a summary of the design criteria for high static-accuracy and high-frequency performance.

TABLE 2 REQUIREMENTS FOR HIGH-FREQUENCY PERFORMANCE

1. Effects of stray capacitance were minimized by using low impedance levels.

2. Diodes with low capacitance and fast turn-off time were used (1N4009's).

3. Catching diodes to reduce the effects of diode capacitance were used.

4. The frequency response of the completed multiplier was improved by adding phase lead to compensate for phase lag in the output amplifier.

5. Completely parallel limiter channels were used. These are less likely to cause phase shift than a series-parallel scheme.

TABLE 3 REQUIREMENTS FOR HIGH STATIC ACCURACY

1. The four summing resistors for each squaring circuit were matched to within 0.01 per cent.

2. The absolute-value circuit diodes were matched for equal forward voltage drops $\pm$0.5 millivolts at 2 milliamperes of forward current.

3. The absolute-value circuit diodes were slightly forward biased for zero input.

4. Ten segments were used for each squaring circuit, i.e., ten parallel limiter channels were used.

5. Potentiometer adjustments of the breakpoints to compensate for component tolerances were used.

6. Diodes were placed in the bias lines for temperature stabilization.

7. For drift-free zero error at zero it is best to have all channels with an "off" diode in the series path at zero. This prevents slight errors in the reference voltages from causing error at zero.

8. A diode was placed in the first limiter channel so that the rounding of its characteristic improved the accuracy near zero.

9. The squaring circuits were designed and adjusted as a unit, so the overall transfer characteristic takes into consideration nonlinearities in the absolute-value circuit and nonlinear loading of the summing resistors.

Chapter 3

ADJUSTMENT AND TESTS

Breakpoint Adjustment

Four methods for accurate breakpoint adjustment were investigated. Iterative d.c. adjustment was used for adjusting the first squaring circuit, but it was too laborious for repeated use. A matching method was used to adjust all squaring circuits except the first (14 were adjusted). In this method the circuit being adjusted is matched to another accurate square-law characteristic by subtracting the outputs of both circuits. The two remaining methods use a "slow" analog computer and a repetitive analog computer respectively. A ramp $Y = kt$ is generated to drive the squaring network and a square $Y^2 = (kt)^2/10$ is generated and compared with the output of the squaring network to produce an error display. It was found difficult to obtain the desired accuracy by this method.[3]

As a fifth method, an attempt was made to adjust an entire multiplier so that it multiplied 10 sin ωt accurately by both 10 and -10 volts. It was found that this usually results in a badly misadjusted multiplier, which multiplies accurately only by 10 and -10.

Adjustments which are sometimes included in analog multipliers (a d.c. adjustment, an X adjustment, a Y adjustment, and a gain adjustment) were not found necessary, although a gain adjustment was included which trims the 5K feedback resistor of the output amplifier.

In the iterative d.c. adjustment method, the output of a squaring network is conducted to the summing junction of an operational amplifier which has an accurate 5K feedback resistor. The input voltage to this squaring network is then set equal to X = Y = 1.000, 2.000, 3.000, ..., 10.000 volts consecutively, and the network's breakpoints are adjusted consecutively for -0.100, -0.400, -0.900, ..., -10.000 volts out of the amplifier. One breakpoint is adjusted for each input. For example, with 5.000 v in, the 5th breakpoint is adjusted for -2.500 volts out. Interaction between the breakpoints requires this sequential adjustment to be made many times before the characteristic converges for ± 5 mv accuracy. Also, about -3 mv of d.c. offset was cancelled by another source (through a 5K summing resistor). Because of the large number of iterations required, this method should be avoided if possible.

The most satisfactory method is to match a new multiplier to one that is already accurately adjusted. A complete multiplier can be adjusted in this manner in about 15 minutes. Setting the input to the new multiplier for $X = Y = 10 \sin \omega t$ and $-X = -Y = -10 \sin \omega t$ (for $f \approx 40$ cps), then the output, $-10 \sin^2 \omega t$, will be generated entirely by its "positive" circuit. (In the "negative" circuit, the inputs will sum to zero at the summing resistors). Setting the input to the reference multiplier equal to $X = -Y = 10 \sin \omega t$ and $-X = Y = -10 \sin \omega t$, its output, $10^{-2} \sin \omega t$, will be generated by its negative circuit. The outputs of the two multiplier networks can be summed at the same summing junction and should cancel. The breakpoints of the positive circuit

of the new multiplier are then adjusted for minimum error. The negative network is next adjusted by interchanging the Y and -Y inputs to the two multiplier networks. In practice, it was possible to match the squaring networks within ±5 mv and typically to ±2 mv.

Tests and Results

The multiplier was tested for static accuracy, thermal drift, and frequency response. Full scale sine waves of various frequencies were multiplied by positive and negative constants and also zero. The multiplier output was then summed with an appropriate input to produce an error display. It was found that the static accuracy was approximately ±10 mv at 25 deg C. Also, multiplier error caused by misadjustment of the ±10 v reference supplies was approximately equal to this adjustment error. Error photographs (Fig. 3) show the error at various frequencies (1 Kc, 5 Kc, and 10 Kc) for $XY/10 = (10)(10 \sin \omega t)/10$. The phase compensation approximately doubled the 0.5 per cent of half-scale error frequency extending it to over 10 Kc. Table 1 shows the dynamic error at various frequencies. This error is caused by a combination of phase shift in the amplifiers and non-linear error in the squaring networks.

Discussion

Referring to the measured specifications of Table 1, the multiplier seems to work well; its frequency response is acceptable for ASTRAC II. Static accuracy and the temperature compensation used were entirely satisfactory. However, the temperature

stabilization by the diodes in the bias networks makes it incorrect to vary the reference voltages to obtain a variable denominator in XY/V. The multiplier can be built and aligned by a reasonably experienced technician (undergraduate engineering student) in about 20 working hours. The cost for components is about $90 per multiplier, the major part of this cost being $60 for trimmer potentiometers. The adjustment of the multiplier is easy, once one properly adjusted squaring circuit is available for matching. With a convenient setup, it takes about 15 minutes per multiplier.

As to possible improvements, as a price of the low-impedance wideband design, the multiplier can draw up to 17 ma from each driving amplifier because the summing resistors are so small. It is suggested that 2K summing resistors would probably be satisfactory and would reduce the loading on the driving amplifiers to about 7.5 ma maximum. The use of 2K summing resistors would give approximately a 5 volt swing out of the absolute-value circuit. (The maximum voltage out of the absolute-value circuit at present is approximately 7.5 volts.) With a 5 volt swing the breakpoint spacing would be 0.5 volts. This 0.5 volt spacing would result in an increased overlapping of the breakpoint adjustments. In the writer's opinion, such overlapping might be about optimum for accurate curve fitting, although it would make the circuit more sensitive to thermal drift and more difficult to adjust.

A second disadvantage is the use of 20 trimmer potentiometers. These are the most expensive and bulky components in the circuit. If the circuit were constructed with all 1 per cent resistors, perhaps

adjustment of fewer breakpoints would be possible. Since only seven multipliers were built, however, it was not deemed worthwhile ordering special resistors for this purpose.

Finally, the method used for phase compensation was probably not as good as splitting the feedback resistor with a capacitor to ground (Fig. 11).

If the ultimate in high frequency performance were desired, however, four separate squaring circuits would be better than the absolute-value squaring circuits, which have cascaded phase shifts from summing resistors, absolute-value circuits, and limiter channels. On the otherhand, the frequency response of the squaring circuits was comparable to that of the amplifiers used.

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