A NEW COLOR-TELEVISION GRAPH PLOTTER FOR DIGITAL COMPUTERS

by

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ABSTRACT

The color-television graph plotter described is an inexpensive and convenient display system for a digital computer. Display output is presented on a standard color television monitor, which completely eliminates the need for digital to analog converters and the difficulties associated with using them to supply analog positioning voltages. Four single-valued functions of 235 points each and an internally generated coordinate net may be displayed while maintaining an acceptable repetition rate of 30 displays per second. The colors of each graph, the coordinate net, and the background are under control of the digital computer program. Red, green, and blue and combinations of these colors are available. Eight bit resolution is provided but may easily be expanded to nine bits. Although the graph plotter described is for use with a Digital Equipment Corporation PDP-9 computer, it may readily be adapted to other digital computers. The graph plotter can be interfaced to computers with word lengths as small as 8 bits; the only requirement being that the computer have some type of automatic data-channel input-output transfer mechanism.

CHAPTER 1

INTRODUCTION

The color-television graph plotter described herein was constructed at The University of Arizona's Computer Science Research Laboratory as a convenient and inexpensive peripheral device for a Digital Equipment Corporation PDP-9 computer. The graph plotter provides a color display of from one to four single-valued functions on a standard color television monitor. The resolution of the Y coordinate is eight bits and may easily be expanded to nine bits. Approximately 235 X coordinate values are available; this limit is determined by the number of unblanked television lines in one field. A hardware graticule generator permits display of a coordinate grid under program control. The program may also select the color of each of the four traces, the graticule, and the background. The colors red, blue, and green and all combinations of them are available. The digital logic implementation of the color graph plotter is similar to the all-analog logic of a B-scan analog-computer display (Korn and Korn, 1964).

Total cost of the logic necessary to construct this unit and interface it to the Digital Equipment Corporation PDP-9 was approximately $700.00. This figure can probably be halved when interfacing to a computer with a DTL/TTL compatible I/O bus, like the Digital Equipment Corporation PDP-15 or PDP-8I. Additional expenses include power supplies and the color television monitor. A standard color television

receiver could be modified for use with this display system, while a commercial color monitor is currently available for $775.00.

Outstanding features of the color graph plotter are simplicity of design and operation as well as inexpensive construction. These features are chiefly a result of using a standard color television monitor for an output device. Conversion of position coordinates to brightening pulses at appropriate times completely eliminates the need for digital to analog converters. The display shares the digital-computer memory via a standard data channel, so that no refresher memory is needed. Figure 1 shows a typical display.

Operation

The scanning direction of a standard television monitor was rotated 90 degrees, with an individual scanning line beginning at the bottom of the screen and ending at the top. Each television field is then scanned from left to right; each scanning line represents an X coordinate value of the plot. To plot a point (X,Y), the screen is brightened when the scanning line corresponding to the X coordinate reaches a vertical position proportional to the Y coordinate. The exact time at which brightening occurs is determined by Y coordinate information obtained from the computer through automatic data-channel transfers synchronized with the scanning rate of the television monitor.

Figure 2 is a simplified block diagram showing how coordinate information is processed. Data extracted from the computer at the beginning of each scanning line is compared to the state of a counter which counts from zero to 377_8 as each line goes from the bottom of the

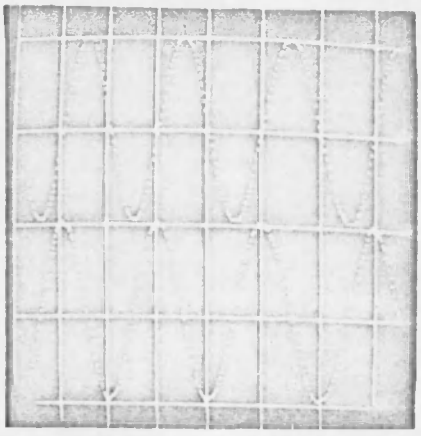

Figure 1. Display Output

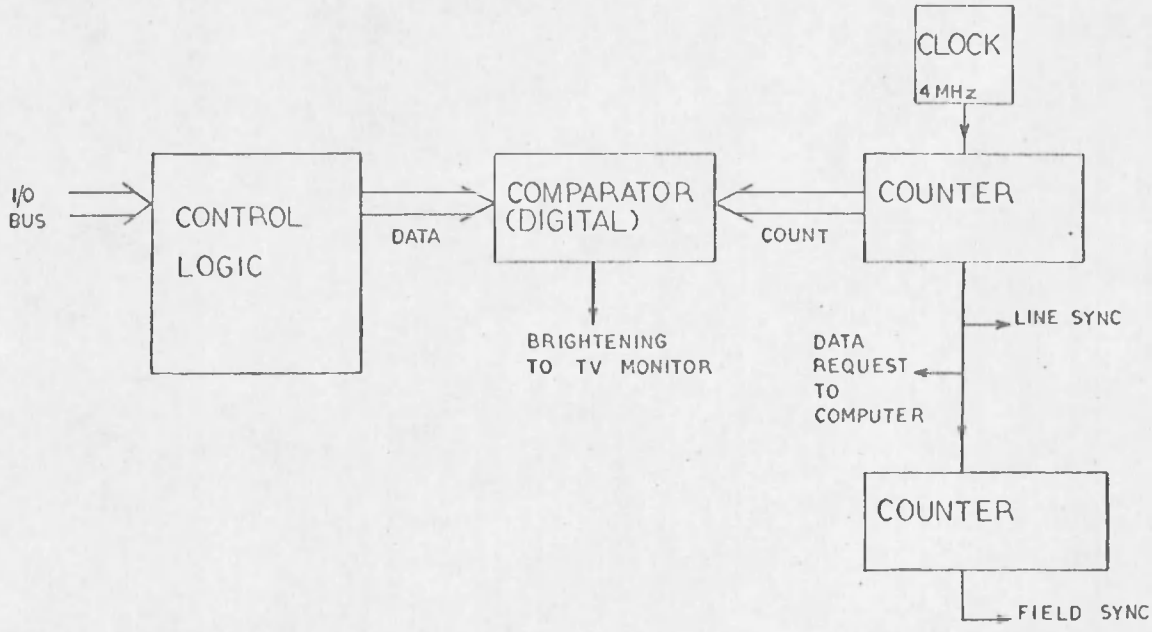

Figure 2. Simplified Block Diagram

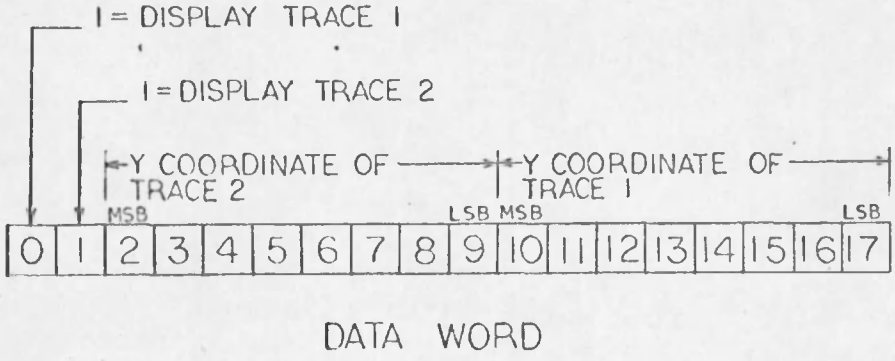

Figure 3. Data Format

screen to the top and then produces a line sync pulse. When the counter state is identical to the Y coordinate data, a brightening pulse is produced. A second counter is used to count lines and to produce sync pulses at the field rate.

Actually, two points may be brightened in each line. The Y coordinates for two points on two individual graphs and brightening information for these points are extracted from a single 18 bit memory location in the computer. An internally generated graticule (coordinate net) may also be displayed.

Color selection is accomplished by switching the various brightening signals to the appropriate color inputs of the television monitor. The primary colors, red, green, and blue, and combinations of them are available. The polarity of the brightening signal for any given color may be inverted to permit selection of a background color. All color information may be specified by the digital-computer program, which causes an input-output (IOT) instruction to set a special color register.

Data Channel Operation

To plot a single curve represented as an array $(X_1, Y_1)...(X_n,Y_n)$, it is necessary that the curve have equal X increments, that is, $X_{i+1}-X_i$ be a constant for $1 \leq i < n$. The array must be arranged in the digital computer memory in order of increasing X coordinate value. Once the array is arranged in the proper order, the X coordinates are no longer needed. The Y coordinates for the curve to be plotted must be in two's complement form and 8 bits in length. They are placed in

the least significant bits (bits 10-17) of each core memory location of the buffer. Bit 0 of each location in the buffer must be set to logical 1; this bit is tested by the display logic to determine whether the point is or is not to be displayed. Figure 3 shows the data format for the graphic display. After the data buffer has been set up, the program loads color information into the accumulator of the computer. One computer IOT instruction then loads the color register from the accumulator and starts the data channel.

As noted earlier, the display needs no refresher memory, but transfers data needed from the digital computer core memory using automatic data-channel transfers, a convenient feature of several small digital computers.

In the PDP-9 digital computer, each data-channel device has two sequential core memory locations associated with it in the digital computer memory. The first memory location serves as a word-count register. This is initialized to the two's complement of the number of data words to be transferred. It is incremented and tested for zero each time a data-channel transfer is made. The second core memory location serves as a current-address register. It is initialized to one less than the address of the first word of the data buffer to be transferred. The current-address register is incremented before each data-channel transfer and is used to establish the address of the next data word to be transferred. When the word-count register is incremented to zero, a signal is sent to the device's data-channel interface to halt its operation and cause a program interrupt advising the program that the buffer transfer has been completed. Detailed informa-

tion on the PDP-9 data channel is contained in the PDP-9 User Handbook (Digital Equipment Corporation, January, 1968).

Application

Two independently brightened points in each scanning line permit the plotting of two single-valued functions during each television field. Different buffers may be displayed on alternate fields, but a limit is set by the maximum flicker rate that can be tolerated. Multi-valued functions may be plotted if they are specially processed by the computer program. Actually, the plotting of multi-valued functions is more easily accomplished on conventional graphic displays: the main purpose of the color graph plotter is to display one to four single-valued functions.

The availability of brightening bits in the data word and the possibility of choosing different colors for each of the two sets of coordinate points makes possible various special effects, such as a plot consisting of alternately colored points.

Display Operation

A block diagram of the graphic plotter is shown in Figure 4. Typical operation proceeds as follows. The color register is first loaded from the accumulator, and the data channel enabled under program control. The data channel waits until the beginning of the next television field to request the first data word which it loads into the buffers. This data is transferred into the registers at the beginning of the next horizontal sync pulse. These are the points which will be displayed on the vertical scanning line about to begin. The unit

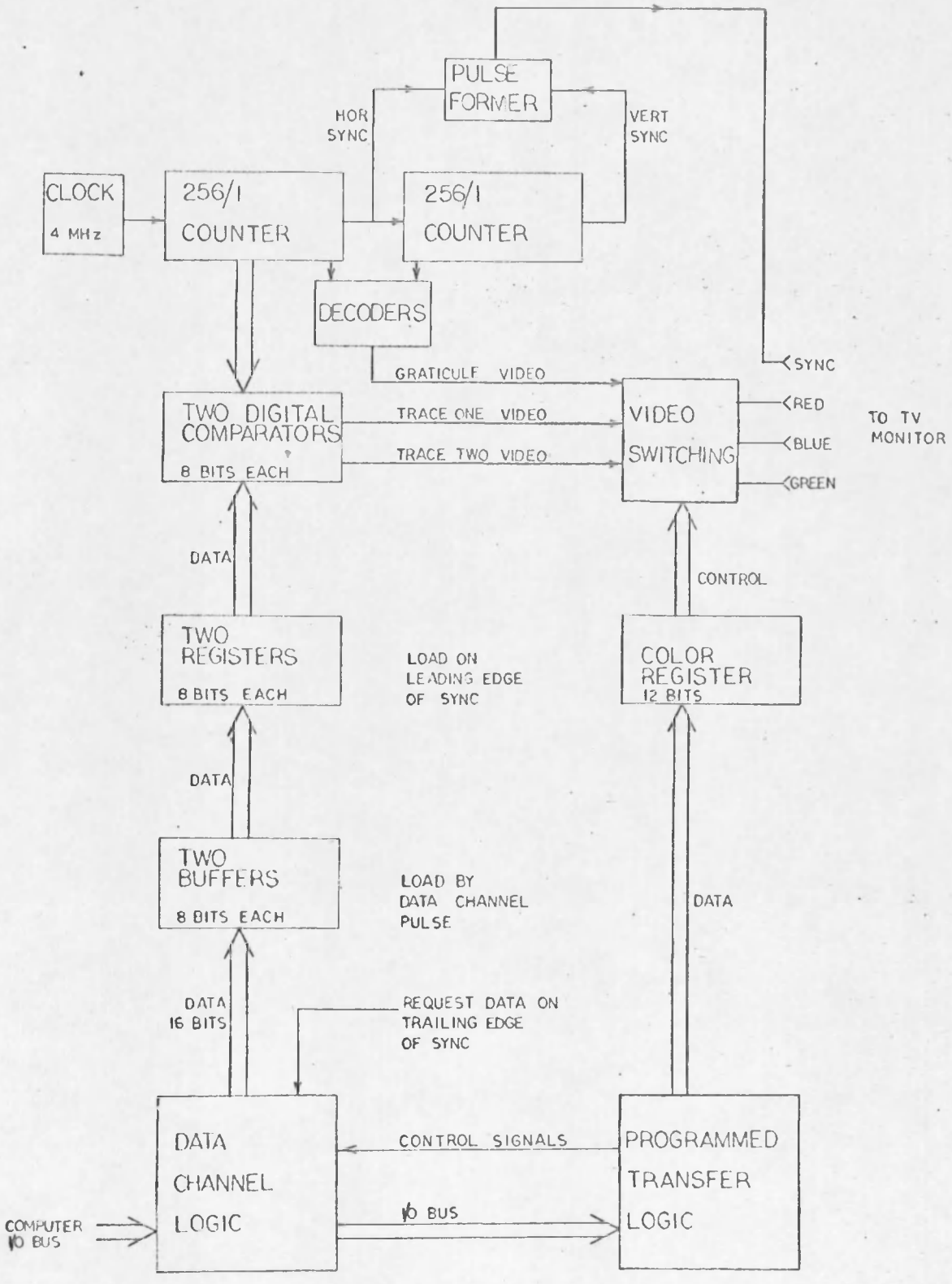

Figure 4. Block Diagram

immediately requests another data-channel cycle (at the trailing edge of the horizontal sync pulse) to insure that data for the next line will be available in the buffers when needed. In the Digital Equipment Corporation PDP-9 computer, data-channel requests may be delayed by direct-memory-access transfers, other data-channel requests with higher priority, program controlled input-output transfers, and certain long arithmetic instructions, so that requesting data one scanning line in advance insures its availability at the proper time.

The coordinates of two points in two's complement form and brightening information for these points are now stored in the data registers. The coordinate information is then compared to the state of a counter which counts up as each line progresses; the output of this counter also provides line sync for the television monitor. When the state of the counter is identical to the Y coordinate information, a brightening pulse corresponding to that coordinate point is produced. The brightening of one, the other, or both points may be inhibited by control bits in the data word. The brightening signals for each graph and the graticule are routed to the appropriate inputs of the color monitor to select the color of each plot, the graticule, and the background. Color selection is under control of a color register which, it will be recalled, was initialized by the computer program. When a data-channel buffer is completed, the computer automatically disables the graph-plotter data channel. This, in turn, causes the plotter to issue a program interrupt request to a service routine which initializes the data channel for the plot during the next television field.

CHAPTER 2

USER INFORMATION

Programming for the color graph plotter is relatively straightforward, but a special buffer format and certain timing restrictions are necessary. Detailed information on programming the PDP-9 input-output system is contained in the PDP-9 User Handbook (Digital Equipment Corporation, January, 1968).

Data Channel Operation

Each data channel has two locations in the digital computer memory associated with it. These serve as the word-count register and the current-address register. In the case of the color display, the word-count register is location 34_8 and the current-address register is location 35_8. The two's complement of the number of words to be transferred is placed in location 34_8. The maximum number of data words is 235_{10}, one word for each unblanked scanning line. One less than the address of the first data word to be transferred is placed in location 35_8. The display data channel is then enabled by an input-output instruction. At the beginning of the next television field following the execution of the enabling instruction, the data channel requests its first data word. The word-count register is first incremented. The current-address register is then incremented and the data word extracted from the incremented address in this register is transferred

to the color graph plotter. When the word-count register increments to zero, an overflow signal is sent to the plotter, the transfer in progress is completed, and the data channel is disabled. A program interrupt request is then made to let the computer initialize locations 34_8 and 35_8 and to enable the data channel again before the next television field begins. With a display of the maximum buffer length of 235_{10}, approximately one millisecond is available from the program interrupt to accomplish reinitialization. If, for some reason, the interrupt request is not serviced within one millisecond, the plotter will display one blank field. Approximately 17 milliseconds are available from the time of the program interrupt request to the beginning of the second television field.

Instruction Set

The instructions available to the programmer are listed in Table 1. The KDSF instruction is contained in a system program. When properly initialized, the operating system will pass control from a program interrupt from the color graph plotter to the programmer's service routine for the plotter. The format of the color register is shown in Table 2.

Data Format

The data format is shown in Table 2.3. The Y coordinates are given in two's complement notation. The zero of the Y coordinate is slightly below the center of the screen due to the time taken by the line retrace interval.

Table 1. Instruction Set

Mnemonic	Code	Function
KDSF	705601	Skip on Display Flag
KDCF	705602	Clear Display Flag
KDCH	705642	Clear Flag and Start Data Channel
KDCL	705622	Clear Flag and Load Color Register from Accumulator
KDAL	705662	Clear Flag, Start Data Channel, and Load Color Register

Table 2. Color Register Format

Accumulator Bit	Color	Function
6	Green	Background Color
7	Blue	Background Color
8	Red	Background Color
9	Green	Graticule Color
10	Blue	Graticule Color
11	Red	Graticule Color
12	Green	Trace 2 Color
13	Blue	Trace 2 Color
14	Red	Trace 2 Color
15	Green	Trace 1 Color
16	Blue	Trace 1 Color
17	Red	Trace 1 Color

Table 3. Data Format

Bit	Function
0	1 = trace 1 displayed
	0 = trace 1 blanked
1	1 = trace 2 displayed
	0 = trace 2 blanked
2-9	Y coordinate of trace 2
10-17	Y coordinate of trace 1

CHAPTER 3

DETAILED CIRCUIT DESCRIPTION

The color plotter was constructed to fit in a standard 19 inch rack cabinet. Interface to the PDP-9 computer was accomplished using compatible logic with levels of -3 volts (logical 1) and 0 volts (logical 0); other computers with I/O busses compatible with DTL/TTL integrated circuit logic may be interfaced even more easily. The location of this logic is shown in Figure 5. The location of a logic card is identified by a letter (row) and number (column). The pins are lettered. Thus, A5H refers to pin H of the R111 logic card in the first row and fifth column. The majority of the unit uses DTL integrated circuits mounted in carriages with six integrated circuits per carriage. The carriages mate with connectors whose pins are numbered from 1 to 88. Each connector is referenced by a letter. Thus, D58 is a pin (on connector D) of a MC 1812 integrated circuit.

If the level input of a DCD gate is at ground at least 400 nanoseconds prior to a -3 volt to 0 volt transition at the pulse input, the flip-flop will trigger. The output of the DTL latches follow the input (d) as long as the clock (c) is high.

The function of the W103 device selector logic card is to select the proper peripheral device and issue various control functions under control of an input-output instruction being executed by the computer.

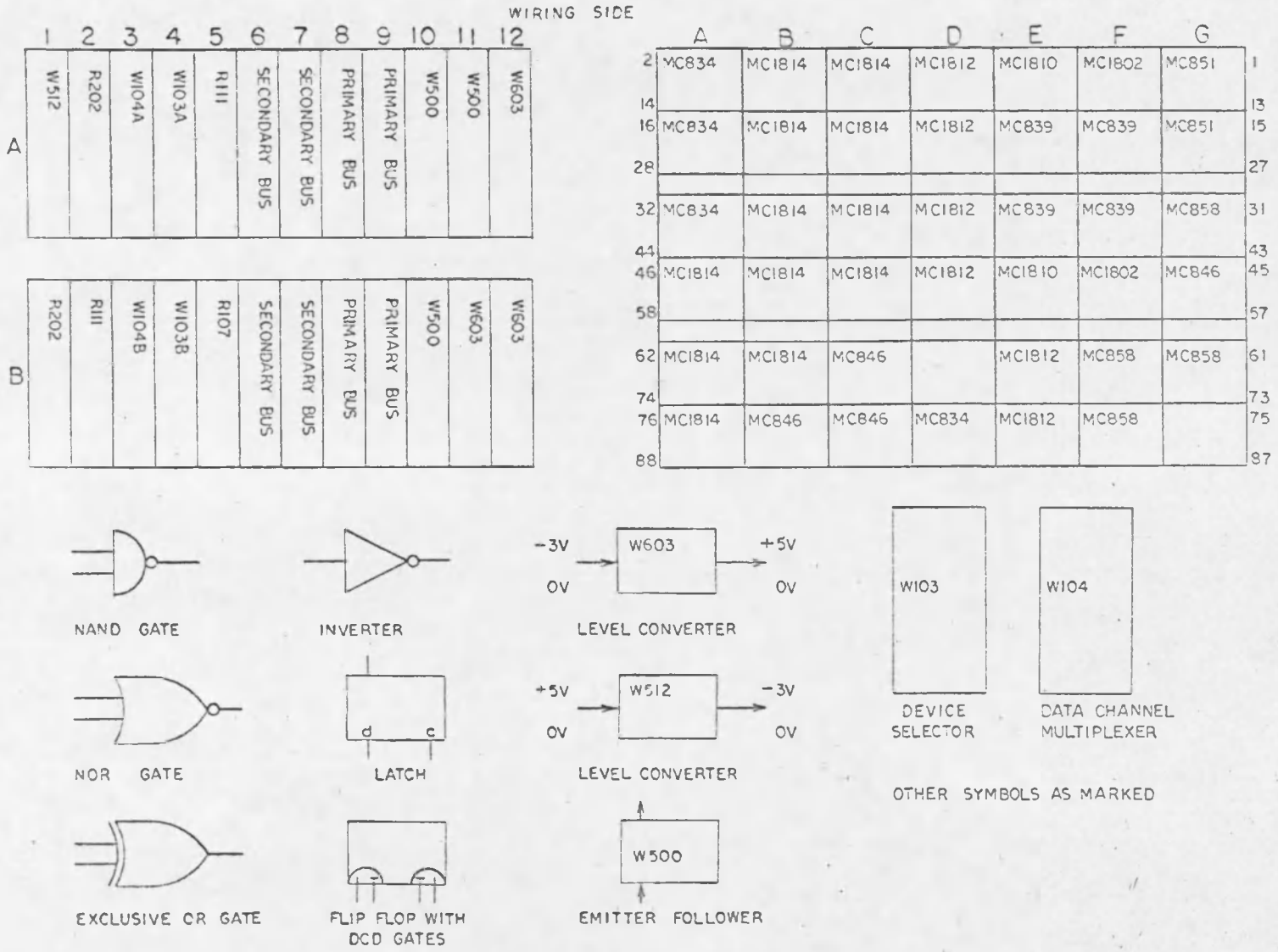

Figure 5. Layout and Logic Symbols

The W104 provides properly timed signals for data-channel operation and establishes a priority level for the peripheral's data channel. More detailed information on the PDP-9 input-output system is given in the PDP-9 Interface Manual (Digital Equipment Corporation, 1968).

Data Transfer

Unless otherwise noted, all signal references in this section are to Figure 6.

During execution of a KDCH or KDAL instruction, SD12 is at -3 volts and the IOT2 pulse is issued. This combination sets B1E. This, in turn, allows the trailing edge of VSYNC to set B1M at the beginning of the next television field. BSYNC has already set A2T. This forces B3S to ground causing the W104 to issue a synchronized RQ signal to the computer. GNT is issued by the computer when it is ready to accept the data request. GNT generates CLR FLG in the W104 which resets A2T. The computer increments the word-count and current-address registers and places the proper data on the I/O BUS lines. Because ENB1 of the W104 has pulled WR RQ to ground at A5H, IOP4 is issued. IOP4 becomes IOT4 in the W103 device selector which has been enabled by a ground SELECT level from the W104. IOT4 becomes IOD4 in Figure 10 and gates data on the I/O BUS into the buffers in Figures 7 and 8. PSYNC then gates the data into the registers at the end of the current scanning line. The trailing edge of BSYNC then sets A2T again to restart the whole cycle for the next data word. When the word-count register is incremented to zero, I/O OFLW causes B1E and B1M to reset to disable the data channel

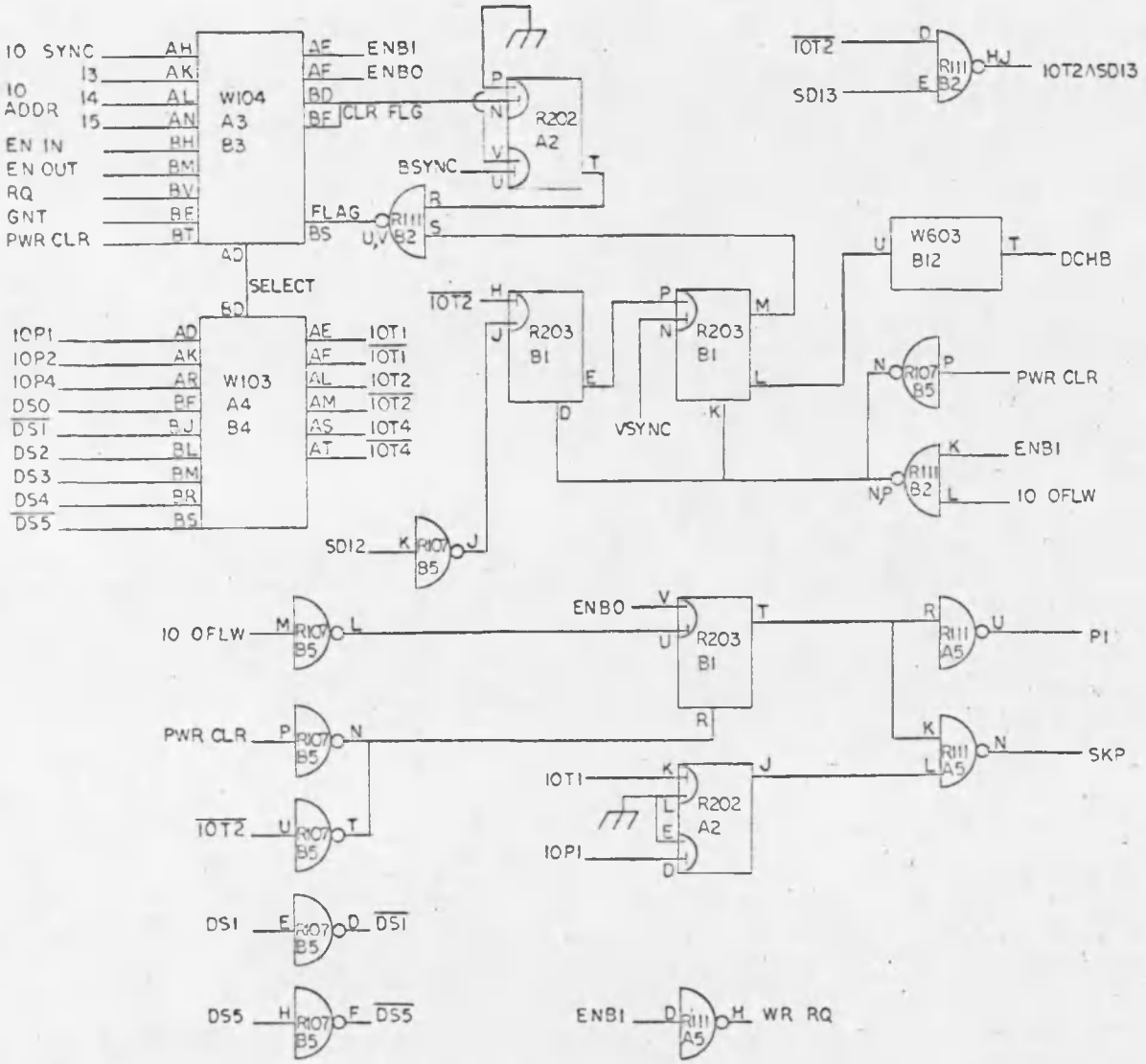

Figure 6. Control Logic

PIN V OF A12, B11, AND B12 IS CONNECTED TO 5V

ALL SUPPLIES ARE BYPASSED WITH .05 uf

EXTERNAL PULLUPS AND MONOSTABLE RESISTORS ARE BYPASSED WITH A SINGLE .33uf

ALL RESISTORS ARE $\frac{1}{4}$ WATT

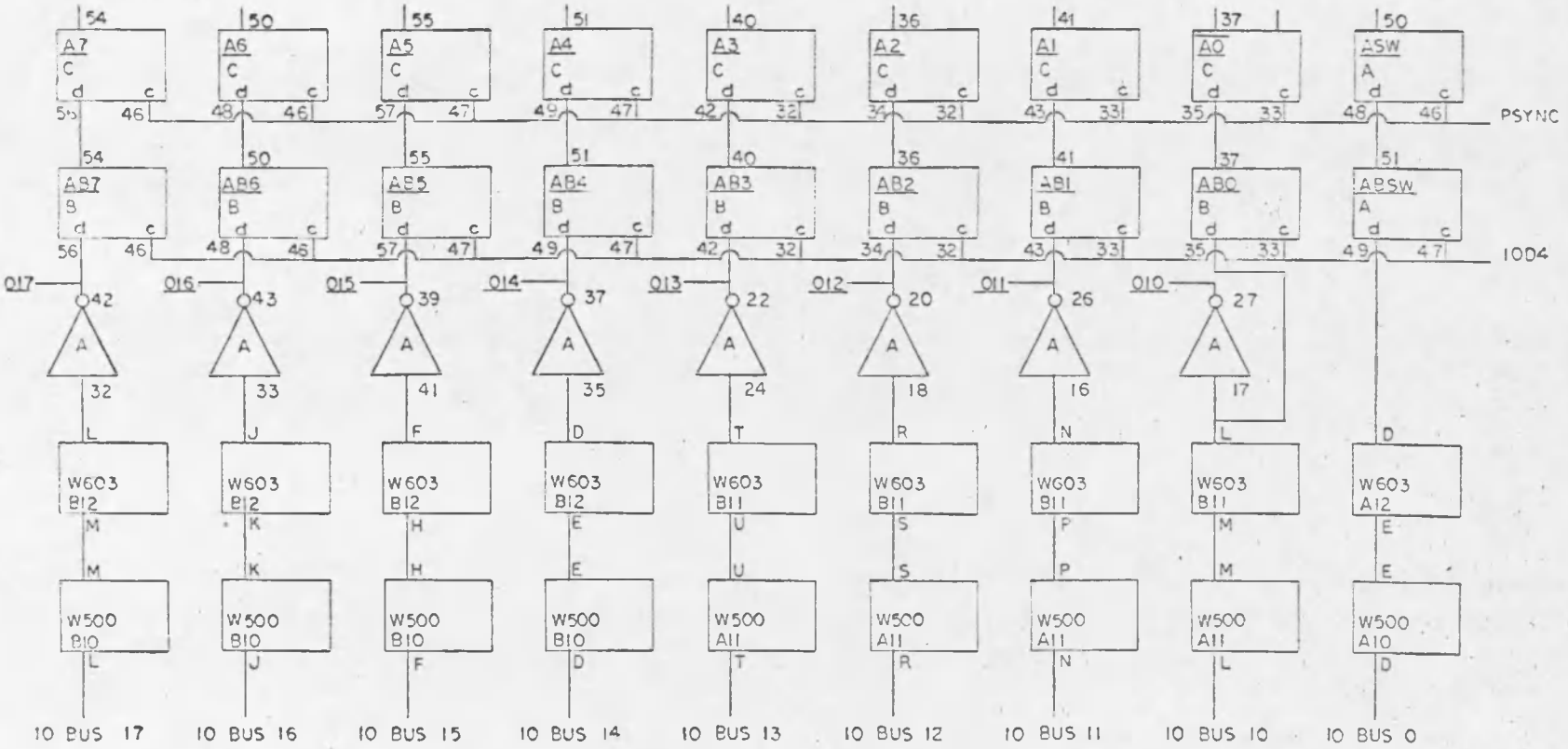

Figure 7. A Data Registers

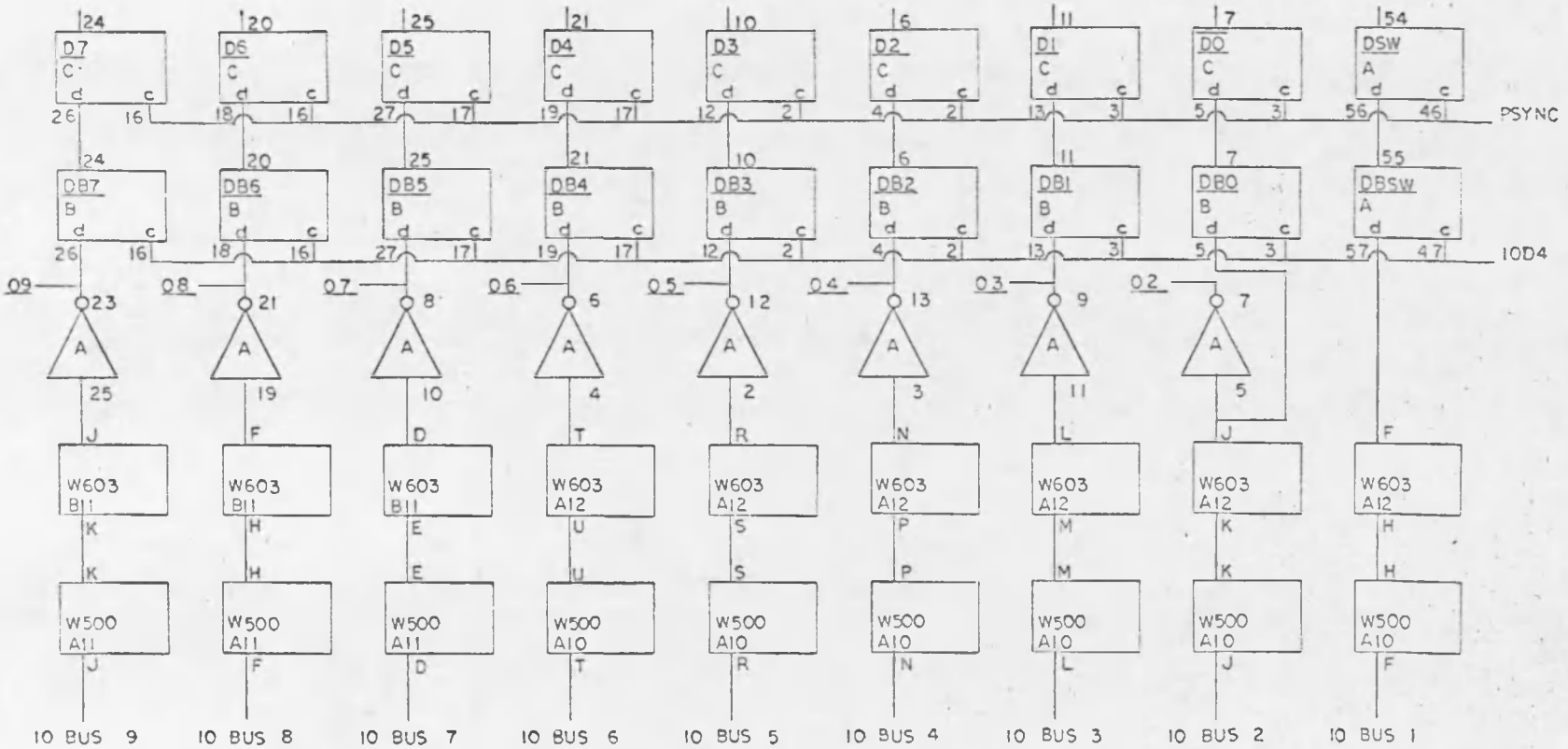

Figure 8. D Data Registers

and B1T is set to cause a program interrupt. The program interrupt flag can be tested by a KDSF instruction which issues IOT1 which sets A2J to ground the SKP line. This causes the computer to skip the next instruction. The trailing edge of IOP1 resets A2J one microsecond later. The flag may be reset by a KDCF, KDCH, KDCL, or KDAL instruction, all of which issue IOT2 which reset B1T.

The KDCL and KDAL instructions cause SD13 to be asserted and issue IOT2 which generates IOT2∧SD13 at B2H. This causes the color register to be loaded from the I/O BUS in Figure 10.

The PWR CLR pulse is issued when the computer is turned on, whenever the I/O reset key on the computer console is depressed, or during the execution of a CAF (Clear All Flags) instruction. It resets all three sections of B1 and initializes the W104.

Video Generation

Unless otherwise noted, all signal references in this section are to Figure 9.

The coordinate information in register A and register D is compared to the state of a 256:1 counter driven by a 4.032 MHz crystal oscillator. When the state of the counter matches the contents of register A, a positive going brightening pulse is produced at TAV. Similarly, coincidence with the D register produces a pulse at TDV. Note the comparator connection to the inverse of the most significant bit. This allows two's complement data to be used.

Television Synchronization and Graticule Generation

The output of the 256:1 counter mentioned above generates sync pulses at the line rate at G12 in Figure 10. It also drives another 256:1 counter which generates sync pulses at the field rate at G26. OVSYNC produces VSYNC at A1F to synchronize the start of a data-channel transfer sequence. It also generates VERT SYNC to synchronize the television monitor. OHSYNC similarly generates HOR SYNC to synchronize the television monitor. OHSYNC and OVSYNC are combined to produce PSYNC at G39 which is used to load the data registers during the blanking intervals. PSYNC generates BSYNC at A1D which is used to request data-channel cycles. PSYNC also generates SYNC which may be used as composite positive going blanking if the monitor requires such a signal.

Horizontal graticule lines are generated at the output of recognition gate F13. Vertical graticule lines are generated at F57. Combined they produce the graticule brightening signal GRATV at G57.

Video Switching

References in this section are to Figure 11 unless otherwise noted. The three video signals TAV, TDV and GRATV are routed to the various color outputs by the signals ARED, DRED, GRATRED, ABLUE, etc. at the gates on the left side of Figure 11. Graticule signals are not mixed with the other video signals at this time to permit analog mixing in an adjustable resistive network at the outputs to the monitor. The "exclusive or" gates controlled by BACKGREEN, BACKRED, and BACKBLUE permit reversal of video polarity in any one channel. This permits

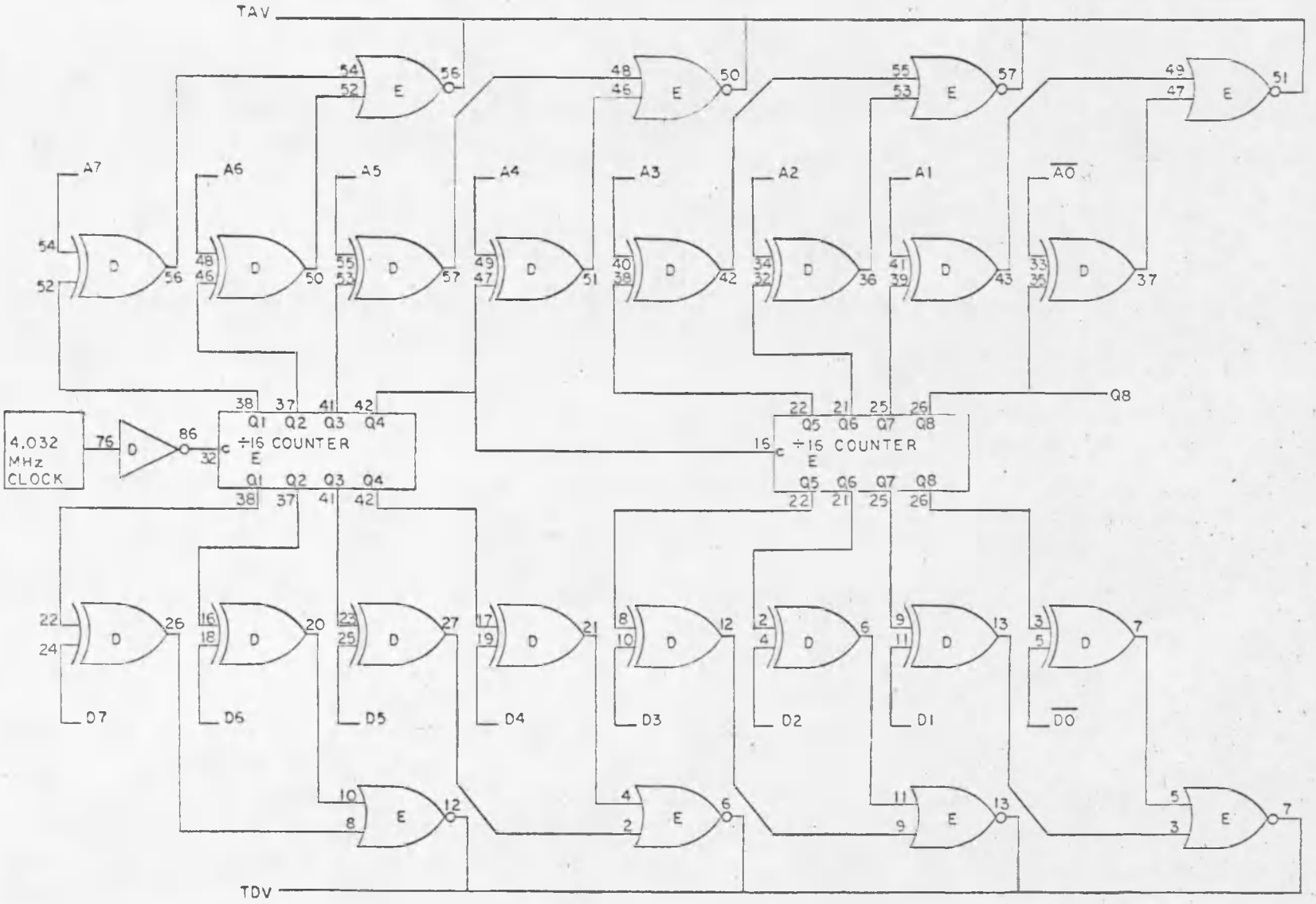

Figure 9. Comparators

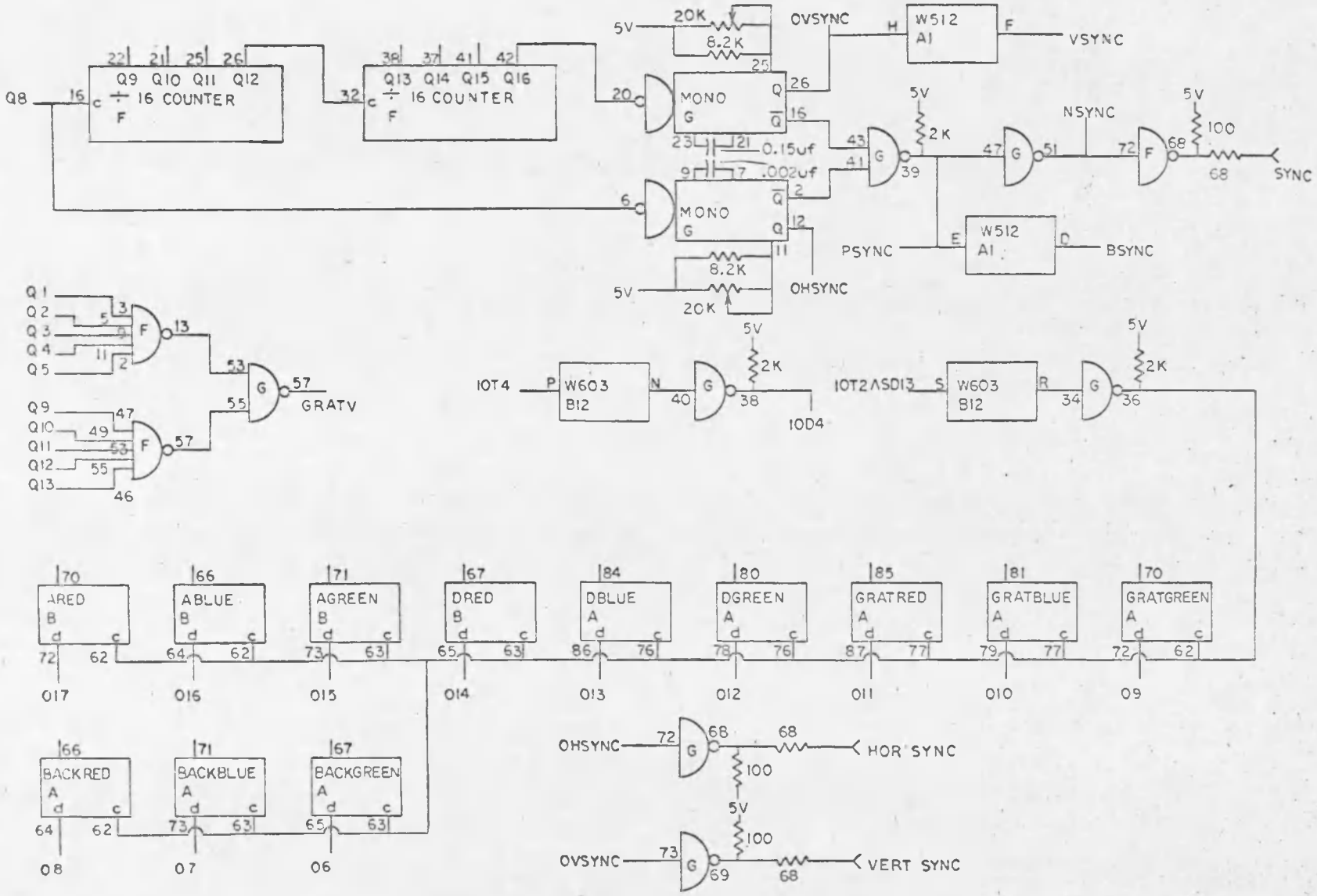

Figure 10. Synchronization and Graticule Logic

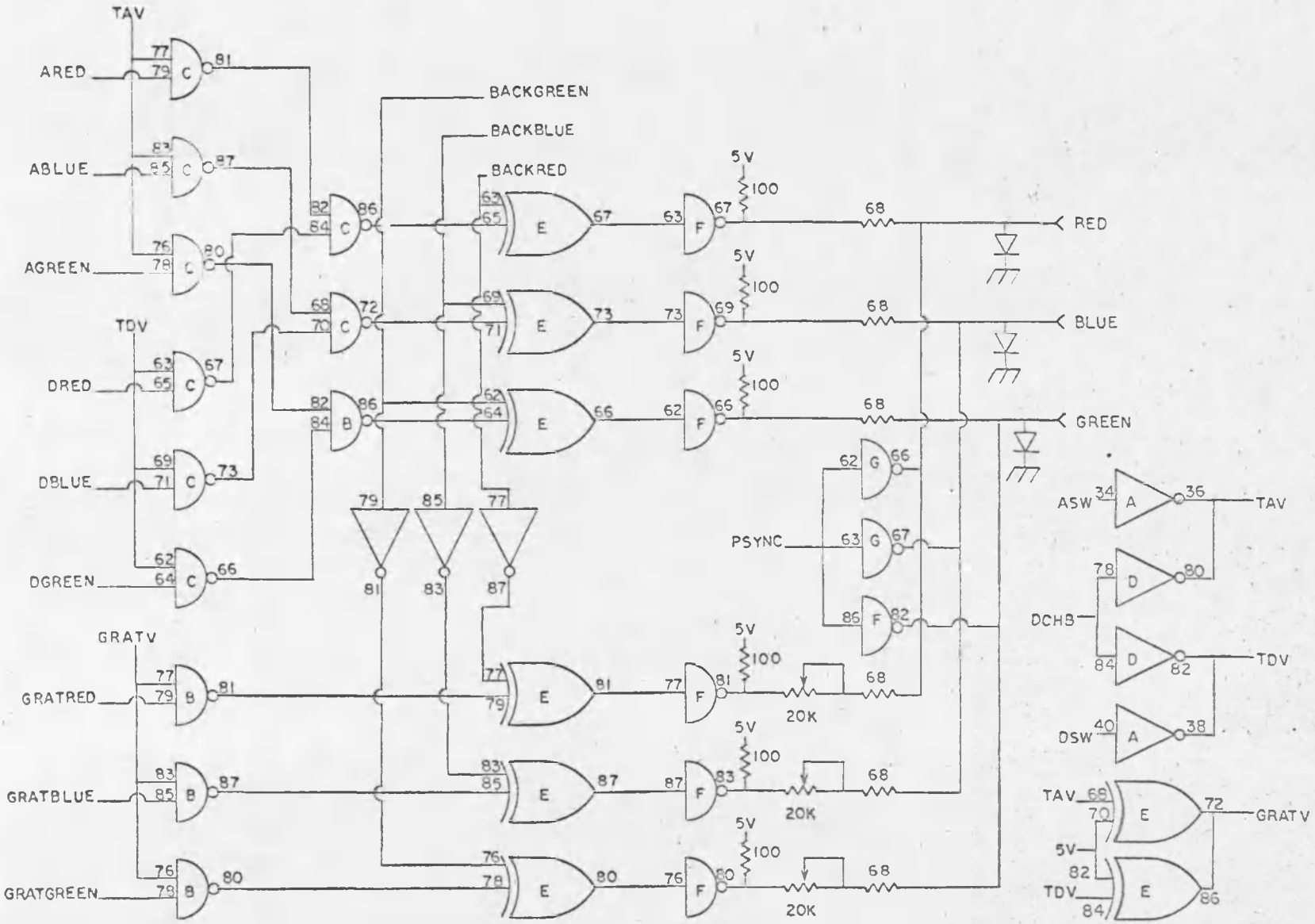

Figure 11. Video Switching

choice of background colors. These are followed by power gates which drive the video output network. PSYNC is used at G66, G67, and F82 to provide a reference for the DC restorer in the television to permit background colors other than black. TAV and TDV are used at E72 and E86 to disable GRATV. Thus, whenever a plotted point coincides with a graticule point, the graticule point is blanked. ASW and DSW from the data register can blank the points associated with them at A36 and A38 by grounding TAV and TDV respectively. DCHB blanks both traces at D80 and D82 whenever the data channel is not active. This permits usage of buffers in computer memory less than the maximum length of 235_{10}. It also prevents the display of extraneous horizontal lines at the last coordinate plotted when the plotter is not being used. The diodes at each of the outputs clip all signals to equal levels.

CHAPTER 4

CONCLUSIONS

The color television graph plotter has performed to our expectations. It is not a substitute for a graphic display (which can draw pictures and characters, not simply graphs), but a useful adjunct. This exceptionally inexpensive unit requires no digital to analog converters, uses a standard television monitor as an output device, and is not difficult to construct or adjust. It completely eliminates the usual difficulties encountered when using coordinate data to provide analog positioning voltages for a display.

Additional features could be added to the plotter, such as choice of various graticules or control of the color of each point. This hardly seems the proper course to follow considering the design objectives of simplicity and low cost. The unit could also accept one additional bit of resolution in the Y coordinate data word. The input to the comparator for the additional bit could then be the output of the 4MHz clock itself.

A single-trace version of the unit could be used with computers with word lengths as small as 8 bits. The only requirement is that the computer have some sort of automatic data-channel circuit, like the Digital Equipment Corporation PDP-8I, PDP-9, and PDP-15, and the CCC/Honeywell DDP-316 and DDP-516. Otherwise, program interrupts and

display servicing at the line rate of the television would make servicing the display an impossible load for a small computer.

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