AN OPERATIONAL TEST INSTRUMENT FOR PCM BIT SYNCHRONIZERS/SIGNAL CONDITIONERS

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Summary The application for a device which will effectively test a PCM bit synchronizer/signal conditioner is described. The general requirements for a bit synchronizer analyzer are listed and some of the problems in implementing these requirements are discussed, including some problems relating to PCM signal conditioners. A description of an instrument capable of performing the required measurements is given.

Introduction For the past few years the use of PCM in telemetry has increased in popularity. It is well known that all gains in signal recovery are made in the bit synchronizer/signal conditioner front end of ground stations, for past that point all data is digital in form and in theory can be processed with minimum error. Yet with this fact known it has not been until recently that the need for a piece of test equipment to evaluate or periodically check this crucial subsystem has been recognized. Formerly, ground station personnel could measure the performance of the bit synchronizer/signal conditioner by collecting numerous pieces of test equipment, connecting them with cables and laboriously set up a test procedure. This was cumbersome to say the least, slow, and not particularly meaningful as the compatibility between the pieces of equipment was not always ideal especially at high bit rates where capacitive loading creates problems. Therefore, it became obvious that a piece of test equipment that was relatively easy to set up, quick in operation, and would make reliable repeatable measurements would be very useful, particularly where a mission might be marginal in signal strength and it would be necessary to verify the proper operation of the bit synchronizer just prior to usage.

The following is a description of an instrument not only capable of making pre-flight test, but also as an instrument for detailed evaluation of a signal conditioner.

Requirements for a Bit Synchronizer Analyzer The operation of a bit synchronizer/signal conditioner is affected by many parameters, which are in general well known. It is only the number of variables and lack of precise measurement standards which complicate the problem of testing. The design of a bit synchronizer analyzer does not imply the generation of measurement standards, but simply allows the

test under accepted conventions, or conditions more closely resembling actual operational use.

What then should the capabilities of such a test instrument conceivably known as a “Bit Synchronizer Analyzer” be? It would seem logical that the instrument should simulate all or nearly all the variable parameters confronting the bit synchronizer such as

1. Variable signal to noise ratio
2. Known or random bit pattern
3. Different code forms such as NRZ, RZ, Split-Phase, etc.
4. Various signal and noise bandwidths
5. Variations in input amplitudes
6. Clock drift and jitter
7. Signal offsets
8. Data dropouts

In order to measure the performance of the bit synchronizer under test it would, in addition, have to perform these functions.

(1) Provide a means for compensating for delays in the synchronizer and subsequently synchronizing the operation of the two units.
(2) Detect and accumulate data bit errors for a known period of time.
(3) Provide a meaningful display of the result of the measurement.
(4) Provide the operational features necessary to make quick, convenient, reliable, accurate measurements without excessive setup time.

A general block diagram of a bit synchronizer analyzer is shown in figure 1. The general operation with a typical bit synchronizer is described as follows.

The clock generator is a stable, calibrated source of timing pulses for the entire system. The bit rate is adjustable throughout the standard IRIG frequencies. The data pattern generator is in reality a simple PCM simulator with NRZ output to a code converter. The code converter transforms the NRZ signal into RZ, NRZ, Split phase, etc., forms and drives a noise mixer. A noise source with bandwidth and spectral density compatible with the selected bit rate also drives the noise mixer. The noise mixer also contains provision for a low pass filter if required to duplicate a known pre-transmission filter in a simulated system. The output amplifier provides a low impedance output to the bit synchronizer under test and to a signal/noise monitoring and control circuit.

The analyzer output is connected to the bit synchronizer under test and the bit synchronizer output connected into the data error detector of the analyzer. The simulator signal is delayed before it is compared with the output of the synchronizer. The errors

resulting from the bit by bit comparison are accumulated over a proper time base selected according to the SIN ratio and displayed on a digital display or externally recorded if desired.

With such a setup, any of the parameters may be preset or varied to statically or dynamically evaluate the performance of a bit synchronizer by observing the change in bit error rate. In the case of a pre-flight check, the analyzer may be set to resemble an input signal condition just prior to or during acquisition. The latter check is a particularly valuable one in that the errors produced in bit synchronizer may not be as a result of the incoming S/N ratio but as a result of R. F. I. or other undefinable perturbations. No matter what the source is, the analyzer will read the true error rate which may or may not be acceptable for a particular operation. If not acceptable and the bit synchronizer is known to perform satisfactorily in another environment, then the analyzer can be used as an interference indicator to troubleshoot the system.

General Considerations of Measurement There are a number of factors to consider in setting up measurement parameters for evaluating error performance. Probably the most difficult parameter to define and measure is the signal to noise ratio. The generally accepted definition of signal to noise ratio in PCM is

$$(1) \quad S/N \quad (db) \quad 20 \log \left(\frac{E_s}{E_n}\right)$$

where E_S = Peak Signal or $\frac{E_{\text{signal (peak-to-peak)}}}{2}$

and E_n = RMS Noise Voltage over the signal bandwidth.

As many bit synchronizer specifications require that the bit synchronizer perform within 1 db of theoretical at some point or points then it is requisite that for this criteria the S/N ratio be accurate within . 5 db or better. Therefore, the ratio $\frac{E_s}{E_n}$ must be accurate within ±6%.

In a practical situation the operator may measure one of these factors with sufficient precision to relax the requirement on the other factor which may be more difficult to define. If, however, conventional meters are to be employed it is difficult to have a readable accuracy of better than 2% even with mirror scales, hence, it may be said that for .5 db accuracy measurements for both signal and noise should be in the order of ±3%. If 1 db accuracy is required then measurements can be relaxed to ±5%.

A serious factor to be taken into consideration is the wave form of the signal. For square sided signals a peak signal can be measured simply by using d. c. transfer techniques. However, in some systems a Gaussian or the linear phase filter is employed to reduce bandwidth requirements. A typical filter response is shown in figure 2. It can be seen that the fundamental frequency of the bit period (f) is down between 2 and 3 db from the low frequency response, therefore, the peak amplitude that exists at any instant is variable depending on the bit pattern.

Figure 3 illustrates the difference in amplitudes existing for a single bit and a group of consecutive bits in the filtered case. 1

Dr. J. H. Crow has pointed one approach to this problem[1]. In essence, with a prior knowledge of the bit pattern and synchronizer parameters one can compensate for the pattern related amplitude distortion by computing a correction factor for each portion of the wave train and then computing the resulting overall effective signal to noise ratio. If the same simple pattern is repetitive then this approach is simplified. A chart can be constructed for several common pattern formats showing the effective S/N ratio. This is probably the simplest overall answer.

It has been assumed in the previous discussion that the noise voltage within the bandwidth was generated in the proper form and measured with a fair degree of accuracy. It must be pointed out that in practice this has not always been the case. The meter used to measure the noise should be a true RMS meter with the accuracy required over a sufficient bandwidth.

This implies a meter bandwidth in the order of 10 mc for 1 mc data bits with 100 usec rise and fall times. If the noise conforms to the Gaussian distribution curve, figure 4, then an average measuring meter may be employed with a correction factor to read rms. With reference to the Gaussian response above, another factor should be noted. The standard deviation σ defines a probability that a noise peak will exceed the rms value of the noise; 2 σ defining the corresponding probability of a peak existing that exceeds 2 times the rms value, etc. It should be noted that those noise pulses causing errors are only those equalling or exceeding the peak signal (for a perfect detector) hence any restriction in the distribution probability of large amplitude noise pulses will limit the measurement of errors at high signal to noise ratios. For example:

if E_s (peak) = 10 v
E_n (rms) = 1 v
then S/N (db) = 20

For an error to exist then a noise pulse of 10 v is required implying a deviation of at least 10 σ .

It is not uncommon for commercial noise generators to have crest factors $\frac{E_{peak}}{E_{rms}}$ of considerably less than 10, in fact often less than 5. A crest factor of 5, in general, will limit the measurement of errors due to noise insertion with the signal to S/N ratios of about 14 db. This may not be to important, however, in a practical sense, because error measurements at high signal/noise ratios generally take considerable time, sometimes hours, to detect an error and one must consider the possibility of other factors such as R. F. I. , line surges, and other perturbations being the main contributory factor to errors.

Figure 5 illustrates a typical bit error probability curve showing the range of general practical interest.

It may be noted that most error rate comparisons to the theoretical curve assume perfect bit synchronization. In actual practice, though synchronizers maintain average bit synchronization, overall performance is somewhat degraded.

Bit Pattern Factors Another parameter to consider is the bit patter Factors of the bit pattern are transition density, pattern symmetry, code form and bit rate.

The transition density is a factor often used in measuring sync acquisition time. The practical limit generally accepted is one transition in 64. For higher densities such as 4 in 64, pattern symmetry becomes an other factor. The four transitions could be sequential or equally spaced throughout the 64 bit periods. The sync acquisition or reacquisition time of some types of bit synchronizers is dependent upon pattern symmetry a well as density.

The code form (RZ, NRZ, Split Phase, etc.) also needs to be defined. Split phase (Manchester or bi-phase) code has at least one transition per bit period, hence, implies a different sync acquisition characteristics than NRZ code where low transition densities readily exist.

System Delays System delays are another parameter to be considered. Usually one bit delay can be expected in the bit decision circuitry. To compare this bit decision with input data, a means must be supplied to delay the input signal a corresponding amount before entering the bit comparator. Other incidental delays can contribute fractions of a bit period delay, hence it is desirable to provide, in addition to integral bit delay periods, fractional bit period delays in the order of one quarter bit period. The proper use of

strobing techniques in the bit per bit comparator preclude the necessity for incremental delays less than one quarter bit period.

Miscellaneous Factors The D. C. off set of the input signal is a variable factor requiring definition as synchronizers must effectively reestablish the optimum quantization level in order to perform close to the theoretical maximum, and generally are limited in the range of offset they will tolerate.

Input clock offset from pre-set frequency, synchronizer clock drift, rate of drift and pulse jitter are all variables to be considered when a precise evaluation is required.

Sync Acquisition Time Another important parameter is the measurement of acquisition and reacquisition time. Measurement of these characteristics is largely dependent on the definition of the term "effective synchronization". While this may often be measured in terms of a particular signal in a particular synchronizer, there appears to be no universally applicable definition which is completely satisfactory. As mentioned previously, the transition density of the bit pattern affects this measurement. The bit synchronizer VCO displacement from the bit rate of the incoming PCM signal is also a factor. To measure acquisition time several approaches can be considered. One approach is to compare clock trains and accumulate errors generated on a bit by bit basis. The determination of when the bit synchronizer is in sync is that point at which the clock bit errors have reduced below some predetermined number.

Another more practical system is the measurement of data error rate. Synchronization is said to occur when the data error rate reduces from some large number to a predetermined number.

Description of a Practial Bit Synchronizer Analyzer The Defense Electronics, Bit Synchronizer Analyzer, Model BA-101, is an instrument which provides the necessary functions for evaluation and operational testing of a Bit Synchronizer/Signal Conditioner. Although the unit does not represent a state of the art breakthrough in terms of new circuit designs, etc., it now permits tests to be reliably performed which were previously not practical. As with most designs, especially in view of the considerations previously discussed, certain inevitable compromises must be made. In the following description, it is apparent that these compromises with theoretical requirements generally enhance operational usefulness and do not materially degrade the validity of the measurements.

As previously discussed, any analyzer must contain at a minimum a source of signal, suitable interface and delay, a means of comparing the simulated and reconstructed data and a display. There are, however, additional requirements, pertaining to the equipment

design. First, the unit is required to be completely self-contained. This implies that the power supply, measuring devices, etc. all are included in the basic unit. Further, since it is an operational instrument, attention must be paid to human engineering aspects. While it is desirable to make the device infallible due to operator error, this would severly restrict the flexibility, therefore, additional care is required in layout, range of simulation, measurement, etc. The front panel and ‘block diagram of the DEI Bit Synchronizer Analyzer are shown in figures 6 and 7.

Basic to the generation of a PCM wave train is the bit rate oscillator or clock. The frequency range of the clock is 1 bit per second to 1, 000, 000 bits per second. A calibrated dial is provided in addition to the normal tuning which deviates the clock frequency ±10%, or ±20%. Inputs for slow drift of the bit rate or low frequency FM and jitter or high frequency FM are provided. External clock inputs are also provided on the plug-in clock assembly.

There are four types of data patterns which provide the data type most useful in the testing of a signal conditioner. One is Variable Transition Density. In this simulation mode, one transition is generated every 2, 4, 8, 16, 32 or 64 bit periods regardless of output code form. These transitions are selected to be either symmetrically distributed over a 64 bit “frame” or occur in consecutive bit positions with no transitions in the remaining bit positions for the rest of the frame. Another simulation mode generates a pattern which is effectively random, yet predictable. A third mode generates a truly random pattern whose bit density is adjustable. Finally, a number of coding switches are provided to allow the simulation of patterns of special interest. These patterns satisfy the requirement that they be useful for evaluation using accepted conventions and resemble typical operating conditions. The necessary gating for data interrupt is also provided. In order to minimize inconsistencies in acquisition and reacquisition time due to random data return in low transition density outputs, the return of data may be selected as random or phase locked to a point in the data frame.

The digital pattern is one component of the composite signal. The amplitude of the signal is first adjusted and the rectangular signal is zero centered in a manner that does not permit normal capacitive discharge decay over a long period of time. The signal is then linearly combined with noise. The noise is of a Gaussian distribution to greater than five sigma, and has a sufficiently uniform spectral density. The amplitudes of both signal and noise are adjustable to allow maximum flexibility. As is shown in the front panel picture, three preset (screwdriver adjustable) signal amplitudes are provided to facilitate rapid repetition of measurements. Normally, these would be set to correspond to specific points of interest. The signal plus noise is then passed through the filter section where one of three switch selectables plug-in filters or no filter is inserted in the signal plus noise path. The filter normally supplied is a 6 pole Bessel Polynomial type with a -3 db

point at the frequency of interest. Of course, provisions are made for other types on special interest.

Following the filter, an amplifier adds an off set voltage to the output signal and provides a low impedance output to the synchronizer under test and the composite signal monitoring circuit. The monitoring circuit allows the convenient measurement of peak signal amplitude, within limitations, rms noise amplitude and signal plus noise. The importance of the proper interface between the bit synchronizer analyzer and the synchronizer cannot be overemphasized, since no degradation of any of the composite characteristics may be tolerated. This is particularly true where there is a relatively long cable run between the two equipments.

The bit synchronizer analyzer receives reconstructed NRZ data and clock from the signal conditioner. Since interface levels are seldom compatible, the appropriate level shifters are included. NRZ data from the internal simulator is suitably delayed and compared to the reconstructed data in a strobed exclusive OR.

Care must be exercised in the choice of the strobe and delay, since it must allow a large amount of transition displacement due to high frequency FM of the clock without creating extraneous errors. By providing appropriate controls and procedure, it is not difficult to select the delay and adjust the strobe without external equipment. The output of the data comparator is a data error and is routed to the input of the display accumulator. In this area, bit decision errors are accumulated over a period of time. The sample period, measured in bits, allows easy comparison of signal conditioner performance to theoretical maximums. It also is an indication of percent bit errors for relation to some acceptable level for a particular mission. A display overrange indicator, used in conjunction with the anticipated performance allows setting of the sample period without external equipment. The display itself is a three digit projection decimal display. Three display modes are provided. The normal mode accumulates errors over a period of time. The accumulate and hold makes a measurement and stores the result until manually reset. The accumulate mode is most useful when accumulating over a long period of time at low bit rates. Although measurements can be made without external devices, a printer is often desirable for long term measurements. The required interface is provided in the unit so that once the test is set up, a printer may be connected and the device left unattended.

The reconstructed and internal clock are compared to indicate a loss of sync in the period of one frame. Such a loss of sync indicates that the synchronizer is operating in an area of unreliable bit synchronization and that the bit decision errors are due at least in part to unreliable synchronization.

As previously discussed, the measurement of time to acquire and reacquire is desirable. However, it is not practical to attempt direct measurement of a parameter which is so nebulously defined. Inevitable, the acquisition characteristics are reflected in the number of bit decision errors during the period since it is virtually impossible to make correct decisions without bit synchronization. Therefore, a workable method which indirectly measures acquisition or reacquisition time in bits is to measure the number of bit decision errors over a period much greater than the anticipated acquisition time. By assuming that 50% errors exist during acquisition, twice the difference of bit decision errors is the time in bit periods to acquire. Repeated measurements under the same conditions especially when the return of data is phase locked, will allow a high confidence in the measurement.

From the descriptions above it is apparent that the necessary measurements can be made without external equipment for an operational check. However, the design of the unit does not preclude the use of external equipment for more specialized tests, such as a PCM simulator capable of generating a larger format.

The Bit Synchronizer Analyzer is packaged for mounting in a standard rack. High reliability silicon logic modules are used throughout. A tilting front panel allows easy access to the test points on the logic modules and front panel. The power supply is a modular unit mounted on the rear of the card frame.

Conclusions A device to effectively test Bit Synchronizer/Signal Conditioners has been developed. The bit decision errors are of primary importance in the signal conditioner and effective measurements can be made in these terms.

References

1. PCM Signal and Noise Performance by Dr. J. H. Crow, NTC, 1962

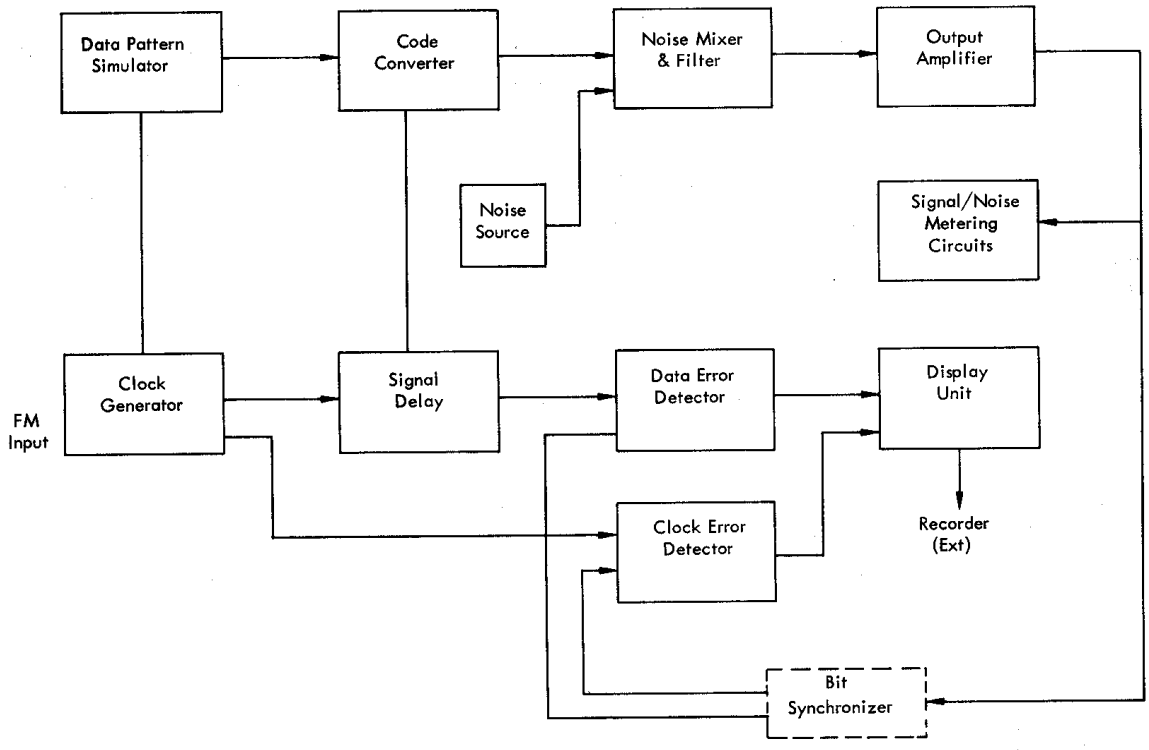

Fig. 1-General Block Diagram, Bit Synchronizer Analyzer

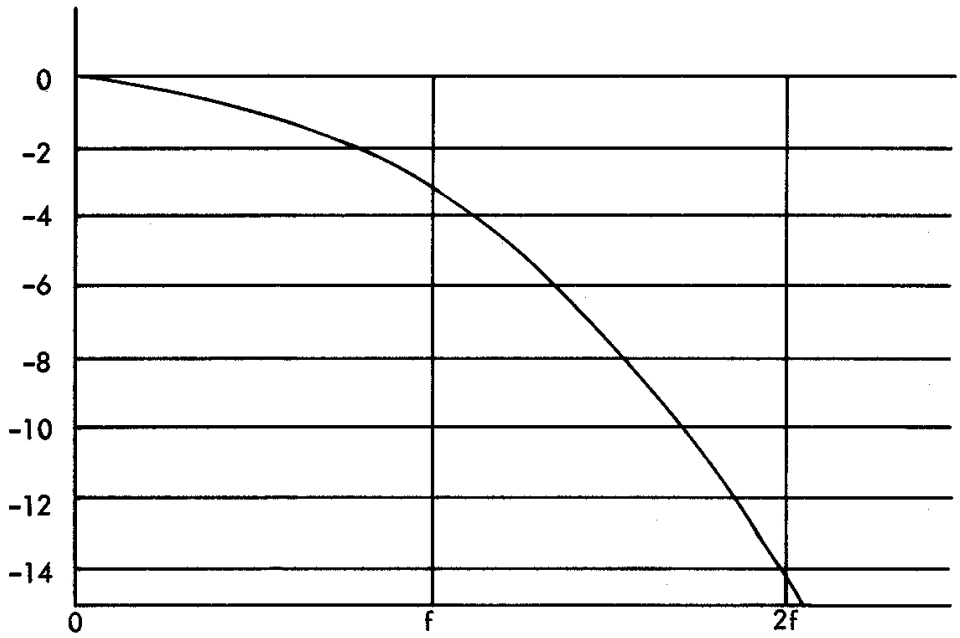

Fig. 2-Typical Response - Linear Phase Filter

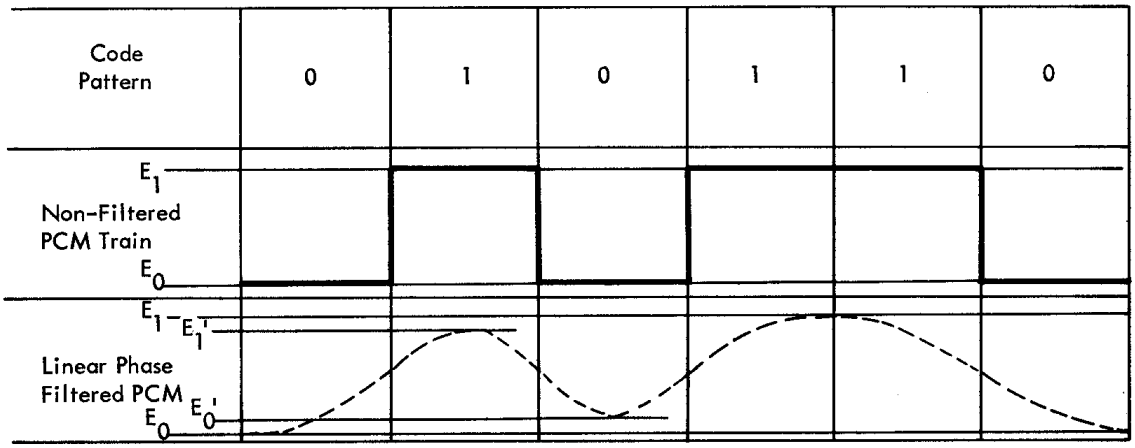

Fig. 3-Typical PCM Waveforms

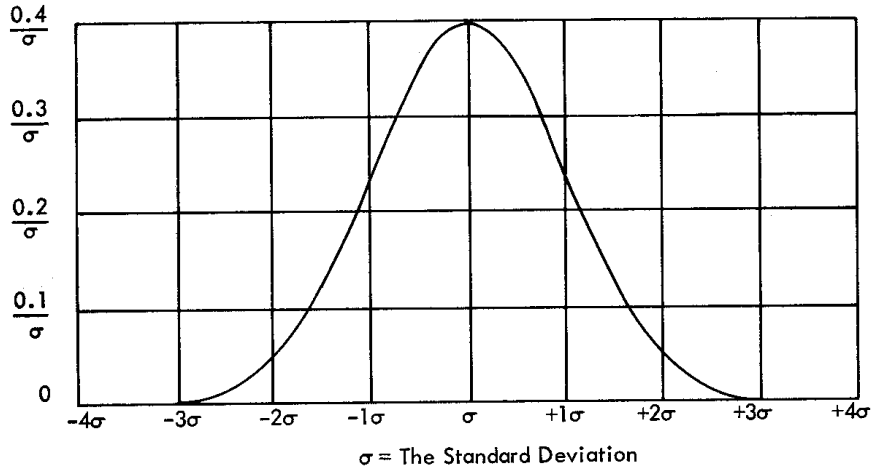

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Fig. 4-The Normal Distribution Curve

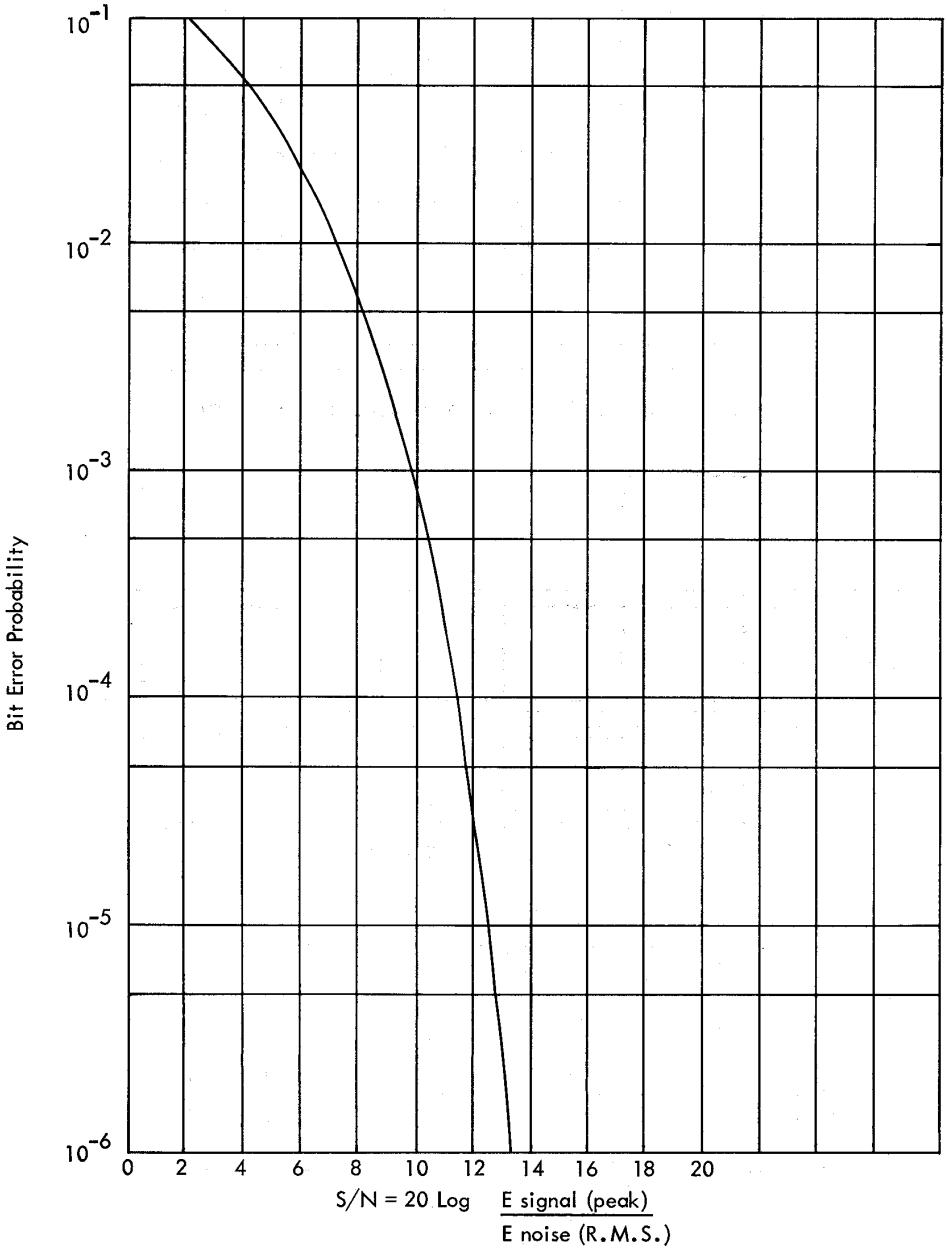

Fig. 5-Bit Error Probability Versus Signal Noise Ratio

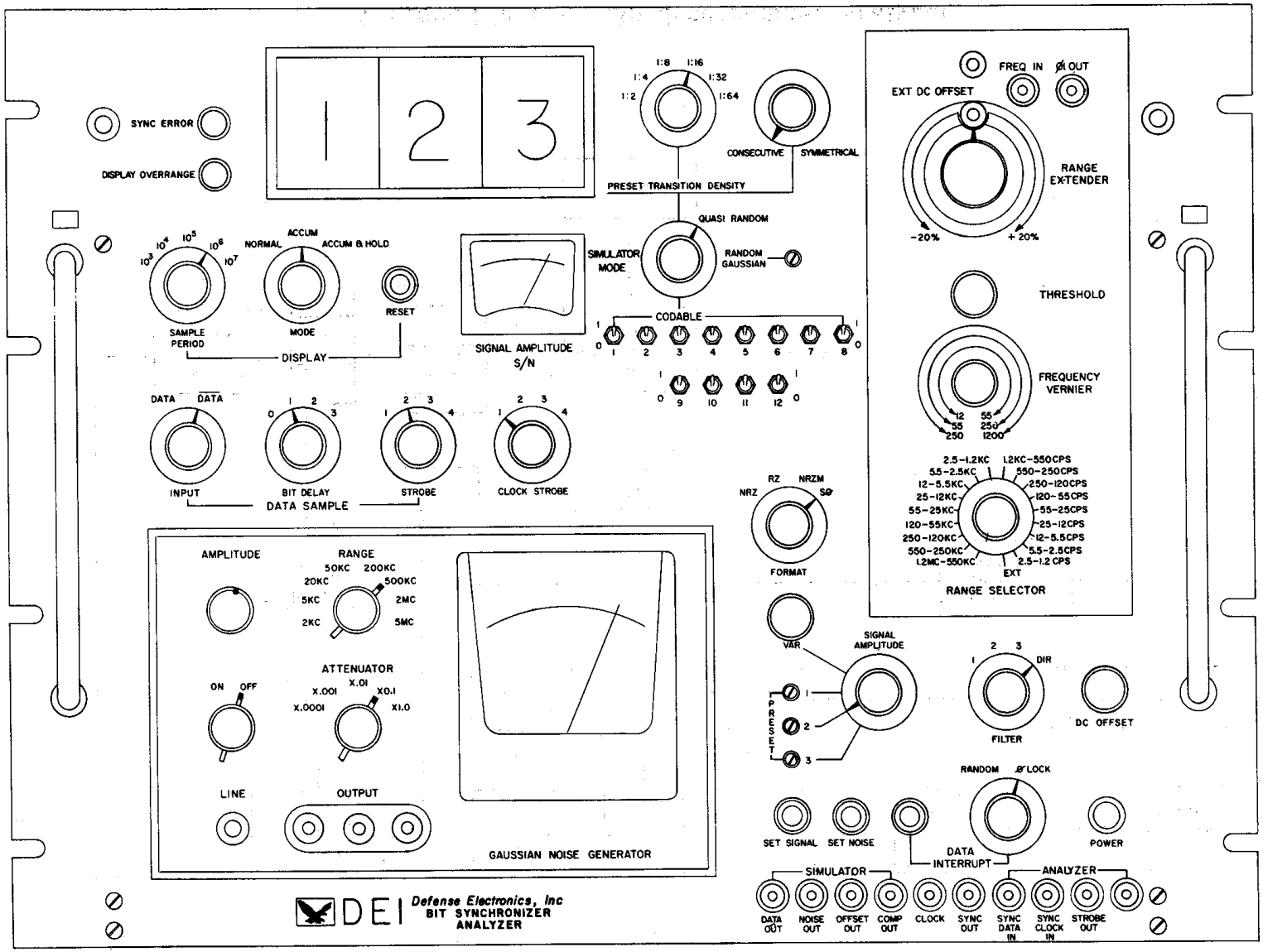

Fig. 6-Bit Sync. Analyzer, Front Panel

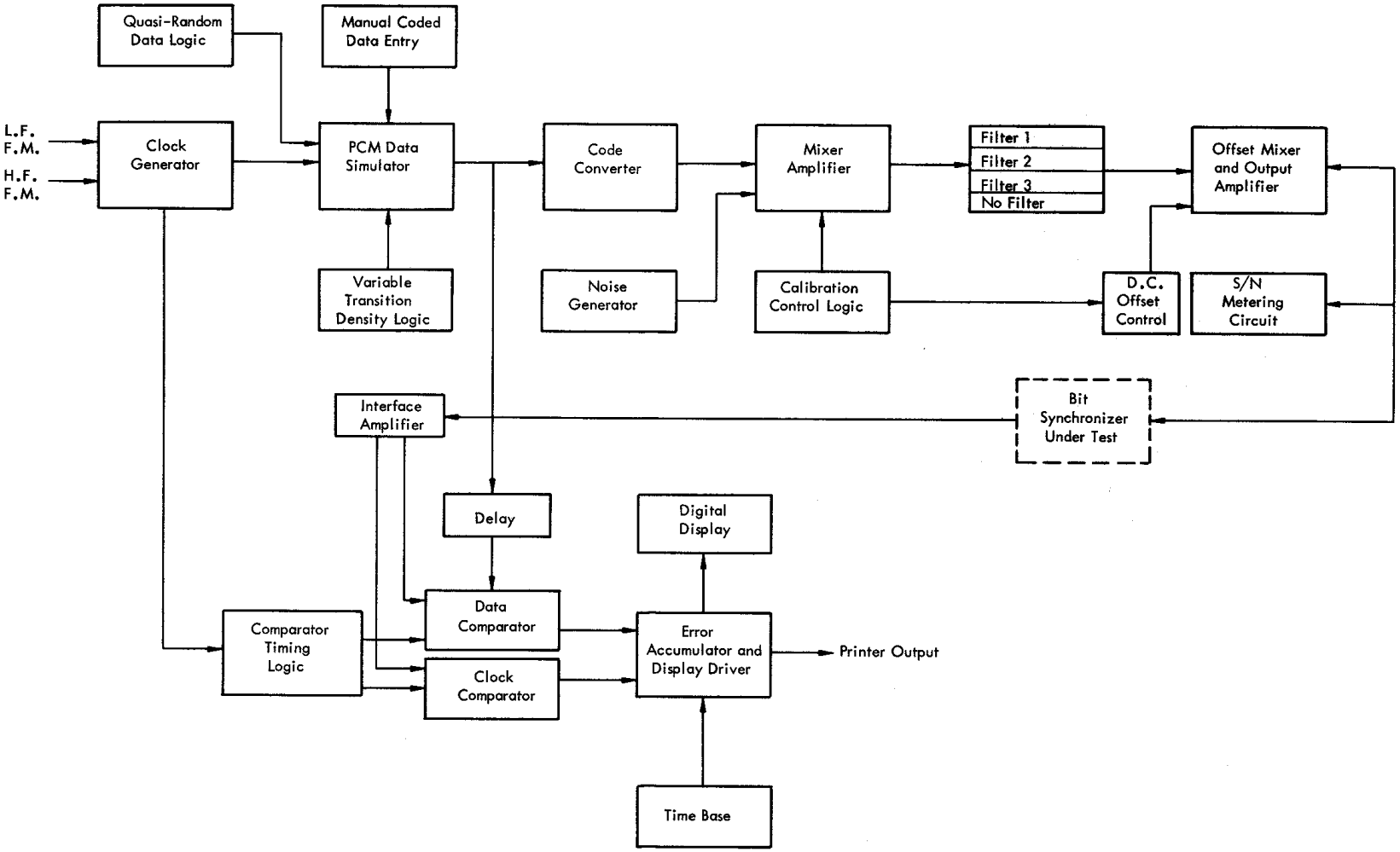

Fig. 7-Block Diagram, Bit Synchronizer Analyzer