

A NEW APPROACH TO SOLID STATE COMMUTATOR DESIGN

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Abstract An electronic commutator is described which employs only two types of modules and is expandable one channel at a time. Either high or low level commutators can be constructed. Data input circuits are completely isolated from gating voltages. Power per channel is 10 milliwatts; volume, 0.4 cubic inch. Commutator modules are suitable for air/spacecraft environments,

Introduction In commutator applications it is sometimes necessary to increase the number of channels by one or more beyond the capacity of the purchased commutator. In other instances it may be desirable to increase or decrease the number of channels without changing the relative sampling rate of existing data inputs. For example, in field use, late measurement lists may require the addition or deletion of measurements with no change in relative sampling rate of measurements already programmed. Also, no part of a data frame should be idle.

Generally, existing airborne commutators cannot be increased in channel capacity (except through use of subcommutators) and ground-based only in groups of channels or via subcommutators. Also, deletion or addition of channels results in idle frame time or change in relative sampling rate of existing data inputs.

The following sections describe an electronic commutator which, in its most basic form, employs only two types of modules and is expandable or contractable one channel at a time. The number of channels selected need not bear an integral relationship with any other number. Change in channel capacity does not change the relative sampling rate of the existing channels nor does it cause idle frame time.

The commutator has been designed around two basic commutator modules: a gate-switch module (one used for each commutator channel desired) and a start-reset module. Power consumption is low and builds up linearly with the number of modules inserted. Total volume of this composite commutator is competitive with standard single-package electronic commutators containing a fixed number of channels. The modules are plugged into a base plate having a capacity equal to the maximum anticipated number of channels required and is suitable for air/spacecraft environment.

Gate Generator In most electronic commutators, the gate voltages necessary to sequentially turn the transistor or diode switches on is derived from a counter (driven by a clock) and associated diode matrices. The counter usually consists of a single binary counter feeding a diode matrix, two ring counters using four layer devices or two binary counters with diode matrices to generate gating voltages equivalent to that produced by two ring counters.

In order for a commutator to be expandable one channel at a time by adding modules, it is convenient to use a ring counter to provide the sequential gate voltages. However, it was felt that a ring counter employing four layer devices would not be sufficiently reliable for 45 or more stages operating up to 100°C. Also, the parts count becomes prohibitive when using the best ring counter circuit. For this reason a special gate generator was designed using a transistor and three passive elements per stage. It will operate reliably with either a very small or very large number of stages over a temperature range of -40°C to 100°C (lower temperatures, if required).

FIGURE 1 is a schematic diagram of an N-Stage gate generator. Briefly, it consists of a group of RC coupled stages (denoted as “gate circuits”) fed by a re-settable multivibrator (denoted as “start-reset” or “SR” module). Operation of the gate generator is as follows: When not connected to the start-reset (SR) circuit, (at points A and D) the gate circuits are quiescent and each stage is saturated and conducting a fraction of a milliampere of collector current. Under this condition the SR runs with a period of T_1 as indicated in the upper two waveforms of FIGURE 2. If the connection between C_1 of the gate circuits and point A of the SR circuit is made, the rectangular waveform produced at point A is supplied to the base of Q_1 via capacitor C_1 and holds that transistor off for period determined by the time constant of C_1R_1 and the adjustable voltage, $-V_F$. The waveform produced at the collector of Q_1 , point Y_1 , is shown in FIGURE 2. During the period that Q_1 is nonconducting, capacitor C_2 charges through resistor R_{11} to potential $-V_1$. Following this period, Q_1 becomes conducting and the potential of y_1 suddenly rises to potential $+V_2$ and this step voltage is applied to the base of Q_2 via capacitor C_2 , thereby cutting off Q_2 for a period of time determined by the time constant C_2R_2 . In this manner all transistors in the string of Q_1 through Q_n are sequentially turned off for a period determined by their respective base circuit time constants and $-V_F$. If the time constants associated with all the stages are equal, the negative gating pulses appearing at the collectors are equal in duration. Time constant $C_A R_A$ of the SR circuit is approximately twice as large as C_1R_1 , C_2R_2 , etc. Time constant $C_B R_B$ is chosen so that T_1 (FIGURE 2) is larger than the longest anticipated frame period. With the lead between point Y_n and capacitor C_R open, the gate circuits once again assume a quiescence condition until a succeeding positive pulse is generated at point A of the start-reset circuit. However, if point Y_n is connected to C_R , the SR is reset by the trailing edge of the negative gate voltage generated at Y_n . Simultaneously, a positive gate voltage is produced at point A of the SR, a negative pulse is generated at Y_1 and the frame is repeated.

It is seen that the function block denoted as start-reset or SR module is a resettable multivibrator which serves to start and sustain the operation of the gate circuits. It has a natural period that is longer than the longest anticipated frame period but can be reset any time following the second channel period. It is this factor which makes it possible for the gate circuits to function with an extremely large range of stages.

Frame sync pulses are available from point A of the SR circuit and clock pulses are taken from point C. Both waveforms are shown in FIGURE 2.

Floating Transistorized Switch As a companion to the gate circuit stage, a transistorized switch was sought which would provide complete isolation between the gating source and the signal source during the sampling interval and yet have a capability for handling a very large range of gating pulse widths. The transistorized switch shown in FIGURE 3 was designed to meet this requirement. It functions well for gating intervals ranging from 10 microseconds to 1 second. Operation is as follows: During the "OFF" time point A is held at a positive potential, V_2 , which is somewhat more positive than the most positive excursion of the input signal. Under this condition capacitor C_1 is charged to its maximum potential via diodes CR_3 and CR_2 . At the same time the bases of Q_1 and Q_2 are held positive with respect to the input signal by current flowing through diodes CR_1 and CR_4 to point A. When a negative gate voltage, $-V_1$, is applied to point A diodes CR_1 , CR_2 , CR_3 and CR_4 are reverse biased and capacitor C_1 proceeds to discharge through base resistors R_1 , R_3 and the base collector junctions of Q_1 and Q_2 thereby turning on the transistor switches.

The most negative signal excursion that can be handled relative to potential levels $+V_2$ and $-V_1$ is approximately $-V_1 + V_d$. The most positive is approximately $V_2 - V_x - 2V_d$, so that the maximum peak to peak signal excursion is E_s (P. P. max.) = $V_2 + V_1 - V_x - 3V_d$, where V_x is the voltage decrease of capacitor C_1 during a channel period, and V_d is the forward drop across a diode.

The floating transistorized switch described has a maximum back (reverse) current of a few nanoamperes during both the "ON" and "OFF" periods and this current is independent of the base current chosen. Direct-coupled switch configurations are simpler but have "ON" time back currents ranging from a fraction of a microampere to several microamperes, depending upon the base current chosen and the preciseness of component values and voltage levels.

Gate-Switch Modules FIGURE 4 combines the floating transistorized switch shown in FIGURE 3 with one gate circuit stage of the Gate Generator shown in FIGURE 1 to form a high level gateswitch module. These modules are cascaded as needed to yield the required channel capacity.

FIGURE 5 combines a gate circuit stage with two floating transistorized switches to form a module which has a differential, low level switching capability. As with the high level unit, complete isolation is obtained between the signal circuits and the gating circuits. Also, the two poles are completely isolated from each other. The common mode voltage range is determined by $-V_1$ and V_2 as discussed in the preceding section.

The gating circuit shown in FIGURES 4 and 5 is also suitable for gating field-effect transistor switches on and off. FIGURE 6 shows one FET circuit configuration in which the gate source potential is held at approximately zero during the "ON" time. The gate resistor R is bootstrapped by being connected to one stage of the buffer amplifier (shown functionally in FIGURE 7).

Other Modules Although the basic commutator requires only a start-reset module and gate-switch modules, three other modules are available: (1) PAM Buffer and A/B Gating unit (2) PDM Keyer, and (3) Power Supply.

Assembled System FIGURE 7 is a functional block diagram showing the inter-connection of the modules. As shown, 2 DC supply voltages are required. Total power required for each of the plug-in modules is as follows:

Start-Reset	10 MW.
Gate-Switch	10 MW.
PAM Buffer	30 MW.
PDM Keyer	70 MW.

If required, a +28V DC power supply is available as a plug-in module. System accuracy in a composite commutator like this is no different from one contained in a single package. Transistor offset is dependent upon choice of transistor and degree of matching (except for the FET which is essentially zero). Reverse current flowing into the signal sources is very low and is entirely composed of reverse-biased diode type of leakages and is in the nanoampere region except when connected to a Buffer amplifier or PDM Keyer. Either of the latter contribute a maximum of 0.1 microampere at +25°C and 0.25 microampere over the range of -20°C to +85°C. Over-all accuracy of the PAM Buffer and PDM Keyer is 0.1% and 0.25%, respectively, over the same temperature range.

GATE CIRCUITS

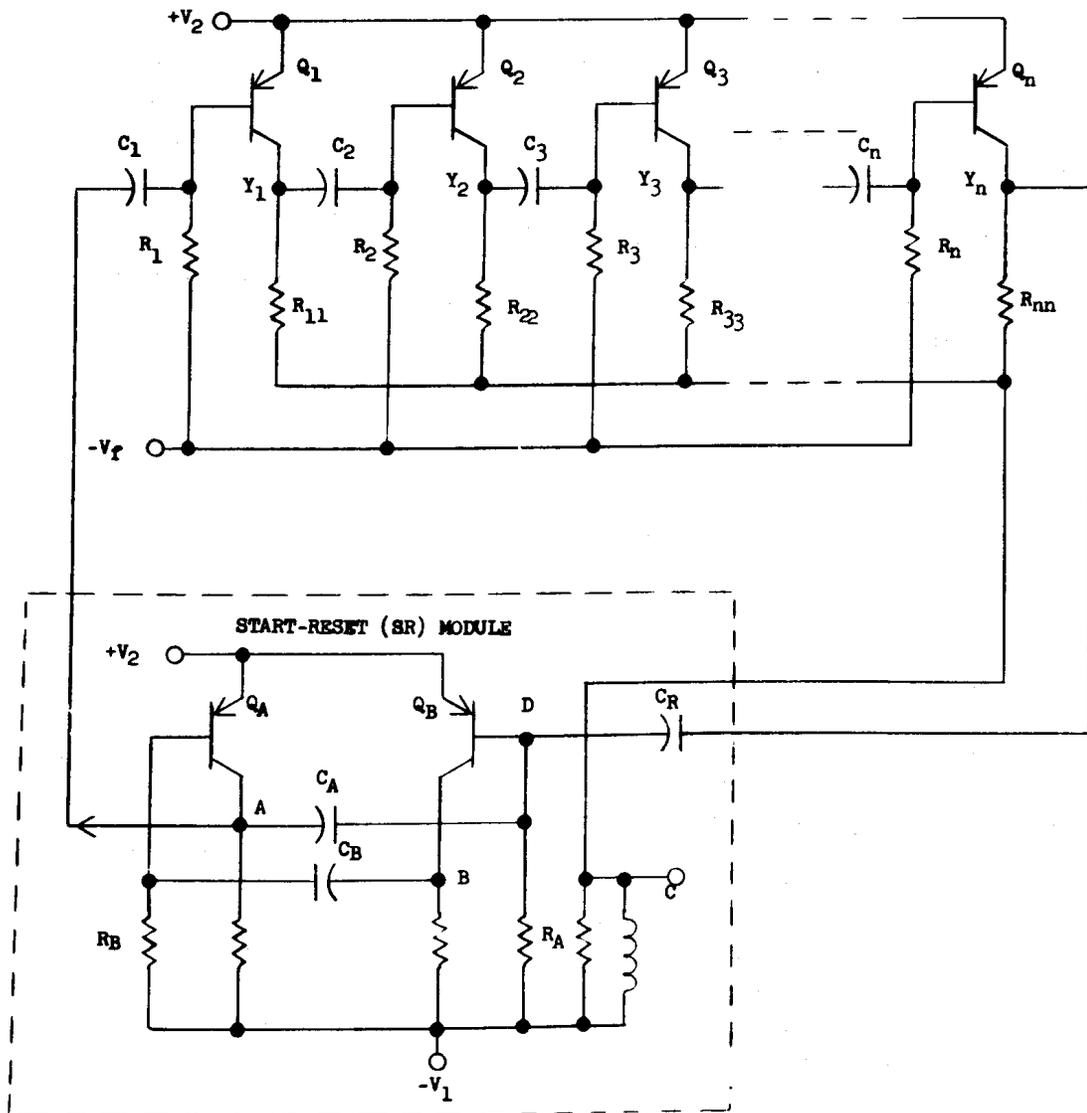


Fig. 1-Gate Generator

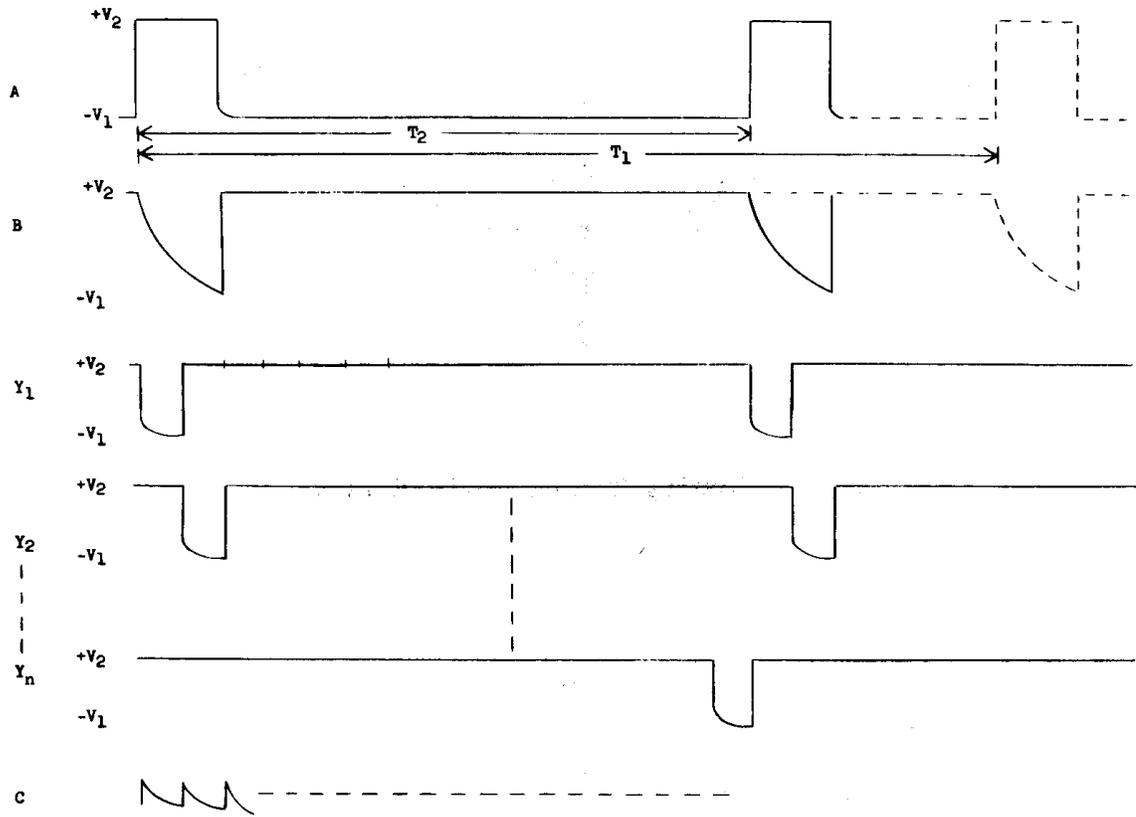


Fig. 2-Gate Generator Waveforms

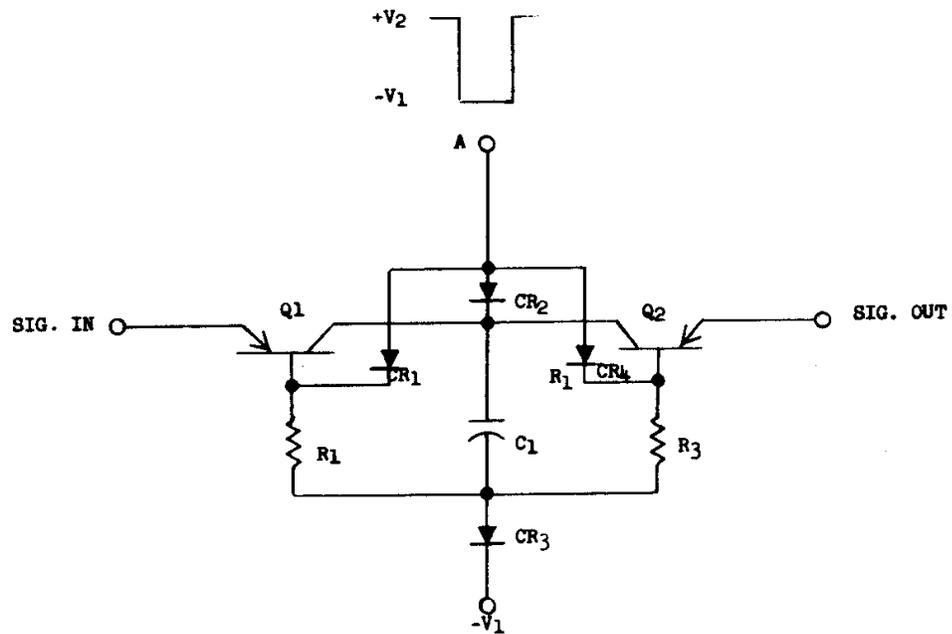


Fig. 3-Floating Transistorized Switch

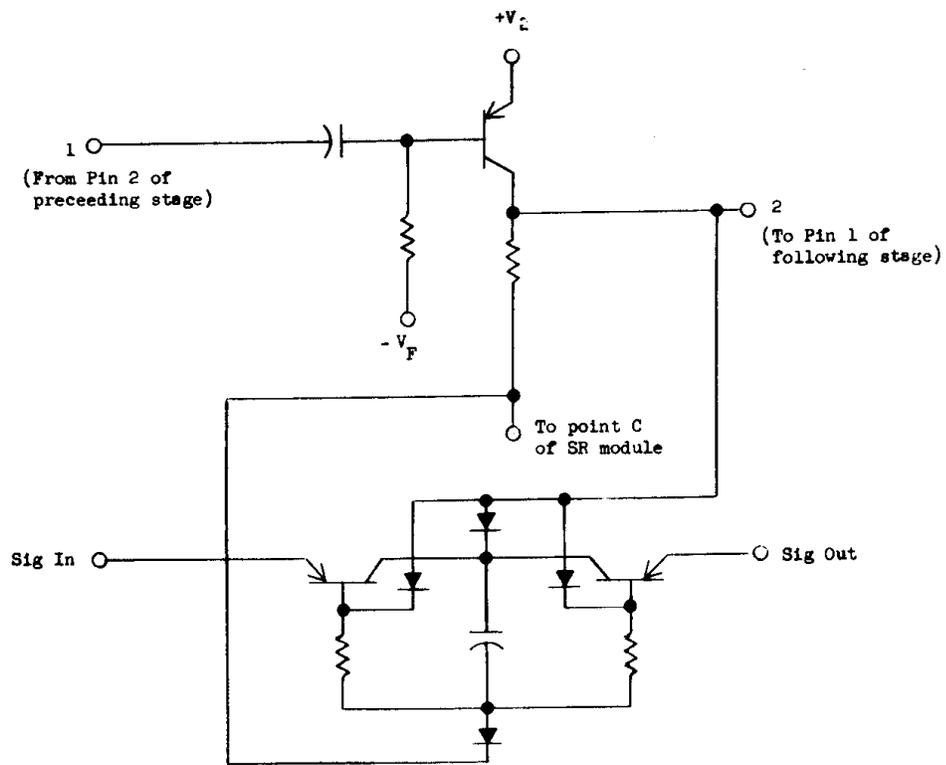


Fig. 4-High Level Gate-Switch Module

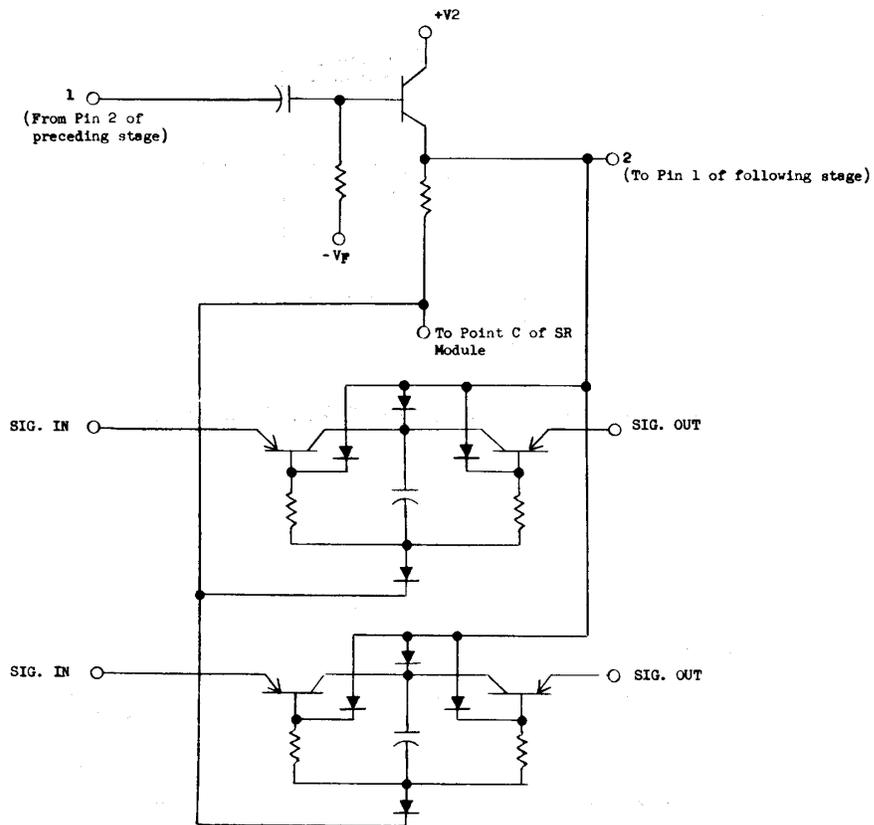


Fig. 5-Low Level Gate-Switch Module

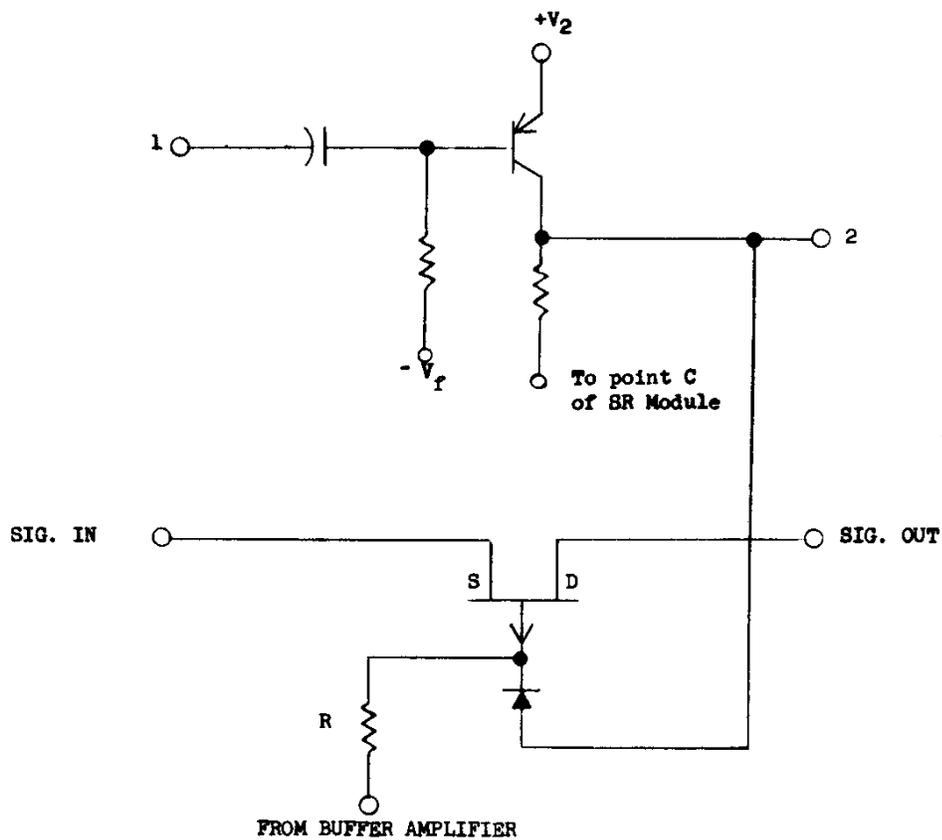


Fig. 6-Gate-Switch Using Field Effect Transistor

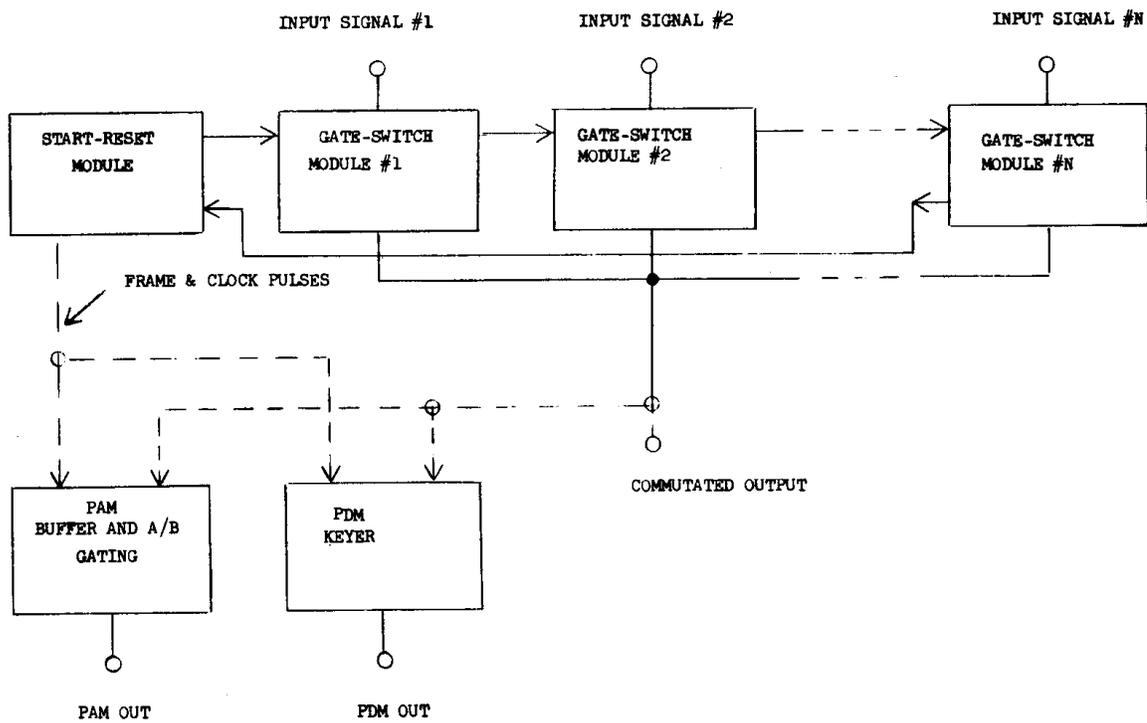


Fig. 7-Functional Block Diagram Showing Connection of Modules