MINIATURE TELEMETRY TRANSMITTER

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Summary The increased use of L and S-Band for telemetry services in conjunction with the need for miniaturized equipment, points up the desirability for compact transmitter units. This report describes a miniature S-Band transmitter and its associated power supply. The design goals are presented together with a discussion of the technical approach used to meet the severe requirements. Illustrations and performance data are included for completeness.

1.0 Introduction This paper is a report on the General Electric Company development of miniature UHF transmitters that is intended to fulfill many of the telemetry and vehicle instrumentation requirements which exist now, as well as those that will exist in the near future, due to increased usage of the L and S-Band telemetry. The development began at General Electric in 1960 and was made possible by the availability of silicon VHF power transistors capable of several watts of RF power output and varactor diodes of sufficient breakdown voltage and cutoff frequency to permit efficient multiplication of VHF power into the UHF spectrum.

By 1963 smaller more efficient components had become available as a result of the industry's movement toward micro-miniaturization. It became evident at that time that the components and techniques required to develop a two watt S-Band transmitter in the range of ten to twenty cubic inches were available. Early in 1964 the requirement for a telemetry transmitter with six cubic inches allotted for the RF and power supply sections respectively became known. This size requirement and the accompanying technical performance objectives were established by the Naval Ordnance Laboratory at Corona, California and are part of an overall Navy objective of developing a miniature general purpose missile instrumentation system. The principal challenges of the program were to package all of the components required to produce a high quality two watt FM transmitter within a total volume of 12 cubic inches, and meet essentially the same performance specifications as were previously met by larger units in a comprehensive range of missile environments, such as temperature, vibration, shock, and electromagnetic compatibility.

Upon completing the design of the preliminary model of the S-Band transmitter, it was seen that with little modification of the S-Band design, an L-Band transmitter for the 1435 to 1535 Mc telemetry band could also be produced. The performance goals for the L-Band unit were the same as for S-Band, however the longer resonators required for the L-Band varactor multiplier made it necessary to increase the length of the cavity section by one inch. The power supply and VHF circuitry of both units are identical, and they differ mainly in the frequency and ratios in the final varactor multiplier stages.

The discussion is principally directed at the S-Band development, however, it is equally applicable to the L-Band version except for these minor differences. Figure 1 shows the transmitter and power supply units.

2.0 Technical Description The S-Band FM telemetry transmitter is an all solid-state transmitter capable of two watts of RIP power output and tunable from 2200 to 2290 Mc. State-of-the-art techniques have been used in the design of the equipment, which fulfill severe requirements on size, frequency stability, and dissipation over a temperature range from -54°C to +95°C.

The power supply uses a high efficiency switching technique to convert and regulate from a DC supply of 27 volts. The package consists of several potted modules using miniature components in a cordwood arrangement. All power connections are on one side of the package.

The transmitter package is fabricated from a solid block with the cavities machined in one end and the remainder containing an encapsulated VCXO module, a circuit board with miniature components, several UHF power transistor stages, and a varactor multiplier stage. Point-to-point wiring is used except for the module. All external connections are made to one surface of the package. The tuning adjustments are external to the package to allow the unit to be easily retuned to a new frequency once the VCXO module has been changed.

2.1 Transmitter A block diagram of the transmitter is shown in Figure 2. The diagram shows the semiconductor types for each stage, typical operating frequencies, nominal power gains, and power levels.

2.1.1 VCXO The oscillator-modulator function of the transmitter is performed by a voltage-controlled crystal oscillator. The oscillator has a frequency range of 22.9 to 23.9 Mc depending upon the operating frequency. This range when multiplied by 96 will give the required output frequency range of 2200 to 2290 Mc. The modulation sensitivity is such that when multiplied by 96 it will give a 125 kc peak deviation for a 1.0 volt rms modulating signal.

2.1.2 Power Stages Power at +4 dbm in the range of 45.8 to 47.7 Mc is supplied by the VCXO module to drive a 2N2368 cascode doubler to 15 mw at 91.4 to 95.6 Mc. A second doubler using a 2N2368 multiplies the frequency to the range of 183 to 191 Mc and to a power level of about 75 mw. The output of this doubler drives a 2N3375 power amplifier to an RF output power of nominally 500 mw.

A 2N3375 transistor doubler increases the power level to 1.5 watts and the frequency to the 366 to 382 Mc range. The 2N3375 is operated as a doubler instead of an amplifier followed by a varactor doubler in order to conserve space. The final power amplifier uses two 2N3375's in parallel to obtain the required dissipation. The output of this stage provides 6. 0 watts at 366 to 382 Mc to drive a varactor multiplier.

2.1.3 Varactor Multipliers The tripler is of the shunt type with series-tuned input and output. The second harmonic is tuned for low conversion loss, while a trimmer capacitor tunes the cavity input loop at the third harmonic. A stud-mounted varactor was selected for high dissipation and mounting convenience.

The cavity doubler is coaxial with a foreshortened quarter-wave resonator and a variable piston capacitor which tune with the varactor dynamic capacitance to cover the range between 1100 and 1145 Mc. The output resonators tune the range of 2200 to 2290 Mc by adjustment of piston capacitors.

2.2 Power Supply The power supply consists of a DC to DC converter, which accepts primary power and converts it to the regulated levels required to operate the transmitter. The converter operates from a 27 volt ± 10 percent source. It provides three output voltages with a total power of 18.5 watts. This requires a conversion efficiency equal to, or greater than, 75 percent to remain within the 25 watts of available power. Normally, this efficiency requirement would be easily attained. However, the six cubic inch volume requirement necessitates a high switching frequency to keep the transformer and choke sizes down to an acceptable size. The converter therefore operates at 30kcps. The main losses in the converter are switching losses in the power switching transistors and core losses. These losses are frequency dependent and are slightly higher than in the usual converter.

3.0 Technical Objectives

Electrical:

Frequency Range	2200-2290 Mc crystal controlled
Frequency Stability	± 0.001%
Power Supply	27 volts DC ± 10%, 25 watts

Minimum Power Output	2.0 watts into 50 ohms
Spurious Modulation	Less than ± 5 kc under all conditions
FM Deviation	Linear within 1% for ± 125 kc
Modulation	FM/FM to IRIG 106-60
Input Impedance	10 K shunted by 20 pf
Sensitivity	± 125 kc for 1.0 volt rms
Response	Flat within 1 db from 100 cycles to 100 kc
Spurious and Harmonic Emissions:	
Antenna Conducted	At least 60 db down with transmitter power output of 2.0 watts
Other	MIL-I-6181D
Minimum Efficiency:	
Overall (transmitter + power supply)	8%
Transmitter only	10.7%
Power Supply only	75%
Mechanical:	
(S-Band Unit)	
Volume	6 cu. in. each for transmitter and power supply
Dimensions	1 in. x 1 in. x 6 in. each for transmitter and power supply
(L-Band Unit)	
Volume	7 cu. in. for transmitter
Dimensions	1 in. x 1 in. x 7 in.
Weight	Approximately 1 pound each for transmitter and power supply
Cooling	Conduction
Temperature	-54°C to +95°C
Vibration	20 G's, 20-2000 cps sinusoidal and random in all axes
Shock	15 G's, 11 ms duration in all axes

4.0 Design Approach This section discusses the techniques used to achieve the required technical objectives of the program.

4.1 VCXO Circuit To maintain a frequency stability of ±.001 percent requires that the crystal be very precise. Crystals can be cut with stabilities of ±.0025 percent for this temperature range; therefore temperature compensation must be used in the oscillator. Temperature compensation of an oscillator using an AT cut quartz crystal is not straightforward since the temperature characteristic of such a crystal has an S-shaped curve. The compensating circuit is a resistor-thermistor network designed to give an output voltage having an S-curve shape with temperature. This voltage provides the static bias for the varicaps which corrects the frequency. The actual frequency stability depends upon how closely the curves are matched.

Automatic gain control is used in the oscillator in order to give good frequency stability over the range of modulation voltages and environmental conditions. By using automatic gain control, the drive level is maintained at a low level under all conditions. Gain control is provided by a transistor biasing network. This network causes the base bias voltage to controlled by the collector current.

One of the most important crystal parameters is suppression of spurious modes. In an oscillator of this type, the spurious crystal modes can be excited by the modulation frequency. This phenomenon can become quite complex depending upon the modulation index, but the predominant excitation occurs when a modulation frequency is applied to the oscillator which is equal to the frequency difference between the fundamental frequency of the oscillator and the frequency of the spurious mode. Whenever one of these spurious modes is excited, there is a discontinuity in the modulation response of the oscillator. The frequency response characteristics of this oscillator must be flat within 1 db from 100 cps to 100 kc. Therefore, any spurious modes within 100 kc of the fundamental mode must be deeply suppressed. Such a crystal requirement is feasible in the 20-30 Mc frequency range.

4.1.1 Modulation Network The modulation network of this VCXO is comprised of a capacitive-resistive input circuit and two voltage variable capacitors connected in series as shown in Figure 3. This arrangement provides the required modulation sensitivity with a linearity of 1%.

Frequency modulation of the oscillator is accomplished by pertubing the resonant frequency of the quartz crystal by changing its load capacitance. The frequency modulation of the crystal is performed by the voltage variable capacitors.

Two varicaps connected back to back are used in preference to a single varicap to realize a more linear net capacitance versus voltage characteristic, therefore improving the linearity of the low-level modulator. When both varicaps have approximately equal capacitance values, the signal voltage will be divided equally across each diode, which reduces the amount of distortion. Further reduction in the distortion or non-linearities is obtained because of the compensating effect of the diodes. When the capacitance of one diode is increasing due to signal voltage, the other is decreasing, thus giving a more constant capacitance for the series combination. Connecting the varactors back to back allows lower bias voltages to be used than with a single diode thereby increasing the useful tuning range of the circuit.

4.1.2 Temperature Compensating Network The temperature compensating network is designed to maintain an oscillator frequency stability of ± 0.001 percent over the specified temperature environment. The network is basically a voltage divider circuit in which the output voltage varies with temperature. This output voltage is used to bias the varicaps in the feedback loop of the oscillator. Thus as the temperature changes, the varicap bias voltage also changes, which in turn corrects the oscillator output frequency. The basic problem in designing the voltage divider circuit is that the output voltage versus temperature curve should be a “mirror image” of the S-curve of the AT quartz crystal with the voltage peaks limited so that the oscillator is not over compensated. Figure 4 shows the temperature characteristic of an AT cut crystal.

The voltage cividerr circuit is shown in Figure 5. The input voltage to the divider circuit has to remain constant over the temperature range, so a zener diode is used to supply this voltage. The temperature coefficient of the zener diode was selected to be ± .001 percent/°C to decrease effects of the input voltage varying with temperature changes. Since the supply voltage to the oscillator is ±15 Vdc, a zener voltage somewhat lower than this value was needed. A diode with an 8.4 volt zener voltage at 10 ma was chosen. The voltage deviation over the temperature range due to the zener diode is approximately ± 13 mv. The high zener current was chosen in order to keep the effect of the change in current drawn by the compensating network small.

Referring now to the compensating network shown in Figure 5, and using the data obtained experimentally, it is now possible to calculate all values of the components used in the network. The value of the thermistor RT1 is chosen so that its minimum value will not cause the network to draw more than 5 percent of the zener current. Also, its value cannot be too high because of the leakage current of the varicaps. Therefore, a GE type ID053 was selected with these considerations in mind. Its nominal values are 10 K at 25°C, 680 ohms at +95°C, and 950 K at -55°C. Shown in Figure 6, is a sketch of the voltage characteristic of the compensating network as compared to the AT cut crystal temperature versus frequency characteristic. Since at the end points, the curve of the oscillator characteristic peaks and changes direction while the voltage divider network

characteristic levels off asymptotically, it was decided to under-compensate the oscillator slightly.

4.1.3 Oscillator Circuit The oscillator portion of the VCXO circuit is shown in Figure 7. The circuit is a variation of the Colpitts type crystal oscillator. The amplifier section of the oscillator is operating class A in a common-emitter circuit. The feedback loop of the oscillator is a low-impedance, series-tuned circuit driven from a low impedance point provided by the capacitive voltage divider C4 and C5 which also sets the amount of feedback voltage. The loop consists of a fundamental mode series-resonant quartz crystal, two voltage variable capacitors connected in series, a variable inductor, and a variable transformer across the crystal. Capacitor C1 serves as a DC blocking path. Capacitor C6 is used to couple power from the oscillator to the multiplier stage. Its value is selected to keep the power output obtained from the oscillator low in order to maintain good long term stability.

The crystal used in this oscillator is a micromodule unit. This type is used because it is the smallest crystal available at the present time in which the necessary characteristics could be obtained.

4.1.4 Frequency Doubler The circuit of the X2 frequency multiplier is shown in Figure 8. The common base configuration is used because it has been found to achieve the best performance, and it provides better isolation of the oscillator stage from the other stages of the transmitter, thus minimizing the effect on the frequency stability of the oscillator due to load variations.

4.2 Power Amplifiers Power Amplifiers are used in two stages of the transmitter, at 182 to 191 Mc and 366 to 382 Mc. The driver amplifier, 182 to 191 Mc, is operated Class A to achieve high gain and temperature stability. The common emitter configuration is used because it provides the most stable amplifier, and advantage may be taken of negative T. C. thermistors to compensate the beta temperature sensitivity.

The final power amplifier is operated at 366 to 382 Mc, which is considered close to the highest practical limit for state-of-the art transistors of several watts RF output capability. On the other hand, the advantages of operating at the highest practical frequency are:

1. Fewer varactor stages needed.
2. Overall efficiency improvement.
3. Easier impedance matching.

4.2.1 Design Analysis In the design of power amplifiers, several circuit conditions are usually given. For instance, the collector voltage, the RF output power, the required power gain, and the operating frequency, are generally specified by the choice of system parameters. Once these are given, the transistors for each stage may be selected. other considerations such as amplifier configuration and maximum operating temperature will affect the choice to some extent.

For the design under consideration, the RCA 2N3375 transistor was chosen for its superior performance at UHF frequencies. The vendor specifications give V_{CBO} and V_{CEV} as 65 V minimum. Since under saturated conditions the AC collector voltage can swing to 2 V_{CC}, a choice of 1/2 V_{CEV} for V_{CC} is a practical limit. In this case 30 volts was chosen to give collector breakdown margin. Once V_{CC} is chosen, the transistor output capacitance, impedances, and collector efficiency can usually be determined from the device data sheet.

4.2.2 Driver Amplifier According to the previous selected system parameters, the operating conditions for the driver are as follows:

1. Operating frequency - 190 Mc nominal
2. RF Output Power - .5 watts
3. Power Gain - 8 db

The common emitter circuit was chosen for stability and temperature compensation reasons. The stage is operated Class A for maximum gain.

4.2.3 Bias Circuit The transistor bias circuit is shown in Figure 9. Some assumptions must be made in order to establish the collector current and emitter resistance. These assumptions are: That the collect efficiency is in the range from 25 to 35 percent for Class A, that the emitter resistor voltage VR3, is five times the base-emitter drop V_{BE}, and that V_{BE} = .8V. The actual collector efficiency assumed here is 33 percent. Vendor data shows that the gain of this device is 11 db typical at this power level, assuming matched conditions. This verifies that at least 8 db gain should be obtainable while allowing some mis-match in the interest of stability.

4.2.4 Thermistor Compensation The performance of the driver amplifier is shown in a subsequent section. However, the amplifier gain over the required temperature range, -54° to +95°C, changed an unacceptable amount. This was due to a change in DC beta, H_{FE}. The transistor bias resistor R_2 was therefore replaced with a thermistor and a fixed resistor. The value of the thermistor and fixed resistor had to be determined empirically since no Vendor data was available showing the DC beta temperature characteristic.

4.2.5 Final Amplifier The final power amplifier must produce a nominal output of six watts. The operating frequency is 366 to 382 Mc. The vendor's data shows that approximately 6 db power gain is typical in this frequency range with 28 V applied to the collector. The common base arrangement is used here since the available gain is higher than for the common emitter configuration at this frequency. The lower common-emitter gain is caused by degeneration due to the emitter lead inductance.

Vendor's data also shows a minimum Class C efficiency of 40 percent at 400 Mc with three watts RF output power. Based on experimental lab results, the power stage collector efficiency is approximately 50 percent.

The total dissipation then is:

$$P_D = P_{DC} + P_1 - P_o = 12 + 1.5 - 6.0 = 7.5 \text{ watts}$$

Where P_1 = stage RF input power and P_{DC} is the DC input power.

The device capability is 11.6 watts at 25°C case temperature. Using the Maximum environmental temperature, 95°C, the dissipation per transistor P_T, is

$$P_T = P_{25}\frac{(T_m - T_H)}{T_m - 25} = 11.6\frac{(200 - 95)}{200 - 25} = 7.0 \text{ watts}$$

where T_m is maximum junction and T_H is maximum case temperature. Thus the final stage requires two transistors if margin is allowed for operation at the maximum environmental temperature. This stage was compensated by the use of sensistors (i.e. positive temperature coefficient thermistors), in the emitter circuit.

4.3 Multipliers The multipliers used in the transmitter utilize both transistors and varactors. As stated before the multiplications are limited to X2 and X3 for circuit simplicity and space saving reasons. The low frequency multipliers use transistors entirely since gain may be achieved by their use and fewer components are needed. Any efficiency improvement provided by transistor amplifier-varactor multiplier combinations is more than offset by their increased circuit complexity.

The use of the varactor at the higher frequencies and power levels is necessary however, if appreciable power must be generated at S-Band with solid-state devices.

4.3.1 Transistor Multipliers There are four transistor multipliers used in the transmitter; all are doublers. Two follow the VCXO module, one from 47.5 to 95, and another from 95 to 190 Mc. The fourth is used to drive the final amplifier and doubles the frequency from 190 to 380 Mc.

The input doubler is forward biased to give additional gain while the following doublers are driven into Class C operation by the signal. Collector compensation must be used in multipliers rather than in the base or emitter, since the conduction angle is quite critical.

4.3.2 Varactor Multipliers The important considerations in the design of narrow band varactor multipliers are:

1. Conversion efficiency
2. Spurious Suppression
3. Bandpass stability

An additional prime consideration here is volume requirement. Several circuit conditions are usually specified in the design, operating frequencies, power levels, required efficiency, and spurious suppression.

The transmitter uses two varactor multipliers, a tripler from 380 Mc to 1140 Mc, and a coaxial cavity doubler from 1140 Mc to 2280 Mc nominal. Both multipliers are of the shunt type with series tuned input and output. Fixed bias is used in each multiplier for tuning and temperature stability.

4.3.3 Tripler Multiplier The requirements for the tripler are:

1. Input operating frequency - 380 Mc nominal
2. RF output power - 3. 7 watts
3. Conversion efficiency - 62 percent

The basic circuit of the tripler is shown in Figure 10. First the varactor parameters must be determined based on the system requirements. The important varactor parameters are: Capacitance at breakdown C_m, breakdown voltage V_B, and cutoff frequency f_c. The impedance levels are dependent on C_m and f_c, but their choice is somewhat arbitrary. However, some restriction should be placed on output impedance levels chosen since the matching losses are increased if this impedance is too low.

4.3.4 Coaxial Cavity Doubler The final multiplier is of the shunt type with foreshortened quarter wave coaxial cavities at input and output. The original concept is shown in Figure 11. The only necessary modifications were a reduction in the amount of rexo1ite supporting material, and adjustment of the coupling loops. The piston capacitors were larger than necessary when first constructed. This allowed an overall reduction in cavity length of .225 inches which was needed in the UHF circuitry compartment.

4.4 Power Supply The power supply is a DC-DC converter which accepts unregulated battery voltage and efficiently converts it to the regulated voltages required to operate the transmitter.

4.4.1 Technical Goals The DC-DC converter has a maximum volume of 6 cubic inches, with a 1 in. x 1 in. x 6 in. configuration. It must consume less than 25 watts from a voltage source of 27 volts ± 10 percent. Operation is required from -54°C to +95°C, with a demonstrated-starting capability over the temperature range. The outputs required by the transmitter are:

+30 V	@	600 ma	Or	18.0 watts
+15 V	@	33 ma	Or	0.5 watts
-50 V	@	2 ma	Or	0.1 watts
			Total	18.6 watts

Based on the required output power and the maximum available input power, the conversion efficiency is required to be equal to, or greater than, 74.5 percent. Allowable weight of the converter is 2.0 pounds maximum.

4.4.2 General Approach There were several factors which entered into the selection of the method of conversion. The factor given prime importance was volume. The 1 in. x 1 in. x 6 in. package was to be attained regardless of other tradeoffs. The efficiency requirement necessitated a variable pulse width type converter with its inherent high efficiency. The package form factor required that the output transformer, the largest single component, fit within the 1 in. x 1 in. package cross section. This required a transformer no greater than 0.85 inches in diameter. The only was to attain this small OD was to operate the converter at a relatively high frequency, which introduced a significant tradeoff. Since size was of first importance, the high frequency was chosen. However, the major losses in this type converter, assuming relatively high output voltage and good rectification efficiency, are transformer losses and switching losses in the power transistors. These losses increase with frequency.

The particular technique used will be explained with reference to Figure 12, which is a block diagram of the DC-DC converter. Primary power is applied to alternate sides of the output transformer primary by means of the power switches, which are transistors operated either in the saturated or cutoff region. These s switches are in turn driven by the pulse width switches.

When rectified and passed through a lowpass filter, the resultant DC voltage is V_{pt}/T. If the numerator, or area under the pulse, is constant and the period between pulses, T, and constant, the result will be a regulated output voltage. This discussion uses V_p, or

transformer primary voltage. However, it applies equally well to any winding on the transformer if the result is modified by the transformation ratio of that particular winding to the primary. The remainder of the blocks in the diagram function in such a manner as to assure that the relationship between the three basic variables, V_p, t, and T, is such that the DC output remains constant.

The square wave oscillator establishes the frequency at which the converter operates and alternately drives the pulse width switches. The quantity T corresponds to half the period of the square wave oscillator. During this time, the oscillator provides drive to one of the pulse width control switches which remains on until turned off by the pulse width control element. The pulse width control element is a square loop core which senses input voltage and is driven to saturation in opposite directions. Saturation of this core terminates drive from the pulse width switch to the power switch. The volt-second capability of the core is thus used to maintain the $V_p t$ product constant. Therefore, if the volt-second capacity of the core and the sqifare wave oscillator frequency are constant, the desired result of a regulated output voltage is attained. However, the saturation flux density of the core changes with temperature and will vary the $V_p t$ product. Therefore, to compensate for temperature effects and provide initial adjustment an output is compared to a reference and any error used to vary the square wave oscillator frequency to maintain the output at a constant level.

Figure 13 is a photograph of the breadboard of the final circuit. The two TO-5 cans in the center of the breadboard were later incorporated into a single TO-5 package utilizing the same semiconductor device.

Figure 14 illustrates the transformer waveshapes.

5.0 Present Package Design As a result of the thermal design studies, the following techniques are used in the package design:

5.1 Transmitter The single vertical wall of this chassis is 0.125 inches thick, while the base is 0.060 thick. Most of the heat producing units are mounted on the thicker wall which provides a good thermal path to the heat sink.

The 2N3375 power transistors are mounted directly on the chassis wall without insulating shims. The smaller transistors are bonded to alumina oxide cups which are attached to the wall. The encapsulated VCXO module is mounted directly to the chassis wall for good heat conduction. The chassis is machined from a solid block to eliminate thermal resistance at joints.

5.2 Power Supply The base of this chassis is 0.100 inches thick and the walls are 0.050 inches thick. These dimensions are increased in certain areas to provide more volume for good heat conduction.

The two encapsulated modules are mounted directly to the chassis base with flat head screws. The power transformer encapsulated module is provided with a metal base plate and center stud. This not only aids in the construction of the module but provides an efficient means of cooling the transformer by heat conduction from the metal base plate to the chassis base. A center wall is provided immediately adjacent to the power transformer for strength and heat dissipation.

The power supply is dip brazed aluminum, gold plated, and the transmitter is solid aluminum, gold plated.

6.0 EMC Considerations The EMC-RFI design objective for this equipment is MIL-1-26600 and MIL-1-6181D. These two specifications are essentially identical.

6.1 Power Supply Preliminary investigation of the breadboard power supply showed the highest level to be 123 db on the unfiltered +27 vdc: primary power line at about 12 Mc. Filtering for this line was developed to obtain 90 db attenuation at this frequency.

The secondary DC power output lines required less attenuation than the primary power input since the interconnecting lines from the power supply to the transmitter will be short compared to a wave length at the frequencies being generated in the power supply. Thus filters with attenuations of 50 db to 60 db at the low frequencies were required.

The power supply chassis has been designed with a single seam. The main chassis is a brazed unit and the cover has a right angle step constructed to be a press fit into the chassis. This type of construction gives at least 80 db of shielding to the power supply frequencies.

The audio frequency susceptibility requirement of the power supply is met by the feedback loop and the lowpass output filters.

6.2 Transmitter The transmitter EMC design required high frequency filtering and shielding. The lowest frequency associated with the transmitter was 20 Mc. The highest frequency was 2290 Mc, and the strongest signal power level was six watts at 380 Mc.

This required that the transmitter case attenuation be a minimum of 65 db. Screw spacing of 3/8 inch with a 30 mil step in the cover, to decrease the possibility of straight through

holes in the seam, was the design chosen. The step in the cover was held to close tolerances so that it is almost a press fit into the main chassis.

The power line filters for the transmitter are pi-section with a small distributed LC feedthru in the chassis wall as the final element.

The transmitter spurious output was specified separately in the equipment specification to be 60 db down from 2.0 watts. This requirement necessitates the use of dual cavities in the final multipliers and traps in the low-level multipliers stages for suppression of the low order sidebands.

7.0 Conclusion Although the tests of the packaged prototype models are incomplete, the testing of the breadboarded circuits is sufficient to prove the basic potential and feasibility of the design. On a breadboard basis, all the design goals for the VCXO circuit were met. The overall output power and efficiency for the transmitter were met. The spurious suppression was marginal, however, improvement in this respect is expected. The power supply goals were met or exceeded.

The authors wish to acknowledge with appreciation the contributions of Mr. T. B. Jackson of the Naval Ordnance Laboratory during the progress of this development.

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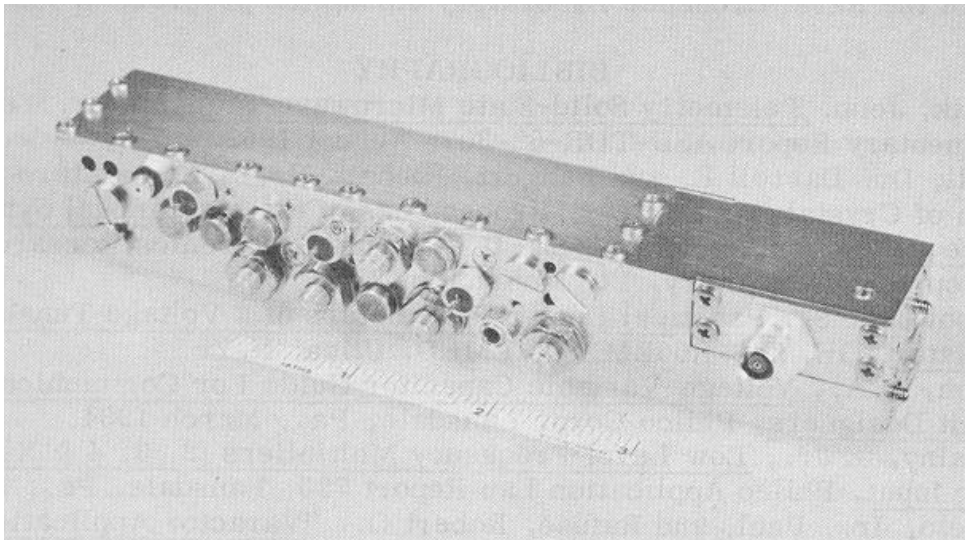
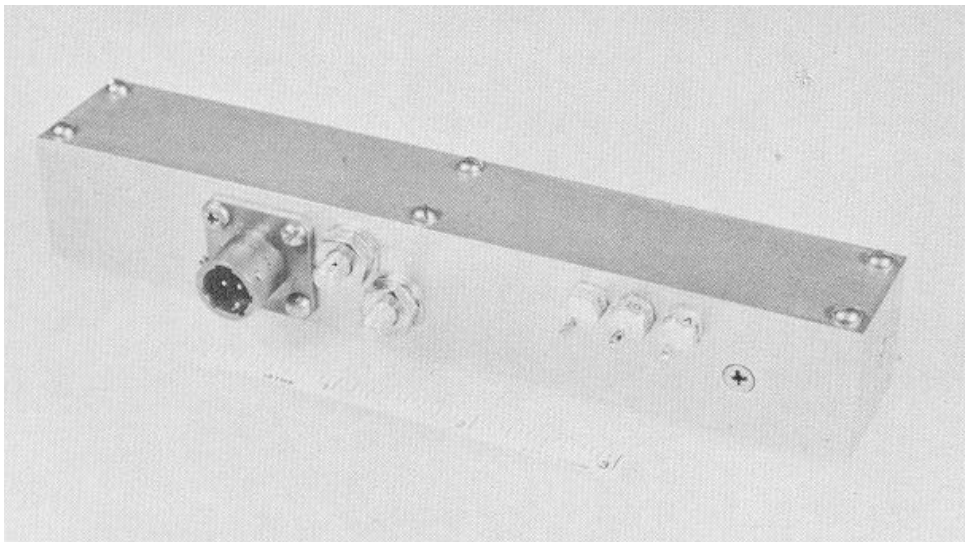
Appendix - Figures 15 through 22 contain a sample of data which shows the current status of development of the program.



TRANSMITTER



POWER SUPPLY

Figure 1. Miniature UHF Telemetry Transmitter

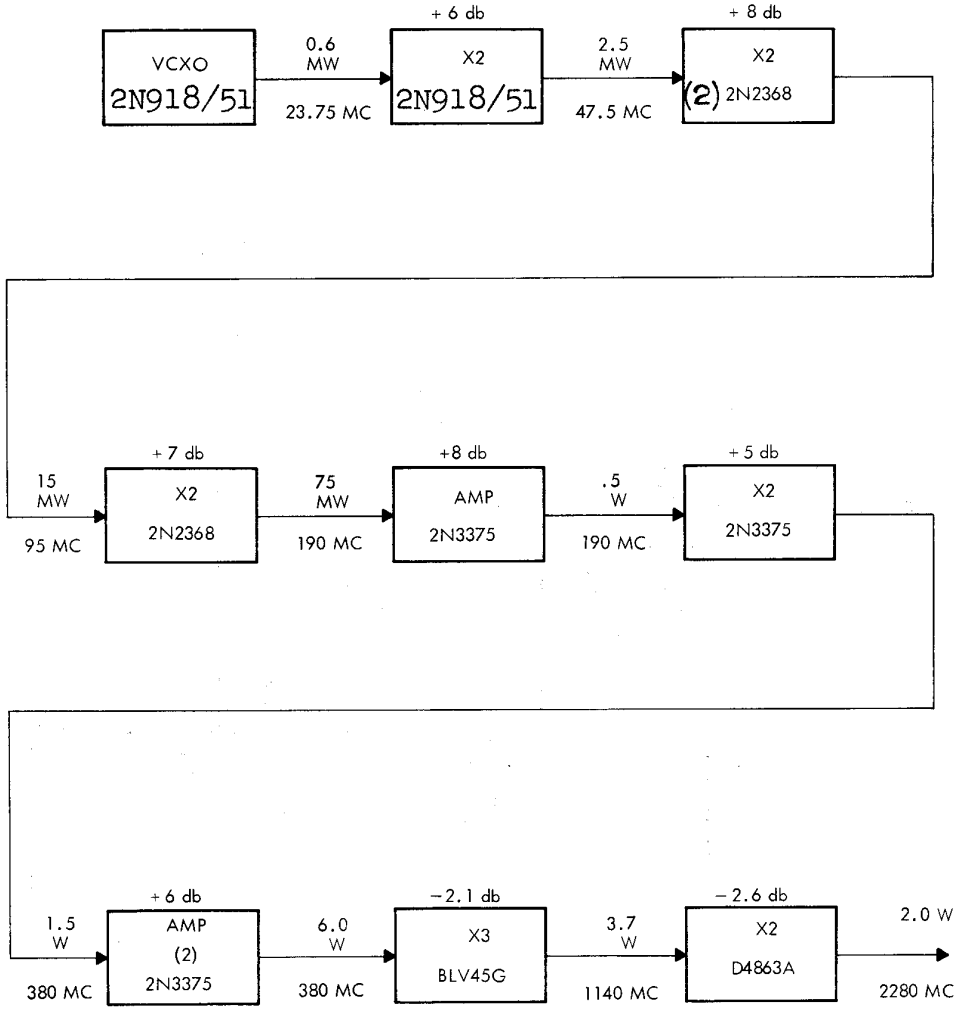


Figure 2. Transmitter Block Diagram

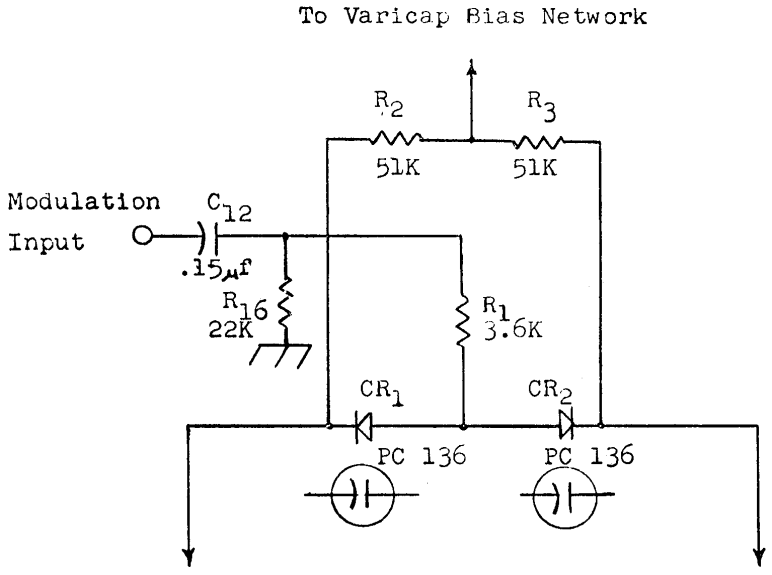


Figure 3. Modulation Net Work

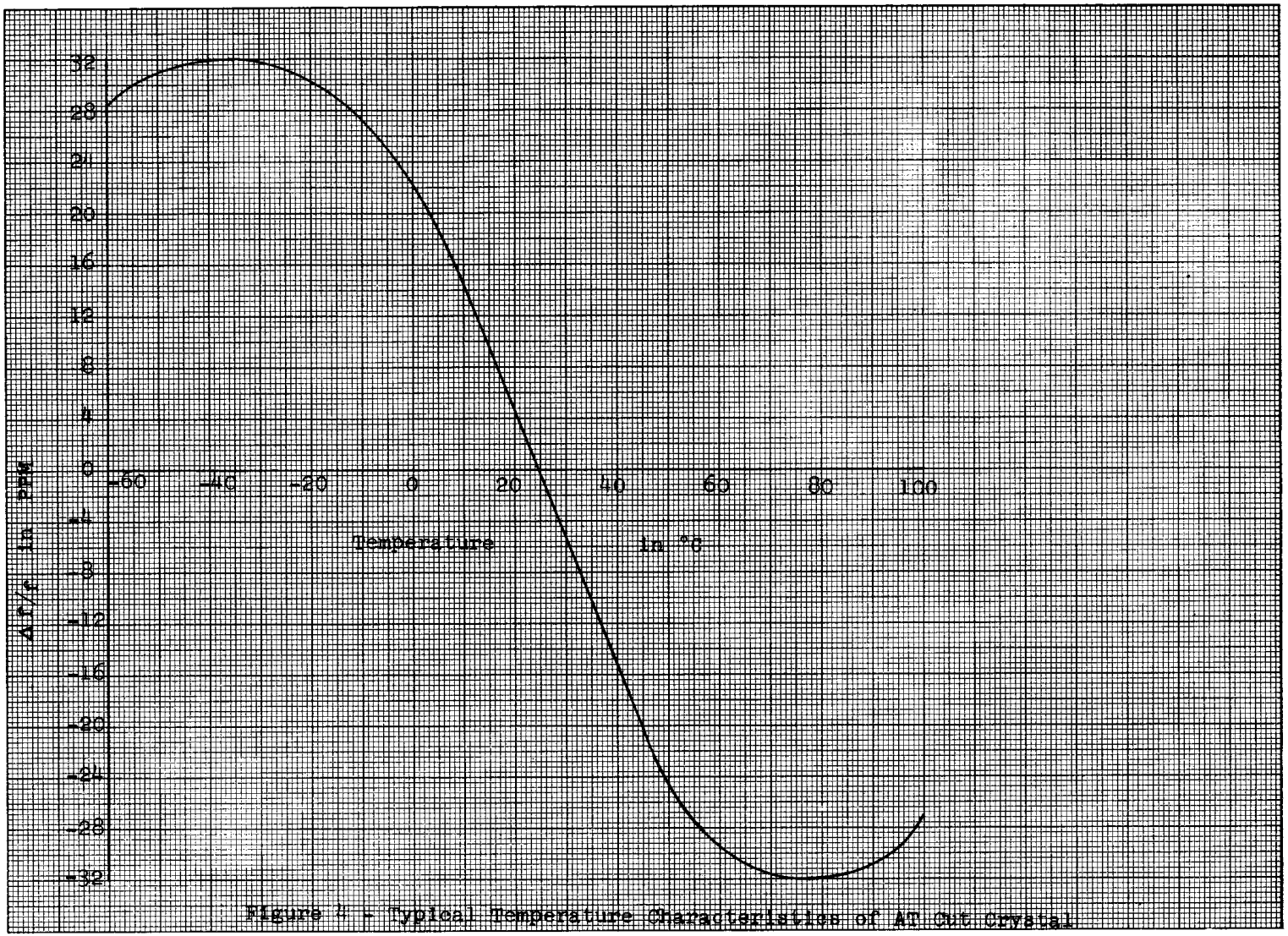


Figure 4. Typical Temperature Characteristic at AT Cut Crystal

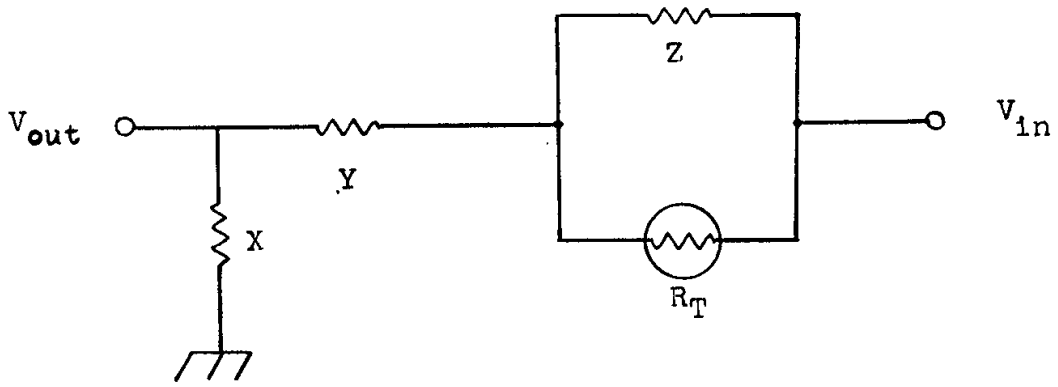


Figure 5. Temperature Compensating Voltage Divider Circuit

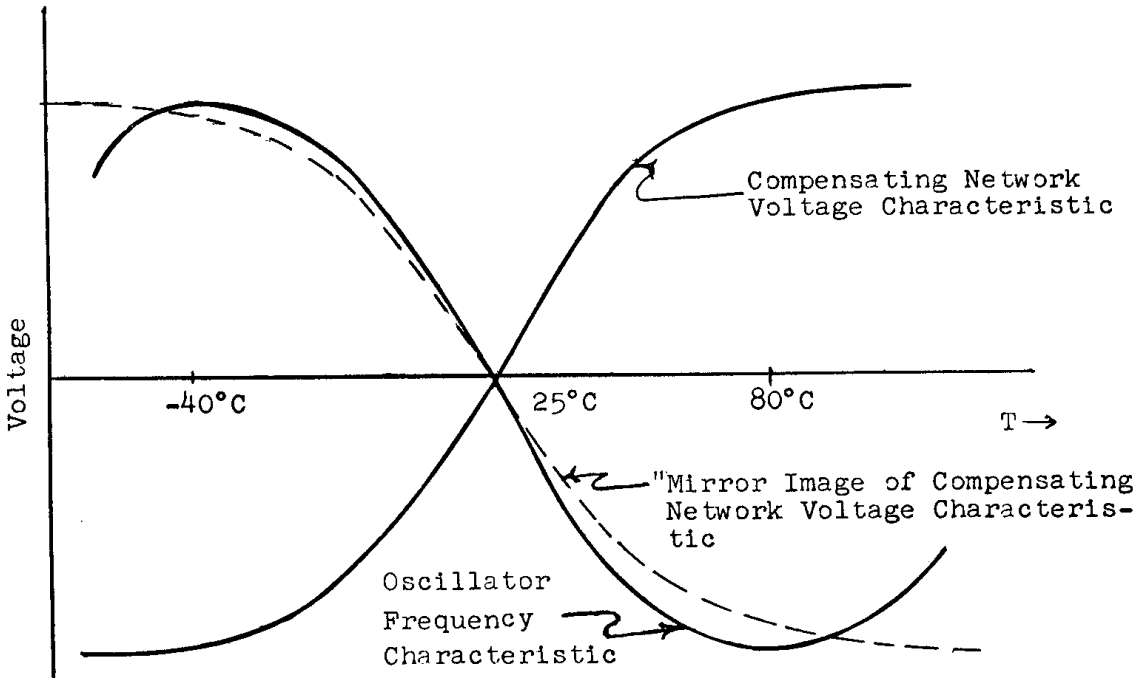


Figure 6. Compensating Network Voltage vs Temperature Characteristic

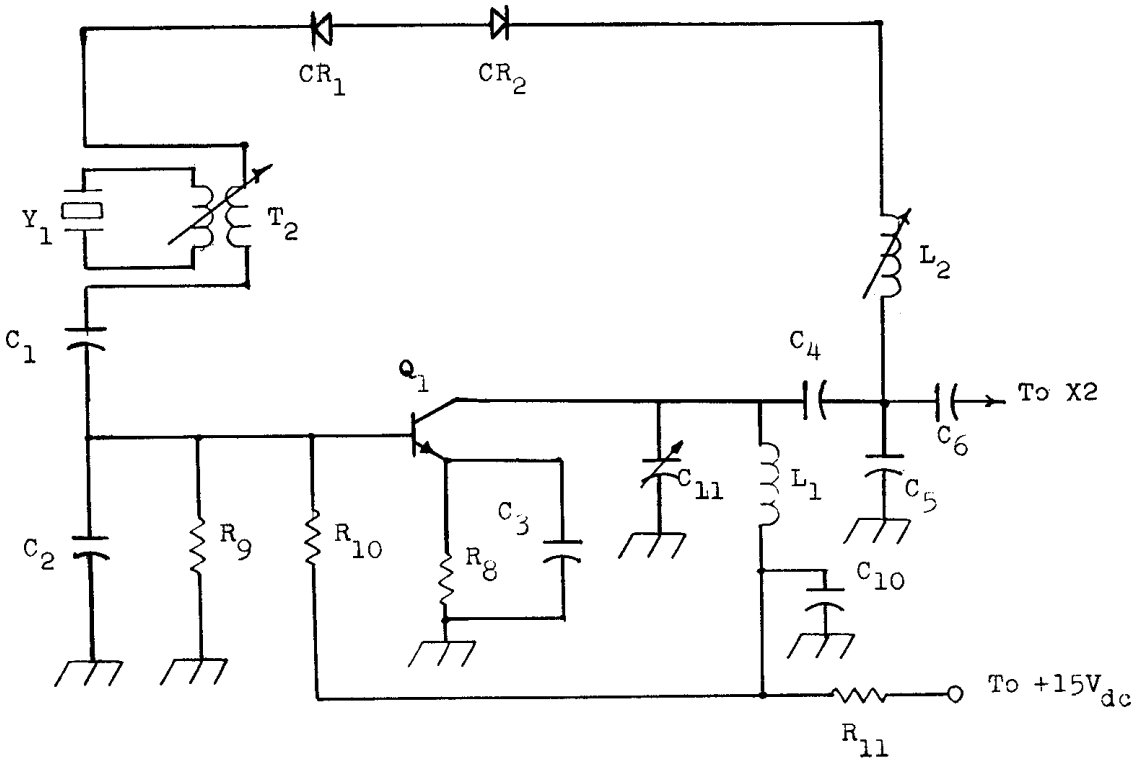


Figure 7. Oscillator Circuit

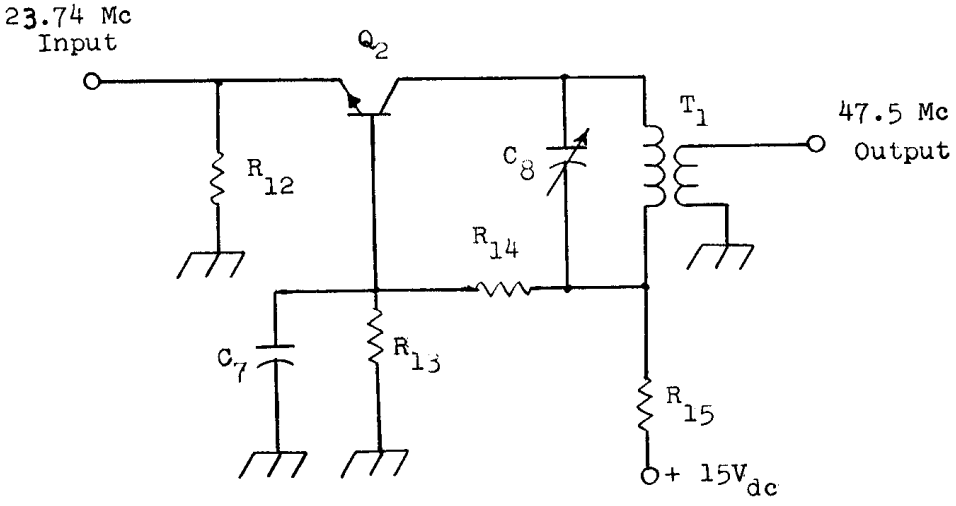


Figure 8. Frequency Multiplier Circuit

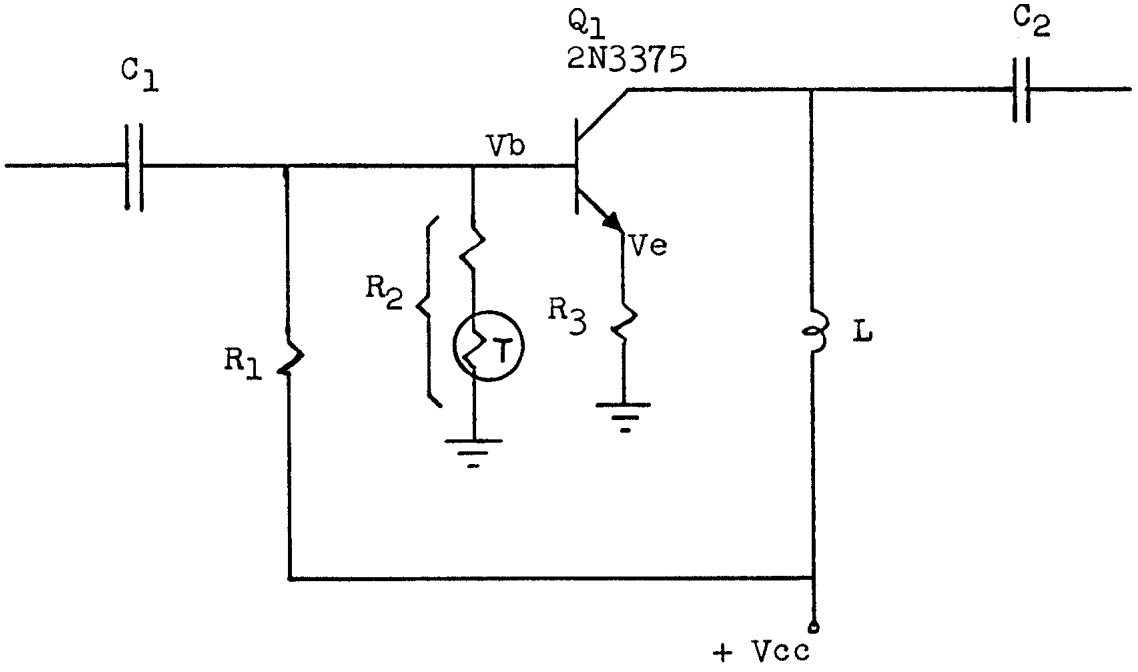


Figure 9. Bias Circuit

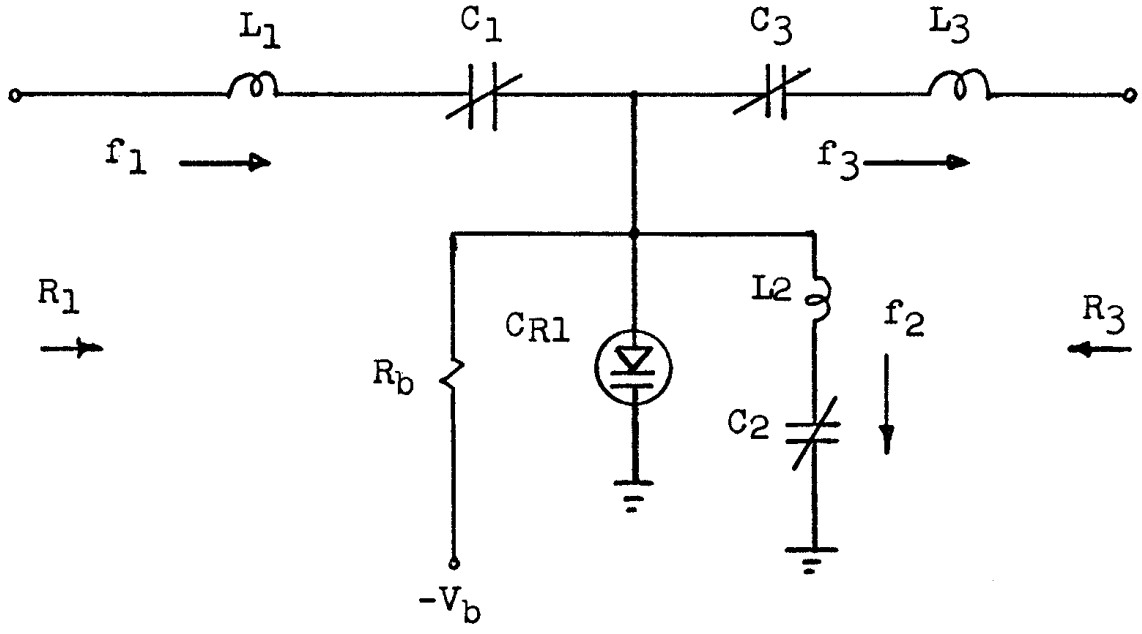


Figure 10. Tripler Circuit

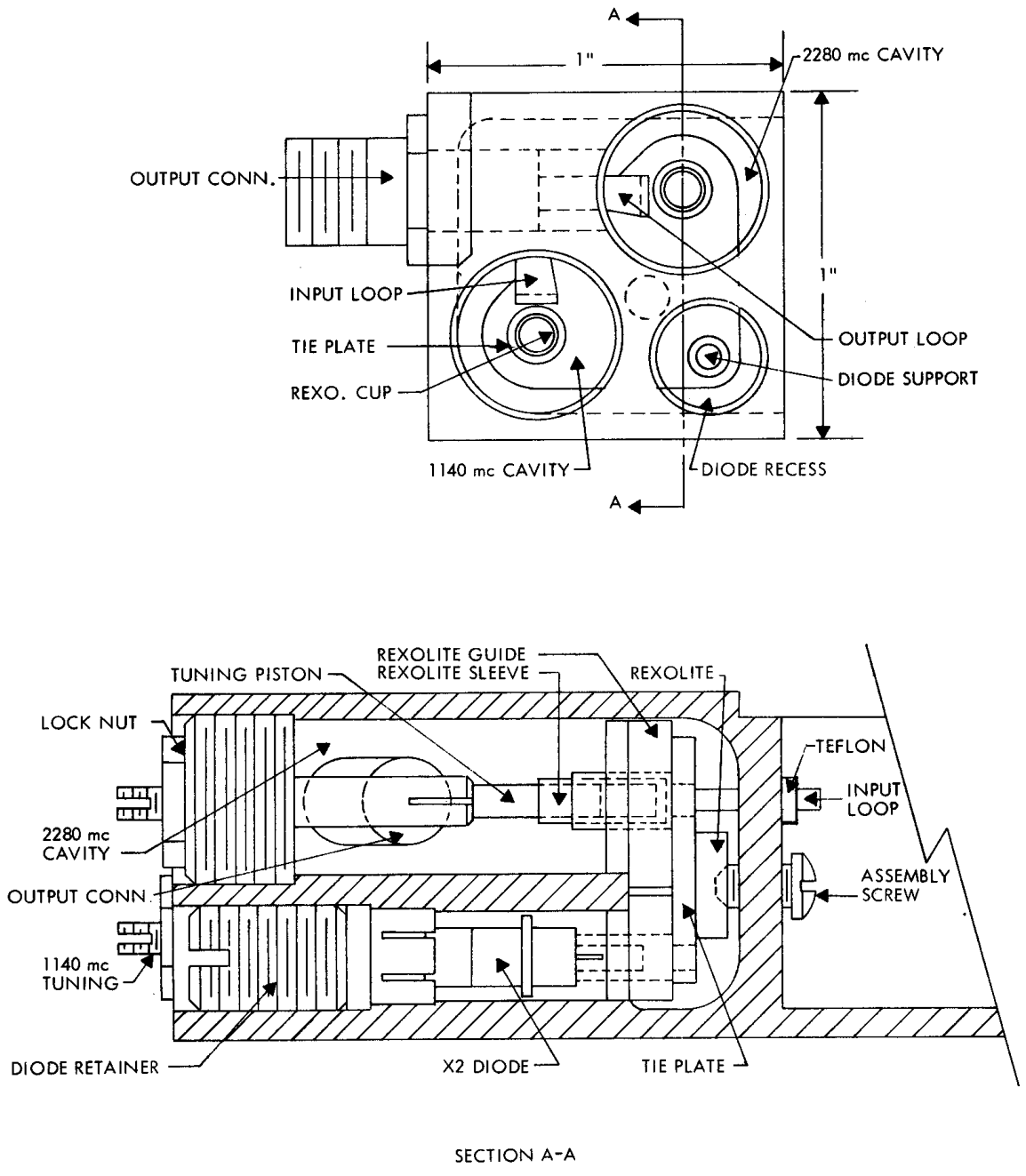


Figure 11. Transmitter Cavity Detail

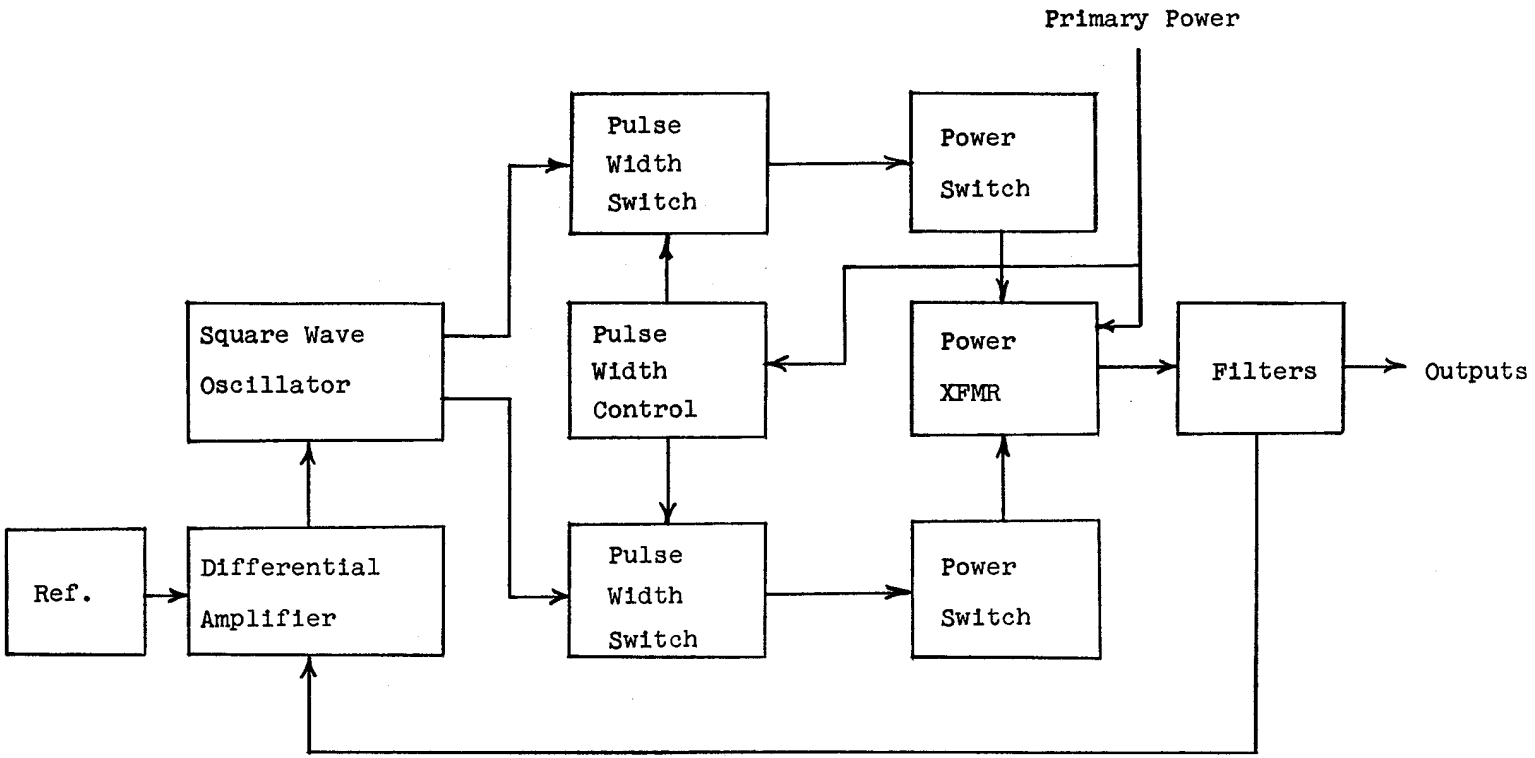


Figure 12. DC-DC Converter Block Diagram

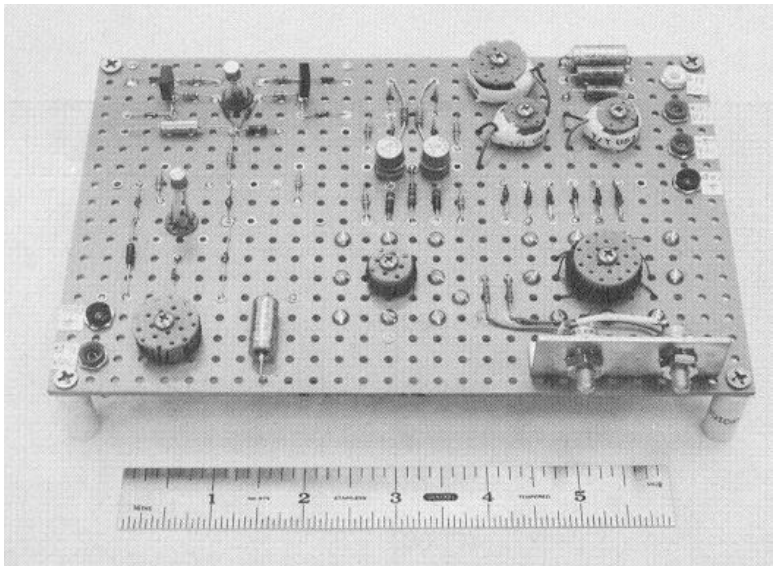
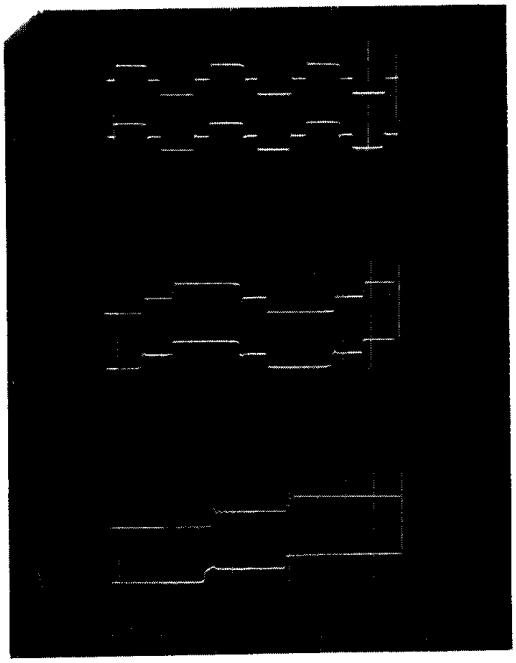


Figure 13. Breadboard of Final Circuit



10 μs/div.

5 μs/div.

2 μs/div.

Transformer voltage waveshapes on the final breadboard. The upper waveshape is the power transformer, whereas, the lower waveshape is the saturating transformer. The vertical scale is 50 V/div. in all cases. Note the 0.4 μs delay between the two waveshapes.

Figure 14. Transformer Voltage Waveshape

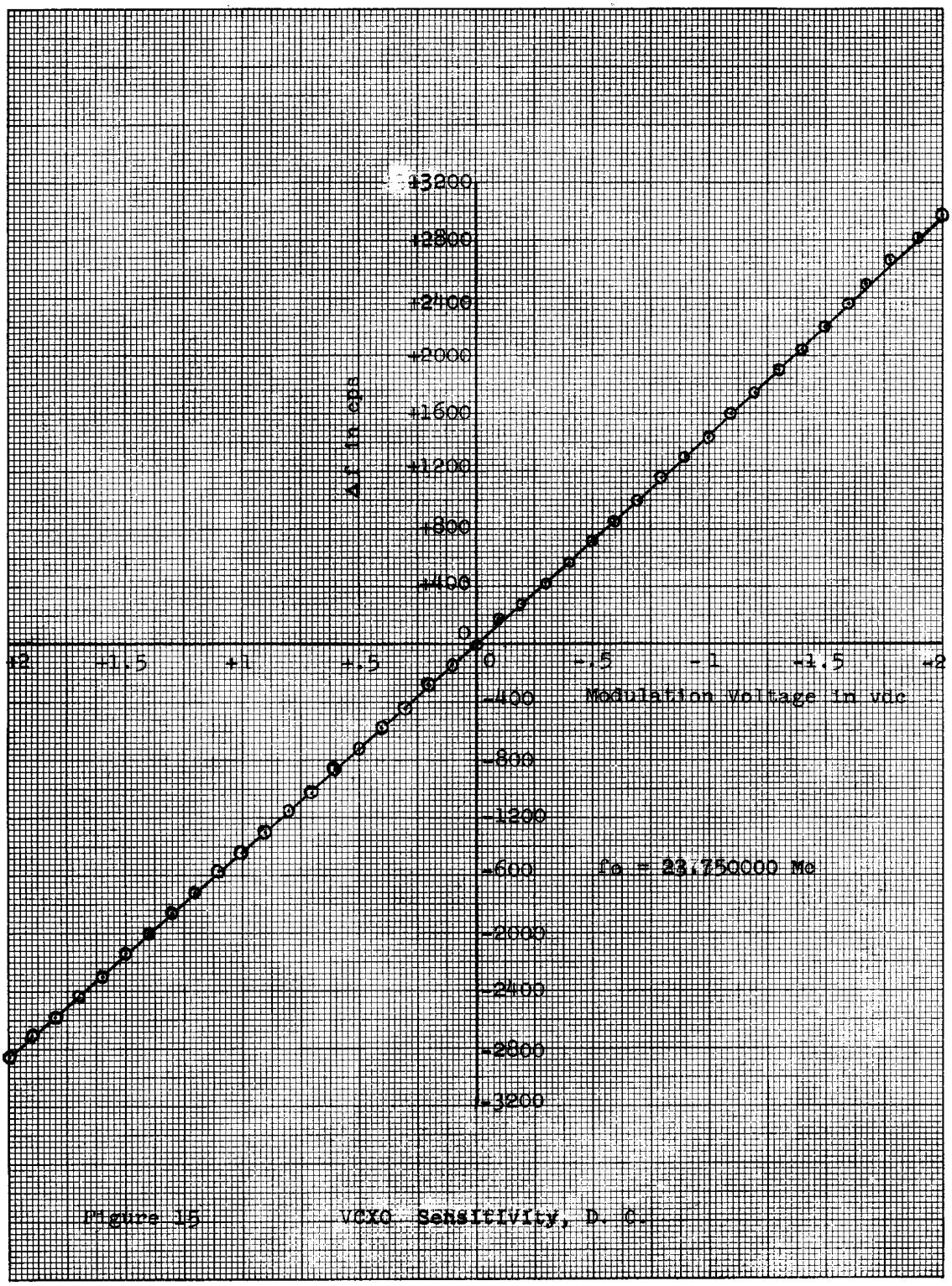


Figure 15. VCXO Sensitivity, D.C.

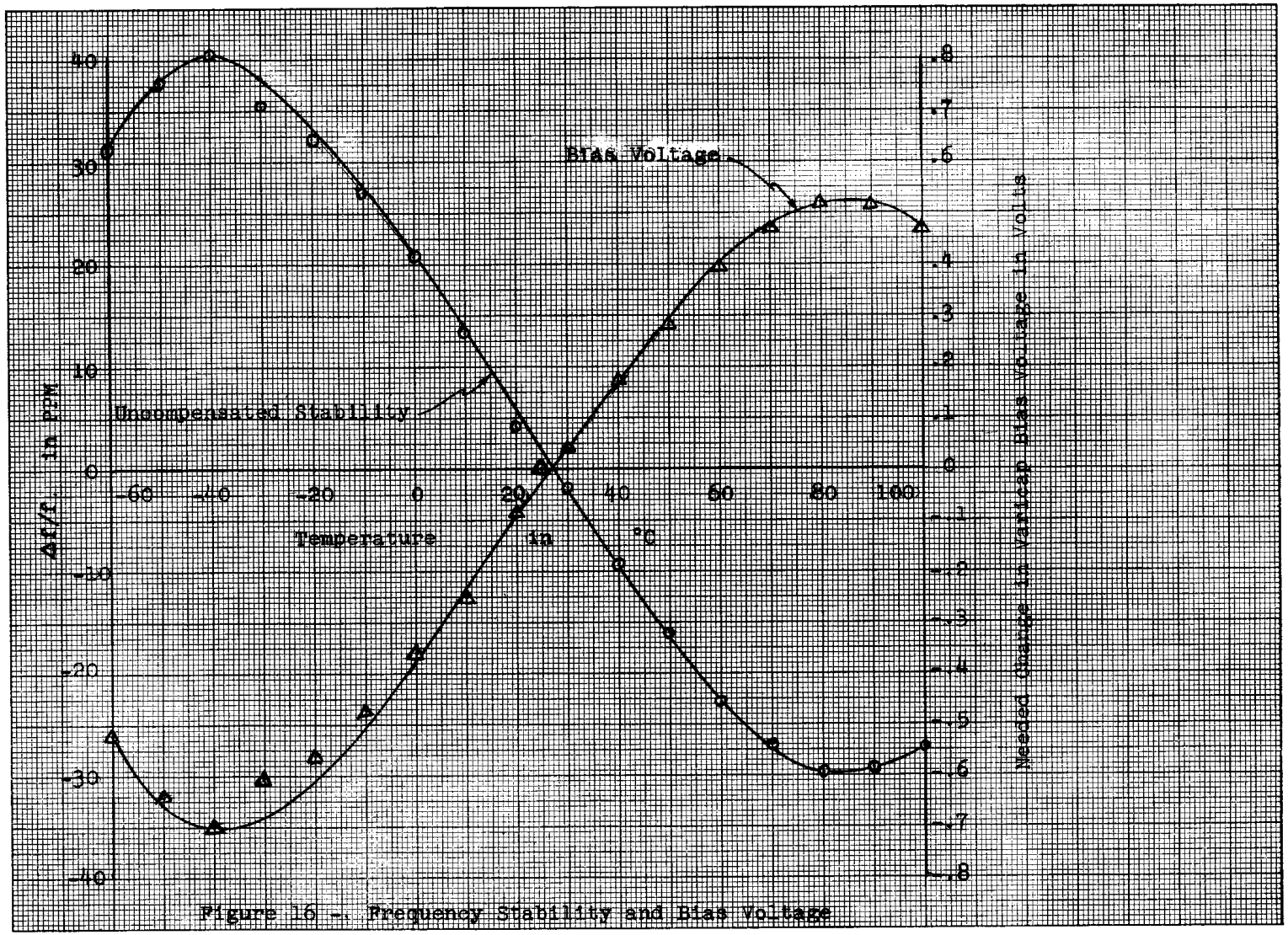


Figure 16 -. Frequency Stability and Bias Voltage

Figure 16. Frequency Stability and Bias Voltage

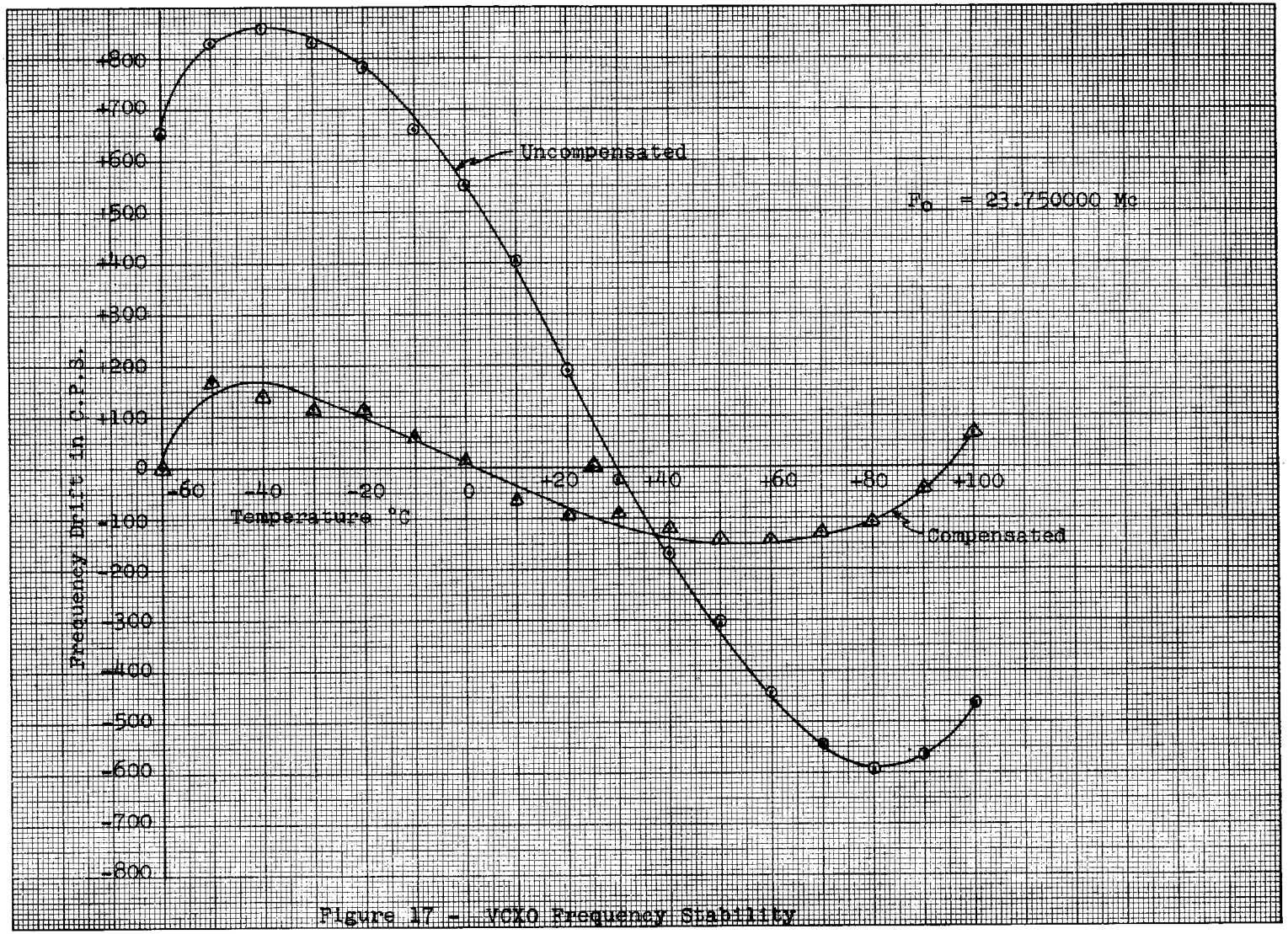


Figure 17. VCXO Frequency Stability

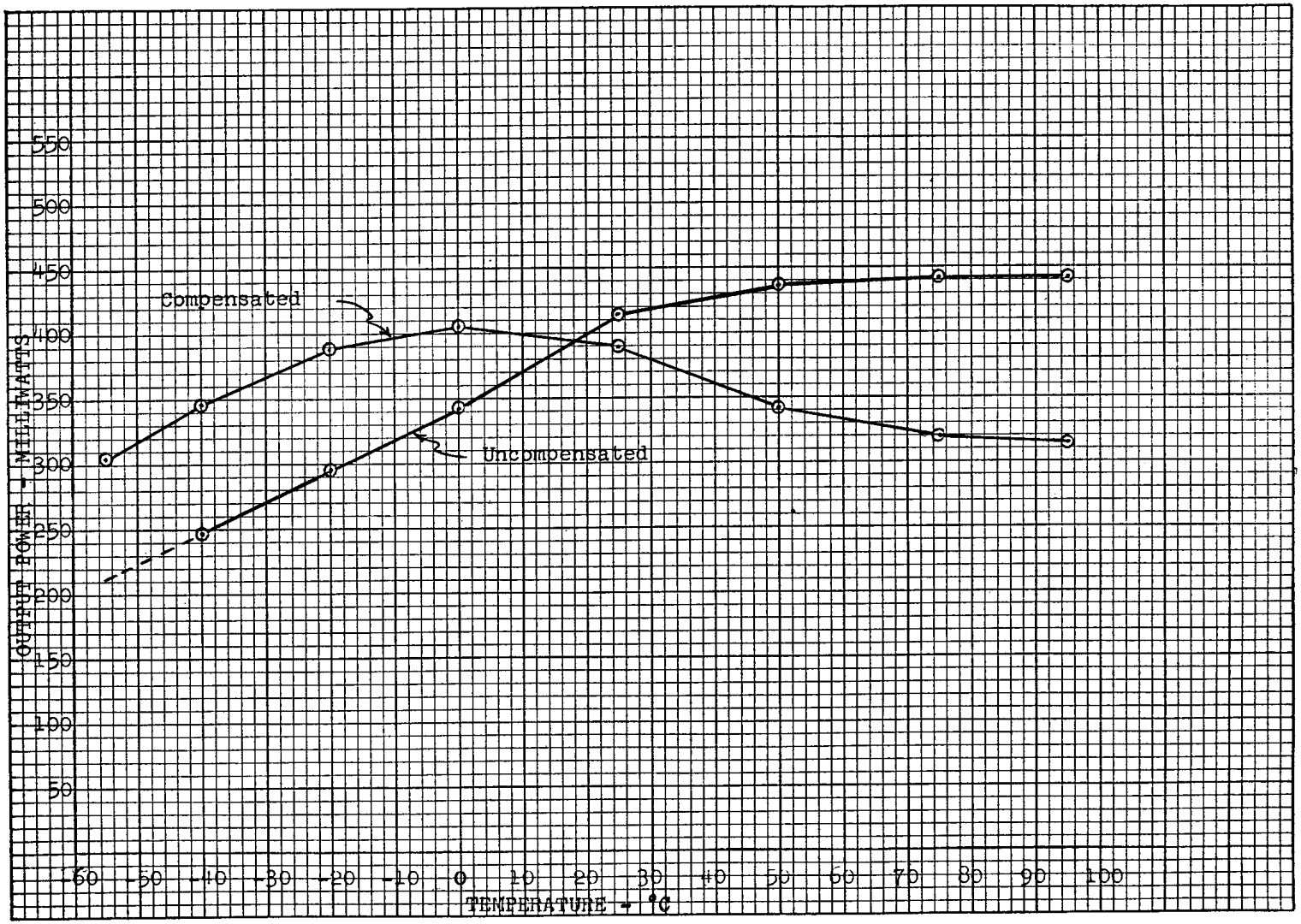


Figure 18. 190 Mc Amplifier, Output vs Temperature

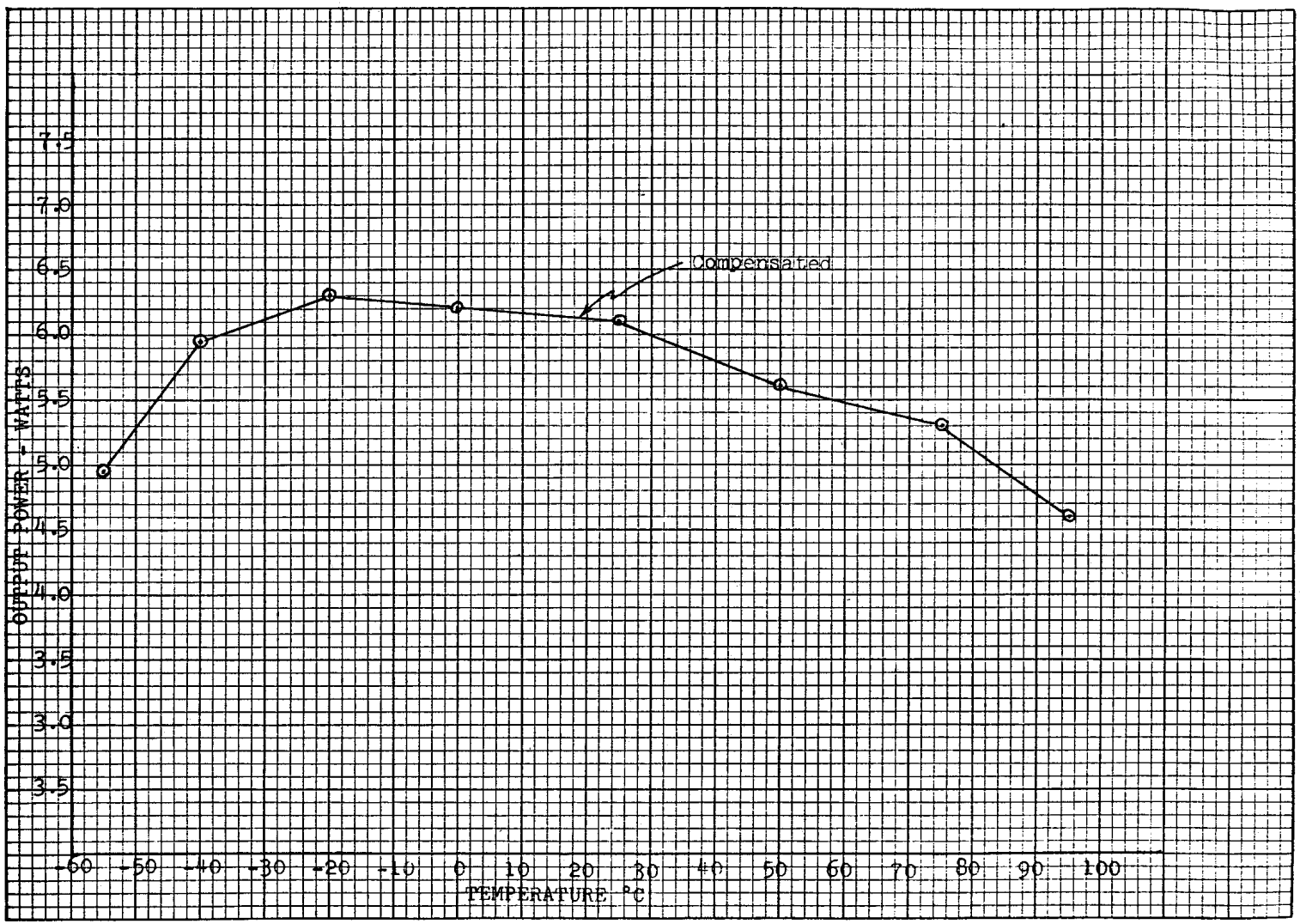


Figure 19. Transmitter Output Through Final Power Amplifier

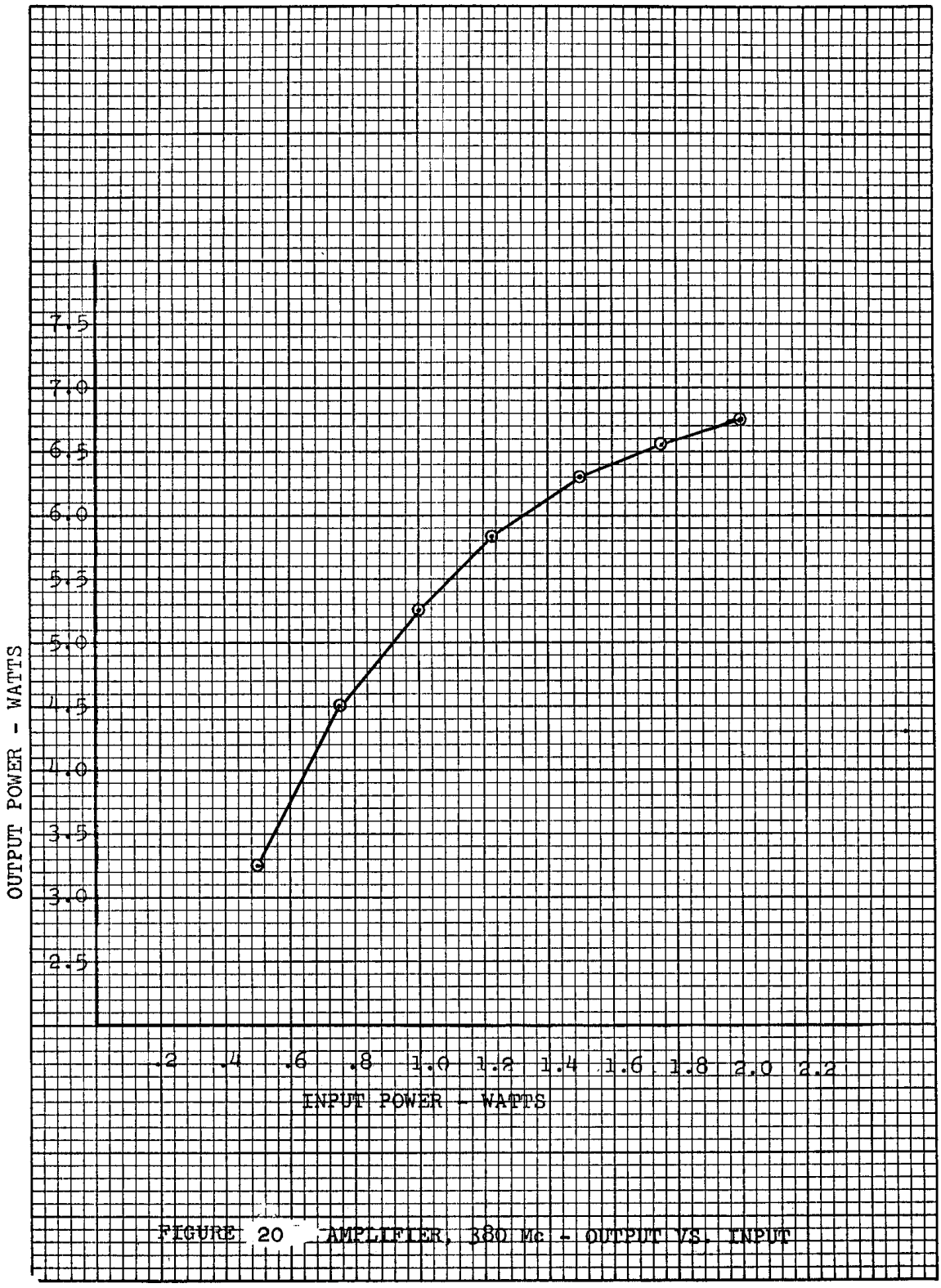


Figure 20. 380 Mc Amplifier, Output vs Input

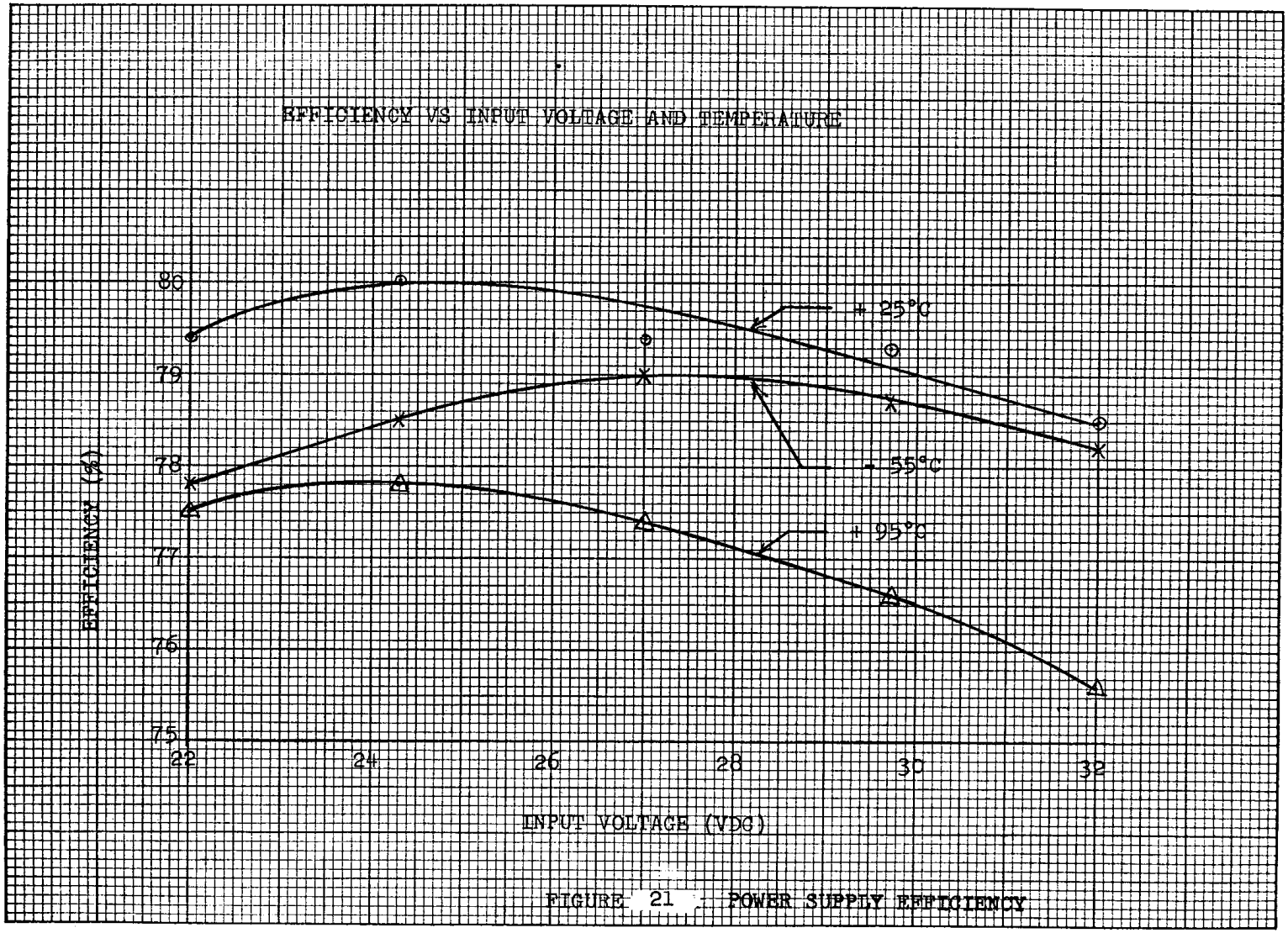


Figure 21. Power Supply Efficiency

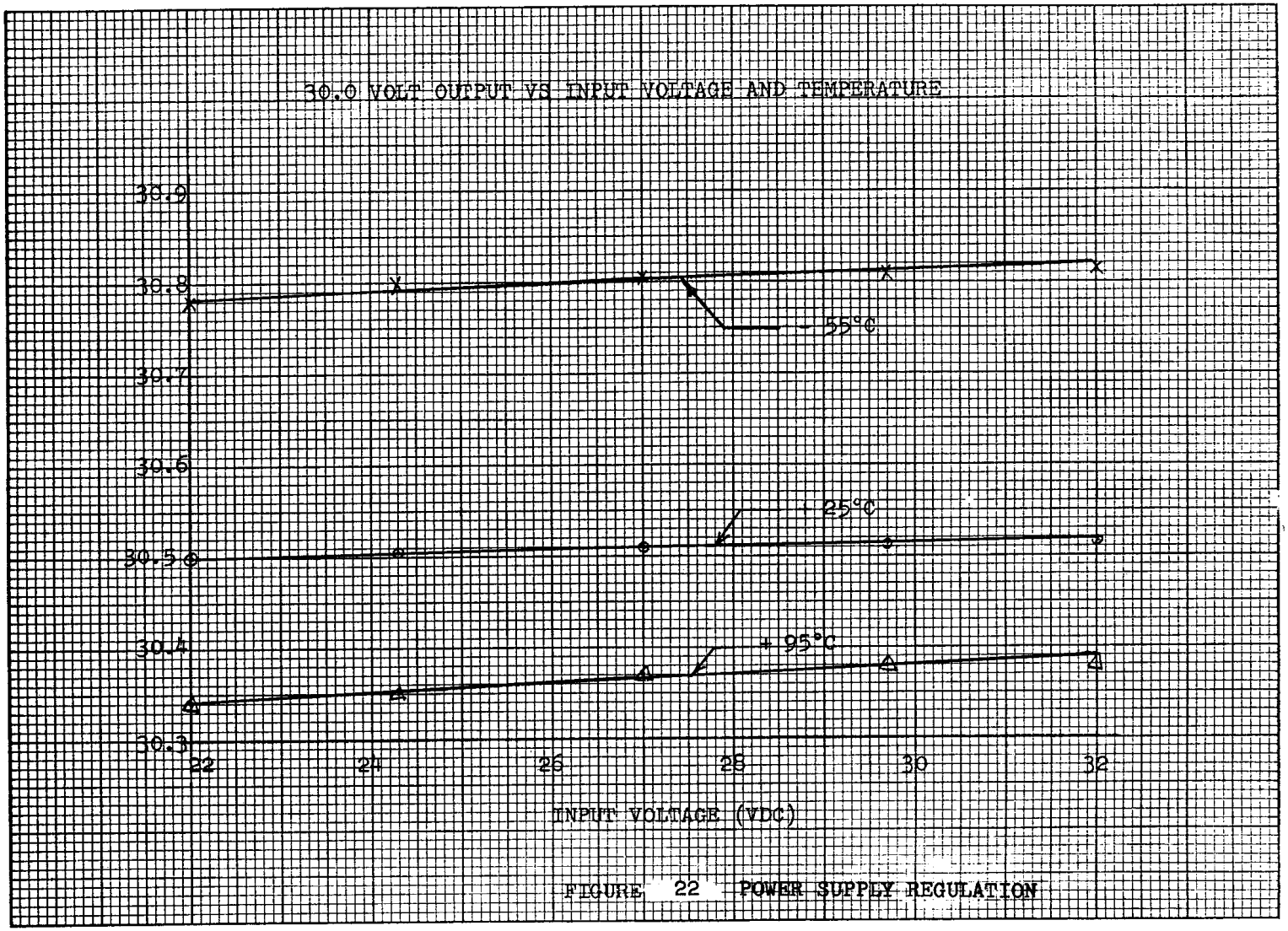


Figure 22. Power Supply Regulation

TABLE I PERFORMANCE-TO-DATE

Measurement	Specification	Data
Frequency	2200 - 2290 Mc	2280 Mc
Stability	± .001%	± .0007%
Output Power	2.0 W/50 ohms	2.2 watts
FM Deviation	± 1% / ± 125 kc	± 0.92%
Sensitivity	± 125 kc / V_{rms}	± 131 kc /V rms
Response	± 1 db / 100~ - 100 kc	90~ - 100 kc
Output VSWR	1-5:1 max. / 50 ohms	1-3:1
Transmitter Eff.	10.7% min.	12.2% R.T.