PROTOTYPE MIMO TRANSMITTER FOR SPIN STABILIZED VEHICLES

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ABSTRACT

This paper describes the design of an inexpensive and scalable transmitter for a Multiple-Input Multiple-Output (MIMO) communication system. The transmitter is intended to be used in aerospace applications, especially in spin stabilized vehicles. A field programmable gate array (FPGA) in the modulator will implement a modified Alamouti space time block code which will take advantage of the cyclostationary nature of the channel to increase the system data rate.

Keywords: Multiple-Input Multiple-Output Systems, Aerospace Telemetry, DSP

INTRODUCTION

Communication systems which use a single transmit antenna and a single receive antenna are subject to fading due to multipath reflections. The ground, atmosphere, and other objects, can reflect an electromagnetic wave, allowing multiple copies of the signal to appear at the receiver with varying signal strengths and arriving at different times. The differential delay created by the varying path lengths can lead to destructive interference which can dramatically decrease the receiver's signal-to-noise ratio (SNR), and result in higher bit error rates (BER).

Transmitting antennas that are mounted on vehicles face another challenge. The transmitting antennas from the receiver can be obscured partially, or completely, by the vehicle. This can be seen in Figure 1 where transmitting antenna 1 has no path to either of the receiving antennas. This problem is typically mitigated by placing multiple transmitting antennas on the vehicle. By judiciously locating the transmitting antennas, it is usually possible to assure that at least one transmitting antenna will be visible regardless of the vehicle attitude. This visible antenna may still experience multipath fading as described above.

While multiple transmit antennas may be necessary on a vehicle, they generate their own set of problems. It is typically impractical to select antenna locations and radiation patterns to assure that only one antenna is visible to the receiver. If the same signal is sent out to both transmitting antennas, the differing path lengths to the receiver can have the same effect as multipath interference. At particular vehicle orientations, this interference may cause the SNR to drop to unacceptably low levels.

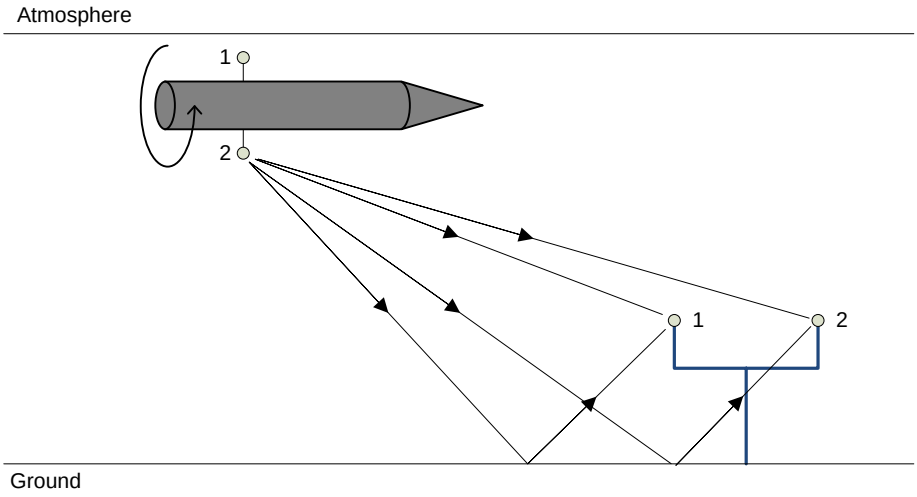

Figure 1 – Multiple Antennas Mounted on a Spinning Vehicle

This problem can be mitigated by using space time block codes (STBC), and other techniques developed for Multiple-Input Multiple-Output (MIMO) communication systems. In these systems, different signals are sent from the transmitting antennas. A receiver that uses two or more antennas recovers these signals, estimates the channel attenuation and phase of each of the individual communication paths, also known as the channel coefficients, or channel state information (CSI). Once the receiver has this information, it can use it to recover the transmitted data. While it is still theoretically possible for the antennas and environment to cause a dramatic reduction in SNR, it becomes far less likely than in a conventional Single-Input Single-Output (SISO) communication system [1].

Estimating the CSI is a challenge for all MIMO systems. It becomes even more challenging when there is high relative velocity between the transmitter and receiver antennas, or high Doppler shifts caused by acceleration. There has been a significant amount of work performed in measuring and modeling the CSI for these channels [2].

Some aerospace vehicles, such as missiles, are spin stabilized. The multiple transmit antennas on these vehicles face all the same challenges as a conventional vehicle, with the added feature that they routinely roll into, and out of, view of the receiver. This can make estimating the CSI even more challenging. However, it also gives a periodic, and hence predictable, component to the CSI. By measuring and exploiting this predictability one could improve the overall system performance. For example, if one could predict the times a transmit antenna would be obscured, it may be possible to transmit less power out of that antenna and devote more of the energy to the antennas which are visible to the receiver.

Many of the conventional models, and channel measurements, for MIMO systems are not well suited for spin stabilized vehicles. There is work underway to create a prototype MIMO transmitter which is reasonably small and inexpensive, which could be used in spin-stabilized vehicles. This paper describes some of the high level design of that prototype.

MIMO

Conventional MIMO systems focus on either increasing the data rate or improving the reliability of a communication link. A system which uses two transmitting and two receiving antennas can theoretically achieve twice the data rate of a SISO system [3]. By carefully selecting the phase and amplitude of the signals sent to the two transmitting antennas, it may be possible to have essentially two independent paths from the transmitter to the receiver. A popular method of performing MIMO for 2x2 (two transmit antennas and two receive antennas) is the Alamouti code [4]. The transmitter designed in this paper will be able to implement a 2x2 Alamouti code with the option to implement more channels.

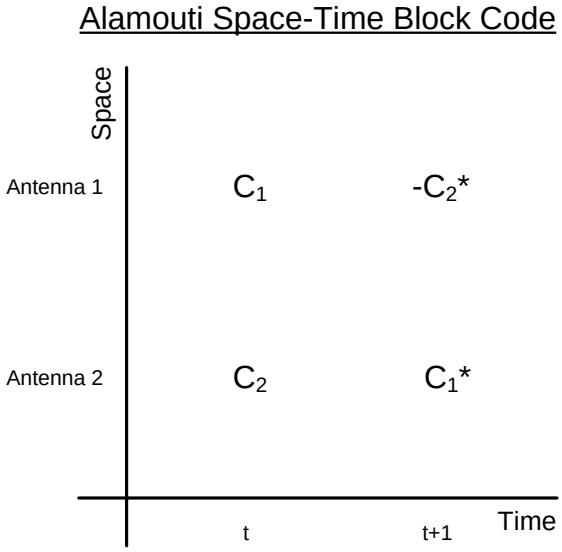

Figure 2 – Alamouti Space-Time Block Code

While the Alamouti code depicted in Figure 2 is popular, it is not the only MIMO modulation available. The special features of a spinning vehicle may also make it desirable to develop a customized modulation technique. It will be helpful if the transmitter is flexible enough to accommodate different modulation formats. To provide this flexibility, the transmitter will use a field programmable gate array (FPGA) for baseband modulation. Data will enter the FPGA via a serial interface. The goal is to accommodate data rates up to 1 Mbps.

The initial FPGA code will implement a 2x2 MIMO transmitter. This requires a total of four outputs from the FPGA, two for each of the transmit antennas. The output data rates will be at least an order of magnitude higher than the data rate. In this case, we will need at least 10 Msamples/sec. This will allow pulse shaping of the output signals so as to control the spectrum and bandwidth of the transmitted signals.

The two outputs for each channel will be sent to digital-to-analog (D/A) converters to create two baseband analog signals. The D/A will have at least 10 bits of precision per sample, with a target SNR of at least 50 dB. The analog signals will be fed into a Quadrature Modulator. By varying

the FPGA outputs, it should be possible to generate arbitrary modulations at the quadrature modular output, including popular PSK, FSK, SOQPSK and other formats.

The Quadrature Modulator was tentatively selected to fall in the unlicensed 2.4 GHz ISM band. The reference carrier is generated through a phase-locked-loop (PLL) device. The frequency of the PLL is typically selected through a combination of a low frequency crystal oscillator, and through instructions sent to it from the FPGA during power-up. It will be possible to move the transmit frequency to one more commonly used by telemetry systems by software control. A block diagram for the transmitter is shown in Figure 3.

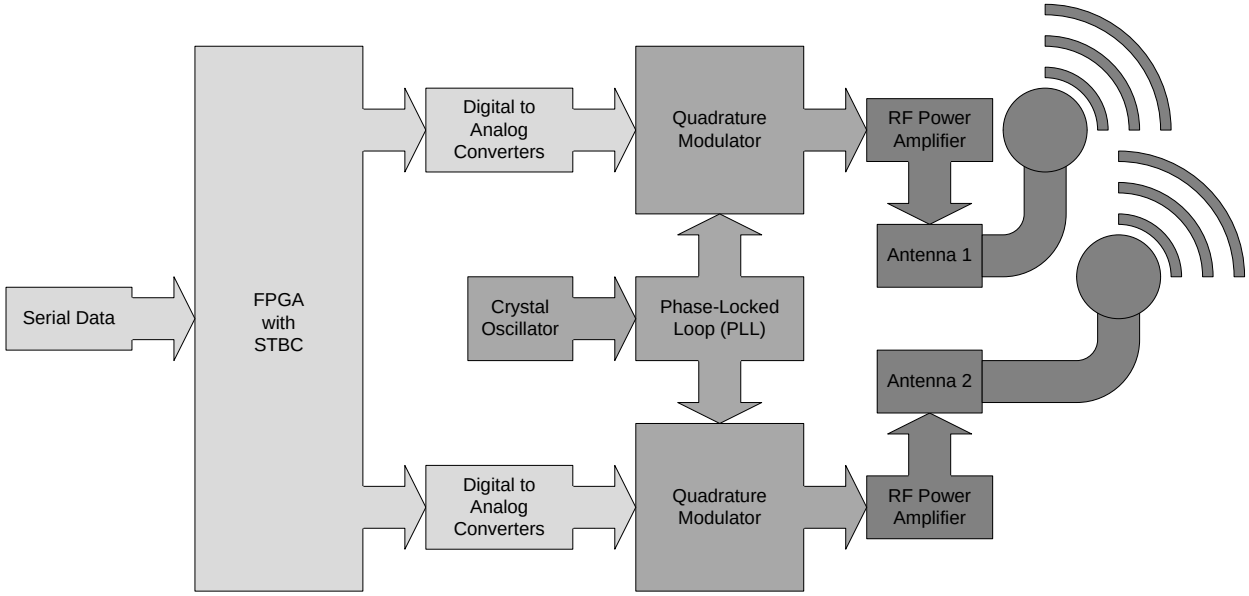

Figure 3 – MIMO Transmitter Block Diagram

HARDWARE DESIGN CONSIDERATIONS

In order to achieve reliable operation, there are many factors that need to be considered at the hardware level. Printed circuit board (PCB) design, signal routing, trace modeling, and component selection all play very important roles in the design of circuitry that operates with reasonable signal integrity in the GHz range.

We began by selecting a PCB design which uses four layers. The two internal layers are dedicated to power and ground planes, as shown in Figure 4. They will use the minimum spacing allowed by the fabricator. This will minimize the size of loop currents, and also minimize the impedance of the power place across all frequencies by adding buried capacitance [5]. To further reduce the impedance of the power supply, decoupling capacitors will be liberally used, and placed near the power pins of all semiconductors. To minimize the inductance of these capacitors, we will use small packages (0402 or smaller) in a parallel design on either side of the power trace [6]

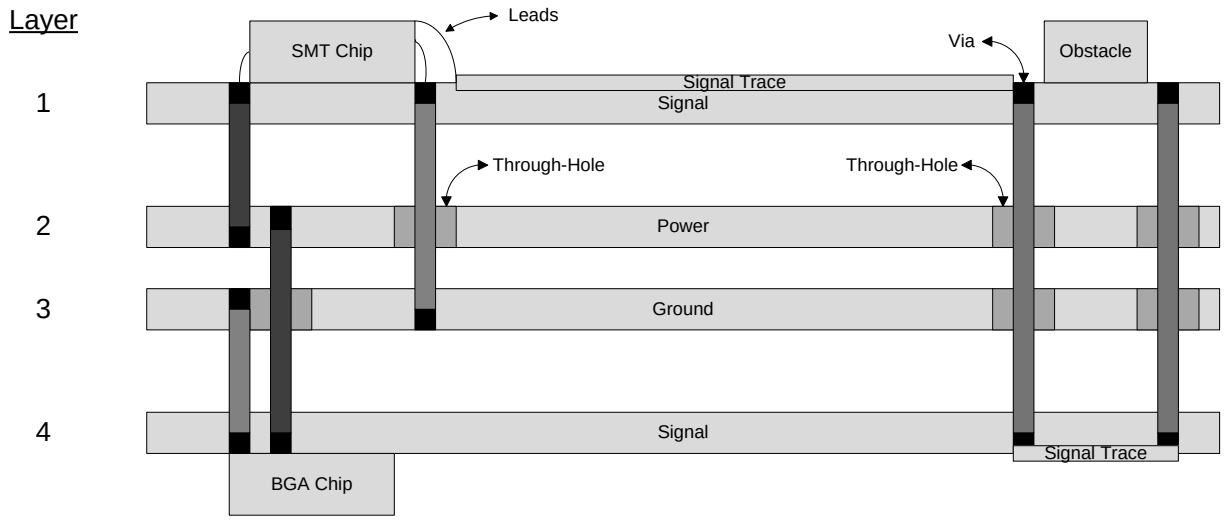

Figure 4 – PCB Cross Section

The FPGA to D/A to Quadrature Modulator (QM) to antenna routing will be kept as short and direct as possible as the lossless transmission line model is most accurate for short line length. The FPGA core can draw a large current during operation, so it will be placed as close as possible to the power input of the PCB and utilize a large decoupling capacitance to help supply current during spikes. The output amplifier is another potentially high current component that will be treated similarly.

We anticipate varying DC levels will need to be supplied for the various components on the board. The easiest method of generating these voltages would be to supply the highest voltage required from an external power supply, and then use low drop-out linear regulators on the board to generate the lower voltages. However in some applications there may be power and thermal constraints which will make this design a problem. We are investigating the use of DC-DC converters to reduce the thermal emissions from the transmitter. This will require additional components, board space, and cost. We are currently investigating the design trade-offs associated with this decision.

Trace routing is a fundamental part of PCB design. The FPGAs we are considering have 256 pins on the bottom and all of these pins need to be accessed for use as power, ground, or I/O. Even unused pins could require a light pull up resistor depending on the manufacturer. Routing space underneath the FPGA will be very limited. Since our board will be four layers, we will have the advantage of being able to route traces to the bottom signal layer to ease routing conditions in the cramped area under the FPGA. High speed signal traces will be given priority to remain on the top layer because trace modeling would become unnecessarily complicated. Vias will be used to access the ground and power planes for pins wherever possible. Pin terminations will be sent to the bottom layer. The bottom layer could also be used to circumvent obstacles as shown in Figure 4.

We may need to turn a signal trace as much as 90 degrees to get to the next stage of the transmitter in our design. While this may sound trivial, it can have disastrous effects if

implemented improperly. Figure 5 illustrates our need to use multiple bends in this worst case for a signal trace. The dark areas in Traces 1 and 2 will not conduct current as frequency increases. The current will get choked off under these conditions. Instead the dark areas will store a positive charge, complicating the transmission line model. This effect is much smaller when utilizing multiple bends as in Trace 2. Trace 3 would be the absolute best case for curbing this effect, but is usually impractical due to most parts and traces having strait-edged geometries.

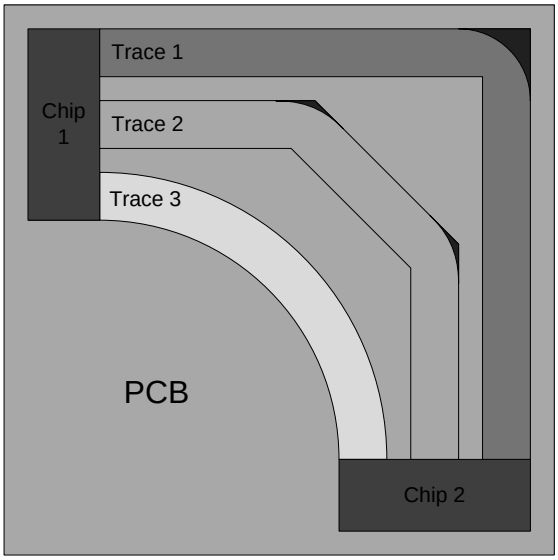

Figure 5 – Trace Geometry

Another important thing we will consider during board layout is where the current loops appear on the ground plane. If a clock or switched circuit current loop intersect the signal loop, then unwanted noise at the clock or switch frequency will likely show up on our signal. The current through a trace on the signal plane will appear underneath the trace on the ground plane. We will route traces to ensure this will not happen.

COMPONENT SELECTION

The components need to be selected very carefully to achieve optimal performance. For example, if the output impedance of the D/As do not match the input impedance of the modulators, then there will be a reflection. We will closely observe the following considerations during parts selection.

The package type and size play a very important role in the design process. While one package type is not better than another for every application, as a general rule we will choose all our parts that operate at high frequency to have the lowest inductance introduced by the pins possible [6]. The package with the lowest inductance currently available is the Ball Grid Array (BGA). The contact pins on this package type are underneath the chip so as to have the shortest lead (and therefore the smallest inductance) possible. The problem with this package is that it is difficult to mount. The only way to tell if all the contacts are soldered properly without thoroughly testing

the part's performance is through nondestructive x-ray imaging. That might sound expensive because it is especially considering it is an added expense just to verify the mounting of a chip. The BGA is also ideal in situations where a high number of I/Os are required in a small area. Since almost the entire bottom of the chip can be covered in pins, it is possible to have hundreds if not thousands of I/Os.

The next best package is the Quad Flat No Leads (QFN). It is essentially the same as the BGA except that the pins are situated around only the edges of the bottom of the chip and show on the side. This makes it possible to solder in a typical lab, but limits the amount of I/Os possible to the amount of space on the sides of the chip.

Quad Flat Packages (QFP) with leads and Small-Outline Integrated Circuit (SOIC) packages can still be considered for high frequency operation, but will have more inductance because its leads are considerably long. The Dual In-line Package (DIP) package is much worse and should not be considered in high frequency systems. The leads on these are meant to be installed through holes in the PCB. At high frequencies, these leads have considerable inductance. This will, in turn, slow the rising and falling edges of a signal, effectively creating an upper limit on how fast the system can operate without the rising and falling edges running into each other. There are many similar packages that will perform as poorly as these and they should also be avoided in high frequency applications. Sockets and other mounting devices for chips should be used carefully. These will effectively increase the lead length to the PCB and complicate any trace modeling.

While the best package for high frequency performance is the BGA, it comes at a higher total cost after mounting. With the appropriate amount of foresight, cheaper alternatives can be utilized with acceptable performance.

DIFFERENTIAL SIGNALING

For the best signal integrity at high frequencies, components that utilize differential signaling will be used wherever possible. Differential signaling is implemented by using two traces to send complimentary signals through the circuit. The advantage of this routing method is that it avoids using the ground plane as a reference for the signal by instead comparing the complimentary signals. Therefore any potential difference between the beginning and end of the ground plane below the signal trace is avoided. Additionally, noise immunity is better than in a single-ended signal since any noise picked up on one line is picked up on the other and eventually canceled out at the termination [7].

Differential lines will be routed next to each other to minimize any difference in path length, and hence differential impedance and time delay. Dissimilarities in the traces could result in distortions in the transmitted signals. There could also be problems with characteristic impedance mismatches of the traces, preventing the circuit from supplying the maximum design power at the antenna output.

We will utilize differential signaling wherever possible in our design due to these inherent advantages. The connections from the FPGA to D/As to QMs to Radio Frequency Power Amplifiers (RFPA) to antenna are of particular importance and the matching of these components will be vital to the optimum performance of our system.

TRACE MODELING

When routing a signal between two components, it is imperative that we match the output impedance of the component sending the signal to the input impedance of the component receiving the signal. Additionally, we must match the characteristic impedance of the trace connecting the components to both impedances. If all of these impedances are not matched, then the signal will be reflected back and forth from the input to the output of the trace. This could potentially create data errors when the reflected wave adds to or subtracts from the incident wave of the next sequence.

Trace modeling software, such as the Hyperlynx™, will be used to calculate the length, width, and height of the copper trace required to have the desired characteristic impedance to match a component's output impedance to the input of the next.

FPGA

The FPGAs considered for our project have a low core supply voltage between 1.15 – 1.25 Volts to lower static and dynamic power consumption. Therefore, the noise margin is especially low and proper PCB design is a priority with respect to this component.

FPGA manufacturers release extensive information on the proper use of their product. This information will include designations for pins and how to access them in software and hardware. The many functions of the FPGA will be studied to identify the most efficient way to process data internally. The FPGA is capable of dealing with high data throughput since its internal logic blocks can be coded to act in parallel.

Most of the FPGAs considered for our project have between 2-4 internal PLLs that can be coded to output to an external pin to be used by the QMs. We are currently investigating the use of this pin to clock the QM to reduce size, cost, and power consumption by eliminating the need for separate PLL and crystal oscillator packages. It can also help with trace routing as the QM can be positioned closer to the FPGA in the layout.

Choosing the proper number of I/Os and internal logic blocks is also very important when selecting an FPGA. Prices for FPGAs vary over a range of more than 30:1, depending on the number if I/O pins and logic blocks, so this is an important decision that must be made before designing the PCB. We require four inputs for the serial data. On the output, we need four for each of the four serial D/As and a few clock pins. Multiple power and ground pins will also need to be considered for the core and I/Os. We decided that less than fifty I/Os are sufficient to handle the information load and keep costs low while leaving extra I/O pins for future work.

PCB SIZING

The size of our PCB may play an important role in a spin stabilized vehicle application as the inertia of all its components must be accounted for. The expected size of our two-antenna prototype PCB is approximately 2”x5”. This size is based on common FPGA, QM, and other component package sizes. This size is tentative based on the required antenna placement and selection, but should not deviate more than half of an inch from the expected margins. If the antennas must be placed further apart, then they will be mounted separate from the main PCB if possible using twisted pairs. Larger PCBs have the advantage of being more electrically similar to infinite planes for trace modeling. In simulation this is a desirable trait that achieves higher accuracy, but it is not always attainable given the application.

CREATING A SCALABLE DESIGN

Designing a scalable design of a MIMO transmitter includes many additional considerations, specifically for the FPGA. Since the Alamouti code is substantially different for higher level transmitters, the FPGA will need to have additional coding options for multiple antenna sets. The number of I/Os must be proportional to the amount of antennas intended to be driven. A set up with a substantial amount of antennas would require a significantly higher amount of I/O pins on the FPGA. So there will be a limit to the maximum amount of antennas possible for a practical, scalable design.

The add-on transmitters will have to have additional QMs, PAs, and antennas, but can be driven by the FPGA on the primary board, limited only by the number of I/Os. For a very high number of channels, a separate, coordinated FPGA may be utilized on an add-on board.

HARDWARE TESTING AND VALIDATION

The first spin of this PCB will include multiple test points along the signal path for validation and helping identify hardware design problems. While test points will be invasive on trace impedance and therefore performance, the effects of this will be minimized by using a coaxial cable as a probe with a short ground wire. The short length coaxial cable must be matched to the trace impedance in question to avoid reflection.

Time Domain Reflectometry (TDR) will be used to measure the transient performance of our system. This will help identify which component, trace, or interconnect could be causing a signal integrity problem. The Vector Network Analyzer (VNA) will be used to measure the frequency domain performance to identify any problem areas in impedance across the entire frequency spectrum.

A common test of the performance of communication system hardware is the eye diagram. This will allow us to compare where the rising and falling edges of the signal fall with respect to where they should be. From this we can determine jitter characteristics and conclude if our system has acceptable performance in minimizing bit errors [6].

CONCLUSION

The hardware design of a MIMO transmitter has been demonstrated. While it was impractical to try to fit every signal integrity and hardware design consideration into this paper, the most important points were identified and expanded upon. In order to effectively use the FPGA to its full potential, the PCB layout must be designed to suit its many capabilities.

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