COMMUNICATIONS OVER AIRCRAFT POWER LINES: A PRACTICAL IMPLEMENTATION

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ABSTRACT

This paper presents a practical implementation of a hardware design for transmission of data over aircraft power lines. The intent of such hardware is to significantly reduce the wiring in the aircraft instrumentation system. The potential usages of this technology include pulse code modulation (PCM), Ethernet and other forms data communications. Details of the field-programmable gate array (FPGA) and printed circuit board (PCB) designs of the digital and analog front end will be discussed.

The power line is not designed for data transmission. It contains considerable noise, multipath effects, and time varying impedance. Spectral analysis data of an aircraft is presented to indicate the difficulty of the problem at hand. A robust modulation is required to overcome the harsh environment and to provide reliable transmission. Orthogonal frequency division multiplexing (OFDM) has been used in power line communication industry with a great deal of success. OFDM has been deemed the most appropriate technology for high-speed data transmission on aircraft power lines. Additionally, forward error correction (FEC) techniques are discussed.

KEYWORDS

Power Line Communications, Orthogonal Frequency Division Multiplexing (OFDM), Digital Up-Conversion (DUC), Digital Down-Conversion (DDC), Forward Error Correction (FEC)

INTRODUCTION

The usefulness of transmitting data over aircraft power lines has been recognized and described elsewhere [1]. Suffice it to say that a significant time and cost savings can be realized, particularly in regard to test instrumentation retrofits, when existing power wiring can be used to communicate test data. Phase I and Phase II of a multi-phase effort to develop an aircraft power line communications system will be discussed. While Phase I was primarily orientated toward a proof-of-concept effort, Phase II work was geared toward producing a practical, ruggedized implementation that could be deployed in actual field tests inside aircraft.

PHASE I SYSTEM OVERVIEW

Figure 1 shows an overview of the Phase I system. Whenever possible, commercial-off-the-shelf (COTS) development or evaluation boards and components were used to reduce cost and development time. Altera Stratix II EP2S60 Data Signal Processing (DSP) Development Boards were used for the baseband portions of the transmitter and receiver. The total bandwidth of the baseband signal is 500 kHz. An Analog Devices AD9857 Digital Up-Converter (DUC) evaluation board up-converted the baseband signal to an intermediate frequency (IF) of 4 MHz. This was then sent via a digital-to-analog converter (DAC) to the transmitter's analog front-end (AFE), consisting of a Class A broadband amplifier, filtration, and power line coupler. On the receiving side, a power line coupler and receiver AFE were used to feed an Analog Devices AD6636 Digital Down-Converter (DDC), which converted the incoming IF signal back down to the baseband signal.

PHASE I BASEBAND SUBSYSTEM

Figure 2 shows a block diagram of the Phase I transmitter baseband portion, as implemented in the DSP board field programmable gate array (FPGA). To facilitate testing, serialized data for transmission could be sourced either from an internal pattern generator capable of generating square waves and psuedo random number (PRN) bit error rate test (BERT) sequences, or an external source. This data was then modulated using differential quadrature phase shift keying (DQPSK). In DQPSK the data to be transmitted is broken up into dibits (bit pairs). The dibit determines the differential angle through which the inphase (I) and quadrature (Q) signals will be modulated. Only differential angles of $\pi/4$, $3\pi/4$, $-\pi/4$ and $-3\pi/4$ are allowed in DQPSK
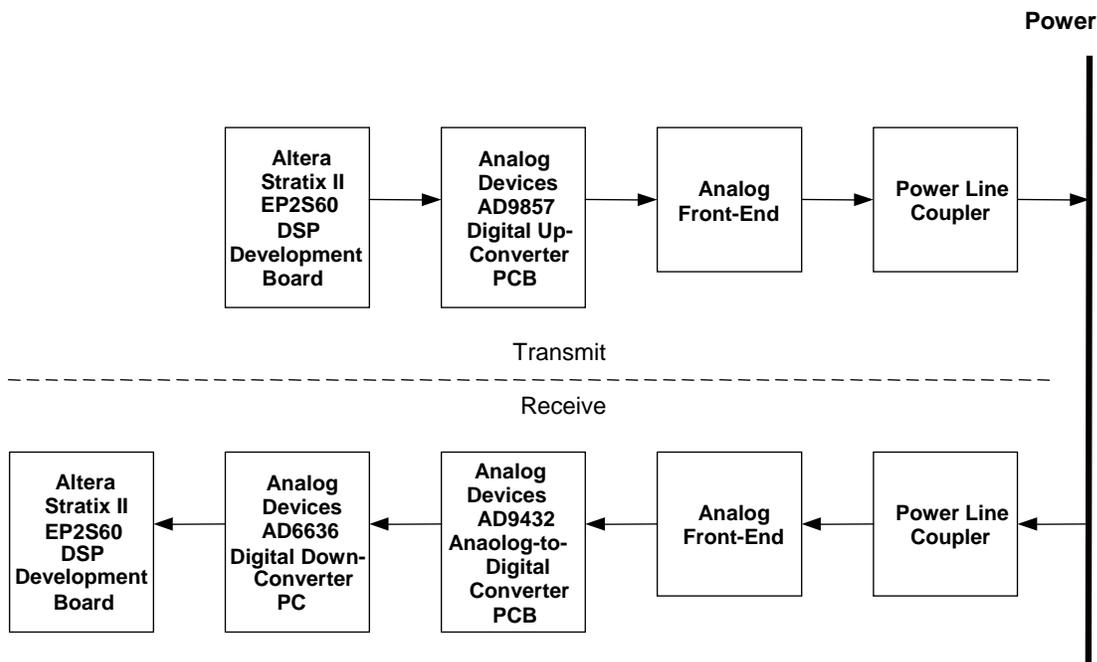

Figure 1 Phase I System Overview

modulation. Figure 3 shows the DQPSK constellation map, where the dotted lines indicate allowable transitions. Figure 4 shows the actual constellation as measured in the lab for the repetitive sequence of dibits (1, 0), (1, 0), (1, 0), etc. (square wave). The robustness of DQPSK modulation comes from the fact that even when there are wide variations in amplitude, the demapper still obtains the correct values. This is because it only responds to the differential angle, not absolute magnitude. Also, DQPSK is somewhat tolerant of modest constellation drift (rotation).

After DQPSK modulation, the resulting serialized data stream is parallelized and fed to a 128-point inverse Fast Fourier Transform (iFFT) to obtain orthogonal frequency-division multiplexing (OFDM) modulation. The OFDM essentially divides the total 500 kHz bandwidth into 128 adjacent subchannels. Each subchannel only has to carry 1/128th of the entire bit rate. OFDM has been found to be very robust in the harsh environment that power lines present, where deep notches in the characteristic transfer function due to the multipath effects result in frequency selective fading [1].

Finally, a cyclic prefix (CP) is inserted into the guard interval at the beginning of the OFDM symbol and the resulting data is windowed by a root raised cosine finite impulse response (FIR) filter before being passed on to the DUC. The matching receiver is similar in nature to the transmitter; it simply performs the inverse operations in the reverse order, i.e., CP removal, FFT and DQPSK demodulation. With such a system, a 500k bits-per-second (bps) data transmission rate was achieved in a laboratory simulation of an aircraft power line.
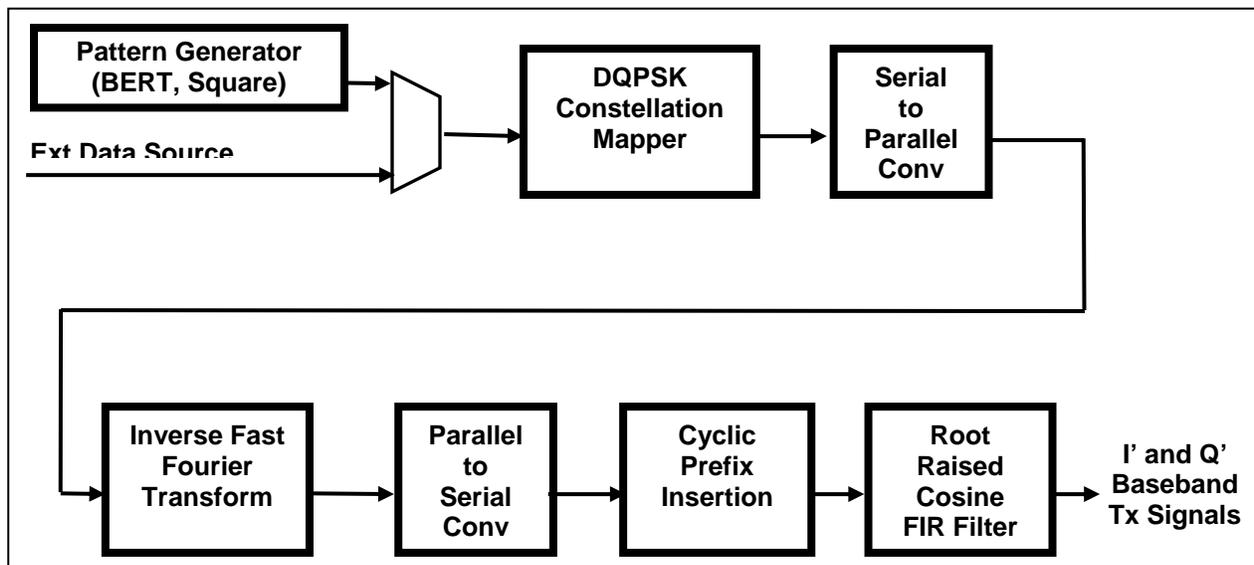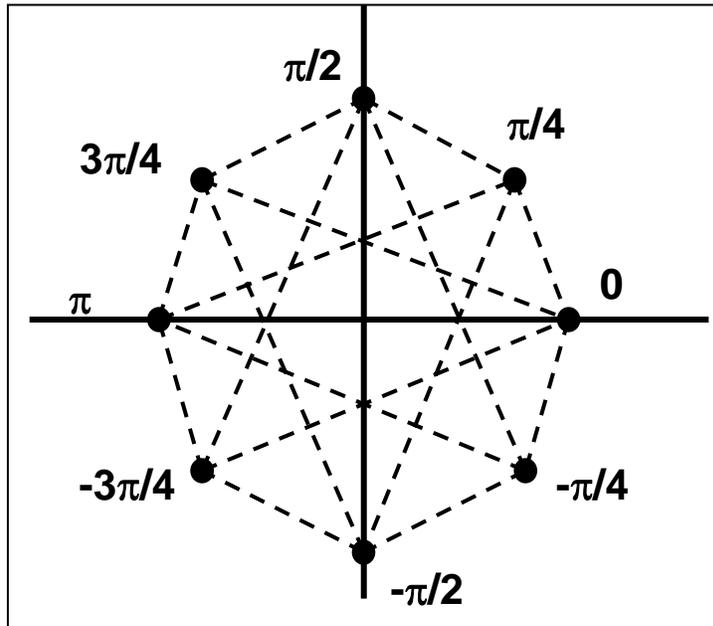

Figure 2 Phase I Baseband Transmitter Block Diagram

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Figure 3 Constellation Mapping Used in DQPSK
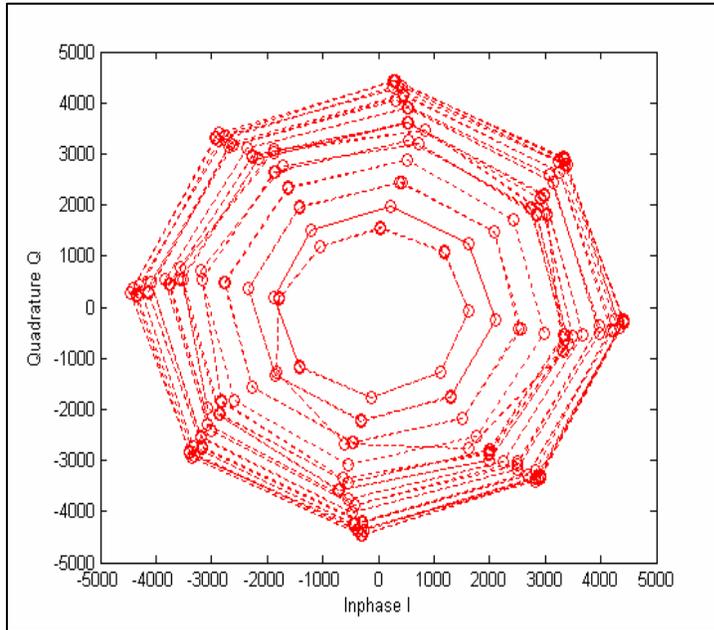

Figure 4 Typical Constellation in the Phase I Receiver

PHASE I—DIGITAL IF

On the transmitting side, a digital up-converter chip generates the digital IF signal. This chip integrates a high-speed direct digital synthesizer (DDS), digital filters, a DAC and other DSP functions. The baseband I and Q data are interpolated and filtered at the first stage. The following quadrature modulator modulates the interpolated IQ data into a quadrature-modulated complex signal. The DDS core provides the sine and cosine local oscillator signal to the modulator. The final stage is the DAC, which converts the complex digital signal into the analog signal. Add reference to figure 5.
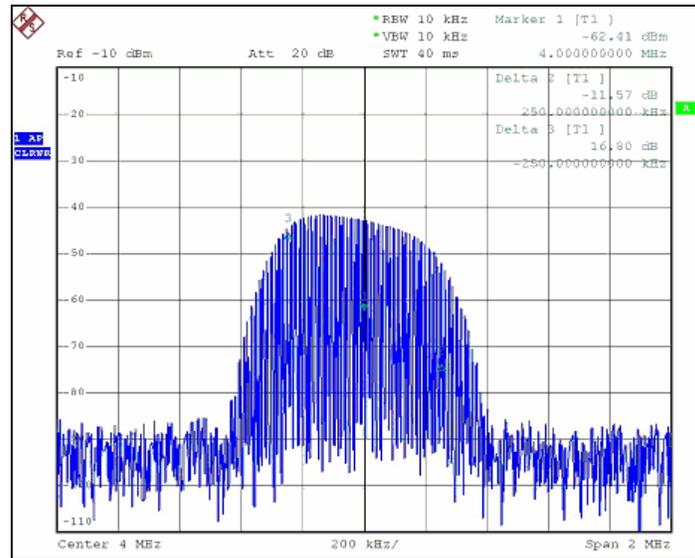

Figure 5 Transmitter Spectrum

On the receiving side, a DDC chip converts the digital IF signal into the baseband IQ data. The following stages are integrated in the DDC chip: a frequency translator, several decimation and digital filtering stages, and clock multiplier circuitry. The DDC obtains the digital data from an analog-to-digital converter (ADC). The frequency translator shifts the complex input signal from IF to baseband. The following digital filtering stages decimate the signal and reject the aliasing. The processed IQ signal is then input into the FPGA (figure 6.)
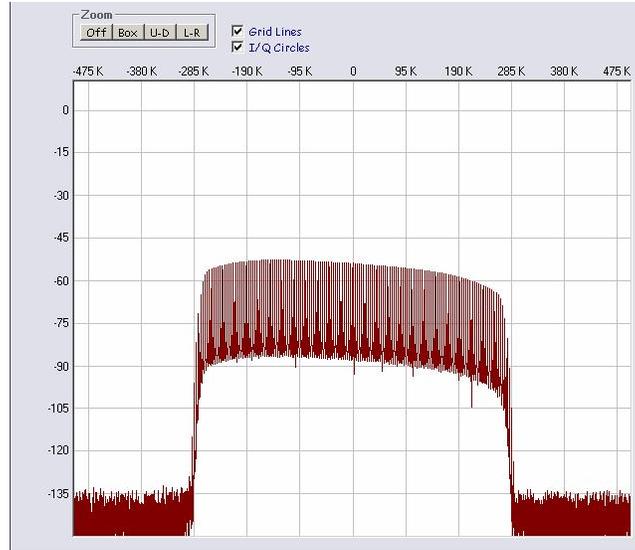
Figure 6 Recovered Baseband Signal Spectrum

PHASE II SYSTEM OVERVIEW

The primary goal of Phase II is to produce a miniaturized, ruggedized power line transceiver based on results from Phase I. Figure 7 shows an overview of the Phase II system. The DUC and DDC functions have been incorporated into the FPGA to reduce PCB space. A custom media access control (MAC) was added and interfaces to the OFDM PHY. First-in first-out (FIFO) queues serve as input and output smoothing buffers that allow the transceiver to interface with external PCM equipment. Clock recovery circuitry enables the synchronization of the external PCM clock domain to the local transceiver domain.
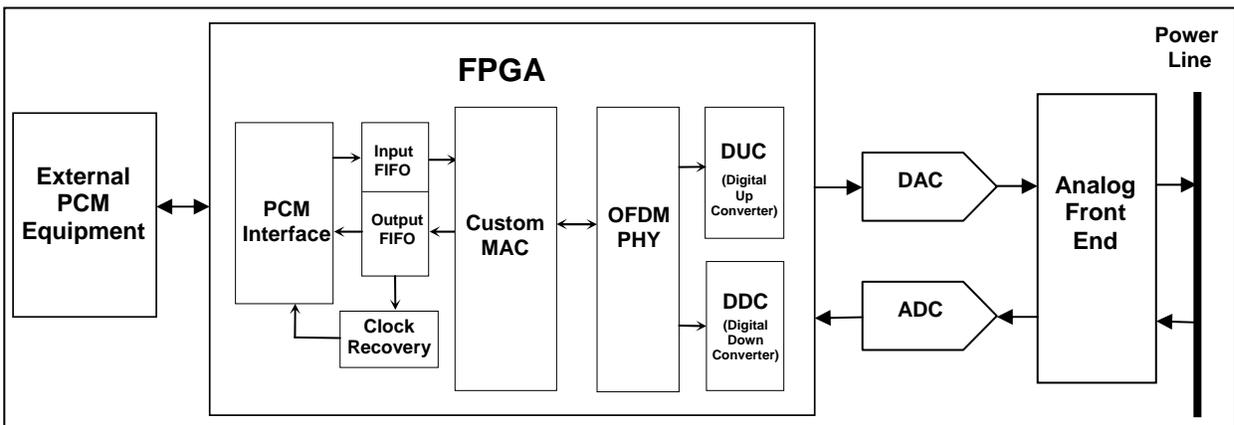

Figure 7 Phase II System Overview

PHASE II BASEBAND SUBSYSTEM

The Phase II transceiver baseband subsystem has been significantly enhanced compared to that of Phase I. Forward error correction (FEC) has been added to reduce bit error rate and ultimately lengthen the distance over which communications can reliably be accomplished. The chosen method is convolutional encoding with puncturing at the transmitter and Viterbi decoding at the receiver side. Coding rates of 1/2, 2/3 and 3/4 are supported. This method works well when errors are randomly dispersed. Bit interleaving has been added to help guarantee this spreading. (Outer Reed-Solomon FEC could be added if bursty noise proves to be a problem.) Pilot subcarrier generation has been added to the transmitter to make detection in the receiver robust against frequency offsets and phase noise. Training sequence generation has been added to guide timing acquisition, coarse and fine frequency acquisition, and channel estimation (equalization and signal to noise ration [SNR] weights calculation).

PHASE II ANALOG FRONT END MODULE STRUCTURE

Before the carrier frequency of the analog signal can be selected, three major considerations must be evaluated:

1. The aircraft power line characteristics: According to [3], the lower frequencies have less attenuation in aircraft power lines. The frequency below 60MHz is chosen to obtain lower channel end-to-end attenuation.
2. The military emission regulations: According to the conducted emission requirement (CE102) of [2], the emissions on all +28 V power leads (includes returns) shall not exceed 60 dBµV from 1 to 10 MHz. This power level is too low to transmit any signal over power lines. Hence, the transmission band has to be placed higher than 10 MHz.
3. The harmonics of the carrier frequency: Harmonics are caused by the nonlinearity of the circuits: The carrier frequency needs to be carefully selected to avoid overlapping between the fundamental frequency and harmonics.

A frequency division duplex (FDD) transceiver is proposed in [3]. An FDD transceiver needs a broad isolation band between transmitting band and receiving band. In the power line communication system, the higher frequency has greater channel loss. A high output power amplifier is required to compensate this loss. The requirement of filters that isolate transmit (Tx) and receive (Rx) will be more stringent due to the high output level of the amplifier. To simplify the design, a time-sharing half-duplex transceiver design is implemented in this phase.

A half-duplex analog front end (AFE) board is shown in figure 8. The half-duplex data transceiver can transmit data in both directions on one signal carrier, but not at the same time. For example, one transceiver can send data on the line and then immediately thereafter receive data on the line from the other transceiver.
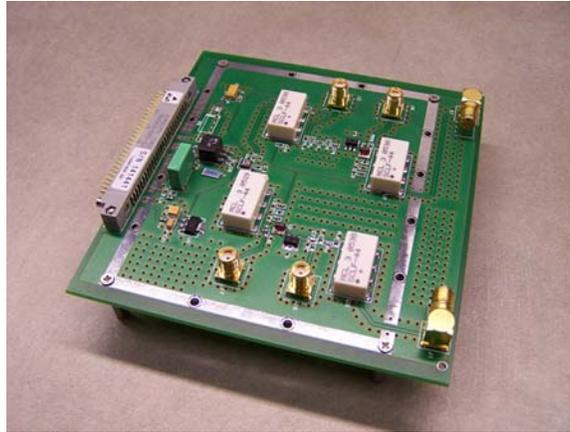
Figure 8 Phase II Analog Front End Circuit Board

SUMMARY

The feasibility of data communications over aircraft power lines was demonstrated in the Phase I study [1]. Based on the knowledge obtained during that phase, a Phase II system has been designed that is miniaturized, ruggedized, and highly enhanced. Training and pilot tone generation, PCM interfacing, convolutional encoding with Veterbi decoding, FEC, timing and frequency acquisition and channel estimation have all been added during Phase II. The result is a system that is deployable in aircraft test missions.

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