ARCHITECTURAL CONSIDERATIONS FOR A VARIABLE BIT RATE DATA ACQUISITION TELEMETRY ENCODER

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ABSTRACT

Modern telemetry systems require flexible bit rate telemetry encoders in order to optimize mission formats for varying data rate requirements and/or signal to noise conditions given a fixed transmitter power. Implementing a variable bit rate telemetry encoder requires consideration of several possible architectural topologies that place different system requirements on data acquisition modules within the encoder in order to maintain adequate signal fidelity of sensor information.

This paper focuses on the requirements, design considerations and tradeoffs associated with differing architectural topologies for implementing a variable bit rate encoder and the resulting implications on the encoder systems data acquisition units.

KEYWORDS

Encoder, sampling, filtering, spectral containment, eye diagram, variable bit rates

INTRODUCTION

Telemetry requirements for vehicle development have many common aspects. Encoders must interface to various types of analog and digital sensors, combine the data into an IRIG compliant format structure and supply the data to a suitable transmitter type for the application. All encoders share these basic functions, but the specific mission drives many other detailed requirements of the encoder.

For example, analog sensors have different output levels, load limitations, excitation needs, fidelity requirements and sampling rates. Encoder developers can therefore design analog sensor modules specifically for a particular customer's needs or design modules that have flexible software programmable interfaces. One benefit of developing modules for specific customer needs is that this generally leads to a simpler design with less up front development cost. The major drawback of this approach is that every iteration made to support a different set of requirements

will result in additional cost. It won't take many iterations before the cumulative incremental costs exceed the upfront additional cost of the flexible sensor module.

The variable sampling rates of analog sensors and changing data interfaces needs almost always leads to different aggregate data rate requirements; therefore, the same rationale used for developing flexible analog sensor modules applies to designing an encoder capable of generating variable data rates.

FACTORS DRIVING VARIABLE DATA RATE NEEDS

What is driving the need for a variable bit rate telemetry encoder, both from a customer and manufacturer's requirements perspective? As mentioned previously, customer A's telemetry requirements and thus data rates will almost certainly be different from their next program or customer B's needs, but there are several other possible factors as well.

Below is a list summarizing some of the possible factors driving the need for variable data bit rate telemetry encoder.

Customer Driven:

- Different mission phases may have changing data acquisitions requirements
  - e.g. a multi-stage rocket may have different active sensors for each stage
- Different missions within the same program have changing data acquisition requirements
  - e.g. captive carry test verses free flight
- Spectral allocations may vary during a program
  - e.g. higher priority program may force reallocations
- Link margin requirements can change during a specific mission or program
  - e.g. changing adjacent spectral allocation use may require lowering the data rate given a fix transmit due to added interference
  - e.g. different data rates require proportionately different transmit powers for the same link margin (with the same FEC)
- General ability to customize data rates in the field

Manufacturer Driven:

- No new development cost to absorb or charge the customer
- Quicker response to the customers needs
- Eases parts logistics, configuration management and manufacturing test to have one base design

VARIABLE BIT RATE ENCODER REQUIREMENTS

In order to design a variable bit rate encoder there are several constraints and considerations that must be addressed prior to starting the detailed design. For example, a data rate range and step size must be determined that adequately addresses market needs. Too much range will add extra cost and complexity, too little will limit the market applications. How many different data rates are needed in a single mission? If the data output feeds an analog transmitter interface the serial

data may need to be spectrally contained at the encoder output if this function is not included in the transmitter. What are the accuracy and jitter limitations of the variable bit rate encoder?

Data Rate Range and Step Size

A survey of past and present bit rate mission requirements over the years at L-3 Communications has yielded information demonstrating that a programmable range of approximately 100ksps to an upper bound of 10Mbps would have satisfied the vast majority of missions. The need for yet higher data rates have been increasing in recent years from data sources such as seekers. In order to address these higher data rate requirements and shrinking bandwidth allocations more spectrally efficient modulation methods were added to the IRIG 106-05 telemetry standard. These tier two modulation methods are shaped-offset quadrature phase shift keying (SOQPSK) and continuous phase modulation (CPM). Using these modulation methods it is reasonable to extend the high end data rate range to 40Mbps. Modern transmitters using data rates above 10Mbps will generally utilize non-shaped serial data interfaces for the SOQPSK and CPM modulation modes.

The minimum step size of the serial bit rate programming range is an important consideration because it may guide the implementation path towards a more complicated approach. If it is desired to allow the user to program the bit rate with a fine fixed resolution step over the whole possible data rate range then design approaches utilizing a numerically controlled oscillator may be appropriate. On the other hand, methods using simple integer divide factors may provide acceptable resolution if the master clock is of high enough frequency.

Mission Formats

A complex mission may have several phases where different events and mechanisms are in operation which requires changing the telemetry gathers and thus aggregate data rate requirements. One option may be to make one large super frame with all the sensor information embedded, but limitations in spectrum and power output can easily make this option not suitable. For example, different phases of the mission may require 20Mbps, 12Mbps and 4Mbps, but each phase has different sensors and thus different format structures. Even if the spectrum allocations were given for an aggregate super frame of 36Mbps, the power limitations of the transmitter may produce inadequate link margins for this format. If a variable bit rate encoder supported multiple formats with different data rates the link margins could be optimized to allocate the maximum allowed energy per symbol time for each of the mission phases.

Spectral Containment

The bottom line is that transmitted signals must meet the IRIG 106-05 spectral mask requirements for the utilized modulation method. Typically this only places a baseband premodulation filtering requirement on the encoder for FM transmitters with analog serial data interfaces. The filter mask requires a 30dB/octave slope, 12dB of which is inherent to the unfiltered NRZ PCM/FM signal. IRIG 106-05 states that “at least a three-pole filter” is required to meet the spectral mask and recommends four or more pole filters with the “-3dB frequency equal 0.7 times the bit rate.” Typically, this analog filter has a linear phase response such as a

Bessel or Gaussian filter. These filters are all-pole filters and contain no stop band zeros.

A key implementation issue discussed in detail later is the importance of remembering that if premodulation filtering is done in both the digital and analog domains one must be cognizant of the composite response in both the frequency and time domains. The composite filtering may easily be within the IRIG 106-05 spectral mask, but the time domain response may have excessive eye pattern overshoot and closure even when the filters are all linear phase.

Data Rate Accuracy and Jitter

Data rate accuracy and jitter are also generally major concerns in any digital communications system. The accuracy of the data rate will directly contribute to the overall tracking range and loop bandwidth of the symbol timing recovery function on the receive side.

Another issue related to the bit rate jitter is the possible implications on the data acquisition systems sampling fidelity of analog sensor inputs. If the data acquisition systems sampling clock is generated from the serial bit rate clock or a common master clock, the amount of jitter on this clock can limit the data acquisition systems analog interface performance.

It is widely known that jitter on a sampling clock will degrade the quality of sampled signal. The amount of degradation can be quantified as the jitter limited signal-to-noise ratio (SNR_{JL}) and is given by the following formula (1).

$$SNR_{JL}\ (dB) = -20 \cdot \mathrm{Log10}\ (2\pi \cdot F_{in} \cdot T_j) \quad (1)$$

where F_{in} = maximum frequency of the input signal
T_j = RMS jitter of the sampling clock

Additionally, if the input signal is oversampled and followed by digital filtering the jitter limited SNR is given by formula (2).

$$SNR_{JLOSR}\ (dB) = -20 \cdot \mathrm{Log10}\ [\ (2\pi \cdot F_{in} \cdot T_j) / \sqrt{OSR}\ ] \quad (2)$$

where OSR = oversampling ratio

Equation (2) shows that the SNR improves by approximately 3dB for every octave of oversampling assuming a brick-wall digital filter is limiting the bandwidth to the area of interest.

If the jitter component of the sampling clock is periodic the noise will reveal itself in the sampled spectrum as discrete spurious components on each side of the input signal. For example, if a 10kHz sinewave is sampled by a clock with a periodic 1kHz jitter component the spectrum will show side tones at 9kHz and 11kHz.

It is interesting to note the jitter limited SNR for various levels of sampling jitter at different input frequencies. Table 1 below grossly demonstrates some of these relationships for sampling sinewaves of various input frequencies given 1nsec of RMS jitter.

Input Freq (Hz)	RMS Sample Jitter (sec)	Jitter Limited SNR (dB)	Equivalent Number of Bits (ENOB)
1000	1.00E-09	104.0	17.0
2000	1.00E-09	98.0	16.0
5000	1.00E-09	90.1	14.7
10000	1.00E-09	84.0	13.7
20000	1.00E-09	78.0	12.7
50000	1.00E-09	70.1	11.3
100000	1.00E-09	64.0	10.3

Table 1: Jitter Limited SNR

Input Freq (Hz)	Peak Sample Jitter (sec)	Peak Jitter Limited SNR (dB)	Minimum Equivalent Number of Bits (ENOB)
1000	5.00E-07	50.1	8.0
2000	5.00E-07	44.0	7.0
5000	5.00E-07	36.1	5.7
10000	5.00E-07	30.1	4.7
20000	5.00E-07	24.0	3.7
50000	5.00E-07	16.1	2.4
100000	5.00E-07	10.1	1.4

Table 2: Peak Jitter Limited SNR

If high fidelity is required, Table 1 clearly shows that the jitter on the sample clock must be taken seriously. While crystal oscillators typically meet the jitter requirements for telemetry data acquisition systems, poor board routing and inadequate power conditioning can significantly degrade the sample clock beyond acceptable limits. Jitter accumulation from a phase-lock loop can also deteriorate the quality of the sample clock.

Figure 1 demonstrates the SNR to RMS jitter relationship graphically for several different jitter magnitudes verses frequency.

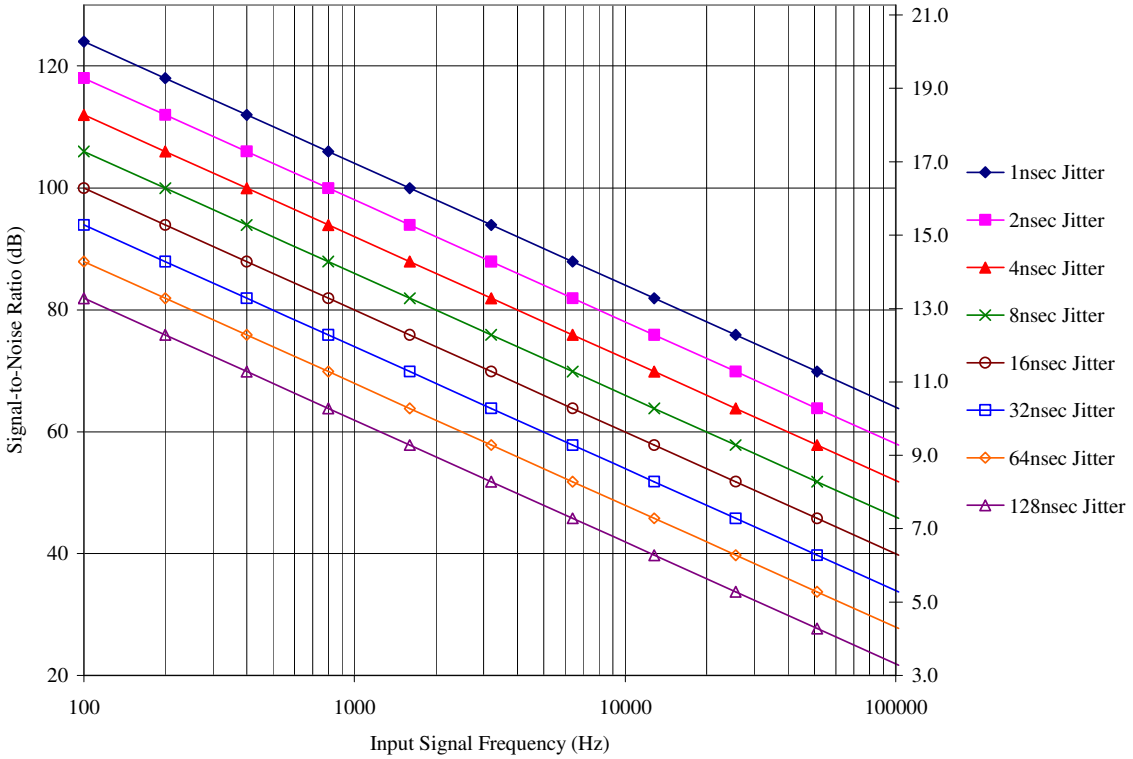

Figure 1: SNR vs. Input Frequency and Jitter Magnitude

The multiple plots for jitter magnitudes of 1nsec through 128nsec in Figure 1 demonstrate a 6dB/octave relationship between the SNR at a fixed frequency verses the jitter magnitude. Figure 1 also clearly shows a SNR reduction of 6dB/octave verses frequency for any fixed jitter magnitude.

In some telemetry encoder data acquisition systems, the sampling clock may not be synchronized to the system bit rate clock. In such cases the system design may require continuously variable interpolation filters to bridge the sampling domains with adequate fidelity. If the asynchronous clock domains are not bridged with an interpolation filter a periodic jitter component will be impressed on the samples. For example, a data acquisition module may use a fixed oscillator for the analog-to-digital converter (ADC) of a sensor module. If the ADC is sampled at 1MHz the sample period is 1usec. Now when the test engineer develops a format for sampling the sensors he may only require a minimum of 80kHz sampling, but due to the format structure and bit rate the closest sampling rate is 90kHz. Since the ADC sample clock is asynchronous to the system bit rate clock each time a sample is requested from the ADC there can be can error of up to half the sampling period or 500nsec. Note that the 1MHz sample clock and the 90kHz sample rate are not integer related and even if they were the jitter magnitude would still be bounded to 500nsec unless the 1MHz sample clock was frequency locked to the desired sample rate.

Depending on the system requirements the 500nsec of periodic jitter may pose major problems and render the sensor information unusable. Table 2 above demonstrates the worst case jitter imposed spurious levels for sampling sinewaves of various input frequencies given this example's 500nsec of maximum periodic jitter.

As one can see from Table 2, the consequences of asynchronously grabbing samples from the fixed 1Msps ADC at 90ksps into the telemetry format will have serious implications. The ADC may have been a 12-bit part with close to 11-bit performance, but by asynchronously bridging the data acquisition sample clock to format bit clock domains, the performance of the data acquisition system would be degraded to as low as 4.7-bits even for a input frequency as low as 10kHz. If the system only used a 100kHz ADC sample clock the situation would be degraded proportionately by another 20dB!

METHODS FOR GENERATING VARIABLE BIT RATES AND FILTERING

Bit rate agility can be implemented in several manners utilizing analog and digital design methods. Each of these methods has specific encoder system design implications. Some of the basic approaches and tradeoffs are listed below in Table 3. When we desire to add the agile bit rate and filter functionality without changing analog components we restrict our investigation to methods 2-5 that requiring digital signal processing techniques.

The design approaches investigated diverge into methods with and without the use of continuously variable interpolation filters. Methods using a continuously variable interpolation (CVI) filter benefit from a fixed sample clock requirement and therefore an easier analog anti-alias filter requirement. The tradeoff is at the expense of a highly intensive digital signal processing requirement using more FPGA resources and thus power. Fixed interpolation

methods require the generation of an analog bit agile clock and a little more complicated anti-alias filter, but need far less FPGA resources and thus power.

Method	Description	Pros	Cons
1	Change the oscillator and analog shaping filter	• Simple to implement • Low cost • Low power • Small size	• Possible long lead times on oscillators • Every design is custom and requires unique analog filter for the desired bit rate
2	Use a DDS with analog output to generate the bit clock and a programmable analog shaping filter	• Helps alleviate parts procurement issues. • Uses one base design to cover the bit rate range	• The programmable analog filter is very difficult to design for such a broad frequency range and the size constraints of the design may make this option not desirable • High power consumption for analog filter • Analog filter requires calibration
3	Use a DDS with analog output to generate the bit clock and digital shaping filter followed by a simpler programmable analog anti-alias filter	• Helps alleviate parts procurement issues • Uses one base design to cover the bit rate range	• The programmable analog filter is difficult to design for such a broad frequency range and the size constraints of the encoder may make this option not desirable • High power consumption for analog filter • Analog filter requires calibration
4	Use an all digital DDS with a continuously variable interpolation polyphase upsampling shaping filter followed by a simple fixed analog anti-alias filter	• Helps alleviate parts procurement issues • Uses one base design to cover the bit rate range • Small size and simpler, lower power analog design • Eliminates calibration of the analog filter	• Significantly more complex digital design than option 5 requiring a larger size FPGA • Requires more digital power than option 5 • Does not eliminate the need for a DAC and anti-alias filter on the DDS used for generating a clean data acquisition sampling locked to the bit clock
5	Use a DDS with analog output to generate the bit clock and digital shaping filter combined with digital upsampling followed by a fixed analog anti-alias filter	• Helps alleviate parts procurement issues • Uses one base design to cover the bit rate range • Small size and simpler, lower power analog design • Eliminates calibration of the analog filter	• More complex digital design than option 3 and higher digital power requirements • Only a slightly more complex analog anti-alias filter design required than option 4

Table 3: Tradeoffs for Variable Bit Rate Generation and Filtering Methods

Note that an analog filtered bit agile clock is always needed somewhere in the system to clean up the DDS bit clock output before the clock can be used for sampling in data acquisition cards unless we force all the data acquisition cards to also use continuously variable interpolations methods. Failure to do so results in possible jitter limited performance as discussed previously.

Given the above tradeoffs, L-3 Communications PCM330E telemetry encoder uses method 5 for bit rate agility which is based on the DDS combined with a fixed rate interpolation approach. The anti-alias filtering requirements are more stringent than the CVI method, but raising the minimum oversampling to 8x makes this compromise a manageable issue while still yielding the key desired benefits of the CVI method.

PREMODULATION FILTERING IMPLEMENTATION ISSUES

Meeting the IRIG 106-05 spectral mask is only one aspect of the premodulation filtering for an analog FM transmitter input signal. The time domain performance of this filtering is also critical because even if the signal meets the spectral mask it can have excessive amounts of ringing and non-linear delay that close the eye pattern of the signal. If the FM receiver doesn't have an equalizer this excessive eye pattern distortion will proportionately degrade the system performance and thus link margins. Even if the receive system has an equalizer the distortion will delay or may prevent acquisition. The IRIG 106-05 telemetry standard recognizes this issue, but only indirectly guides the systems design by recommending a four or more pole linear phase response. This guideline is rooted in the past when all the premodulation filtering was performed in the analog domain with either Bessel or Gaussian response filters. The nominal step responses of these filters inherently have little to no over/undershoot to degrade the eye pattern.

Modern systems using combined digital and analog filtering techniques must consider the composite response of this filtering. The analog component of this filtering is typically just for anti-aliasing, but designing the digital filter directly to the desired response is a mistake because even though the digital filter should dominate the composite inband response the analog anti-aliasing filter will have significant time domain implications for reasonable oversampling ratios (8x) of the serial bit rate.

If the desired response is to have no more than 3dB of attenuation at the 0.7x the bit rate the digital filtering should have less attenuation to allow for the digital-to-analog converters (DAC) sin(x)/x response and the passband attenuation of the analog filter. Typically the analog filtering will always have attenuation at 0.7x the bit rate because in order to have a step response with minimal over/undershoot the attenuation must roll off gradually out to around 2x to 3x the symbol rate. This requirement therefore dictates that the oversampling ratio be above 7x to allow for the analog filters transition band to adequately attenuate DAC images. If only a 4x oversampling ratio is used while the DAC sin(x)/x response and anti-alias transition band requirements are not considered, the eye pattern will look very distorted as shown in Figure 2.

The data rate in Figure 2 is 20Msps using a 4x oversampled Cosine filter response with a 3dB bandwidth of 14MHz followed by a 7^{th} order Butterworth filter with 20MHz 3dB bandwidth. Notice the excessive eye closure and overshoot generated by not considering the DAC sin(x)/x response and anti-alias filters transition band requirements. Additionally, the response type of the anti-aliasing filter requires attention. For example, all the 20Msps eye patterns below in Figure 3 use the same 8x oversampled digital shaping filter that takes the DAC sin(x)/x response and anti-alias filter oversampling requirements into account. Each of the anti-alias filters are 7^{th} order responses with 40MHz 3dB bandwidths. The eye patterns were generated from randomized data over 200 Monte Carlo runs using ideal components for the anti-alias filters. Real filters would have limited quality factors and tolerances that would only degrade the eye patterns from the ideal responses shown. The quality factors and tolerances were purposely left out of the simulations because the main point of the simulations is to show the various levels of eye pattern degradation caused by the different anti-alias filter response choices, not the effects of component limitations.

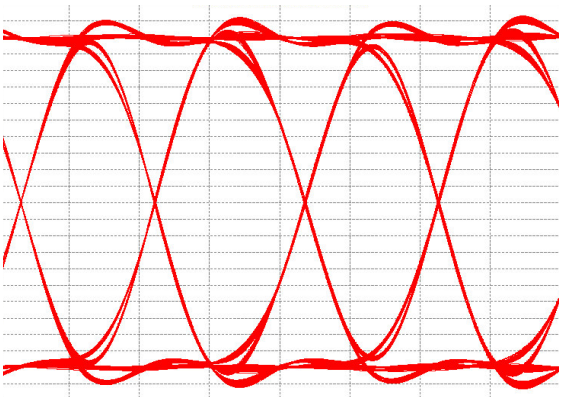

Figure 2: 4x Oversampling with Butterworth Anti-Alias Filter

The Bessel filter shows a clean eye pattern with minimal (~2.5%) closure and inter-symbol interference, but the stopband attenuation of the DAC images is not adequate. The Chebyshev filter has 0.5dB passband ripple that displays good attenuation of the DAC images, but the poor group delay causes noticeable inter-symbol interference and eye closure of about 7%. The Butterworth filter response attenuates the images sufficiently and has minimal inter-symbol interference, but still shows approximately 6% eye pattern distortion. Clearly, what is needed is a filter response that addresses both the time domain and frequency domain requirements simultaneously.

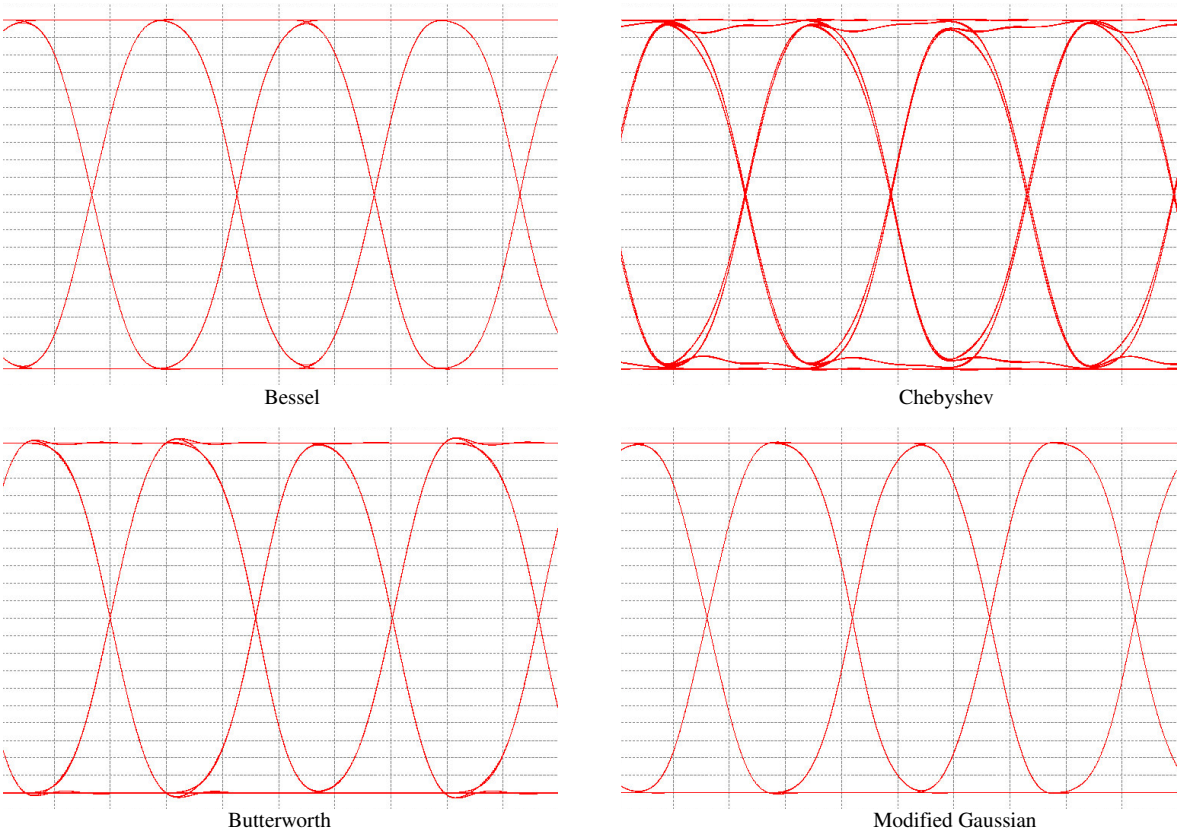

Figure 3: Eye Pattern Distortion vs. Anti-Alias Filter Response

The last example filter is the modified Gaussian filter. This filter exhibits the advantages of the Bessel filter having minimal (~2%) eye closure and inter-symbol interference while also attenuating the DAC images greater than 65dB. The Gaussian filter is similar to the Bessel filter, in that the passband group delay is flat and the attenuation is gradual out to 2x to 3x the serial data rate, but was modified to add stopband zeros to better attenuate the DAC images.

After designing the nominal composite filter response, the analog components finite quality factors and tolerances need to be considered. The nominal analog anti-alias filter response can then be compensated for by adjusting the digital shaping filters response if required. If a nonsymmetrical impulse response is utilized, both the non-ideal amplitude and group delay characteristics of the analog filter can be corrected.

CONCLUSIONS

The need for variable bit rate telemetry encoders are driven from different, but harmonious customer and manufacturer needs such as mission format flexibility and reduced response time to changing customer requirements. These basic needs then place specific requirements on the functionality of the encoder that can be implemented in several possible manners each with specific advantages and disadvantages relating all the way back to the sensor fidelity and out to the encoder's filtered premodulation output. Specific examples stressed the importance of minimizing sampling clock jitter to maintain signal fidelity and considering the composite response of the premodulation filtering to minimize eye pattern distortion of the serial data output feeding an FM transmitter.

Implementation tradeoffs continually change as devices with more capability come to market. The recent introduction of yet lower power, higher density field programmable gate arrays (FPGAs) may warrant further investigation into continuously variable interpolation (CVI) techniques for bridging clock domain boundaries between the analog sensors ADC sampling and PCM data rate as well as the analog boundary between the encoder's filtered premodulation output and the FM modulation input of the transmitter. The benefits relating to utilizing one fixed high rate system clock may now favor CVI methods for new encoder developments.

REFERENCES

Brannon, Brad, "Aperture Uncertainty and ADC System Performance," AN-501, Analog Devices, Norwood, MA 02062-9106, November 6, 1998

harris, fred, "FPGA Interpolators Using Polynomial Filters," Proceedings of: The 8th International Conference on Signal Processing Applications and Technology, Toronto Canada, September 13-16 1998.

Telemetry Group, Range Commanders Council, "Document 106-05 Part I: Telemetry Standards," Secretariat, Range Commanders Council, White Sands Missile Range, New Mexico, 88002, July 2005