IRIG-106 CHAPTER 10 RECORDER WITH BUILT-IN DATA FILTERING MECHANISM

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ABSTRACT

Sixteen years ago, RCC added Chapter 8 to the IRIG-106 standard for the acquisition of 100% MIL-STD-1553 data from up to eight buses for recording and/or transmission. In the past 5 years, the RCC recording committee added Chapter 10 to the IRIG-106 standard for acquisition of 100% data from PCM, MIL-STD-1553 busses, Video, ARINC-429, Ethernet, IEEE-1394, and others. IRIG-106 Chapter 10 recorder suppliers have further developed customer-specific interfaces to meet additional customer needs. These needs have included unique radar and avionic bus interfaces such as F-16 Fibre Channel, F-35 Fibre Channel, F-22 FOTR, and others. IRIG-106 Chapter 8 and Chapter 10 have provided major challenges to the user community when the acquired avionics bus data included data that must be filtered and never leave the test platform via TM or recording media. The preferred method of filtering data to ensure that it is never recorded or transmitted is to do so at the interface level with the avionic busses.

This paper describes the data filtering used on the F-22 Program for the MIL-STD-1553 buses and the FOTR bus as part of the IRIG-106 Chapter 10 Multiplexer/Recorder System. This filtering method blocks selected data at the interface level prior to being transferred over the system bus to the media(s). Additionally, the paper describes the configuration method for defining the data to be blocked and the report generated in order to allow for a second party to verify proper programming of the system.

KEY WORDS

Recorder, IRIG-106 Chapter 10, Data Filtering, MIL-STD-1553

INTRODUCTION

Two decades ago there was no standard method to acquire, transmit, and/or record 100% of all avionics bus data used on a test article. This was primarily due to transmission and recording bandwidth limitations. Few avionic busses had bandwidth that exceeded the 1 Mbps rate. Those platforms that used high data rate busses such as the Eurofighter with its STANAG 3910 and other platforms implemented unique proprietary solutions to acquire 100% of bus data. The first attempt to standardize the acquisition and recording of 100% avionic bus data was IRIG-106 Chapter 8. That standard dictated that each bus output its 100% data using up to four tracks for use with an analog track recorder, and output a composite PCM data from up to eight MIL-STD-1553 busses. Later that standard was revised to include 100% data from 64 or more ARINC-429 busses.

In the past few years a new recording standard has emerged to unify the recording format to allow data exchange among ranges, and to deal with the ever-expanding data rates of avionic and video found in modern aircraft. IRIG-106 Chapter 10 provided the recording standard to acquire and record vast amounts of data. This standard did a great job in defining the recording format of many common data types found in most test platforms. However, the application of the standard by various manufacturers fell short in recognizing several user-community needs when the Chapter 10 multiplexer / recorder system is already tapping on avionic buses for data recording. The shortcomings included: 1) the inability to recognize the need to block the recording of selected data that should never leave the test platform, 2) the inability to use the multiplexer / recorder system as a potential platform to TM selected avionics bus data - this topic is treated in [TBD], 3) the inability to use the Multiplexer / recorder system as a data acquisition system among other sensor instrumentation units, which has been shown to be effective in system applications [refer to TBD], and 4) the inability to allow the user to use an off the shelf recording media [refer to TBD].

This paper will concentrate on the first industry shortcoming referenced above; i.e. the inability to block selected avionics bus data sources at the interface level in order to prevent that data from leaving the test platform via recording media and / or TM.

BACKGROUND

The IRIG-106 Chapter 10 recording standard defines the recording media format and packet data format of incoming data sources for recording. The recorder is assumed to record 100% of all incoming data. For various reasons the data owner may wish to block certain selected bus data from leaving the test platform. This possibility was not conceived during the definition phase of the Chapter 10 standard. Some users allow the recording of all aircraft bus data, followed by post flight data filtering as described in [1]. This method was applied only to PCM and 1553 and cannot be applied across-the-board to all unique busses. Most importantly, this method requires the consent of the data owner to remove the required blocked data from the aircraft. The best approach in blocking selected avionics bus data is to do so at the interface level using hardware state machines to remove the desired data. This can be done well before any Chapter 10 packet encapsulation is done as well as before any data forwarding to the onboard processors for recording occurs.

We will review the filtering approaches for MIL-STD-1553 buses and for a unique F-22 avionics bus called FOTR. The latter bus is a 400 MHz fiber optic bus carrying multiple types of packet data formats. We will also review the user setup for filtering data from both busses.

MIL-STD-1553 DATA FILTERING

The acquisition of MIL-STD-1553 bus data is implemented using four or eight channels per card. An IRIG-106 Chapter 10 multiplexer using a 64-bit 66MHz [Processor? Backplane? TBD]with a modified compact PCI bus hosts the card. For the purpose of this discussion, we will concentrate on the four-channel card. Incoming bus data passes through front-end transformers (two per bus) and a receiver section (one per bus) to a Virtex2 Xilinx FPGA. The FPGA receives time data directly from the backplane, interfaces to a PCI bridge via a local bus operating at 32-bit 66MHx, and uses an 80MHz clock for various operations. The FPGA is designed to monitor four MIL-STD-1553 buses, validate bus words and messages, provide time tag, generate a status word, format data packets into channel FIFO, and manage local bus descriptors for forwarding the data to the multiplexer's processor for recording. The data filtering mechanism was placed in the receiving front-end of the word / message data tracker for each bus.

Per Channel Filter Recourses

The filter mechanism uses a Dual Port BlockRAM of 512 x 32-bit organized as 256 x 64-bit wide, a two 16-bit wide target register to hold one or two 1553 command words, comparator logic of 32-bit wide, and a Finite State Machine Controller (FSMC) with some glue logic to control the filter process.

1553 Filter Operation

A software driver initializes the BlockRAM with user configuration data. This includes data to be blocked identified by the first command word for non RT-to-RT messages or by both command words for RT-to-RT messages, and messages to be tagged for telemetry purposes directly from the IRIG-106 multiplexer unit. Bus message tracker logic detects the arrival of 1553 command word(s) and places the word(s) in the target register(s). The Finite State Machine Controller (FSMC) performs sequential search through the 256 addresses of the BlockRAM at a rate of 1/80 MHz per address. The 32-bit comparator logic searches for command word(s) matches between the holding register and the BlockRAM contents. The FSMC returns the discard and tag bits. The glue logic inhibits flagged discard 1553 messages from ingress to data buffers. Refer to figure 1 for the 1553 filter block diagram.

The FSMC, BlockRAM and comparator logic operate at 80MHz rate. The worst-case search to find a match or give-up for no match is 256 cycles, this equals to 256 x 1/80MHz = 3.2 uS. Once the message tracker identifies the message command word(s), the filter mechanism makes a determination to discard (block) the message within 3.2 uS , and before any 1553 data word is assembled to be written to local buffers.

The filter mechanism is duplicated four times in the FPGA for each 1553 channel. The user setup is done through TTC software called TTCWare. This software supports the configuration of distributed data acquisition systems and Chapter 10 multiplexer and recording systems.

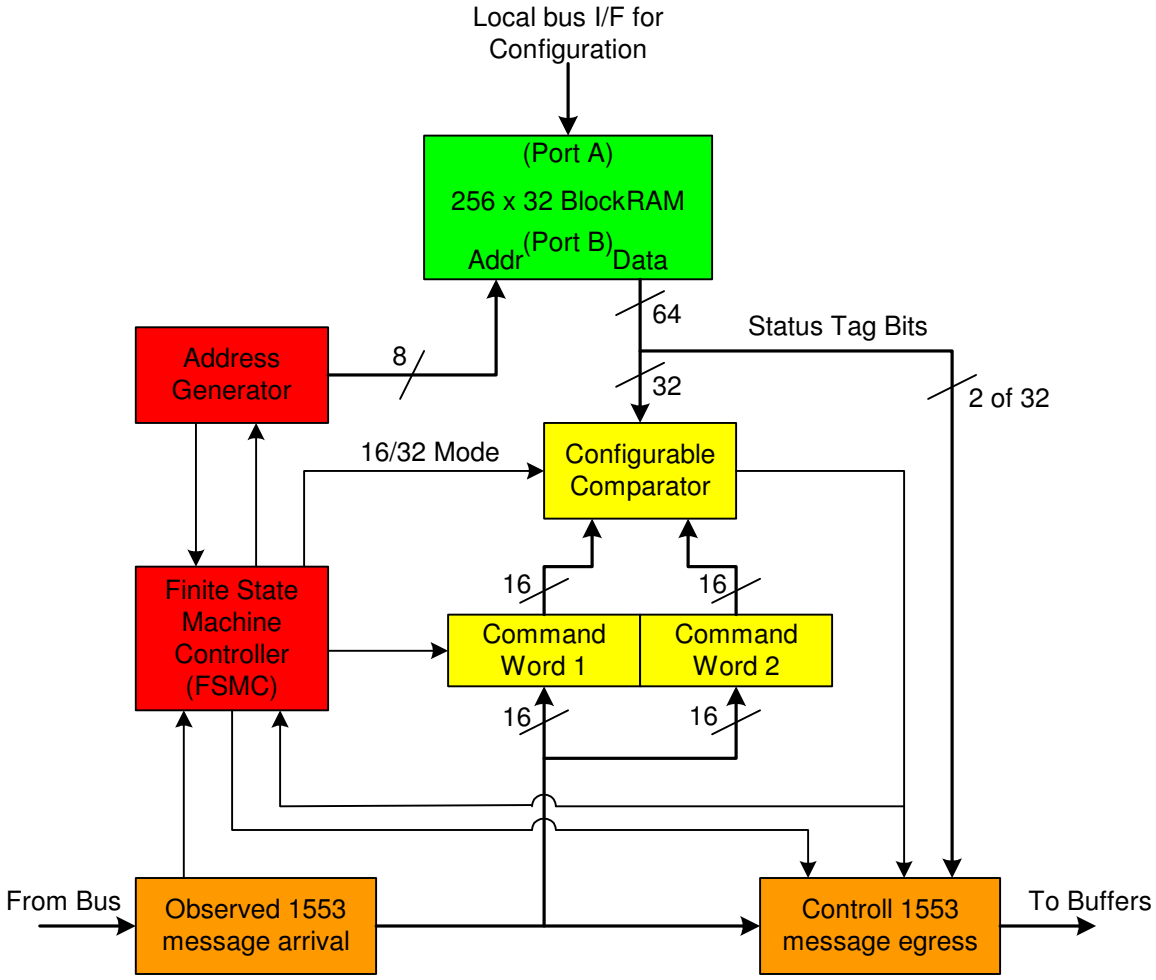


Figure 1. 1553 Filter Block Diagram

1553 Filter Software Configuration

Figure 2 shows the user graphical interface for configuring those messages to be filtered (deleted) or to be marked for transmission. Each bus can be programmed to select up to 256 messages. A filtered message is removed from recording by the FPGA receiving circuit. Criteria for message selection for deletion is the message command word or both command words in the case of RT-to-RT. In some cases, the user may use the "Two Man Rule" to verify and sign the filter configuration report as shown in figure 3. If actual configuration verification is required, the user may query the multiplexer for the filter information, or in extreme cases, they may simulate 1553 data and verify that indeed the programmed information is being filtered.

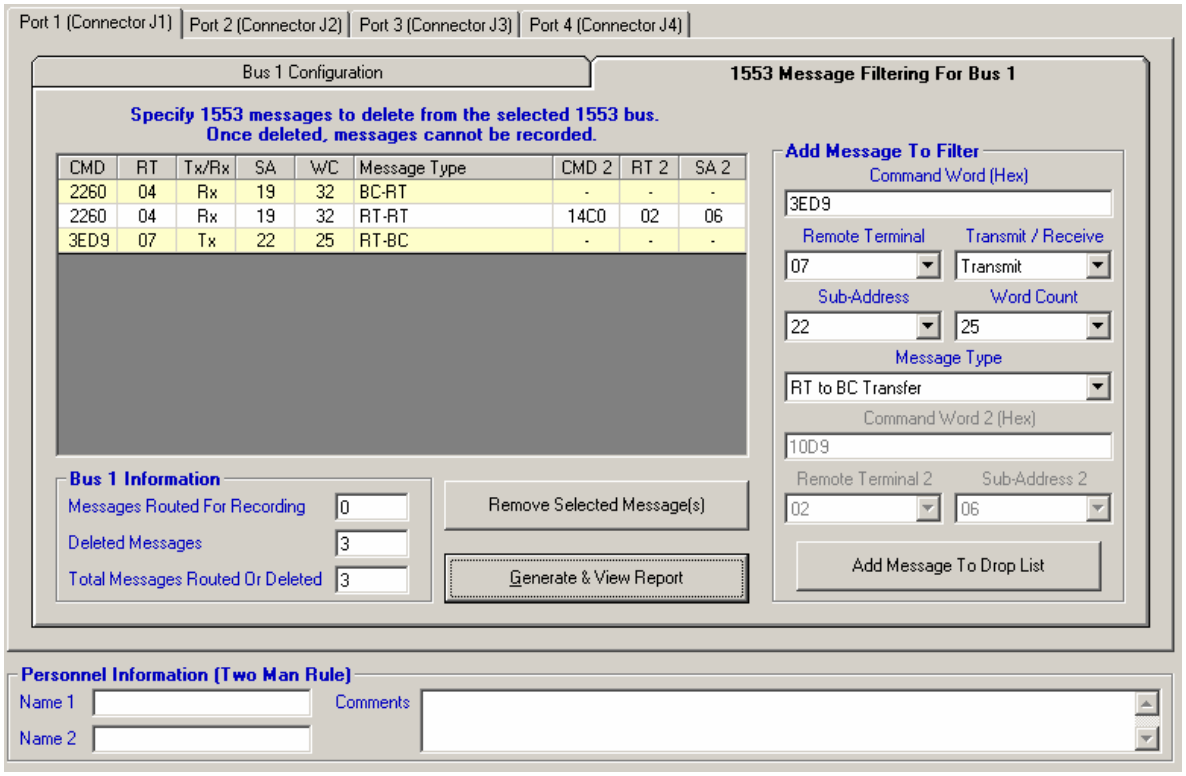
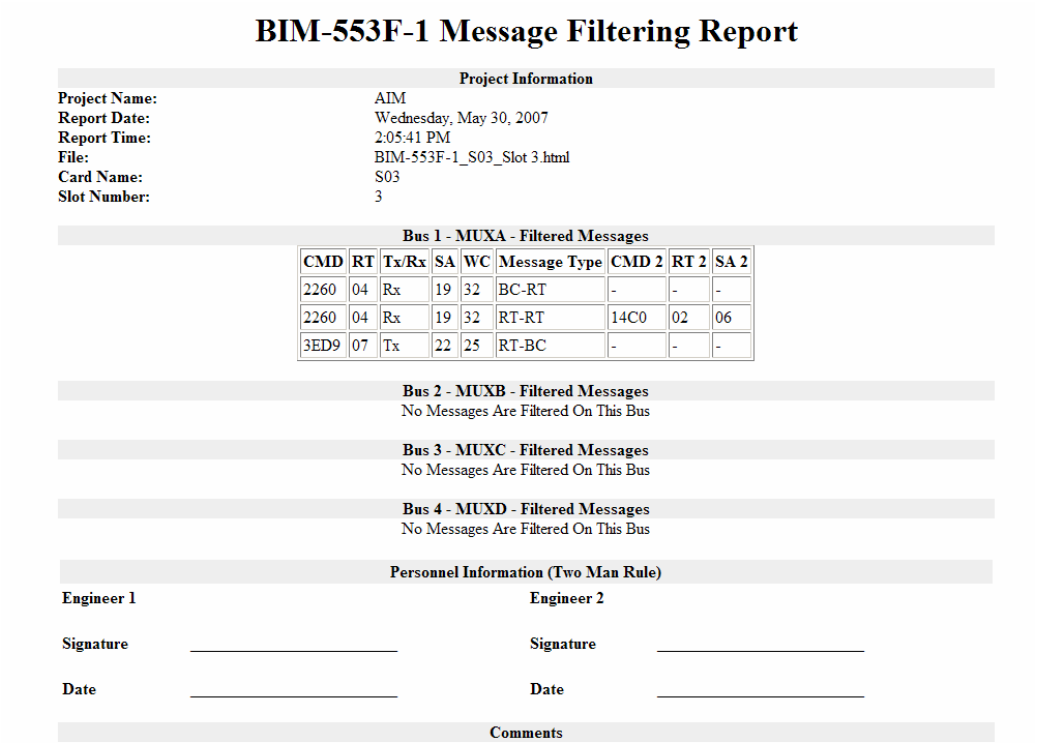


Figure 2. 1553 Filter Configuration



BIM-553F-1 Message Filtering Report

Project Information

Project Name: AIM
Report Date: Wednesday, May 30, 2007
Report Time: 2:05:41 PM
File: BIM-553F-1_S03_Slot 3.html
Card Name: S03
Slot Number: 3

Bus 1 - MUXA - Filtered Messages

CMD	RT	Tx/Rx	SA	WC	Message Type	CMD 2	RT 2	SA 2
2260	04	Rx	19	32	BC-RT	-	-	-
2260	04	Rx	19	32	RT-RT	14C0	02	06
3ED9	07	Tx	22	25	RT-BC	-	-	-

Bus 2 - MUXB - Filtered Messages
No Messages Are Filtered On This Bus

Bus 3 - MUXC - Filtered Messages
No Messages Are Filtered On This Bus

Bus 4 - MUXD - Filtered Messages
No Messages Are Filtered On This Bus

Personnel Information (Two Man Rule)

Engineer 1 **Engineer 2**

Signature _____ **Signature** _____

Date _____ **Date** _____

Comments

Figure 3. 1553 Filter Configuration Report

F-22 FOTR DATA FILTERING

The acquisition of Fiber Optic FOTR bus data is implemented using two channels per card. An IRIG-106 Chapter 10 multiplexer using a 64-bit 66MHz modified PCI Backplane. The card operates in "receive mode only" to acquire several data types from the bus. Encapsulation of the FOTR data into the Chapter 10 data packets and the various data types available over the FOTR bus are beyond the scope of this paper and will not be discussed here.

Incoming fiber optic bus data passes through a front-end MCM (Multi-Chip Module) receiver device to a Spartan 3E Xilinx FPGA. The main functions of this FPGA are Local Bus Control, Packet/Message Buffer Control and RX Packet/Message Processing Engine. The FPGA receiver circuit diagram is shown in figure 4.

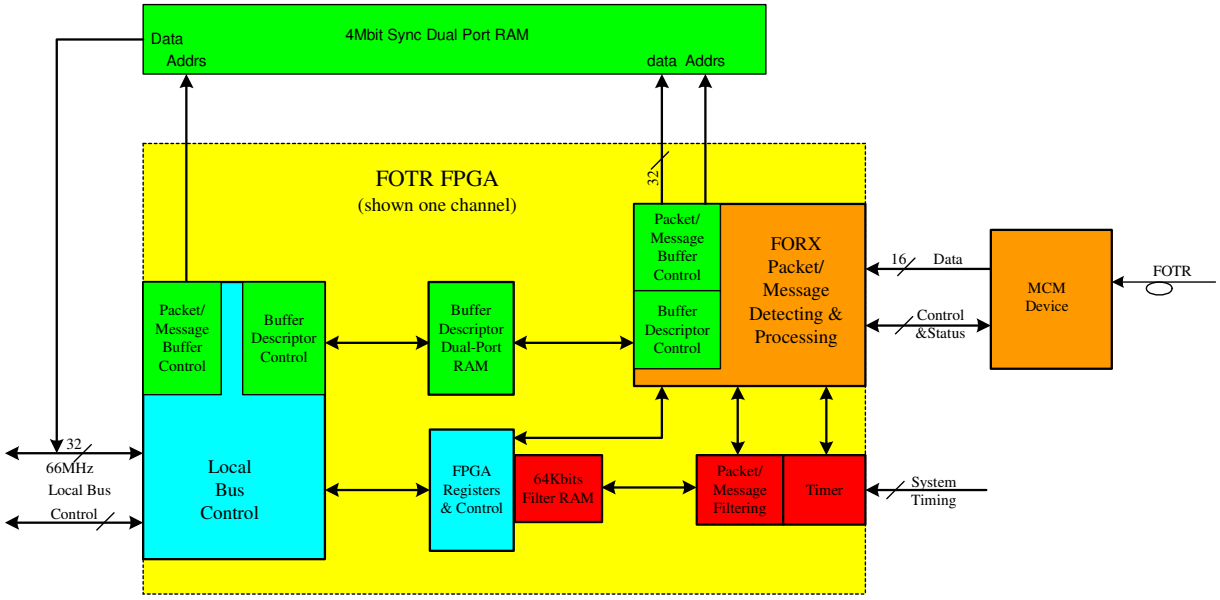


Figure 4. FOTR Receiver Diagram

FOTR Filter Operation

Refer to figure 5 for the FOTR Filter Operation Flowchart. At the start of incoming packet/messages, the Filtering Word Block identifies the filtering word (16-bit) to be used as the address into the filtering memory (64Kx1). The data from the filtering memory at the next clock cycle will make the filtering decision. If the filtering memory data bit is 1, the current packet/message is accepted. Otherwise, the current packet/message should be filtered and the Filtering Block would interrupt the Packet/Message Detecting & Processing Block and the Packet Buffer Control Block. When the interrupt occurs, the Packet/Message Detecting & Processing restarts its packet/message detection machine and the Packet Buffer Control Block

stops writing the current packet/message data words to the packet buffer and resets its data write pointer to the maintained current Chapter 10 intra-packet header.

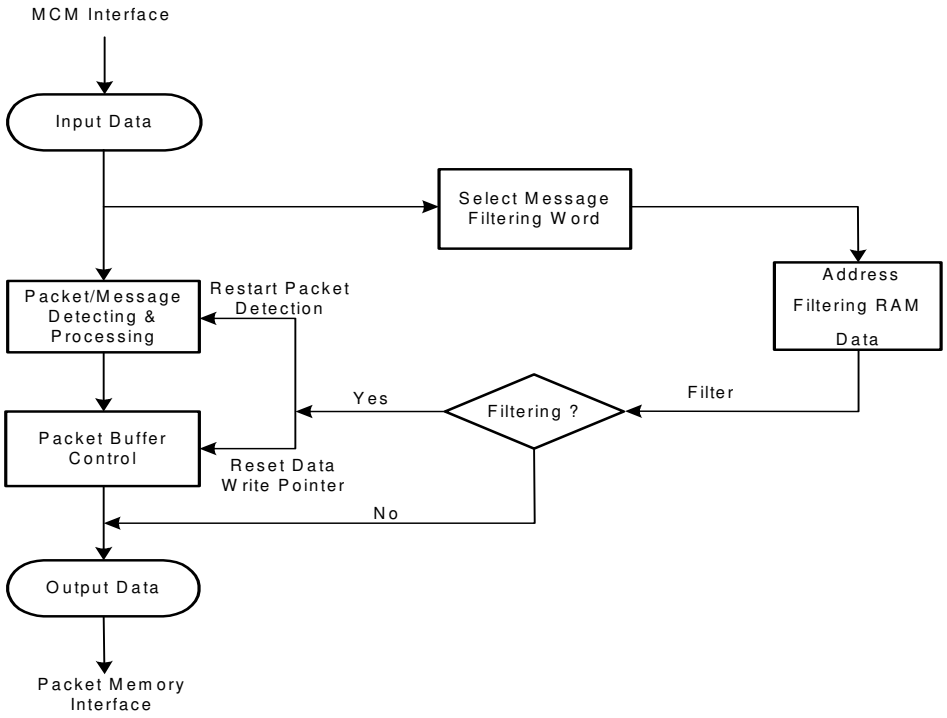


Figure 5. FOTR Filter Operation Flowchart

FOTR Filter Software Configuration

Filter configuration for the FOTR is done in a similar manner to the MIL-STD-1553 Bus. For this bus, there are up to 64K labels for filtering, which are set using a graphical user interface by specifying a label or range of labels. Filtered messages are removed from recording by the FPGA receiving circuit. The criteria for message selection for deletion is based on the message label and offset location of the label within the message. The “Two Man Rule” can be used similar to the 1553 bus filtering.

Conclusions

IRIG-106 Chapter 10 recording standard provided the user community with the tools to format and record all incoming bulk avionics data available to the multiplexer / recorder unit(s). This paper showed a bus application design that allows the user to filter and block selected data as close as possible to the bus interface.

REFERENCES

[1] Dennis Manning, Rick Williams, Paul Ferrill, "Data Filtering Unit (DFU) …", Proceedings of the 42nd Annual International Telemetry Conference (ITC/USA 2006), USA, October 23-26, 2006.

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[3] Albert Berdugo, " Design of a Gigabit Data Acquisition and Multiplexer System", Proceedings of the 39th Annual International Telemetry Conference (ITC/USA 2003), USA, October 21-23, 2003.