

A VERY HIGH SPEED HARD DECISION SEQUENTIAL DECODER

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Summary There are numerous applications for high data rate coding systems for earth orbiting space-missions with power limited links. Studies indicated that a 40 Mbps hard decision sequential decoder would best meet the requirements. A prototype decoder has been designed and fabricated using the fastest commercially available digital integrated circuits, MECL III. Thus far, an internal computational rate of 70 Million computations per second has been achieved. Computational efficiency of the decoding algorithm was greatly improved by incorporating two modifications to the Fano algorithm; “double quick threshold loosening” and “diagonal steps.” Preliminary results indicate that an output error rate of 10^{-5} can be achieved with E_b/N_o less than 5.4 dB at data rates up to 40 Mbps. At lower data rates, even less signal energy is required. This decoder is believed to be at least 5 times faster than any previous sequential decoder.

Introduction The trade-off studies which preceded the development for a 40 Mbps hard decision sequential decoder have been reviewed in detail elsewhere ^{1,2}. Basically, the results indicated that the choice was between Viterbi decoding of a constraint length 7 convolutional code, and sequential decoding of long constraint convolutional codes, assuming a coding bandwidth expansion factor of two was permissible. Since both systems have similar performance efficiency at a bit error probability of 10^{-5} , the decision to implement a sequential decoder was based primarily on its ability to achieve error rates down to 10^{-8} with relatively little additional signal power, compared to Viterbi decoding. Soft decision sequential decoding was ruled out because the required logic complexity precludes operation at 40 Mbps.

Appropriate applications of high data rate coding systems are for earth orbiting space missions with power limited links. For applications in which a Tracking and Data Relay Satellite (TDRS) system ^{3,4} will be used in place of direct to ground transmission of data, the communication link from the orbiting satellite to the relay satellite may be power

limited. The communications link at K-band from the TDRS to a central ground station is not considered to be power limited even at high data rates. Earth survey type spacecraft carry imaging instruments which generate data in the tens of megabits per second. For example, on ERTS A ⁵, one instrument, the Multispectral Scanner, images earth scenes with 24 apertures, resulting in a 15 Mbps data rate. Advanced ERTS missions are expected to have even higher data rate requirements. The ERTS A 15 Mbps link has a substantial power margin ⁶ with both 30' and 85' ground antenna stations for meeting a 10^{-5} bit error probability requirement, without coding. However, such S-or K-band links are power limited when transmitting through a TDRS; thus systems with sequential decoding can use the power saving.

Another application, and also the original motivation for the study and subsequent development of a high data rate coding system, was for potential use in the Space Station/Base program. The shuttle-launched space station's external ground communication link can be either directed through the Manned Space Flight S-band network stations or by a TDRS system using K-band. For the Space Station concept ⁷, the total data volume, assuming time division multiplexing of all digital data and a digital TV link with moderate data compression, requires a link of less than 40 Mbps capability. Thus, it is clear the 40 Mbps decoder can meet the requirements of several link applications, particularly when the TDRS System is used.

Hardware Description The 40 Mbps sequential decoder employs a rate 1/2, systematic convolutional code of constraint length 41 or 33. The code used has the generator 715, 473, 701, 317, 46, expressed in octal digits. The decoder may be used with both BPSK and QPSK modems. The decoder is completely self-synchronizing and provides for resolution of the 90° phase ambiguities in QPSK modems.

Differential encoding and decoding may be used to resolve 180° modem ambiguities. The differential encoder/decoder may be located between the data source/sink and the convolutional encoder/sequential decoder since the code used is transparent to 180° phase changes. The usual differential decoding penalty is thereby avoided since isolated errors at the decoder output are virtually non-existent.

The decoder was implemented using a modification of the Fano algorithm ⁸. Briefly, the operation of the Fano algorithm is as follows. Starting at the first node in the code tree, a path is traced through the tree by moving ahead one node at a time. At each node encountered, the decoder evaluates a branch metric for each branch stemming from that node. The branch metric is a function of the transition probabilities between the received symbols and the transmitted symbols along the hypothesized branch.

The decoder will initially choose the branch with the largest metric value (corresponding to the closest fit to the received symbols). The metric is then added to a path metric,

which is the running sum of branch metrics along the path presently being followed. Along with the path metric, the decoder keeps track of the running threshold T . As long as the path metric keeps increasing, the decoder assumes it is on the right track and keeps moving forward, raising T to lie within a fixed constant, A , below the path metric. If, on the other hand, the path metric decreases at a particular node, such that it becomes less than T , the decoder assumes it may have made a mistake and backs up. It will then systematically search nodes at which the path metric is greater than T until it finds a path that starts increasing again, or until it exhausts all nodes lying above T . Eventually it will find a path that appears to have an increasing path metric.

Eventually, the decoder will penetrate sufficiently deep into the tree that with high probability the first few branches followed are correct, and will not be returned to by the decoder in a backward search. At this point, the information bits corresponding to these branches can be considered decoded and the decoder may erase received data pertaining to these branches.

The decoder was implemented as a syndrome decoder in order to permit specialization of the large main buffer memory. A block diagram of the decoder is shown in Fig. 1. The syndrome is formed by passing the received information bits through a replica of the encoder. The generated check bits are exclusive-ORed with the received check bits. The resulting syndrome contains all information necessary for the sequential decoder to determine the information bit error sequence. The syndromes are stored via one port of a 65,000 bit, two-port random access memory (RAM). The decoding logic is connected to the second port. The RAM is implemented using the AMS 6002, 1024 bit MOS memory chip. The memory buffer registers and control logic are implemented using TTL logic.

The received information bits are delayed by a 65,000 bit MOS shift register. The delayed information bits are exclusive-ORed with the output of the syndrome sequential decoder, which is the information bit error sequence, resulting in the corrected information sequence.

These large buffers are necessary because the number of computations to decode an information bit is a random variable. The RAM is provided to store received syndromes until they can be decoded. The buffer memory is provided with refresh circuitry to insure against data loss, even at very low data rates. Provision is made for reducing the memory size down to 1000 bits in order to reduce the decoding delay in low data rate applications.

The performance of the sequential decoder is primarily determined by two parameters: the buffer memory size and the speed advantage of the decoding logic (the ratio of computation rate to the data rate). The decoding logic was implemented using the fastest commercially available logic family, MECL III, in all speed critical parts of the decoding

logic. MECL 10,000 series logic was used in less critical parts of the decoding logic. Approximately 100 MECL III I.C.'s and 185 MECL 10,000 I.C.'s were used in the decoding logic. The design goal for the decoder was a computation cycle time of 10 ns. Thus far, a cycle time of 14 ns has been achieved.

The MECL III circuits are all contained on one 64 square inch seven layer printed circuit board. Three of the layers are power planes. The other four contain the signal interconnections. The planes and the signal layers were interleaved and line widths controlled so as to maintain a 50 ohm transmission line environment. All signal lines were terminated with 50 ohm resistors. The layout of the board was of critical importance in achieving the desired cycle time. Approximately 7 ns of delay is contributed by the logic circuits. The layout generates delay at the rate of 1 ns per 5-6 inches of wire length. There are four levels of gating between flip flops requiring five levels of interconnection. Each level of wiring may require several inches in length. Thus, even with great care in layout, several nanoseconds of delay will result.

The MECL 10,000 portion of the decoding logic was packaged using a welded stitch wiring technique. All interconnections were terminated using 100 ohm resistors which provided a good impedance match for this type of wiring. The layout was not as critical here since only one level of logic was used between flip flops.

The tree searching capability of the decoder requires a fast buffer memory to store the results of previous computations. A 250 word, 2-bit per word RAM is provided. The RAM is implemented using the Advanced Memory Systems 0641 64-bit ECL memory chip. These devices have access times of 10 nano-seconds.

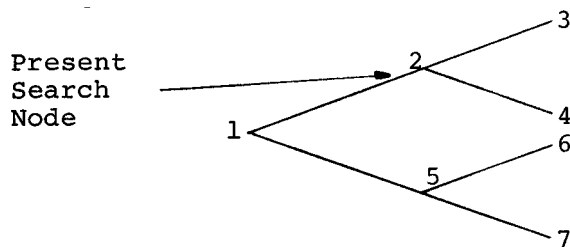
The sequential decoder is packaged in a 10-1/2" high rack-mountable chassis. A photograph of the decoder chassis is shown in Fig. 2. The decoder is contained on 19 circuit boards which plug into the backplane. The power supplies for the unit are mounted in a separate rack chassis. Cooling is provided by two large fans: one on the front panel and the other on the back panel. Small U-shaped metal fins were soldered to the studs of the MECL III devices to minimize their temperature rise.

Algorithm Modifications Previous studies have shown that sequential decoder performance may be improved by modifying the basic Fano algorithm ⁽¹⁾. The modifications are especially effective at very high data rates where the decoding logic speed advantage is small and where the decoder is operating below R_{comp} (E_b/N_o greater than 4.6 db for rate 1/2 codes with hard decisions). The 40 Mbps sequential decoder incorporates two of these modifications.

The first of these modifications is called "double quick threshold loosening" and has been described in detail previously ⁽¹⁾. This scheme greatly reduces the number of short

searches required. The decoder can decode past all single isolated errors and nearly all isolated pairs of errors without initiating a backsearch. The technique capitalizes on code structure and a particular choice of branch metrics and threshold spacing by permitting the threshold to be lowered twice without a backsearch if the present value of threshold was reached by tightening twice.

The second new modification is called “diagonal steps.” The technique of “diagonal steps” may be understood by considering the tree diagram below.



In the unmodified Fano algorithm, the decoder’s attention is restricted to nodes 1, 2, 3 and 4 if the present search node is at node 2. The decoder could step forward to either node 3 or 4 or step back to node 1. If nodes 3 and 4 are both below threshold but node 6 or 7 is above threshold, the decoder must first step back to node 1, then forward to node 5 and then forward to node 6 or 7 for a total of three steps. The diagonal step technique permits the decoder to go from node 2 to node 6 in only one step thus saving 2 computations. Furthermore, when moving forward, the modified algorithm always chooses the best node of 3, 4, 6, 7 to be searched first. If the branch of the tree stemming from node 6 is searched first but subsequently violates threshold, the decoder will return to node 5. Since the branches stemming from not yet been searched, the decoder can step 5 to node 3 instead of getting there by node 1. This special “move” also saves two above technique is effective on short best nodes are always searched first, thus searches. The technique is also effective on long back searches since two computations are saved every time the decoder returns to the forward mode from the backward mode, a very frequent occurrence.

During a deep backsearch, diagonal stepping nearly doubles the effective computation rate. Consider an exhaustive search of a very large binary tree. The unmodified Fano algorithm visits every node in the tree (except nodes at the ends) three times: once when arriving at a node for the first time, once when returning from the upper branch; and once when returning from the lower branch. Now consider the operation of the diagonal stepping algorithm assuming that the upper branches are visited first. Node 2 in the above diagram is visited once when arriving at this node for the first time and once when returning from node 4. Note that when returning from branches stemming from node 3 that node 2 is not visited as in the Fano algorithm. The branches stemming from node 4 are reached by a diagonal step from node 3. Thus, nodes on the upper branches of the tree are visited only twice.

Now consider node 5. Node 5 is visited only once; when returning from node 7. After branches stemming from node 2 have been searched, the nodes stemming from node 5 are searched by a diagonal step from node 2 to node 6. Nodes stemming from node 6 are then searched. When we return to node 6, we reach branches stemming from node 7 by a diagonal step from node 6. Finally, we visit node 5 when we return from node 7. Thus, all nodes on lower branches of the tree are visited only once. Thus, on the average, we visit each node in the tree 1-1/2 times as compared to three visits per node in the unmodified Fano algorithm.

Note that in actual sequential decoding, this factor of two improvement in computational efficiency is not fully realized. This is because at the ends of the tree where the decoder path metric is close to threshold, many of the lower branches are not visited by either the Fano algorithm or by the diagonal stepping algorithm. In effect, the binary tree is “pruned” by threshold violations and nodes at the ends of the tree that are visited at all are visited the same number of times by both the Fano algorithm and the diagonal stepping algorithm.

Results At the time this paper was written, the checkout of the sequential decoder was only just completed and only a few results were available. The test results are plotted in Fig. 3 as the signal-to-noise ratio necessary to obtain a 10^{-5} bit error rate versus data rate. Unfortunately, a high speed pseudo-random error generator was not yet available. These results were obtained by varying the decoder computation rate while holding the data rate constant at one megabit per second. The points were obtained by averaging over 2×10^8 bits. The operating speed of the decoding logic is presently 70 megacomputations per second. It is believed that this figure can be extended somewhat by “fine tuning” the circuit boards. The experimental results appear to be in agreement with simulation results previously obtained ⁽¹⁾.

Nearly all output errors were the result of buffer overflows. Whenever an overflow occurs at least the next 500 bits output from the decoder will contain errors at the channel error rate. Occasionally, overflow events last up to ten times as long depending upon the channel input error rate. The decoder provides an output signal whenever the decoder is in the overflow state so that these bits may be considered erased if desired.

Conclusions The successful development of this high speed sequential decoder prototype demonstrates that sequential decoding may be considered as a viable technique for very high data rate telemetry and communications systems where error rates of 10^{-5} and below are required. The very high internal operating speed of the decoder represents a factor of five increase in speed over any previous sequential decoder implementation known to the authors ⁹.

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References

1. LINKABIT Corporation, "Coding Systems Study for High Data Rate Telemetry Links (Final Report)," on Contract NAS2-6024 NASA Ames Research Center, Moffett Field, California, NASA CR-114278, 1971.
2. D. R. Lumb and A. J. Viterbi, "High Data Rate Coding for the Space Station Telemetry Links," International Telemetering Conference Proceedings, Volume VII, 1971, pp. 101-106.
3. Goddard Space Flight Center, "Tracking and Data Relay Satellite (TDRS) System Concept - Phase A Study Final Report," Volume 1 and 2, November 1969.
4. P. F. Barritt and E. J. Habib, "Tracking and Data Relay Satellite System: An Overview," AIAA 7th Annual Meeting and Technical Display, October 1970, Paper #70-1305.
5. M. Maxwell and J. Pandelides, "The Telecommunication System for the Earth Resources Technology Satellite (ERTS) A and B," National Telemetering Conference Convention Record, 1971, pp. 137-147.
6. General Electric, "Earth Resources Technology Satellite Spacecraft System Design Studies Final Report. Volume II, Subsystems Studies, Book 1 of 2, Refer to Section 4.4.1.4," prepared for Goddard Space Flight Center, CR-112499, Document No.-70SD4207, February 11, 1970.
7. North American Rockwell, Space Division, "Modular Space Station Phase B Extension, Preliminary System Design, Volume IV: Subsystems Analyses, Section 7.4," prepared for Manned Spacecraft Center under Contract NAS9-9953, January 1972.
8. J. M. Wozencraft and I. M. Jacobs, "Principles of Communication Engineering," John Wiley and Sons, Inc., New York, N. Y., 1965.
9. G. D. Forney, Jr. and E. K. Bower, "A High-Speed Sequential Decoder: Prototype Design and Test," IEEE Trans. on Communication Technology, Vo. COM-19, October 1971 (Pt. II) . 821-835.

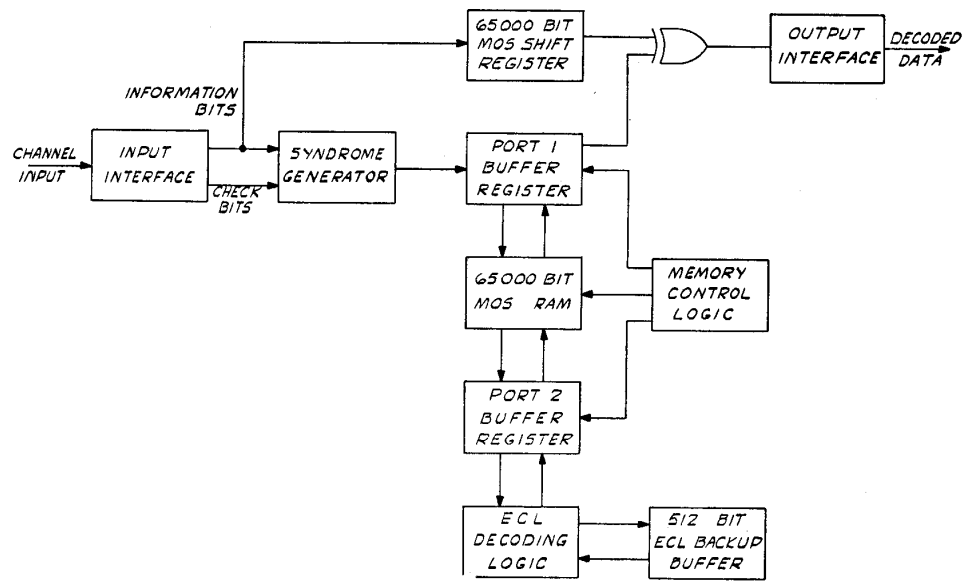


Figure 1. 40 Mbps Sequential Decoder Block Diagram.

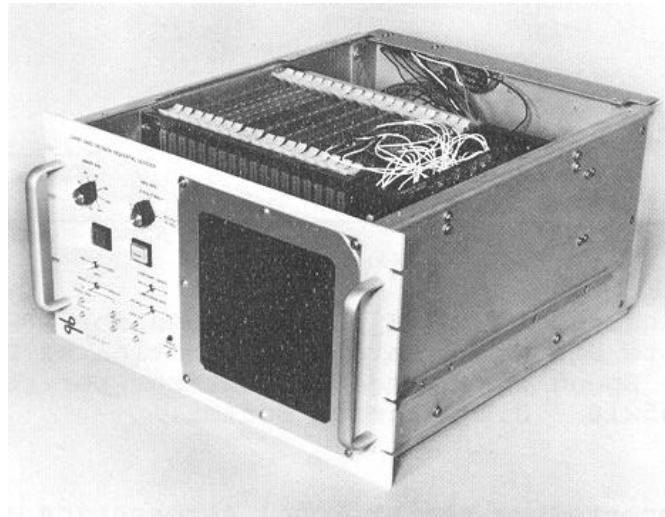


Figure 2. High Speed Sequential Decoder.

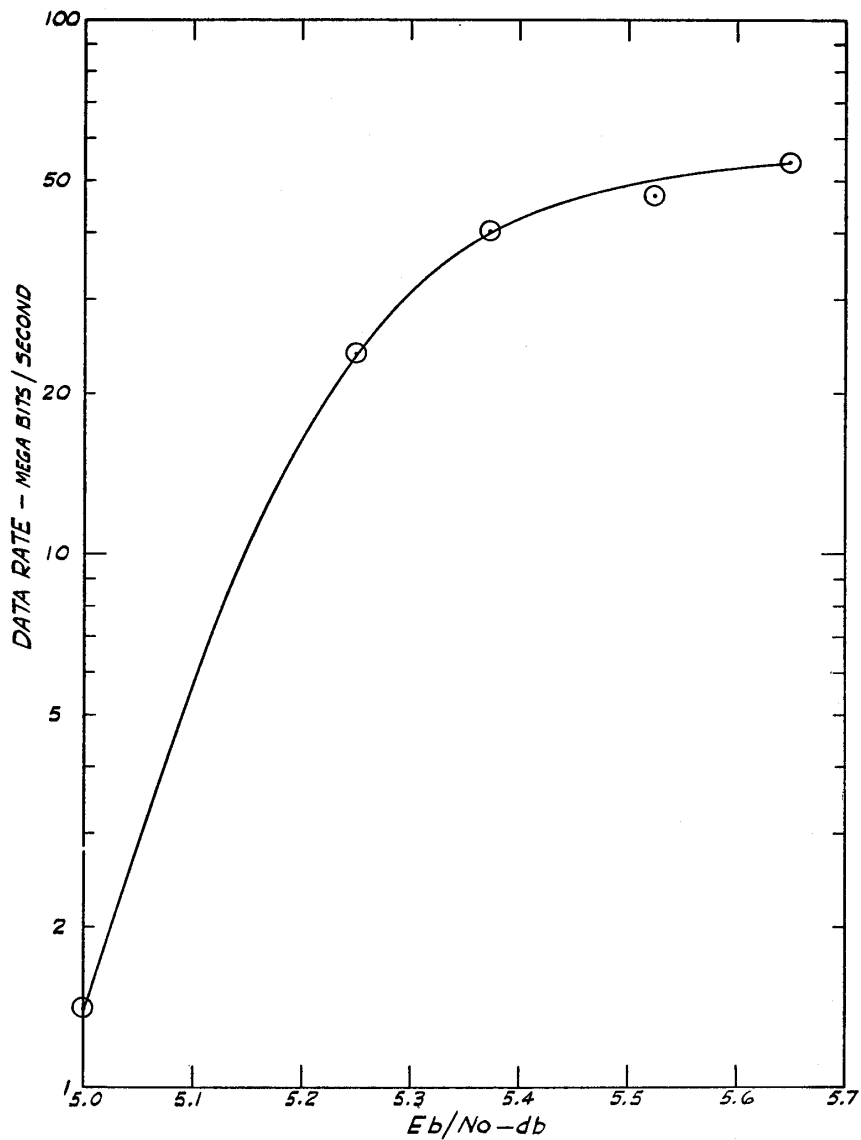


Figure 3. Preliminary Results. E_b/N_0 Required for 10^{-5} Composite Bit Error Rate as a Function of Data Rate. Decoder Speed is 70 Megacomputations per second, $K=41$, 65×10^3 Bit Syndrome Buffer.

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