INTRODUCTION

Alcatel Bell Space has offered since many years its versatile OMNISAT demodulator, which is able to handle data streams from a wide variety of Earth Observation Satellites (data coming from more than 30 satellites are currently demodulated with OMNISAT equipment all over the world). In order to expand the capabilities of the existing OMNISAT demodulator, Alcatel Bell Space (ABSp) has developed, in cooperation with ESA, a new earth observation data acquisition system: the Alcatel 9910 OMNISAT.

The new product integrates signal processing functions of a complete receive chain (from RF signal to the decoded bit-stream) into one single and modular equipment. The functionality is split over an X-Band Downconverter (XDBC), a High Data Rate Demodulator (HDRD) and a Data Ingest and Front End Processing function (DIFEP). A High Data Rate Test Modulator (HDRM) provides loop-back test functionality. It is compatible with the current generation OMNISAT and can be used as direct replacement for it.

![OMNISAT chassis with opened keyboard drawer](image)

Figure 1: OMNISAT chassis with opened keyboard drawer

Up to 4 Demodulator boards HDRD can be housed in the same crate, for the parallel receiving of multiple downlinks. On the same manner, up to 2 Data Ingest and Front End Processing functions DIFEP can be housed in one crate.
The equipment is able to process signals with a bit rate up to 500 Mbit/s; it is delivered either with pre-configured missions characteristics for which Alcatel gives support, or customer configurable for any number of missions.

The functionality is hosted into a COTS industrial PC platform, in order to provide a cheaper, reconfigurable equipment as a core building block of present and future acquisition facilities. This new OMNISAT architecture permits a significant reduction both in investment and ownership cost, compared with the previous generation.

This paper describes the architecture of the OMNISAT equipment, which is based on the latest System On Programmable Chip (SOPC) technology.

Thanks to the modular architecture of the OMNISAT, the product can target the low-end market (minimum configuration, e.g. only a demodulator function) as well as the high-end market (a full-blown OMNISAT, e.g. with conversion of a signal from RF frequency to a decoded bit stream, or multiple demodulators in one single unit). This makes the Alcatel 9910 OMNISAT product a very powerful solution for all data acquisition facilities.

Figure 2 shows a block diagram of a typical OMNISAT equipment configuration. The architectural design of the individual functional building blocks of the OMNISAT equipment is presented hereafter.

Figure 2: a typical Alcatel 9910 OMNISAT configuration
HIGH DATA RATE DEMODULATOR (HDRD)

The HDRD is a demodulator that consists of single PCI board, which contains all the analogue and digital circuitry. The main function of the HDRD is to receive a digitally modulated IF signal and to deliver at his output the digitally demodulated (and decoded) data.

The HDRD can cope with a variety of modulation schemes: BPSK, QPSK, OQPSK, Unbalanced QPSK and Asynchronous QPSK; 8PSK is on the roadmap. The maximum symbol rate of the IF signal is limited to 250 Msym/s (that is 250 Mbit/s BPSK, 500 Mbit/s QPSK, 750 Mbit/s 8PSK).

The HDRD IF input frequency is selectable in the range from 70 MHz to 850 MHz (typical values are 375 MHz, 720 MHz, 750 MHz). The demodulator achieves very fast carrier frequency acquisition (acquisition time < 400 ms) by employing FFT-based frequency estimation algorithms.
The HDRD analogue front-end performs optional IF filtering, gain adjustment and complex (I,Q) downconversion to zero IF. The complex baseband signal is then low pass filtered and sampled by two analogue to digital converters.

The remaining part of the demodulator functionality is implemented in programmable digital hardware, and is split over two Field Programmable Gate Arrays (FPGA).

The largest FPGA is a high speed device from the Altera Stratix family, which hosts the high speed digital hardware blocks (digital integrate and dump filters, timing error detectors, carrier phase/frequency error detectors, differential decoders, Viterbi decoder).

The second FPGA is an Altera Excalibur device which contains an embedded ARM processor core. The embedded software that runs on the ARM typically performs the lower rate digital demodulation functions. These functions are: Fast Fourier Transform (FFT) aided acquisition of the true carrier frequency, loop filtering of the timing error signals and the phase error signal, Automatic Gain Control (AGC) loop filtering, lock detection, signal quality estimation (e.g. Es/No) and low-level monitor and control functions.

A PCI interface chip on the HDRD board allows the communication between the host computer PCI bus and the digital hardware on the demodulator board.
The HDRD has two digital data outputs (ECL) and two corresponding clock outputs which are directly accessible from the back panel of the equipment. In order to support a variety of extra digital output requirements, a dedicated Digital Output Board is developed. This board is internally connected to the HDRD such that a maximum of 8 HDRD digital outputs can be provided (differential data + clock for data1, data2 or merged data 1+2). Additionally, this dedicated output board provides alternative electrical interfaces such as LVDS, RS422, TTL, and an Optical interface.

X-BAND DOWNCONVERTER (XBDC)

The X-band Down Converter converts the RF 8.0 to 8.4 GHz input band to a fixed IF frequency of 720 MHz. The IF output of the XBDC is internally connected to one of the two IF inputs of the HDRD.

Figure 5: Down Converter board

The XBDC physically consists of an external RF band-pass filter and a shielded module, containing the following functionality: power supply filtering, the RF input chain, LO and reference generation, the IF output chain and monitoring and control. A single downconversion stage is used for reasons of cost and implementation simplicity.

An XBDC module takes the place of two full size PCI boards.
HIGH DATA RATE MODULATOR (HDRM)

The HDRM is a modulator developed for testing purposes: it generates a digitally modulated IF signal that can be used in loop-back tests. Therefore the HDRM has two IF outputs, one is connected to one of the IF inputs of the HDRD (internal loop back), the other is connected to an N-type connector on the back panel of the equipment (for external loop-back tests).

![Figure 6 : Test Modulator board](image)

The HDRM supports the same modulation schemes as the HDRD, and the same range of IF frequencies.

The in-phase and quadrature test bit streams are either internally generated by Pseudo Random Pattern Generators, or taken from external data-clock inputs. In the baseline equipment, 4 ECL interfaces are provided on the HDRM board for the data and clock inputs of the external modulation data. A separate dedicated Digital Input Board (DIB) has been developed to support other electrical interfaces (LVDS, RS422, TTL, Optical) when needed. The HDRM modulator functions are located on a single PCI board containing all the analogue and digital hardware circuitry. The PCI bus interface allows the HDRM modulator functions to be monitored and controlled via the standard COTS computer.

The HDRM board also contains a fixed noise source of which the output can be added to the IF signal. This feature supports testing of signal to noise ratio conditions ranging from 0dB to 18 dB Es/No.

DATA INGEST AND FRONT-END PROCESSING

The Direct Ingest and Front-End Processing (DIFEP) are a high performance data acquisition and first-level processing system. It is highly configurable, supporting a wide range of missions. It includes the ingest boards, the associated software and the mission specific support packages (including level 0 processing).
The ingest boards receive data and clock from the High Data Rate Demodulator via external wiring, and host the frame synchronisation functionality of the receive chain. One ingest board is capable of handling the full bitrate for BPSK and QPSK, two ingest boards are needed in case of Asynchronous QPSK.

The mission specific software support packages includes frame synchronisation and decoding (frame synchronisation, derandomisation, deinterleaving, Reed-Solomon error detection and correction, CRC error detection, time tagging, quality annotation, decrypt, decompress) up to ISP / VCDU level depending to the concerned mission. A quicklook functionality is available.

The DIFEP software consists of a set of separate modules, each performing a specific task. Several modules may be linked together forming a complete processing chain, or run separately for stepwise processing. For multi-channel missions, several processing chains may run in parallel. The linkage between subsystems may be disk and/or IPC mechanisms, thus, providing a large number of processing combinations.

The hardware is designed for real-time ingest and processing of data, but it is also well suited for hardware accelerated offline processing of frame synchronisation, PRN descrambling, CRC checking and Reed-Solomon decoding.

The DIFEP may also be configured with output capabilities for testing and/or data retransmission purposes.

**FRONT-END PROCESSING OUTPUT BOARD**

The Alcatel 9910 OMNISAT can be equipped with one or two output boards that host playback functionality. These Front-End Processing output boards transform the stored data into a data+clock signal which can be fed to the input of the High Data Rate Modulator. In case of Asynchronous QPSK, two output boards are needed for full playback capacity.

**STORAGE OF ACQUIRED DATA**

For high-rate systems Wide-Ultra 320 SCSI 15k disks are well suited to insure the reception of all data during reception. In addition, Wide-Ultra 320 SCSI RAID controllers can be used to allow for striping to balance the data load on several disks (typically 2) and to increase the fault tolerance of the equipment.

For mid-rate systems, standard Wide-Ultra 160 10k SCSI disks with standard controllers are proposed; for low-rate systems, both SCSI and IDE disks can be used. In this case, the data can be stored on the system disk of the host computer.
OMNISAT HOST COMPUTER

The OMNISAT Host Computer is a 4U height, 14-slot rack-mount COTS Industrial PC with 6.4" LCD display, built-in slim keyboard and Touch Pad drawer. The chassis is depicted in Figure 7: Alcatel 9910 OMNISAT hardware. The PC’s backplane (PCI) hosts the processor board (an SBC - Single Board Computer) and the OMNISAT specific boards (HDRD, HDRM, DIFEP).

Up to 12 slots are available; examples of full configurations are given below:

- XBDC (2 slots) + HDRD (2 slots) + DOB + HDRM (2 slots) + DIB + DIFEP (2 slots), a complete receiving system for low cost configurations
- 4 HDRD + 4 DOB, four channels in parallel
- 2 DIFEP, two channels data ingest and front-end processing

The Single Board Computer is equipped with a Pentium 4 processor, contains 1 Gbyte RAM and supports a 64-bit / 66 MHz PCI bus. An on-board Ultra-320 SCSI controller allows the use of high speed storage. Optionally an external SCSI RAID controller can be used, depending upon the required performance. The board also contains a dual 10/100/1000Base-T Ethernet, BCM5703/5704 controller (64-bit PCI-X).
The SBC operating system is Linux, with RTAI real-time extensions to support high-speed interaction with the OMNISAT specific hardware. The performance of the Linux operating system is both processing and cost efficient, and is well proven in other ABSp products.

**Figure 8 : Software architecture**

The Single Board Computer hosts the OMNISAT monitoring and control software, which is socket based. This Software architecture allows several monitoring clients and one control client to connect to the system (via TCP/IP) at the same time. Clients can run either locally or remotely. Examples of clients are the GUI (a local client), the operational control centre or the RS232 interface.

**MONITORING & CONTROL**

The graphical user interface (GUI), provides a user-friendly interface to the monitoring and control software. It can run locally on the equipment, or remotely via Ethernet / TCP/IP, on any Linux, Unix, or Windows platform. IEEE488 and RS232 data link for Monitoring & Control is provided as well.

A scheduling function allows for the complete automation of system operations according to a spacecraft pass schedule over earth station.
CONCLUSIONS

Thanks to its modular design, the Alcatel 9910 OMNISAT is the ideal receiving equipment for all earth observations stations.

A variety of modulation/decoding schemes are supported, which allows for the reception of all types of signals; additionally, the Alcatel 9910 OMNISAT is capable of handling the storage of the processed data stream.

Thanks to its modular design, the OMNISAT product can target the low-end market segment by providing only a subset of its total functionality (e.g. only one demodulator function, converting a signal from IF frequency to a decoded bit stream), as well as the high-end market (a full-blown Alcatel 9910 OMNISAT, e.g. with conversion of a signal from RF frequency to a decoded bit stream, or multiple demodulators in one single unit). This makes the Alcatel 9910 OMNISAT product a very powerful solution for all data acquisition facilities.

The Alcatel 9910 OMNISAT is compatible with

- The existing OMNISAT equipment
- The existing earth observation satellites
- The future earth observation satellites

and is field-upgradable for any mission after installation.